S/M NO : SL26M1W001

Service Manual

LCD DVD Combo 26"

Model : DSL-26M1WC

Caution

: In this Manual, some parts can be changed for improving. their performance without notice in the parts list. So, if you need the latest parts information, please refer to PPL(Parts Price List)in Service Information Center.

DAEWOO ELECTRONICS

AUG.2007

DSL26M1WC SERVICE MANUAL

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PART 4: Detailed Circuit

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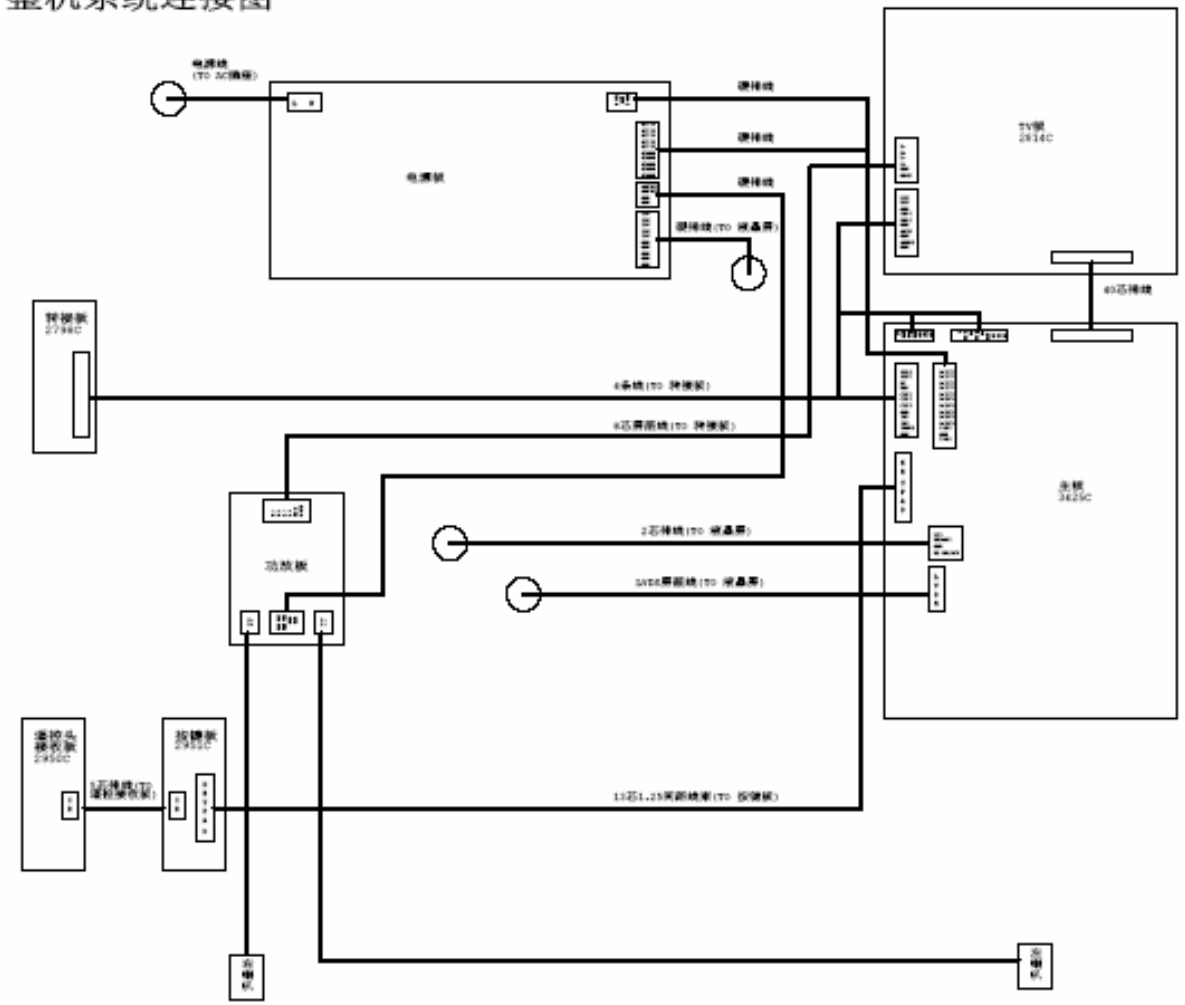
Part 1 Brief Introduction Of The DSL26M1TC

Schematic Diagram

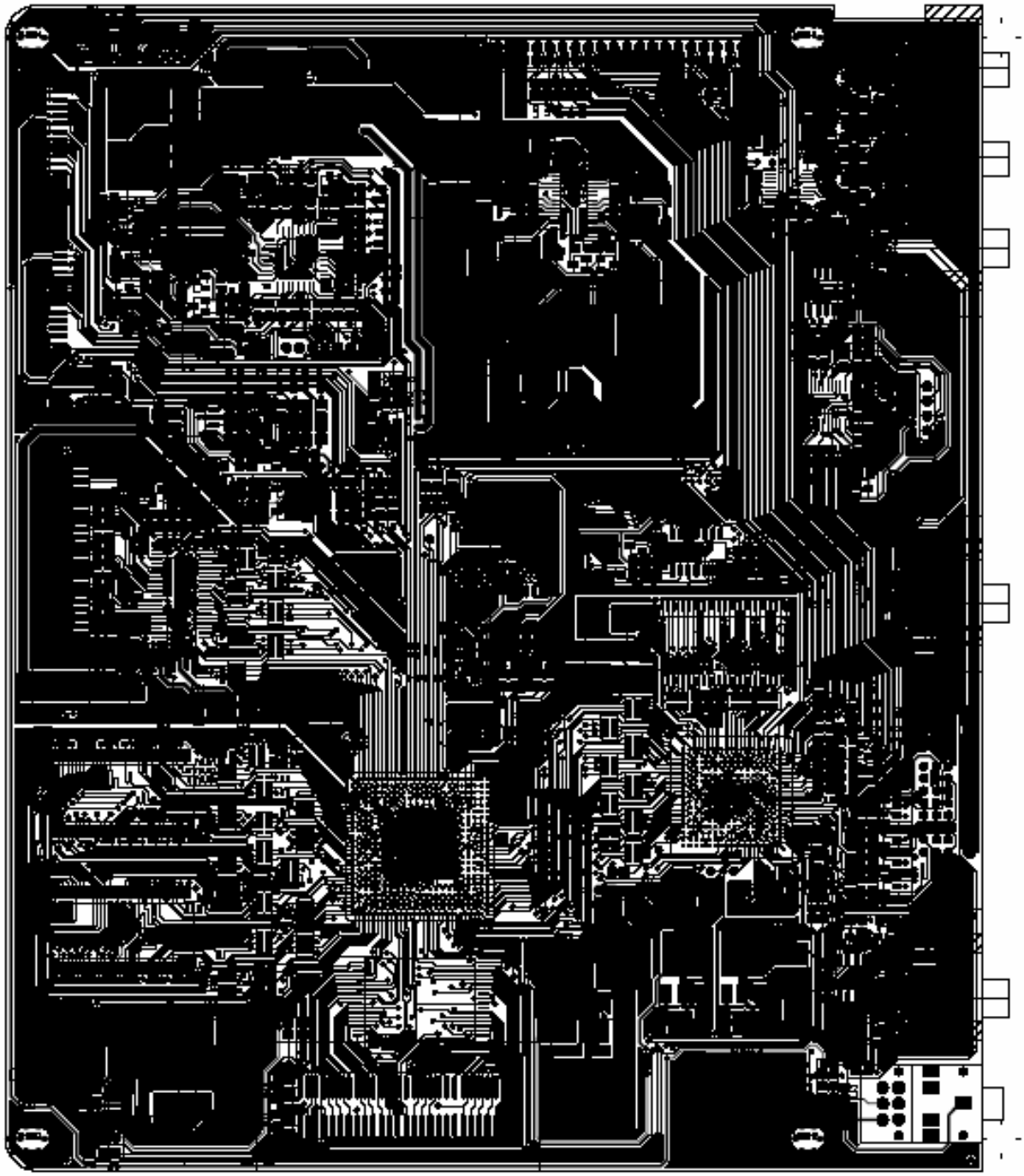
整机系统连接图



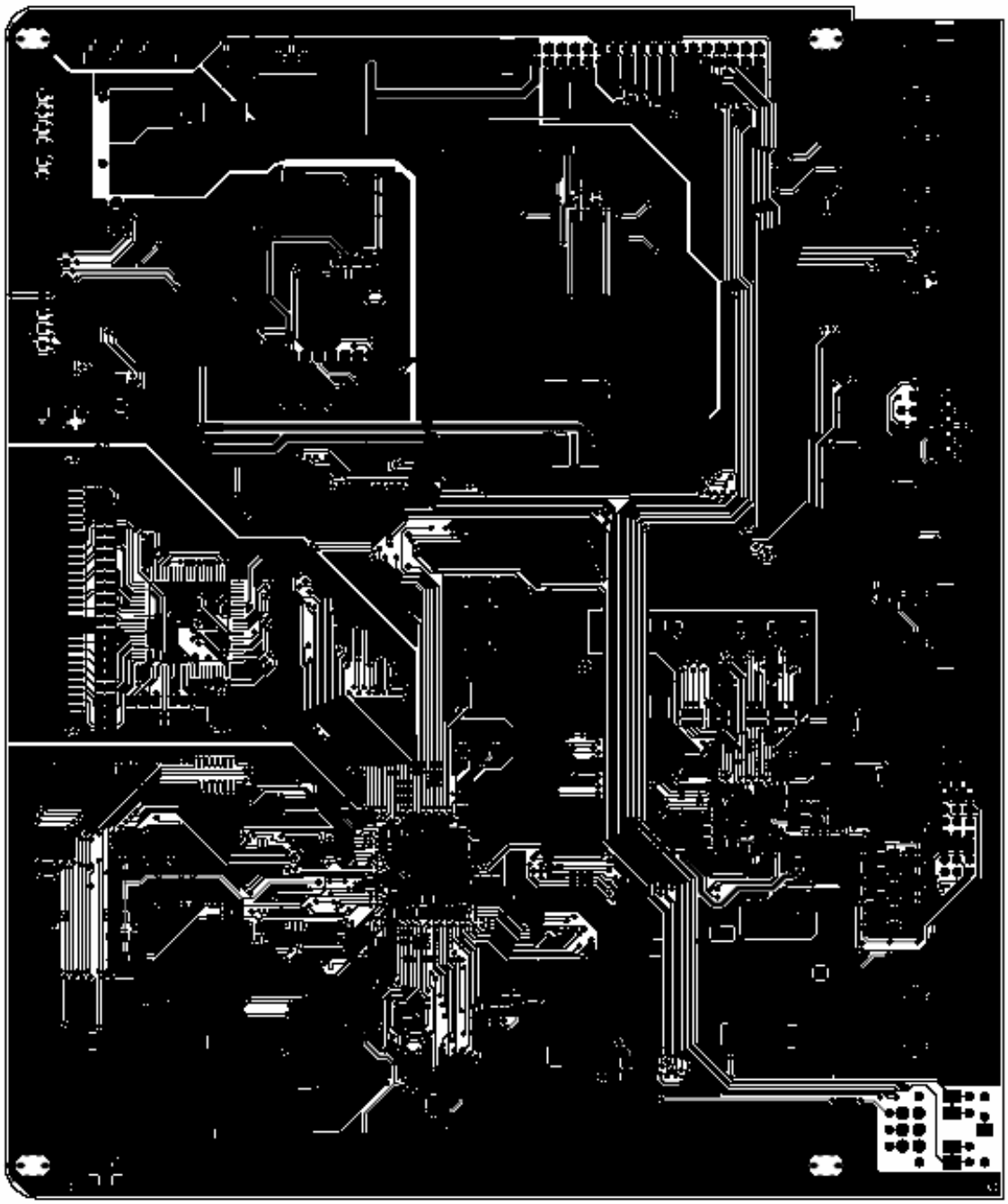
Printed Circuit

1. Main board

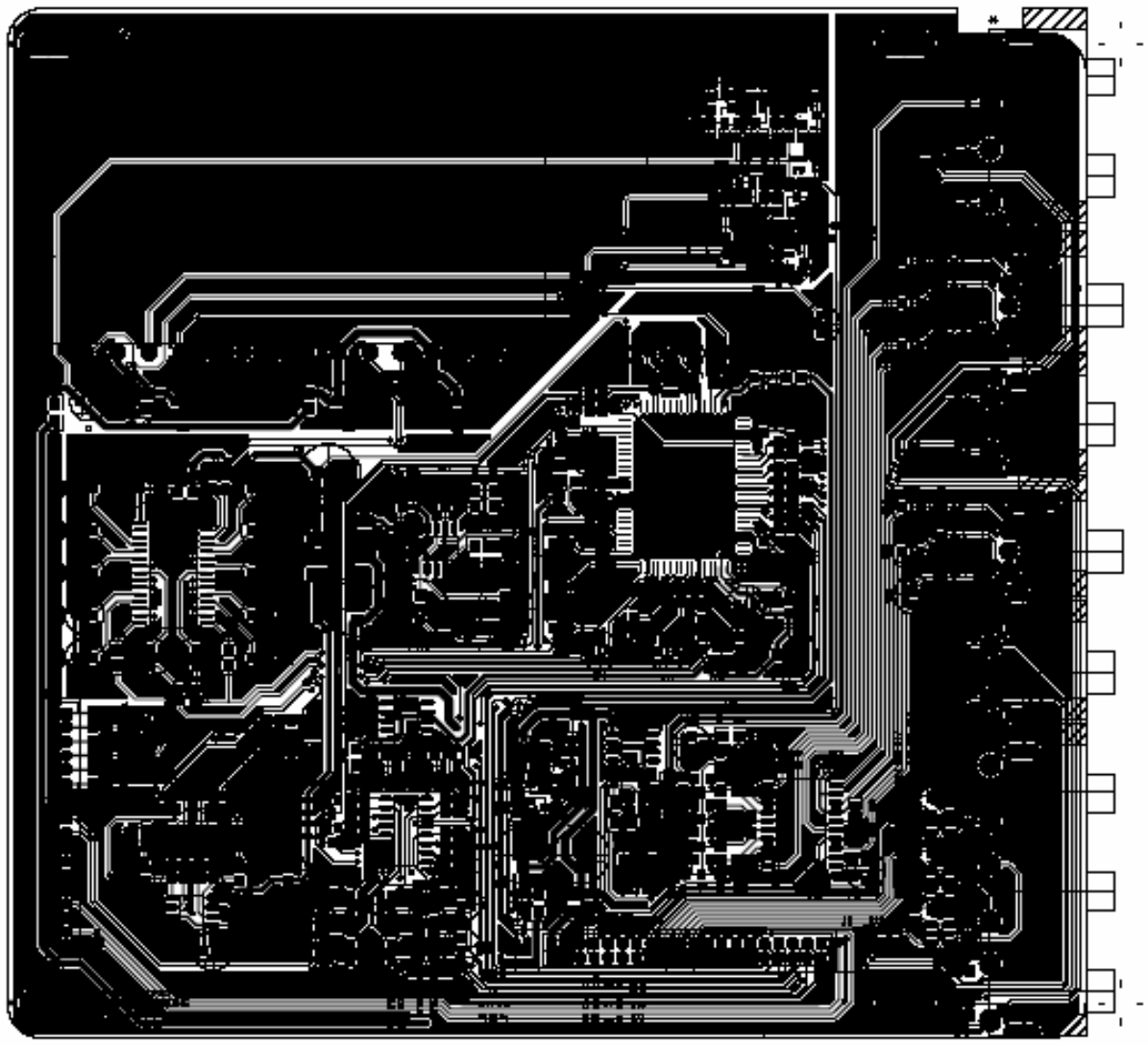
A: TOP LAYER



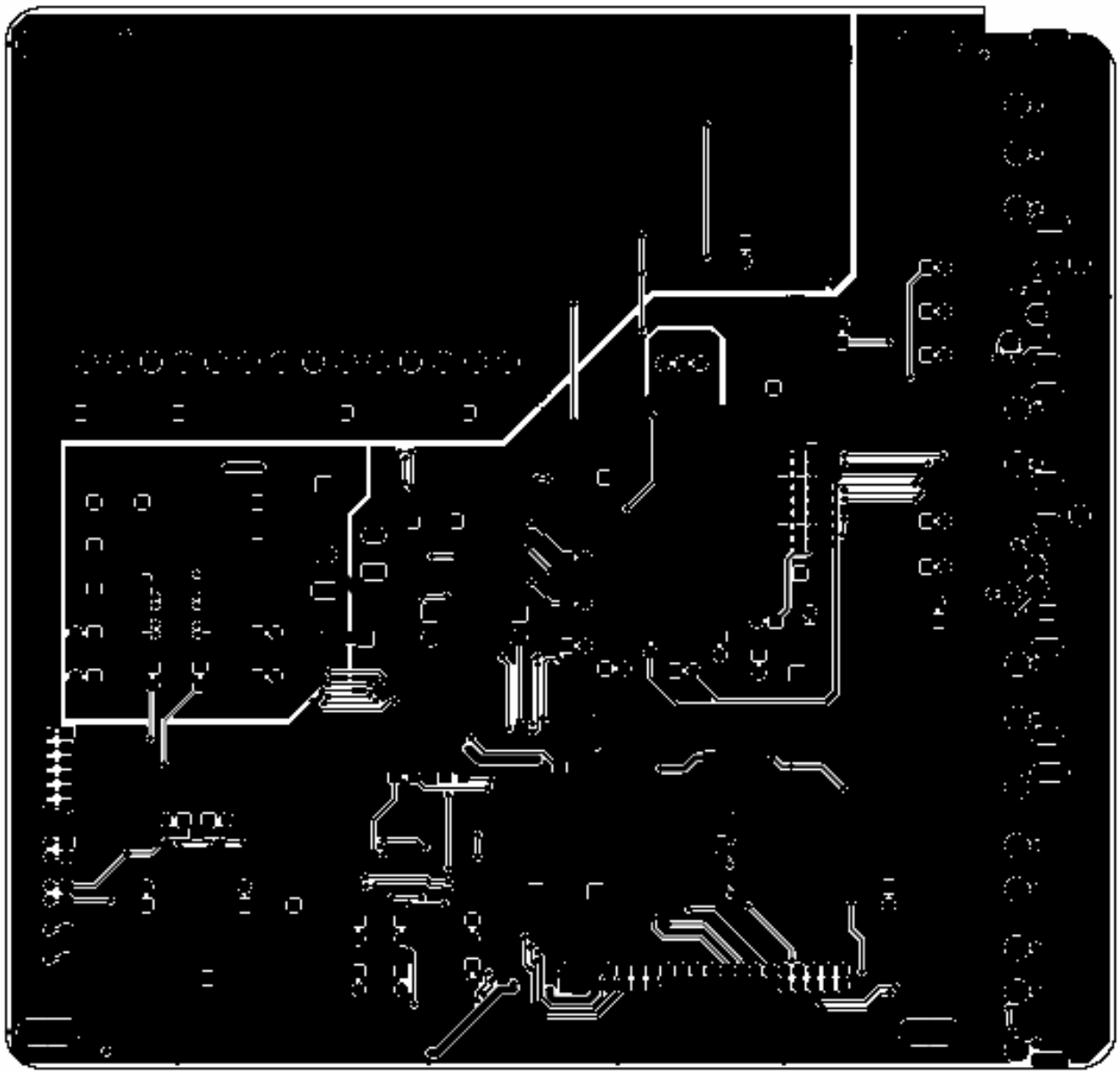
B: BOTTOM LAYER



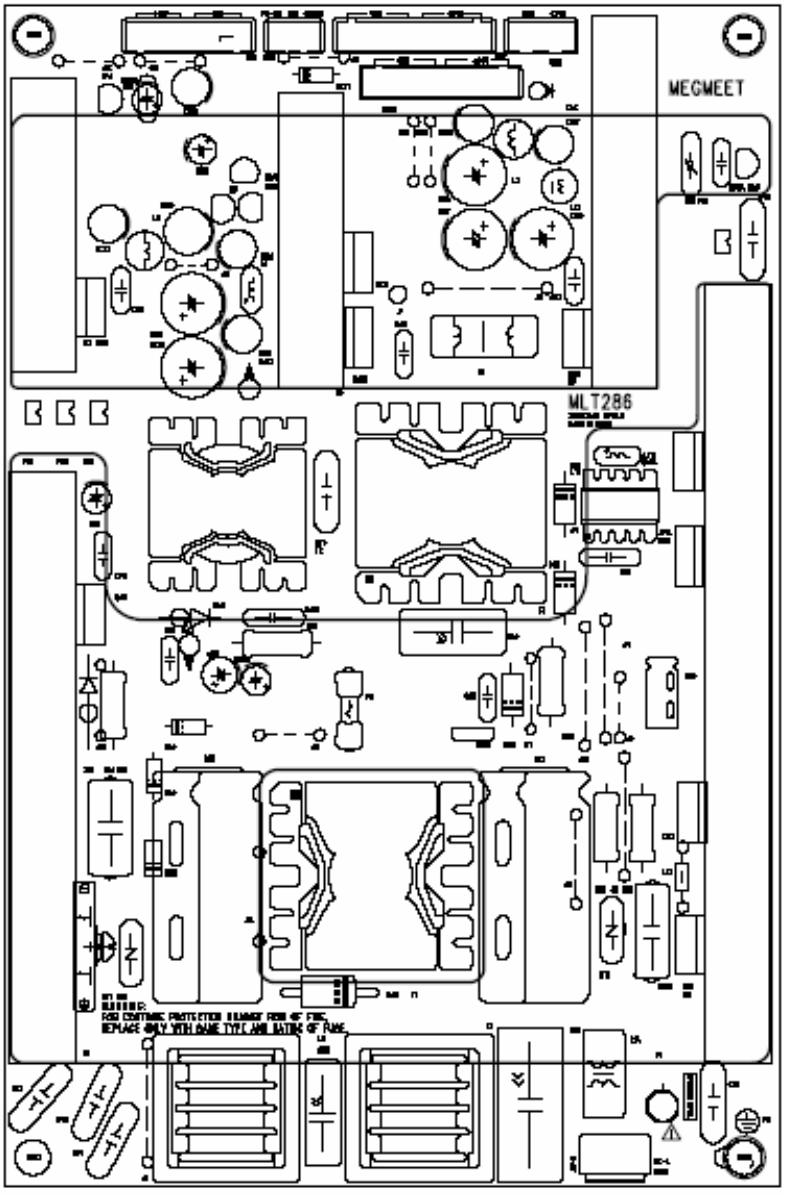
2. TV Board
A: TOP LAYER



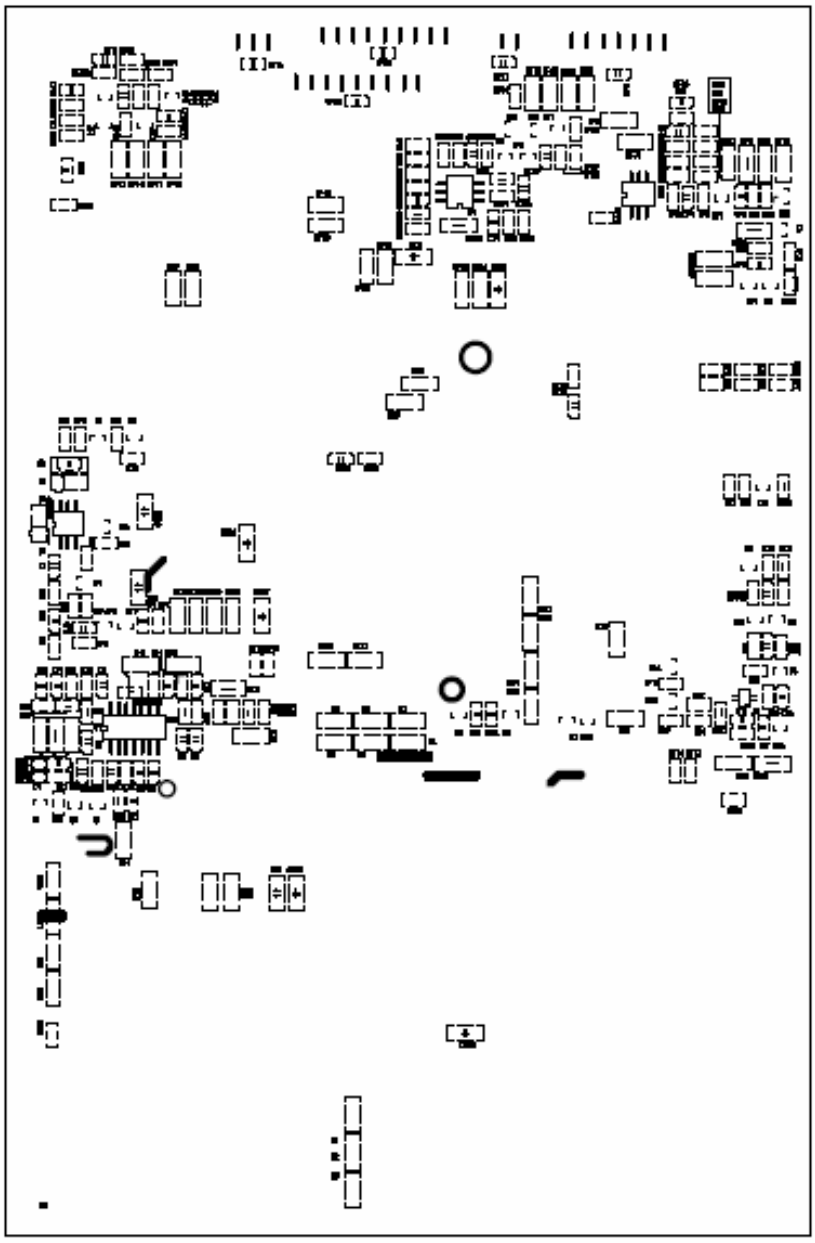
B: BOTTOM LAYER



3. Power board
A: TOP LAYER

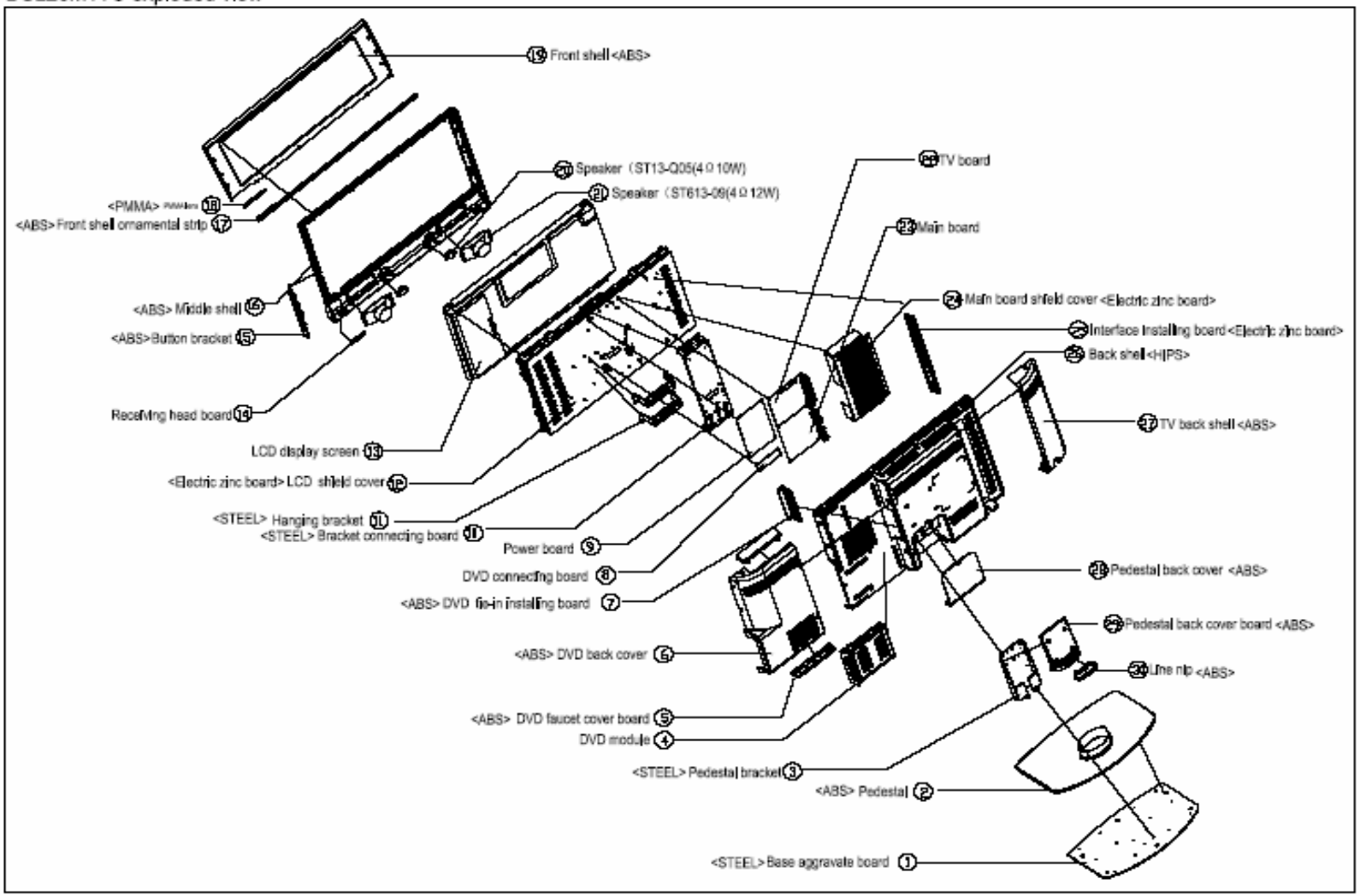


B: BOTTOM LAYER



Part 2 Exploded view

DSL26M1TC exploded view



Part 3 Key ICS And Assemblies

On Main Board			On rotate connecting board		
Serial No	Position	Type	Serial no	Position	Type
1	U8 U5	HYB25DC256160CE-5	1	U1	FSAV330
2	U23	S29AL016M90TEI	2	U2	74HCT4052
3	U3	PW118B-10	3	U3	L7808C-V
4	U13	HY57V161610ETP-7			
5	U24	THC63LVDM83R			
6	1U1	ATMEGA8L	On TV Board		
7	U4	24LC128A			
8	U6 U11	24LC21A	Serial no	Position	Type
9	U2	74LVC125	1	U1	L7809
10	U1	AP1084-1.8V	2	U6 U12	LM317L
11	U9	AP1084-2.5V	3	U8	CD4052
12	9U1	CM2006	4	U7	TEA6415CD
13	U17	AZ1117H-3.3	5	U13	NJM4558
14	U16	AZ1117H-1.8	6	U4	BH3547F
15	U10	IRF7314TR	7	U10	MSP3410G-QA-B8-V3
16	U7	FSAV330	8	U3	SN74AVC1T45
17	2U1	FAN5236MTC	9	5U1	NJW1147
18	2U3 2U4 2U5 2U6	FDS6680			
19	2U2	78L05			
20	U3	PW3300B-10			

ICS ON MAIN BOARD

1. 74LVC125A

FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard no. 8-1A
- Specified from –40 to +85 °C and –40 to +125 °C.

DESCRIPTION

The 74LVC125A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V.

The 74LVC125A consists of four non-inverting buffers/line drivers with 3-state outputs (nY) which are controlled by the output enable input ($n\overline{OE}$). A HIGH at $n\overline{OE}$ causes the outputs to assume a high-impedance OFF-state.

FUNCTION TABLE

See note 1.

INPUTS		OUTPUTS
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don't care;
   Z = high-impedance OFF-state.

PINNING

PIN	SYMBOL	DESCRIPTION
1, 4, 10, 13	$1\overline{OE}$ to $4\overline{OE}$	data enable input (active LOW)
2, 5, 9, 12	1A to 4A	data input
3, 6, 8, 11	1Y to 4Y	data output
7	GND	ground (0 V)
14	V_{CC}	supply voltage

2. CM2006

Features

- Includes ESD protection, level-shifting, buffering and sync impedance matching
- VESA VSIS Version 1 Revision 2 Compatible Interface
- Supports Optional NAVI Signalling requirements
- 7 channels of ESD protection for all VGA port connector pins meeting IEC-61000-4-2 Level 4 ESD requirements (±8kV contact discharge)
- Very low loading capacitance from ESD protection diodes on VIDEO lines, 3pF maximum
- Schmitt triggered input buffers for HSYNC and VSYNC lines
- Bi-directional level shifting N-channel FETs provided for DDC_CLK & DDC_DATA channels
- Backdrive protection on all lines
- Compact 16-lead QSOP package

Applications

- VGA and DVI-I ports in:
  - Monitors
  - Set Top Boxes

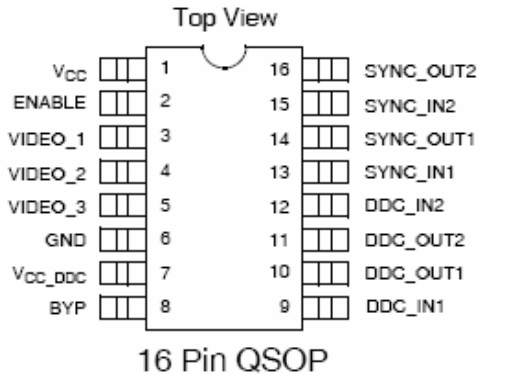
Product Description

The CM2006 connects between the VGA or DVI-I port connector and the internal analog or digital flat panel controller logic. The CM2006 incorporates ESD protection for all signals, level shifting for the DDC signals and buffering for the SYNC signals. ESD protection for the video, DDC and SYNC lines is implemented with low-capacitance current steering diodes.

All connector interface pins are designed to safely handle the high current spikes specified by IEC-61000-4-2 Level 4 (±8kV contact discharge). The ESD protection for the DDC, SYNC and VIDEO signal pins is designed to prevent "back current" when the device is powered down while connected to a video source that is powered up.

Separate positive supply rails are provided for the VIDEO / SYNC signals and DDC signals to facilitate interfacing with low voltage video controller ICs and microcontrollers to provide design flexibility in multi-supply-voltage environments.

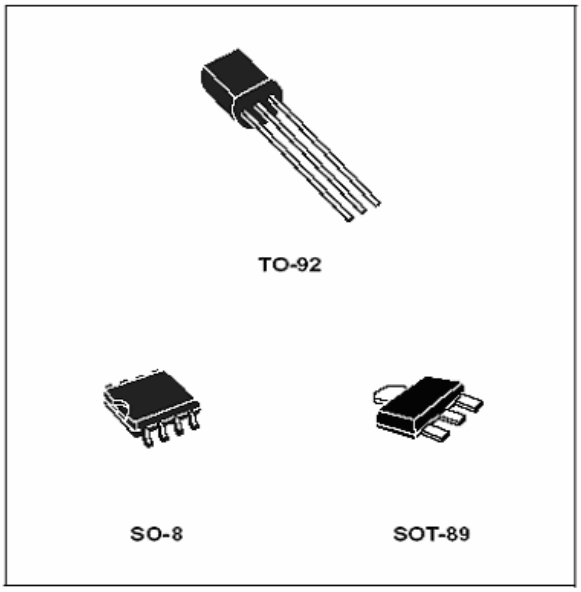
Two Schmitt-Triggered non-inverting buffers redrive and condition the HSYNC and VSYNC signals from the video Connector (SYNC1, SYNC2). These buffers accept VESA VSIS compliant TTL input signals and convert them to CMOS output levels that swing between Ground and V_{CC}.



16 Pin QSOP

3. 78L05

- OUTPUT CURRENT UP TO 100 mA
- OUTPUT VOLTAGES OF 3.3; 5; 6; 8; 9; 10; 12; 15; 18; 20; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- NO EXTERNAL COMPONENTS ARE REQUIRED
- AVAILABLE IN EITHER ±5% (AC) OR ±10% (C) SELECTION



DESCRIPTION

The L78L00 series of three-terminal positive regulators employ internal current limiting and thermal shutdown, making them essentially indestructible. If adequate heat-sink is provided, they can deliver up to 100 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local or on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power pass elements to make high-current voltage regulators. The L78L00 series used as Zener diode/resistor combination replacement, offers an effective output impedance improvement of typically two orders of magnitude, along with lower quiescent current and lower noise.

4. FSAV330

General Description

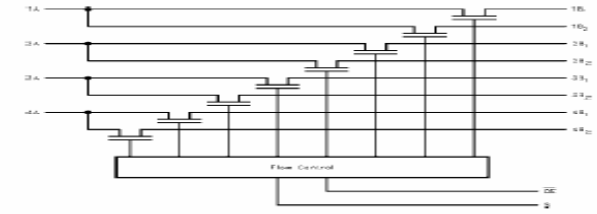
The Fairchild Video Switch FSAV330 is a quad single pole/ double throw high-speed CMOS TTL-compatible video switch. The low On Resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

When $\overline{OE}$ is LOW, the select pin connects the A Port to the selected B Port output. When $\overline{OE}$ is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

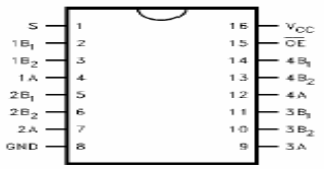
Features

- Replacement for the P15V330
- Wide bandwidth 300 MHz
- 4Ω switch connection between two ports
- Minimal propagation delay through the switch
- Low I_{CC}
- Zero bounce in flow-through mode
- Control inputs compatible with TTL level

Logic Diagram



Connection Diagram



Pin Descriptions

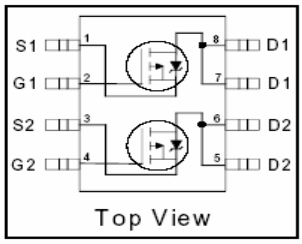
Pin Name	Description
$\overline{OE}$	Bus Switch Enable
S	Select Input
A	Bus A
B_1–B_2	Bus B

Truth Table

S	$\overline{OE}$	Function
X	H	Disconnect
L	L	$A = B_1$
H	L	$A = B_2$

5. IRF7314

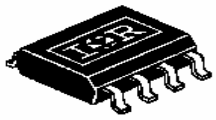
- Generation V Technology
- Ultra Low On-Resistance
- Dual P-Channel MOSFET
- Surface Mount
- Fully Avalanche Rated



Top View

V_{DSS} = -20V

$R_{DS(on)}$ = 0.058Ω



SO-8

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

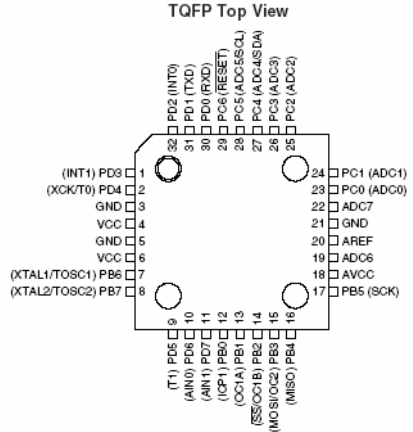
The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques.

6. ATMEGA8L

Features

- High-performance, Low-power AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 130 Powerful Instructions – Most Single-clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- Nonvolatile Program and Data Memories
  - 8K Bytes of In-System Self-Programmable Flash
    Endurance: 10,000 Write/Erase Cycles
  - Optional Boot Code Section with Independent Lock Bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - 512 Bytes EEPROM
    Endurance: 100,000 Write/Erase Cycles
  - 1K Byte Internal SRAM
  - Programming Lock for Software Security
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler, one Compare Mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Three PWM Channels
  - 8-channel ADC in TQFP and MLF package
    Eight Channels 10-bit Accuracy
  - 6-channel ADC in PDIP package
    Eight Channels 10-bit Accuracy
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Five Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, and Standby
- I/O and Packages
  - 23 Programmable I/O Lines
  - 28-lead PDIP, 32-lead TQFP, and 32-pad MLF
- Operating Voltages
  - 2.7 - 5.5V (ATmega8L)
  - 4.5 - 5.5V (ATmega8)
- Speed Grades
  - 0 - 8 MHz (ATmega8L)
  - 0 - 16 MHz (ATmega8)
- Power Consumption at 4 Mhz, 3V, 25°C
  - Active: 3.6 mA
  - Idle Mode: 1.0 mA
  - Power-down Mode: 0.5 µA

TQFP Top View



7. HYB25DC256160CE-5

1.2 Description

The 256 Mbit Double-Data-Rate SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a quad-bank DRAM.

The 256 Mbit Double-Data-Rate SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a *2n* prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256 Mbit Double-Data-Rate SDRAM effectively consists of a single 2*n*-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during Reads and by the memory controller during Writes. DQS is edge-aligned with data for Reads and center-aligned with data for Writes.

The 256 Mbit Double-Data-Rate SDRAM operates from a differential clock (CK and $\overline{CK}$; the crossing of CK going HIGH and $\overline{CK}$ going LOW is referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable Read or Write burst lengths of 2, 4 or 8 locations. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access. As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

Note: The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

Table 2 Ordering Information for Lead Containing Products

Product Type[2]	Org.	CAS-RCD-RP Latencies	Clock (MHz)	CAS-RCD-RP Latencies	Clock (MHz)	Speed	Package
HYB25DC256160CT–6	×16	2.5-3-3	166	2-3-3	133	DDR333	P-TSOPII-66

Table 3 Ordering Information for Lead free (RoHS[1] Compliant) Products

Product Type[2]	Org.	CAS-RCD-RP Latencies	Clock (MHz)	CAS-RCD-RP Latencies	Clock (MHz)	Speed	Package
HYB25DC256800CE–5	×8	3-3-3	200	2.5-3-3	166	DDR400B	P-TSOPII-66
HYB25DC256160CE–5	×16						
HYB25DC256160CE–6	×16	2.5-3-3	166	2-3-3	133	DDR333	
HYB25DC256800CF–5	×8	3-3-3	200	2-3-3	133	DDR400A	P-TFBGA-60
HYB25DC256160CF–5	×16						
HYB25DC256160CF–6	×16	2.5-3-3	166	2-3-3	133	DDR333	

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

2) HYB: designator for memory components
25D: DDR SDRAMs at V_{DD} = 2.5 V
256: 256-Mbit density
400/800/160: Product variations ×4, ×8 and ×16
C: Die revision C
L: low power (available on request)
E/F: Package type TSOP(contains Lead), TSOP(Lead & Halone free), FBGA(Lead & Halone free) and FBGA (contains Lead)

2 Pin Configuration

The pin configuration of a DDR SDRAM is listed by function in Table 1 (60 pins). The abbreviations used in the Pin#/Buffer# column are explained in Table 2 and Table 3 respectively. The pin numbering for FBGA is depicted in Figure ? and that of the TSOP package in Figure ?

Table 4 Pin Configuration of DDR SDRAM

Ball#/Pin#	Name	Pin Type	Buffer Type	Function
Clock Signals				
G2, 45	CK	I	SSTL	**Clock Signal** *Note: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).*
G3, 46	$\overline{CK}$	I	SSTL	**Complementary Clock Signal**
H3, 44	CKE	I	SSTL	**Clock Enable Rank** *Note: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after V_{DD} is applied on first power up. After V_{REF} has become stable during the power on and initialization sequence, it must be mantained for proper operation of the CKE receiver. For proper self-refresh entry and exit, V_{REF} must be mantained to this input.*
Control Signals				
H7, 23	$\overline{RAS}$	I	SSTL	**Row Address Strobe**
G8, 22	$\overline{CAS}$	I	SSTL	**Column Address Strobe**
G7, 21	$\overline{WE}$	I	SSTL	**Write Enable**
H8, 24	$\overline{CS}$	I	SSTL	**Chip Select** *Note: All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code. The standard pinout includes one $\overline{CS}$ pin.*
Address Signals				

4 Functional Description

The 256 Mbit Double-Data-Rate SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. The 256 Mbit Double-Data-Rate SDRAM is internally configured as a quad-bank DRAM.

The 256 Mbit Double-Data-Rate SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a 2*n* prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256 Mbit Double-Data-Rate SDRAM consists of a single 2*n*-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A12 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

4.1 Initialization

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. The following criteria must be met:

No power sequencing is specified during power up or power down given the following criteria:

- V_{DD} and V_{DDQ} are driven from a single power converter output
- V_{TT} meets the specification
- A minimum resistance of 42 Ω limits the input current from the V_{TT} supply into any pin and V_{REF} tracks $V_{DDQ}/2$ or the following relationship must be followed:
- V_{DDQ} is driven after or with V_{DD} such that $V_{DDQ} < V_{DD} + 0.3$ V
- V_{TT} is driven after or with V_{DDQ} such that $V_{TT} < V_{DDQ} + 0.3$ V
- V_{REF} is driven after or with V_{DDQ} such that $V_{REF} < V_{DDQ} + 0.3$ V

The DQ and DQS outputs are in the High-Z state, where they remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200 µs delay prior to applying an executable command.

Once the 200 µs delay has been satisfied, a Deselect or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a Precharge ALL command should be applied. Next a Mode Register Set command should be issued for the Extended Mode Register, to enable the DLL, then a Mode Register Set command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any executable command. During the 200 cycles of clock for DLL locking, a Deselect or NOP command must be applied. After the 200 clock cycles, a Precharge ALL command should be applied, placing the device in the "all banks idle" state.

Once in the idle state, two AUTO REFRESH cycles must be performed. Additionally, a Mode Register Set command for the Mode Register, with the reset DLL bit deactivated (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

4.2.1 Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given Read or Write command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a Read or Write command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst wraps within the block if a boundary is reached. The block is uniquely selected by A1-Ai when the burst length is set to two, by A2-Ai when the burst length is set to four and by A3-Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both Read and Write bursts.

4.2.3 Read Latency

The Read latency, or CAS latency, is the delay, in clock cycles, between the registration of a Read command and the availability of the first burst of output data. The latency can be programmed 2, 2.5 and 3 clocks. CAS latency of 1.5 is supported for DDR200 components only.

If a Read command is registered at clock edge n, and the latency is *m* clocks, the data is available nominally coincident with clock edge *n* + *m* (see Figure 6).

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

4.2.4 Operating Mode

The normal operating mode is selected by issuing a Mode Register Set Command with bits A7-A12 set to zero, and bits A0-A6 set to the desired values. A DLL reset is initiated by issuing a Mode Register Set command with bits A7 and A9-A12 each set to zero, bit A8 set to one, and bits A0-A6 set to the desired values. A Mode Register Set command issued to reset the DLL should always be followed by a Mode Register Set command to select normal operating mode.

All other combinations of values for A7-A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used as unknown operation or incompatibility with future versions may result.

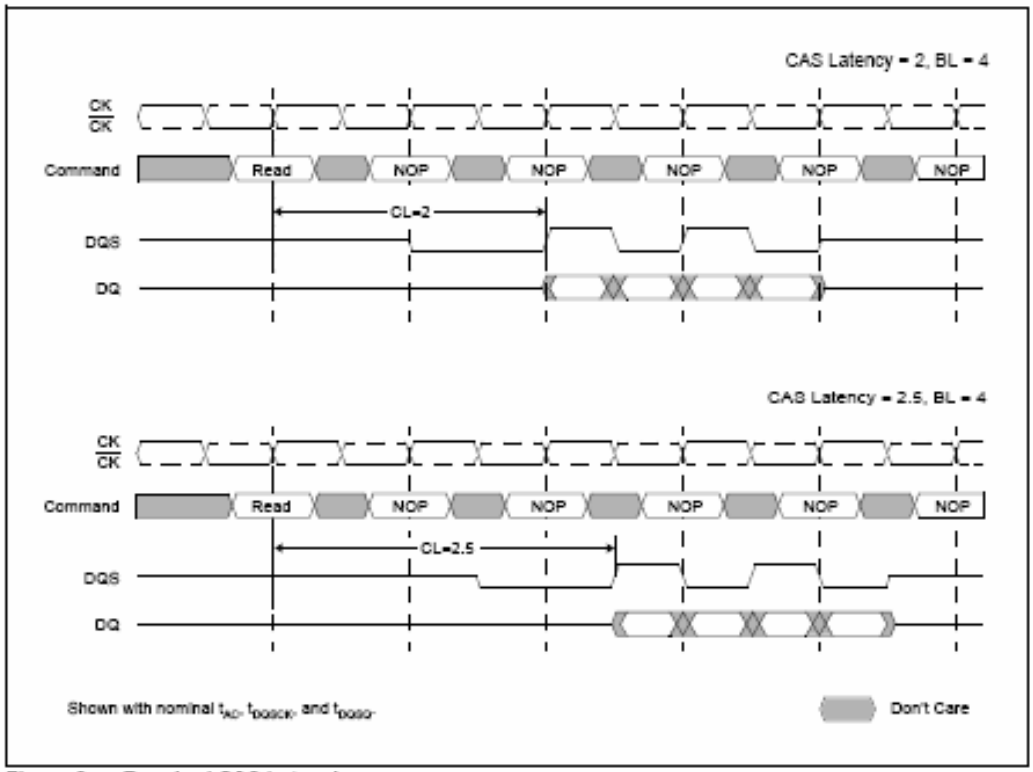


Figure 6 Required CAS Latencies

4.3.1 DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled, 200 clock cycles must occur before a Read command can be issued. This is the reason 200 clock cycles must occur before issuing a Read or Write command upon exit of self refresh operation.

4.3.2 Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II. In addition this design version supports a weak driver mode for lighter load and/or point-to-point environments which can be activated during mode register set. *I-V* curves for the normal and weak drive strength are included in this document.

8. FAN5236

FAN5236

Dual Mobile-Friendly DDR / Dual-output PWM Controller

Features

- Highly flexible dual synchronous switching PWM controller includes modes for:
  - DDR mode with in-phase operation for reduced channel interference
  - 90° phase shifted two-stage DDR Mode for reduced input ripple
  - Dual Independent regulators 180° phase shifted
- Complete DDR Memory power solution
  - V_{TT} Tracks VDDQ/2
  - VDDQ/2 Buffered Reference Output
- Lossless current sensing on low-side MOSFET or precision over-current using sense resistor
- V_{CC} Under-voltage Lockout
- Converters can operate from +5V or 3.3V or Battery power input (5 to 24V)
- Excellent dynamic response with Voltage Feed-Forward and Average Current Mode control
- Power-Good Signal
- Also supports DDR-II and HSTL
- Light load Hysteretic mode maximizes efficiency
- QSOP28, TSSOP28

Applications

- DDR V_{DDQ} and V_{TT} voltage generation
- Mobile PC dual regulator
- Server DDR power
- Hand-Held PC power

General Description

The FAN5236 PWM controller provides high efficiency and regulation for two output voltages adjustable in the range from 0.9V to 5.5V that are required to power I/O, chip-sets, and memory banks in high-performance notebook computers, PDAs and Internet appliances. Synchronous rectification and hysteretic operation at light loads contribute to a high efficiency over a wide range of loads. The hysteretic mode of operation can be disabled separately on each PWM converter if PWM mode is desired for all load levels. Efficiency is even further enhanced by using MOSFET's $R_{DS(ON)}$ as a current sense component.

Feed-forward ramp modulation, average current mode control scheme, and internal feedback compensation provide fast response to load transients. Out-of-phase operation with 180 degree phase shift reduces input current ripple. The controller can be transformed into a complete DDR memory power supply solution by activating a designated pin. In DDR mode of operation one of the channels tracks the output voltage of another channel and provides output current sink and source capability -- features essential for proper powering of DDR chips. The buffered reference voltage required by this type of memory is also provided. The FAN5236 monitors these outputs and generates separate PGx (power good) signals when the soft-start is completed and the output is within ±10% of its set point. A built-in over-voltage protection prevents the output voltage from going above 120% of the set point. Normal operation is automatically restored when the over-voltage conditions go away. Under-voltage protection latches the chip off when either output drops below 75% of its set value after the soft-start sequence for this output is completed. An adjustable over-current function monitors the output current by sensing the voltage drop across the lower MOSFET. If precision current-sensing is required, an external current-sense resistor may optionally be used.

Generic Block Diagrams

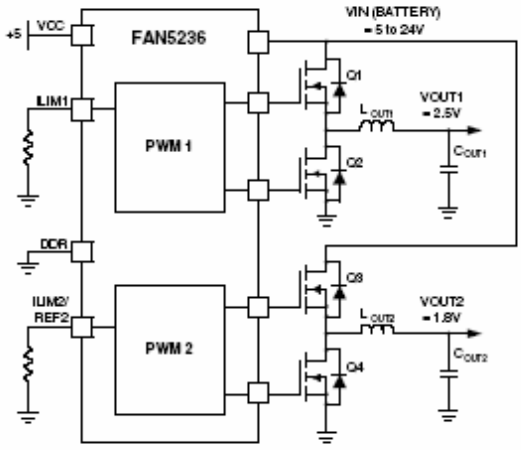


Figure 1. Dual output regulator

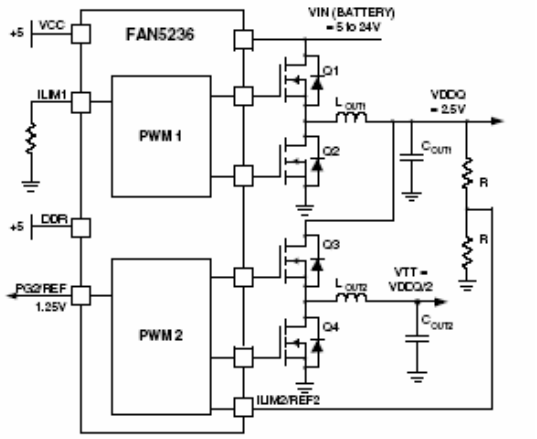
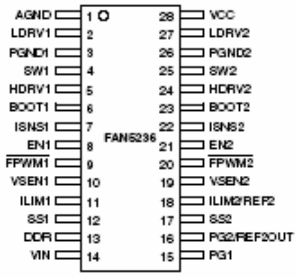


Figure 2. Complete DDR Memory Power Supply

Pin Configurations



QSOP-28 or TSSOP-28
θ_{JA} = 90°C/W

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	AGND	**Analog Ground.** This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin.
2 27	LDRV1 LDRV2	**Low-Side Drive.** The low-side (lower) MOSFET driver output. Connect to gate of low-side MOSFET.
3 26	PGND1 PGND2	**Power Ground.** The return for the low-side MOSFET driver. Connect to source of low-side MOSFET.
4 25	SW1 SW2	**Switching node.** Return for the high-side MOSFET driver and a current sense input. Connect to source of high-side MOSFET and low-side MOSFET drain.
5 24	HDRV1	**High-Side Drive.** High-side (upper) MOSFET driver output. Connect to gate of high-side MOSFET.
6 23	BOOT1 BOOT2	**BOOT.** Positive supply for the upper MOSFET driver. Connect as shown in Figure 3.
7 22	ISNS1 ISNS2	**Current Sense Input.** Monitors the voltage drop across the lower MOSFET or external sense resistor for current feedback.
8 21	EN1 EN2	**Enable.** Enables operation when pulled to logic high. Toggling EN will also reset the regulator after a latched fault condition. These are CMOS inputs whose state is indeterminate if left open.
9 20	$\overline{\text{FPWM1}}$ $\overline{\text{FPWM2}}$	**Forced PWM mode.** When logic low, inhibits the regulator from entering hysteretic mode. Otherwise tie to VOUT. The regulator uses VOUT on this pin to ensure a smooth transition from Hysteretic mode to PWM mode.
10 19	VSEN1 VSEN2	**Output Voltage Sense.** The feedback from the outputs. Used for regulation as well as PG, under-voltage and over-voltage protection and monitoring.
11	ILIM1	**Current Limit 1.** A resistor from this pin to GND sets the current limit.
12 17	SS1 SS2	**Soft Start.** A capacitor from this pin to GND programs the slew rate of the converter during initialization. During initialization, this pin is charged with a 5µA current source.
13	DDR	**DDR Mode Control.** High = DDR mode. Low = 2 separate regulators operating 180° out of phase.

Pin Definitions (continued)

14	VIN	**Input Voltage.** Normally connected to battery, providing voltage feed-forward to set the amplitude of the internal oscillator ramp. When using the IC for 2-step conversion from 5V input, connect through 100K to ground, which will set the appropriate ramp gain and synchronize the channels 90° out of phase.
15	PG1	**Power Good Flag.** An open-drain output that will pull LOW when VSEN is outside of a ±10% range of the 0.9V reference.
16	PG2 / REF2OUT	**Power Good 2.** When not in DDR Mode: Open-drain output that pulls LOW when the VOUT is out of regulation or in a fault condition **Reference Out 2.** When in DDR Mode, provides a buffered output of REF2. Typically used as the VDDQ/2 reference.
18	ILIM2 / REF2	**Current Limit 2.** When not in DDR Mode, A resistor from this pin to GND sets the current limit. **Reference** for reg #2 when in DDR Mode. Typically set to VOUT1 / 2.
28	VCC	**VCC.** This pin powers the chip as well as the LDRV buffers. The IC starts to operate when voltage on this pin exceeds 4.6V (UVLO rising) and shuts down when it drops below 4.3V (UVLO falling).

Absolute Maximum Ratings

Absolute maximum ratings are the values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

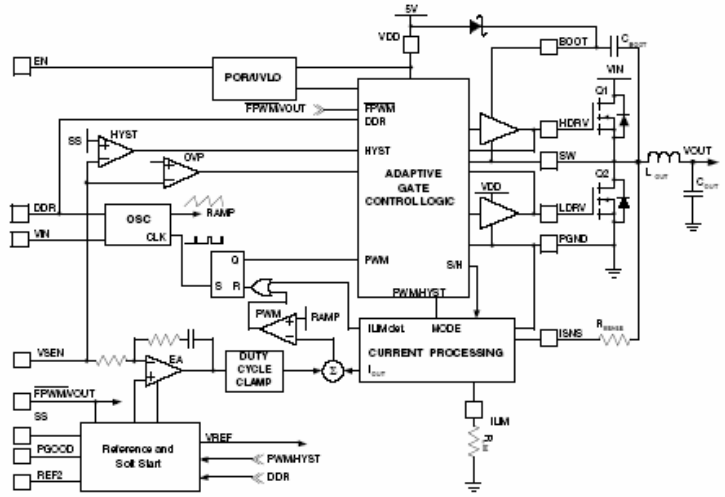
Parameter	Min.	Typ.	Max.	Units
VCC Supply Voltage:			6.5	V
VIN			27	V
BOOT, SW, ISNS, HDRV			33	V
BOOTx to SWx			6.5	V
All Other Pins	–0.3		VCC+0.3	V
Junction Temperature (T_J)	–10		150	°C
Storage Temperature	–65		150	°C
Lead Soldering Temperature, 10 seconds			300	°C

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCC		4.75	5	5.25	V
Supply Voltage VIN		5		24	V
Ambient Temperature (T_A)		–10		85	°C

Electrical Specifications Recommended operating conditions, unless otherwise noted. (continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
DDR, EN Inputs					
Input High		2			V
Input Low				0.8	V
FPWM Inputs					
FPWM Low				0.1	V
FPWM High	FPWM connected to output	0.9			V



Typical Applications

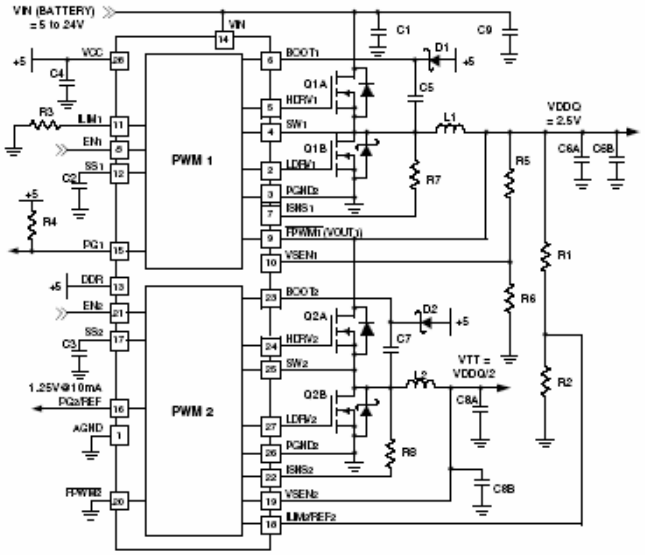


Figure 4. DDR Regulator Application

Table 1. DDR Regulator BOM

Description	Qty	Ref.	Vendor	Part Number
Capacitor 68µf, Tantalum, 25V, ESR 150mΩ	1	C1	AVX	TPSV686*025#0150
Capacitor 10nf, Ceramic	2	C2, C3	Any	
Capacitor 68µf, Tantalum, 6V, ESR 1.8Ω	1	C4	AVX	TAJB686*006
Capacitor 150nF, Ceramic	2	C5, C7	Any	
Capacitor 180µf, Specialty Polymer, 4V, ESR 15mΩ	2	C6A, C6B, C8A, C8B	Panasonic	EEFUE0G181R
Capacitor 0.1µF, Ceramic	2	C9	Any	
18.2KΩ, 1% Resistor	3	R1, R2, R6	Any	
56.2KΩ, 1% Resistor	2	R3	Any	
10KΩ, 5% Resistor	2	R4	Any	
32.4KΩ, 1% Resistor	1	R5	Any	
1.5KΩ, 1% Resistor	1	R7	Any	
499Ω, 1% Resistor	1	R8	Any	
Schottky Diode 30V	2	D1, D2	Fairchild	BAT54
Inductor 6.4µH, 6A, 8.64mΩ	1	L1, L2	Panasonic	ETQ-P6F6R4HFA
Dual MOSFET with Schottky	1	Q1, Q2	Fairchild	FDS6986S
DDR Controller	1	U1	Fairchild	FAN5236

Circuit Description

Overview

The FAN5236 is a multi-mode, dual channel PWM controller intended for graphic chipset, SDRAM, DDR DRAM or other low voltage power applications in modern notebook, desktop, and sub-notebook PCs. The IC integrates a control circuitry for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider.

The two synchronous buck converters can operate from either an unregulated DC source (such as a notebook battery) with voltage ranging from 5.0V to 24V, or from a regulated system rail of 3.3V to 5V. In either mode of operation the IC is biased from a +5V source. The PWM modulators use an average current mode control with input voltage feed-forward for simplified feedback loop compensation and improved line regulation. Both PWM controllers have integrated feedback loop compensation that dramatically reduces the number of external components.

Depending on the load level, the converters can operate either in fixed frequency PWM mode or in a hysteretic mode. Switch-over from PWM to hysteretic mode improves the converters' efficiency at light loads and prolongs battery run time. In hysteretic mode, comparators are synchronized to the main clock that allows seamless transition between the operational modes and reduced channel-to-channel interaction. The hysteretic mode of operation can be inhibited independently for each channel if variable frequency operation is not desired.

The FAN5236 can be configured to operate as a complete DDR solution. When the DDR pin is set high, the second channel can provide the capability to track the output voltage of the first channel. The PWM2 converter is prevented from going into hysteretic mode if the DDR pin is set high. In DDR mode, a buffered reference voltage (buffered voltage of the REF2 pin), required by DDR memory chips, is provided by the PG2 pin.

Converter Modes and Synchronization

Table 3. Converter modes and Synchronization

Mode	VIN	VIN PIn	DDR PIn	PWM 2 w.r.t. PWM1
DDR1	Battery	VIN	HIGH	IN PHASE
DDR2	+5V	R to GND	HIGH	+ 90°
DUAL	ANY	VIN	LOW	+ 180°

When used as a dual converter (as in Figure 5), out-of-phase operation with 180 degree phase shift reduces input current ripple.

For the "2-step" conversion (where the VTT is converted from VDDQ as in Figure 4) used in DDR mode, the duty cycle of the second converter is nominally 50% and the optimal phasing depends on VIN. The objective is to keep noise generated from the switching transition in one converter from influencing the "decision" to switch in the other converter.

When VIN is from the battery, it's typically higher than 7.5V. As shown in Figure 6, 180° operation is undesirable since the turn-on of the VDDQ converter occurs very near the decision point of the VTT converter.

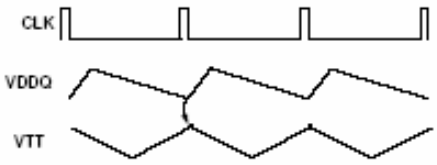


Figure 6. Noise-susceptible 180° phasing for DDR1

In-phase operation is optimal to reduce inter-converter interference when VIN is higher than 5V, (when VIN is from a battery), as can be seen in Figure 7. Since the duty cycle of PWM1 (generating VDDQ) is short, it's switching point occurs far away from the decision point for the VTT regulator, whose duty cycle is nominally 50%.

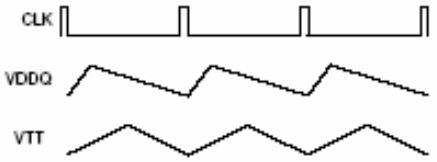


Figure 7. Optimal In-Phase operation for DDR1

When VIN = 5V, 180° phase shifted operation can be rejected for the same reasons demonstrated Figure 6. In-phase operation with VIN = 5V is even worse, since the switch point of either converter occurs near the switch point of the other converter as seen in Figure 8. In this case, as VIN is a little higher than 5V it will tend to cause early termination of the VTT pulse width. Conversely, VTT's switch point can cause early termination of the VDDQ pulse width when VIN is slightly lower than 5V.

Over-Voltage / Under-voltage Protection

Should the VSNS voltage exceed 120% of VREF (0.9V) due to an upper MOSFET failure, or for other reasons, the over-voltage protection comparator will force LDRV high. This action actively pulls down the output voltage and, in the event of the upper MOSFET failure, will eventually blow the battery fuse. As soon as the output voltage drops below the threshold, the OVP comparator is disengaged.

This OVP scheme provides a 'soft' crowbar function which helps to tackle severe load transients and does not invert the output voltage when activated — a common problem for latched OVP schemes.

Similarly, if an output short-circuit or severe load transient causes the output to droop to less than 75% of its regulation set point. Should this condition occur, the regulator will shut down.

Over-Temperature Protection

The chip incorporates an over temperature protection circuit that shuts the chip down when a die temperature of about 150°C is reached. Normal operation is restored at die temperature below 125°C with internal Power On Reset asserted, resulting in a full soft-start cycle.

Design and Component Selection Guidelines

As an initial step, define operating input voltage range, output voltage, minimum and maximum load currents for the controller.

Output Inductor Selection

The minimum practical output inductor value is the one that keeps inductor current just on the boundary of continuous conduction at some minimum load. The industry standard practice is to choose the minimum current somewhere from 15% to 35% of the nominal current. At light load, the controller can automatically switch to hysteretic mode of operation to sustain high efficiency. The following equations help to choose the proper value of the output filter inductor.

$$\Delta I = 2 - I_{MIN} = \frac{\Delta V_{OUT}}{ESR} \qquad (x)$$

where ΔI is the inductor ripple current and ΔV_{OUT} is the maximum ripple allowed.

$$L = \frac{V_{IN} - V_{OUT}}{F_{SW} \times \Delta I} \times \frac{V_{OUT}}{V_{IN}} \qquad (9)$$

for this example we'll use:

V_{IN} = 20V, V_{OUT} = 2.5V
ΔI = 20% * 6A = 1.2A
F_{SW} = 300KHz.

therefore
L = 6µH

Output Capacitor Selection

The output capacitor serves two major functions in a switching power supply. Along with the inductor it filters the sequence of pulses produced by the switcher, and it supplies the load transient currents. The output capacitor requirements are usually dictated by ESR, Inductor ripple current (ΔI) and the allowable ripple voltage (ΔV).

$$ESR < \frac{\Delta V}{\Delta I} \qquad (10)$$

In addition, the capacitor's ESR must be low enough to allow the converter to stay in regulation during a load step. The ripple voltage due to ESR for the converter in Figure 5 is 120mV P-P. Some additional ripple will appear due to the capacitance value itself:

$$\Delta V = \frac{\Delta I}{C_{OUT} \times 8 \times F_{SW}} \qquad (11)$$

which is only about 1.5mV for the converter in Figure 5 and can be ignored.

The capacitor must also be rated to withstand the RMS current which is approximately 0.3 X (ΔI), or about 400mA for the converter in Figure 5. High frequency decoupling capacitors should be placed as close to the loads as physically possible.

Input Capacitor Selection

The input capacitor should be selected by its ripple current rating.

Two-Stage Converter Case

In DDR mode (Figure 4), the VTT power input is powered by the VDDQ output, therefore all of the input capacitor ripple current is produced by the VDDQ converter. A conservative estimate of the output
current required for the 2.5V regulator is:

$$I_{REG1} = I_{VDDQ} + \frac{I_{VTT}}{2}$$

As an example, if average I_{VDDQ} is 3A, and average I_{VTT} is 1A, I_{VDDQ} current will be about 3.5A. If average input voltage is 16V, RMS input ripple current will be:

$$I_{RMS} = I_{OUT(MAX)} \sqrt{D - D^2} \qquad (12)$$

where D is the duty cycle of the PWM1 converter:

$$D < \frac{V_{OUT}}{V_{IN}} = \frac{2.5}{16} \qquad (13)$$

therefore:

$$I_{RMS} = 3.5\sqrt{\frac{2.5}{16} - \left(\frac{2.5}{16}\right)^2} = 1.49A \quad (14)$$

Dual Converter 180° phased

In Dual mode (Figure 5), both converters contribute to the capacitor input ripple current. With each converter operating 180° out of phase, the RMS currents add in the following fashion:

$$I_{RMS} = \sqrt{I_{RMS(1)}^2 + I_{RMS(2)}^2} \text{ or} \quad (15a)$$

$$I_{RMS} = \sqrt{(I_1)^2(D_1 - D_1^2) + (I_2)^2(D_2 - D_2^2)} \quad (15b)$$

which for the dual 3A converters of Figure 5, calculates to:

$$I_{RMS} = 1.4A$$

Power MOSFET Selection

Losses in a MOSFET are the sum of its switching (P_{SW}) and conduction (P_{COND}) losses.

In typical applications, the FAN5236 converter's output voltage is low with respect to its input voltage, therefore the Lower MOSFET (Q2) is conducting the full load current for most of the cycle. Q2 should therefore be selected to minimize conduction losses, thereby selecting a MOSFET with low $R_{DS(ON)}$.

In contrast, the high-side MOSFET (Q1) has a much shorter duty cycle, and it's conduction loss will therefore have less of an impact. Q1, however, sees most of the switching losses, so Q1's primary selection criteria should be gate charge.

High-Side Losses:

Figure 15 shows a MOSFET's switching interval, with the upper graph being the voltage and current on the Drain to Source and the lower graph detailing V_{GS} vs. time with a constant current charging the gate. The x-axis therefore is also representative of gate charge (Q_G) . $C_{ISS} = C_{GD} + C_{GS}$, and it controls t1, t2, and t4 timing. C_{GD} receives the current from the gate driver during t3 (as V_{DS} is falling). The gate charge (Q_G) parameters on the lower graph are either specified or can be derived from MOSFET datasheets.

Assuming switching losses are about the same for both the rising edge and falling edge, Q1's switching losses, occur during the shaded time when the MOSFET has voltage across it and current through it.

These losses are given by:

$$P_{UPPER} = P_{SW} + P_{COND}$$

$$P_{SW} = \left(\frac{V_{DS} \times I_L}{2} \times 2 \times t_S\right) F_{SW} \quad (16)$$

$$P_{COND} = \left(\frac{V_{IN}}{V_{OUT}}\right) \times I_{OUT}^2 \times R_{DS(ON)} \quad (17)$$

P_{UPPER} is the upper MOSFET's total losses, and P_{SW} and P_{COND} are the switching and conduction losses for a given MOSFET. $R_{DS(ON)}$ is at the maximum junction temperature (T_J). t_S is the switching period (rise or fall time) and is t2+t3 Figure 15.

The driver's impedance and C_{ISS} determine t2 while t3's period is controlled by the driver's impedance and Q_{GD}. Since most of t_S occurs when $V_{GS} = V_{SP}$ we can use a constant current assumption for the driver to simplify the calculation of t_S :

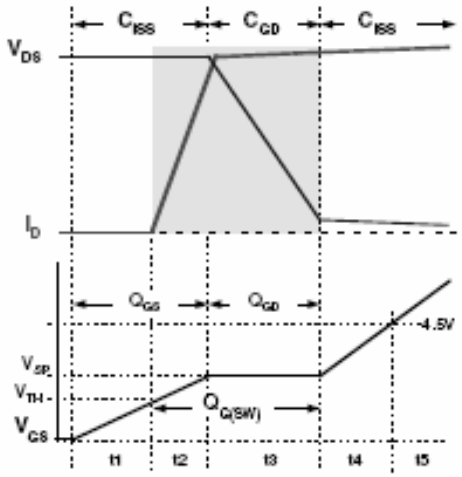


Figure 15. Switching losses and Q_G

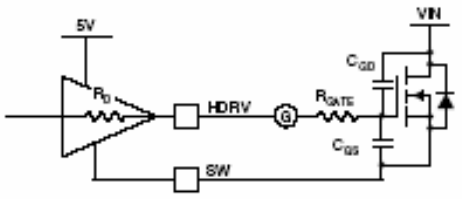


Figure 16. Drive Equivalent Circuit

$$t_S = \frac{Q_{G(SW)}}{I_{DRIVER}} = \frac{Q_{G(SW)}}{\left(\frac{VCC - V_{SP}}{R_{DRIVER} + R_{GATE}}\right)} \quad (18)$$

Most MOSFET vendors specify Q_{GD} and Q_{GS}. $Q_{G(SW)}$ can be determined as: $Q_{G(SW)} = Q_{GD} + Q_{GS} - Q_{TH}$ where Q_{TH} is the the gate charge required to get the MOSFET to it's threshold (V_{TH}). For the high-side MOSFET, V_{DS} = VIN.

9. FDS6680

FAIRCHILD
SEMICONDUCTOR TM

April 1998

FDS6680

Single N-Channel Logic Level PWM Optimized PowerTrench™ MOSFET

General Description

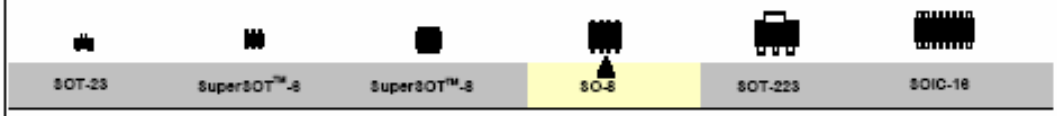
This N-Channel Logic Level MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

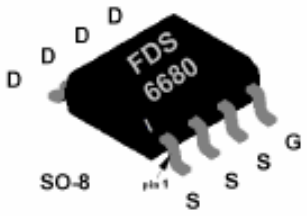
The MOSFET features faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications.

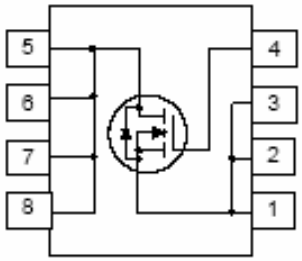
The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

Features

- 11.5 A, 30 V. $R_{DS(ON)}$ = 0.010 Ω @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 0.015 Ω @ V_{GS} = 4.5 V.
- Optimized for use in switching DC/DC converters with PWM controllers.
- Very fast switching.
- Low gate charge (typical Qg = 19 nC).







Absolute Maximum Ratings T_A = 25°C unless other wise noted

Symbol	Parameter		FDS6680	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current - Continuous	(Note 1a)	11.5	A
	- Pulsed		50	
P_D	Power Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

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FDS6680 Rev.D1

Electrical Characteristics (T_A = 25 °C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = 250 µA, Referenced to 25 °C		23		mV/ °C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.7	3	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp.Coefficient	I_D = 250 µA, Referenced to 25 °C		-5		mV/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 11.5 A		0.0065	0.01	Ω
		T_J =125°C		0.014	0.017	
		V_{GS} = 4.5 V, I_D = 9.5 A		0.0125	0.015	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	50			A
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 11.5 A		40		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		2070		pF
C_{oss}	Output Capacitance			510		pF
C_{rss}	Reverse Transfer Capacitance			235		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DS} = 15 V, I_D = 1 A		13	21	ns
t_r	Turn - On Rise Time	V_{GS} = 10 V, R_{GEN} = 6 Ω		10	18	ns
$t_{D(off)}$	Turn - Off Delay Time			36	58	ns
t_f	Turn - Off Fall Time			13	23	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 11.5 A, V_{GS} = 5 V		19	27	nC
Q_{gs}	Gate-Source Charge			7		nC
Q_{gd}	Gate-Drain Charge			6		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.1	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A (Note 2)			1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a. 50°C/W on a 1 in² pad of 2oz copper.

b. 105°C/W on a 0.04 in² pad of 2oz copper.

c. 125°C/W on a 0.006 in² pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

FDS6680 Rev.E1

Typical Electrical Characteristics

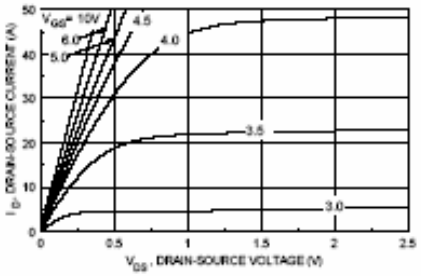

Figure 1. On-Region Charaeteristies.

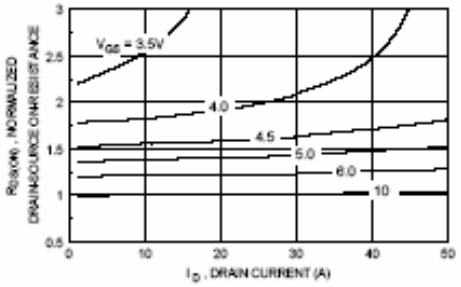

Figure 2. On-Resistanee Variation with Drain Current and Gate Voltage.

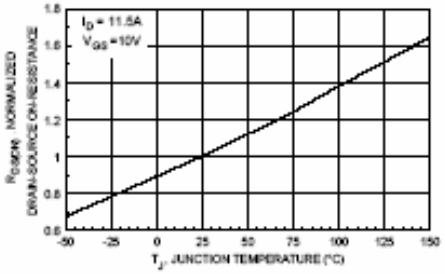

Figure 3. On-Resistanee Variation with Temperature.

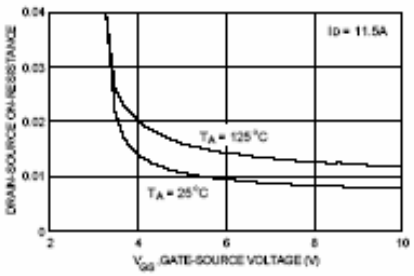

Figure 4. On-Resistanee Variation with Gate-to-Souree Voltage.

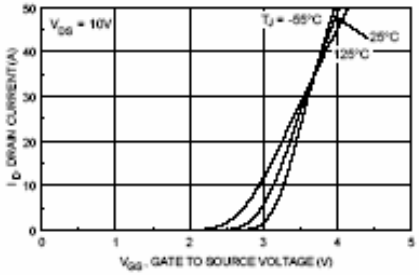

Figure 5. Transfer Characteristics.

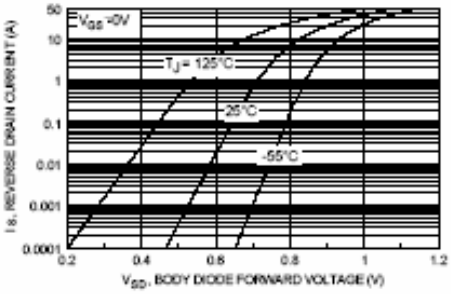

Figure 6. Body Diode Forward Voltage Variation with Souree Current and Temperature.

Typical Electrical And Thermal Characteristics

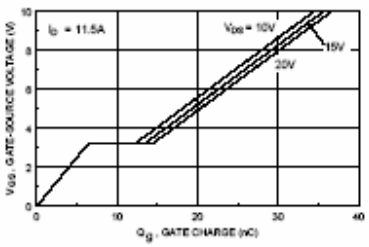

Figure 7. Gate Charge Characteristics.

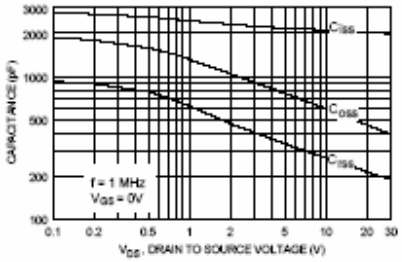

Figure 8. Capacitance Characteristics.

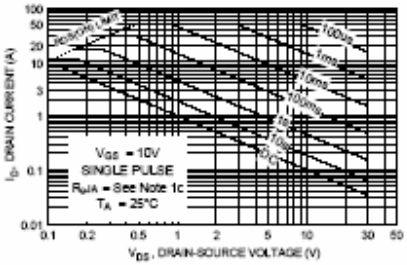

Figure 9. Maximum Safe Operating Area.

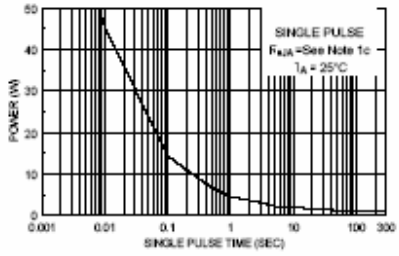

Figure 10. Single Pulse Maximum Power Dissipation.

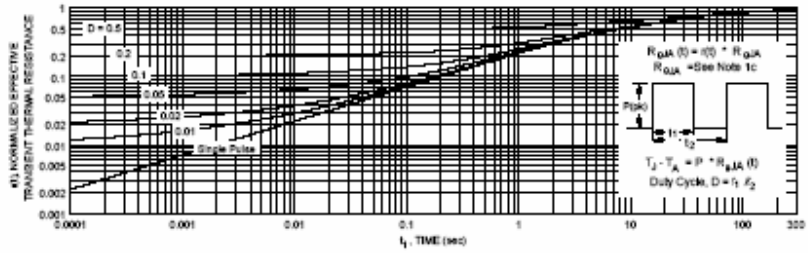

Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

TRADEMARKS

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CoolFET™	MICROWIRE™	UHC™
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E²CMOS™	PowerTrench™	
FACT™	QFET™	
FACT Quiet Series™	QS™	
FAST®	Quiet Series™	
FASTr™	SuperSOT™-3	
GTO™	SuperSOT™-6	
HiSeC™	SuperSOT™-8	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

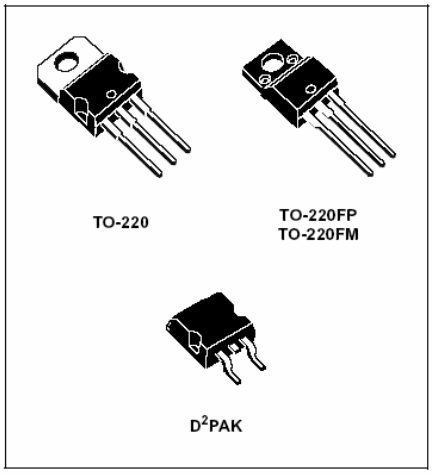
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

ICS on TV Board

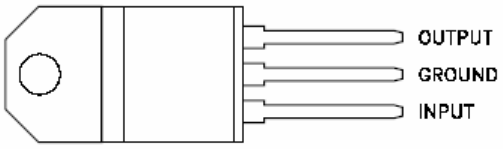
1. L7809

- OUTPUT CURRENT IN EXCESS OF 1A
- OUTPUT VOLTAGES OF 5; 6; 8; 9; 12; 15; 18; 20; 24V
- THERMAL OVERLOAD PROTECTION
- OUTPUT TRANSITION SOA PROTECTION
- 2% OUTPUT VOLTAGE TOLERANCE
- GUARANTEED IN EXTENDED TEMPERATURE RANGE



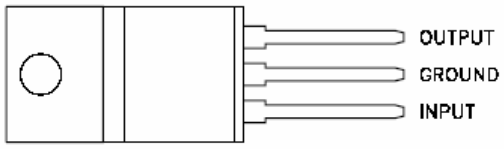
DESCRIPTION

The L7800A series of three terminal positive regulators is available in TO-220, TO-220FP, TO-220FM and D^2PAK packages and several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problem associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current, Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltage and currents.



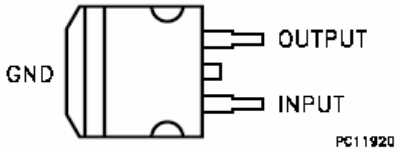
CS05710

TO-220 (Any Type)



CS05700

TO-220FP/TO-220FM



PC11920

D^2PAK

2. CD4052B

The CD4052B is a differential 4-Channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

Features

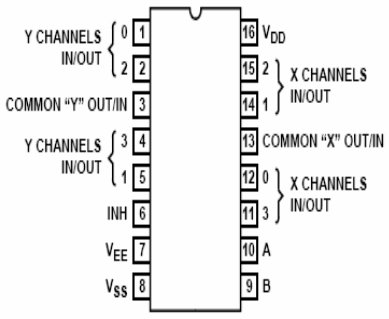
- Wide Range of Digital and Analog Signal Levels
  - Digital . . . . . 3V to 20V
  - Analog. . . . . $\leq 20V_{P-P}$
- Low ON Resistance, 125Ω (Typ) Over $15V_{P-P}$ Signal Input Range for V_{DD}-V_{EE} = 18V
- High OFF Resistance, Channel Leakage of ±100pA (Typ) at V_{DD}-V_{EE} = 18V
- Logic-Level Conversion for Digital Addressing Signals of 3V to 20V (V_{DD}-V_{SS} = 3V to 20V) to Switch Analog Signals to $20V_{P-P}$ (V_{DD}-V_{EE} = 20V)
- Matched Switch Characteristics, r_{ON} = 5Ω (Typ) for V_{DD}-V_{EE} = 15V
- Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2μW (Typ) at V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10V
- Binary Address Decoding on Chip
- 5V, 10V and 15V Parametric Ratings
- 10% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range, 100nA at 18V and 25°C
- Break-Before-Make Switching Eliminates Channel Overlap

Applications

- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating

PInputs

CD4052B (PDIP, CDIP, TSSOP)
TOP VIEW



3. NJM4558

■ GENERAL DESCRIPTION

The NJM4558/4559 integrated circuit is a dual high-gain operational amplifier internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

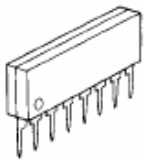
Combining the features of the NJM741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics.Excellent channel separation allow the use of the dual device in single NJM741 operational amplifier applications providing density.It is especially well suited for applications in differential-in,defferential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

■ PACKAGE OUTLINE

NJM4558D
NJM4559D

NJM4558M
NJM4559M

NJM4558V
NJM4559V

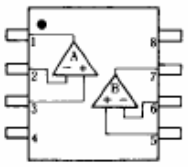


NJM4558L
NJM4559L

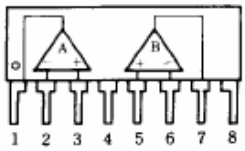
■ FEATURES

- Operating Voltage (±4V~±18V)
- High Voltage Gain (100dB typ.)
- High Input Resistance (5MΩ typ.)
- Package Outline DIP8,DMP8,SIP8,SSOP8
- Bipolar Technology

■ PIN CONFIGURATION



NJM4558D,NJM4558M,NJM4558V
NJM4559D,NJM4559M,NJM4559V



NJM4558L
NJM4559L

PIN FUNCTION
1.A OUTPUT
2.A –INPUT
3.A +INPUT
4.V⁻
5.B +INPUT
6.B –INPUT
7.B OUTPUT
8.V⁺

■ ELECTRICAL CHARACTERISTICS

(V^+/V^-=±15V,Ta=25°C)

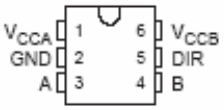
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	R_S≤10kΩ	-	0.5	6	mV
Input Offset Current	I_{IO}		-	5	200	nA
Input Bias Current	I_B		-	25	500	nA
Input Resistance	R_{IN}		0.3	5	-	MΩ
Large Signal Voltage Gain	A_V	R_L≥2kΩ,V_O=±10V	86	100	-	dB
Maximum Output Voltage Swing 1	V_{OM1}	R_L≥10kΩ	± 12	± 14	-	V
Maximum Output Voltage Swing 2	V_{OM2}	R_L≥2kΩ	± 10	± 13	-	V
Input Common Mode Voltage Range	V_{ICM}		± 12	14	-	V
Common Mode Rejection Ratio	CMR	R_S≤10kΩ	70	90	-	dB
Supply Voltage Rejection Ratio	SVR	R_S≤10kΩ	76.5	90	-	dB
Operating Current	I_{CC}		-	3.5	5.7	mA
Slew Rate						
NJM4558	SR		-	1	-	V/μs
NJM4559	SR		-	2	-	V/μs
Equivalent Input Noise Voltage	V_{NI}	RIAA,R_S=2.2kΩ,30kHz LPF	-	1.4	-	μVrms
Gain Bandwidth Product	GB					
NJM4558				3		MHz
NJM4559				6		MHz

4. SN74AVC1T45

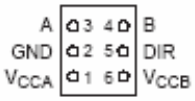
SN74LVC1T45
SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS
SCES515 – DECEMBER 2003

- **Available in the Texas Instruments NanoStar™ and NanoFree™ Packages**
- **Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range**
- **V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State**
- **DIR Referenced to V_{CCA}**
- **Low Power Consumption, 10-μA Max I_{CC}**
- **±24-mA Output Drive at 3.3 V**
- **I_{off} Supports Partial-Power-Down Mode Operation**

DBV OR DCK PACKAGE
(TOP VIEW)



YEP OR YZP PACKAGE
(BOTTOM VIEW)



description/ordering information

This single-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A-port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V. The B-port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

The SN74LVC1T45 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input.

The SN74LVC1T245 is designed so that DIR is supplied by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are in the high-impedance state.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

PRODUCT PREVIEW

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Tape and reel	SN74LVC1T45YEPR	TBD
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74LVC1T45YZPR	
	SOT (SOT-23) – DBV	Tape and reel	SN74LVC1T45DBVR	TBD
	SOT (SC-70) – DCK	Tape and reel	SN74LVC1T45DCKR	TBD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

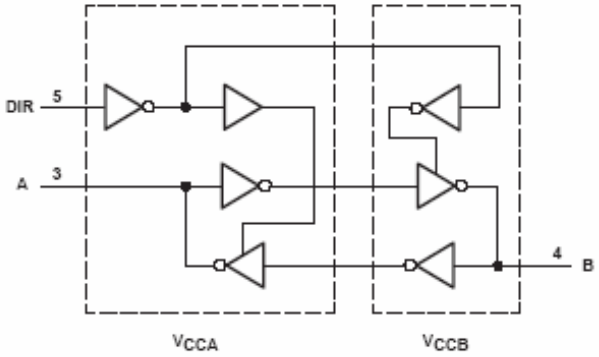
‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.
YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

PRODUCT PREVIEW

FUNCTION TABLE

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CCA} and V_{CCB} . . . . . −0.5 V to 6.5 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O
(see Note 1) . . . . . −0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)
A port . . . . . −0.5 V to V_{CCA} + 0.5V
B port . . . . . −0.5 V to V_{CCB} + 0.5V
Input clamp current, I_{IK} (V_I < 0) . . . . . −50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −50 mA
Continuous output current, I_O . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DBV package . . . . . 165°C/W
DCK package . . . . . 259°C/W
YEP/YZP package . . . . . 123°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 8)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.65	5.5	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs (see Note 7)	1.65 V to 1.95 V		$V_{CCI} \times 0.65$		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		$V_{CCI} \times 0.7$		
V_{IL}	Low-level input voltage	Data inputs (see Note 7)	1.65 V to 1.95 V			$V_{CCI} \times 0.35$	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			$V_{CCI} \times 0.3$	
V_{IH}	High-level input voltage	DIR (Referenced to V_{CCA}) (see Note 8)	1.65 V to 1.95 V		$V_{CCA} \times 0.65$		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		$V_{CCA} \times 0.7$		
V_{IL}	Low-level input voltage	DIR (Referenced to V_{CCA}) (see Note 8)	1.65 V to 1.95 V			$V_{CCA} \times 0.35$	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			$V_{CCA} \times 0.3$	
V_I	Input voltage				0	5.5	V
V_O	Output voltage				0	V_{CCO}	V
I_{OH}	High-level output current			1.65 V to 1.95 V		−4	mA
				2.3 V to 2.7 V		−8	
				3 V to 3.6 V		−24	
				4.5 V to 5.5 V		−32	
I_{OL}	Low-level output current			1.65 V to 1.95 V		4	mA
				2.3 V to 2.7 V		8	
				3 V to 3.6 V		24	
				4.5 V to 5.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	Data input	1.65 V to 1.95 V			20	ns/V
			2.3 V to 2.7 V			20	
			3 V to 3.6 V			10	
			4.5 V to 5.5 V			5	
		Control input	1.65 V to 5.5 V			5	
T_A	Operating free-air temperature				−40	85	°C

NOTES: 4. V_{CCI} is the V_{CC} associated with the data input port.
5. V_{CCO} is the V_{CC} associated with the output port.
6. All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
7. For V_{CCI} values not specified in the data sheet, $V_{IH(min)} = V_{CCI} \times 0.7$ V, $V_{IL(max)} = V_{CCI} \times 0.3$ V.
8. For V_{CCI} values not specified in the data sheet, $V_{IH(min)} = V_{CCA} \times 0.7$ V, $V_{IL(max)} = V_{CCA} \times 0.3$ V.

PRODUCT PREVIEW

5. NJW1147

AUDIO PROCESSOR with BBE ViVA

■ GENERAL DESCRIPTION

The NJW1147 is a TV audio processor with BBE ViVA High Definition 3D Sound process. BBE's traditional sound clarity enhancement technology is combined with the new ViVA 3D process to create an authentic and exciting spatial effect. BBE ViVA is compatible with news, music and movie programs as well as video games.

The NJW1147 contains all necessary functions to process TV audio signal such as volume control, tone control, balance, mute, AGC and NJRC's proprietary surround sound process, eala. The eala reproduces a natural surround sound with clear vocal orientation.

The total modes and variables are controlled by the I²C bus interface.

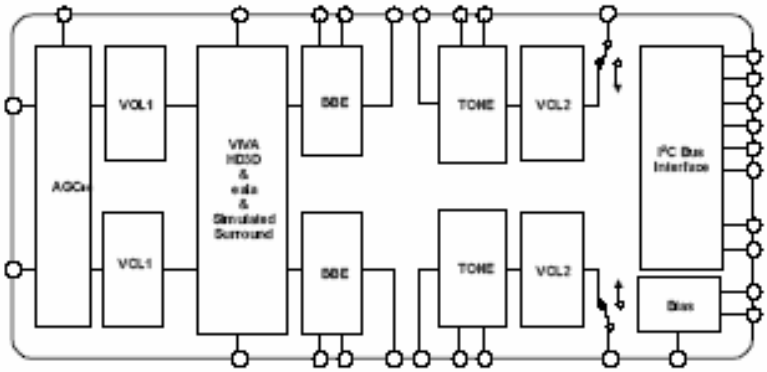
■ PACKAGE OUTLINE

NJW1147M

■ FEATURES

- Operating Voltage 8 to 13V
- I²C BUS Interface
- BBE Sound Enhancement (Low Boost and High Boost: 15dB max.)
- BBE ViVA High Definition 3D Sound
- eala (NJRC Original Surround)
- AGC Circuit (It reduces volume difference among input sources.)
- Simulated Surround
- Bi-CMOS Technology
- Package Outline SDMP30

■ BLOCK DIAGRAM



■ PIN FUNCTION

No.	Symbol	Function	No	Symbol	Function
1	INa	Ach Input	16	Vcc	Power Supply Pin
2	BBE1a	Ach BBE Filter1 (Process)	17	AUX1	Auxiliary Output1
3	BBE2a	Ach BBE Filter2 (Lo Contour)	18	AUX0	Auxiliary Output0
4	BBE OUTa	Ach Output for the Other Accessories	19	CTL	DAC Output for Tone Low Frequency
5	TONE INa	Ach Input From the Other Accessories	20	CTH	DAC Output for Tone High Frequency
6	TONE-Ha	Ach Treble Filter	21	VREF	Reference Voltage
7	TONE-La	Ach Bass Filter	22	SR-FIL	Surround Filter
8	OUTa	Ach Output	23	OUTb	Bch Output
9	AGC	AGC Filter	24	TONE-Lb	Bch Bass Filter
10	SS-FIL	Simulated Stereo Filter	25	TONE-Hb	Bch Treble Filter
11	CVB	DAC Output for Bch Volume & Balance	26	TONE INb	Bch Input from the Other Accessories
12	CVA	DAC Output for Ach Volume & Balance	27	BBE OUTb	Bch Output for the Other Accessories
13	SDA	SDA Data Input (I²C BUS)	28	BBE2b	Bch BBE Filter2 (Process)
14	SCL	SCL Data Input (I²C BUS)	29	BBE1b	Bch BBE Filter1 (Lo Contour)
15	GND	GND	30	INb	Bch Input

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+	14	V
Power Dissipation	P_D	700	mW
Operating Temperature Range	Topr	-20 to +75	°C
Storage Temperature Range	Tstg	-40 to +125	°C

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V+=9V, R_g=600Ω, R_L=47kΩ, Vin=100mVrms/1kHz unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		8.0	9.0	13.0	V
Supply Current	I_{CC}	No Signal	-	13	25	mA
Reference Voltage	V_{REF}	No Signal	4.0	4.5	5.0	V
Maximum Input Voltage	V_{IM}	VOL=-20dB,THD=1%	2.8	3.0	-	Vrms
Maximum Output Voltage	V_{OM}	OUTPUT VOL=0dB,THD=1%	-	2.5	-	Vrms
Channel Balance	G_{CB}	VOL=0dB	-1.5	0.0	1.5	dB
Balance BoostA	BA_{BST}	CHS="0", BAL="11111"	-2.0	0.0	2.0	dB
Balance CutA	BA_{CUT}	CHS="1", BAL="11111" Vin = 1Vrms	-	-	-70	dB
Balance Boost B	BB_{BST}	CHS="1", BAL="11111"	-2.0	0.0	2.0	dB
Balance Cut B	BB_{CUT}	CHS="0", BAL="11111" Vin = 1Vrms	-	-	-70	dB
Total Harmonic Distortion	THD	Vo=0.5Vrms BW=400Hz to 30kHz	-	-	0.5	%
Maximum Gain	G_{MAX}	VOL= 0dB	-2.0	0.0	2.0	dB
Minimum Gain	G_{MIN}	VOL= MUTE	-	-	-70	dB
Channel Separation	CS	Vin = 2Vrms	-	-	-70	dB
Output Noise 1	V_{NO1}	VOL = 0dB BW=400Hz to 30kHz	- -	-90 (31.6)	-85 (56.2)	dBV (μVrms)
Output Noise 2	V_{NO2}	VOL = MUTE BW = 400Hz to 30kHz	- -	-106 (5.0)	-96 (15.8)	dBV (μVrms)
AUX Output Voltage	V_{AUX}	Logic Output: High	4.5	-	5.0	V
		Logic Output: Low	0	-	0.3	

BW: Band Width

♦ TONE CONTROL

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
High Frequency Boost	HF_{BST}	BCT="1", TREB="1111", f=10kHz	12.5	15.0	17.5	dB
High Frequency Flat	HF_{FLT}	TREB="0000", f=10kHz	-2.0	0.0	2.0	dB
High Frequency Cut	HF_{CUT}	BCT="0", TREB="1111", f=10kHz	-17.5	-15.0	-12.5	dB
Low Frequency Boost	LF_{BST}	BCB="1", BASS="1111", f=100Hz	12.5	15.0	17.5	dB
Low Frequency Flat	LF_{FLT}	BASS="0000", f=100Hz	-2.0	0.0	2.0	dB
Low Frequency Cut	LF_{CUT}	BCB="0", BASS="1111", f=100Hz	-17.5	-15.0	-12.5	dB

♦ SUB-TONE CONTROL

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
High Frequency Boost	SHF_{BST}	BCST="1", SUB-TREB="11", f=10kHz	2.0	3.0	4.0	dB
High Frequency Cut	SHF_{CUT}	BCST="0", SUB-TREB="11", f=10kHz	-4.0	-3.0	-2.0	dB
Low Frequency Boost	SLF_{BST}	BCSB="1", SUB-BASS="11", f=100Hz	2.0	3.0	4.0	dB
Low Frequency Cut	SLF_{CUT}	BCSB="0", SUB-BASS="11", f=100Hz	-4.0	-3.0	-2.0	dB

♦ AGC CONTROL

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
AGC Boost	AGC_{BST}	Vin=50mVrms, f=1kHz	1.5	3.5	5.5	dB
AGC Flat1	AGC_{FLT1}	Vin=150mVrms, f=1kHz	-2.5	0.0	2.5	dB
AGC Flat2	AGC_{FLT2}	Vin=300mVrms, f=1kHz	-2.5	0.0	2.5	dB
AGC Flat3	AGC_{FLT3}	Vin=400mVrms, f=1kHz	-2.5	0.0	2.5	dB
AGC Flat4	AGC_{FLT4}	Vin=540mVrms, f=1kHz	-2.5	0.0	2.5	dB
AGC Cut	AGC_{CUT}	Vin=2Vrms, f=1kHz	-14	-10	-8.0	dB

♦ BBE

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
BBE Low Frequency Boost Range	BBE_{LOW}	BBE-Low="1111", f = 50Hz	-	15.0	-	dB
BBE High Frequency Boost Range	BBE_{HIGH}	BBE-High="1111", f = 10KHz	-	15.0	-	dB

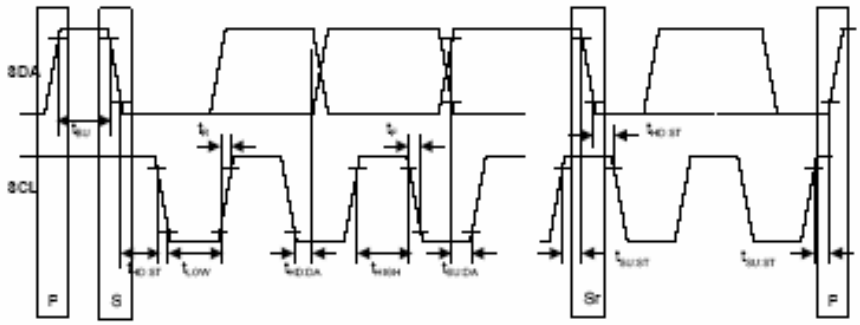
♦ SURROUND (SURROUND-ON)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Surround Gain1	SR_{GAIN1}	Ain→Aout, f=100Hz SUR0="0", SUR="1"	3.5	5.5	7.5	dB
Surround Gain2	SR_{GAIN2}	Ain→Bout, f=100Hz SUR0="0", SUR="1"	-3.0	-1.0	1.0	dB
Surround Gain3	SR_{GAIN3}	Ain→Aout, f=100Hz SUR0="1", SUR="1"	8.0	10.0	12.0	dB
Surround Gain4	SR_{GAIN4}	Ain→Bout, f=100Hz SUR0="1", SUR="1"	5.0	7.0	9.0	dB
Simulated Surround Gain1	SR_{SIM1}	Ain+Bin→Aout, f=1kHz SUR0="1", SUR="0"	1.0	3.0	5.0	dB
Simulated Surround Gain2	SR_{SIM2}	Ain+Bin→Bout, f=1kHz SUR0="1", SUR="0"	1.0	3.0	5.0	dB

■ I²C BUS BLOCK CHARACTERISTICS (SDA, SCL)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
High Level Input Voltage	V_{IH}	3.0	-	5.0	V
Low Level Input Voltage	V_{IL}	0	-	1.5	V
High Level Input Current	I_{IH}	-	-	10	μA
Low Level Input Current	I_{IL}	-	-	10	μA
Low Level Output Voltage (3mA at SDA pin)	V_{OL}	0	-	0.4	V
Maximum Output Current	I_{OL}	-3.0	-	-	mA
Maximum Clock Frequency	f_{SCL}	0	-	100	kHz
Data Change Minimum Waiting Time	t_{BUF}	4.7	-	-	μs
Data Transfer Start Minimum Waiting Time	$t_{HD:STA}$	4.0	-	-	μs
Low Level Clock Pulse Width	t_{LOW}	4.7	-	-	μs
High Level Clock Pulse Width	T_{HIGH}	4.0	-	-	μs
Minimum Start Preparation Waiting Time	$t_{SU:STA}$	4.7	-	-	μs
Minimum Data Hold Time	$t_{HD:DAT}$	5.0	-	-	μs
Minimum Data Preparation Time	$t_{SU:DAT}$	250	-	-	ns
Rise Time	t_R	-	-	1.0	μs
Fall Time	t_F	-	-	300	ns
Minimum Stop Preparation Waiting Time	$t_{SU:STO}$	4.7	-	-	μs

I²C BUS Load Condition: Pull up resistance 4kΩ (Connected to +5V)
Load capacitance 200pF (Connected to GND)



6. MSP3410G-QA-B8-V3

Multistandard Sound Processor Family

Release Note: Revision bars indicate significant changes to the previous edition. The hardware and software description in this document is valid for the MSP 34x0G version B5 and following versions.

1. Introduction

The MSP 34x0G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Figure 1–1 shows a simplified functional block diagram of the MSP 34x0G.

This new generation of TV sound processing ICs now includes versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free.

Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP 34x0G has optimum stereo performance without any adjustments.

All MSP 34x0G versions are pin and software downward-compatible to the MSP 34x0D. The MSP 34x0G further simplifies controlling software. Standard selection requires a single I^2C transmission only.

The MSP 34x0G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/stereo/bilingual; no I^2C interaction is necessary (Automatic Sound Selection).

The ICs are produced in submicron CMOS technology. The MSP 34x0G is available in the following packages: PLCC68, PSDIP64, PSDIP52, PQFP80, and PLQFP64.

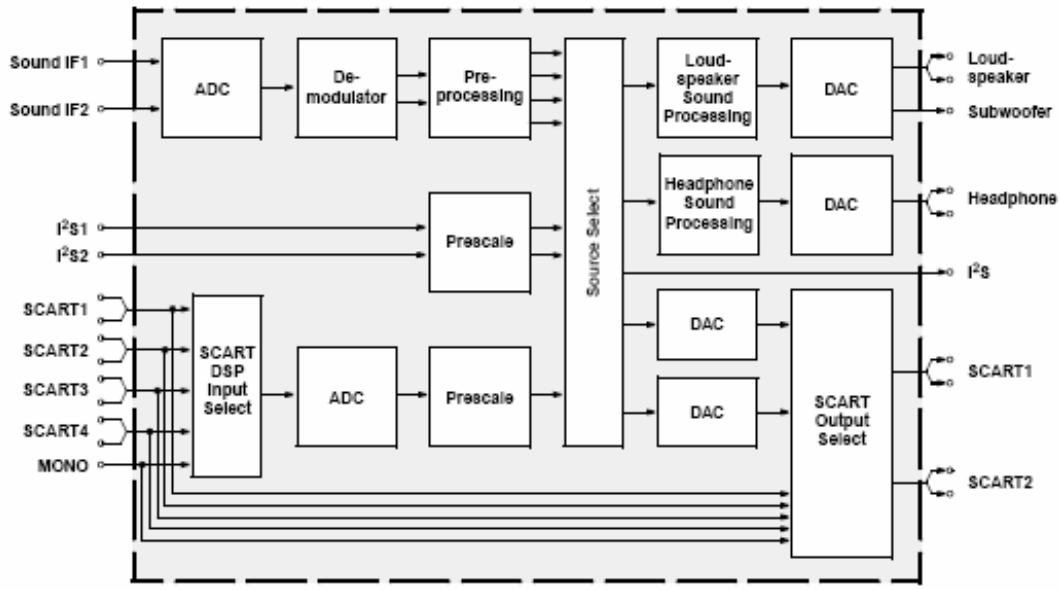


Fig. 1–1: Simplified functional block diagram of the MSP 34x0G

Table 2–1: Performed actions of the Automatic Sound Selection

Selected TV Sound Standard	Performed Actions
B/G-FM, D/K-FM, M-Korea, and M-Japan	Evaluation of the identification signal and automatic switching to mono, stereo, or bilingual. Preparing four demodulator source channels according to Table 2–2. Identification is acquired after 500 ms.
B/G-NICAM, L-NICAM, I-NICAM, and D/K-NICAM	Evaluation of NICAM-C-bits and automatic switching to mono, stereo, or bilingual. Preparing four demodulator source channels according to Table 2–2. NICAM detection is acquired within 150 ms.
	In case of bad or no NICAM reception, the MSP switches automatically to FM/AM mono and switches back to NICAM if possible. A hysteresis prevents periodical switching.
B/G-FM, B/G-NICAM or D/K1-FM, D/K2-FM, D/K3-FM, and D/K-NICAM	Automatic searching for stereo/bilingual-identification in case of mono transmission. Automatic and non-audible changes between Dual-FM and FM-NICAM standards while listening to the basic FM-Mono sound carrier. Example: If starting with B/G-FM-Stereo, there will be a periodical alternation to B/G-NICAM in the absence of FM-Stereo/Bilingual or NICAM-identification. Once an identification is detected, the MSP keeps the corresponding standard.
BTSC-STEREO, FM Radio	Evaluation of the pilot signal and automatic switching to mono or stereo. Preparing four demodulator source channels according to Table 2–2. Detection of the SAP carrier. Pilot detection is acquired after 200 ms.
BTSC-SAP	In the absence of SAP, the MSP switches to BTSC-Stereo if available. If SAP is detected, the MSP switches automatically to SAP (see Table 2–2).

Table 2–2: Sound modes for the demodulator source channels with Automatic Sound Select

			Source Channels in Automatic Sound Select Mode			
Broadcasted Sound Standard	**Selected MSP Standard Code[3)]**	**Broadcasted Sound Mode**	**FM/AM** (source select: 0)	**Stereo or A/B** (source select: 1)	**Stereo or A** (source select: 3)	**Stereo or B** (source select: 4)
M-Korea B/G-FM D/K-FM M-Japan	02 03, 08[1)] 04, 05, 07, 0B[1)] 30	MONO	Mono	Mono	Mono	Mono
		STEREO	Stereo	Stereo	Stereo	Stereo
		BILINGUAL: Languages A and B	Left = A Right = B	Left = A Right = B	A	B
B/G-NICAM L-NICAM I-NICAM D/K-NICAM D/K-NICAM (with high deviation FM)	08, 03[2)] 09 0A 0B, 04[2)], 05[2)] 0C	NICAM not available or error rate too high	analog Mono	analog Mono	analog Mono	analog Mono
		MONO	analog Mono	NICAM Mono	NICAM Mono	NICAM Mono
		STEREO	analog Mono	NICAM Stereo	NICAM Stereo	NICAM Stereo
		BILINGUAL: Languages A and B	analog Mono	Left = NICAM A Right = NICAM B	NICAM A	NICAM B
BTSC	20, 21	MONO	Mono	Mono	Mono	Mono
		STEREO	Stereo	Stereo	Stereo	Stereo
	20	MONO+SAP	Mono	Mono	Mono	Mono
		STEREO+SAP	Stereo	Stereo	Stereo	Stereo
	21	MONO+SAP	Left = Mono Right = SAP	Left = Mono Right = SAP	Mono	SAP
		STEREO+SAP	Left = Mono Right = SAP	Left = Mono Right = SAP	Mono	SAP
FM Radio	40	MONO	Mono	Mono	Mono	Mono
		STEREO	Stereo	Stereo	Stereo	Stereo

[1)] The Automatic Sound Select process will automatically switch to the mono compatible analog standard.
[2)] The Automatic Sound Select process will automatically switch to the mono compatible digital standard.
[3)] The MSP Standard Codes are defined in Table 3–7 on page 22.

2.4. Source Selection and Output Channel Matrix

The Source Selector makes it possible to distribute all source signals (one of the demodulator source channels, SCART, or I^2S input) to the desired output channels (loudspeaker, headphone, etc.). All input and output signals can be processed simultaneously. Each source channel is identified by a unique source address.

For each output channel, the sound mode can be set to sound A, sound B, stereo, or mono by means of the output channel matrix.

If Automatic Sound Select is on, the output channel matrix can stay fixed to stereo (transparent) for demodulated signals.

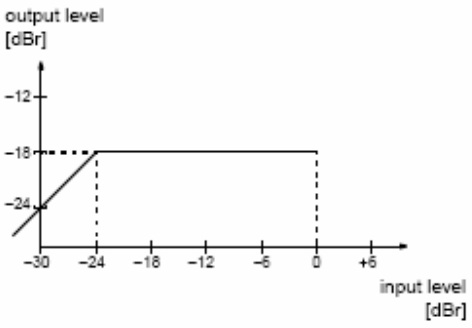


Fig. 2–4: Simplified AVC characteristics

2.5. Audio Baseband Processing

2.5.1. Automatic Volume Correction (AVC)

Different sound sources (e.g. terrestrial channels, SAT channels, or SCART) fairly often do not have the same volume level. Advertisements during movies usually have a higher volume level than the movie itself. This results in annoying volume changes. The Automatic Volume Correction (AVC) solves this problem by equalizing the volume level.

To prevent clipping, the AVC's gain decreases quickly in dynamic boost conditions. To suppress oscillation effects, the gain increases rather slowly for low level inputs. The decay time is programmable by means of the AVC register (see page 31).

For input signals ranging from –24 dBr to 0 dBr, the AVC maintains a fixed output level of –18 dBr. Fig. 2–4 shows the AVC output level versus its input level. For prescale and volume registers set to 0 dB, a level of 0 dBr corresponds to full scale input/output. This is

- SCART input/output 0 dBr = 2.0 V_{rms}
- Loudspeaker and Aux output 0 dBr = 1.4 V_{rms}

2.6. SCART Signal Routing

2.6.1. SCART DSP In and SCART Out Select

The SCART DSP Input Select and SCART Output Select blocks include full matrix switching facilities. To design a TV set with four pairs of SCART-inputs and two pairs of SCART-outputs, no external switching hardware is required. The switches are controlled by the ACB user register (see page 37).

2.6.2. Stand-by Mode

If the MSP 34x0G is switched off by first pulling STANDBYQ low and then (after >1 µs delay) switching off the 5-V, but keeping the 8-V power supply (**'Stand-by'-mode**), the SCART switches maintain their position and function. This allows the copying from selected SCART-inputs to SCART-outputs in the TV set's stand-by mode.

In case of power on or starting from stand-by (switching on the 5-V supply, RESETQ going high 2 ms later), all internal registers except the ACB register (page 37) are reset to the default configuration (see Table 3–5 on page 20). The reset position of the ACB register becomes active after the first I^2C transmission into the Baseband Processing part (subaddress 12_{hex}). By transmitting the ACB register first, the reset state can be redefined.

2.5.2. Loudspeaker and Headphone Outputs

The following baseband features are implemented in the loudspeaker and headphone output channels: bass/treble, loudness, balance, and volume. A square wave beeper can be added to the loudspeaker and headphone channel. The loudspeaker channel additionally performs: equalizer (not simultaneously with bass/treble), spatial effects, and a subwoofer crossover filter.

2.5.3. Subwoofer Output

The subwoofer signal is created by combining the left and right channels directly behind the loudness block using the formula (L+R)/2. Due to the division by 2, the D/A converter will not be overloaded, even with full scale input signals. The subwoofer signal is filtered by a third-order low-pass with programmable corner frequency followed by a level adjustment. At the loudspeaker channels, a complementary high-pass filter can be switched on. Subwoofer and loudspeaker output use the same volume (Loudspeaker Volume Register).

2.7. I^2S Bus Interface

It is possible to route in an external coprocessor for special effects, like surround processing and sound field processing. Routing can be done with each input source and output channel via the I^2S inputs and outputs.

Two possible interface formats are supported:

1. The SONY format: I2S_WS changes at the word boundaries.
2. The PHILIPS format: I2S_WS changes one I2S_CL period before the word boundaries.

The I^2S bus interface consists of five pins:

1. I2S_DA_IN1, I2S_DA_IN2:
   For input, four channels (two channels per line, 2*16 bits) per sampling cycle (32 kHz) are transmitted.
2. I2S_DA_OUT:
   For output, two channels (2*16 bits) per sampling cycle (32 kHz) are transmitted.
3. I2S_CL:
   Gives the timing for the transmission of I^2S serial data (1.024 MHz).
4. I2S_WS:
   The I2S_WS word strobe line defines the left and right sample.

The MSP 34x0G normally serves as the master on the I^2S interface. In this case, the clock and word strobe lines are driven by the MSP 34x0G. In slave mode, these lines are input to the MSP 34x0G and the master clock is synchronized to 576 times the I2S_WS rate (32 kHz). NICAM operation is not possible in this mode.

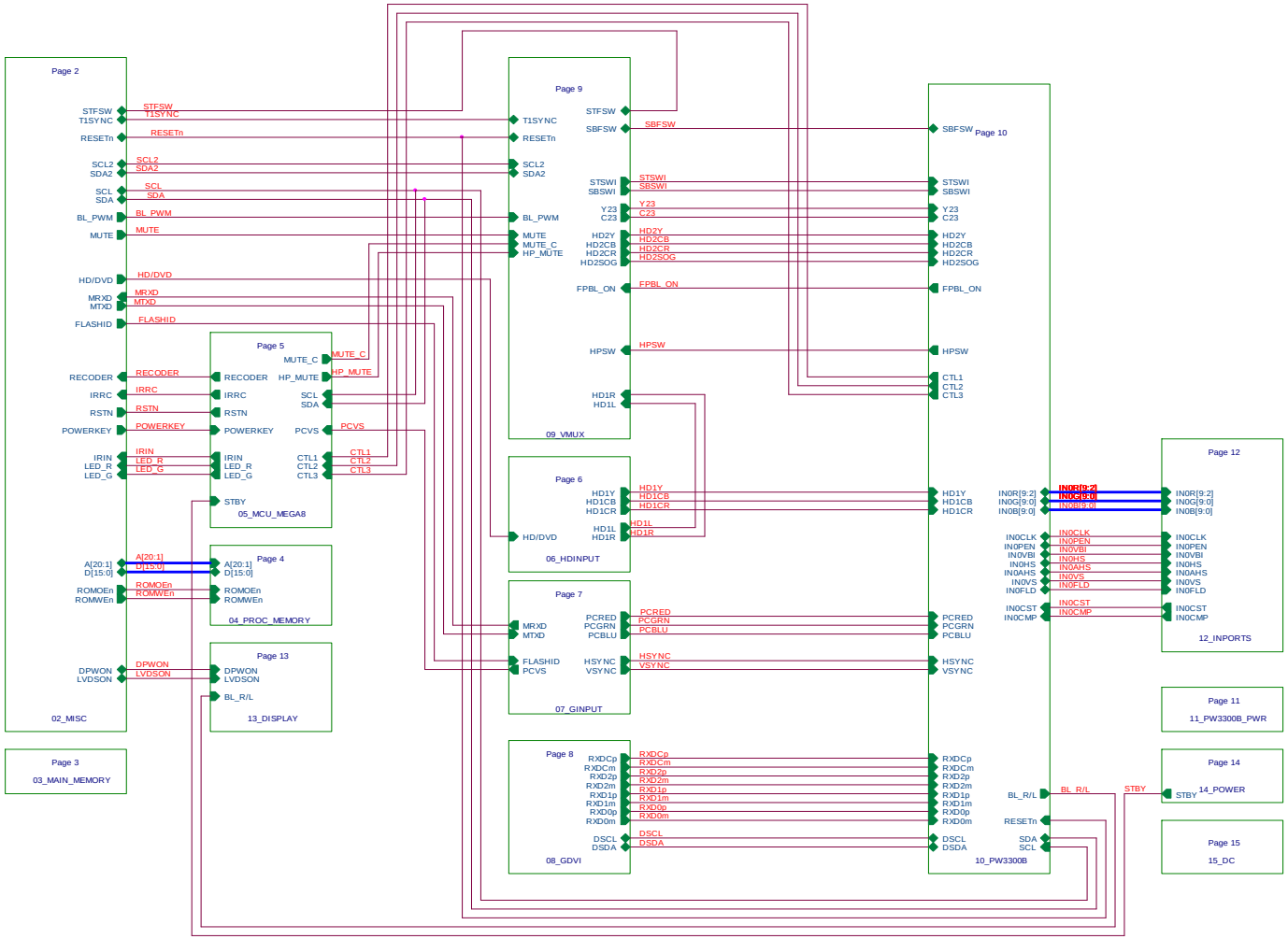
All I^2S options can be set by means of the MODUS register (see page 25).

A precise I^2S timing diagram is shown in Fig. 4–26 on page 65.

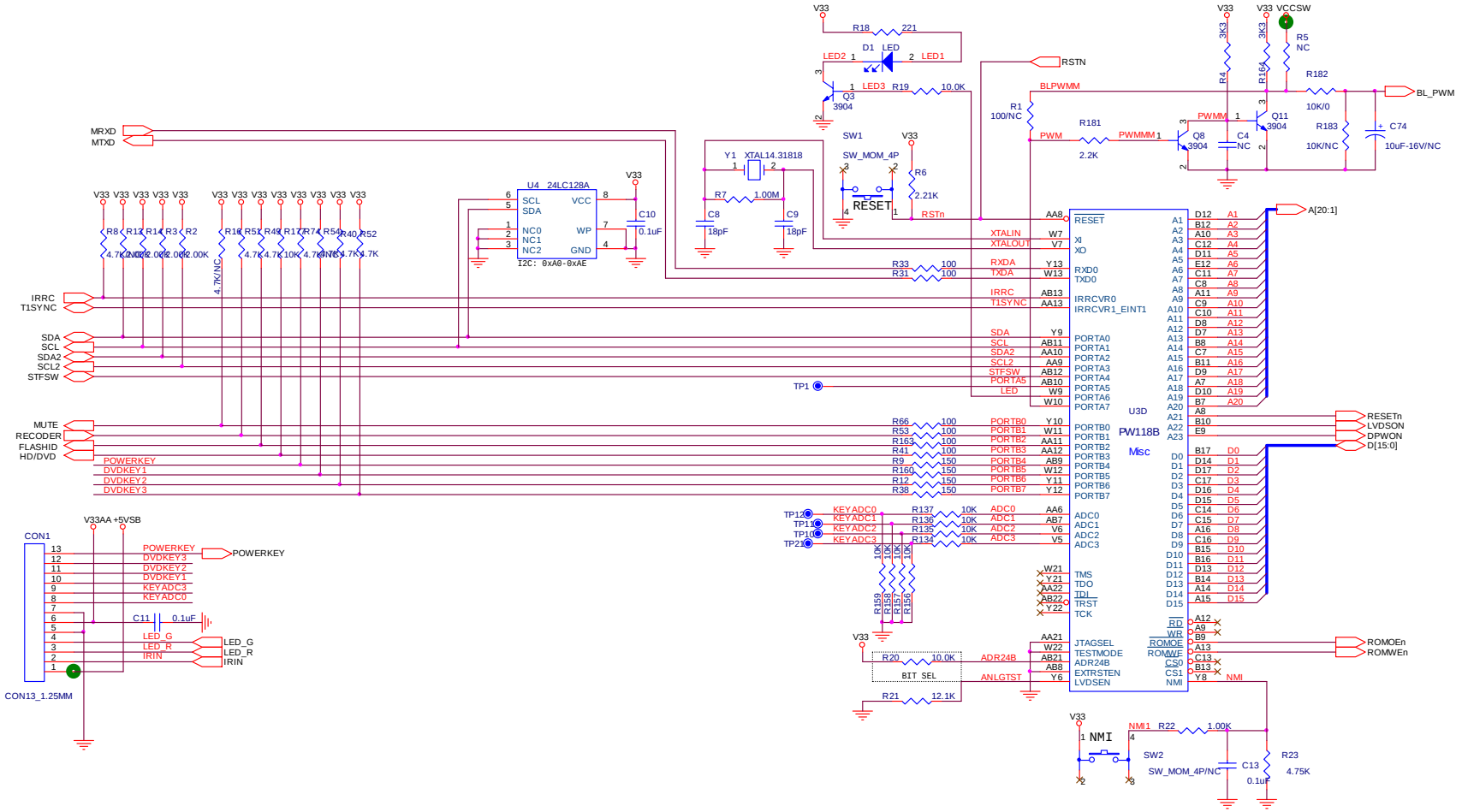
Part 4 Detailed Circuit

MAIN BOARD

1. TOP

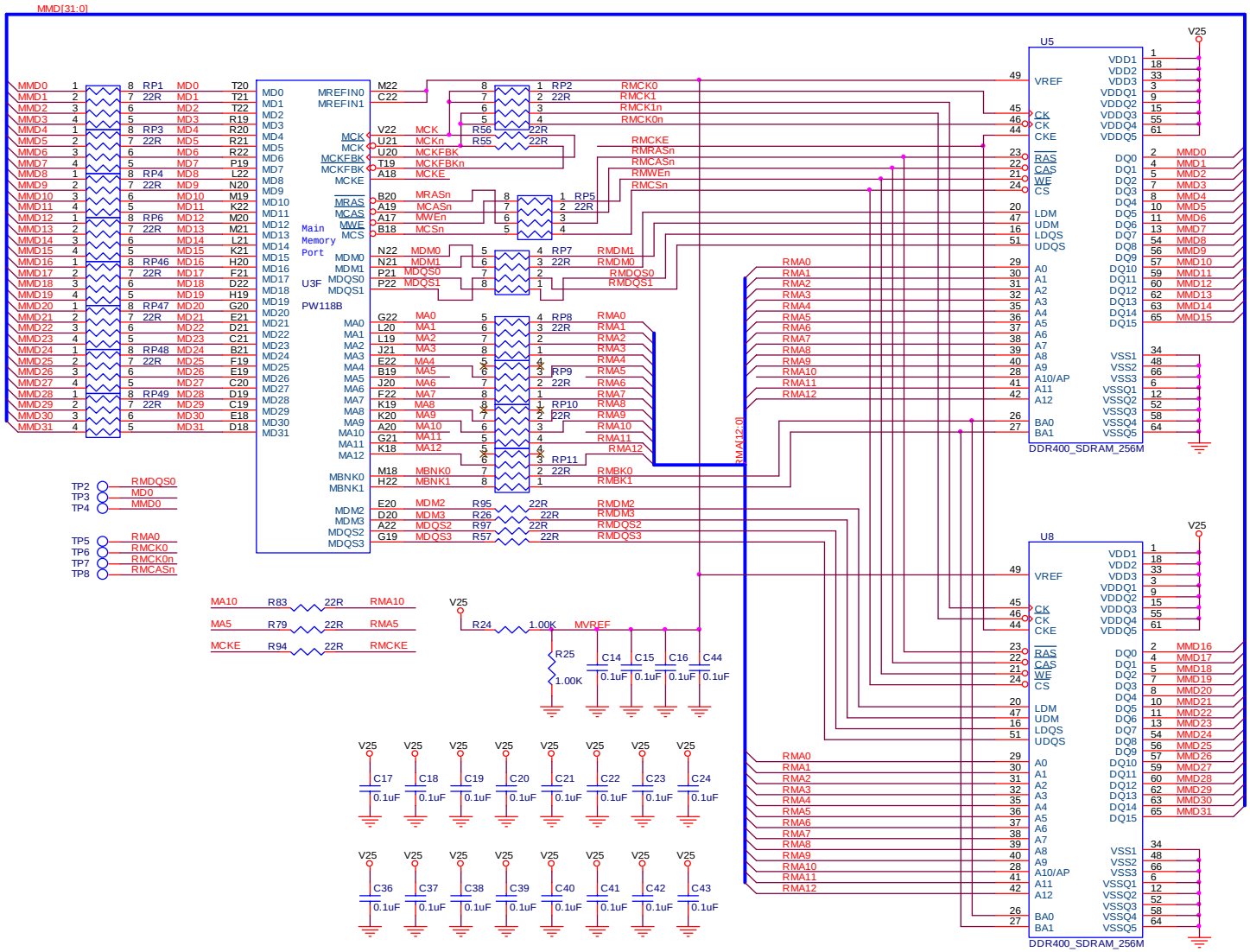


2. MISC

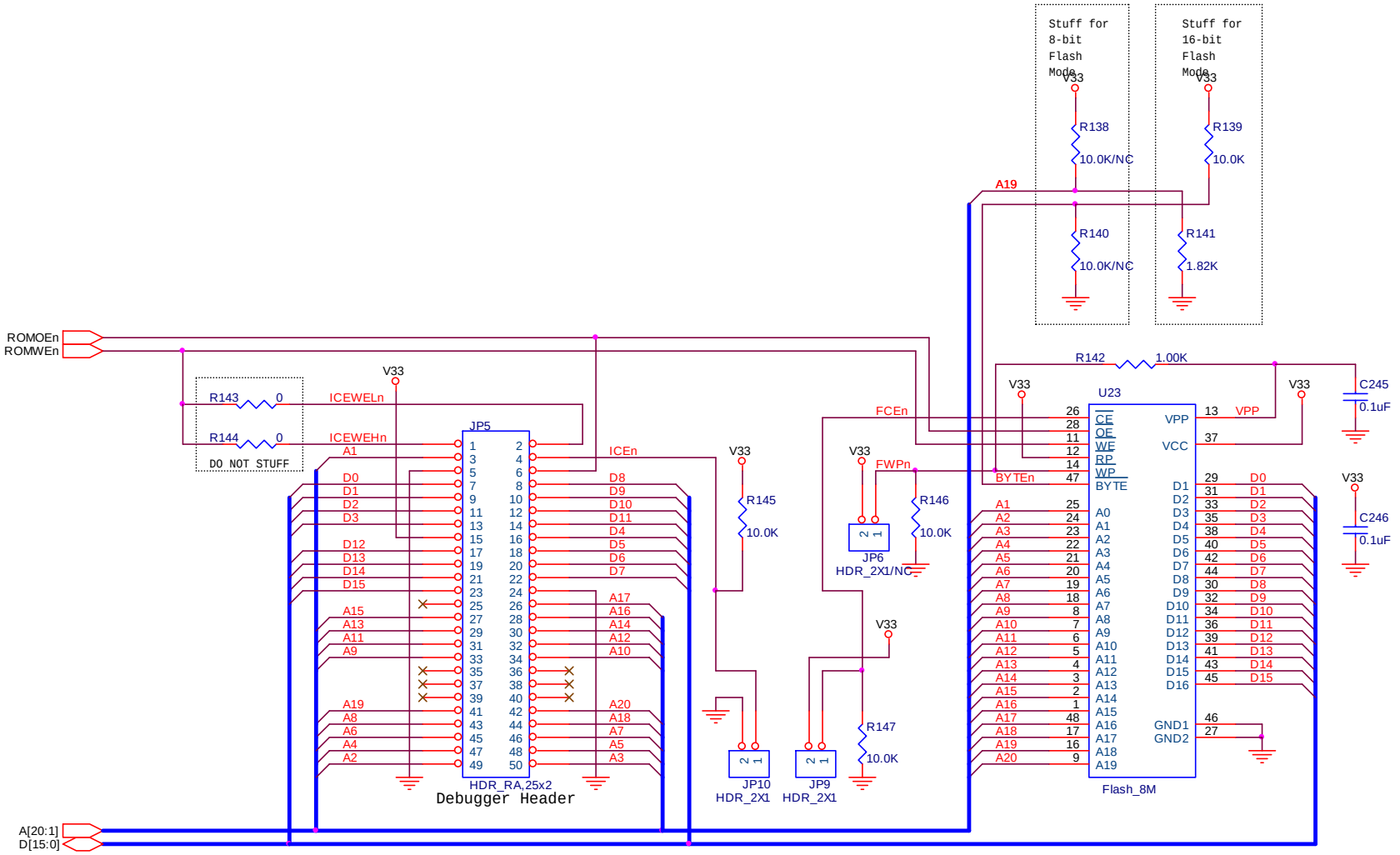


V33
R18 221
D1 LED
LED2
LED1
LED3
R19 10.0K
Q3 3904
RSTN
BLPWMM
R1 100/NC
R181 2.2K
PWM
PWMMM
Q8 3904
C4 NC
Q11 3904
R4 3K3
R164 3K3
VCCSW
R5 NC
R182 10K/0
R183 10K/NC
C74 10uF-16V/NC
BL_PWM
MRXD
MTXD
Y1 XTAL14.31818
R7 1.00M
C8 18pF
C9 18pF
SW1 SW_MOM_4P
RESET
R6 2.21K
RSTn
U4 24LC128A
SCL
SDA
NC0
NC1
NC2
VCC
WP
GND
I2C: 0xA0-0xAE
C10 0.1uF
R8 R13 R14 R3 R2
R16 R51 R49 R17 R74 R54 R40 R52
4.7K/NC
IRRC
T1SYNC
SDA
SCL
SDA2
SCL2
STFSW
MUTE
RECODER
FLASHID
HD/DVD
POWERKEY
DVDKEY1
DVDKEY2
DVDKEY3
TP1
XTALIN
XTALOUT
RXDA
TXDA
IRRC
T1SYNC
SDA
SCL
SDA2
SCL2
STFSW
PORTA5
LED
R33 100
R31 100
RESET
XI
XO
RXD0
TXD0
IRRCVR0
IRRCVR1_EINT1
PORTA0
PORTA1
PORTA2
PORTA3
PORTA4
PORTA5
PORTA6
PORTA7
U3D
PW118B
Misc
A[20:1]
RESETn
LVDSON
DPWON
D[15:0]
PORTB0
PORTB1
PORTB2
PORTB3
PORTB4
PORTB5
PORTB6
PORTB7
R66 100
R53 100
R163 100
R41 100
R9 150
R160 150
R12 150
R38 150
TP12
TP11
TP10
TP21
KEYADC0
KEYADC1
KEYADC2
KEYADC3
R137 10K
R136 10K
R135 10K
R134 10K
ADC0
ADC1
ADC2
ADC3
R159 10K
R158 10K
R157 10K
R156 10K
TMS
TDO
TDI
TRST
TCK
JTAGSEL
TESTMODE
ADR24B
EXTRSTEN
LVDSEN
RD
WR
ROMOE
ROMWE
CS0
CS1
NMI
ROMOEn
ROMWEn
R20 10.0K
BIT SEL
ADR24B
ANLGTST
R21 12.1K
V33AA +5VSB
CON1
CON13_1.25MM
POWERKEY
DVDKEY3
DVDKEY2
DVDKEY1
KEYADC3
KEYADC0
C11 0.1uF
LED_G
LED_R
IRIN
NMI1
R22 1.00K
SW2 SW_MOM_4P/NC
C13 0.1uF
R23 4.75K

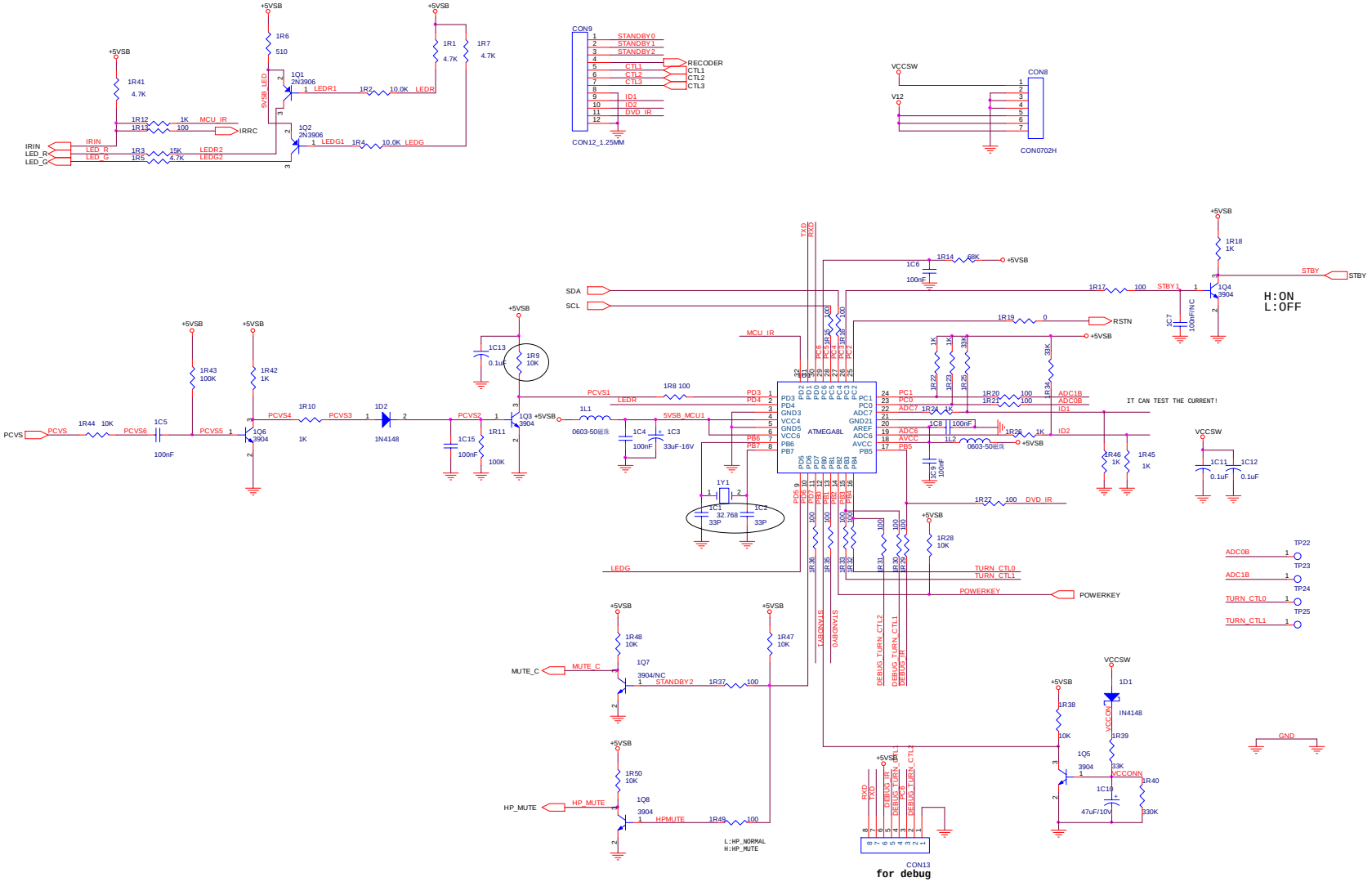
3. MAIN_MEMORY



4. PROC_MEMORY

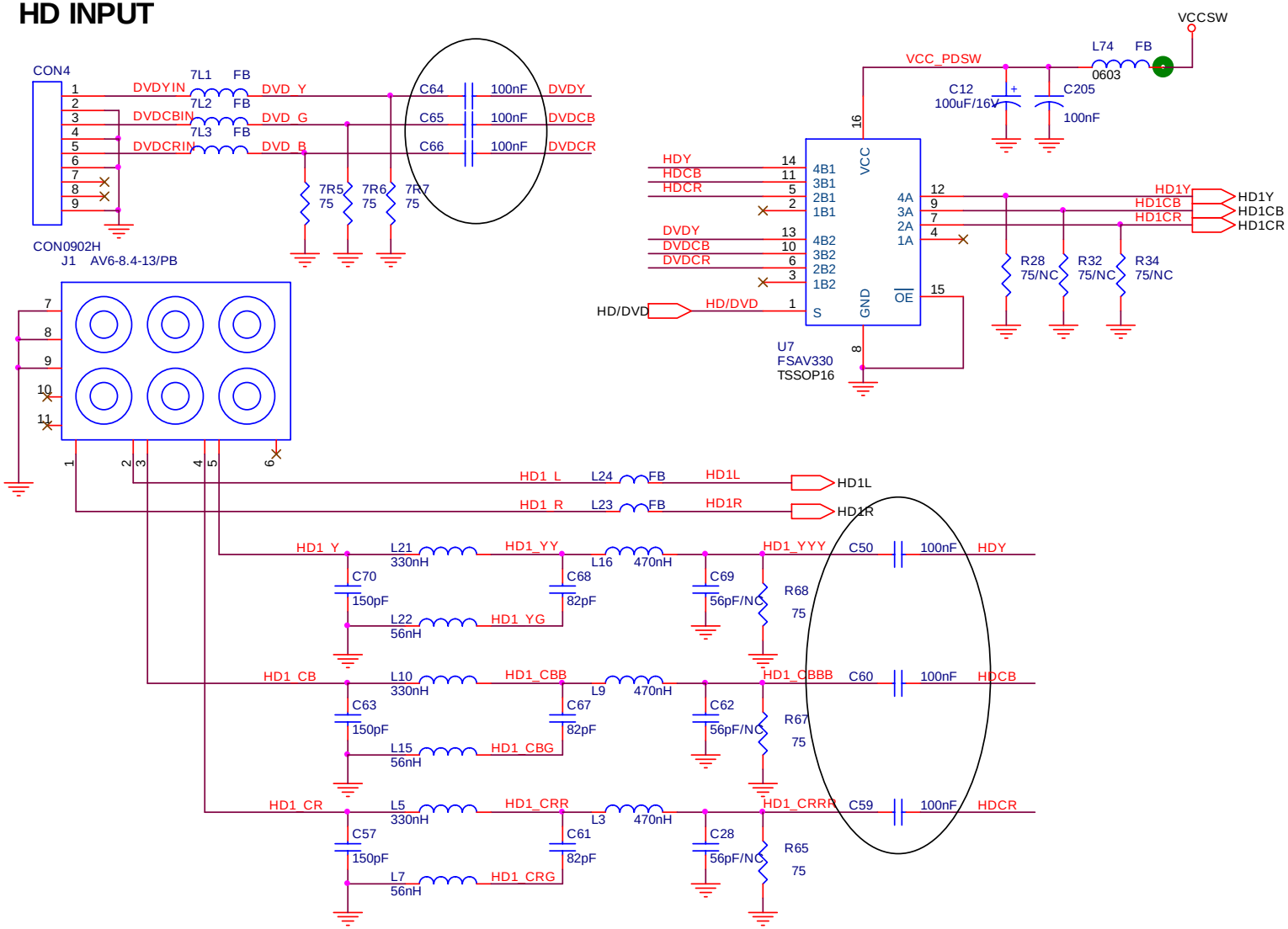


5. MCU MEGA8


+5VSB
1R6
510
1R1
4.7K
1R7
4.7K
1R41
4.7K
1Q1
2N3906
LEDR1
1R2
10.0K
LEDR
5VSB_LED
1R12
1K
MCU_IR
1R13
100
IRRC
1Q2
2N3906
LEDG1
1R4
10.0K
LEDG
IRIN
LED_R
LED_G
1R3
15K
LEDR2
1R5
4.7K
LEDG2
CON9
STANDBY0
STANDBY1
STANDBY2
CTL1
CTL2
CTL3
ID1
ID2
DVD_IR
RECODER
CTL1
CTL2
CTL3
CON12_1.25MM
VCCSW
V12
CON8
CON0702H
SDA
SCL
MCU_IR
1R14
68K
1C6
100nF
1R17
100
STBY1
1Q4
3904
1R18
1K
STBY
H:ON
L:OFF
1R19
0
RSTN
1C7
100nF/NC
1R22
1K
1R23
1K
1R25
33K
1R39
33K
1R20
100
1R21
100
ADC1B
ADC0B
ID1
IT CAN TEST THE CURRENT!
1R24
1K
1C8
100nF
1R26
1K
ID2
1L2
0603-50磁珠
1C9
100nF
1R46
1K
1R45
1K
VCCSW
1C11
0.1uF
1C12
0.1uF
1R43
100K
1R42
1K
1R10
1K
1D2
1N4148
PCVS
1R44
10K
1C5
100nF
1Q6
3904
PCVS1
PCVS2
PCVS3
PCVS4
PCVS5
PCVS6
1C13
0.1uF
1R9
10K
1Q3
3904
1L1
0603-50磁珠
1R8
100
LEDR
5VSB_MCU1
1C4
100nF
1C3
33uF-16V
1C15
100nF
1R11
100K
ATMEGA8L
1Y1
8.768
1C1
33P
1C2
33P
1R27
100
DVD_IR
1R28
10K
TURN_CTL0
TURN_CTL1
POWERKEY
LEDG
TP22
TP23
TP24
TP25
ADC0B
ADC1B
TURN_CTL0
TURN_CTL1
GND
1R48
10K
1Q7
3904/NC
MUTE_C
STANDBY2
1R37
100
1R47
10K
1R50
10K
1Q8
3904
HP_MUTE
HPMUTE
1R49
100
L:HP_NORMAL
H:HP_MUTE
STANDBY1
STANDBY0
DEBUG_TURN_CTL2
DEBUG_TURN_CTL1
DEBUG_IR
RXD
TXD
CON13
for debug
1D1
IN4148
VCCON
1R38
10K
1Q5
3904
1R39
33K
VCCONN
1C10
47uF/10V
1R40
330K

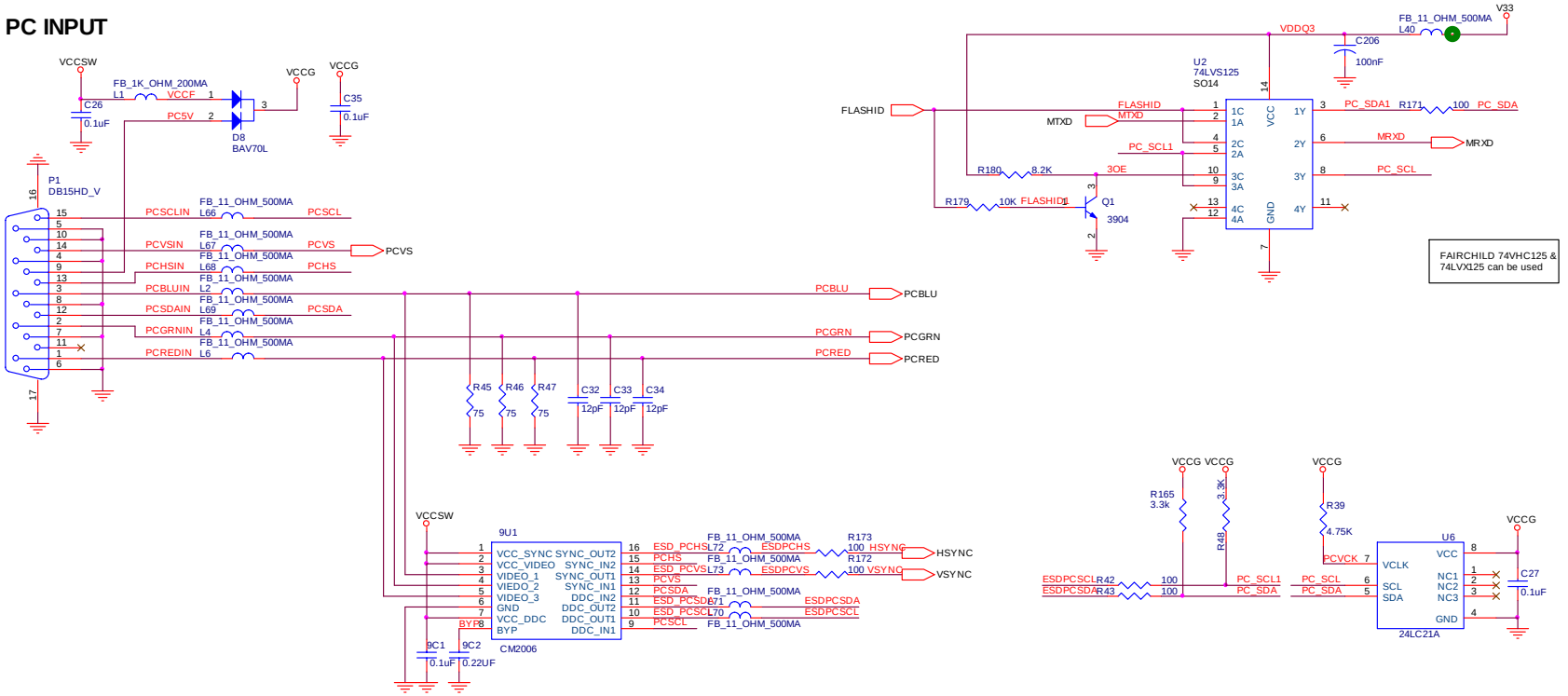
6. HDINPUT

HD INPUT

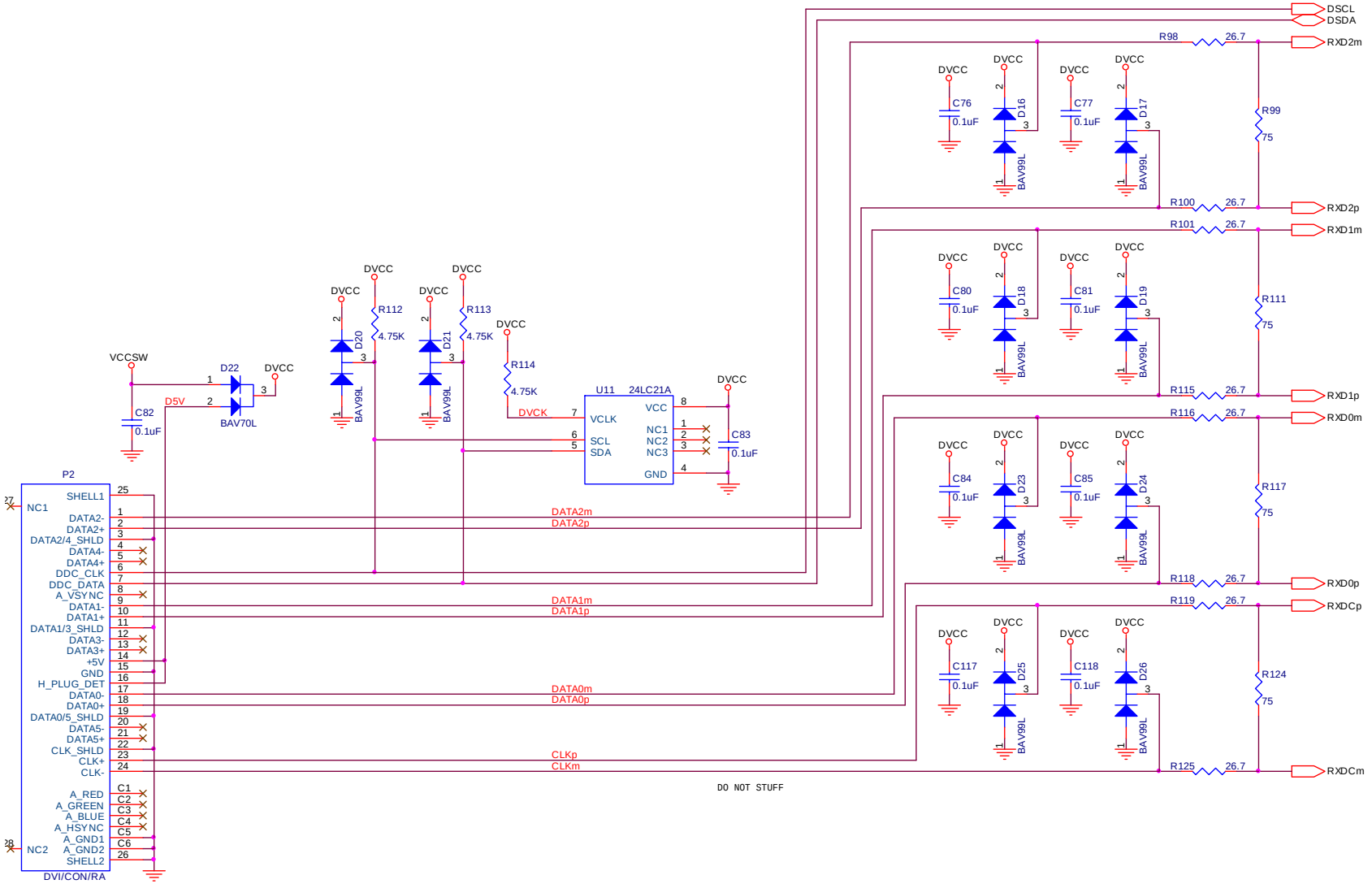


7. GINPUT

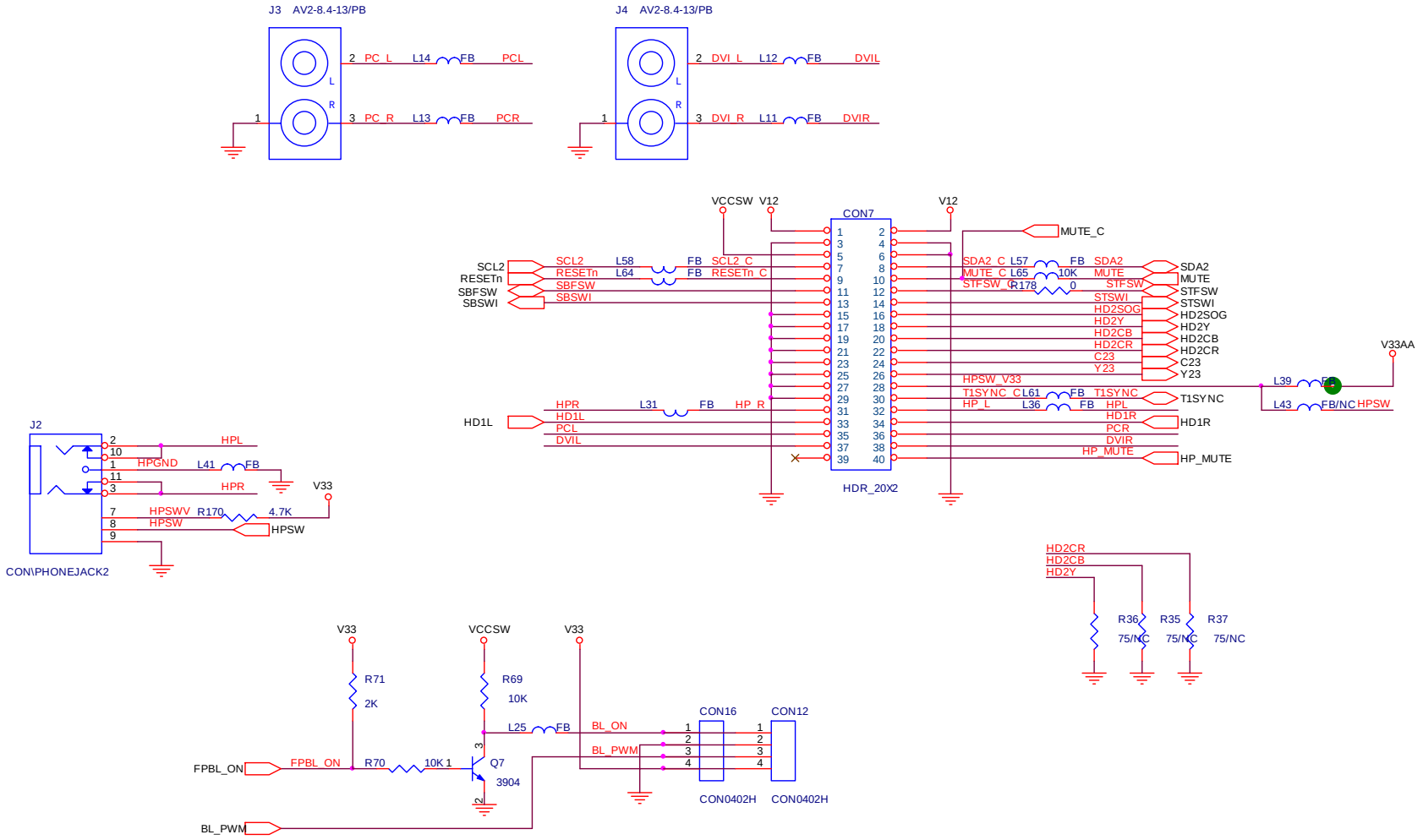
PC INPUT



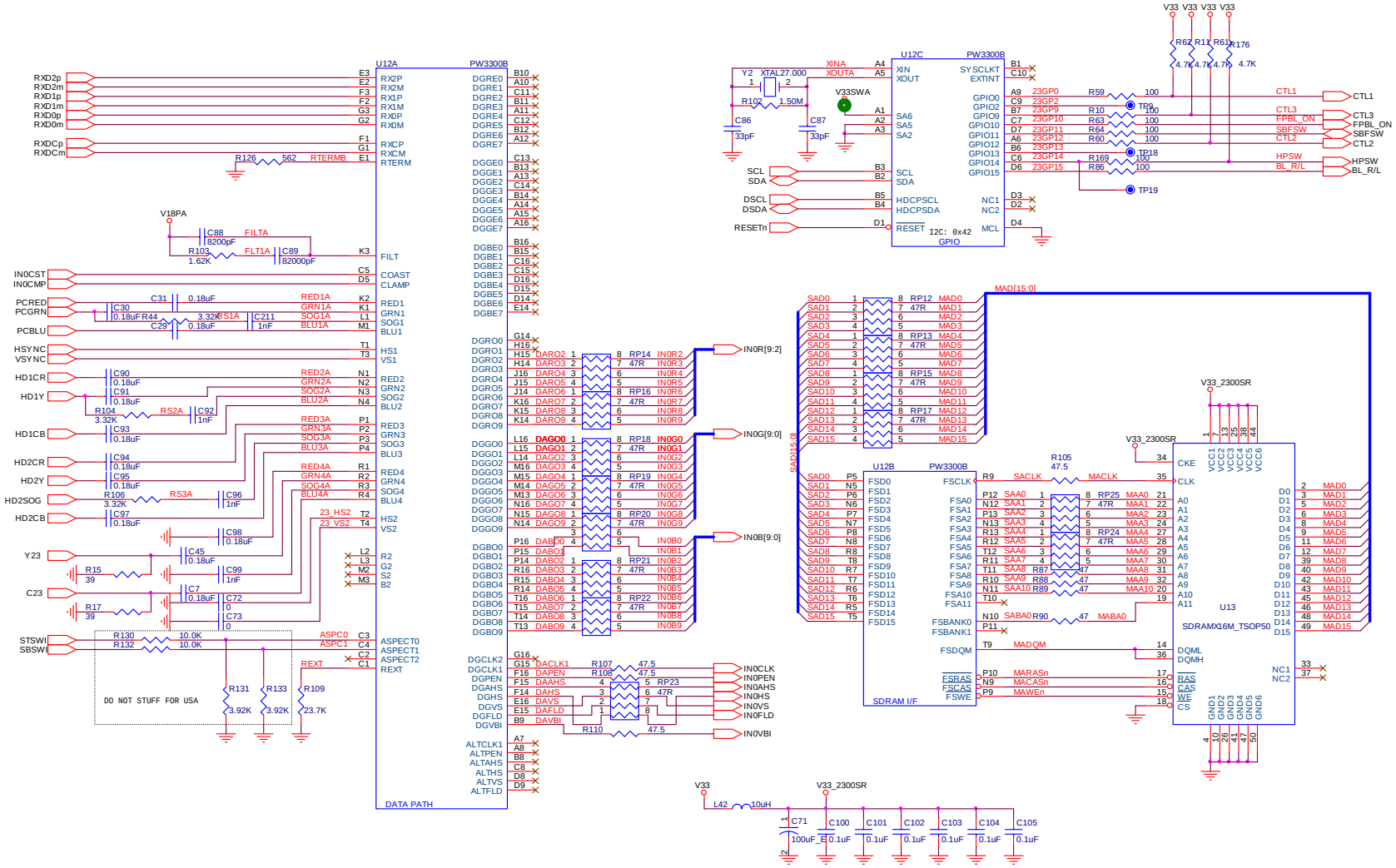
8. GDVI


DSCL
DSDA
RXD2m
RXD2p
RXD1m
RXD1p
RXD0m
RXD0p
RXDCp
RXDCm
DVCC
VCCSW
D5V
D22
BAV70L
C82
0.1uF
R112
4.75K
R113
4.75K
R114
4.75K
D20
D21
BAV99L
U11
24LC21A
VCLK
SCL
SDA
DVCK
VCC
NC1
NC2
NC3
GND
C83
P2
SHELL1
NC1
DATA2-
DATA2+
DATA2/4_SHLD
DATA4-
DATA4+
DDC_CLK
DDC_DATA
A_VSYNC
DATA1-
DATA1+
DATA1/3_SHLD
DATA3-
DATA3+
+5V
GND
H_PLUG_DET
DATA0-
DATA0+
DATA0/5_SHLD
DATA5-
DATA5+
CLK_SHLD
CLK+
CLK-
A_RED
A_GREEN
A_BLUE
A_HSYNC
A_GND1
A_GND2
SHELL2
NC2
DVI/CON/RA
DATA2m
DATA2p
DATA1m
DATA1p
DATA0m
DATA0p
CLKp
CLKm
DO NOT STUFF
R98
R99
R100
R101
R111
R115
R116
R117
R118
R119
R124
R125
26.7
75
C76
C77
C80
C81
C84
C85
C117
C118
D16
D17
D18
D19
D23
D24
D25
D26

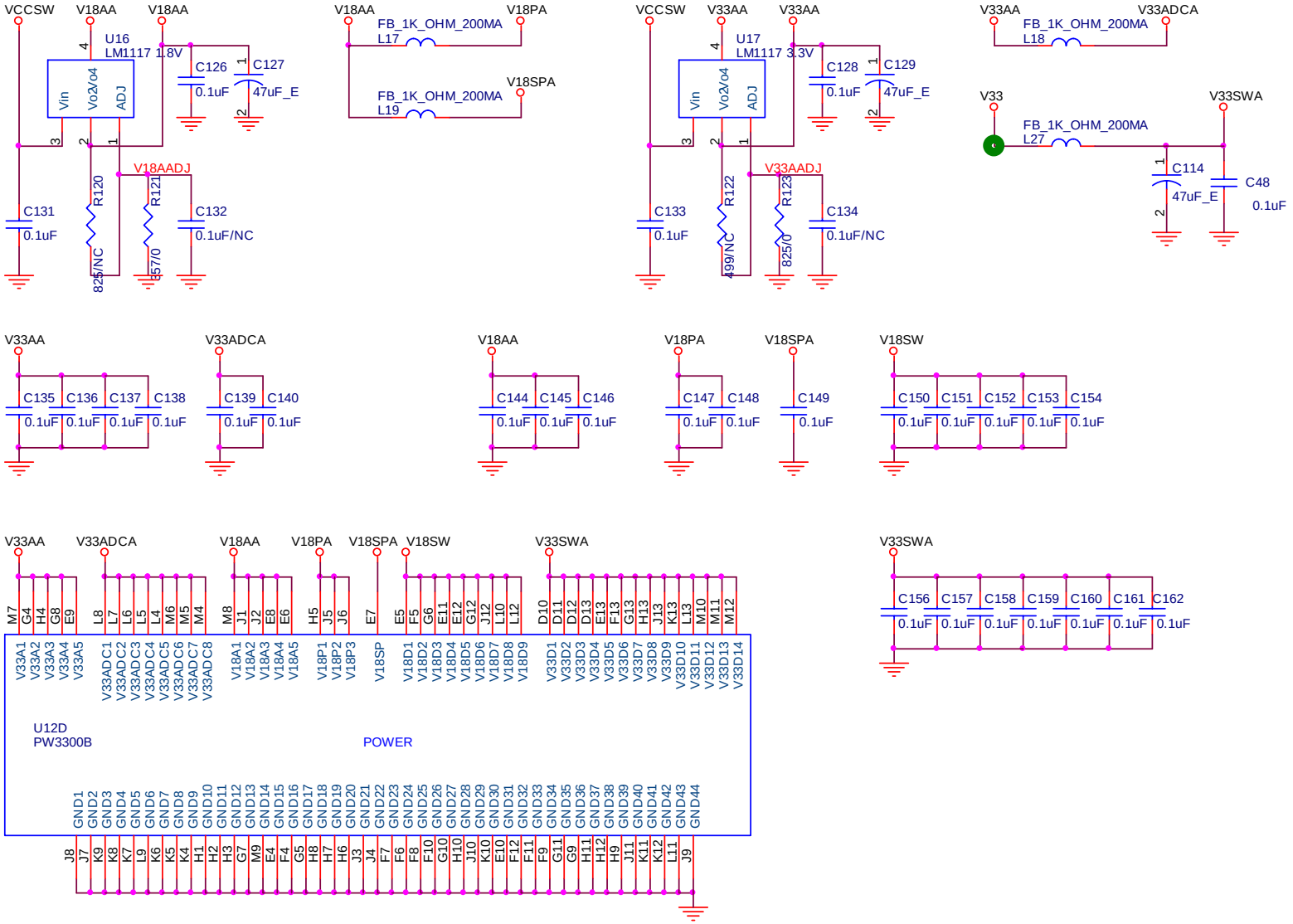
9. VMUX


J3 AV2-8.4-13/PB
J4 AV2-8.4-13/PB
PC_L L14 FB PCL
PC_R L13 FB PCR
DVI_L L12 FB DVIL
DVI_R L11 FB DVIR
VCCSW V12
V12
CON7
HDR_20X2
MUTE_C
SCL2 L58 FB SCL2_C
RESETn L64 FB RESETn_C
SBFSW
SBSWI
SDA2_C L57 FB SDA2
MUTE_C L65 10K MUTE
STFSW_C R178 0 STFSW
STSWI
HD2SOG
HD2Y
HD2CB
HD2CR
C23
Y23
HPSW_V33
T1SYNC_C L61 FB T1SYNC
HP_L L36 FB HPL
HD1R
PCR
DVIR
HP_MUTE
HPR L31 FB HP_R
HD1L
PCL
DVIL
V33AA
L39
L43 FB/NC HPSW
J2
HPL
HPGND L41 FB
HPR
V33
HPSWV R170 4.7K
HPSW
CON\PHONEJACK2
HD2CR
HD2CB
HD2Y
R36 75/NC
R35 75/NC
R37 75/NC
V33
VCCSW
V33
R71 2K
R69 10K
L25 FB
BL_ON
BL_PWM
CON16
CON12
FPBL_ON
FPBL_ON R70 10K
Q7 3904
BL_PWM
CON0402H
CON0402H

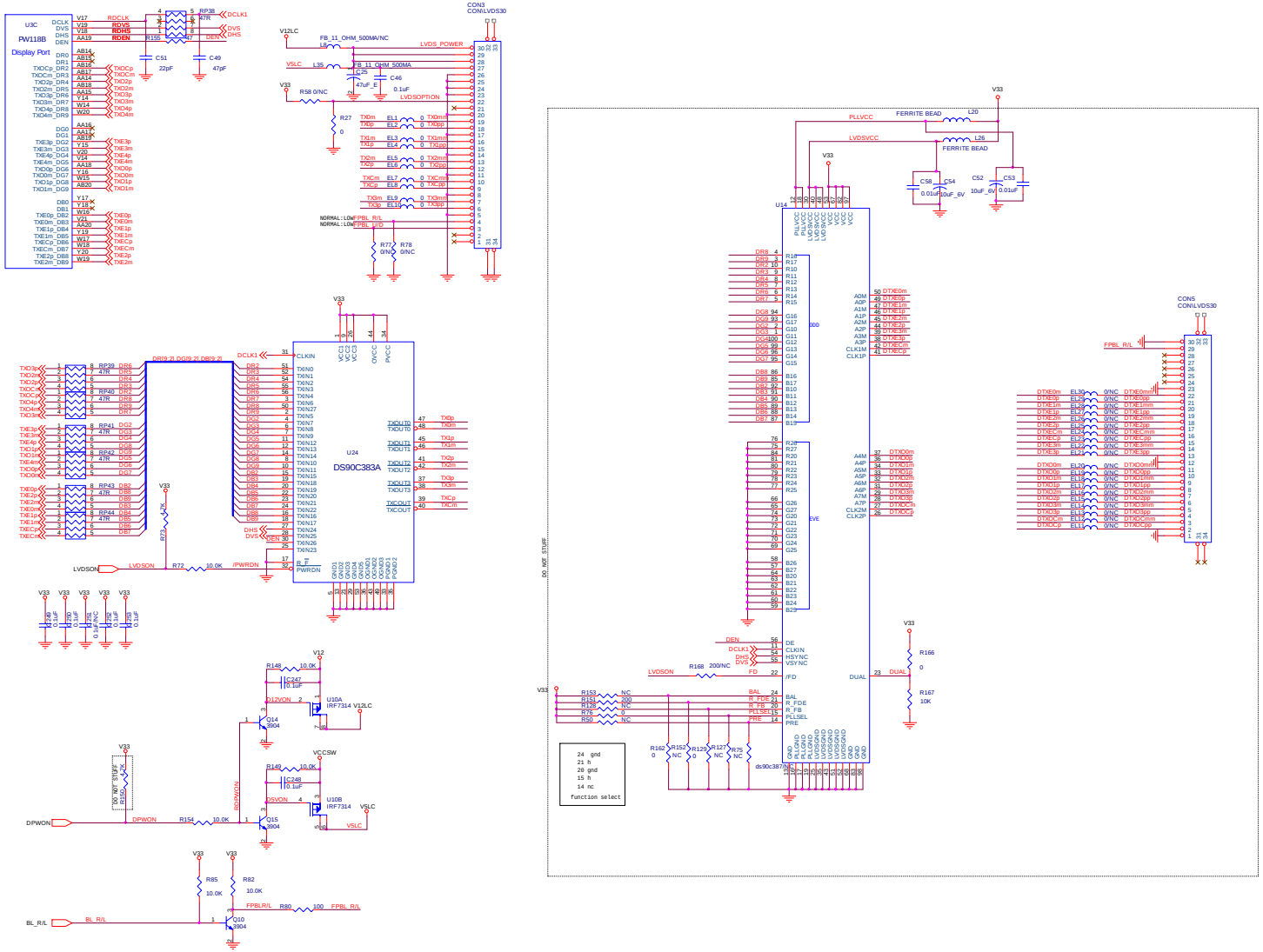
10. PW3300B


U12A
PW3300B
RXD2p
RXD2m
RXD1p
RXD1m
RXD0p
RXD0m
RXDCp
RXDCm
RTERMB
V18PA
FILTA
FILT1A
FILT
IN0CST
IN0CMP
COAST
CLAMP
PCRED
PCGRN
PCBLU
RED1A
GRN1A
SOG1A
BLU1A
RED1
GRN1
SOG1
BLU1
HSYNC
VSYNC
HS1
VS1
HD1CR
HD1Y
HD1CB
RED2A
GRN2A
SOG2A
BLU2A
RED2
GRN2
SOG2
BLU2
HD2CR
HD2Y
HD2SOG
HD2CB
RED3A
GRN3A
SOG3A
BLU3A
RED3
GRN3
SOG3
BLU3
RED4A
GRN4A
SOG4A
BLU4A
RED4
GRN4
SOG4
BLU4
23_HS2
23_VS2
HS2
VS2
Y23
C23
R2
G2
M2
S2
B2
M3
STSWI
SBSWI
ASPC0
ASPC1
REXT
ASPECT0
ASPECT1
ASPECT2
REXT
DO NOT STUFF FOR USA
DATA PATH
DGRE0
DGRE1
DGRE2
DGRE3
DGRE4
DGRE5
DGRE6
DGRE7
DGGE0
DGGE1
DGGE2
DGGE3
DGGE4
DGGE5
DGGE6
DGGE7
DGBE0
DGBE1
DGBE2
DGBE3
DGBE4
DGBE5
DGBE6
DGBE7
DGRO0
DGRO1
DGRO2
DGRO3
DGRO4
DGRO5
DGRO6
DGRO7
DGRO8
DGRO9
DGGO0
DGGO1
DGGO2
DGGO3
DGGO4
DGGO5
DGGO6
DGGO7
DGGO8
DGGO9
DGBO0
DGBO1
DGBO2
DGBO3
DGBO4
DGBO5
DGBO6
DGBO7
DGBO8
DGBO9
DGCLK2
DGCLK1
DGPEN
DGAHS
DGHS
DGVS
DGFLD
DGVBI
ALTCLK1
ALTPEN
ALTAHS
ALTHS
ALTVS
ALTFLD
IN0R[9:2]
IN0G[9:0]
IN0B[9:0]
IN0CLK
IN0PEN
IN0AHS
IN0HS
IN0VS
IN0FLD
IN0VBI
U12C
XIN
XOUT
XTAL27.000
SCL
SDA
DSCL
DSDA
RESETn
HDCPSCL
HDCPSDA
RESET
I2C: 0x42
GPIO
SYSCLKT
EXTINT
GPIO0
GPIO2
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
NC1
NC2
MCL
CTL1
CTL3
FPBL_ON
SBFSW
CTL2
HPSW
BL_R/L
V33
V33SWA
MAD[15:0]
SAD[15:0]
U12B
SDRAM I/F
FSCLK
FSDQM
FSBANK0
FSBANK1
SACLK
MACLK
MADQM
MARASn
MACASn
MAWEn
MABA0
V33_2300SR
U13
SDRAMX16M_TSOP50
CKE
CLK
DQML
DQMH
RAS
CAS
WE
CS
NC1
NC2
L42
10uH

11. PW3300B_PWR

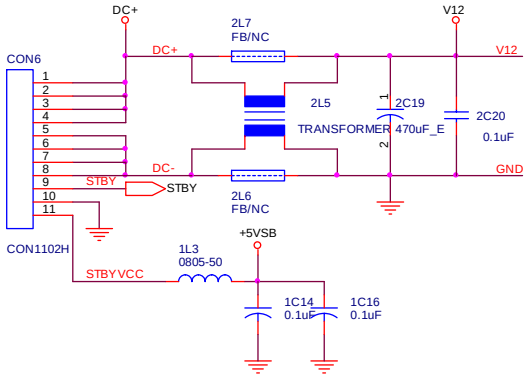


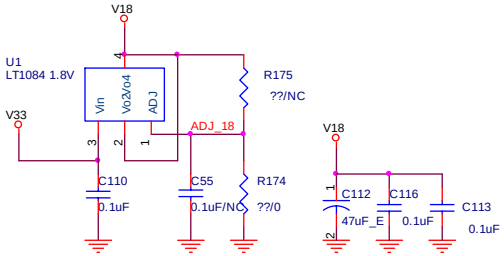
12. DISPLAY

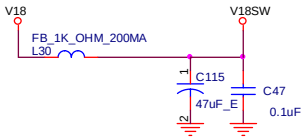

U3C
PW118B
Display Port
DCLK
DVS
DHS
DEN
RDCLK
RDVS
RDHS
RDEN
RP38
47R
DCLK1
DVS
DHS
DEN
C51
22pF
C49
47pF
CON3
CON/LVDS30
V12LC
FB_11_OHM_500MA/NC
L6
LVDS_POWER
VSLC
L35
FB_11_OHM_500MA
C26
47uF_E
C46
0.1uF
LVDSOPTION
V33
R58 0/NC
R27
0
TXD0m
TXD0p
TXD1m
TXD1p
TXD2m
TXD2p
TXD3m
TXD3p
NORMAL::LOW
FPBL_R/L
R77
0/NC
R78
0/NC
U24
DS90C383A
CLKIN
TXIN0
TXIN1
TXIN2
TXIN3
TXIN4
TXIN6
TXIN27
TXIN5
TXIN7
TXIN8
TXIN9
TXIN12
TXIN13
TXIN14
TXIN10
TXIN11
TXIN15
TXIN18
TXIN19
TXIN20
TXIN21
TXIN22
TXIN16
TXIN17
TXIN24
TXIN25
TXIN26
TXIN23
TXOUT0
TXOUT1
TXOUT2
TXOUT3
TXCOUT
PWRDN
LVDSON
R72
10.0K
/PWRDN
R73
47K
V12
R148
10.0K
C247
0.1uF
U10A
IRF7314
Q14
3904
V12LC
VCCSW
R149
10.0K
C248
0.1uF
U10B
IRF7314
Q15
3904
VSLC
DPWON
R154
10.0K
R85
10.0K
R82
10.0K
Q10
3904
BL_R/L
FPBLR/L
R80
100
FPBL_R/L
PLLVCC
FERRITE BEAD
L20
LVDSVCC
L26
FERRITE BEAD
C58
0.01uF
C54
10uF_6V
C52
10uF_6V
C53
0.01uF
U14
DS90C387A
CLKIN
R168
200/NC
LVDSON
R153
R151
R128
R76
R50
NC
200
0
R162
R152
R129
R127
R75
R166
R167
10K
DUAL
24 gnd
21 h
20 gnd
15 h
14 nc
function select
CON5
CON/LVDS30
FPBL_R/L

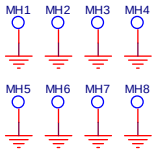
13. POWER

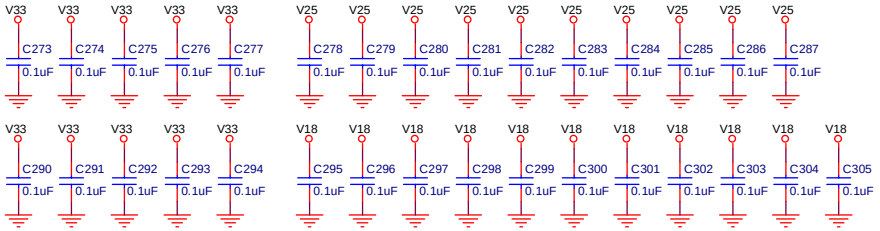
POWER INPUT

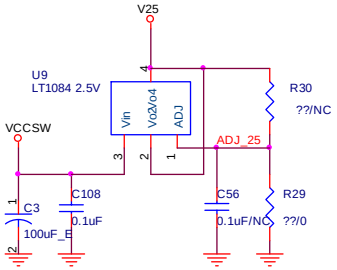


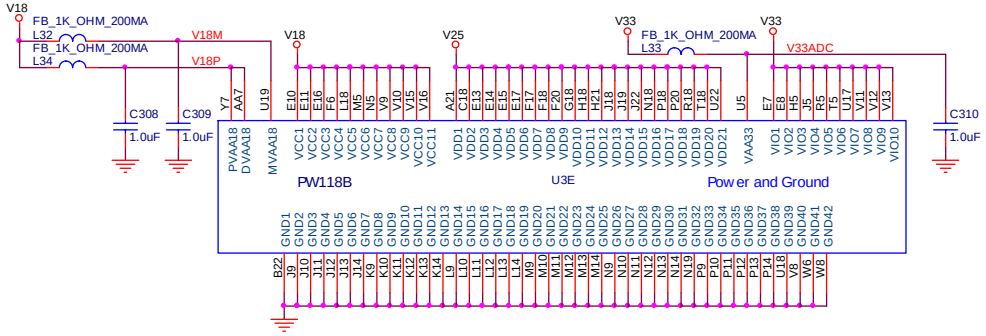


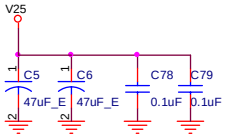






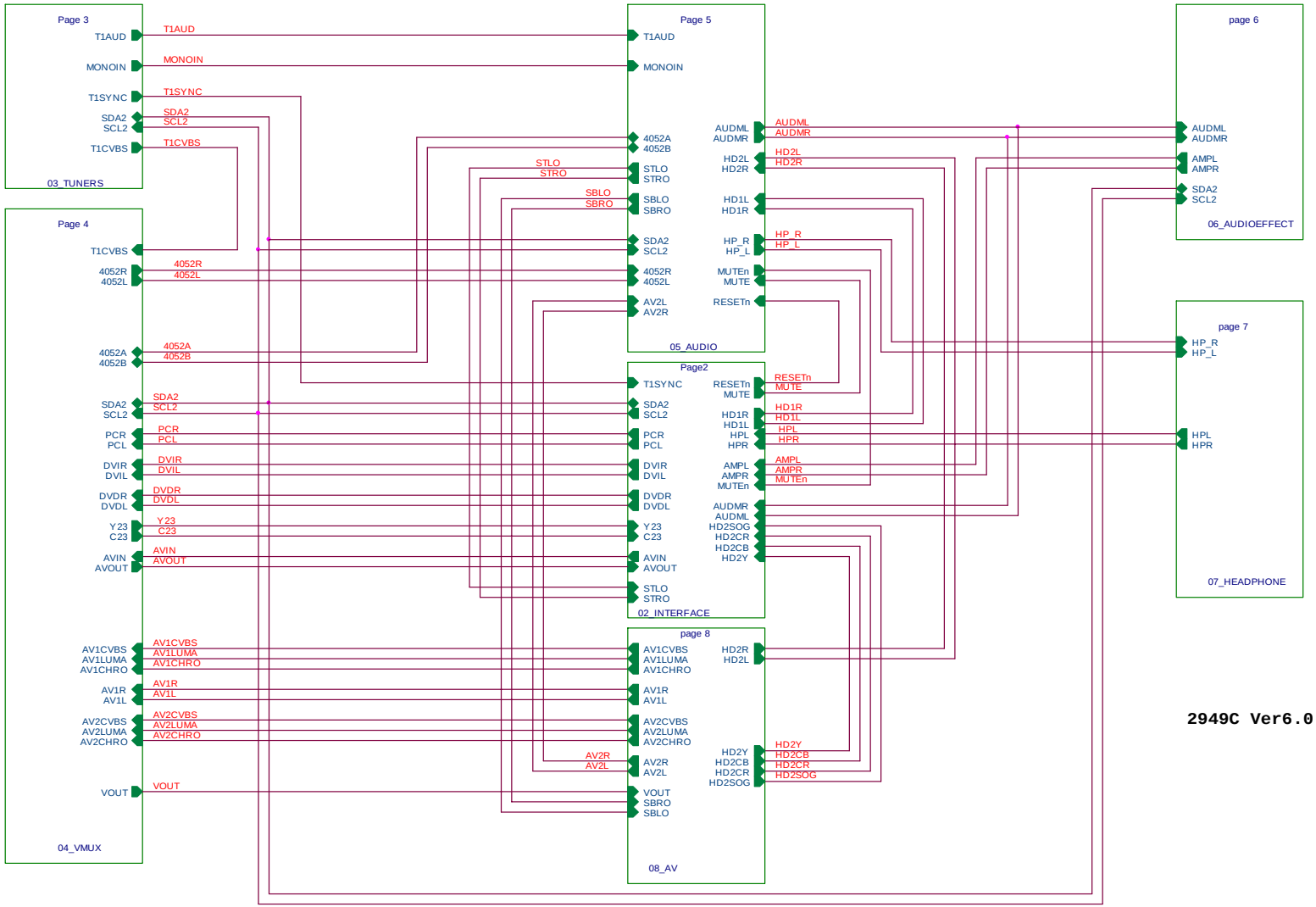






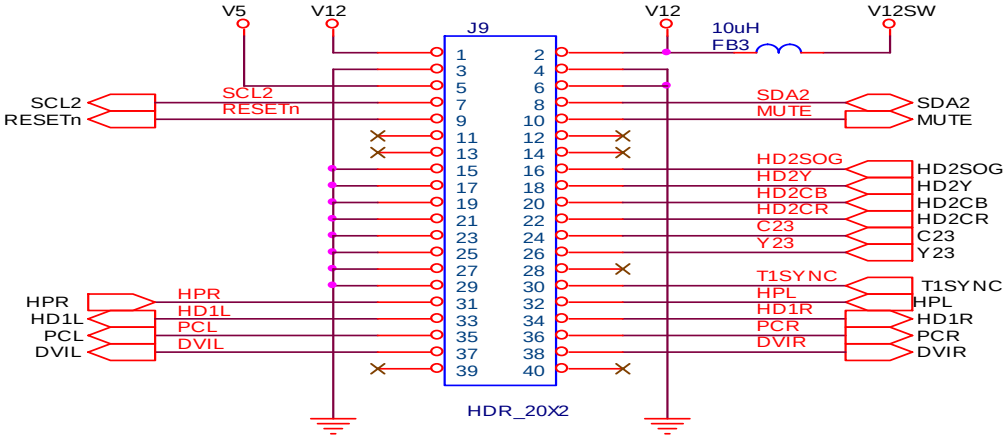
TV BOARD

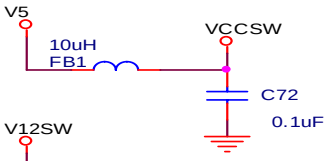
1. TOP

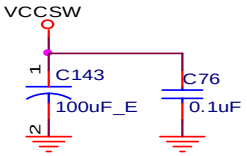


2949C Ver6.0(20070125)

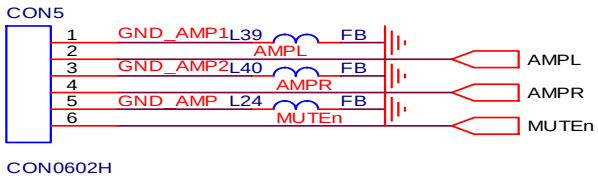
2. INTERFACE

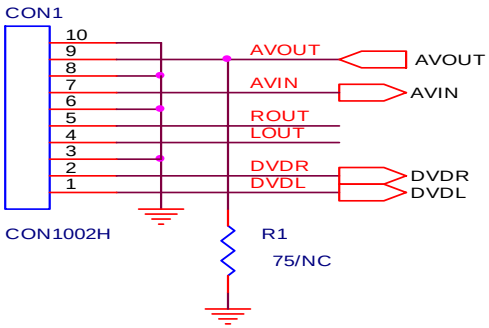


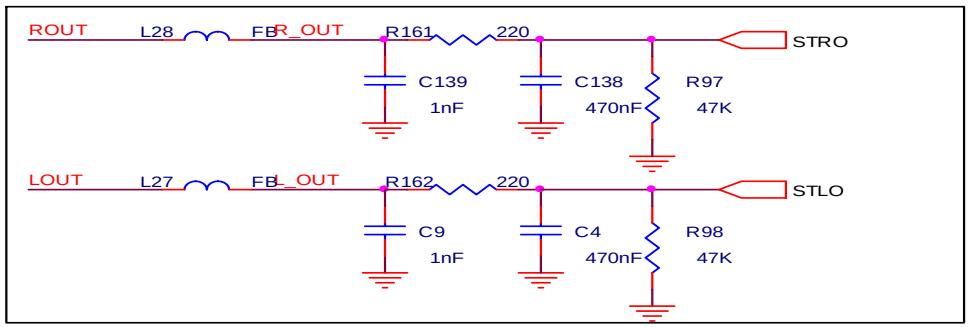




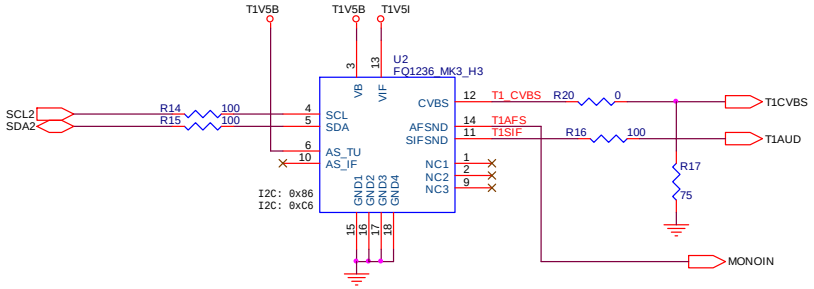
TO AMP BOARD

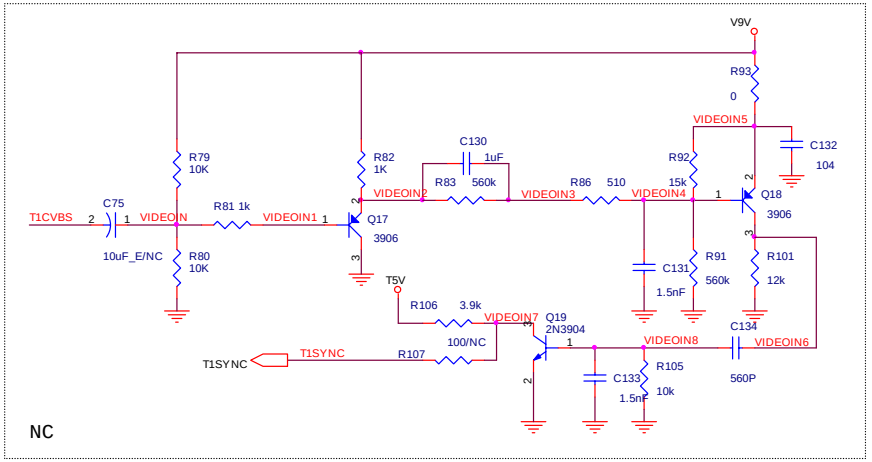


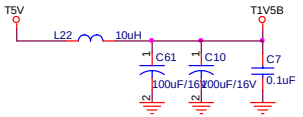


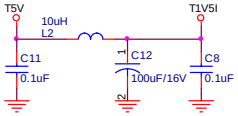


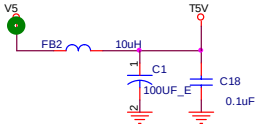
3. TUNERS

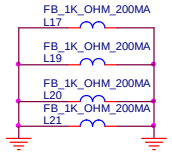

T1V5B
T1V5B
T1V5I
U2
FQ1236_MK3_H3
SCL2
SDA2
R14
R15
100
100
SCL
SDA
VB
VIF
CVBS
AFSND
SIFSND
AS_TU
AS_IF
NC1
NC2
NC3
GND1
GND2
GND3
GND4
I2C: 0x86
I2C: 0xC6
T1_CVBS
R20
0
T1AFS
T1SIF
R16
100
R17
75
T1CVBS
T1AUD
MONOIN

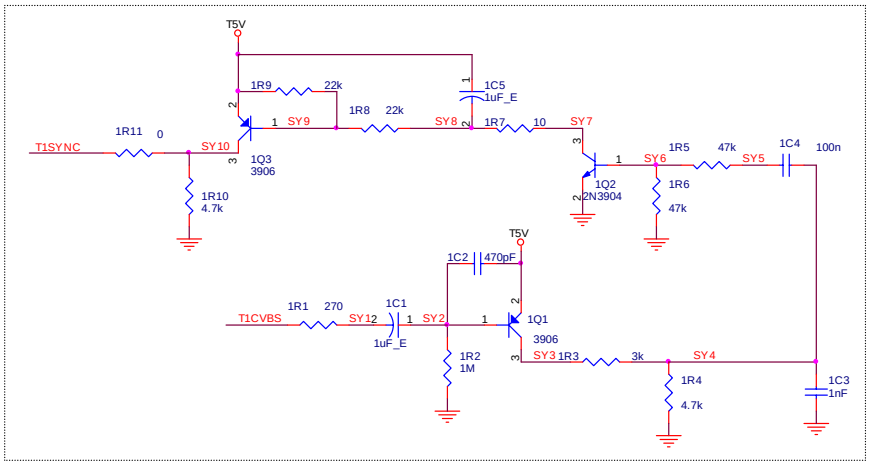

V9V
R93
0
VIDEOIN5
C132
104
R79
10K
R82
1K
C130
1uF
R83
560k
R92
15k
T1CVBS
C75
VIDEOIN
R81 1k
VIDEOIN1
VIDEOIN2
VIDEOIN3
R86
510
VIDEOIN4
Q18
3906
Q17
3906
10uF_E/NC
R80
10K
C131
1.5nF
R91
560k
R101
12k
T5V
R106
3.9k
VIDEOIN7
Q19
2N3904
C134
VIDEOIN6
T1SYNC
T1SYNC
R107
100/NC
VIDEOIN8
R105
10k
C133
1.5nF
560P
NC


T5V
T1V5B
L22
10uH
C61
C10
C7
100uF/16V
100uF/16V
0.1uF

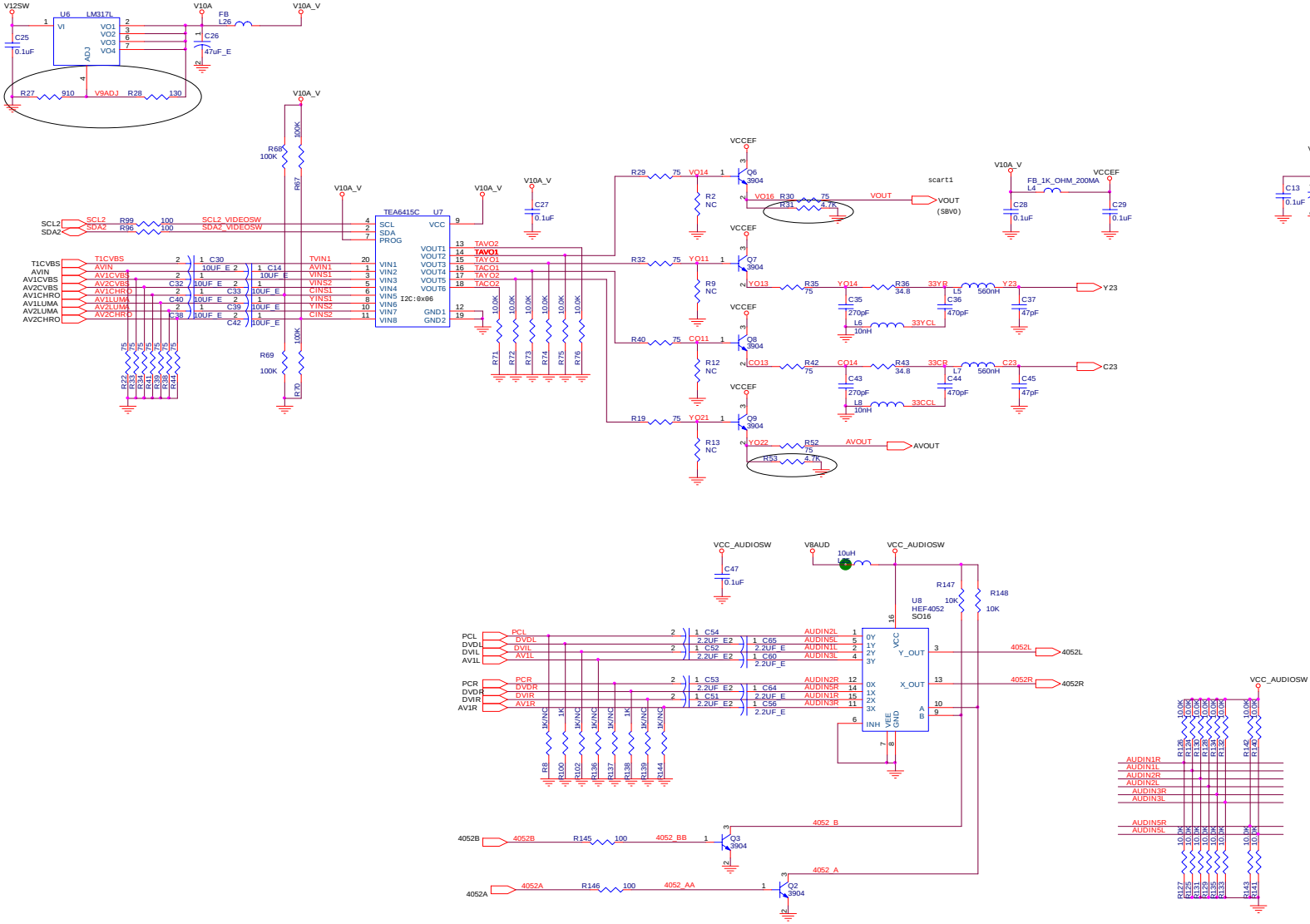

T5V
T1V5I
10uH
L2
C11
C12
C8
0.1uF
100uF/16V
0.1uF


V5
T5V
FB2
10uH
C1
C18
100UF_E
0.1uF

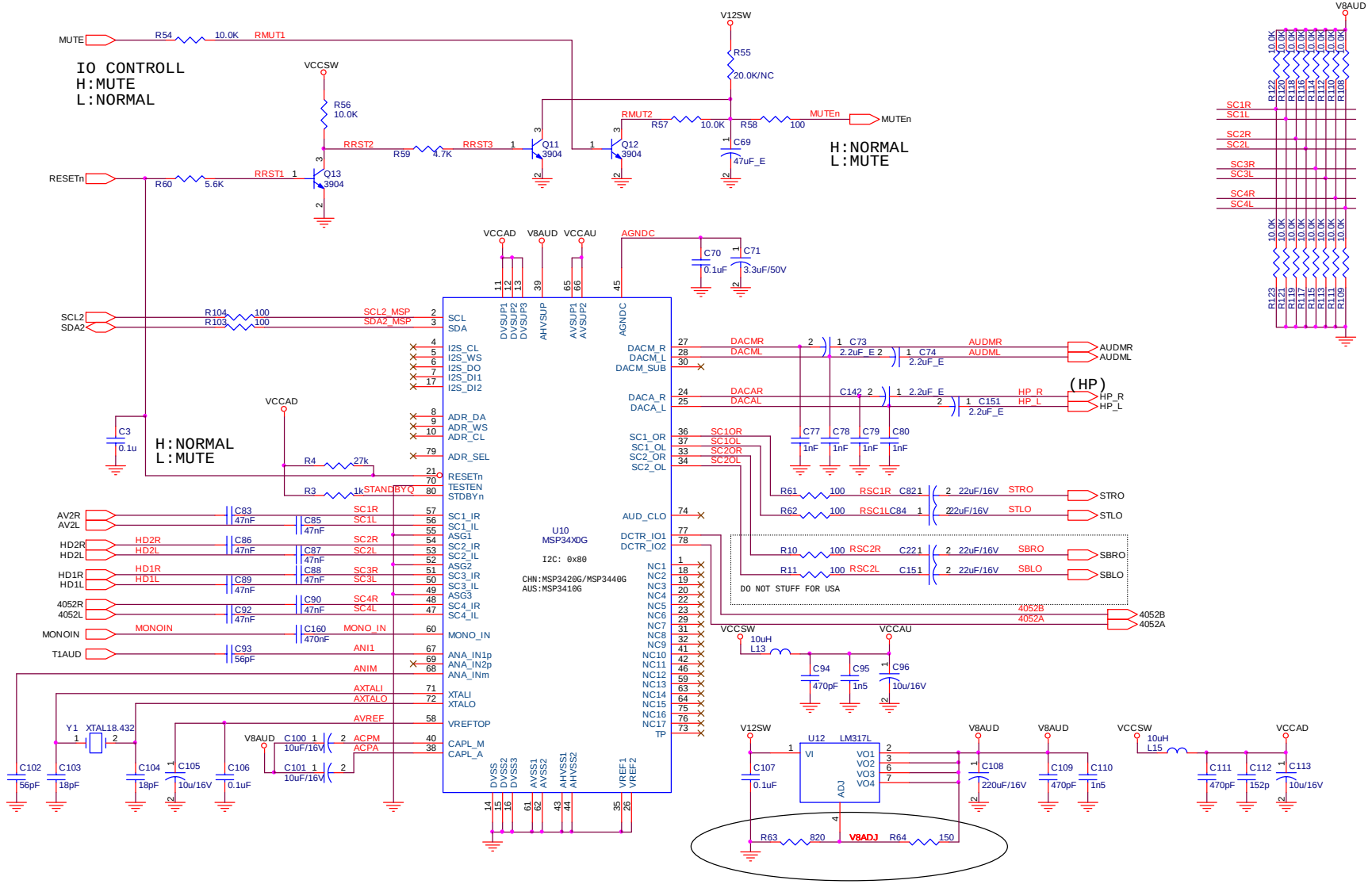

FB_1K_OHM_200MA
L17
FB_1K_OHM_200MA
L19
FB_1K_OHM_200MA
L20
FB_1K_OHM_200MA
L21


T5V
1R9
22k
1C5
1uF_E
1R8
22k
SY8
1R7
10
SY7
T1SYNC
1R11
0
SY10
1Q3
3906
SY9
1R10
4.7k
1Q2
2N3904
SY6
1R5
47k
SY5
1C4
100n
1R6
47k
T5V
1C2
470pF
T1CVBS
1R1
270
SY12
1C1
1uF_E
SY2
1Q1
3906
1R2
1M
SY3
1R3
3k
SY4
1R4
4.7k
1C3
1nF

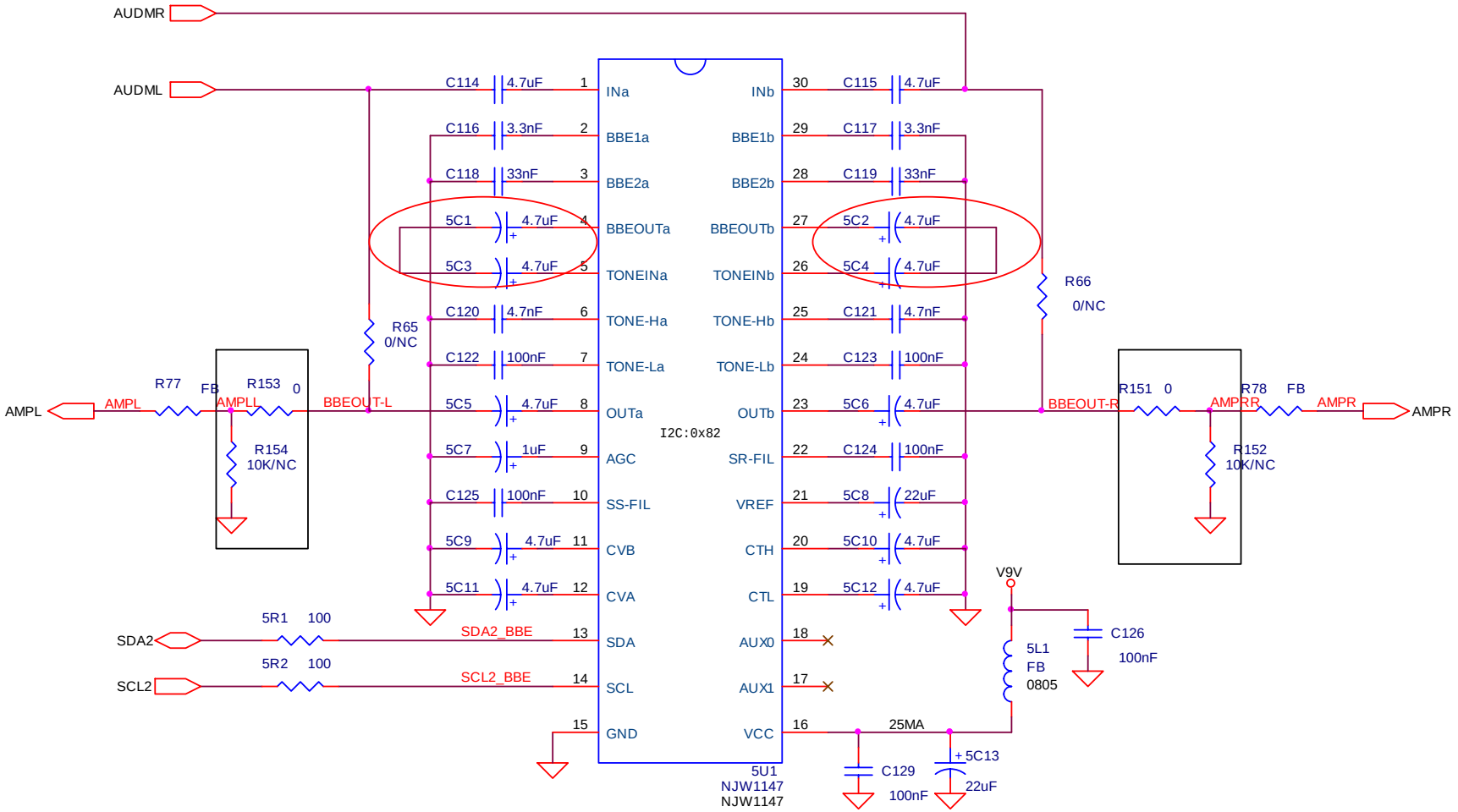
4. VMUX


V12SW
U6 LM317L
V10A
V10A_V
FB L26
C25 0.1uF
C26 47uF_E
R27 910
V9ADJ
R28 130
U7 TEA6415C
I2C:0x86
SCL2
SDA2
SCL2_VIDEOSW
SDA2_VIDEOSW
R99 100
R96 100
T1CVBS
AVIN
AV1CVBS
AV2CVBS
AV1CHRO
AV1LUMA
AV2LUMA
AV2CHRO
TVIN1
VINS1
VINS2
CINS1
YINS1
YINS2
CINS2
R68 100K
R67
R69 100K
R70
R71 10.0K
R72 10.0K
R73 10.0K
R74 10.0K
R75 10.0K
R76 10.0K
C27 0.1uF
TAVO2
TAVO1
TACO1
TACO2
VCCEF
Q6 3904
Q7 3904
Q8 3904
Q9 3904
R29 75
R32 75
R40 75
R19 75
VO14
YO11
CO11
YO21
R2 NC
R9 NC
R12 NC
R13 NC
VO16
R30 75
R31 4.7K
VOUT
scart1
VOUT (SBV0)
FB_1K_OHM_200MA L4
C28 0.1uF
C29 0.1uF
YO13
R35 75
YO14
R36 34.8
33YR
L5 560nH
Y23
C35 270pF
C36 470pF
C37 47pF
L6 10nH
33YCL
CO13
R42 75
CO14
R43 34.8
33CR
L7 560nH
C23
C43 270pF
C44 470pF
C45 47pF
L8 10nH
33CCL
YO22
R52 75
AVOUT
R53 4.7K
U1 L7809
V9V
V12SW
C13 0.1uF
C5 100uF_E
C6 100uF_E
C2 0.1uF
VCC_AUDIOSW
V8AUD
10uH
C47 0.1uF
U8 HEF4052 SO16
R147 10K
R148 10K
PCL
DVDL
DVIL
AV1L
PCR
DVDR
DVIR
AV1R
C54 2.2UF_E2
C52 2.2UF_E2
C53 2.2UF_E2
C65 2.2UF_E
C64 2.2UF_E
C51 2.2UF_E
C60 2.2UF_E
C56 2.2UF_E
AUDIN2L
AUDIN5L
AUDIN1L
AUDIN3L
AUDIN2R
AUDIN5R
AUDIN1R
AUDIN3R
Y_OUT
X_OUT
4052L
4052R
R8 1K/NC
R100 1K
R102 1K/NC
R136 1K/NC
R137 1K/NC
R138 1K
R139 1K/NC
R144 1K/NC
4052_B
4052_A
4052B
4052A
R145 100
R146 100
4052_BB
4052_AA
Q3 3904
Q2 3904
R125 10.0K
R126 10.0K
R134 10.0K
R135 10.0K
R140 10.0K
R141 10.0K
R127 10.0K
R128 10.0K
R129 10.0K
R130 10.0K
R133 10.0K
R142 10.0K
R143 10.0K

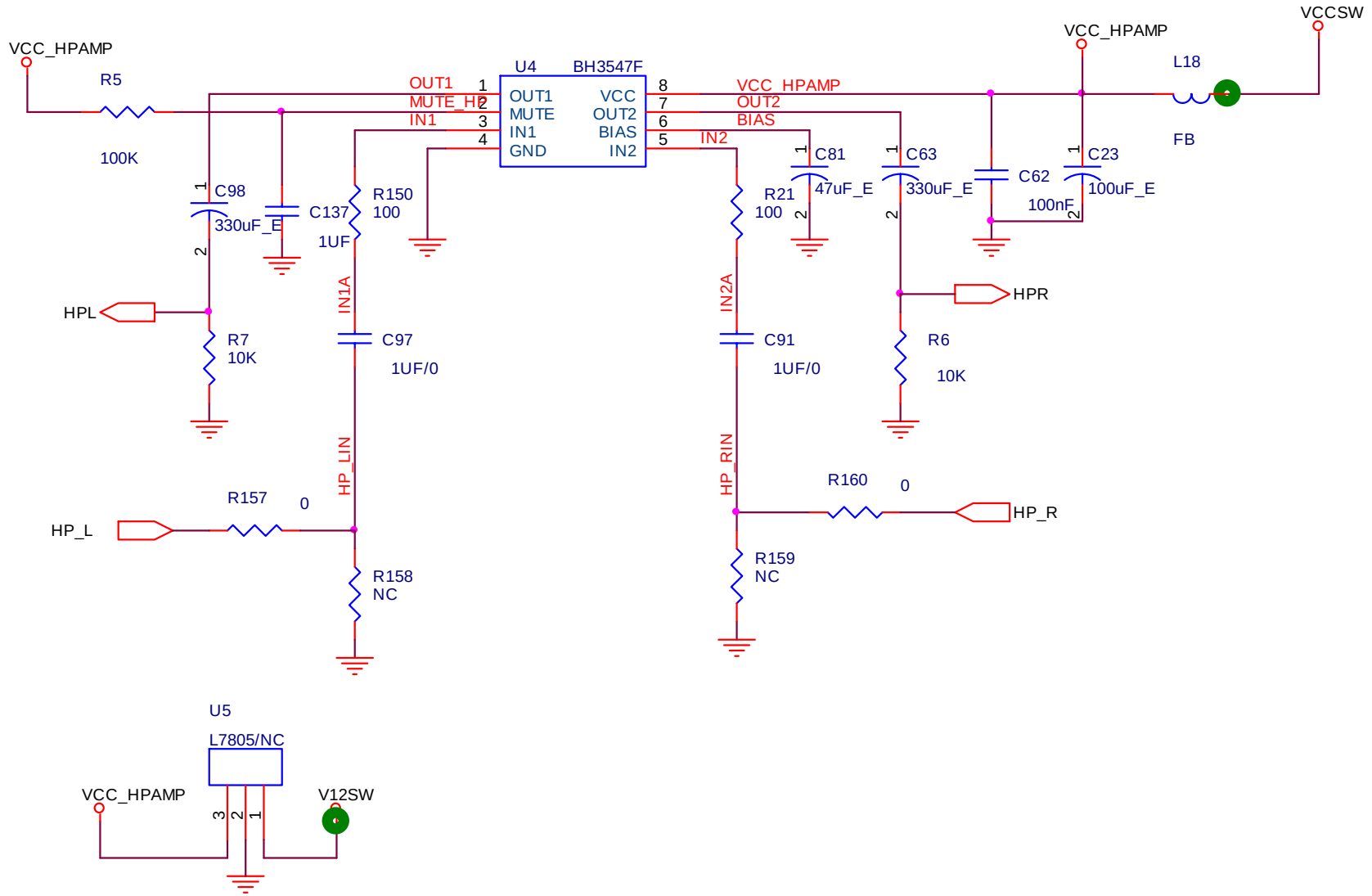
5. AUDIO


MUTE
R54
10.0K
RMUT1
IO CONTROLL
H:MUTE
L:NORMAL
VCCSW
R56
10.0K
RRST2
R59
4.7K
RRST3
Q11
3904
Q12
3904
V12SW
R55
20.0K/NC
RMUT2
R57
10.0K
R58
100
MUTEn
C69
47uF_E
H:NORMAL
L:MUTE
RESETn
R60
5.6K
RRST1
Q13
3904
V8AUD
SC1R
SC1L
SC2R
SC2L
SC3R
SC3L
SC4R
SC4L
VCCAD
VCCAU
AGNDC
C70
0.1uF
C71
3.3uF/50V
SCL2
SDA2
R104
R103
SCL2_MSP
SDA2_MSP
I2S_CL
I2S_WS
I2S_DO
I2S_DI1
I2S_DI2
ADR_DA
ADR_WS
ADR_CL
ADR_SEL
RESETn
TESTEN
STDBYn
C3
0.1u
H:NORMAL
L:MUTE
R4
27k
R3
1k
STANDBYQ
U10
MSP34X0G
I2C: 0x80
CHN:MSP3420G/MSP3440G
AUS:MSP3410G
DACM_R
DACM_L
DACM_SUB
DACA_R
DACA_L
DACMR
DACML
DACAR
DACAL
AUDMR
AUDML
(HP)
HP_R
HP_L
C73
C74
C142
C151
2.2uF_E
SC1_OR
SC1_OL
SC2_OR
SC2_OL
SC1OR
SC1OL
SC2OR
SC2OL
C77
C78
C79
C80
1nF
AUD_CLO
DCTR_IO1
DCTR_IO2
R61
R62
R10
R11
RSC1R
RSC1L
RSC2R
RSC2L
C821
C84
C221
C151
22uF/16V
STRO
STLO
SBRO
SBLO
DO NOT STUFF FOR USA
4052B
4052A
AV2R
AV2L
HD2R
HD2L
HD1R
HD1L
4052R
4052L
MONOIN
T1AUD
C83
C85
C86
C87
C88
C89
C90
C92
C160
C93
47nF
470nF
56pF
SC1R
SC1L
SC2R
SC2L
SC3R
SC3L
SC4R
SC4L
MONO_IN
ANI1
ANIM
AXTALI
AXTALO
AVREF
ACPM
ACPA
ANA_IN1p
ANA_IN2p
ANA_INm
XTALI
XTALO
VREFTOP
CAPL_M
CAPL_A
ASG1
ASG2
ASG3
SC1_IR
SC1_IL
SC2_IR
SC2_IL
SC3_IR
SC3_IL
SC4_IR
SC4_IL
MONO_IN
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10
NC11
NC12
NC13
NC14
NC15
NC16
NC17
TP
Y1
XTAL18.432
C102
C103
C104
C105
C106
C100
C101
56pF
18pF
10uF/16V
0.1uF
VCCSW
10uH
L13
C94
C95
C96
470pF
1n5
10u/16V
V12SW
U12
LM317L
VI
VO1
VO2
VO3
VO4
ADJ
C107
C108
C109
C110
220uF/16V
470pF
1n5
R63
820
V8ADJ
R64
150
VCCSW
10uH
L15
VCCAD
C111
C112
C113
470pF
152p
10uF/16V

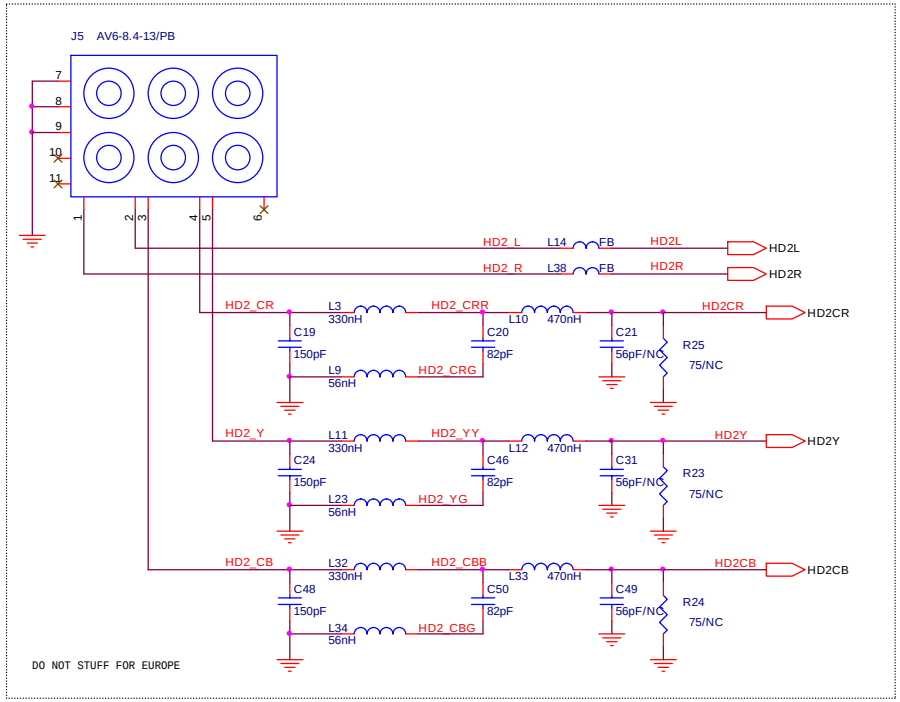
6. AUDIOEFFECT

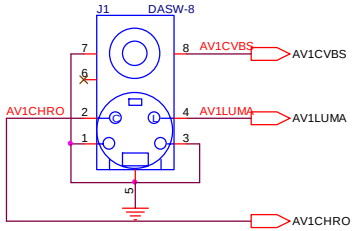


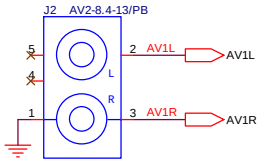
7. HEADPHONE


VCC_HPAMP
R5
100K
C98
330uF_E
C137
1UF
R150
100
HPL
R7
10K
IN1A
C97
1UF/0
HP_LIN
R157
0
HP_L
R158
NC
U4
BH3547F
OUT1
MUTE_HP
IN1
OUT1
MUTE
IN1
GND
VCC
OUT2
BIAS
IN2
VCC_HPAMP
OUT2
BIAS
IN2
C81
47uF_E
R21
100
IN2A
C91
1UF/0
HP_RIN
R159
NC
C63
330uF_E
C62
100nF
C23
100uF_E
VCC_HPAMP
L18
FB
VCCSW
HPR
R6
10K
R160
0
HP_R
U5
L7805/NC
VCC_HPAMP
V12SW

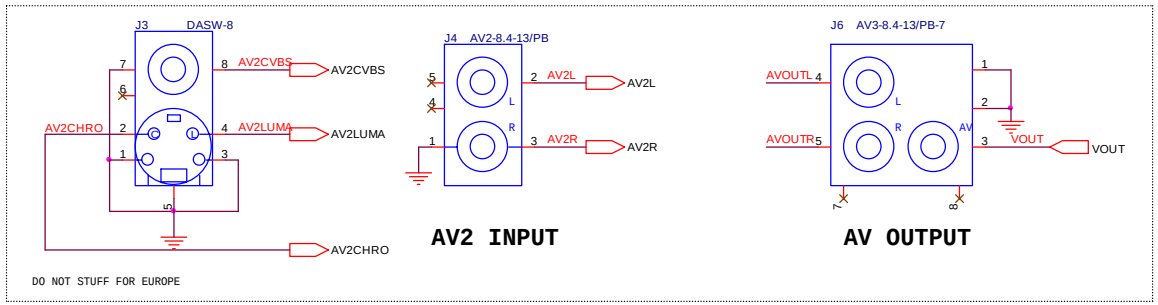
8. AV





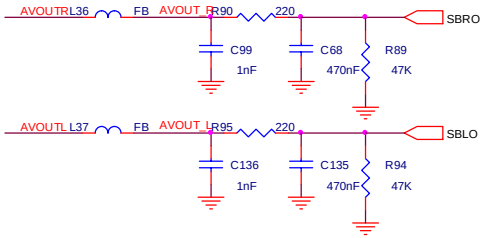


AV1 INPUT



AV2 INPUT

AV OUTPUT



Part5 Part list of DSL26M1TC

Bom No	Part No	Part Name	QTY	
LTD06M-3425C01	02.11.LTD06M3425C01	Main board	1	
Part No	Name	Specification	QTY	LOCA No
01.57.R.2.E000J	SMD resistor	0603-0Ω ±5%	19	C72 C73 1R19 R143 R144 R178 EL1 EL2 EL3 EL4 EL5 EL6 EL7 EL8 EL9 EL10 L2 L4 L6
01.57.R.2.E000J	SMD resistor	0603-0Ω ±5%	3	R1 R27 R58
01.57.R.2.E220J	SMD resistor	0603-22Ω±5%	9	R55 R56 R57 R79 R83 R94 R95 R97 R26
01.57.R.2.E270J	SMD resistor	0603-27Ω±5%	8	R98 R100 R101 R115 R116 R118 R119 R125
01.57.R.2.E390J	SMD resistor	0603-39Ω±5%	2	(R15) (R17)
01.57.R.2.E470J	SMD resistor	0603-47Ω±5%	9	R87 R88 R89 R90 R105 R107 R108 R110 R155
01.57.R.2.E750J	SMD resistor	0603-75Ω±5%	13	R45 R46 R47 R65 R67 R68 7R5 7R6 7R7 R99 R111 R117 R124
01.57.R.2.E101J	SMD resistor	0603-100Ω±5%	35	R10 1R8 R31 R33 R41 R42 R43 R53 R59 R60 R63 R64 R80 R86 1R13 1R15 1R16 1R17 1R20 1R21 1R27 1R29 1R30 1R31 1R32 1R33 1R35 1R36 R163 R171 R172 R173 R169 1R37 R66
01.57.R.2.E151J	SMD resistor	0603-150Ω±5%	4	R9 R12 R38 R160
01.57.R.2.E201J	SMD resistor	0603-200Ω±5%	2	R18 (2R11)
01.57.R.2.E511J	SMD resistor	0603-510Ω±5%	1	1R6
01.57.R.2.E561J	SMD resistor	0603-560Ω±5%	1	R126
01.57.R.2.E102J	SMD resistor	0603-1KΩ±5%	16	R22 R24 R25 R142 2R2 2R7 1R10 1R12 1R18 1R22 1R23 1R24 1R26 1R42 1R45 1R46
01.57.R.2.E182J	SMD resistor	0603-1.8KΩ±5%	4	2R10 2R4 R103 R141
01.57.R.2.E202J	SMD resistor	0603-2KΩ±5%	5	R2 R3 R13 R14 R71
01.57.R.2.E222J	SMD resistor	0603-2.2KΩ±5%	1	R6
01.57.R.2.E332J	SMD resistor	0603-3.3KΩ±5%	5	R165 R48 R44 R104 R106
01.57.R.2.E392J	SMD resistor	0603-3.9KΩ±5%	2	R131 R133
01.57.R.2.E472J	SMD resistor	0603-4.7KΩ±5%	22	R11 1R1 1R7 2R8 R40 R49 R51 R52 R54 R61 R62 R73 1R41 R150 R23 R39 R170 R176 R112 R113 R114 1R5
01.57.R.2.E752J	SMD resistor	0603-7.5KΩ±5%	1	R180
01.57.R.2.E822J	SMD resistor	0603-8.2KΩ±5%	1	2R3

01.57.R.2.E103J	SMD resistor	0603-10KΩ ±5%	36	2R5 2R6 R69 R70 1R28 1R38 1R44 R156 R157 R158 R159 R177 1R2 1R4 R19 R20 R72 R82 R85 R130 R132 R139 R145 R146 R147 R148 R149 R154 R134 R135 R136 R137 1R9 R179 1R47 1R48
01.57.R.2.E103J	SMD resistor	0603-10KΩ ±5%	1	R164
01.57.R.2.E123J	SMD resistor	0603-12KΩ ±5%	1	C74
01.57.R.2.E123J	SMD resistor	0603-12KΩ ±5%	1	R21
01.57.R.2.E153J	SMD resistor	0603-15KΩ ±5%	1	1R3
01.57.R.2.E203J	SMD resistor	0603-20KΩ ±5%	2	2R1 2R9
01.57.R.2.E243J	SMD resistor	0603-24KΩ ±5%	1	R109
01.57.R.2.E333J	SMD resistor	0603-33KΩ ±5%	3	1R25 1R34 1R39
01.57.R.2.E683J	SMD resistor	0603-68KΩ ±5%	1	1R14
01.57.R.2.E104J	SMD resistor	0603-100KΩ ±5%	2	1R43 1R11
01.57.R.2.E334J	SMD resistor	0603-330KΩ ±5%	1	(1R40)
01.57.R.2.E105J	SMD resistor	0603-1MΩ ±5%	1	(R7)
01.57.R.2.E155J	SMD resistor	0603-1.5MΩ ±5%	1	(R102)
01.57.R.3.E000J	SMD resistor	0805-0Ω ±5%	4	R29 R174 R121 R123
01.57.R.8.EP2204	SMD row resistor	22Ω*4 ±5%	15	RP1 RP2 RP3 RP4 RP5 RP6 RP7 RP8 RP9 RP10 RP11 RP46 RP47 RP48 RP49
01.57.R.8.EP4704	SMD row resistor	47Ω*4 ±5%	21	RP12 RP13 RP14 RP15 RP16 RP17 RP18 RP19 RP20 RP21 RP22 RP23 RP38 RP39 RP40 RP41 RP42 RP43 RP44 RP24 RP25
01.54.CS.2.E120N50V	SMD capacitor	0603-12P NPO±5%/50V	2	(1C1) (1C2)
01.54.CS.2.E180N50V	SMD capacitor	0603-18P NPO±5%/50V	2	(C8) (C9)
01.54.CS.2.E220N50V	SMD capacitor	0603-22P NPO±5%/50V	1	C51
01.54.CS.2.E330N50V	SMD capacitor	0603-33P NPO±5%/50V	2	(C86) (C87)
01.54.CS.2.E470N50V	SMD capacitor	0603-47P NPO±5%/50V	1	(C49)
01.54.CS.2.E820N50V	SMD capacitor	0603-82P NPO±5%/50V	3	C61 C67 C68
01.54.CS.2.E151N50V	SMD capacitor	0603-150P NPO±5%/50V	3	C57 C63 C70
01.54.CS.2.E221N50V	SMD capacitor	0603-220P NPO±5%/50V	2	C1 C2
01.54.CS.2.E102X50V	SMD capacitor	0603-102 X7R±10%/50V	4	C92 C96 (C99) C211
01.54.CS.2.E822X50V	SMD capacitor	0603-822 X7R±10%/50V	1	(C88)
01.54.CS.2.E823X50V	SMD capacitor	0603-823 X7R±10%/50V	1	(C89)

01.54.CS.2.E104Y50V	SMD capacitor	0603-104 Y5V-20+80%/50V	146	C10 C11 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 2C2 C23 2C3 C24 2C4 2C5 C26 2C6 C27 2C9 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C46 C47 C48 C78 C79 9C1 C100 C101 C102 C103 C104 C105 C108 C110 1C11 1C12 C113 1C13 1C14 C116 1C16 C126 C128 C131 C133 C135 C137 C139 C140 C145 C146 C147 C149 C150 C151 C152 C153 C154 C156 C157 C158 C159 C160 C161 C162 2C10 2C11 2C13 2C14 2C16 2C17 2C18 2C20 C245 C246 C247 C248 C249 C250 C252 C253 C273 C274 C275 C276 C277 C278 C279 C280 C281 C282 C283 C284 C285 C286 C287 C290 C291 C292 C293 C294 C295 C297 C298 C299 C300 C301 C302 C303 C304 C305 1C4 1C5 1C6 1C8 1C9 1C15 C205 C206 C7 C29 C30 C31 C45 C90 C91 C93 C94 C64 C65 C66 C50 C60 C59
01.54.CS.2.E104Y50V	SMD capacitor	0603-104 Y5V-20+80%/50V	13	C76 C77 C80 C81 C82 C83 C84 C85 C117 C118 C95 C97 C98
01.54.CS.2.E224Y16V	SMD capacitor	0603-224 Y5V-20+80%/16V	1	9C2
01.54.CS.2.E105Y16V	SMD capacitor	0603-105 Y5V-20+80%/16V	3	C308 C309 C310
01.54.CS.1.E104Y16V	SMD capacitor	0402-104 Y5V-20+80%/16V	5	C136 C138 C296 C144 C148
01.13.L.Z.ESA50	SMD magnetism bead	0603-50Ω	38	L1 L17 L18 L19 L32 L33 L34 L66 L67 L68 L69 L70 L71 L72 L73 L13 L14 L23 L24 L25 L57 L58 L61 L64 L65 7L1 7L2 7L3 L74 1L2 1L1 L31 L36 L41 L40 L39 L11 L12
01.13.L.Z.ESB50	SMD magnetism bead	0805-50Ω	4	(1L3) L27 L30 L35
01.13.L.Z.ED50A	SMD magnetism	50Ω (3.5*6.0*0.8)	2	2L2 2L4
01.13.L.L.S.E182	Inductor	NLV25T-056J-PF	3	L7 L15 L22
01.13.L.L.S.E183	Inductor	NLV25T-R33J-PF	3	L5 L10 L21
01.13.L.L.S.E184	Inductor	NLV25T-R47J-PF	3	L3 L9 L16
01.13.L.L.S.E007	SMD inductor	0805-10UH	1	L42
01.13.L.L.S.E059	SMD jar install inductor	SLF12575T-100M5R4PF	2	2L3 2L1

01.13.L.L.D.E056	DIP inductor	LCL-11201HA	1	2L5
01.34.CL.S.E47U16V	SMD aluminum electrolyse	CDVS-47UF/16V 6.3*5.4	3	1C10 2C7 1C3
01.34.CL.S.E100U16V	SMD aluminum electrolyse	CDVS-100UF/16V 6.3*5.4	10	C12 C5 C6 C25 C114 C115 C127 C129 C3 C71
01.34.CL.S.E220U25V	SMD aluminum electrolyse	CDVS-220UF/25V 8*10.5	5	2C12 2C1 2C21 2C19 C112
01.34.CL.S.E680U16V	SMD aluminum electrolyse	CDVS-680UF/16V 10*10.5	2	2C15 2C8
01.00.JZ.E27000	DIP oscillator	27.000MHZ-49S-20P	1	Y2
01.00.JZ.E14318	DIP oscillator	14.318MHZ-49S-20P	1	Y1
01.00.JZ.E32768F	DIP oscillator	32.768KHZ 12.5PF±20PPM	1	1Y1
01.41.D.FS.EGIC	Radiation diode	SA0603GIC-2A-01	1	D1
01.41.D.PS.ELL4148	Diode	LL4148 SMD	2	(1D1) 1D2
01.41.D.PS.ES1BB	Diode	PESD5V0S1BB SMD	9	EP5 EP7 EP8 EP9 EP10 EP13 EP14 EP11 EP12
01.42.Q.S.E2N3904	Audion	2N3904 SMD	10	Q3 Q7 Q10 1Q3 Q14 1Q4 Q15 1Q5 1Q6 Q1
01.42.Q.S.E2N3906	Audion	2N3906 SMD	2	1Q2 1Q1
01.42.Q.S.EBAV70L	Audion	BAV70L SMD	2	D8 D22
01.41.D.PS.EBAV99	Diode	BAV99LT1 SMD	10	D16 D17 D18 D19 D20 D21 D23 D24 D25 D26
01.41.D.PS.E54S	Diode	BAT54S SMD	2	2D2 2D1
01.44.IC.S.E118B	IC	PW118B-10 SMD	1	U3
01.46.IC.E3300B	IC	PW3300B-10 SMD	1	U12
01.46.IC.EHYB25DC5	IC	HYB25DC256160CE-5 SMD	2	U8 U5
01.46.IC.E161610	IC	HY57V161610ETP-7 SMD	1	U13
01.44.IC.S.E29AL016	IC	S29AL016M90TEI SMD	1	U23
01.44.IC.S.EVDM83R	IC	THC63LVDM83R SMD	1	U24
01.44.IC.S.EATMEGA8L	IC	ATMEGA8L SMD	1	1U1
01.44.IC.S.ECM2006	IC	CM2006 SMD	1	9U1
01.46.IC.E74L125	IC	74LVC125 SMD	1	U2
01.46.IC.E24LC128A	IC	24LC128A SMD	1	U4
01.46.IC.E24LC21A	IC	24LC21A SMD	2	U6 U11
01.44.IC.S.E108418	IC	AP1084-1.8V SMD	1	U1
01.44.IC.S.E108425	IC	AP1084-2.5V SMD	1	U9
01.44.IC.S.EA11173V3	IC	AZ1117H-3.3 SMD	1	U17
01.44.IC.S.EA11171V8	IC	AZ1117H-1.8 SMD	1	U16
01.44.IC.S.E7314	IC	IRF7314TR SMD	1	U10
01.44.IC.S.EV330	IC	FSAV330 SMD	1	U7

01.44.IC.S.E5236	IC	FAN5236MTC SMD	1	2U1
01.44.IC.S.E6680	IC	FDS6680 SMD	4	2U3 2U4 2U5 2U6
01.44.IC.D.E78L05	IC	78L05 DIP	1	2U2
01.40.CON.S13.AY.E019	SMD jack	1.25-13A	1	CON1
01.40.CON.DPH.E038	Jack	PH-9A	2	CON4 CON13
01.40.CON.S13.AY.E020	SMD jack	1.25-12A	1	CON9
01.40.CON.DPH.E032	Jack	PH-7A	1	CON8
01.40.CON.DPH.E020	Jack	PH-4A	2	CON16 CON12
01.40.CON.DPH.E005	Jack	PH-11A	1	CON6
01.40.CON.S13.AY.E004	SMD jack	1.25-30A	1	CON3
01.40.CON.DCZ.E273	Jack	2.0*20A(40pin) DIP	1	CON7
01.40.CON.DCZ.E066	Horizontal double row(earphone)Jack	CKX-3.5-02K(with switch) DIP	1	J2
01.40.CON.DCZ.E167	Same jack	AV2-8.4-13/PB	2	J3 J4
01.40.CON.DCZ.E301	Same core jack	AV5-13/PB-06/A	1	J1
01.40.CON.DCZ.E007	VGA jack	EV-015FC/15pin DIP	1	P1
01.40.CON.DCZ.E345	DVI Jack	FF-DVI01-RF	1	P2
01.39.SW.QC.ED665	Touch switch	6*6*5(DIP 300g)	1	SW1
01.37.PCB.4.E3425C2	Circuit board	Main board3425C-V2.0	1	
Bom No	Part No	Part Name	QTY	
LTD06T-2949C01	02.22.LTD06T2949C01	TV board	1	
Part No	Name	Specification	QTY	LOCA No
01.57.R.2.E000J	SMD resistor	0603-0Ω ±5%	7	R93 R151 R153 R157 R160 R20 1R11
01.57.R.2.E100J	SMD resistor	0603-10Ω±5%	1	1R7
01.57.R.2.E330J	SMD resistor	0603-33Ω±5%	2	R36 R43
01.57.R.2.E750J	SMD resistor	0603-75Ω±5%	19	R19 R22 R29 R30 R32 R33 R34 R35 R38 R39 R40 R41 R42 R44 R52 R17 R23 R24 R25
01.57.R.2.E101J	SMD resistor	0603-100Ω±5%	19	R10 R11 R14 R15 R16 5R1 5R2 R58 R61 R62 R96 R99 R103 R104 R47 R145 R146 R168 R1753
01.57.R.2.E131J	SMD resistor	0603-130Ω±5%	1	R28
01.57.R.2.E151J	SMD resistor	0603-150Ω±5%	1	R64
01.57.R.2.E221J	SMD resistor	0603-220Ω±5%	4	R90 R95 R161 R162
01.57.R.2.E271J	SMD resistor	0603-270Ω±5%	1	1R1

01.57.R.2.E511J	SMD resistor	0603-510Ω ±5%	1	R86
01.57.R.2.E821J	SMD resistor	0603-820Ω ±5%	1	R63
01.57.R.2.E911J	SMD resistor	0603-910Ω ±5%	1	R27
01.57.R.2.E102J	SMD resistor	0603-1KΩ ±5%	5	R3 R81 R82 R100 R138
01.57.R.2.E302J	SMD resistor	0603-3KΩ ±5%	1	1R3
01.57.R.2.E392J	SMD resistor	0603-3.9KΩ ±5%	1	R106
01.57.R.2.E472J	SMD resistor	0603-4.7KΩ ±5%	5	R59 R31 R53 1R4 1R10
01.57.R.2.E512J	SMD resistor	0603-5.1KΩ ±5%	2	R167 R174
01.57.R.2.E562J	SMD resistor	0603-5.6KΩ ±5%	1	R60
01.57.R.2.E103J	SMD resistor	0603-10KΩ ±5%	54	R6 R7 R79 R80 R105 R147 R148 R54 R56 R57 R71 R72 R73 R74 R75 R76 R108 R109 R110 R111 R112 R113 R114 R115 R116 R117 R118 R119 R120 R121 R122 R123 R124 R125 R126 R127 R128 R129 R130 R131 R132 R133 R134 R135 R140 R141 R142 R143 R166 R169 R170 R171 R173 R176
01.57.R.2.E123J	SMD resistor	0603-12KΩ ±5%	1	R101
01.57.R.2.E153J	SMD resistor	0603-15KΩ ±5%	1	R92
01.57.R.2.E223J	SMD resistor	0603-22KΩ ±5%	2	1R8 1R9
01.57.R.2.E273J	SMD resistor	0603-27KΩ ±5%	1	R4
01.57.R.2.E3092F	SMD resistor	0603-30.9KΩ ±1%	2	R165 R172
01.57.R.2.E473J	SMD resistor	0603-47KΩ ±5%	6	R89 R94 R97 R98 1R5 1R6
01.57.R.2.E104J	SMD resistor	0603-100KΩ ±5%	5	R67 R68 R69 R70 R5
01.57.R.2.E564J	SMD resistor	0603-560KΩ ±5%	2	R83 R91
01.57.R.2.E105J	SMD resistor	0603-1MΩ ±5%	1	1R2
01.57.R.3.E000J	SMD resistor	0805-0Ω ±5%	2	C91 C97
01.57.R.3.E101J	SMD resistor	0805-100Ω ±5%	2	R21 R150
01.54.CS.2.E6P0N50V	SMD capacitor	0603-6P NP0±0.25%/50V	2	(C103) (C104)
01.54.CS.2.E470N50V	SMD capacitor	0603-47P NP0±5%/50V	4	C37 C45 C165 C174
01.54.CS.2.E560N50V	SMD capacitor	0603-56P NP0±5%/50V	2	C93 C102
01.54.CS.2.E820N50V	SMD capacitor	0603-82P NP0±5%/50V	3	C20 C46 C50
01.54.CS.2.E101N50V	SMD capacitor	0603-100P NP0±5%/50V	2	C161 C170
01.54.CS.2.E151N50V	SMD capacitor	0603-150P NP0±5%/50V	4	C19 C24 C48 C112

01.54.CS.2.E271X50V	SMD capacitor	0603-270P 10%X7R/50V	2	C35 C43
01.54.CS.2.E471X50V	SMD capacitor	0603-470P X7R±10%/50V	6	C36 C44 C94 C109 C111 1C2
01.54.CS.2.E561X50V	SMD capacitor	0603-560P X7R±10%/50V	1	C134
01.54.CS.2.E102X50V	SMD capacitor	0603-102 X7R±10%/50V	11	C77 C78 C79 C80 C99 C136 1C3 C9 C139 C164 C173
01.54.CS.2.E152X50V	SMD capacitor	0603-152 X7R±10%/50V	4	C95 C110 C133 C131
01.54.CS.2.E332X50V	SMD capacitor	0603-332 X7R±10%/50V	2	(C116) (C117)
01.54.CS.2.E472X50V	SMD capacitor	0603-472 X7R±10%/50V	2	(C121) (C120)
01.54.CS.2.E333X50V	SMD capacitor	0603-333 X7R±10%/50V	2	(C118) (C119)
01.54.CS.2.E473Y50V	SMD capacitor	0603-473 Y5V-20+80%/50V	8	C83 C85 C86 C87 C88 C89 C90 C92
01.54.CS.2.E104Y50V	SMD capacitor	0603-104 Y5V-20+80%/50V	29	C2 C7 C8 C11 C13 C18 C25 C27 C28 C29 C47 C67 C70 C72 C76 C106 C107 C3 1C4 C122 C123 C124 C125 C126 C129 C132 C62 C167 C168
01.54.CS.2.E474Y50V	SMD capacitor	0603-474 Y5V+80-20%/50V	5	C4 C138 C68 C135 C160
01.54.CS.2.E105Y16V	SMD capacitor	0603-105 Y5V-20+80%/16V	4	C130 C137 1C1 1C5
01.54.CS.3.E475Y16V	SMD capacitor	0805-475 Y5V+80-20%/16V	2	C114 C115
01.13.L.Z.ESA50	SMD magnetism bead	0603-50Ω	13	L14 L24 L36 L37 L38 L39 L40 L4 R77 R78 L18 L27 L28
01.13.L.Z.ESB50	SMD magnetism bead	0805-50Ω	6	5L1 L17 L19 L20 L21 L26
01.13.L.L.S.E124	Circle line inductor	0805-10nH	2	L8 L6
01.13.L.L.S.E182	Inductor	NLV25T-056J-PF	3	L9 L23 L34
01.13.L.L.S.E183	Inductor	NLV25T-R33J-PF	3	L3 L11 L32
01.13.L.L.S.E184	Inductor	NLV25T-R47J-PF	3	L10 L12 L33
01.13.L.L.S.E125	Circle line inductor	0805-560nH	2	L7 L5
01.13.L.L.S.E007	SMD inductor	0805-10UH	8	FB1 L2 FB2 FB3 L13 L15 L22 L25
01.34.CL.D.E1U50VC	Electrolyse capacitor	CD110-1UF/50V 5*11	1	5C7
01.34.CL.D.EV2U250VC	Electrolyse capacitor	CD110-2.2UF/50V 5*11	12	C51 C52 C53 C54 C56 C60 C64 C65 C73 C74 C142 C151
01.34.CL.D.E3U350VC	Electrolyse capacitor	CD110-3.3UF/50V 5*11	1	C71
01.34.CL.D.E4U750VC	Electrolyse capacitor	CD110-4.7UF/50V 5*11	10	5C1 5C2 5C3 5C4 5C5 5C6 5C9 5C10 5C11 5C12

01.34.CL.D.E10U25VC	Electrolyse capacitor	CD110-10UF/25V 5*11	17	C14 C30 C32 C33 C38 C39 C40 C42 C96 C105 C113 C100 C101 C162 C163 C169 C171 C172
01.34.CL.D.E22U16VC	Electrolyse capacitor	CD110-22UF/16V 5*11	6	C15 C22 C82 C84 5C8 5C13
01.34.CL.D.E47U16VC	Electrolyse capacitor	CD110-47UF/16V 5*11	2	C26 C81
01.34.CL.D.E100U16VC	Electrolyse capacitor	CD110-100UF/16V 5*11	6	C1 C10 C12 C61 C23 C166
01.34.CL.D.E220U25VD	Electrolyse capacitor	CD110-220UF/25V 8*12	5	C108 C6 C5 C66 C143
01.34.CL.D.E330U16VD	Electrolyse capacitor	CD110-330UF/16V 6.3*12	2	C98 C63
01.00.JZ.E18432A	DIP oscillator	18.432MHZ-49S-12P	1	Y1
01.41.D.PS.ES1BB	Diode	PESD5V0S1BB SMD	18	EP1 EP2 EP3 EP4 EP5 EP6 EP7 EP8 EP9 EP10 EP11 EP12 EP13 EP14 EP15 EP16 EP17 EP18
01.42.Q.S.E2N3904	Audion	2N3904 SMD	11	Q2 Q3 Q6 Q7 Q8 Q9 Q11 Q12 Q13 Q19 1Q2
01.42.Q.S.E2N3906	Audion	2N3906 SMD	4	Q17 Q18 1Q1 1Q3
01.44.IC.D.EL7809	IC	L7809 DIP	1	U1
01.44.IC.S.E317L	IC	LM317L SMD	2	U6 U12
01.44.IC.S.E4052	IC	CD4052 SMD	1	U8
01.44.IC.S.E6415	IC	TEA6415CD SMD	1	U7
01.44.IC.S.E3547	IC	BH3547F SMD	1	U4
01.46.IC.E3440G	IC	MSP3440G SMD	1	U10
01.44.IC.S.E3410G	IC	MSP3410G-QA-B8-V3 SMD	1	U10
01.44.IC.S.E1147	IC	NJW1147 SMD	1	5U1
01.44.IC.S.E4558	IC	NJM4558 SMD	1	U13
01.31.GPT.E035	Tuner	JS-6H1/111A2	1	U2
01.31.GPT.E015	Tuner	JS-6B2/121A2	1	U2
01.40.CON.DPH.E028	Jack	PH-6A	1	CON5
01.40.CON.DPH.E002	Jack	PH-10A	1	CON1
01.40.CON.DCZ.E499	Jack	H-DASW-8C-5 DIP	2	J1 J3
01.40.CON.DCZ.E167	Same jack	AV2-8.4-13/PB	2	J2 J4
01.40.CON.DCZ.E300	Same jack	AV3-8.4-13/PB-7	1	J6
01.40.CON.DCZ.E301	Same core jack	AV5-13/PB-06/A	1	J5
01.40.CON.DCZ.E273	Jack	2.0*20A(40pin) DIP	1	J9

01.37.PCB.2.E2949C6	Circuit board	TV board 2949C-V6.0	1	
Bom No	Part No	Part Name	QTY	
LTD06A-2758C01	02.17.LTD06A2758C01	Power amplifier board	1	
Part No	Name	Specification	QTY	LOCA No
01.13.L.Z.ESB50	SMD magnetism bead	0805-50Ω	4	1R1 1R2 1R4 1R5
01.57.R.2.E000J	SMD resistor	0603-0Ω ±5%	1	R5
01.57.R.2.E472J	SMD resistor	0603-4.7KΩ±5%	1	R6
01.57.R.2.E124J	SMD resistor	0603-120KΩ±5%	4	R1 R2 R3 R4
01.57.R.3.E000J	SMD resistor	0805-0Ω ±5%	1	J3
01.54.CS.2.E221N50V	SMD capacitor	0603-220P NPO±5%/50V	1	C6
01.54.CS.2.E102X50V	SMD capacitor	0603-102 X7R±10%/50V	4	C22 C23 C24 C25
01.54.CS.2.E104Y50V	SMD capacitor	0603-104 Y5V-20+80%/50V	6	C9 C10 C11 C12 C13 C27
01.54.CS.2.E105Y16V	SMD capacitor	0603-105 Y5V-20+80%/16V	1	C14
01.54.CS.3.E105Y16V	SMD capacitor	0805-105 Y5V-20+80%/16V	2	C7 C8
01.54.CS.2.E224Y16V	SMD capacitor	0603-224 Y5V-20+80%/16V	4	C18 C19 C20 C21
01.54.CS.2.E474Y50V	SMD capacitor	0603-474 Y5V+80-20%/50V	5	C1 C2 C3 C4 C5
01.34.CL.D.E10U50VC	Electrolyse capacitor	CD110-10UF/50V 5*11	3	C15 C16 C17
01.00.CD.DS.E10450V	Radial alone stone capacitor	104/50V X7R±10% feet distance5.08	4	C30 C31 C32 C33
01.00.CD.DL.E47463V	Film capacitor	474/63V	2	C28 C29
01.13.L.L.S.E085	SMD jar install inductor	SLF12575T-470M2R7	4	L5 L6 L7 L8
01.13.L.Z.ESA50	SMD magnetism bead	0603-50Ω	1	L9
01.13.L.Z.ESC100	SMD magnetism bead	1206-100Ω	4	L1 L2 L3 L4
01.42.Q.S.E2N7002	Transistor	2N7002 SMD	1	Q1
01.41.D.FS.EGIC	Radiation diode	SA0603GIC-2A-01	1	D1
01.44.IC.S.E3008D	IC	TPA3008D2PHP SMD	1	U1
01.40.CON.DTJ.E008	Jack	TJC3-4A	1	JP2
01.40.CON.DPH.E028	Jack	PH-6A	1	JP1
01.37.PCB.2.E2758C6	Circuit board	Power amplifier board2758C-V6.0	1	
Bom No	Part No	Part Name	QTY	
LTD06I-2798C01	02.14.LTD06I2798C01	DVD hinge board	1	
Part No	Name	Specification	QTY	LOCA No
01.57.R.2.E750J	SMD resistor	0603-75Ω±5%	2	R4 R8

01.57.R.2.E101J	SMD resistor	0603-100Ω ±5%	6	R9 R10 R11 R12 R33 R38
01.57.R.2.E102J	SMD resistor	0603-1KΩ ±5%	2	R3 R7
01.57.R.2.E103J	SMD resistor	0603-10KΩ ±5%	28	R1 R2 R5 R6 R14 R15 R16 R17 R18 R19 R20 R21 R23 R24 R25 R26 R27 R28 R29 R30 R31 R32 R34 R35 R36 R37 R39 R40
01.57.R.3.E000J	SMD resistor	0805-0Ω ±5%	2	C21 C22
01.13.L.Z.ESB50	SMD magnetism bead	0805-50Ω	5	L1 L3 L12 L13 L14
01.13.L.Z.ESB120	SMD magnetism bead	0805-120Ω	4	L35 L36 L37 L38
01.54.CS.2.E331X50V	SMD capacitor	0603-330P X7R±10%/50V	8	C30 C31 C32 C33 C42 C43 C44 C45
01.54.CS.2.E104Y50V	SMD capacitor	0603-104 Y5V-20+80%/50V	3	C3 C16 C18
01.54.CS.2.E105Y16V	SMD capacitor	0603-105 Y5V-20+80%/16V	10	C7 C8 C9 C10 C11 C12 C13 C14 C19 C20
01.34.CL.D.E100U25VB	Electrolyse capacitor	CD11X-100UF/25V 6.3*7	3	C15 C17 C54
01.34.CL.D.E220U16VB1	Electrolyse capacitor	CD11X-220UF/16V 6.3*7	2	C1 C5
01.34.CL.D.E330U25VE	Electrolyse capacitor	CD110-330UF/25V 8*14	1	C57
01.13.L.L.S.E078	Circle line inductor	0805-330NH 5%	8	L4 L5 L6 L7 L8 L9 L10 L11
01.33.CT.ED47U25V	SMD tantalum capacitor	T491D476K025AT	1	C2
01.42.Q.S.E3904	Audion	SMBT3904 SMD	6	Q1 Q2 Q3 Q4 Q5 Q6
01.44.IC.S.EV330	IC	FSAV330 SMD	1	U1
01.44.IC.S.E74HCT4052	IC	74HCT4052 SMD	1	U2
01.44.IC.D.EL7808	IC	L7808C-V DIP	1	U3
01.40.CON.DPH.E038	Jack	PH-9A	1	J4
01.40.CON.DPH.E002	Jack	PH-10A	1	J3
01.40.CON.S13.AY.E020	SMD jack	1.25-12A	1	J5
01.40.CON.DPH.E032	Jack	PH-7A	1	J6
01.40.CON.DCZ.E274	Jack	HDD44F	2	J1 J2
01.37.PCB.2.E2798C8	Circuit board	Hinge board2798C-V8.0	1	
Bom No	Part No	Part Name	QTY	
LTD06K-2951C01	02.15.LTD06K2951C01	Key board	1	
Part No	Name	Specification	QTY	LOCA No
01.57.R.3.E222J	SMD resistor	0805-2.2KΩ ±5%	2	R2 R6
01.57.R.3.E392J	SMD resistor	0805-3.9KΩ ±5%	2	R3 R7

01.57.R.3.E822F	SMD resistor	0805-8.2K ±1%	2	R1 R5
01.54.CS.3.E221N50V	SMD capacitor	0805-220P NPO±5%/50V	2	C1 C2
01.39.SW.QC.ED665	Touch switch	6*6*5(DIP300g)	10	K1 K2 K3 K4 K5 K6 K7 K8 K9 K10
01.40.CON.S13.AY.E019	SMD jack	1.25-13A	1	J1
01.40.CON.DPH.E024	Jack	PH-5A	1	J2
01.37.PCB.2.E2951C2	Circuit board	Key board2951C-V2.0	1	
Part No	Name	Specification	QTY	LOCA No
01.57.R.3.E101J	SMD resistor	0805-100Ω ±5%	1	R1
01.34.CL.D.E10U25VB	Electrolyse capacitor	CD11X-10UF/25V 4*7	1	C1
01.41.D.FD.E3RB	Radiation diode	Φ3 DIP	1	LED1
01.44.IC.D.E0038B	IC	HS0038B DIP	1	IR1
01.00.SJ.6600.E010	Plastic part	6600-IR receiver support(7.5MM)	1	
01.40.CON.DPH.E058	Jack	PH-5A	1	J1
01.37.PCB.2.E2950C2	Circuit board	Remote control receiving board2950C-V2.0	1	