Compal confidential

Schematics Document
Mobile Yonah uFCPGA with Intel
Calistoga_PM+ICH7-M core logic

2006-01-13

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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Title: Cover Sheet			
Size: Custom	Document Number: LA-2821P		Rev: 1.0
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File Name : LA-2821P

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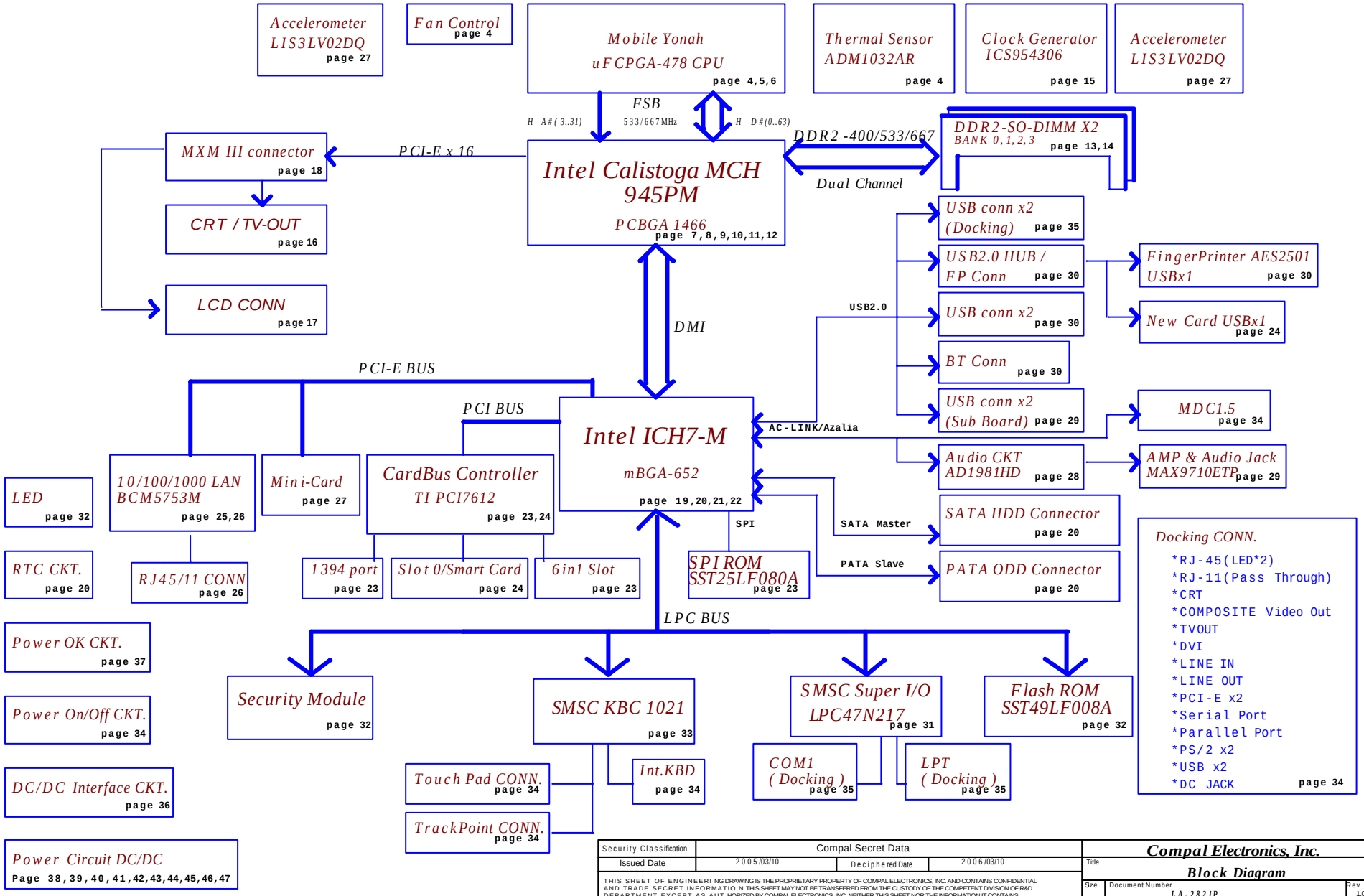

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Title: **Block Diagram**

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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (18.5V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V power rail for Processor I/O and MCH/ICH core power	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+2.5VALW	3.3V always on power rail	ON	ON	ON*
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_VCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Internal PCI Devices

DEVICE	Bus	PCI Device ID	IDSEL #
LAN	1	D8	AD24
Azalia	0	D27	AD11
PCI-E	0	D28	AD12
USB1.1/2.0	0	D29	AD13
PCI to PCI (DMI to PCI)	0	D30	AD14
AC97 MODEM	0	D30	AD14
AC97 Audio	0	D30	AD14
PATA/SATA	0	D31	AD15
LPC I/F	0	D31	AD15
SMBUS	0	D31	AD15
CPU I/F	0	D31	AD15
DMA	0	D31	AD15
PMU	0	D31	AD15

External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
Mini-PCI	D4	AD20	0	F
CARDBUS	D6	AD22	2	C D E G

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010
USB HUB	5C	01011100

Symbol Note :

: means Digital Ground

: means Analog Ground

Note: Layout Related Memo

: Layout Note related Area Mark.

: Question Area Mark.(Wait check)

12/12 : Modified Area Mark.

: C-BOM impact

: Modified Area Mark(Compare with EAL60).

@ : means just reserve , no build

* SPI@ : means just build when SPI I/F BIOS function reserve.
* FWH@ : means just build when FWH I/F BIOS function reserve.
* NOXDP@ : means just build when XDP function disable.
  XDP@ : means just build when XDP function enable. When this time, docking PCI express will not work.
* TPM1.2@ : means just build when TPM1.2 function enable.
* TPM@ : means just build when TPM function enable.
* SC@ : means just build when SmartCard function enable.
* SATA@ : means just build when SATA I/F HDD enable.
  NOSATA@ : means just build when SATA I/F HDD disable.
* NC@ : means just build when New Card function enable.
  NONC@ : means just build when New Card function disable.
* MDC1.5@ : means just build when MDC1.5 function enable.
* 7612@ : means just build when TI PCI7612 chip selected.
  7611@ : means just build when TI PCI7611MLS chip selected.
  250@ : means just build when SMsC LPC47N250 chip selected.
* 1021@ : means just build when SMsC KBC1021 chip selected.
* 1981HD@ : means just build when AD1981HD chip selected.
  45@ : means need be mounted when 45 level assy or rework stage.
* ACCEL@ : means just build when Accelerometer chip LIS3LV02DQ selected.
* NODP@ : means just build when No DP design Clock Gen. selected.
  DP@ : means just build when DP design Clock Gen. selected.
  LPNO@ : means just build when No LP design ICS Clock Gen. selected.
* LP@ : means just build when LP design ICS Clock Gen. selected.
* DB@ : means just build when Mini-PCI E Debug Card function enable.

* : means define for SMT build when this stage

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Title: Notes List

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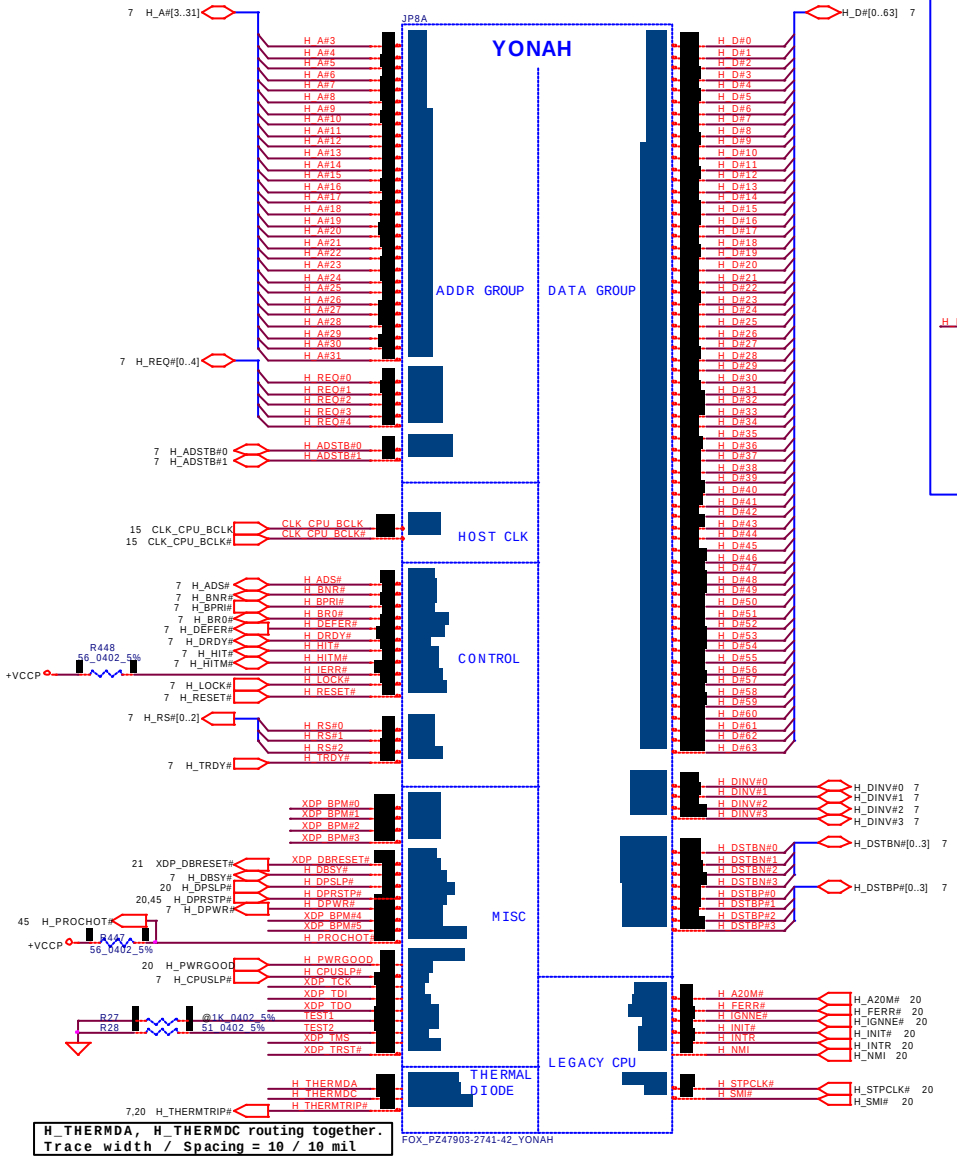

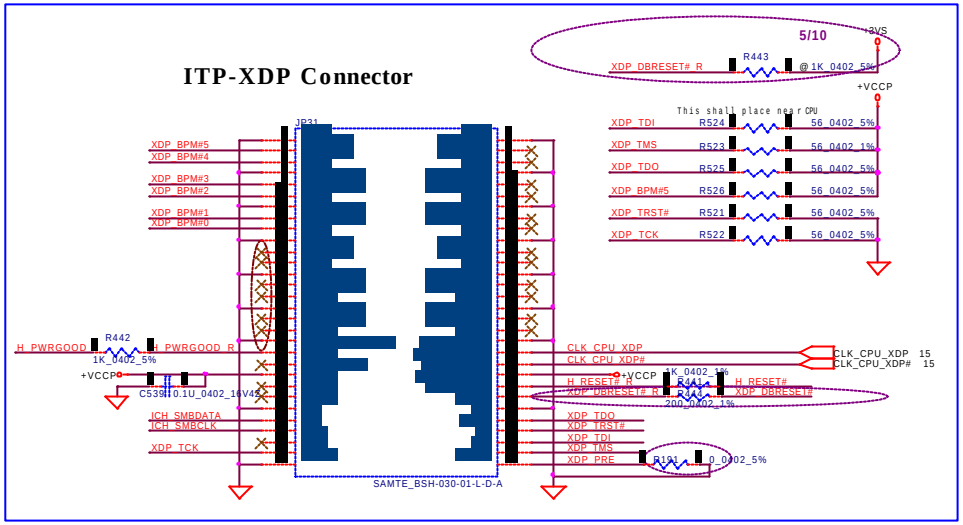

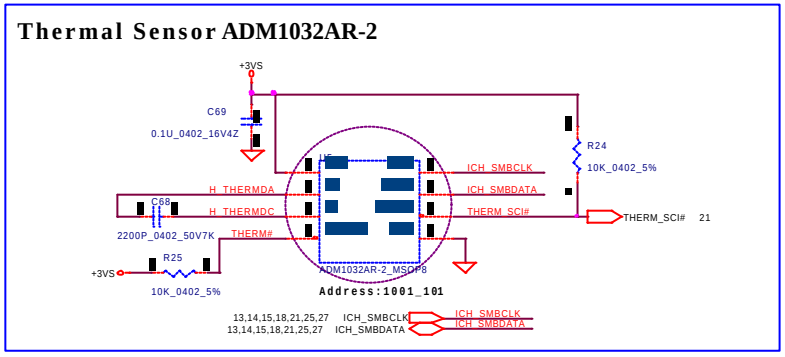

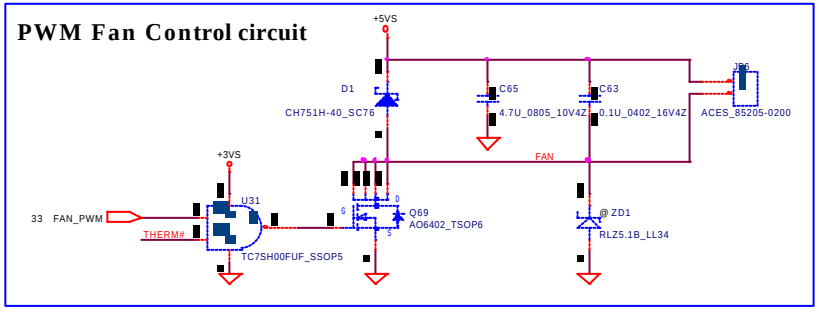

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Title: Yonah CPU in mFCPGA479

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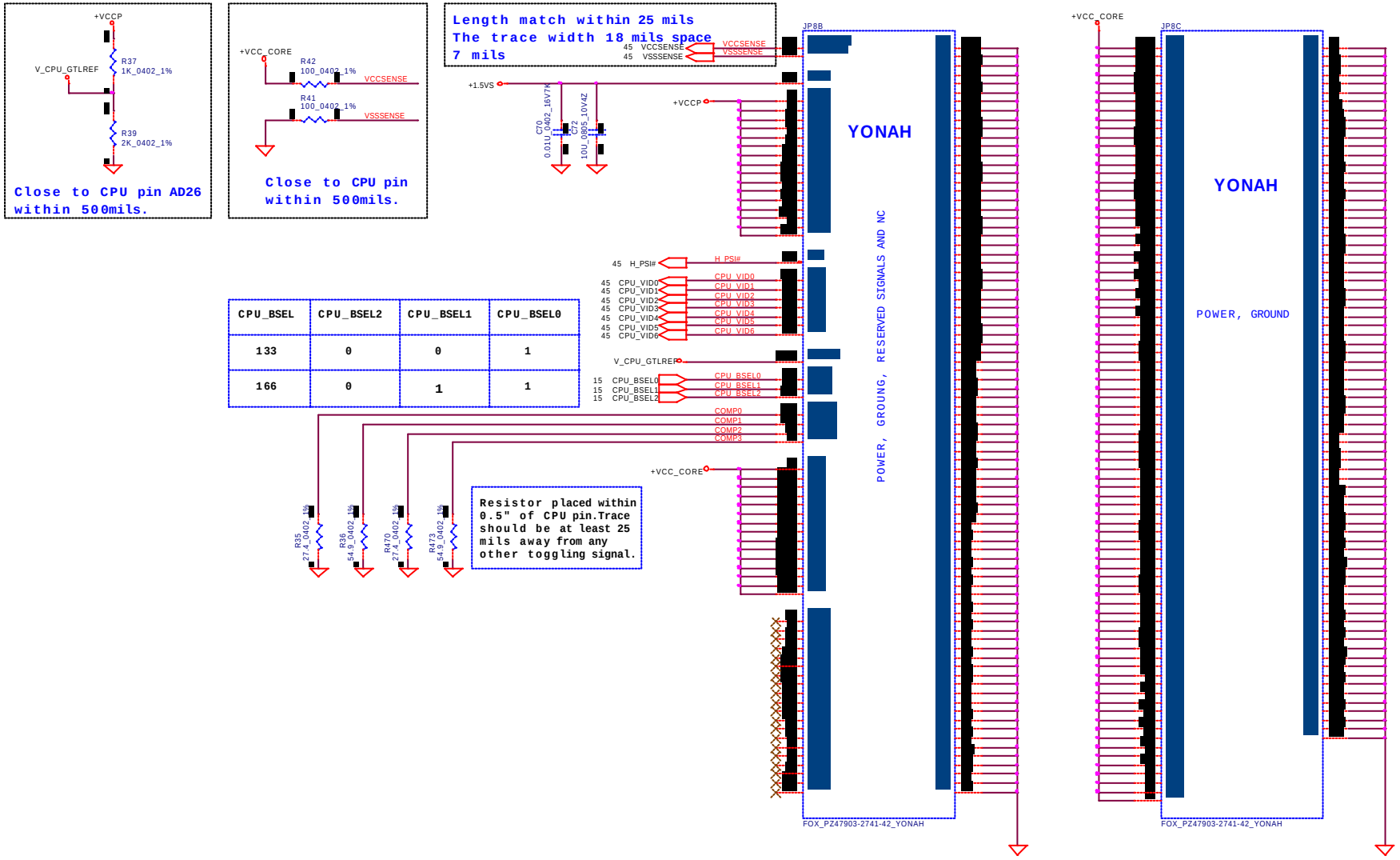

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

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Compal Electronics, Inc.

Title: Yonah CPU in mFCPGA479

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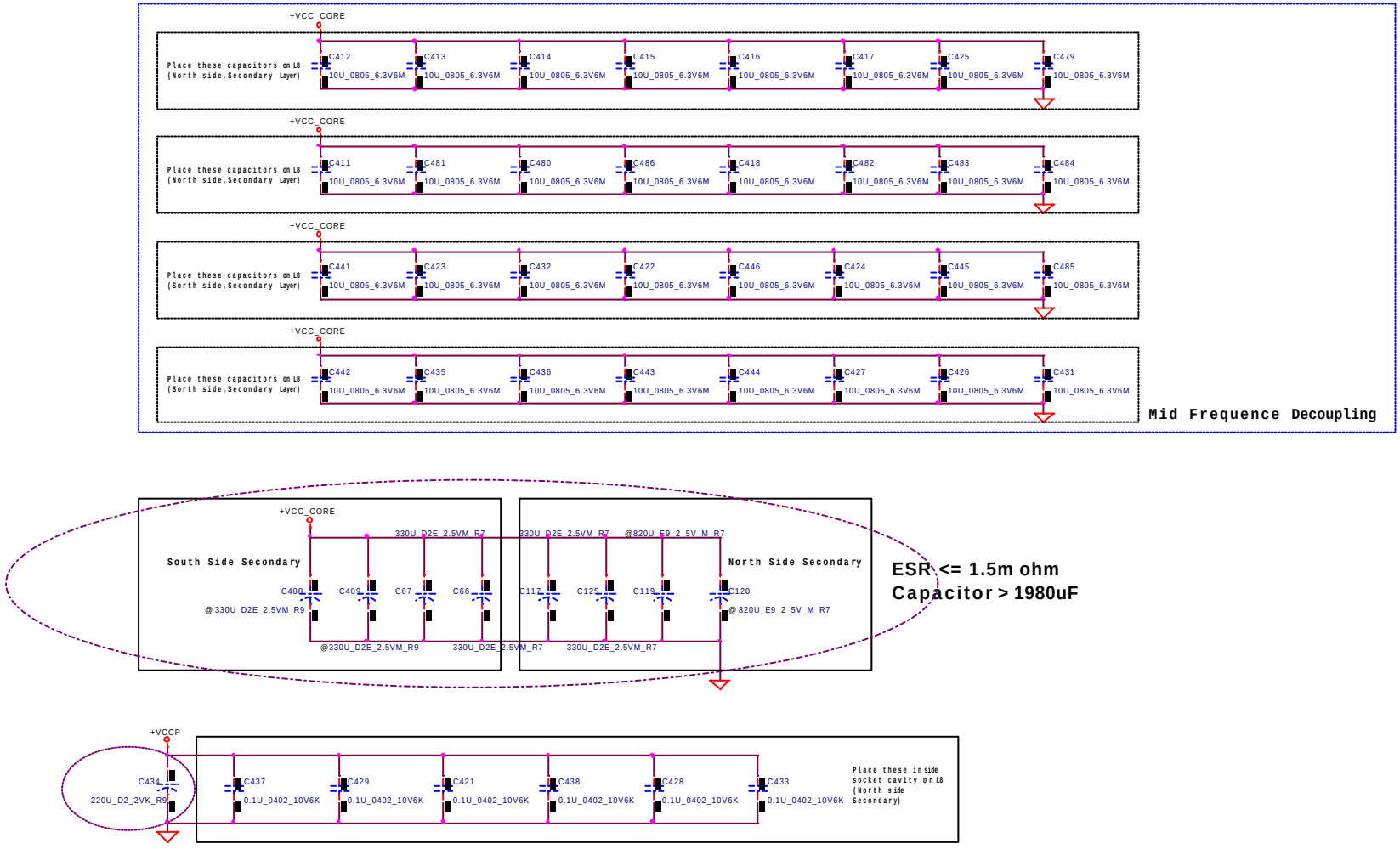

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Compal Electronics, Inc.

Title: CPU Bypass capacitors

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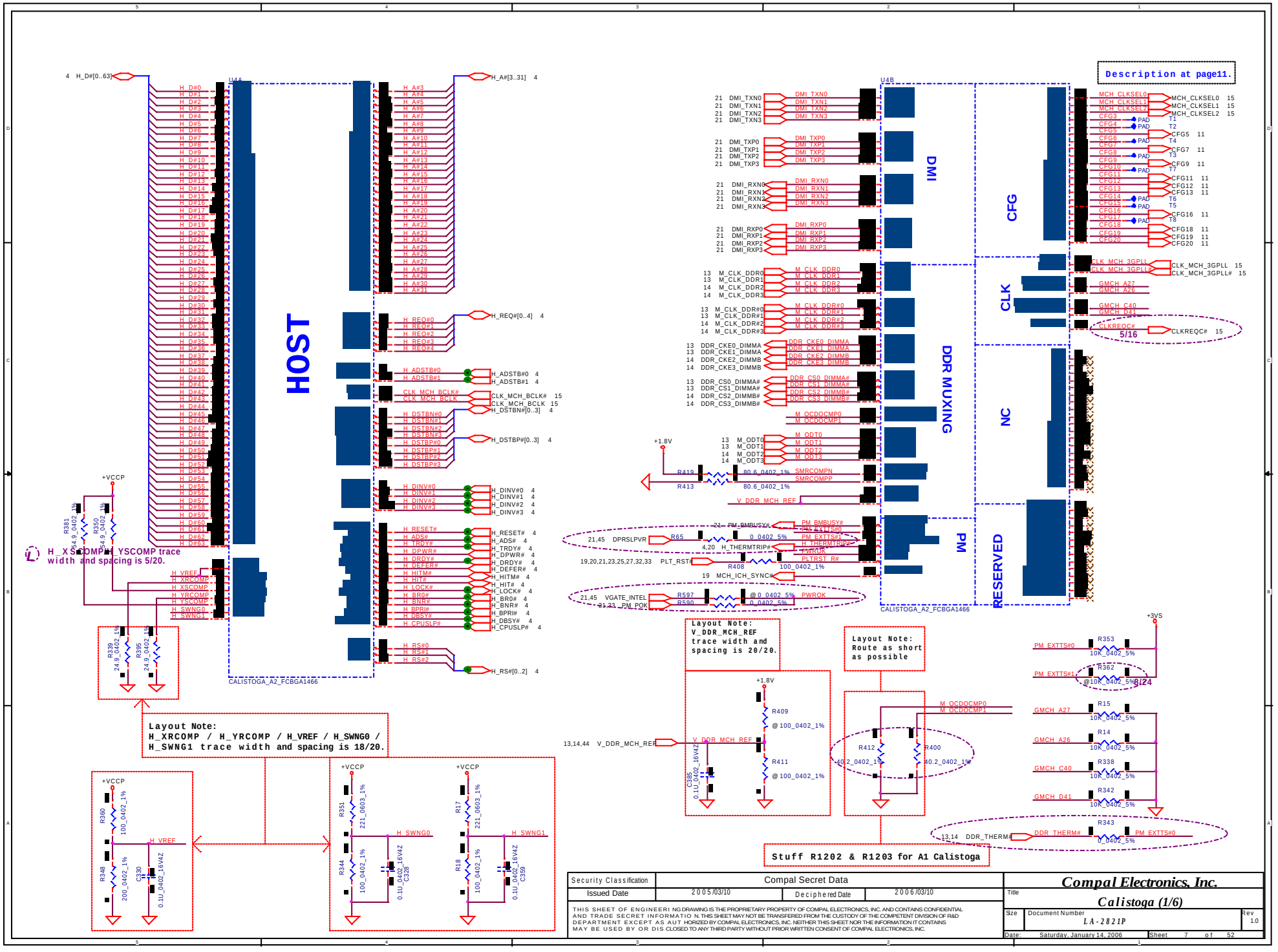

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Title: Calistoga (1/6)

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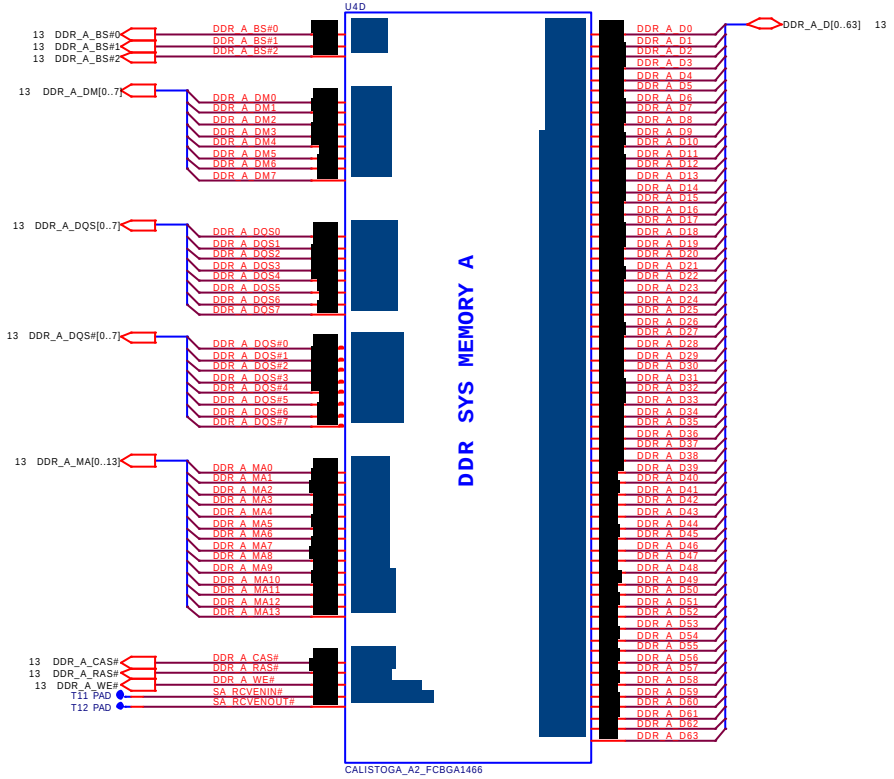

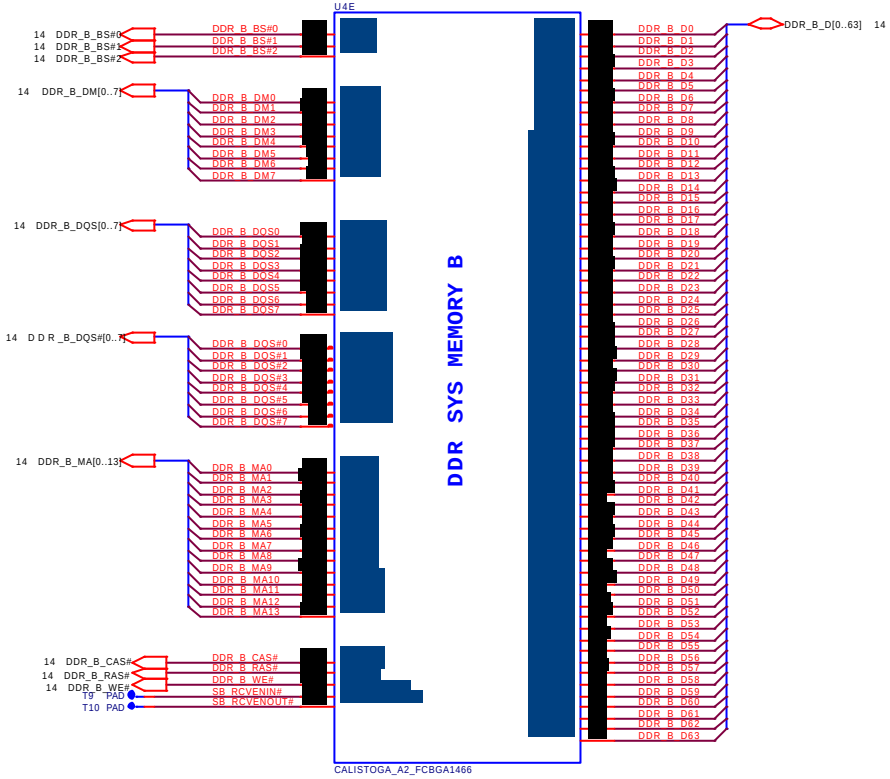

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Title: Calistoga (2/6)

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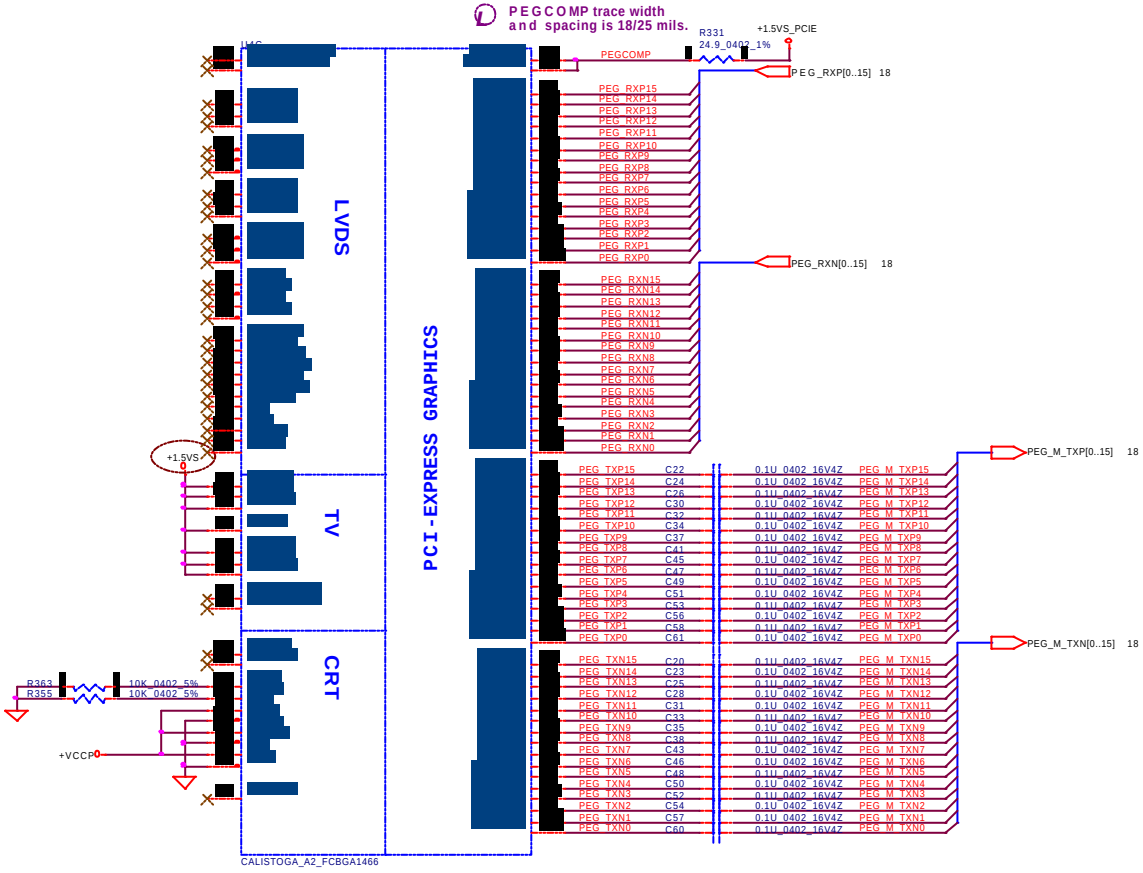

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Title: Calistoga (3/6)

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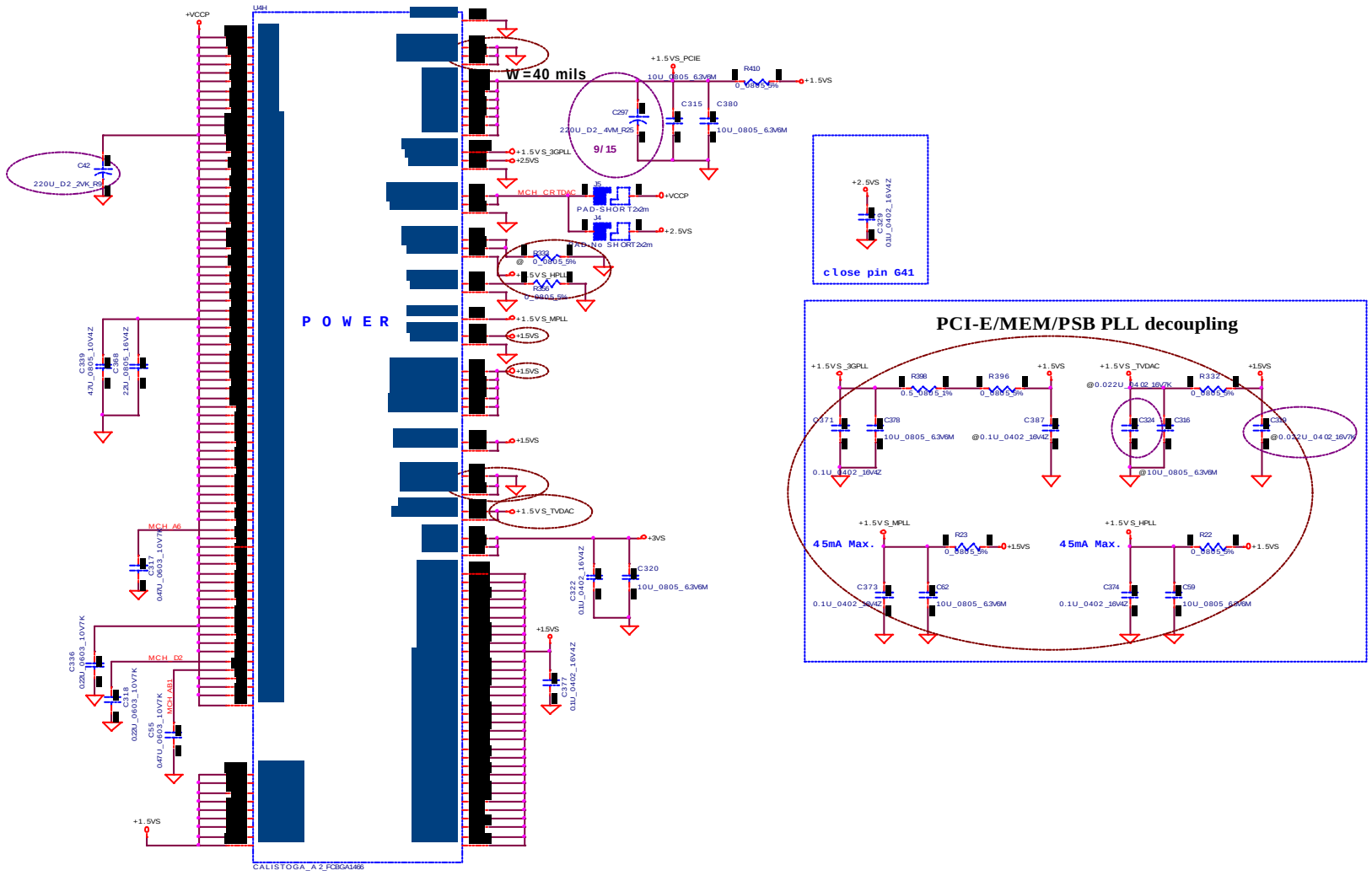

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Calistoga (4/6)

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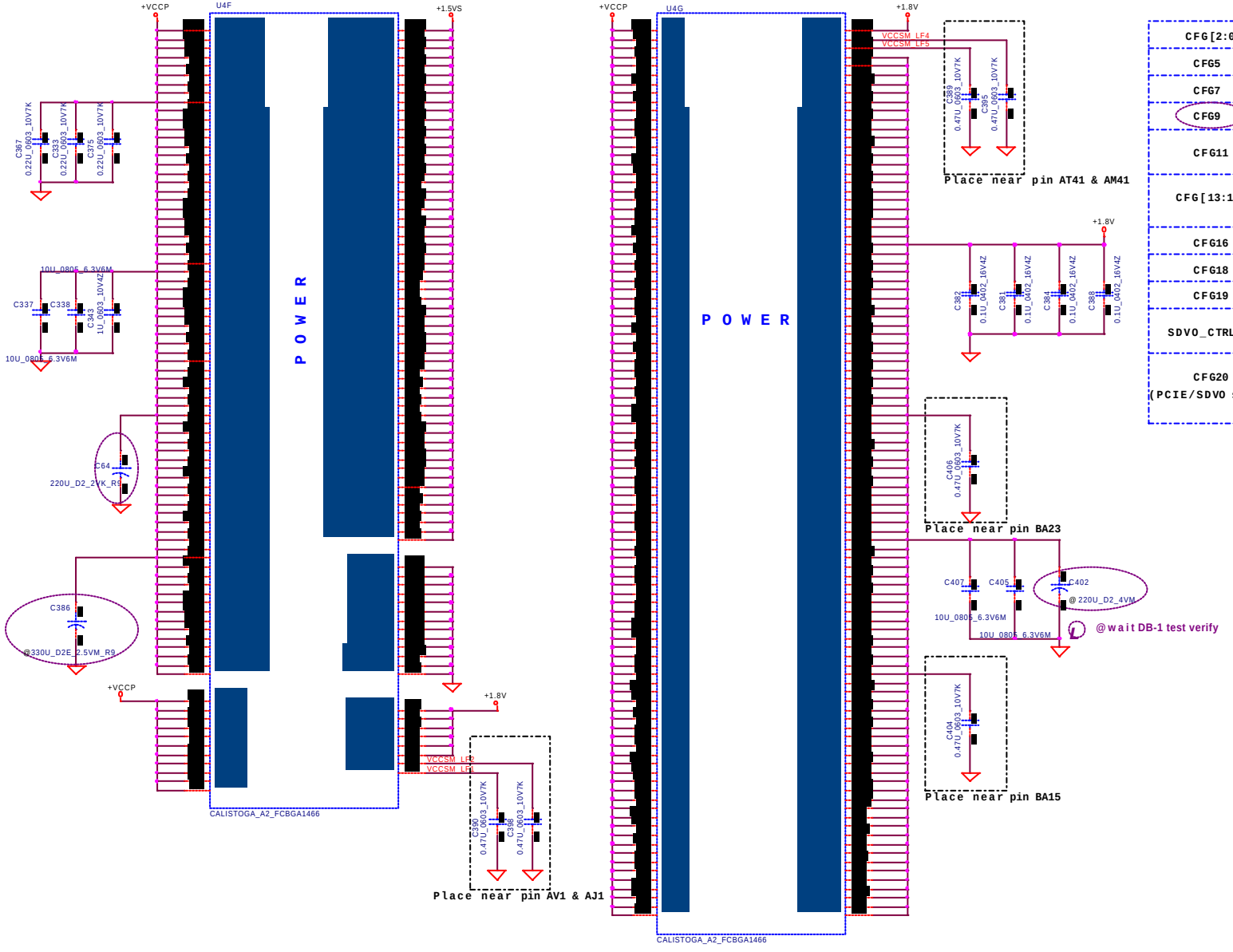
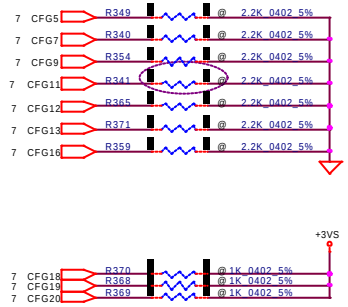


Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable * 1 = Normal Operation (Default)
CFG11	1 = Calistoga * According to Intel Napa Schematic Checklist & CRB Rev1.502 document 2.2Kohm pull-down resistor no request) 0 = Reserved
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



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Title: Calistoga (5/6)

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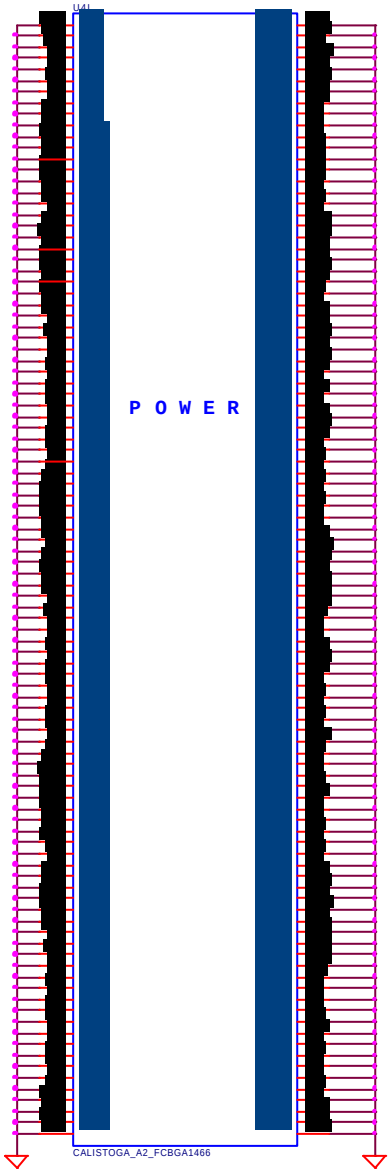

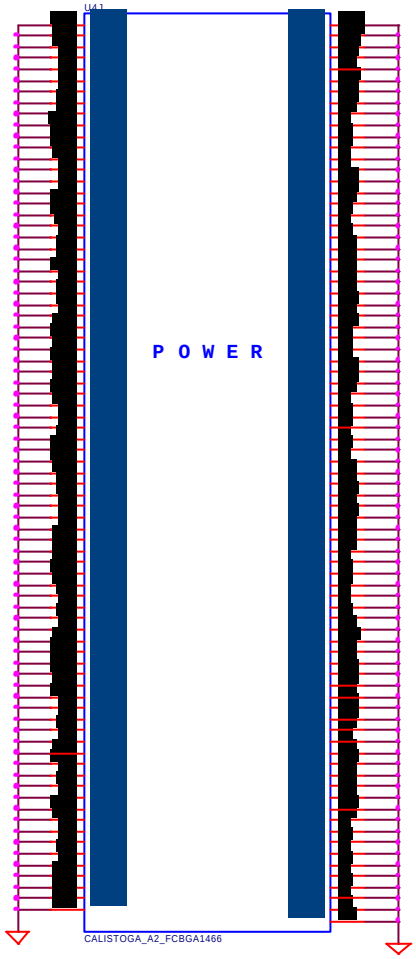

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Title: Calistoga (6/6)

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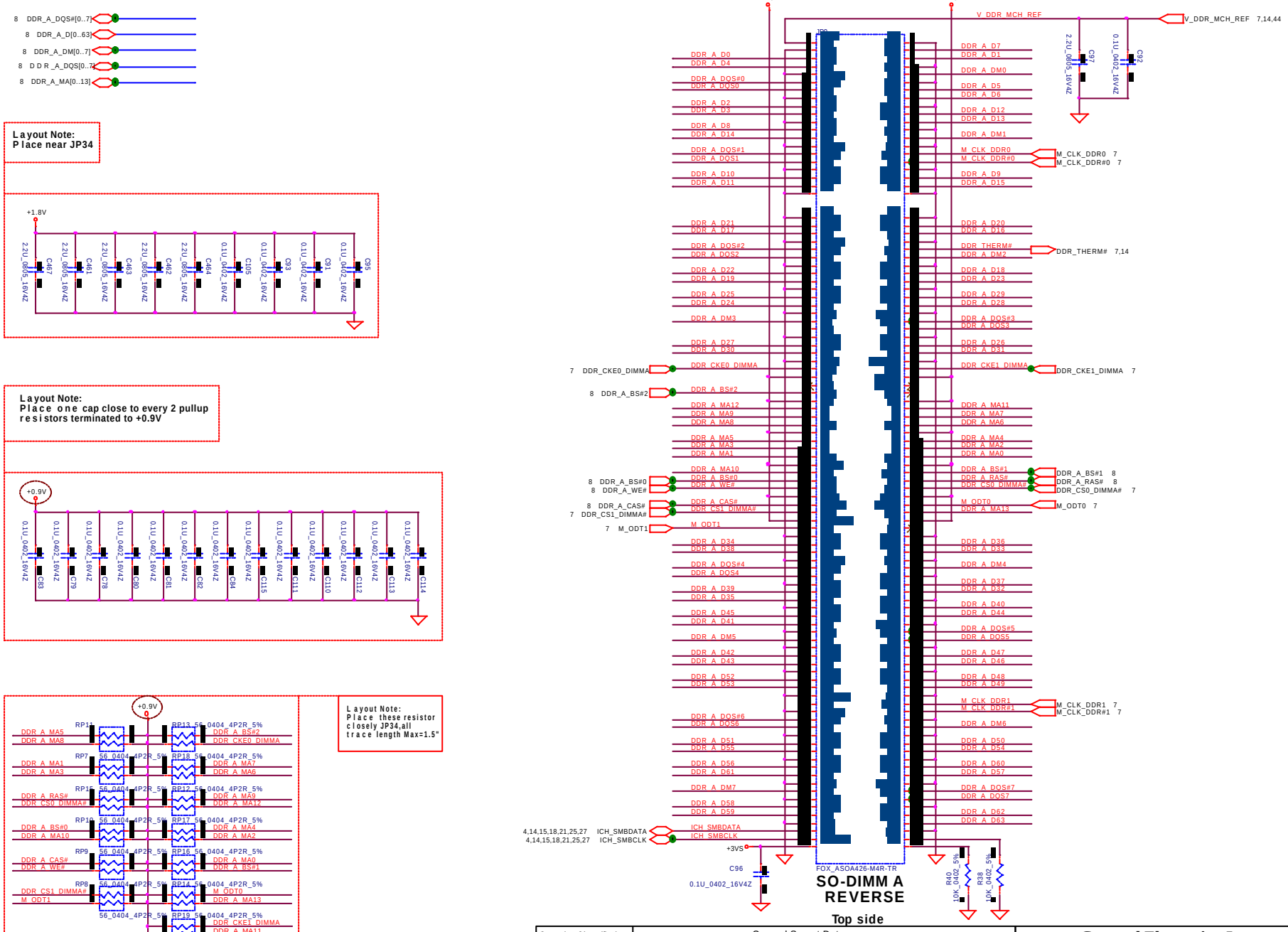

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Title	Compal Electronics, Inc.		
	DDRII-SODIMM SLOT1		
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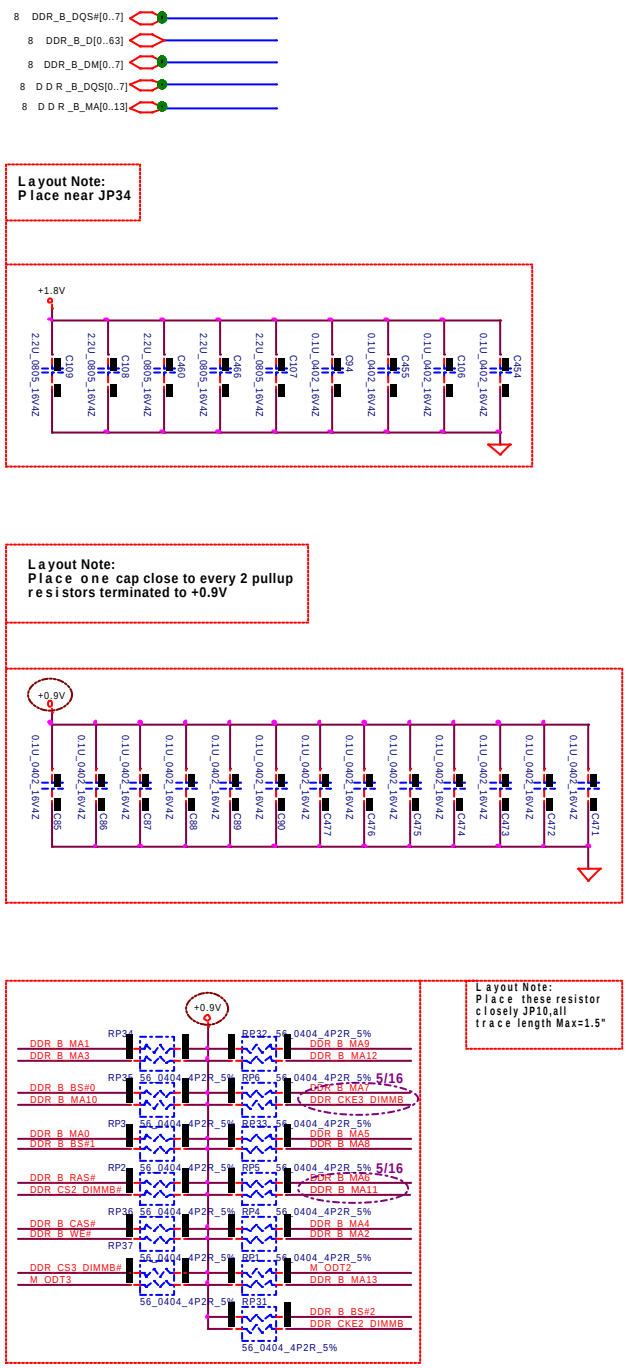

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Title: DDRII-SODIMM SLOT2

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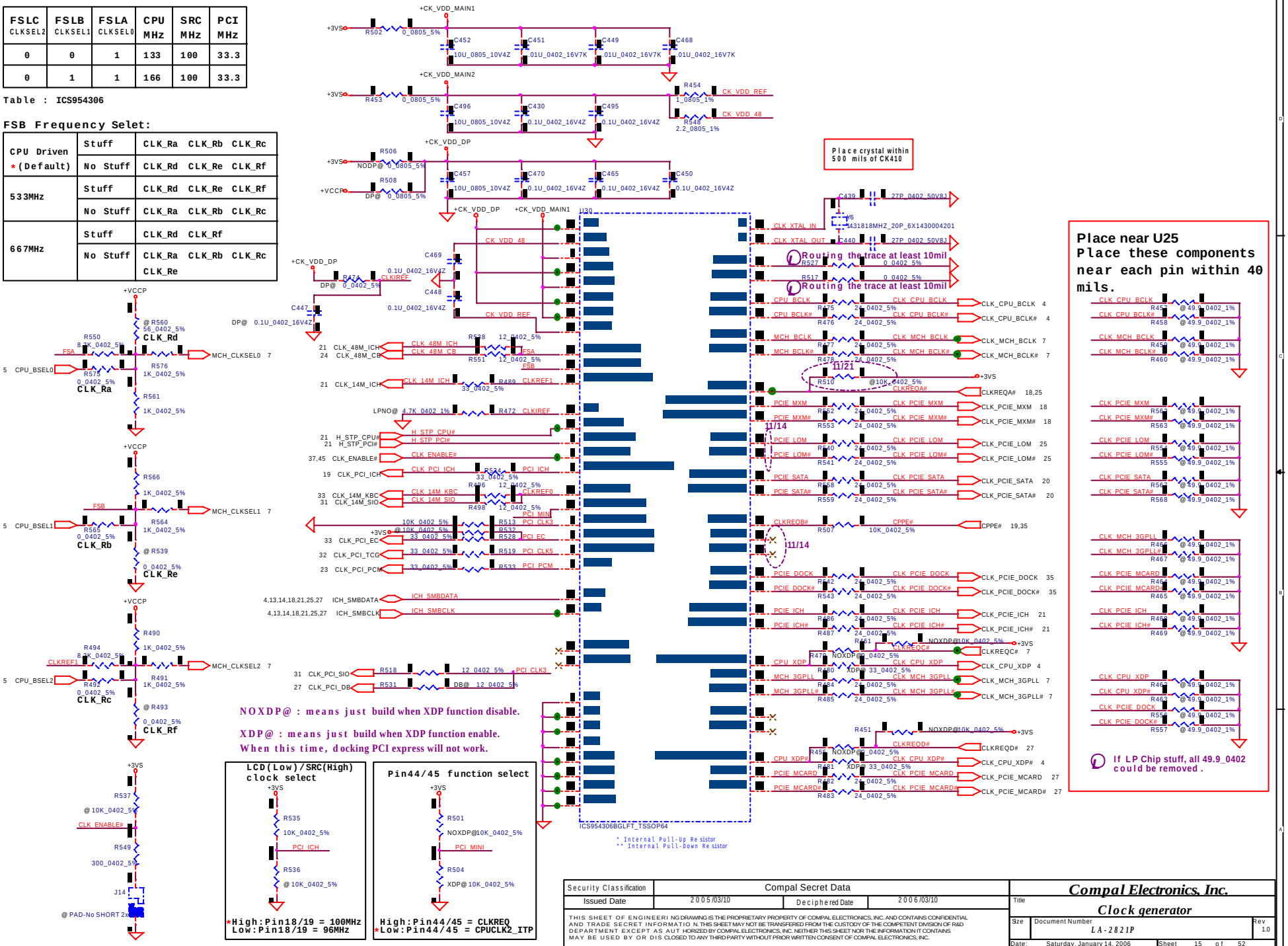
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS954306

FSB Frequency Selet:

CPU Driven *(Default)	Stuff	CLK_Ra CLK_Rb CLK_Rc
	No Stuff	CLK_Rd CLK_Re CLK_Rf
533MHz	Stuff	CLK_Rd CLK_Re CLK_Rf
	No Stuff	CLK_Ra CLK_Rb CLK_Rc
667MHz	Stuff	CLK_Rd CLK_Rf
	No Stuff	CLK_Ra CLK_Rb CLK_Rc CLK_Re



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Title: **Clock generator**

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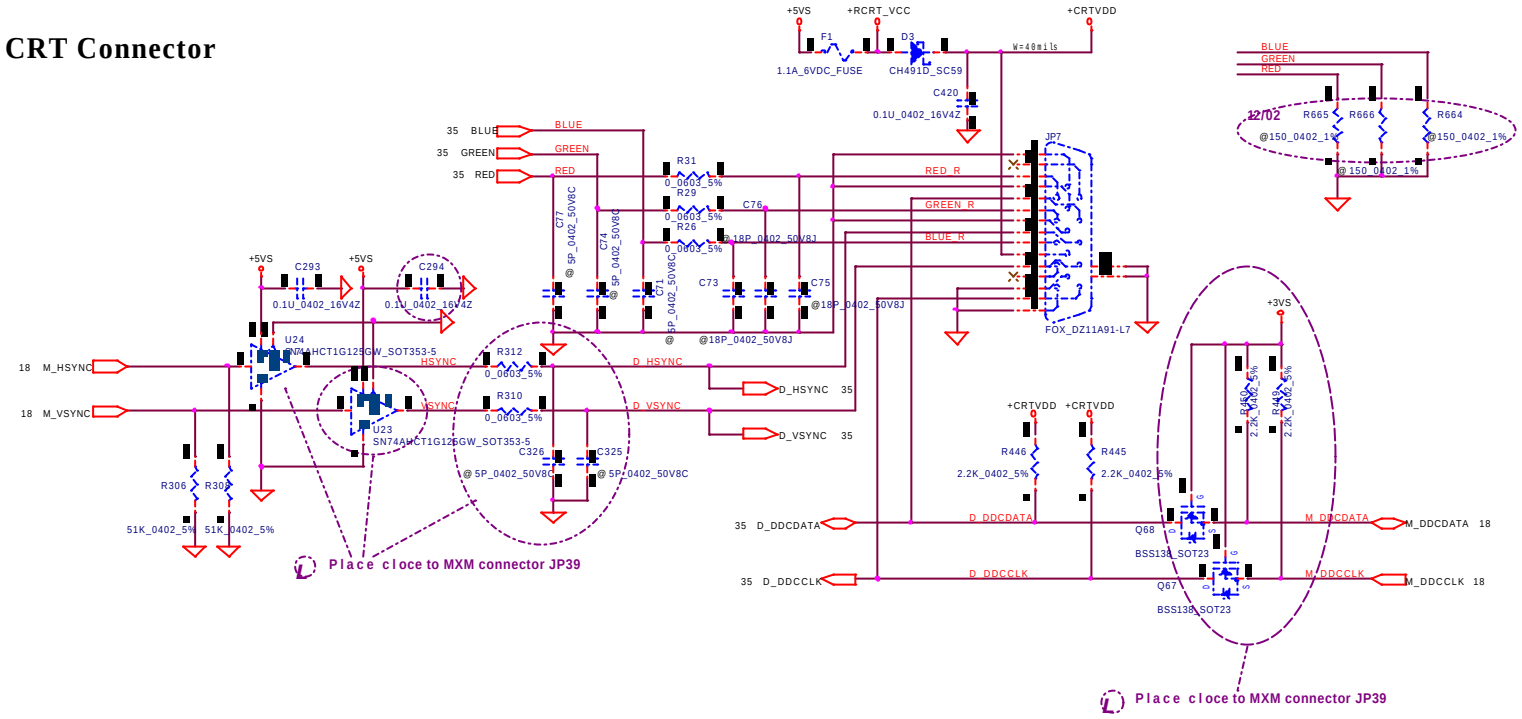
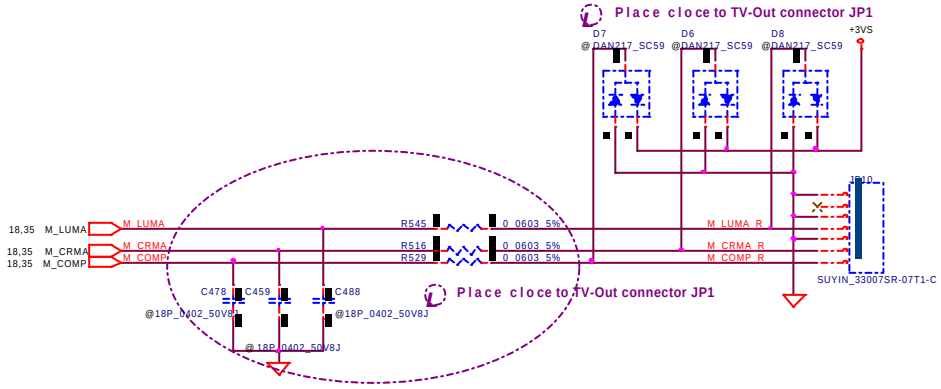
CRT Connector



TV-Out Connector



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title: CRT & TVout Connector

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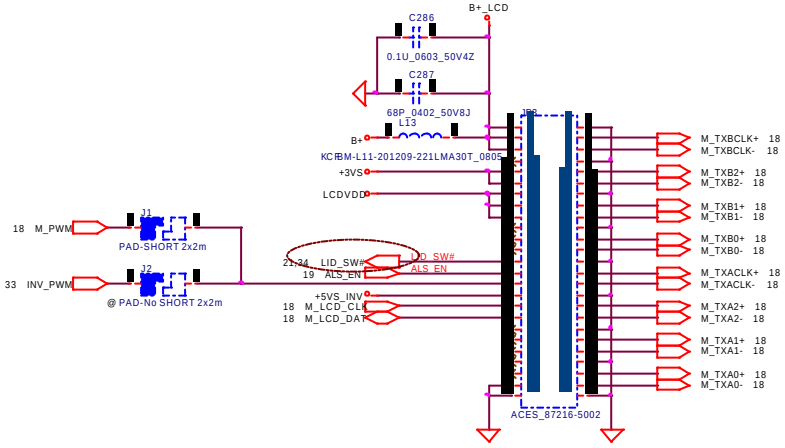
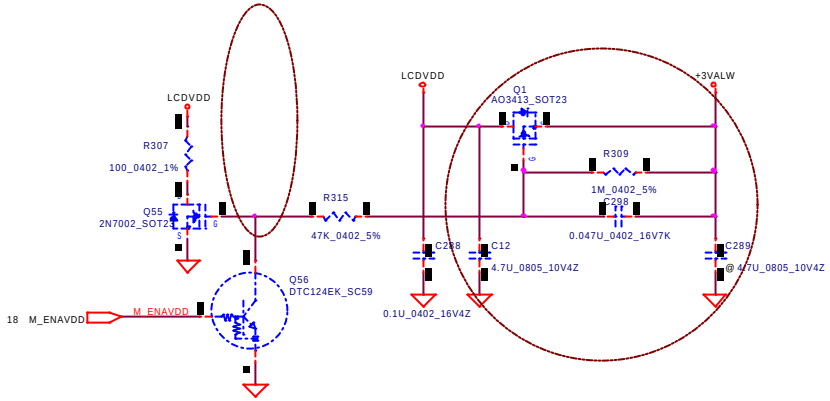
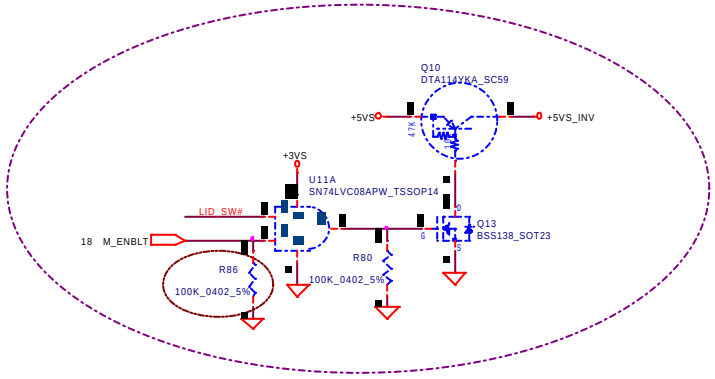
Date: Saturday, January 14, 2006 | Sheet 16 of 52

MXM LVDS CONN



LCD POWER CIRCUIT





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Issued Date	2005/03/10	Deciphered Date	2006/03/10

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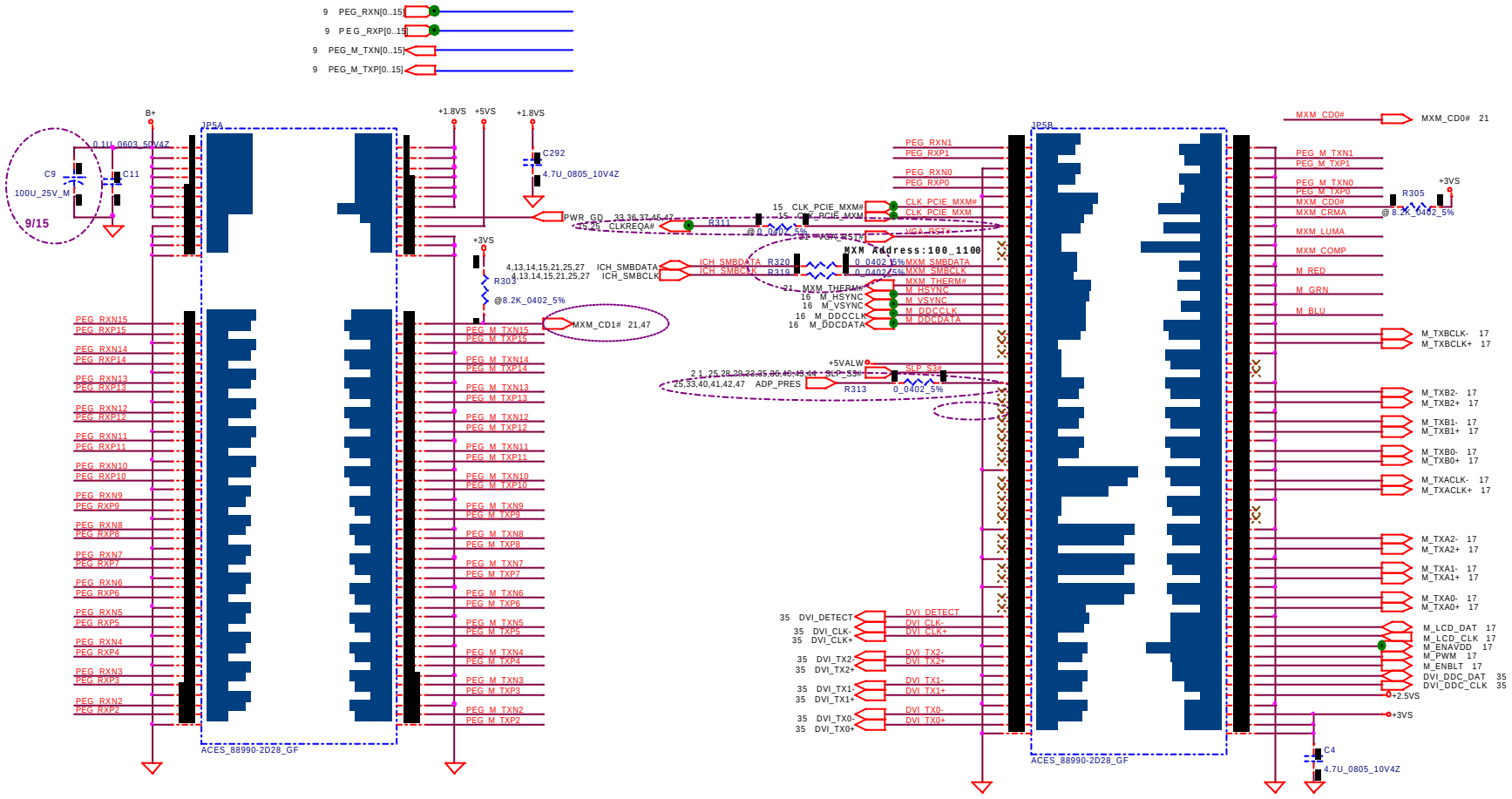
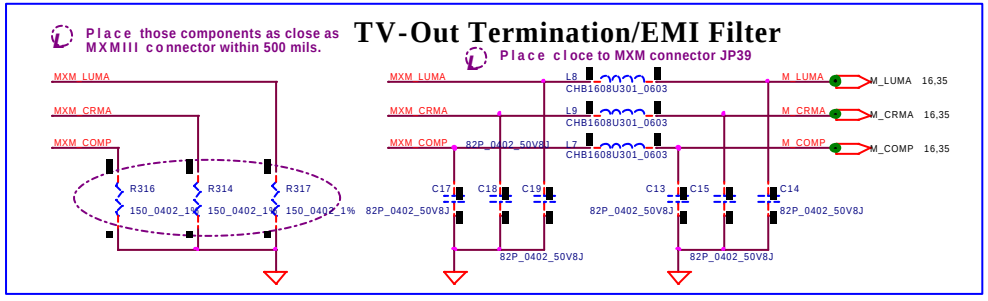
Compal Electronics, Inc.

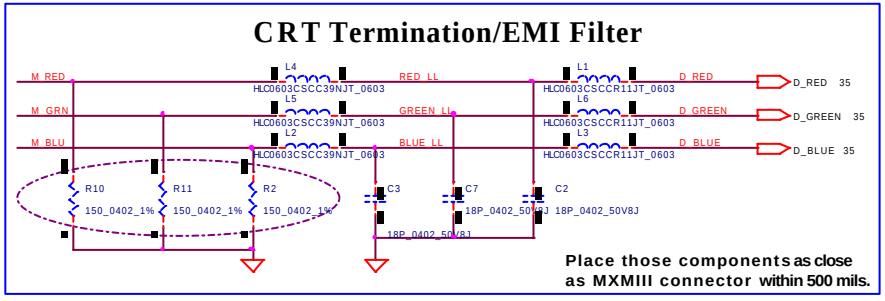
Title: **LCD CONN.**

Size | Document Number: LA-2821P | Rev: 1.0

Date: Saturday, January 14, 2006 | Sheet 17 of 52







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Issued Date	2005/03/10	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title: MXM III CONN

Size	Document Number	Rev
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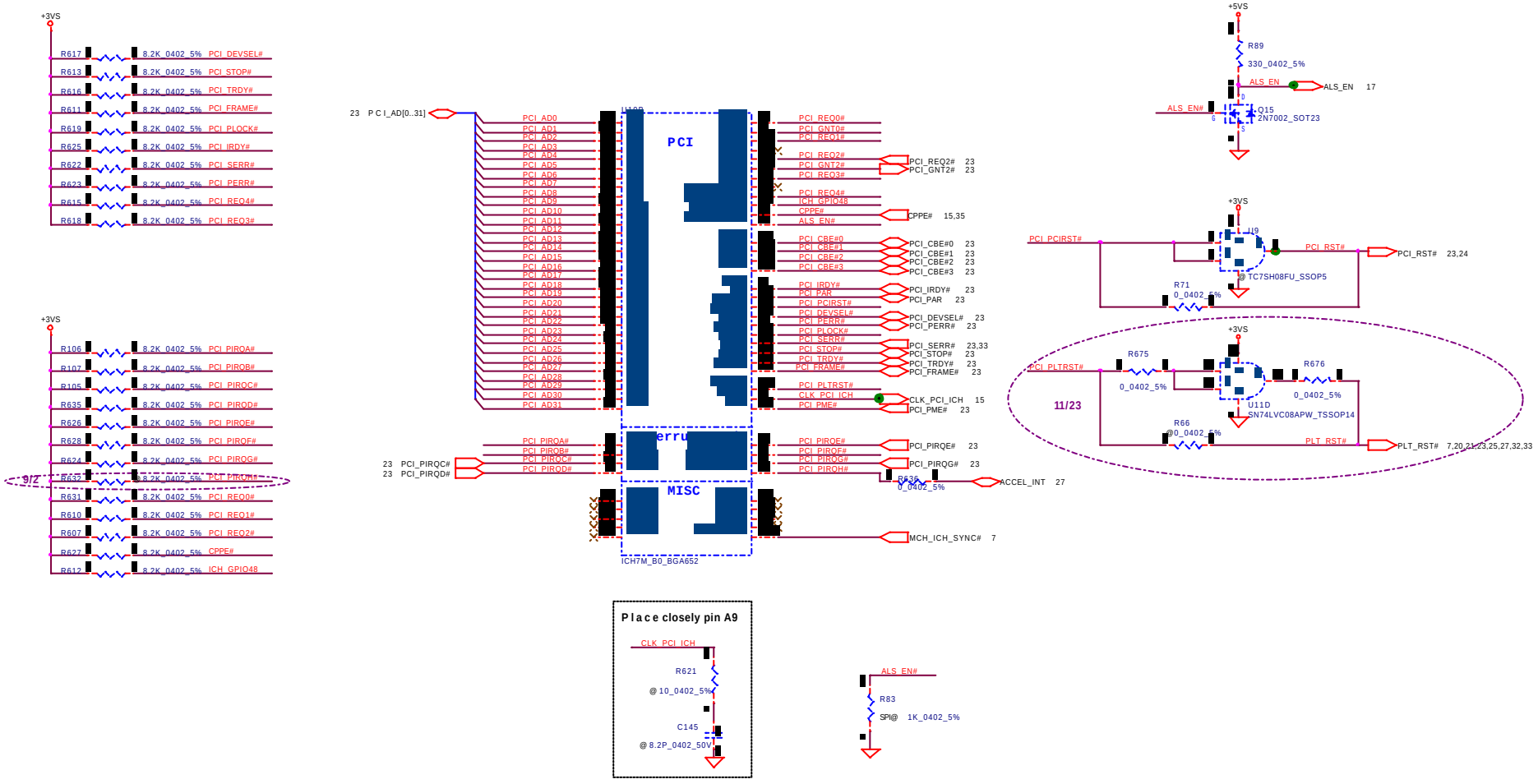

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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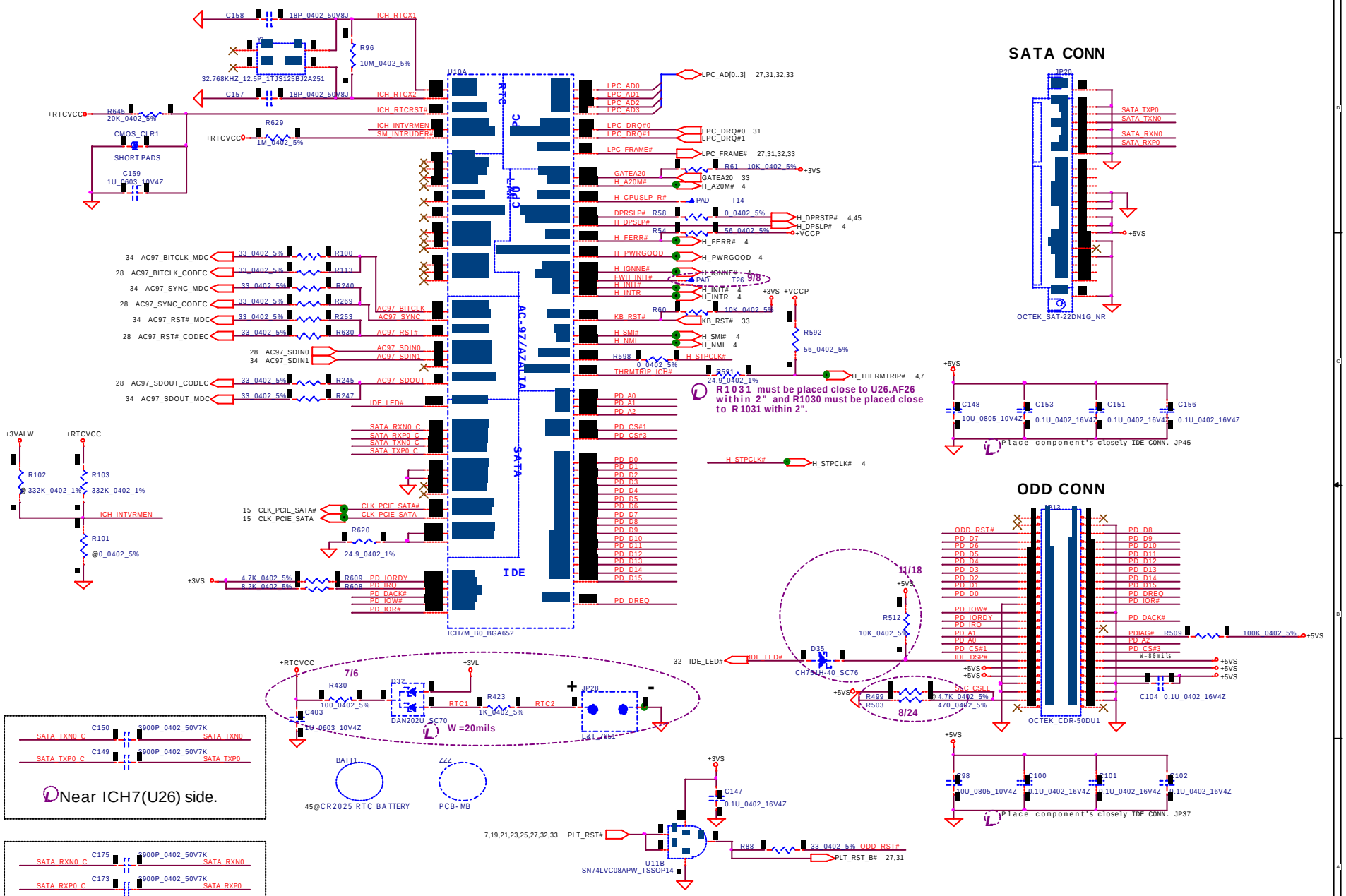
Compal Electronics, Inc.

Title: ICH7-M(1/4)

Size	Document Number	Rev
	LA-2821P	1.0

Date: Saturday, January 14, 2006 | Sheet 19 of 52



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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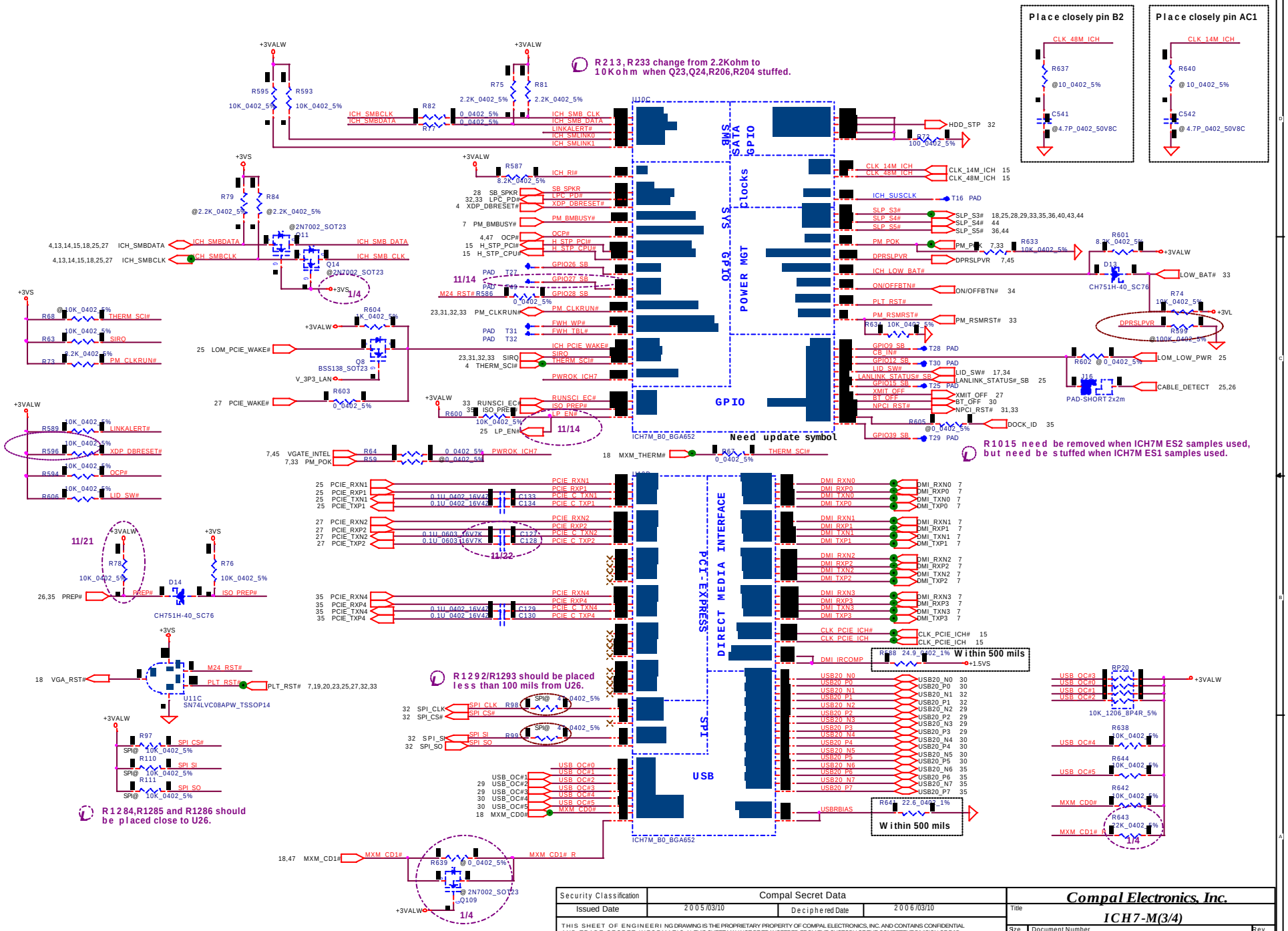
Compal Electronics, Inc.

Title: ICH7-M(2/4)

Size: | Document Number: LA-2821P | Rev: 1.0

Date: Saturday, January 14, 2006 | Sheet 20 of 52


Place closely pin B2
Place closely pin AC1
R213,R233 change from 2.2Kohm to 10Kohm when Q23,Q24,R206,R204 stuffed.
R1015 need be removed when ICH7M ES2 samples samples used, but need be stuffed when ICH7M ES1 samples used.
Need update symbol
ICH7M_B0_BGA652
GPIO
SMB
SATA
GPIO
Clocks
SAS
OD9
POWER MGT
PCI-EXPRESS
DIRECT MEDIA INTERFACE
SPI
USB
R1292/R1293 should be placed less than 100 mils from U26.
R1284,R1285 and R1286 should be placed close to U26.
Within 500 mils
Within 500 mils
U11C SN74LVC08APW_TSSOP14
CH751H-40_SC76
PAD-SHORT 2x2m
Security Classification
Compal Secret Data
Issued Date
2005/03/10
Deciphered Date
2006/03/10
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Compal Electronics, Inc.
Title
ICH7-M(3/4)
Size
Document Number
LA-2821P
Rev
1.0
Date: Saturday, January 14, 2006
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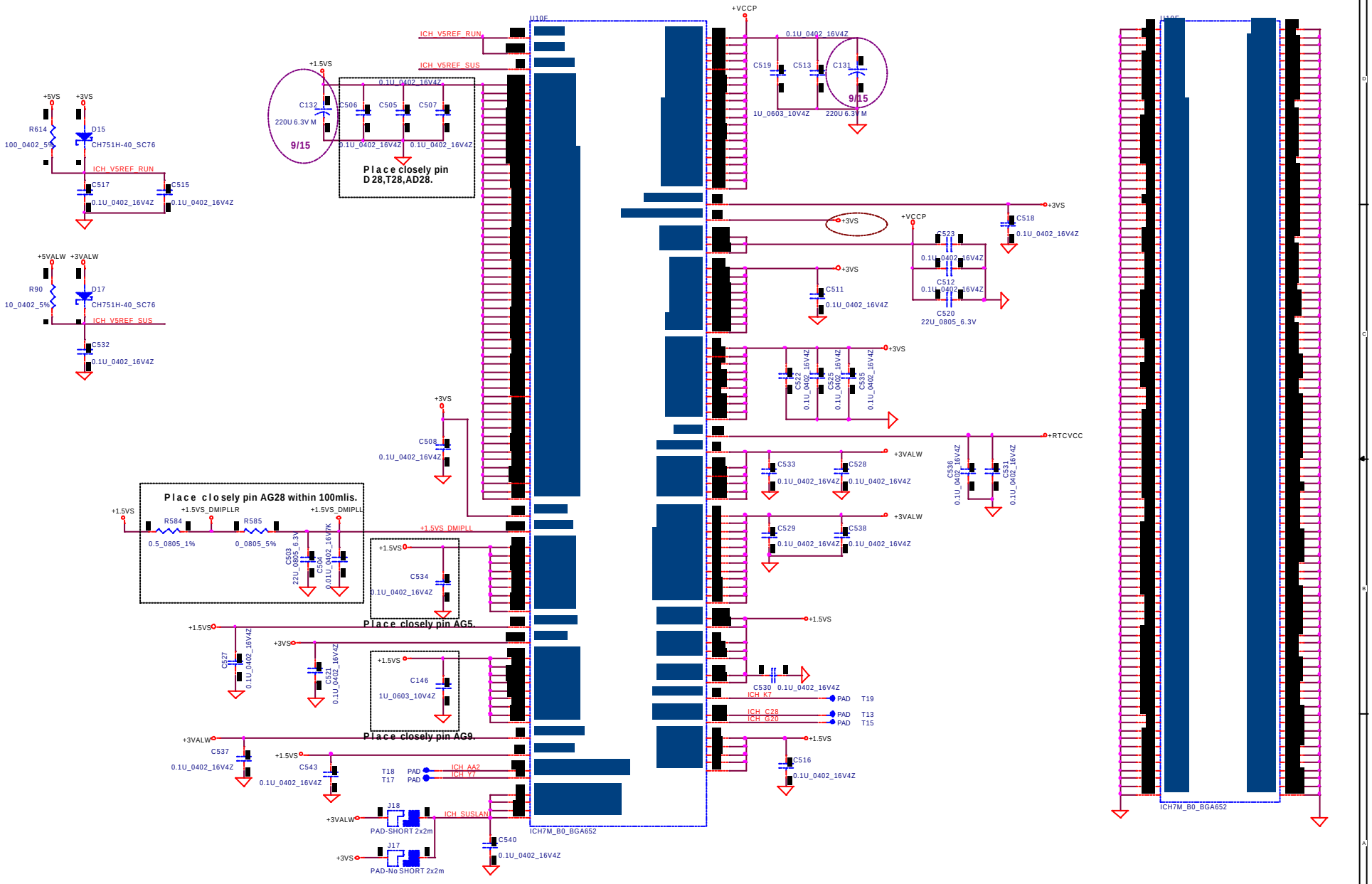

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Compal Electronics, Inc.

Title: ICH7-M(4/4)

Size	Document Number	Rev
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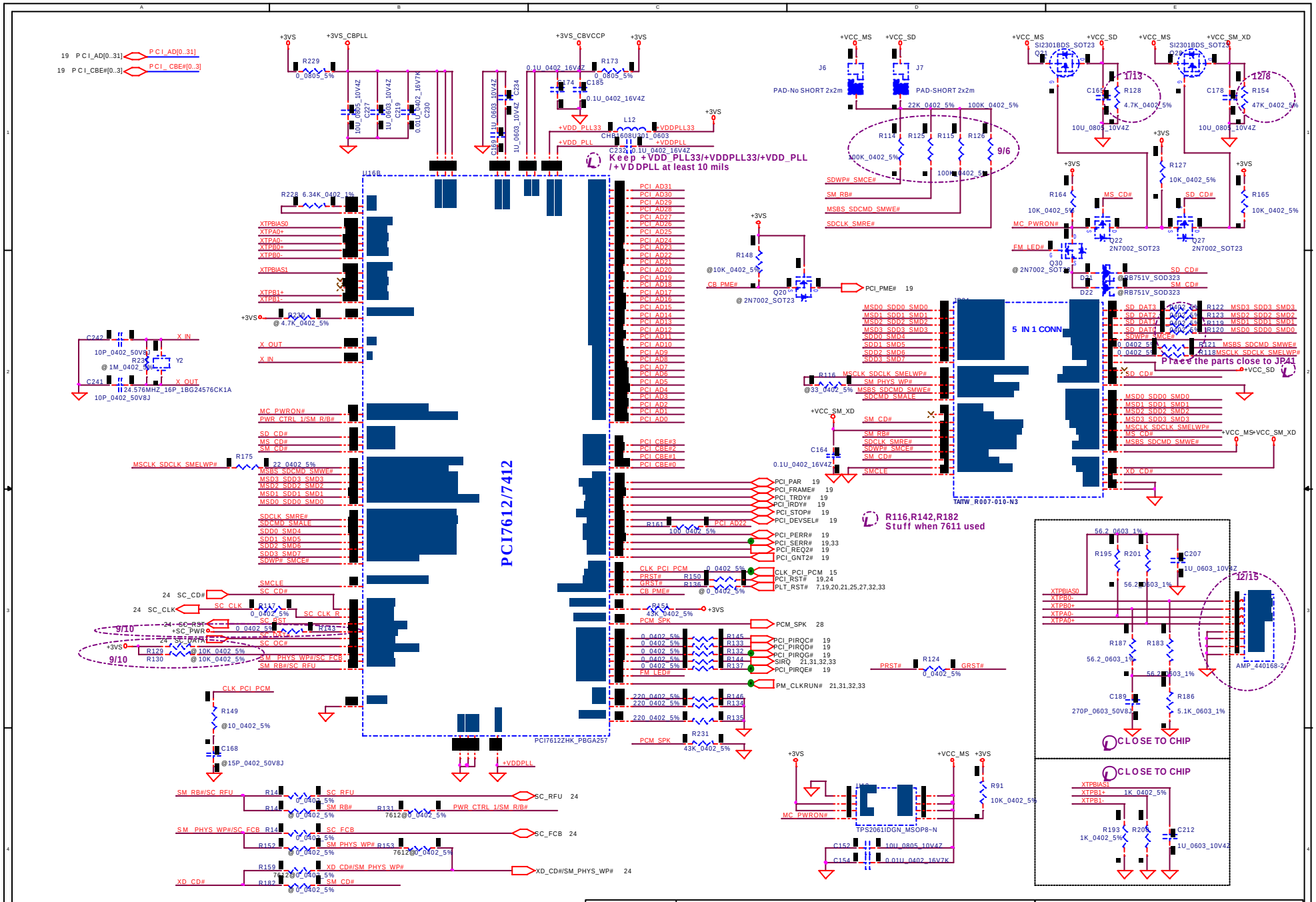
Date: Saturday, January 14, 2006 | Sheet 22 of 52



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title: TI PCI7612 PCI/CardReader

Size	Document Number	Rev
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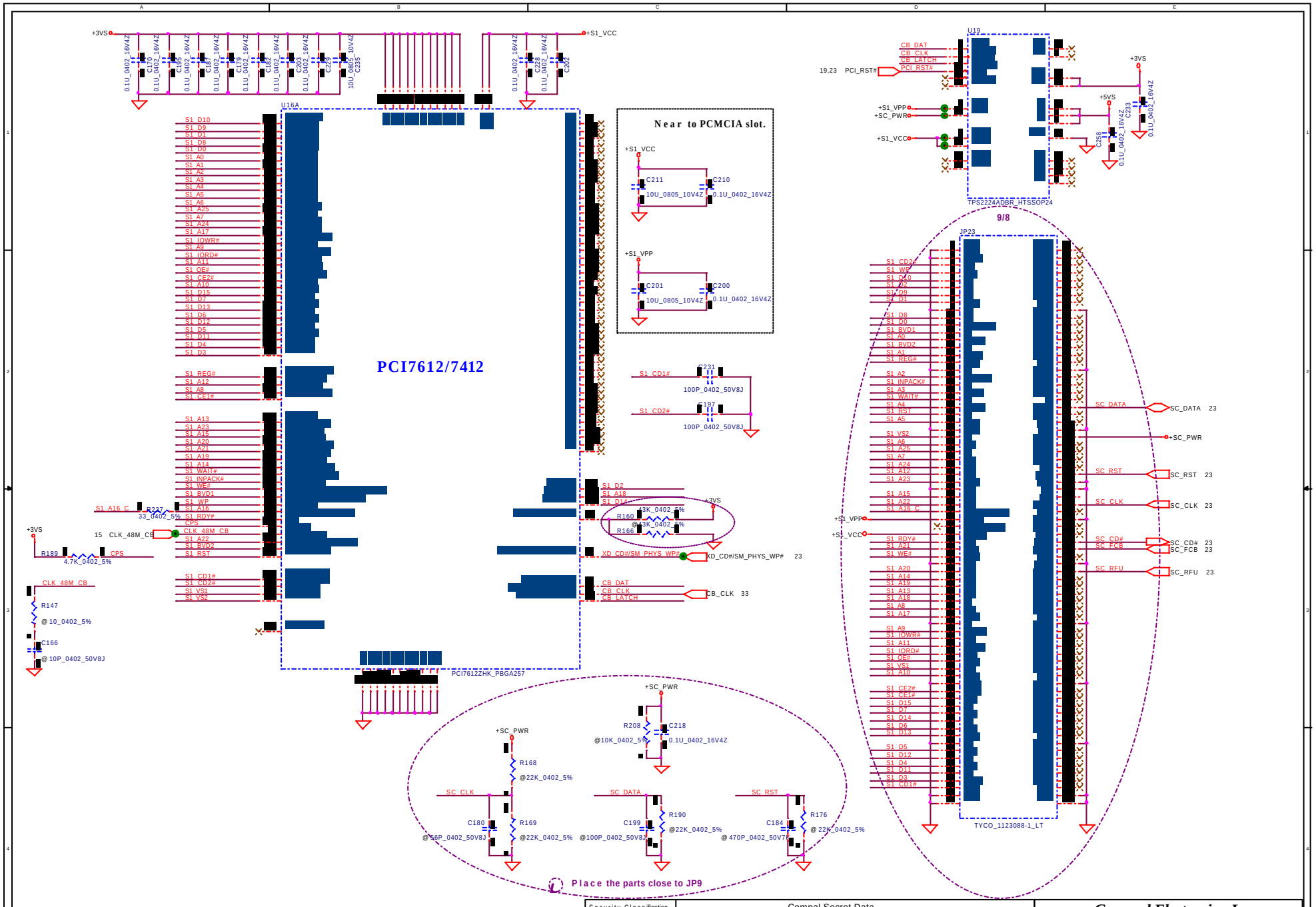

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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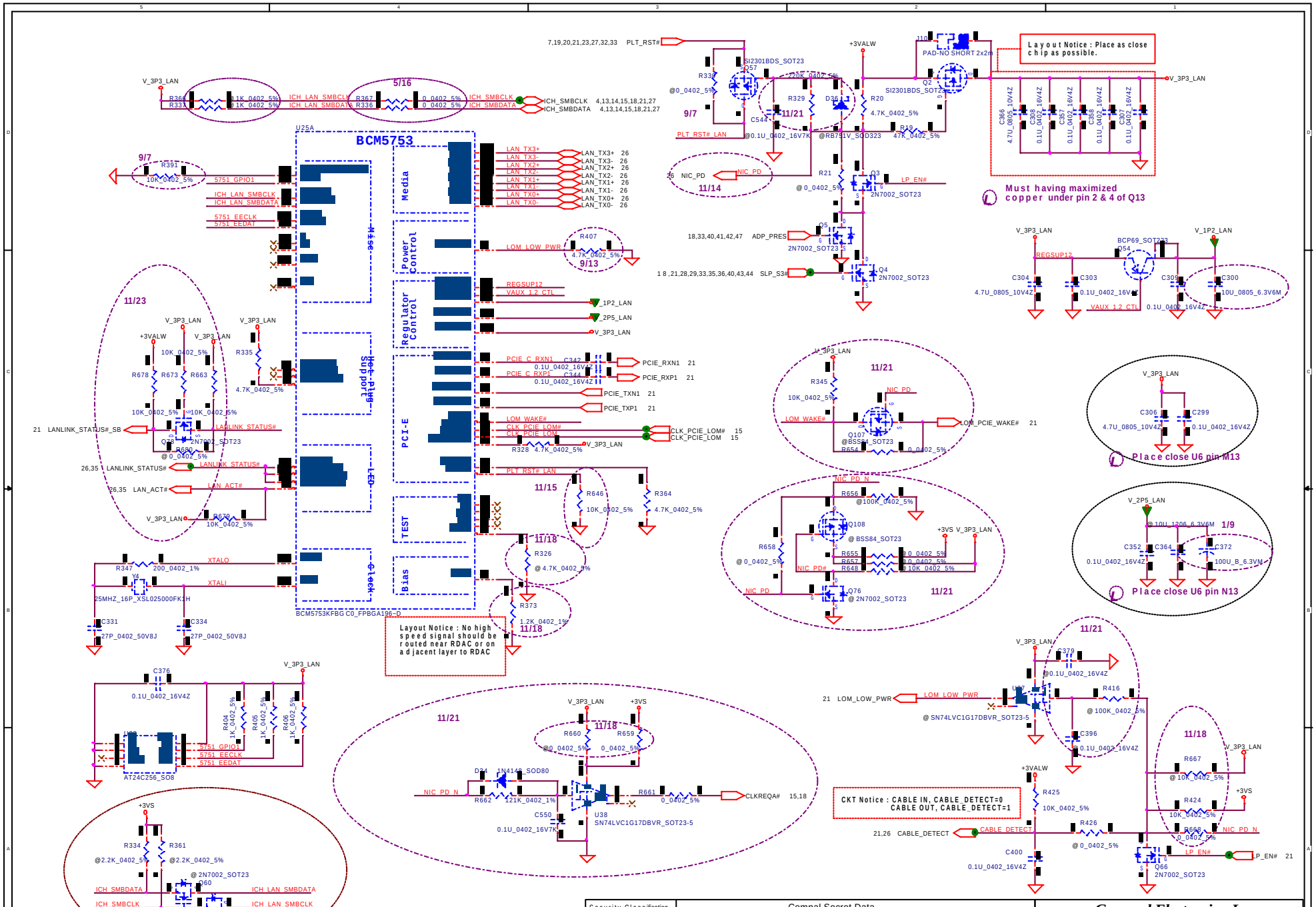
Compal Electronics, Inc.

Title: TI PCI7612 CB/SmartCard

Size | Document Number: LA-2821P | Rev: 1.0

Date: Saturday, January 14, 2006 | Sheet 24 of 52



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Issued Date	2005/03/10	Deciphered Date	2006/03/10

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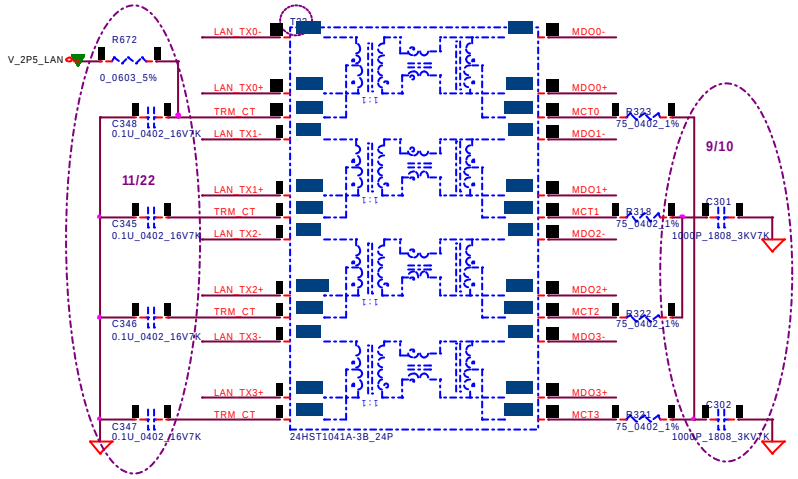
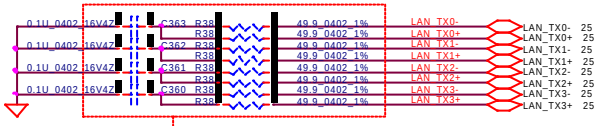
Compal Electronics, Inc.

Title: BCM5753M

Size: | Document Number: LA-2821P | Rev: 1.0

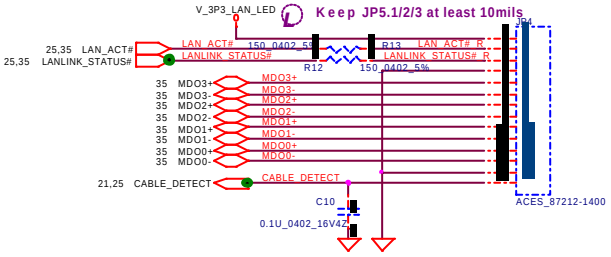
Date: Saturday, January 14, 2006 | Sheet 25 of 52

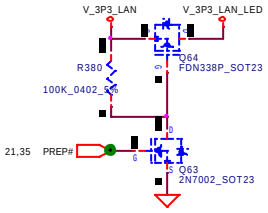


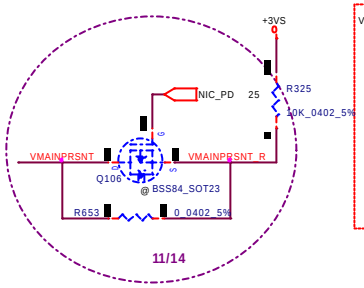


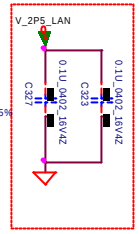
Layout Notice : Place termination as close as BCM5753M as possible

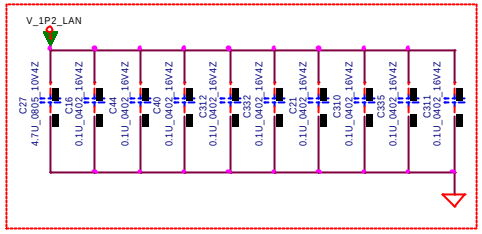
To RJ-45 CONN.



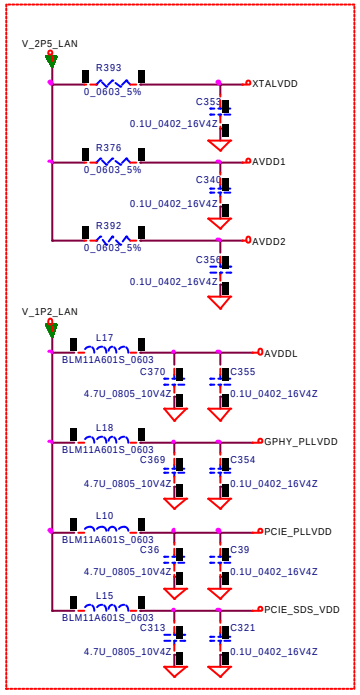


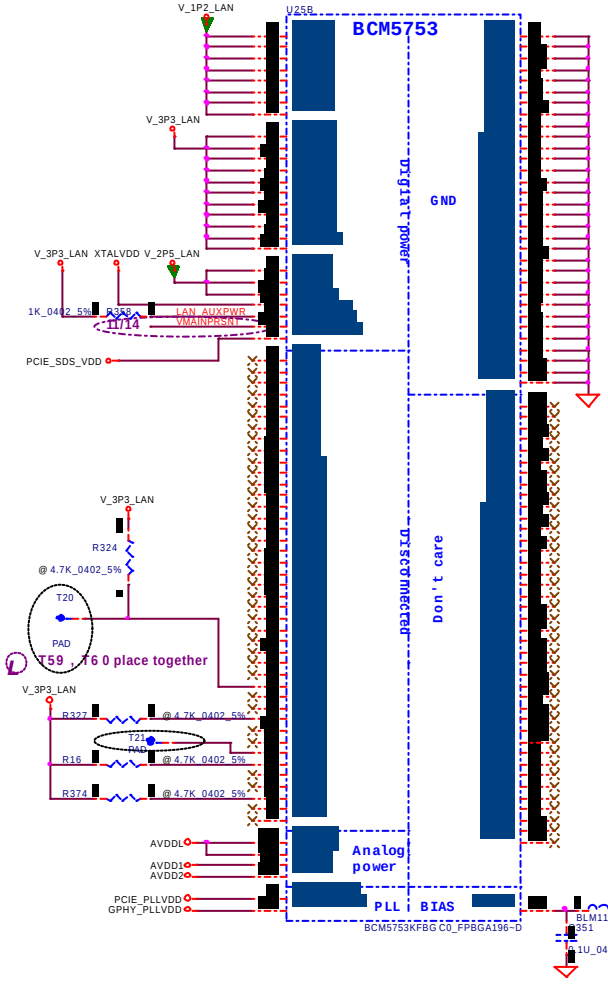






Layout Notice : Filter place as close chip as possible.





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Compal Electronics, Inc.

Title: Magnetic & RJ45/RJ11

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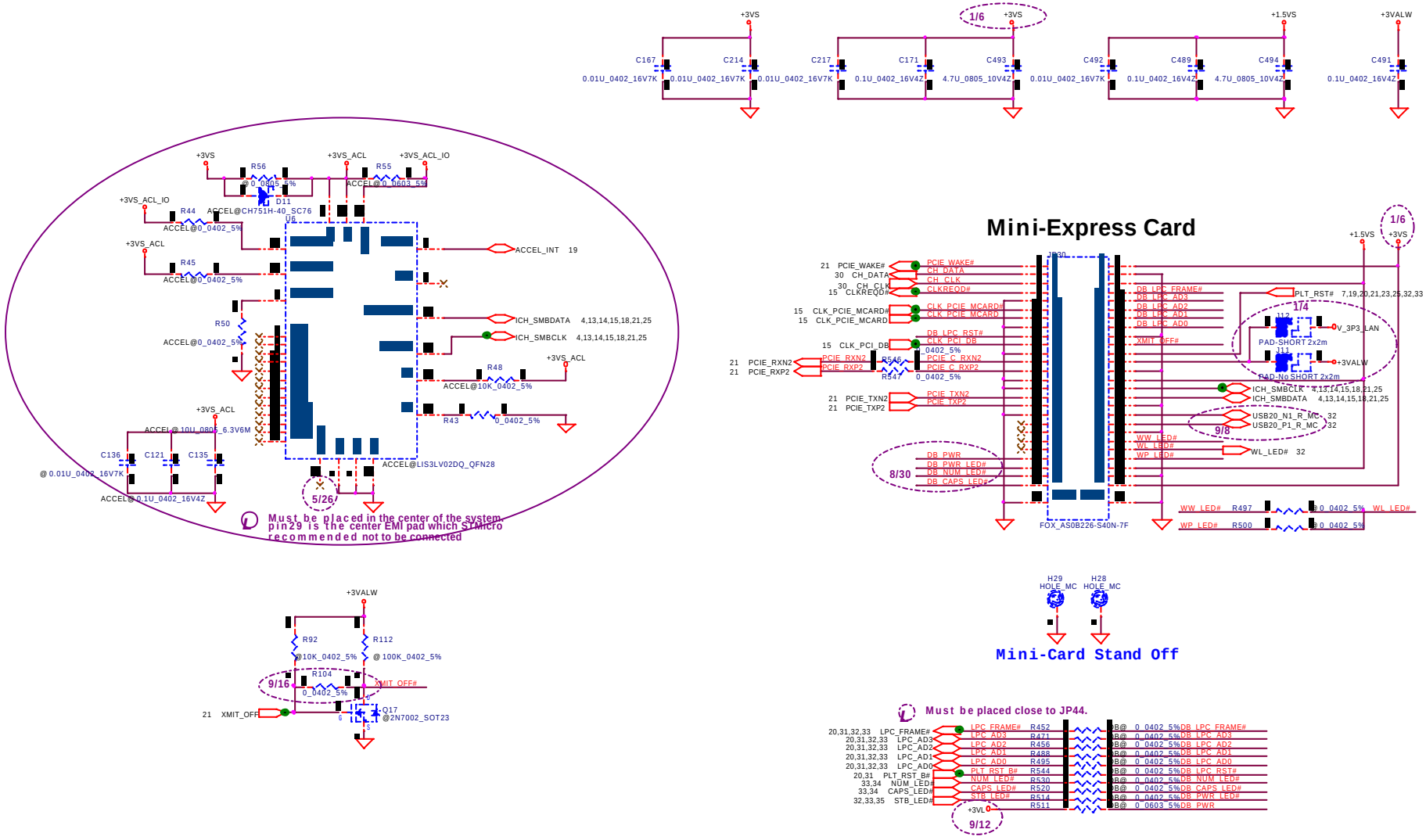

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Issued Date	2005/03/10	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title: Mini-Card/Mini-PCI/Accelerometer

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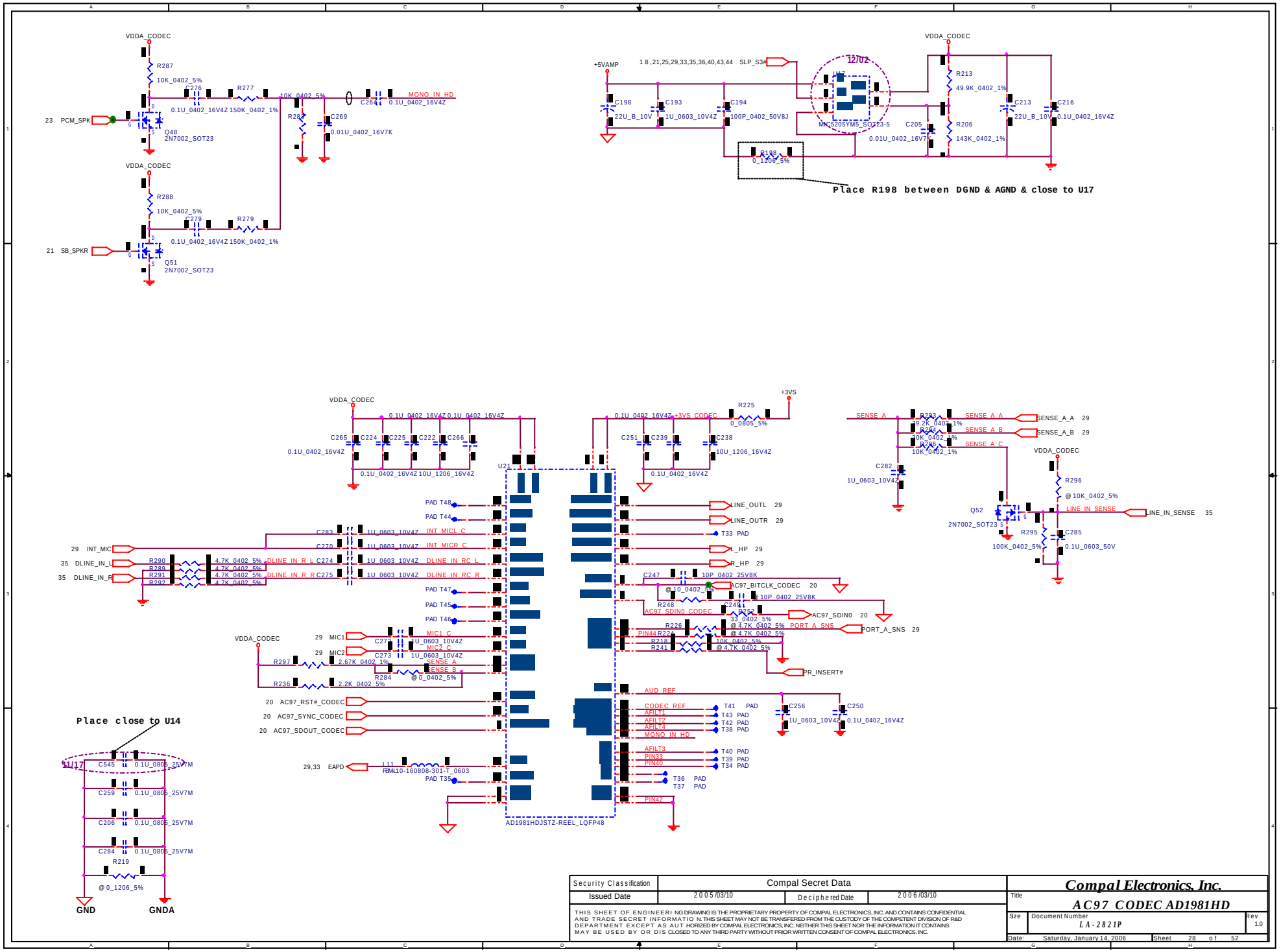
Date: Saturday, January 14, 2006 | Sheet 27 of 52



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Compal Electronics, Inc.

Title: **AC97 CODEC AD1981HD**

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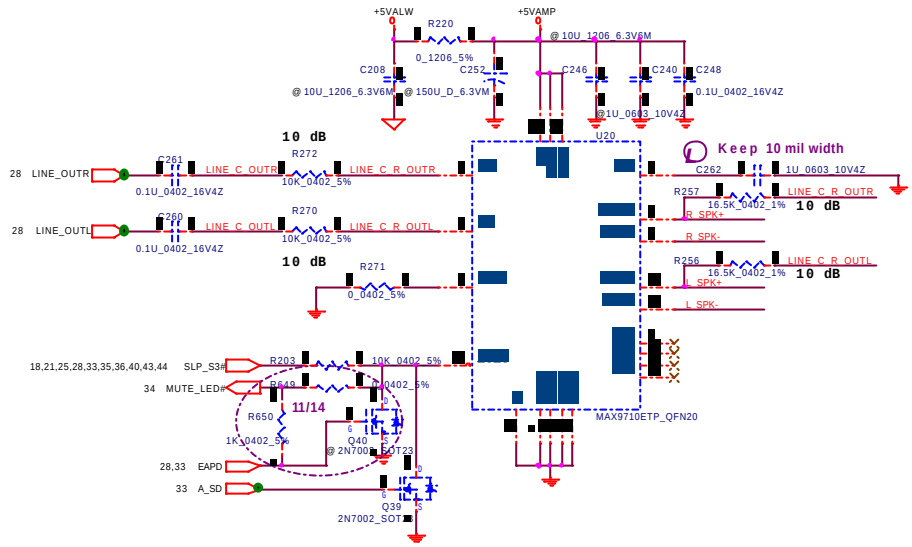
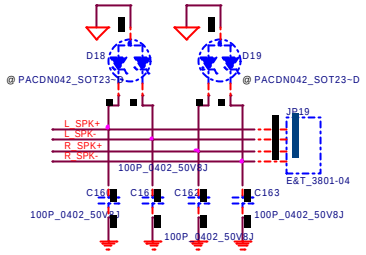
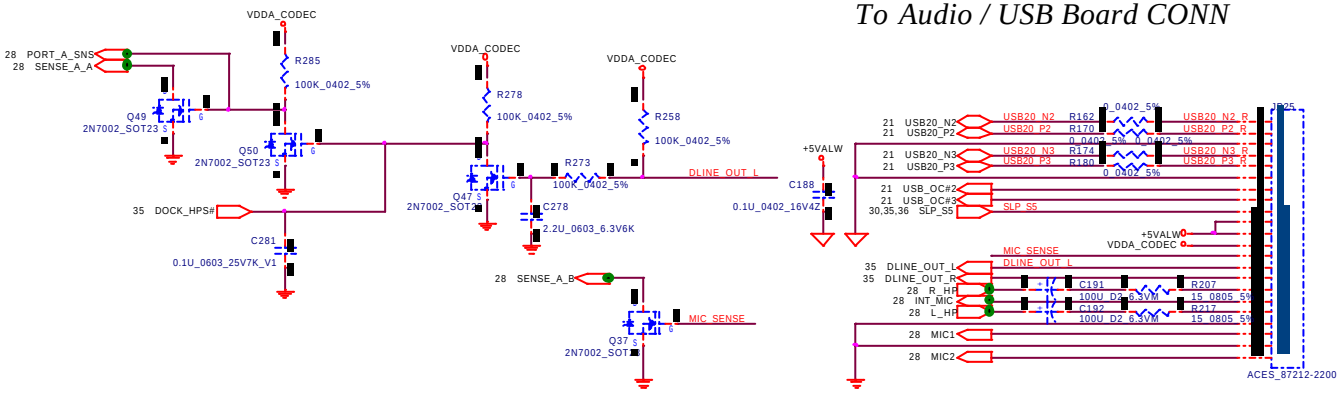
AMP. FOR INTERNAL SPEAKER





U39 Gain Settings		
GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

To Audio / USB Board CONN



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Compal Electronics, Inc.

Title: **AMP & Audio Jack**

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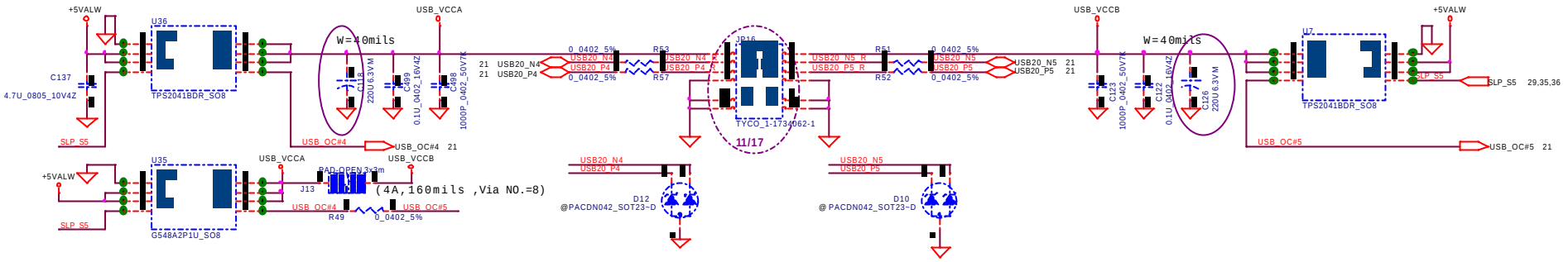
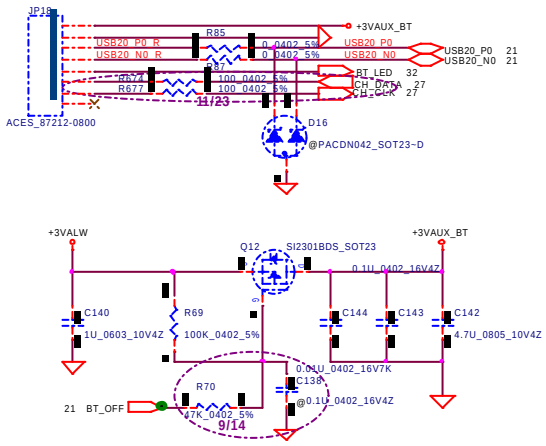
USB CONNECTOR 1



BT Connector



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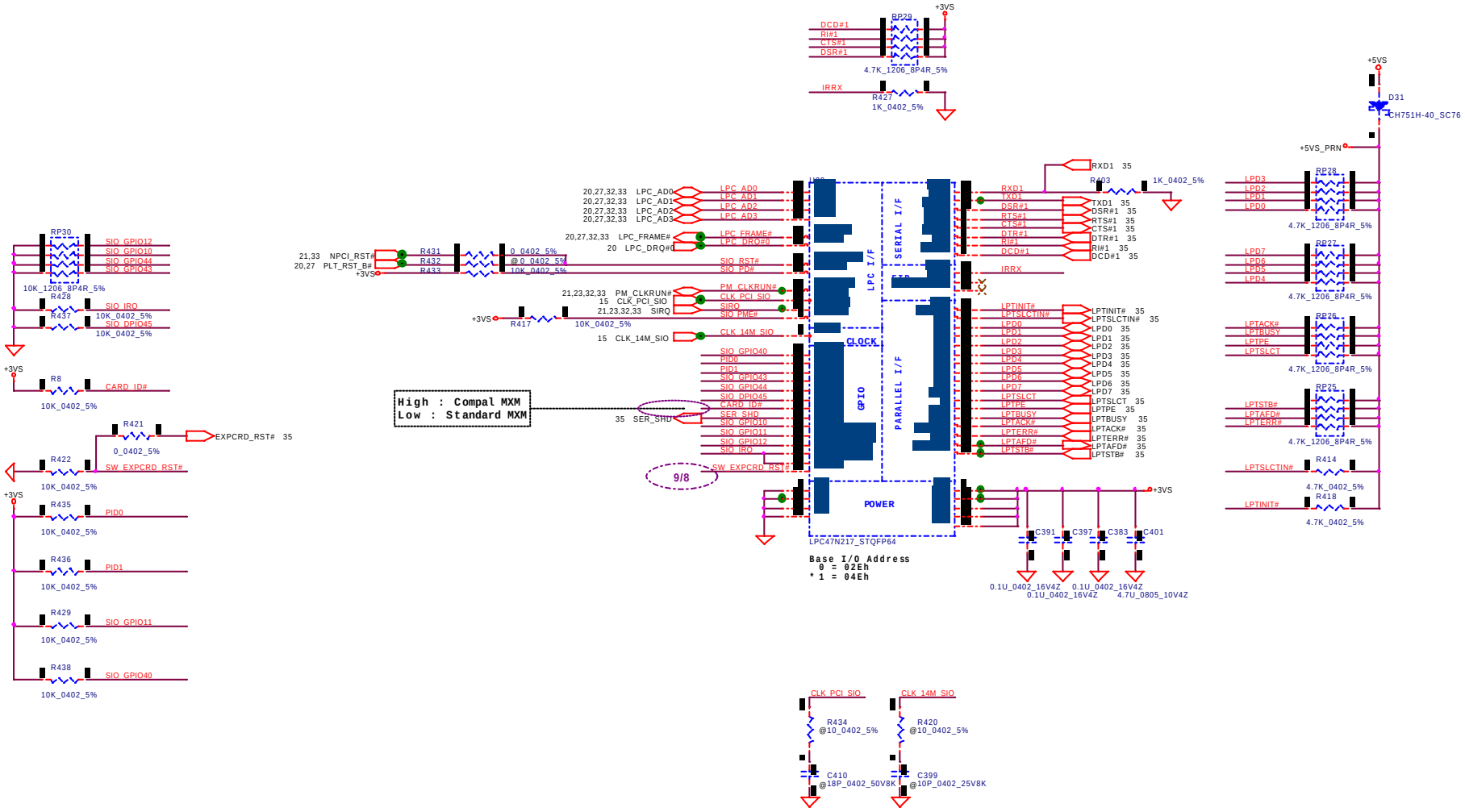
Compal Electronics, Inc.

Title: USB I/O & BT Connector

Size: | Document Number: LA-2821P | Rev: 1.0

Date: Saturday, January 14, 2006 | Sheet 30 of 52



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Issued Date	2005/03/10	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title: **SUPER I/O LPC47N217**

Size | Document Number: LA-2821P | Rev: 1.0

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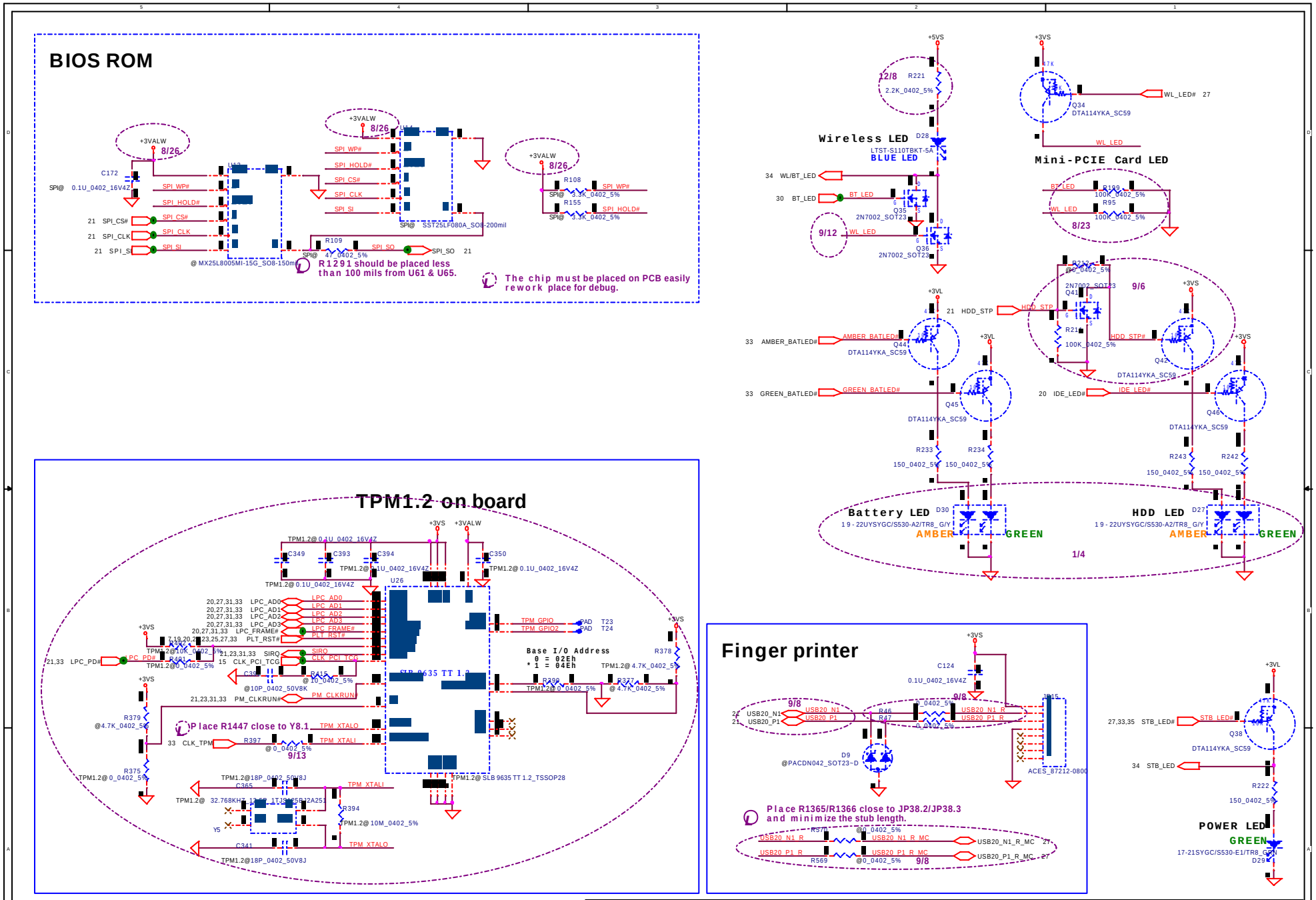

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Issued Date	2005/03/10	Deciphered Date	2006/03/10

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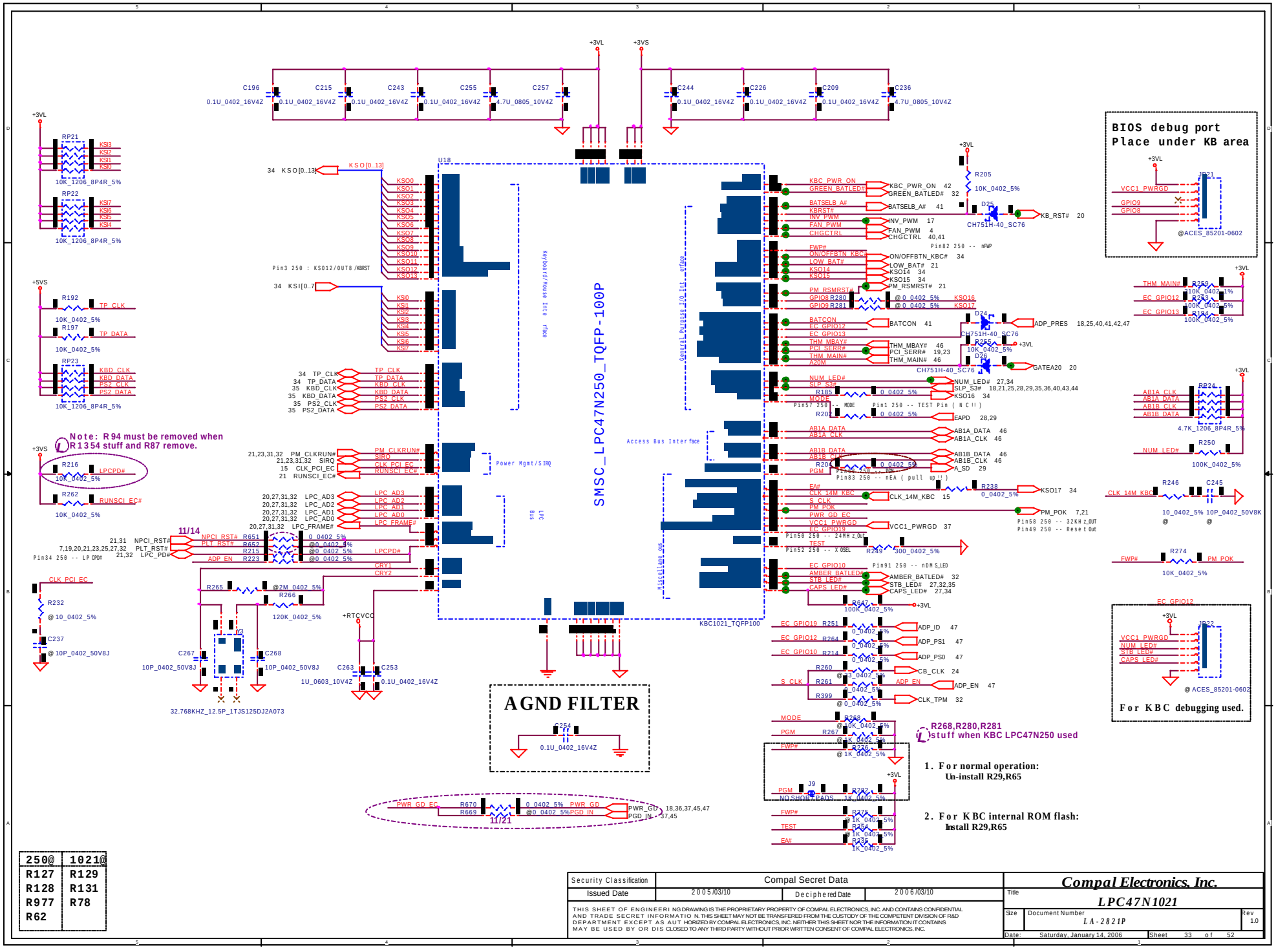
Compal Electronics, Inc.

Title: TCG/BIOS ROM/PS2/LED/SW

Size | Document Number: LA-2821P | Rev: 1.0

Date: Saturday, January 14, 2006 | Sheet 32 of 52



250@	1021@
R127	R129
R128	R131
R977	R78
R62	

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Issued Date	2005/03/10	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title: LPC47N1021

Size: | Document Number: LA-2821P | Rev: 1.0

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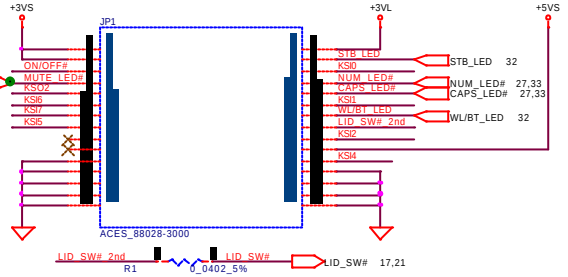
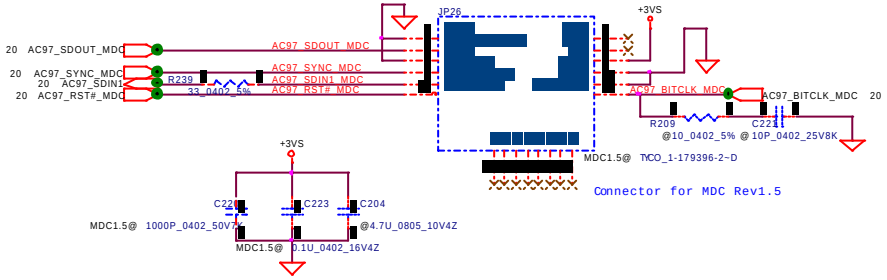
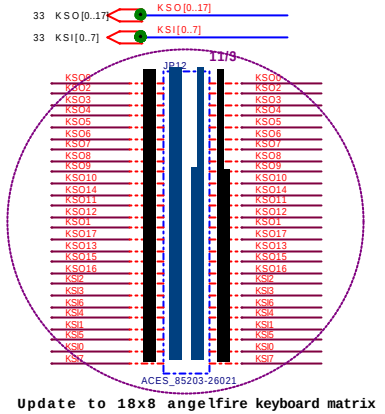
SWITCH BOARD.



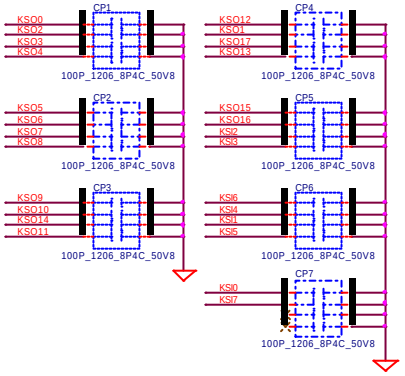
MDC 1.5 Conn.



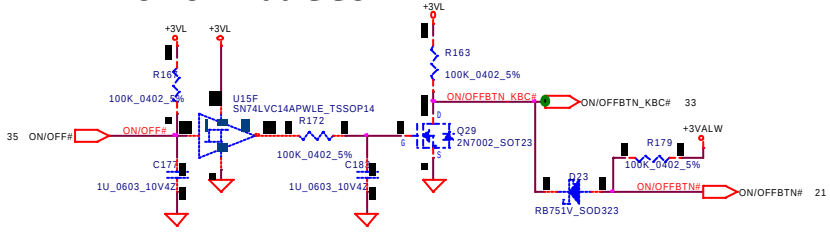
INT_KBD CONN.



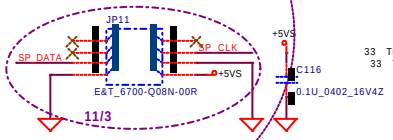
Update to 18x8 angelfire keyboard matrix



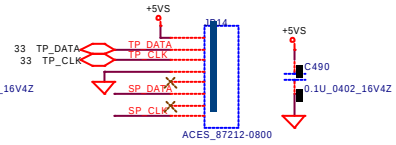
Power button



TrackPoint CONN.



T/P BOARD.



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Compal Electronics, Inc.

Title: MDC/KBD/ON_OFF/LID

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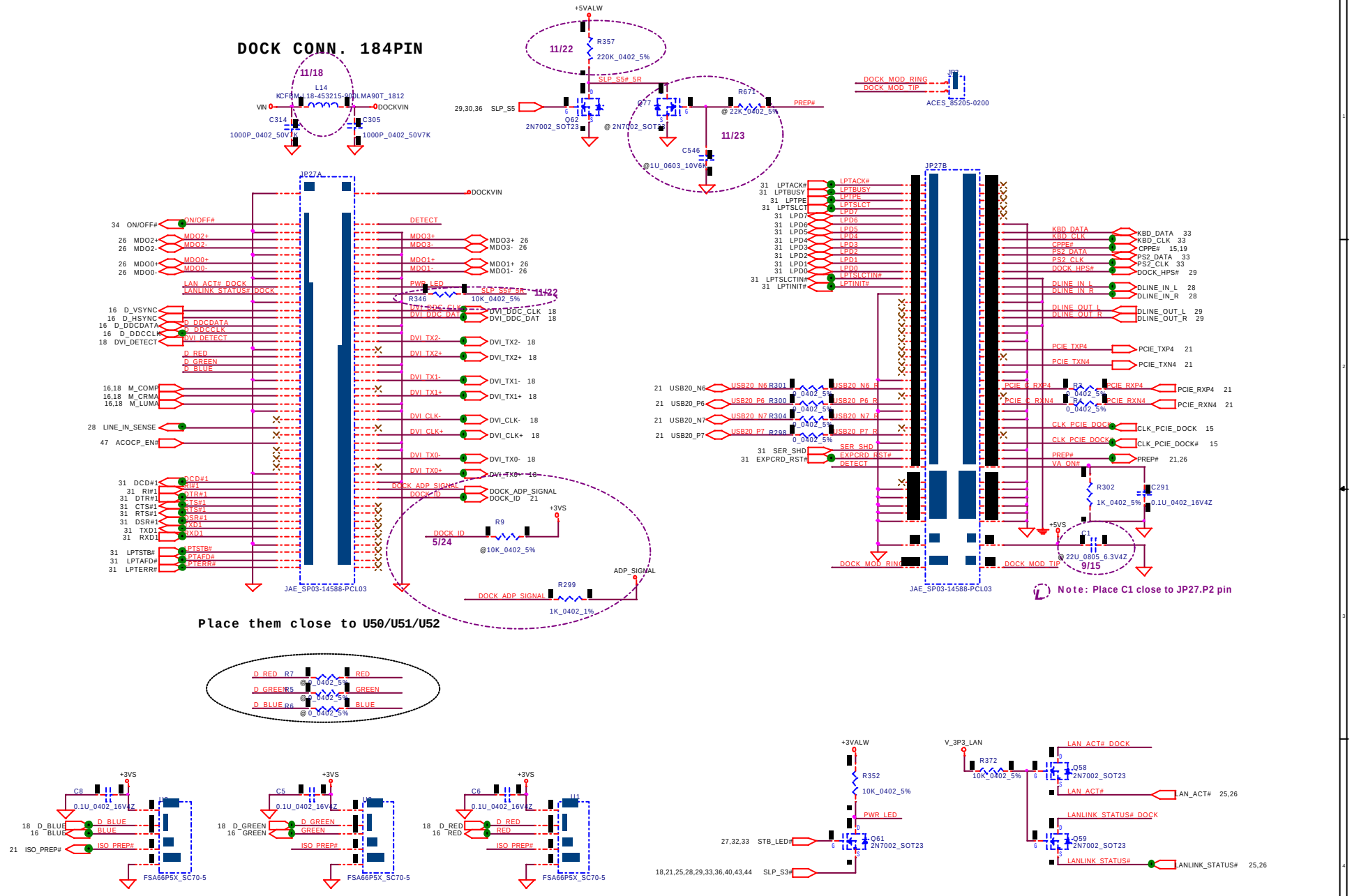
DOCK CONN. 184PIN



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Issued Date	2005/03/10	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title: **Docking CONN.**

Size	Document Number	Rev
	LA-2821P	1.0

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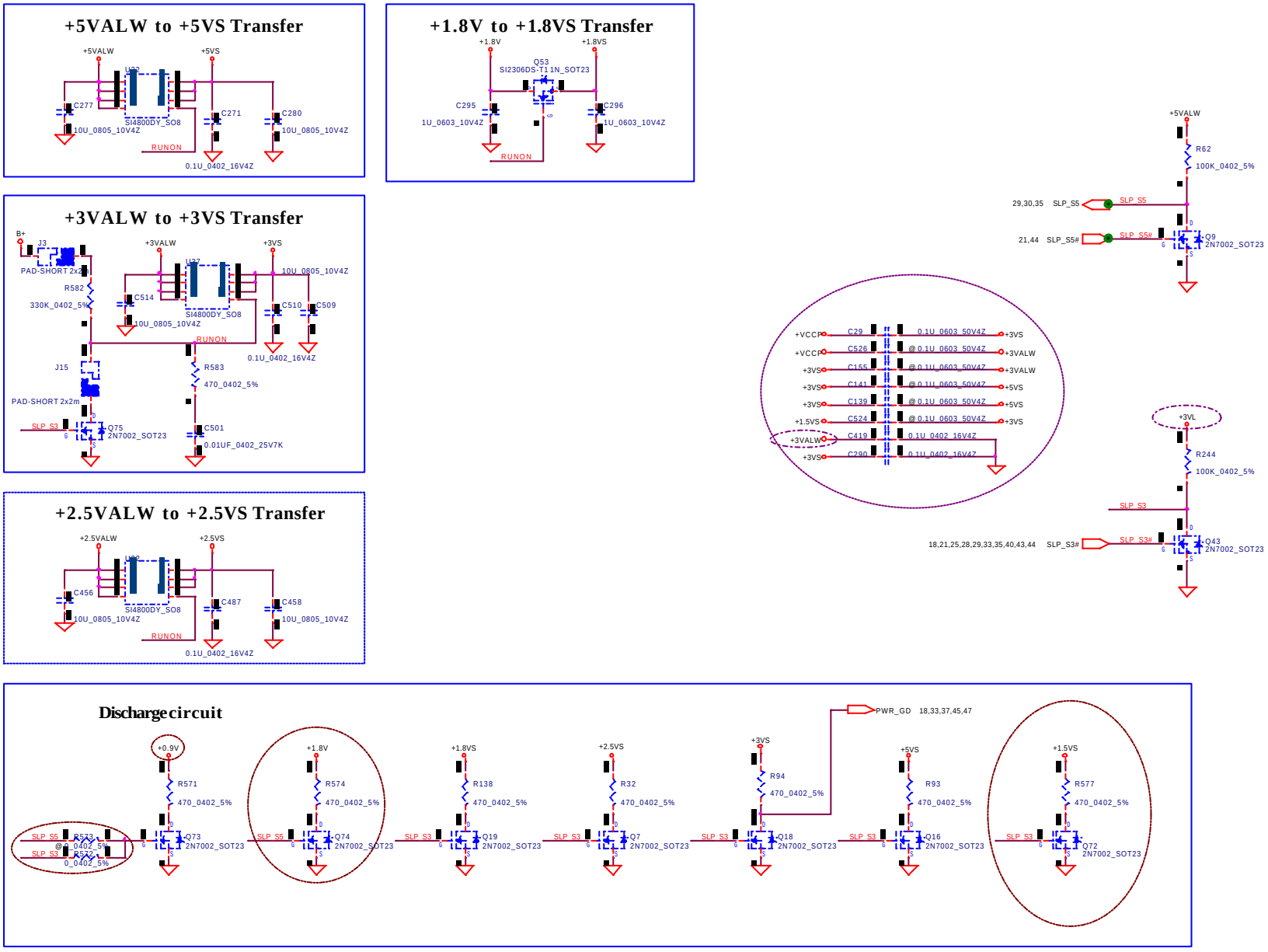

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Compal Electronics, Inc.

Title: **DC/DC Circuits**

Size	Document Number	Rev
	LA-2821P	1.0

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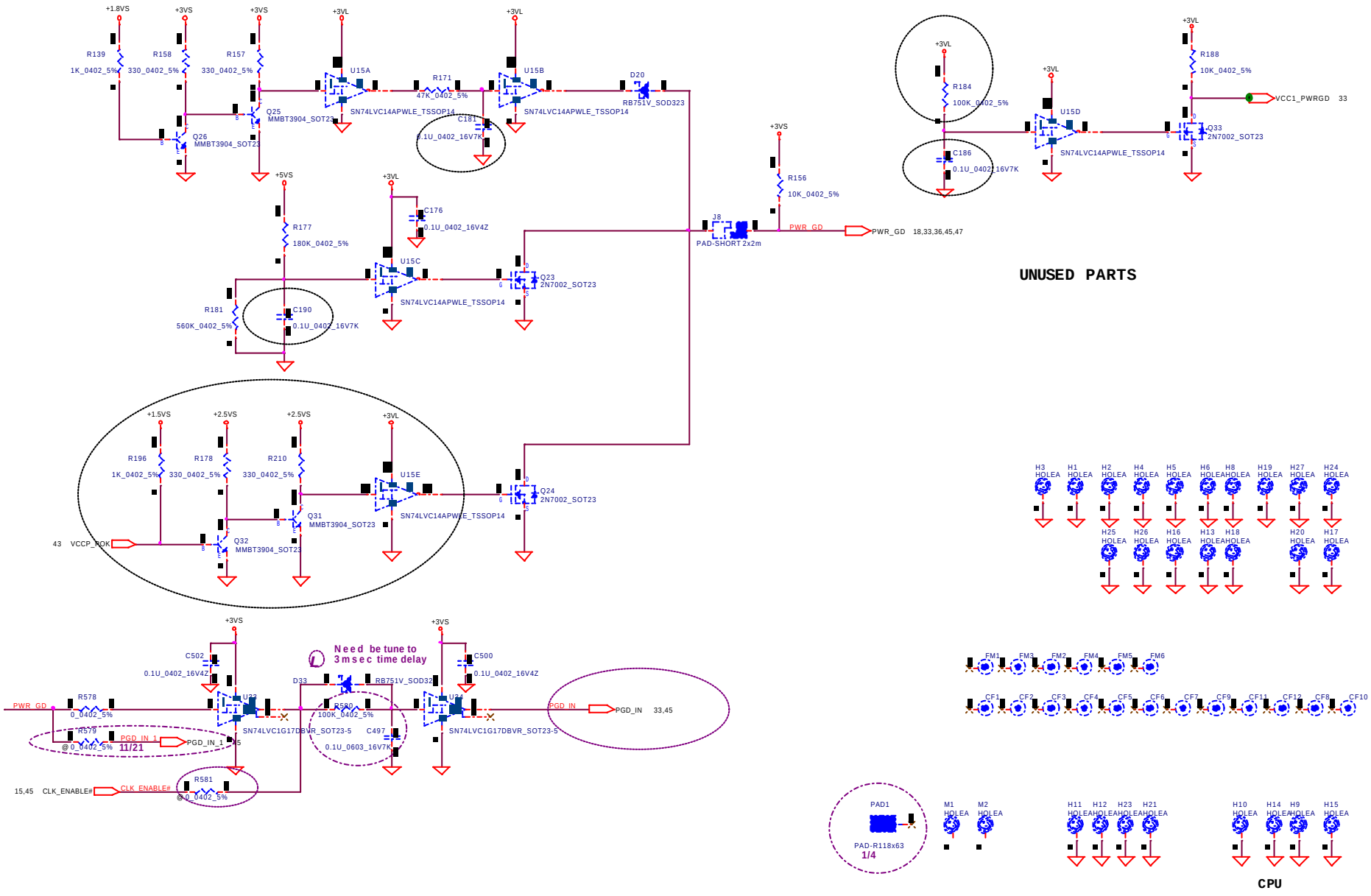

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title: POK CKT
				Size / Document Number: LA-2821P / Rev: 1.0
				Date: Saturday, January 14, 2006 / Sheet 37 of 52

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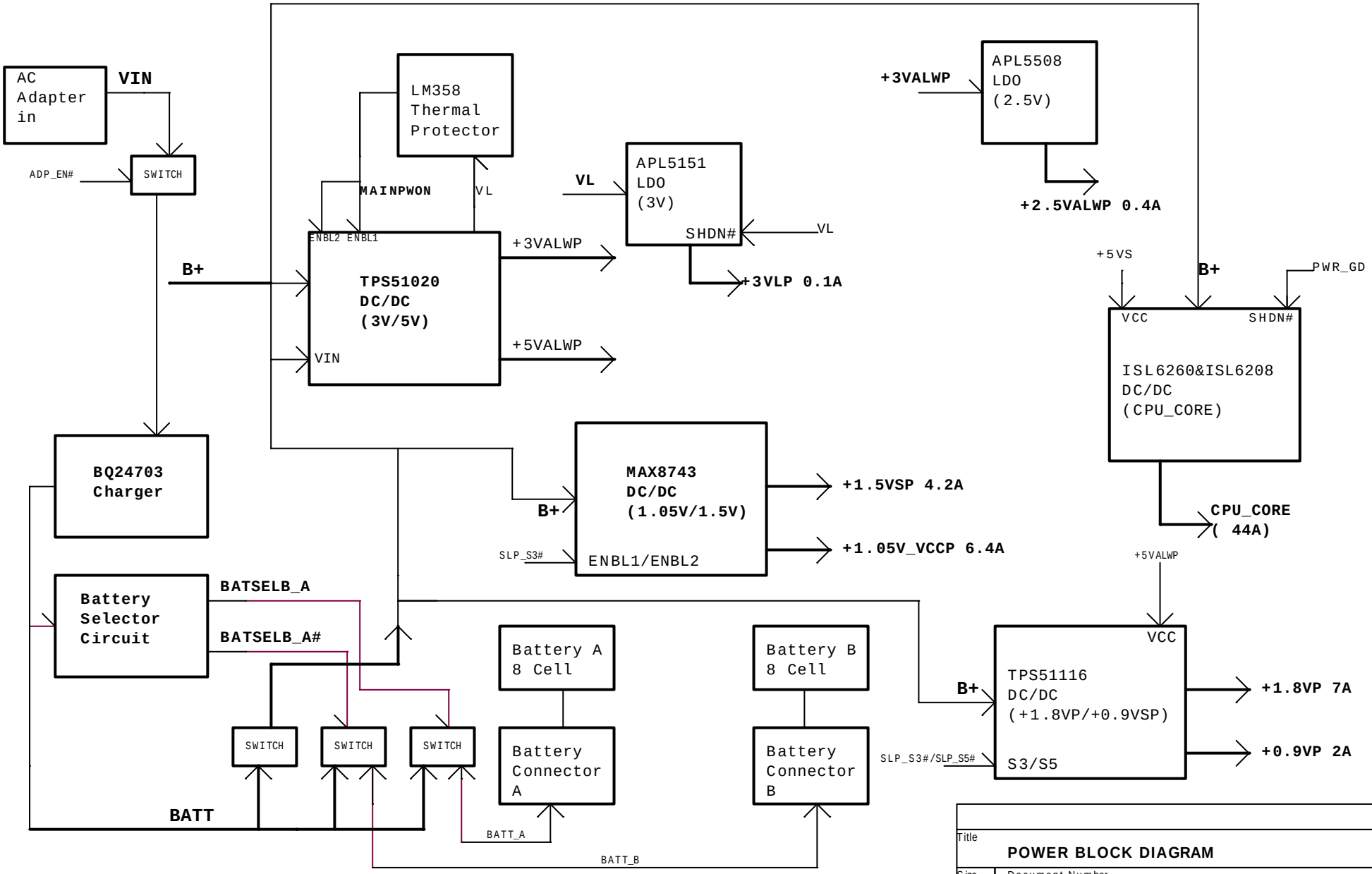

Title
POWER BLOCK DIAGRAM

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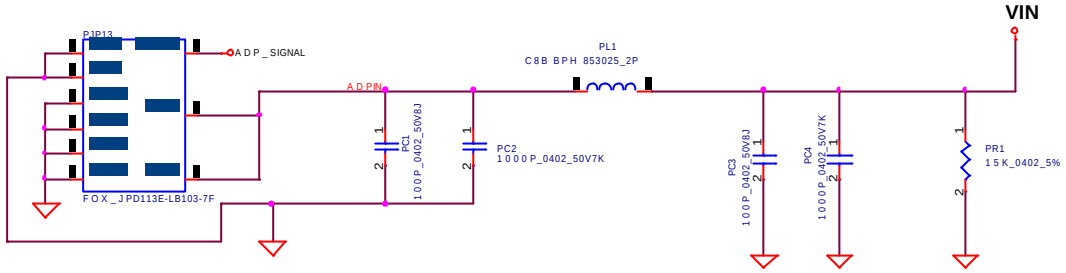

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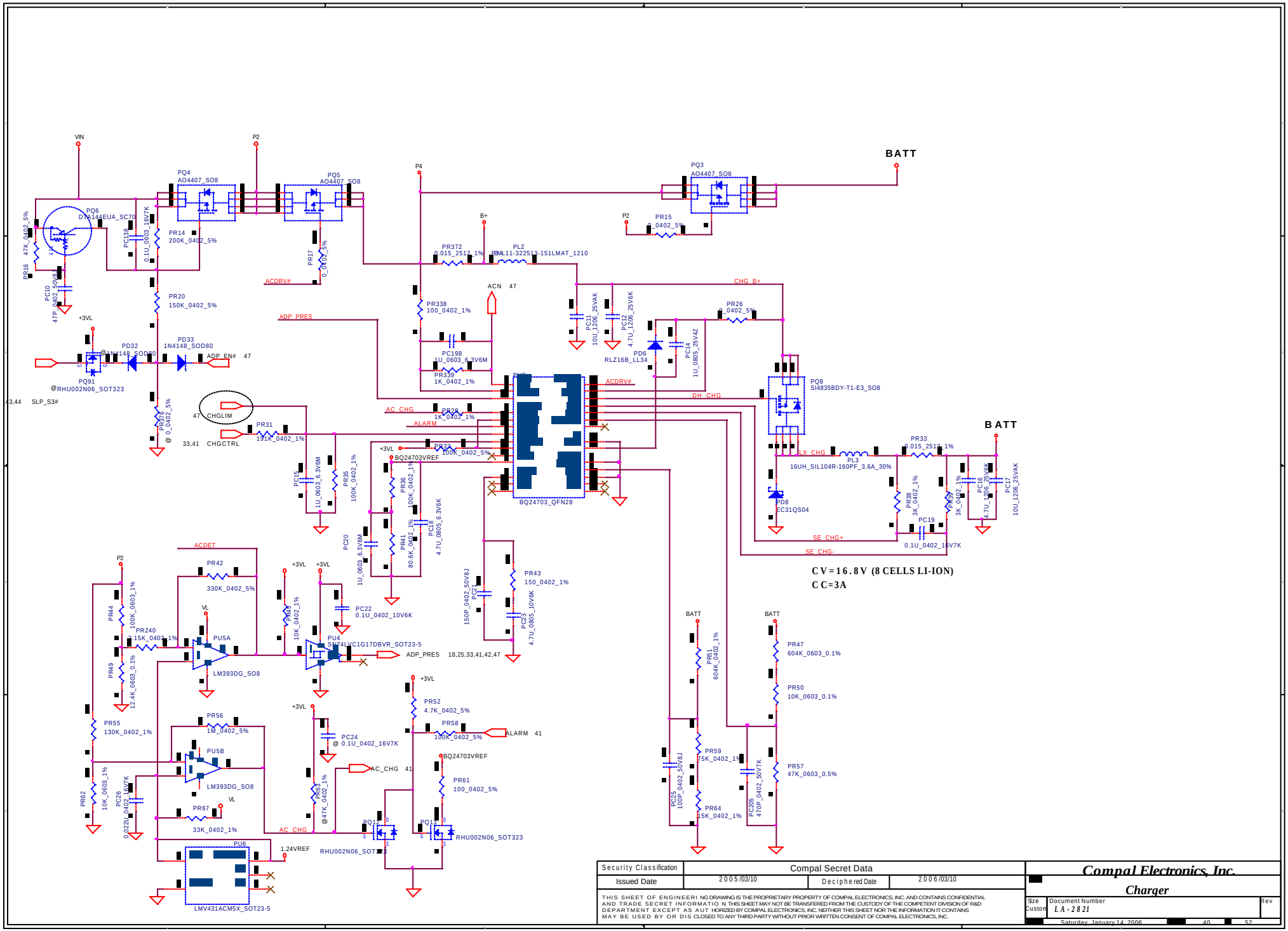
Compal Electronics, Inc.

Title: **DCIN**

Size: Custom | Document Number: **LA-2821** | Rev

Date: Saturday, January 14, 2006 | Sheet 39 of 52



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Compal Electronics, Inc.

Charger

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Custom	LA-2821	

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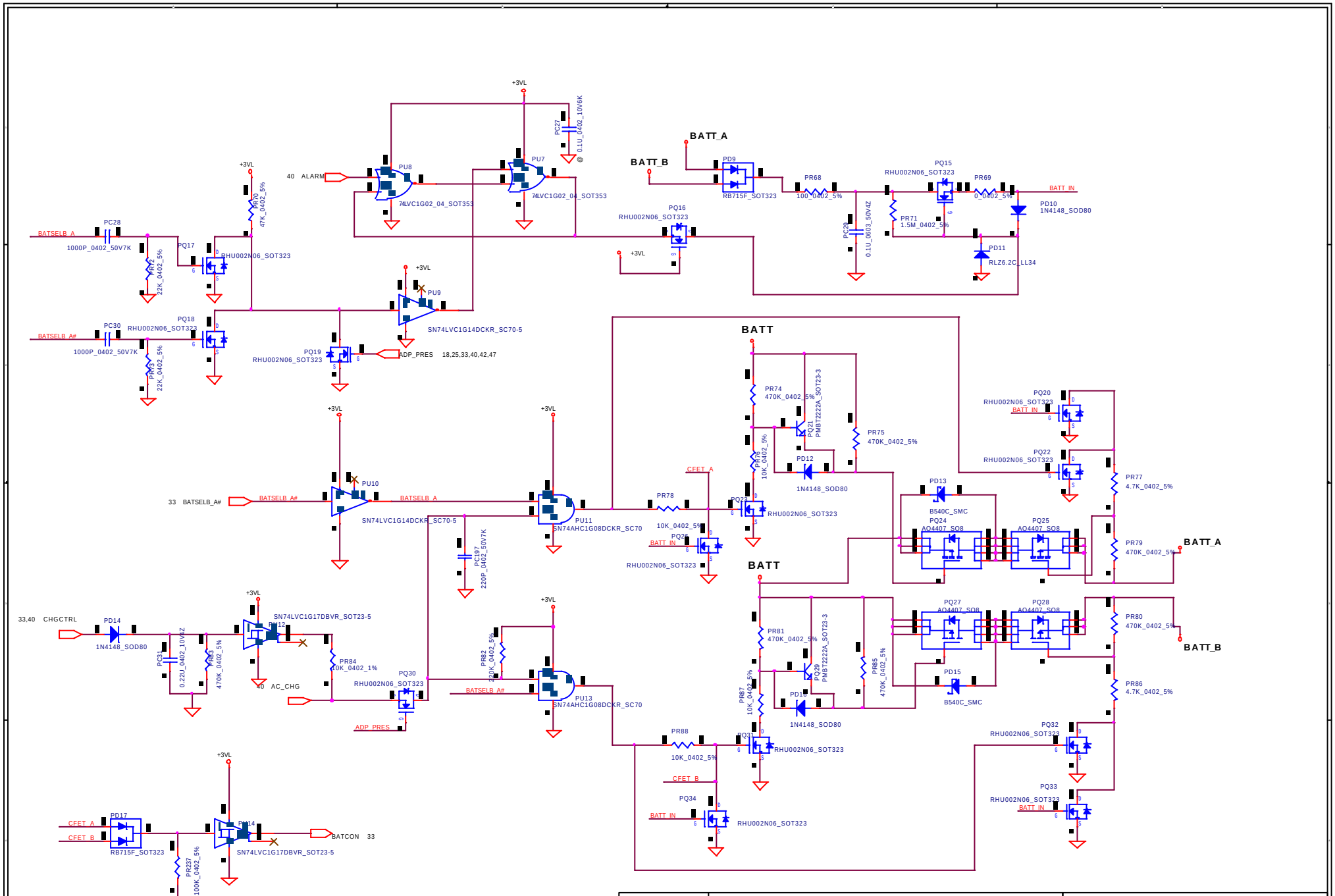

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Compal Electronics, Inc.

Battery selector

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Custom	LA-2821	

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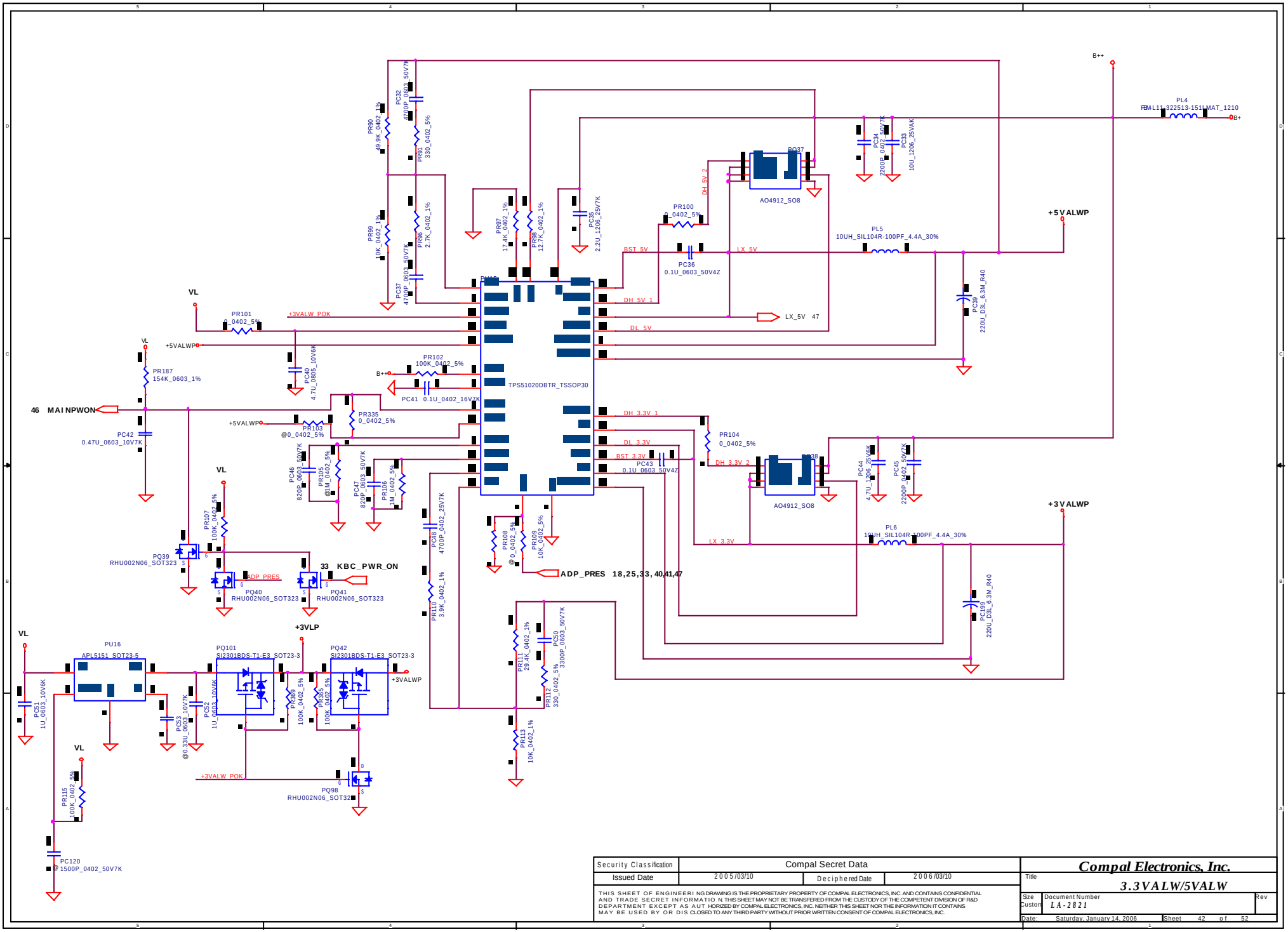

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Compal Electronics, Inc.

Title: 3.3VALW/5VALW

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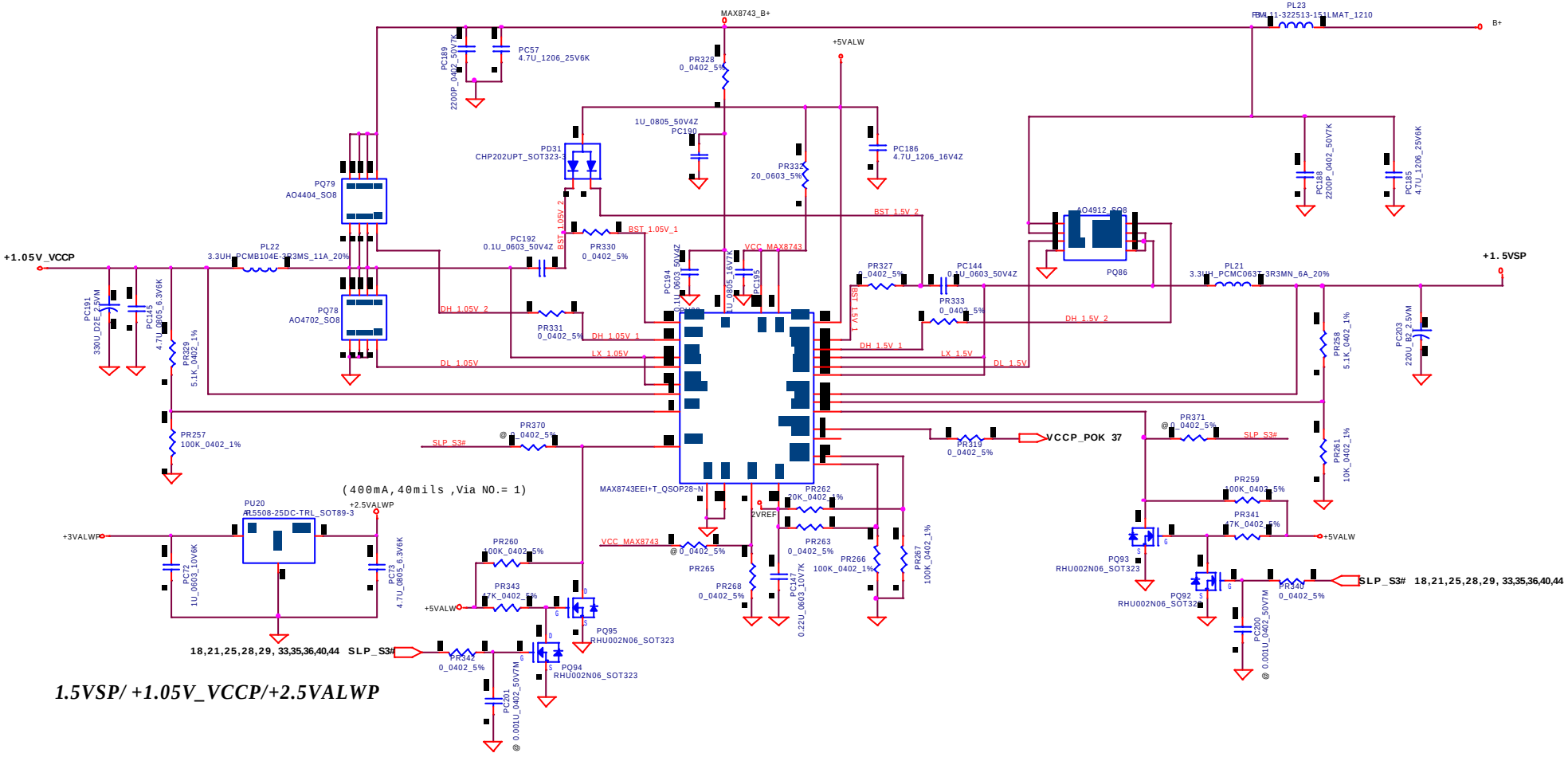

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

2.5VALW/1.5VS/1.05VCCP

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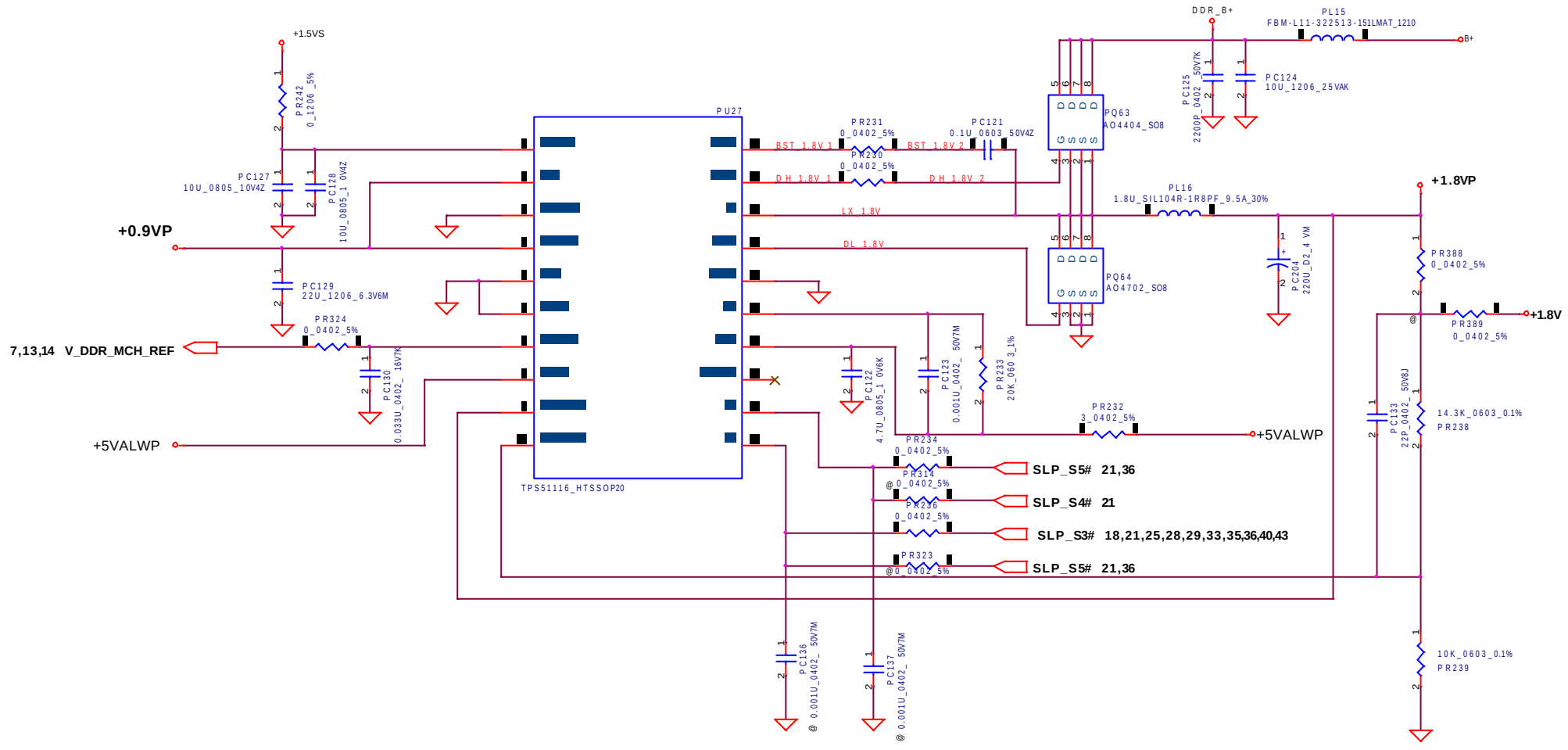

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Issued Date	2005/03/10	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title: **1.8V/0.9VS**

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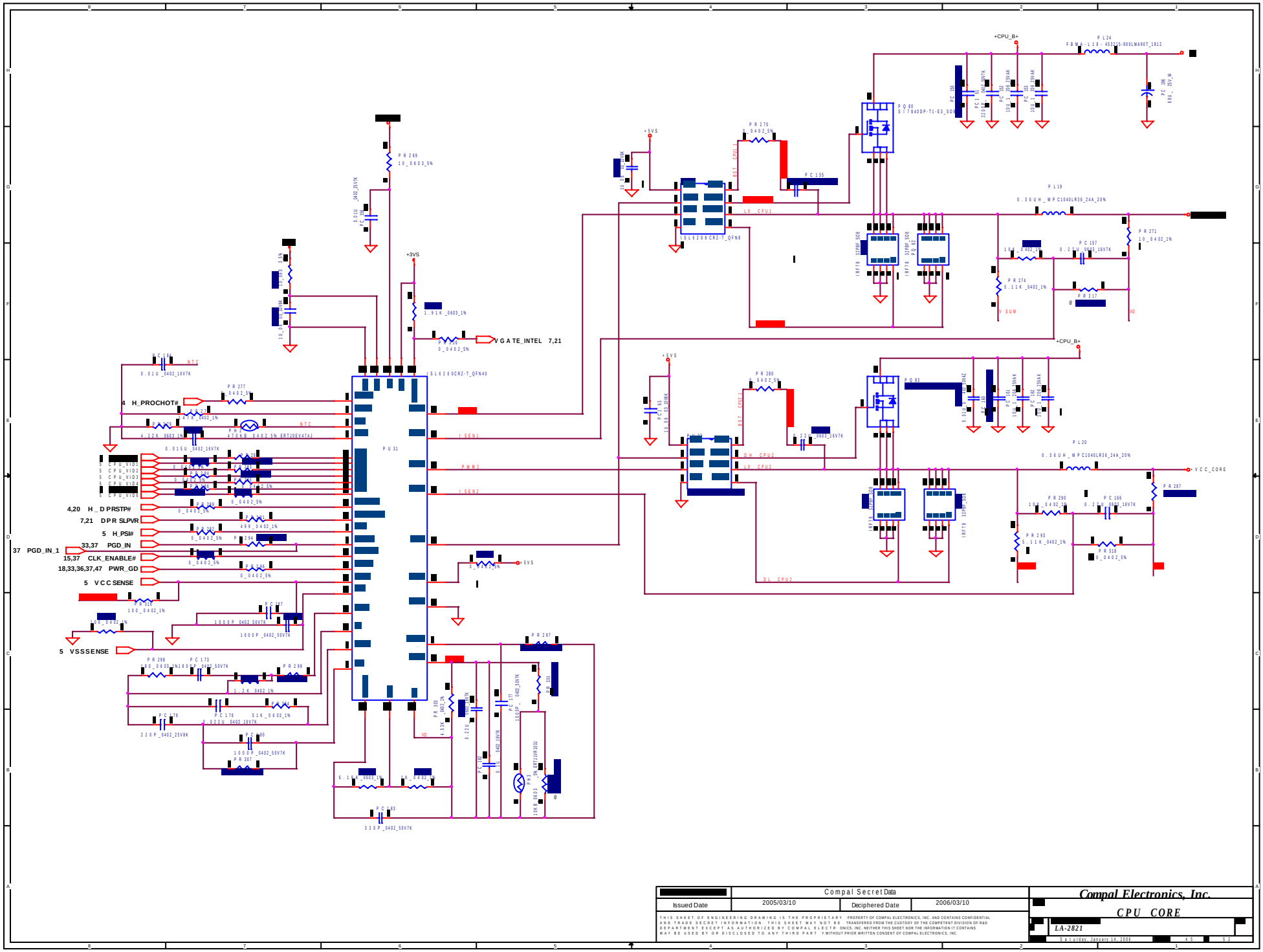

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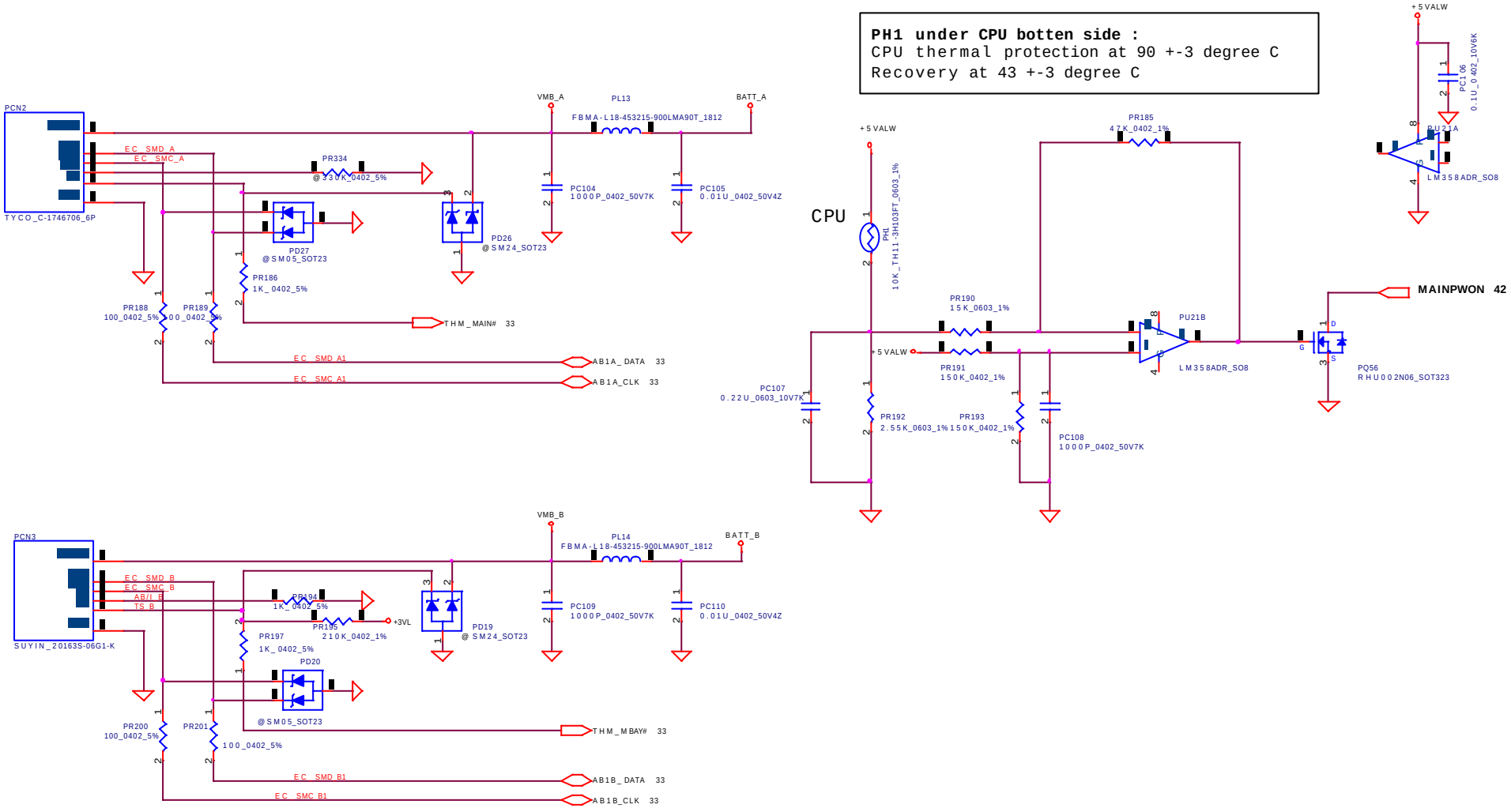
Compal Electronics, Inc.

CPU CORE

LA-2821

Saturday, January 14, 2006 | 4.5 | 5.2



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Compal Electronics, Inc.

Title: **BATTERY CONN**

Size: Custom | Document Number: *LA-2821* | Rev

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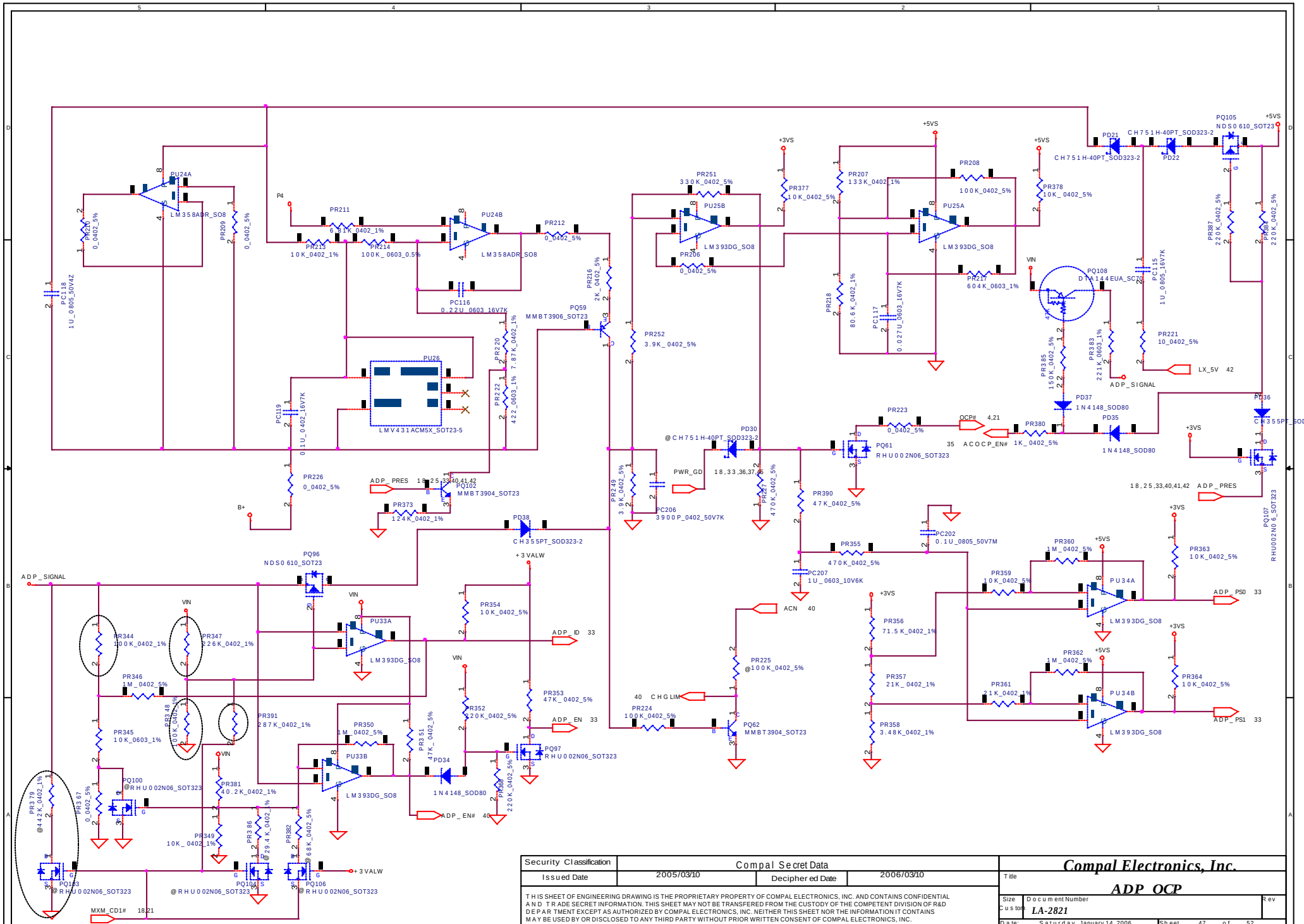

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Compal Electronics, Inc.

Title: **ADP_OCP**

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EAL80 from Pre DB-1 Step to DB-1 Step LA-2821 REV:0.0 -> 0.1 Modify <94.03.26.~94.04.08. >

1. Change +0.9V discharge circuit control signal from SLP_S3 to SLP_S5. <Page 36> 94.03.26.
-Change Q27.2(2N7002) connection from SLP_S3 to SLP_S5. (Modify CKT&Layout)

2. Just reserve a test pad for TPM_GPIO directly. <Page 32> 94.03.28.
-Del R1248 and connect TP62 to JP33.8 directly. (Modify CKT& Layout)

3. Change TPM1.2 +3VL Power Rail to +3VALW by Customer request. <Page 32> 94.03.28.
-Change +3VL that connects to R1242.1 to +3VALW. (Modify CKT&Layout)

4. Correct U25.39/38's net name from CLK_PCIE_NC/NC# to PCIE_NC/NC#. <Page 15> 94.03.28.
-Change U25.39/38 connection from CLK_PCIE_NC/CLK_PCIE_NC# to PCIE_NC/PCIE_NC#. (Modify CKT&Layout)

5. Change the RC parts for POK Time delay request. <Page 37> 94.03.29.
-Change R117 from 100K_0402_5% to 150K_0402_1%. (Modify CKT&BOM)
-Change C87 from 0.1U_0402 to 0.47U_0603_X7R. (Modify CKT,BOM&Layout)

6. Update the PCI7611MLS/PCI7612 related schematic by Vendor recommend. <Page 23,24> 94.03.29.
-Change R93,R97 from 7612@0_0402 to 0_0402; R103 from 7611@0_0402 to @0_0402. (Modify CKT&BOM)
-Add R1308(0_0402) between U42.K3 and U42.K5; change R106 from 0_0402 to @0_0402. (Modify CKT,BOM &Layout)
-Change R1299 from 43K_0402 to @43K_0402. (Modify CKT&BOM)

7. Reserve a 68UF Cap. by LAN Chip Vendor request. <Page 25> 94.03.29.
-Reserve C976(@68U_B2_4VM) close to U6.M14. (Modify CKT,BOM&Layout)

8. Reserve two resistors(@0_0402) to isolate VGATE and VGATE_INTEL. <Page 37> 94.03.29.
-Reserve R1306(@0_0402) between PU31.40 and U45.2. (Modify CKT,BOM&Layout)
-Reserve R1307(@0_0402) between U48.4 and PR326.2. (Modify CKT,BOM&Layout)

9. Change Calistoga LVDS function power source to GND for disabling by customer recommend. <Page 10> 94.03.29.
-Change U15.B30/C30/A30 connection from +2.5VS to GND. (Modify CKT&Layout)
-Change U15.A28/B28/C28 connection from +1.5VS to GND. (Modify CKT&Layout)

10. Remove DPRSLPVR Pull-down resistor by customer recommend. <Page 21> 94.03.29.
-Change R1015 from 100K_0402_5% to @100K_0402_5%. (Modify CKT&BOM)

11. Stuff SPI related function Pull-High resistors by customer/Intel recommend. <Page 21,32> 94.03.29.
-Change R1284~R1286 from @10K_0402_5% to 10K_0402_5%. (Modify CKT&BOM)

12. Reserve 0 ohm resistor for PM_EXTTS#1 and DPRSLPVR connection by Customer/Intel recommend. <Page 7,21> 94.03.29.
-Reserve R1309(@0_0402_5%) between PM_EXTTS#1 and DPRSLPVR connection. (Modify CKT&Layout)

13. Add +1.8V discharge circuit. <Page 36> 94.03.30.
-Add R1310(470_0402_5%) and Q90(2N7002_SOT23) for +1.8V discharge schematic related. (Modify CKT,BOM&Layout)

14. Change ICH7 HD function power source to +3VS for wake on ring function from Azalia modem disabling by customer recommend. <Page 22> 94.03.30.
-Change U26.R7 connection from +3VALW to +3VS. (Modify CKT&Layout)

15. Change TPM1.2 +3VL Power Rail to +3VALW by Customer request. <Page 32> 94.03.30.
-Change +3VL that connects to C193.1 to +3VALW. (Modify CKT&Layout)

16. Update ICH7M HD Audio, Codec Chip and MDC related Schematic. <Page 20,34,36> 94.03.30.
-Add R1313,R1314,R1315(33_0402) for ICH7/MDC/Codec related update. (Modify CKT,BOM&Layout)
-Create net name AC97_RST#_MDC, AC97_RST#_CODEC, AC97_SYNC_MDC, AC97_SYNC_CODEC, AC97_SDOUT_MDC, AC97_SDOUT_CODEC, AC97_BITCLK_MDC, AC97_BITCLK_CODEC, AC97_SDIN0_CODEC, AC97_SDIN1_MDC for ICH7/MDC/Codec related update. (Modify CKT&Layout)

17. Reserve 0ohm option resistors for +0.9V discharge circuit control signal SLP_S3 and SLP_S5 selecting. <Page 36> 94.03.30.
-Reserve R1311(@0_0402) to connect SLP_S5 to Q27.2. (Modify CKT&Layout)
-Add R1312(0_0402) to connect SLP_S3 to Q27.2. (Modify CKT,BOM&Layout)

18. Populate the 68UF Cap. and reserve 10UF Cap. by LAN Chip Vendor/Customer request. <Page 25> 94.03.30.
-Change C976 from @68U_B2_4VM to 68U_B2_4VM, remove C243(@10U_1206_6.3V). (Modify CKT&BOM)

19. Swapping DDR2 SO-DIMM Data Group pin definition for Layout routing smoothly. <Page 13,14> 94.03.31.
-Swapping JP34 and JP10 Data Group pin definition. (Modify CKT&Layout)

---------- 3th Netin

20. Correct Calistoga chip power pin connection base on CRB Rev:1.301 recommend. <Page 11> 94.04.01.
-Disconnect U15.AV1 and U15.AJ1 to +1.8V and modify the related schematic. (Modify CKT&Layout)
-Change U15.AT41/AM41 net name from MCH_AT41/MCH_AM41 to VCCSM_LF4/VCCSM_LF5. (Modify CKT&Layout)

21. Change C899~C930 from 10U_1206_X5R to 10U_00805_X5R to meet Intel Napa ESL request. <Page 6> 94.04.01.
-Change C899~C930 from 10U_1206_X5R to 10U_00805_X5R. (Modify CKT,BOM&Layout)

22. Change C940~C945 from 0.1U_0402_Y5V to 0.1U_0402_X5R to meet Intel request, avoid thermal risk. <Page 6> 94.04.01.
-Change C940~C945 from 0.1U_0402_Y5V to 0.1U_0402_X5R. (Modify CKT&BOM)

23. Update ICS954306 PCB Footprint for Layout routing. <Page 15> 94.04.01.
-Change U25 PCB Footprint from ICS954306_TSSOP64 to ICS954306BGLFT_TSSOP64. (Modify CKT,BOM&Layout)

24. Remove the R1153 2.2Kohm pull-high resistor for leverage AF1.0 CFG9 setup. <Page 11> 94.04.01.
-Remove R1153(@2.2K_0402). (Modify CKT&BOM)

25. Add net name for USB signals layout rule create. <Page 30> 94.04.04.
-Add net names USB20_N1_R, USB20_P1_R, USB20_N4_R, USB20_P4_R, USB20_HUB_N1_R, USB20_HUB_P1_R on JP16.6/7/2/3 JP22.4/3. (Modify CKT&Layout)

---------- 4th Netin

26. Remove the R555,R612 8.2Kohm pull-high resistors because the signals be double pulled up. <Page 18> 94.04.04.
-Remove R555,R612(@8.2K_0402). (Modify CKT&BOM)

27. Reserve Audio mute control signals on KBC to leverage AF1.0 designing. <Page 33> 94.04.04.
-Reserve R140,R141(@0_0402) onU47.57/56 for EAPD/A_SD. (Modify CKT&Layout)

28. Correct net name for USB signals layout rule create. <Page 29,35> 94.04.04.
-Correct net names to USB20_N2_R, USB20_P2_R, USB20_N3_R, USB20_P3_R, USB20_N6_R, USB20_P6_R, USB20_N7_R, USB20_P7_R, on JP27.1/2/4/5 JP30.2/4/6/8. (Modify CKT&Layout)

29. Add (NC@0_0402) to connect CP_USB# and NC_CPPE# for New Card function usage. <Page 24> 94.04.04.
-Add R1316(NC@0_0402) to connect CP_USB# and NC_CPPE#. (Modify CKT,BOM&Layout)
-Change R1272,R1273 from @10K_0402 to @100K_0402. (Modify CKT&BOM)

---------- 5th Netin

30. Del JP39.157's ADP_PRES connection to leverage AF1.0 and standard MXM pin definition. <Page 18> 94.04.04.
-Del JP39.157's ADP_PRES connection. (Modify CKT&Layout)

31. Reserve the circuit to control the mute to block the speaker pop on power up by customer recommend. <Page 29> 94.04.04.
-Reserve D59(@RB751V), R613(@1M_0402), R431(@10K_0402), C93(@2.2U_0805), R439(@10K_0402), R438(@10_0402) and the related circuit on U39.19. (Modify CKT,BOM&Layout)

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EAL80 from DB-1 Step to DB-2 Step LA-2821 REV:0.1 -> 0.2 Modify <94.05.10.~94.05.27. >

1. Change HDD I/F from PATA to SATA. <Page 20> 94.05.10.

-Change U26.AF18 from NC to IDE_LED#. (Modify CKT&Layout)
-Change U26.AF3 from GND to SATA_RXN0_C. (Modify CKT&Layout)
-Change U26.AE3 from GND to SATA_RXP0_C. (Modify CKT&Layout)
-Change U26.AG2 from NC to SATA_TXN0_C. (Modify CKT&Layout)
-Change U26.AH2 from NC to SATA_TXP0_C. (Modify CKT&Layout)
-Add R1256(24.9_0402_1%) between U26.AH10/AG10 and GND. (Modify CKT,BOM&Layout)
-Del R1326,R1327(NOSATA@0_0402). (Modify CKT,BOM&Layout)
-Add JP45, C955~C958(3900P_0402) and related schematic for SATA connector. (Modify CKT,BOM&Layout)

2. Remove R1294(1K_0402) Pull-High to +3VS to avoid double Pull-High risk. <Page 20> 94.05.10.

-Remove R1294(@1K_0402). (Modify CKT&BOM)

3. Add the accelerometer device LIS3LV02DQ and modify the related schematic. <Page 02,21,27,33> 94.05.11.

-Add U64(LIS3LV02DQ_QFN28),R1355(0_0805_5%),R1356(0_0603_5%),R1357~R1361(0_0402_5%), R1362(10K_0402_5%),C994(0.01U_0402_16V7K),C995(0.1U_0402_16V4Z) and C996(4.7U_0805_10V4Z) at the center of the system. (Modify CKT,BOM&Layout)
-Add R1364(0_0402_5%) between "ACCEL_INT#" and U26.E20(SB_GPIO9); Reserve R1363(@0_0402_5%) between "ADP_PWRID" and U26.E20(SB_GPIO9). (Modify CKT,BOM&Layout)
-Reserve R1354(@0_0402_5%) between "ACCEL_INT#" and U47.34(KBC_GPIO23). (Modify CKT,BOM&Layout)

4. Change USB port assignments as customer request. <Page 02,21,24,30,32> 94.05.11.

-Change R1317(NC@0_0402_5%) connection Net from "USB20_P0_HUB" to "USB20_P1_HUB" and from "USB20_P0" to "USB20_P1". (Modify CKT&Layout)
-Change R1318(NC@0_0402_5%) connection Net from "USB20_N0_HUB" to "USB20_N1_HUB" and from "USB20_N0" to "USB20_N1". (Modify CKT&Layout)
-Change R562(0_0402_5%) connection Net from "USB20_HUB_P1_R" to "USB20_P0_R" and from "USB20_HUB_P1" to "USB20_P0". (Modify CKT&Layout)
-Change R586(0_0402_5%) connection Net from "USB20_HUB_N1_R" to "USB20_N0_R" and from "USB20_HUB_N1" to "USB20_N0". (Modify CKT&Layout)
-Change R983(NONC@0_0402_5%) connection Net from "USB20_P0" to "USB20_P1". (Modify CKT&Layout)
-Change R982(NONC@0_0402_5%) connection Net from "USB20_N0" to "USB20_N1". (Modify CKT&Layout)
-Change R1335(0_0402_5%) connection Net from "USB20_HUB_P2_R" to "USB20_HUB_P1_R" and from "USB20_HUB_P2" to "USB20_HUB_P1". (Modify CKT&Layout)
-Change R1334(0_0402_5%) connection Net from "USB20_HUB_N2_R" to "USB20_HUB_N1_R" and from "USB20_HUB_N2" to "USB20_HUB_N1". (Modify CKT&Layout)
-Change R1276(NC@0_0402_5%) connection Net from "USB20_P5_R" to "USB20_HUB_P2_R" and from "USB20_P5" to "USB20_HUB_P2". (Modify CKT&Layout)
-Change R1274(NC@0_0402_5%) connection Net from "USB20_N5_R" to "USB20_HUB_N2_R" and from "USB20_N5" to "USB20_HUB_N2". (Modify CKT&Layout)
-Change R607(0_0402_5%),D51.3 connection Net from "USB20_P1_R" to "USB20_P5_R" and from "USB20_P1" to "USB20_P5". (Modify CKT&Layout)
-Change R606(0_0402_5%),D51.2 connection Net from "USB20_N1_R" to "USB20_N5_R" and from "USB20_N1" to "USB20_N5". (Modify CKT&Layout)
-Change U53(NC@USB2502) pin15 connection from Net "USB_OC#0" to "USB_OC#1". (Modify CKT&Layout)
-Change U41(TPS2041B) pin5 connection from Net "USB_OC#1" to "USB_OC#5". (Modify CKT&Layout)

5. Change PCIE port assignments as customer request. <Page 02,21,24,25,27,35> 94.05.12.

-Change U26.K26/K25/J28/J27 to NC. (Modify CKT&Layout)
-Change C712 connection from PCIE_C_TXN3 to PCIE_C_TXN4 ; from PCIE_TXN3 to PCIE_TXN4. (Modify CKT&Layout)
-Change C713 connection from PCIE_C_TXP3 to PCIE_C_TXP4 ; from PCIE_TXP3 to PCIE_TXP4. (Modify CKT&Layout)
-Change C952 connection from PCIE_C_TXN4 to PCIE_C_TXN5 ; from PCIE_TXN4 to PCIE_TXN5. (Modify CKT&Layout)
-Change C953 connection from PCIE_C_TXP4 to PCIE_C_TXP5 ; from PCIE_TXP4 to PCIE_TXP5. (Modify CKT&Layout)
-Change C959 connection from PCIE_C_RXN3 to PCIE_C_RXN4 ; from PCIE_RXN3 to PCIE_RXN4. (Modify CKT&Layout)
-Change C960 connection from PCIE_C_RXP3 to PCIE_C_RXP4 ; from PCIE_RXP3 to PCIE_RXP4. (Modify CKT&Layout)
-Change JP9.A24 connection from PCIE_TXN3 to PCIE_TXN4. (Modify CKT&Layout)
-Change JP9.A25 connection from PCIE_TXP3 to PCIE_TXP4. (Modify CKT&Layout)
-Change R1347 connection from PCIE_C_RXN4 to PCIE_C_RXN5 ; from PCIE_RXN4 to PCIE_RXN5. (Modify CKT&Layout)
-Change R1346 connection from PCIE_C_RXP4 to PCIE_C_RXP5 ; from PCIE_RXP4 to PCIE_RXP5. (Modify CKT&Layout)
-Change JP30.151 connection from PCIE_TXN4 to PCIE_TXN5. (Modify CKT&Layout)
-Change JP30.149 connection from PCIE_TXP4 to PCIE_TXP5. (Modify CKT&Layout)

6. Change SRC clock assignments as customer request. <Page 15> 94.05.13.

-Change U25.20 connection from "MCH_3GPLL" to "PCIE_LOM". (Modify CKT&Layout)
-Change U25.21 connection from "MCH_3GPLL#" to "PCIE_LOM#". (Modify CKT&Layout)
-Change U25.22 connection from "PCIE_LOM" to "PCIE_NC". (Modify CKT&Layout)
-Change U25.23 connection from "PCIE_LOM#" to "PCIE_NC#". (Modify CKT&Layout)
-Change U25.26 connection from "PCIE_MCARD" to "PCIE_DOCK". (Modify CKT&Layout)
-Change U25.27 connection from "PCIE_MCARD#" to "PCIE_DOCK#". (Modify CKT&Layout)
-Change U25.37 connection from "PCIE_DOCK" to "MCH_3GPLL". (Modify CKT&Layout)
-Change U25.36 connection from "PCIE_DOCK#" to "MCH_3GPLL#". (Modify CKT&Layout)
-Change U25.39 connection from "PCIE_NC" to "PCIE_MCARD". (Modify CKT&Layout)
-Change U25.38 connection from "PCIE_NC#" to "PCIE_MCARD#". (Modify CKT&Layout)

7. Change CLKREQ assignments as customer request. <Page 07,15,24,27> 94.05.13.

-Change R1344.2 connection from "CLKREQB#" to "CLKREQC#". (Modify CKT&Layout)
-Change R1279.1/R1280.1/C961.1 connection from "CLKREQD#" to "CLKREQA#". (Modify CKT&Layout)
-Change R1336 connection from "CLKREQB#" to "CLKREQD#"; from "CLKREQB#_MC" to "CLKREQD#_MC". (Modify CKT&Layout)
-Add R1120(NOXDP@10K_0402) from net "CLKREQC#" to +3VS pull-high. (Modify CKT,BOM&Layout)
-Change R1142 from NOXDP@10K_0402 to NOXDP@0_0402. (Modify CKT&BOM)
-Add R1147(NOXDP@10K_0402) from net "CLKREQD#" to +3VS pull-high. (Modify CKT,BOM&Layout)
-Change R1254 from NOXDP@10K_0402 to NOXDP@0_0402. (Modify CKT&BOM)
-Change R1106(10K_0402) connection from +3VS pull-high to between CLKREQB# and CPPE#. (Modify CKT&Layout)

8. Reserve test Mini-Card that supports USB interface as customer request. <Page 27,32> 94.05.13.

-Add R1365(@0_0402) between JP38.2 and JP44.36. (Modify CKT&Layout)
-Add R1366(@0_0402) between JP38.3 andto JP44.38. (Modify CKT&Layout)

9. Del R1344 & R1336 and short directly because of double reserved. <Page 07,27> 94.05.16.

-Del R1344(@0_0402_5%) and short directly. (Modify CKT&Layout)
-Del R1336(0_0402_5%) and short directly. (Modify CKT,BOM&Layout)

10. Update LAN Controller schematic related caused by chipset changed from BCM5751M to BCM5753M. <Page 25,26> 94.05.16.

-Update the related schematic. (Modify CKT&Layout)
-Change R275,R289 from 47K_0402 to 1K_0402. (Modify CKT,BOM&Layout)
-Change R276 from 4.7K_0402 to 1K_0402. (Modify CKT,BOM&Layout)
-Add R1370,R1371(0_0402) and reserve R1372,R1373(@2.2K_0402),Q92,Q93(@2N7002) for SMBus connection. (Modify CKT,BOM&Layout)
-Add R1367(1K_0402) from U6.H12 to +3VS. (Modify CKT,BOM&Layout)

11. Remove U37,D32,R504, and C577. Remove CLKREQA# connection from NIC to CK clock by customer recommend. <Page 25> 94.05.16.

-Remove U37,D32,R504, and C577. (Modify CKT,BOM&Layout)

12. Update Accelerometer related schematic by Vendor STMicro recommend. <Page 27> 94.05.16.

-Remove C994(@0.01U_0402), Change C996 from 4.7U_0805 to 10U_0805. (Modify CKT,BOM&Layout)

13. Modify ICH7 Power_OK connection to be able to be enable same as NB. <Page 21> 94.05.16.

-Add R1368(0_0402) and reserve R1369(@0_0402) for U26.AD22 connection. (Modify CKT,BOM&Layout)

14. Swap RP11,RP13 pin connection for DDR2 shift trace routing issue improving. <Page 14> 94.05.16.

-Change RP11.2 connection from DDR_B_MA11 to DDR_CKE3_DIMMB. (Modify CKT&Layout)
-Change RP11.1 connection from DDR_CKE3_DIMMB to DDR_B_MA7. (Modify CKT&Layout)
-Change RP13.2 connection from DDR_B_MA6 to DDR_B_MA11. (Modify CKT&Layout)
-Change RP13.1 connection from DDR_B_MA7 to DDR_B_MA6. (Modify CKT&Layout)

---------- 1st Netin

15. Update the SATA supported related. <Page 20> 94.05.17.

-Delete JP23,R458,R1324,R1325,R300. (Modify CKT,BOM&Layout)
-Add C997(10U_0805),C998~C1000(0.1U_0402) close to JP45 +3VS pins. (Modify CKT,BOM&Layout)

16. Dual design SPI ROM for SOP8-150mil/200mil package. <Page 32> 94.05.17.

-Add U65(SPI@SST25LF080A-200mil). (Modify CKT,BOM&Layout)

17. TPM1.2 on board designing reserve related. <Page 32> 94.05.17.

-Add U66(TPM1.2@SLB9635TT),C1001~C1004(0.1U_0402),C1005,C1006(18P_0402),Y8(32.768KHz), R1375~R1381 and related schematic update. (Modify CKT,BOM&Layout)

---------- 2nd Netin

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EAL80 from DB-1 Step to DB-2 Step LA-2821 REV:0.1 -> 0.2 Modify <94.05.10.~94.05.27. >

18. Update TPM1.2 on board designing schematic. <Page 32,36> 94.05.18.
- Change pin5 (VSB) to +3VALW and move C1004 to connect to pin5 . (Modify CKT&Layout)
- Delete SMBus connection with R1380,R1381 on U66.2 & U66.6; Connect U66.6 to JP33.8, U66.2 to T87 . (Modify CKT,BOM&Layout)
- Delete +3V power from JP33.4 . (Modify CKT& Layout)
- Delete +3V power reserved schematic and parts include Q91,C977,C978 . (Modify CKT,BOM &Layout)

19. Add DC/DC schematic about +2.5VALW to +2.5VS for power sequence fail issue fixed. <Page 36> 94.05.18.
- Add U67(SI4800DY_SO8),C1007,C1008,C1009 . (Modify CKT,BOM&Layout)

20. Delete MDC 1.0 Connector reserved related to save layout space . <Page 34> 94.05.18.
- Del JP25(MDC1.0 Conn),C13(0.1U_0402) . (Modify CKT,BOM&Layout)

21. Change the power source designing from +3VALW to +3VS for DB-2 LS-2712 issue fixed . <Page 34> 94.05.18.
- Change JP18.1 and JP18.3 connection from +3VALW to +3VS . (Modify CKT& Layout)

---------- 3rd Netin

22. Change the ICH7 RTC Cap. Value for SVTP measure fail issue fixed . <Page 20> 94.05.19.
- Change C516,C528 from 18P_0402 to 10P_0402 . (Modify CKT&BOM)

23. Update LAN chip schematic related by customer recommend . <Page 25> 94.05.19.
- Change R275,R289 from 1K_0402 to @1K_0402 . (Modify CKT&BOM)
- Del D32,R504,C577,U37 . (Modify CKT,BOM&Layout)
- Add R1380(0_0402) and reserve R1381(@0_0402) . (Modify CKT,BOM&Layout)
- Del C40,C45,C53,C62,C64 for +3VS power rail cancel . (Modify CKT,BOM &Layout)

24. Update KBC related designing by customer recommend . <Page 33> 94.05.20.
- Add ADP_EN to S_CLK(GPIO22) by R1385(0_0402) . (Modify CKT,BOM&Layout)
- Add ADP_ID to EC_GPIO19 by R1382(0_0402) . (Modify CKT,BOM&Layout)
- Add ADP_PS1 to EC_GPIO12 by R1383(0_0402) . (Modify CKT,BOM&Layout)
- Add ADP_PS0 to EC_GPIO10 by R1384(0_0402) . (Modify CKT,BOM&Layout)
- Remove R87(@0_0402) . (Modify CKT&BOM)

25. Update ICH7 related designing by customer recommend . <Page 21,35> 94.05.20.
- Change R1363 from 0_0402 to ACCEL@0_0402 . (Modify CKT&BOM)
- Change R1363.2 connection from ADP_PWRID to ADP_ID . (Modify CKT&Layout)
- Reserve R1386(@0_0402) from PREP2# to U26.AD20(ICH7_GPIO38) . (Modify CKT&Layout)
- Reserve R1387(@10K_0402) from PREP2# to +3VS . (Modify CKT&Layout)

26. Update LAN chip schematic related by customer recommend . <Page 25> 94.05.20.
- Change R73.1 and R36.1 connection from +3VS to V_3P3_LAN . (Modify CKT& Layout)

27. Update CardReader chip schematic related by customer recommend . <Page 23> 94.05.20.
- Del U46 and related net . (Modify CKT,BOM&Layout)
- Del R591,R593 . (Modify CKT,BOM&Layout)
- Change R594 connection to between +VCC_SD and SDWP#_SMCE# . (Modify CKT&Layout)
- Change R602 connection to between +VCC_SD and SM_RB# . (Modify CKT&Layout)
- Change JP41.36 connection to MSBS_SDCMD_SMWE# . (Modify CKT&Layout)
- Change JP41.27 connection to SDCLK_SMRE# . (Modify CKT&Layout)
- Change JP41.28 connection to SDWP#_SMCE# . (Modify CKT&Layout)
- Change JP41.26 connection to SM_RB# . (Modify CKT&Layout)
- Add R1388(0_0402) between MC_PWRON# and MC_PWRON . (Modify CKT,BOM&Layout)
- Remove Q77,D45,D46,R595,D48 . (Modify CKT&BOM)

28. Update Clock Gen. schematic related by customer recommend . <Page 15> 94.05.20.
- Del R1328,R1329,R1330,R1331,R1332 and related net . (Modify CKT,BOM&Layout)
- Change U25.15 connection to FSB . (Modify CKT&Layout)
- Change U25.16,24,41 connection to +CK_VDD_DP . (Modify CKT&Layout)
- Change C734,C735,C736 connection to +CK_VDD_DP . (Modify CKT&Layout)
- Add R1389(NODP@0_0805),R1390(DP@0_0805),C1010(10U_0805) and related net . (Modify CKT,BOM&Layout)
- Change R1352,R1333 from @0_0402 to 0_0402 . (Modify CKT,BOM&Layout)

29. Update MXM schematic related by customer recommend . <Page 18> 94.05.23.
- Reserve R1391(@0_0402) from JP39.125 to CLKREQA# . (Modify CKT&Layout)
- Add R1392(0_0402) from JP39.157 to ADP_PRES . (Modify CKT,BOM&Layout)

30. Update LAN chip schematic related by customer recommend . <Page 25> 94.05.23.
- Reserve R284(@4.7K_0402_5%) from U6.L3 to V_3P3_LAN . (Modify CKT&Layout)
- Add T59 on U6.L3 . (Modify CKT&Layout)
- Add T60 on U6.M5 . (Modify CKT&Layout)
- Reserve Q94(@2N7002_SOT23) and change R1380 connection as update schematic . (Modify CKT&Layout)
- Del R1381 and short Q29.3 to GND directly . (Modify CKT& Layout)

31. Update Clock Gen. schematic related by customer recommend . <Page 15> 94.05.23.
- Reserve R1393(@0_0402_5%) from U25.46(CLKIREF) to +CK_VDD_DP . (Modify CKT&Layout)
- Reserve C1011(@0.1U_0402) from U25.46(CLKIREF) to GND . (Modify CKT&Layout)
- Reserve R1394(@10K_0402) from U25.2(PCI_EC) to +3VS . (Modify CKT&Layout)
- Remove R1353,R1333(@0_0402_5%) . (Modify CKT&BOM)

32. Update AC97 Codec to keep AD1981HD only schematic related by customer recommend and DFx issue improved . <Page 15,28> 94.05.23.
- Del C391,R403,R406,R388,R158,R159,C410,C408,C401,C398,R415,R364,C397,R1085(CLK_14M_CODEC) ,R418 and short U14.42 to GNDA . (Modify CKT,BOM&Layout)
- Add T88~T101 test point on the bottom side . (Modify CKT&Layout)

33. Update ICH7 SPI I/F related schematic by customer recommend . <Page 21> 94.05.24.
- Change R1284.1,R1285.1 and R1286.1 connection from +3VS to +3VALW . (Modify CKT& Layout)

34. Update TI PCI7611MLS/PCI7612 related schematic by customer recommend . <Page 23> 94.05.24.
- Change R594.2 and R602.2 connection from +VCC_SD to +VCC_SM_XD . (Modify CKT&Layout)

35. Update ICH7 SATA I/F related schematic by customer recommend . <Page 20> 94.05.24.
- Del JP45 pin8,9,10 +3VS connection . (Modify CKT& Layout)
- Del C997~C1000 . (Modify CKT,BOM&Layout)

36. Update ICH7 PATA I/F related schematic for SATA HDD support . <Page 20> 94.05.24.
- Add R556(100K_0402) . (Modify CKT&BOM)

37. Change some Capacitors for Lead Free designing . <Page 6,18,22,30> 94.05.25.
- Remove C939(@220U_C6_6.3V) and add C983(330U_D2E_2.5V) . (Modify CKT&BOM)
- Remove C633(@47U_25V_M) and add C1013~C1017(10U_1206_25V6M) . (Modify CKT,BOM&Layout)
- Remove C671(@100U_6.3V_M) and add C1012(150U_D_6.3VM) . (Modify CKT,BOM&Layout)
- Remove C670(@220U_C6_6.3V) and add C979(330U_DD2E_2.5V) . (Modify CKT&BOM)
- Remove C1,C527(@100U_6.3V) and add CC568,C567(150U_D_6.3V) . (Modify CKT&BOM)

38. Update the Accelerometer related and install the related BOM for Accelerometer enable . <Page 19,21,27,33>
- Change the net name from ACCEL_INT# to ACCEL_INT, ACCEL#_SB to ACCEL_SB, ACCEL_INT#_KBC to ACCEL_INT_KBC . (Modify CKT&Layout)
- Note R94 must be removed when R1354 stuff and R87 remove . (Modify CKT&BOM)
- Reserve D61,C1018,R1395,Q95 between ACCEL_INT and Q78.1 . (Modify CKT&Layout)
- Remove R1358,R1360 . (Modify CKT&BOM)

---------- 9rd Netin/BOM Transfer

39. Update Docking related schematic for Customer Smart Adaptor new function request . <Page 21,35>
- Change JP30.118 and R1387.1 net name to DOCK_ID . (Modify CKT&Layout)
- Add JP30.117(DOCK_ADP_SIGNAL) to ADP_SIGNAL by R1401(1K_0402_1%) . (Modify CKT,BOM&Layout)

40. Update AD1981HD related schematic for Vendor ADI review result . <Page 28>
- Change U18.2 connection from GND to AGND, move R258 between C551.1 and U18.2 . (Modify CKT& Layout)
- Change C409,C427,C431 from 0.1U_0402 to 0.1U_0805 . (Modify CKT,BOM&Layout)
- Add R1400(0_1206) between GND and AGND close to Codec area . (Modify CKT,BOM&Layout)
- Disconnect U14.14 and U14.15, disconnect U14.40 and U14.33 to AGND and add T102,T103,T104 on pin 14,40,33 . (Modify CKT&Layout)
- Add R1399(0_0805) replace L36(CHB2012U121(0805)) . (Modify CKT&BOM)
- Add C1019(10P_0402) to GND . (Modify CKT,BOM&Layout)

41. Update Accelerometer related schematic for Customer review result . <Page 27>
- Remove R1355(@0_0805), add D62(ACCEL@CH751H) between U64.3/19 and +3VS . (Modify CKT,BOM&Layout)
- Del R1358 and R1360 pull-down resistors . (Modify CKT,BOM& Layout)
- Add R1398(0_0402) to GND, del U64.29 to GND connection . (Modify CKT,BOM&Layout)

42. Change the Audio Amp chip from TI TPA6017A2_TSSP20 to MAXIM MAX9710_QFN20 and update related schematic for Customer Spec modified request . <Page 29>
- Change U39 from TPA6017A2_TSSOP20 to MAX9710ETP_QFN20 . (Modify CKT,BOM&Layout)
- Del D59,R613,R431,C93,R439,R438,C663,C664,R971~R974,C661 . (Modify CKT,BOM&Layout)
- Change C503,C502 from 0.047U to 0.1U . (Modify CKT,BOM&Layout)
- Add R1403(10K_0402) from U39.5 to C503.2, R1404(10K_0402) from U39.5 to U39.7 . (Modify CKT,BOM&Layout)
- Add R1405(10K_0402) from U39.1 to C502.2, R1406(10K_0402) from U39.1 to U39.19 . (Modify CKT,BOM&Layout)
- Add R1407(0ohm) from U39.4 to AGND;Add C1020(10U_1206) from +5VALW and GND . (Modify CKT,BOM&Layout)
- Add C1021(1U_0603) from U39.2 to AGND . (Modify CKT,BOM&Layout)
- Change C662 from @100U_6.3V to @150U_D_6.3V . (Modify CKT&Layout)

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EAL80 from DB-1 Step to DB-2 Step LA-2821 REV:0.1 -> 0.2 Modify <94.05.10.~94.05.30. >

43. Reserve a 0ohm resistor for time delay pass through schematic by Customer request. <Page 37> 94.05.27.
-Reserve R1402(@0_0402) between PWR_GD and PGD_IN . (Modify CKT&Layout)

44. Change the resistor value to tune the delay schematic by Customer request. <Page 37> 94.05.27.
-Change R38 from 100K_0402 to 47K_0402 . (Modify CKT&BOM)

45. Change BOM option for Intel chipset ver:A1 by Customer recommend . <Page 7,21> 94.05.27.
-Change R1309 from @0_0402 to 0_0402, remove R1015(@100K_0402) . (Modify CKT&BOM)

46. Add a 0ohm resistor for debug by Customer recommend . <Page 4,20> 94.05.27.
-Add R1408(0_0402) between U26.H22 and H_STPCLK# . (Modify CKT,BOM&Layout)

47. Add a 0.1UF CAP to improve Cut Moat issue for RGB signals . <Page 36> 94.05.27.
-Add C1022(0.1U_0603) between +3VS and +VCCP . (Modify CKT,BOM&Layout)

48. Add 10Kohm pull-high to +VCC_SM_XD for TI FAE recommend . <Page 23> 94.05.27.
-Add R1396 and R1397(10K_0402) Pull-High to +VCC_SM_XD for MSBS_SDCMD_SMWE# and SDCLK_SMRE# . (Modify CKT,BOM&Layout)

49. Update TPM related schematic for Vendor review result . <Page 32> 94.05.27.
-Add R1409(TPM1.2@0_0402) from U66.7 to GND, remove R1379(@4.7K_0402) . (Modify CKT,BOM&Layout)
-Change C193.1 connection from +3V to +3VALW for TPM1.2 . (Modify CKT& Layout)

EAL80 from SI-1 Step to SI-2 Step LA-2821 REV:0.3 -> 0.4 Modify <94.08.23.~94.09.21. >

1. Add discharge circuit for BT_LED and WL_LED to solve the LED always light on issue. <Page 32> 94.08.23.
-Add R1440 and R1441(100K_0402) for BT_LED and WL_LED discharge . (Modify CKT,BOM&Layout)

2. Remove DPRSLPVR NB side PullHigh resistor for Intel document update. <Page 7> 94.08.24.
-Remove R1209(@10K_0402) for DPRSLPVR . (Modify CKT&BOM)

3. Keep TPM1.2 on Board and Delete TPM1.1 Module Connector designing. <Page 32> 94.08.24.
-Del JP33,R1236,R1242,R1253,C191,C192,C193 and related schematic. (Modify CKT,BOM&Layout)

4. Update TPM1.2 chip PCB layout footprint. <Page 32> 94.08.24.
-Change U66 PCB Footprint from SLD9630TT_TSSOP28 to SLB-9635-TT-1P2_TSSOP28. (Modify CKT&Layout)

5. Correct ODD CSEL option setting. <Page 20> 94.08.24.
-Remove R460(@4.7K_0402) and add R557(470_0402). (Modify CKT&BOM)

6. Correct SPI I/F Power Source for Capell_Valley_CRB_Schematics_Rev1_502.pdf update . <Page 32> 94.08.26.
-Change U61.8, U65.8, R1287.1 and R1288.1 Power Rail from +3VS to +3VALW. (Modify CKT&Layout)

7. Modify Mini-Card debug interface design for customer update . <Page 27> 94.08.30.
-Move +3VALW from pin 39 to pin 45 and move CAPS_LED# from pin 41 to pin 51. (Modify CKT&Layout)

8. Update ADI1981HD CIS symbol and PCB Footprint . <Page 28> 94.08.30.
-Update U14 CIS symbol and change PCB Footprint from AD1981B_LQFP48 to AD1981HDJSTZ-REEL_LQFP48. (Modify CKT&Layout)

9. Change PCI-E Ports for ICH7 modify . <Page 21,24,35> 94.08.31.
-Change ExpressCard (NC) connection to port 3, Change Docking connection to port 4. (Modify CKT&Layout)

10. Update Accelerometer related design for customer request . <Page 19,21,33,36> 94.09.02.
-Del D61, C1018, R1395 & Q95. (Modify CKT&Layout)
-Add Q75, R187; change D12 to Dual LED. (Modify CKT,BOM&Layout)
-Add net HDD_STP# from GPIO19 of ICH7 to Q75. (Modify CKT&Layout)
-Install R1374 and change R1060 to no-stuff. (Modify CKT&BOM)
-Del R1363 and R1364; Add SB GPIO test pad T80,T89,T99,T106. (Modify CKT,BOM&Layout)

11. Modify Mini-Card debug interface design for customer update . <Page 27> 94.09.02.
-Remove R1435 and R1436(@0_0402). (Modify CKT&BOM)

12. Modify TI PCI7612 designing for vendor request . <Page 23> 94.09.06.
-Change R573 from 10K_0402 to 0_0402. (Modify CKT&BOM)
-Change R594,R1396 and R1397 from 10K_0402 to 100K_0402. (Modify CKT&BOM)
-Change R602 from 10K_0402 to 22K_0402. (Modify CKT&BOM)

13. Update Accelerometer related design for customer request . <Page 19,21,33,36> 94.09.02.
-Add net HDD_STP from GPIO19 of ICH7 to Q84.2. (Modify CKT&Layout)
-Add Q84(2N7002) and R1442(100K_0402) for HDD_STP. (Modify CKT,BOM&Layout)
-Reserve R1443(@0_0402) for HDD_STP#. (Modify CKT&Layout)

14. Update ICH7 GPIO related design for customer request . <Page 21> 94.09.06.
-Del R1321 and R1323 related reserved schematic. (Modify CKT&Layout)

15. Modify LAN controller related for customer request . <Page 25> 94.09.07.
-Add and change R277 from @0_0402 to 10K_0402. (Modify CKT&BOM)
-Remove R1380(@0_0402) and add Q94(2N7002). (Modify CKT&BOM)
-Change R506 pull-up to +3VALW from V_3P3_LAN. (Modify CKT&Layout)
-Add Q100(SI2301BDS), reserve R83(@0_0402) and related schematic. (Modify CKT,BOM&Layout)

16. Modify PCMCIA Connector design for M/E team request . <Page 24> 94.09.08.
-Change JP9 PCBFootprint from SLINK_AFH-1000-17A0-3_104P to TYCO_C-PT05-023-D1_150P_LT. (Modify CKT,BOM&Layout)

17. Delete New Card, USB HUB related design for customer Spec update . <Page 15,21,24,30,31> 94.09.08.
-Delete R1272,R1273,R1274,R1275,R1276,R1277,R1278,R1279,R1280,R1282,R1316,C959,C960,C961,C962, C963,C964,C965,C966,C967,C968,C969,C970,C971,C972,C973,U60,R535,C541,L34,C521,C529,C535,C517, C558,C540,C559,R981,U53,Y6,R984,C22,C27,L37,R1353,R537,R539,R523,R1317,R1318,R1099,R1102, R1100,R1103,C712,C713; Add T107. (Modify CKT,BOM&Layout)
-Delete R982,R983 reserve. (Modify CKT&Layout)

18. Modify MiniCard related design for customer request. <Page 27> 94.09.08.
-Add Q101,Q102,R1445; Reserve R1444(@0_0805). (Modify CKT,BOM&Layout)

19. Delete FWH I/F BIOS related design for customer request. <Page 15,19,20,21,32> 94.09.08.
-Del &U21(SST49LF008A-33-4C-NH),U21,U20,R273,R278,RP42,R1125,C42,C333. (Modify CKT,BOM&Layout)
-Del R279,C43 reserve. (Modify CKT&Layout)
-Add T108,T109,T110. (Modify CKT&Layout)
-Delete BIOS_SEL1 and replace with short to GND directly. (Modify CKT&Layout)

20. Wire VGA Thermal inform signal with System side for function workable. <Page 21> 94.09.09.
-Add R252(0_0402). (Modify CKT&BOM)

21. Modify MiniCard related design for customer. <Page 27> 94.09.10.
-Add J44(JUMP_43X39) and reserve J45(@JUMP_43X39) for Power Source option. (Modify CKT&Layout)
-Change R1444.1 connection from +3VALW to +3VS. (Modify CKT&Layout)
-Remove Q101,Q102,R1445 and add R1444. (Modify CKT&BOM)

22. Modify TI PCI7612 designing for vendor request . <Page 23> 94.09.10.
-Change R573.1 power connection to +SC_PWR from +5VS. (Modify CKT&Layout)
-Change power rail to R615 & R616 to +3VS from +5VS and remove both R615 & R616. (Modify CKT, BOM&Layout)

23. Modify LAN Transformer designing for customer request . <Page 26> 94.09.10.
-Change R270,R271 connection by add C333 between ground and R270/R271 . (Modify CKT,BOM&Layout)

24. Create an option to use the 32KHz clock from KBC for TPM1.2 for customer request . <Page 32,33> 94.09.10.
-Reserve R1446(@0_0402) to connect U47.58 and U66.13. (Modify CKT&Layout)

25. Delete MiniPCI Debug I/F reserve for Layout space free . <Page 19,27,32> 94.09.12.
-Del R1117,R235,R441,R447,R451,R452 and JP20. (Modify CKT,BOM&Layout)
-Del R448,C537,R437 and Q49 reserve. (Modify CKT&Layout)
-Change R1420.1 connection from +3VALW to +3VL. (Modify CKT&Layout)
-Change C292,C538,C542 power source from +3VS to +3VS_MINI. (Modify CKT&Layout)
-Add H29,H30(H_C236D157)(MiniCard Stand Off). (Modify CKT,BOM&Layout)

26. Change Jopen PAD for CIC DFx request . <Page 15> 94.09.12.
-Change J29 PCBfootprint to JUMP_43X39. (Modify CKT&Layout)

27. Change LAN chip desgin to switch LAN power with LP_EN# for customer request . <Page 25> 94.09.13.
-Install R15(4.7K_0402_5%) and no-stuff U36(@SN74LVC1G17DBVR_SOT23-5). (Modify CKT&BOM)

28. Modify TPM1.2 related design about the ADP_EN for customer request . <Page 32,33> 94.09.13.
-Reserve R1447(@0_0402) close to Y8.1. (Modify CKT&Layout)
-Reserve R1448(@0_0402) for ADP_EN. (Modify CKT&Layout)

29. Modify BT related design for customer request . <Page 30> 94.09.14.
-Change R454 to 47K from 1K. (Modify CKT&BOM)
-Reserve a 0.1uF cap (no-stuff) from R454.2 to ground. (Modify CKT&Layout)

30. Modify LAN chip related design for customer request . <Page 25> 94.09.14.
-Add R458(0_0402) between Q100.2 and Q94.1. (Modify CKT,BOM&Layout)

31. Modify BITCLK related design for EMI request . <Page 20,28,34> 94.09.14.
-Reserve R1032,C722 close to U14.6. (Modify CKT&Layout)
-Move R1028, C721 close to JP32.12; R1314,R371 close to U26.U1. (Modify CKT&Layout)

32. Modify LID_SW# related design for M/E request . <Page 34> 94.09.14.
-Add R1449 close to JP18.16. (Modify CKT,BOM&Layout)

33. Modify Clock Gen. related design for Vendor request . <Page 15> 94.09.14.
-Change R1092 from 475_0402_1% to 4.7K_0402_1%. (Modify CKT&BOM)

34. Modify NB chip CFG11 related design for Intel CRB Rev1_502 update . <Page 11> 94.09.14.
-Remove R1154(@2.2K_0402_5%). (Modify CKT&BOM)

35. Modify Smart AC Adaptor related design for customer request . <Page 11> 94.09.14.
-Change R1237 from 10K_0402 to 100K_0402. (Modify CKT&BOM)

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EAL80 from SI-1 Step to SI-2 Step LA-2821 REV:0.3 -> 0.4 Modify <94.08.23.~94.09.21. >

36. Add DDR2 Module Thermal inform function to NB for customer request. <Page 7,13,14> 94.09.15.

-Add R1450(0_0402) between DDR_THERM# and PM_EXTTS#0 . (Modify CKT,BOM&Layout)

37. Reserve a cap at JP30.P2 pin for +5VS of Docking for customer request. <Page 35> 94.09.15.

-Reserve C1033(@22U_0805_6.3V4Z) close to JP30.P2. (Modify CKT&Layout)

38. Delete Bulk Cap. Daul Layout design reserve for DFx request. <Page 18> 94.09.15.

-Change C633 from @47U_25V(Non-LF) to 100U_25V(250',10sec,LF); Del C1013~C1017 . (Modify CKT,BOM&Layout)

-Del C823(100U 6.3V M B (6.3X6.0) CV-AX),C939,C830,C806(220U_C6_6.3V_M_R15) . (Modify CKT&Layo ut)

-Del C979(220U_D2_2VK_R9); Change C670 to SF22001M300. (Modify CKT,BOM&Layout)

-Del C1012(150U_D_6.3VM); Change C671 to SF22001M300. (Modify CKT,BOM&Layout)

-Del C567,C568(150U_D_6.3VM); Change C1,C527 to SF22001M300. (Modify CKT,BOM&Layout)

39. Remove all Clock Gen. pairs Pull-Down Resistors for LP design recommend. <Page 15> 94.09.15.

-Remove R1071,R1073,R1076,R1082,R1119,R1122,R1094,R1096,R1258,R1260,R1112,R1116,R1250,R1252, R1124,R1127,R1134,R1137,R1238,R1239. (Modify CKT&BOM)

40. Modify XMIT_OFF related design for S/W request. <Page 27> 94.09.16.

-Add R1424(0_0402) between XMIT_OFF and XMIT_OFF#. (Modify CKT,BOM&Layout)

41. Modify TI PCMCIA Controller related design for Vendor request. <Page 23,24> 94.09.16.

-Add R591(0_0402) close to U42.E2. (Modify CKT,BOM&Layo ut)

-Add R617~R620,R623,R624(0_0402) close to JP41. (Modify CKT,BOM&Layout)

-Reserve C369,C372,C373,R593,R599,R613,R614 close to JP9. (Modify CKT&Layout)

-Remove R565. (Modify CKT&BOM)

42. Modify Audio Codec related design to avoid a small amount of noise on pin 2 could cause the codec to power up in a test mode. <Page 28> 94.09.21.

-Change R422 from @0_0402 to 10K_0402. (Modify CKT&BOM)

43. Modify ICH7 related design for ICH7M & 3945abg Host Interface auto-detect sequence Issue (Sighting# 80332). <Page 21> 94.09.21.

-Change decoupling caps (C710 & C711) from 0.1uF_0402 to 0.15uF_0603). (Modify CKT,BOM&L ayout)

44. Modify Clock Gen. all series termination resistors for the differential signals related design for ICS recommend. <Page 15> 94.09.21.

-Change R1070,R1072,R1075,R1081,R1118,R1121,R1257,R1259,R1093,R1095,R1144,R1145,R1123,R1126,R1111, R1115,R1249,R1251 from 33_0402 to 24_0402. (Modify CKT&BOM)

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