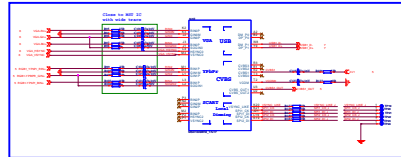
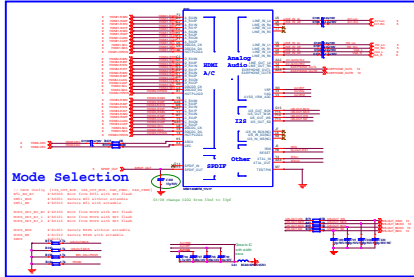


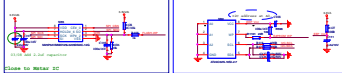
RGB & CVBS & USB



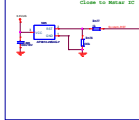
HDMI & Audio



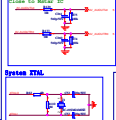
Boot Loader SPI Flash



RESET



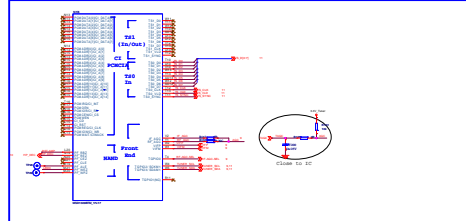
Audio Line Out



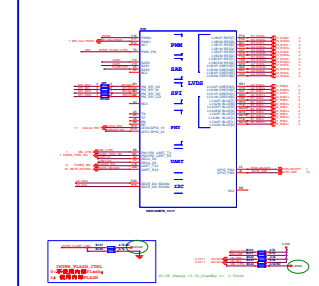
System STM



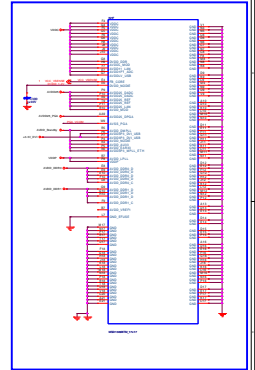
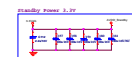
Front End



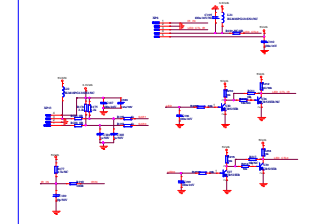
GPIO & LVDS

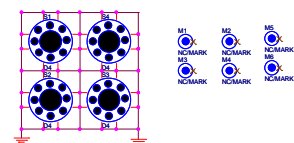
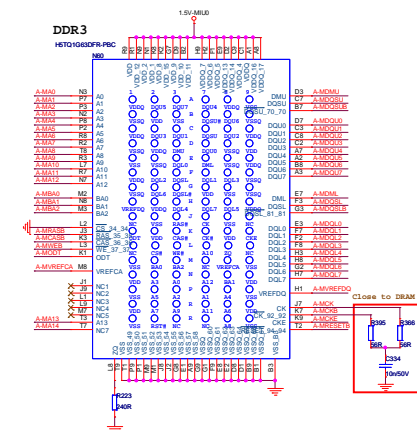
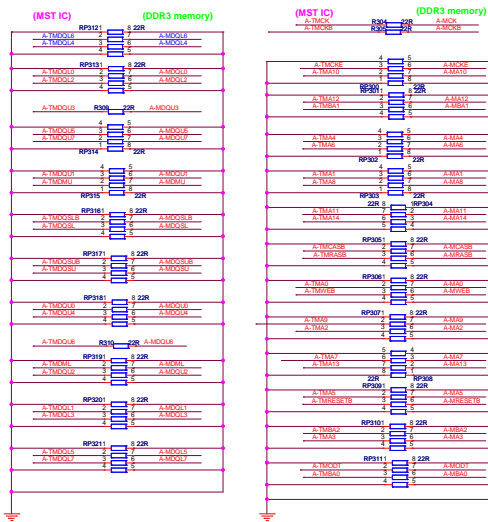
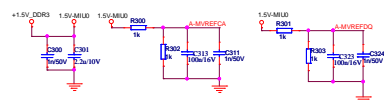
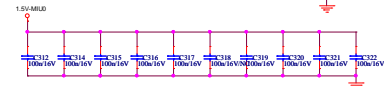


Decouple Capitors Close to IC pins

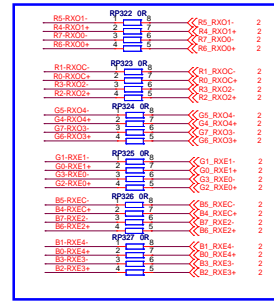
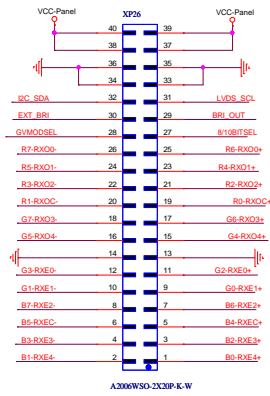
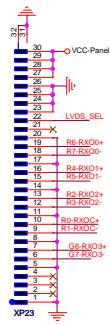


KEY PADS IR

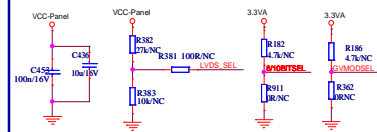




LVDS CONNECTOR 2 for CMI 24'



Power decouple



Note: 靠近LVDS插座

[illegible]

The schematic diagram illustrates the signal connections for the AVS-WBP-RGB module. It is divided into two main parts: RGB and HD.

RGB Section:

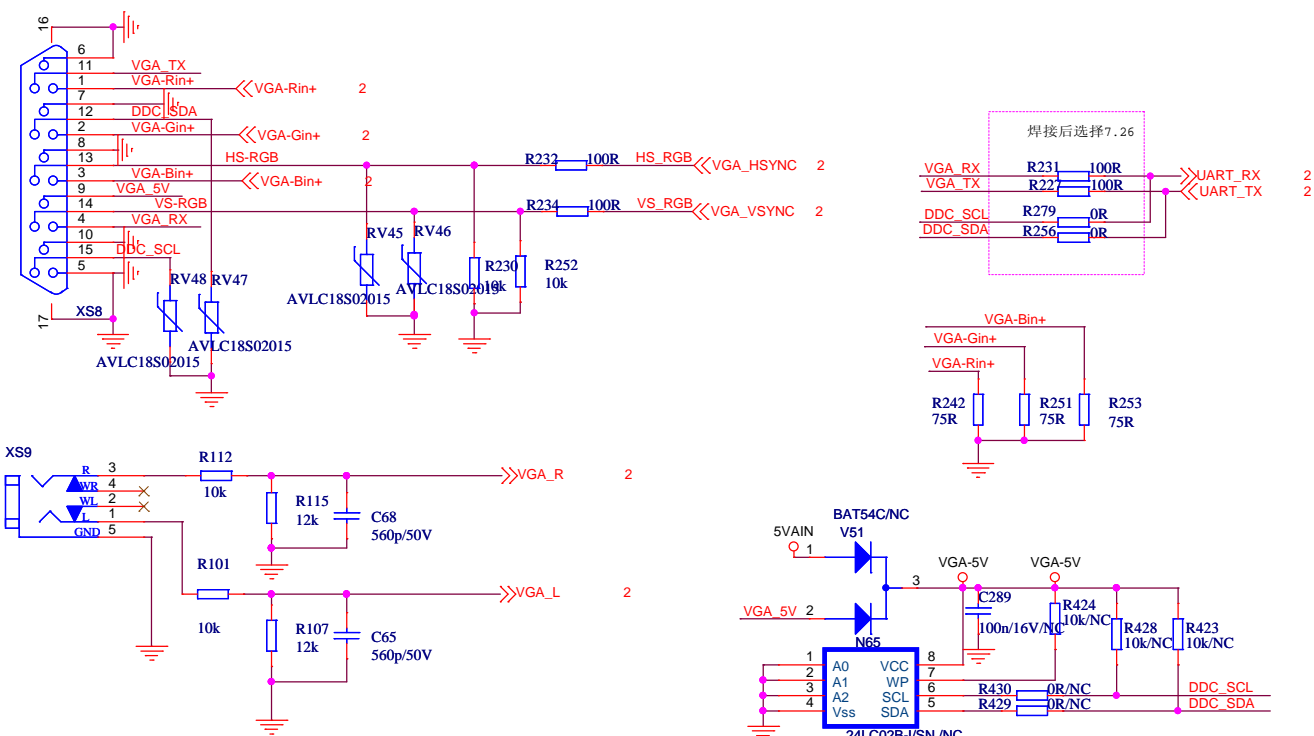
- Connector X5B:** A 6-pin connector with pins 1-6 and 7-8. Pins 1, 3, and 5 are connected to ground (GND). Pins 2, 4, and 6 are connected to RGB1_VPSP*_GND, RGB1_VPSP*_BTH, and RGB1_VPSP*_RTH, respectively. Pins 7 and 8 are connected to ground (GND).
- Signal Traces:** The RGB1_VPSP*_GND, RGB1_VPSP*_BTH, and RGB1_VPSP*_RTH signals are connected to termination resistors RV36, RV37, and RV38, respectively.
- Resistor Network:** A network of resistors (R234, R245, R246, R247, R248, R249, R250, R251) is connected to the signal traces and a 500pF capacitor, which is connected to ground.


HD Section:

- Connector XS10:** A 6-pin connector with pins 1-4 and 5-8. Pins 1, 3, and 5 are connected to ground (GND). Pins 2, 4, and 6 are connected to HD_L, HD_R, HD_Ln, and HD_Rn, respectively. Pins 7 and 8 are connected to ground (GND).
- Signal Traces:** The HD_L, HD_R, HD_Ln, and HD_Rn signals are connected to termination resistors RV39, RV40, and RV39, respectively.
- Resistor Network:** A network of resistors (R234, R245, R246, R247, R248, R249, R250, R251) is connected to the signal traces and a 500pF capacitor, which is connected to ground.

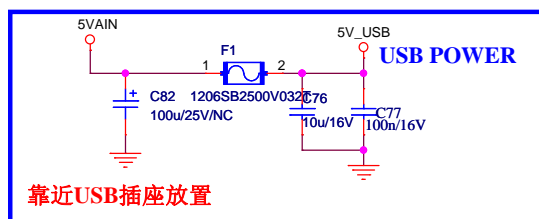
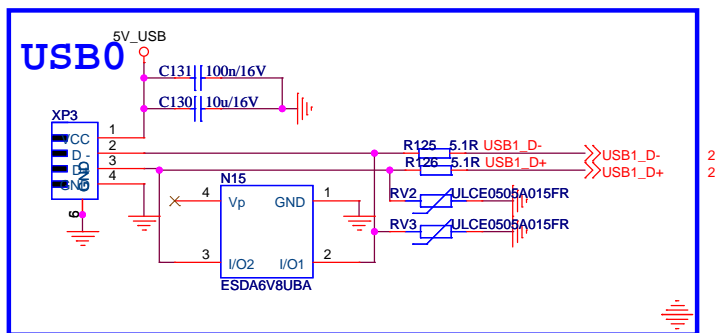
The circuit diagram shows a 5V input connected to the input of a 74VHC125 buffer. The output of the buffer is connected to a 10k pull-up resistor and a 100nF decoupling capacitor. The output is labeled CVB81_OUT.


VGA



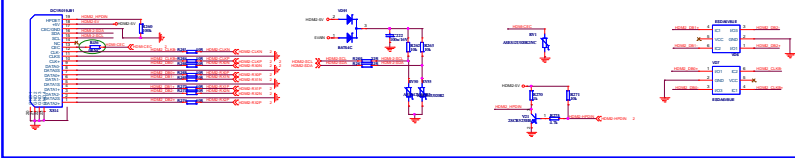
		Hisense Electric Co., Ltd. No.11, Jiangxi Road, Qingdao, China WWW.HISENSE.COM			
		Title Hisense MSD30XBT			
		Size	Schematic Name A <Doc>		Rev 1.0
		Date: Monday, January 21, 2013		Sheet 6 of 11	

USB INTERFACE

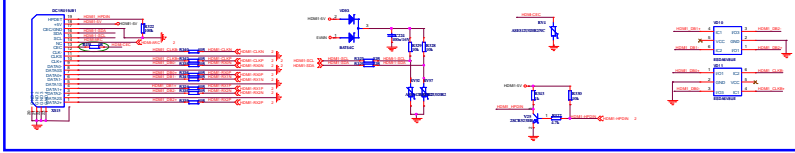


			Hisense Electric Co., Ltd. No.11,Jiangxi Road,Qingdao,China WWW.HISENSE.COM		
Title			Hisense MSD30XBT		
Size	Schematic Name				Rev
	A <Doc>				1.0
Date:			Monday, November 12, 2012	Sheet 7	of 11

HDMI1



HDMI2



HDMI3

