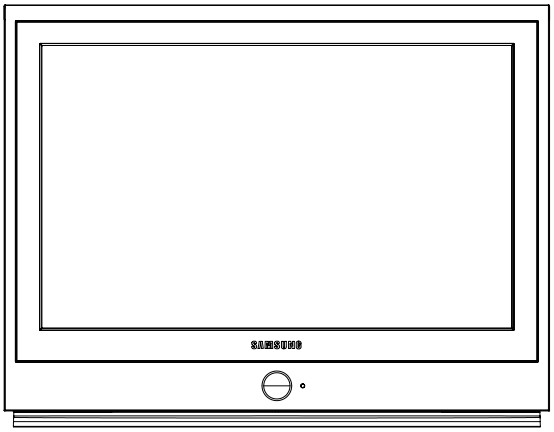
# LCD-TV

| Chassis | Model |
| --- | --- |
| VN32EO | LW32A23W |
| VN40EO | LW40A23W |

# SERVICE Manual

LCD-TV

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# Block Diagram

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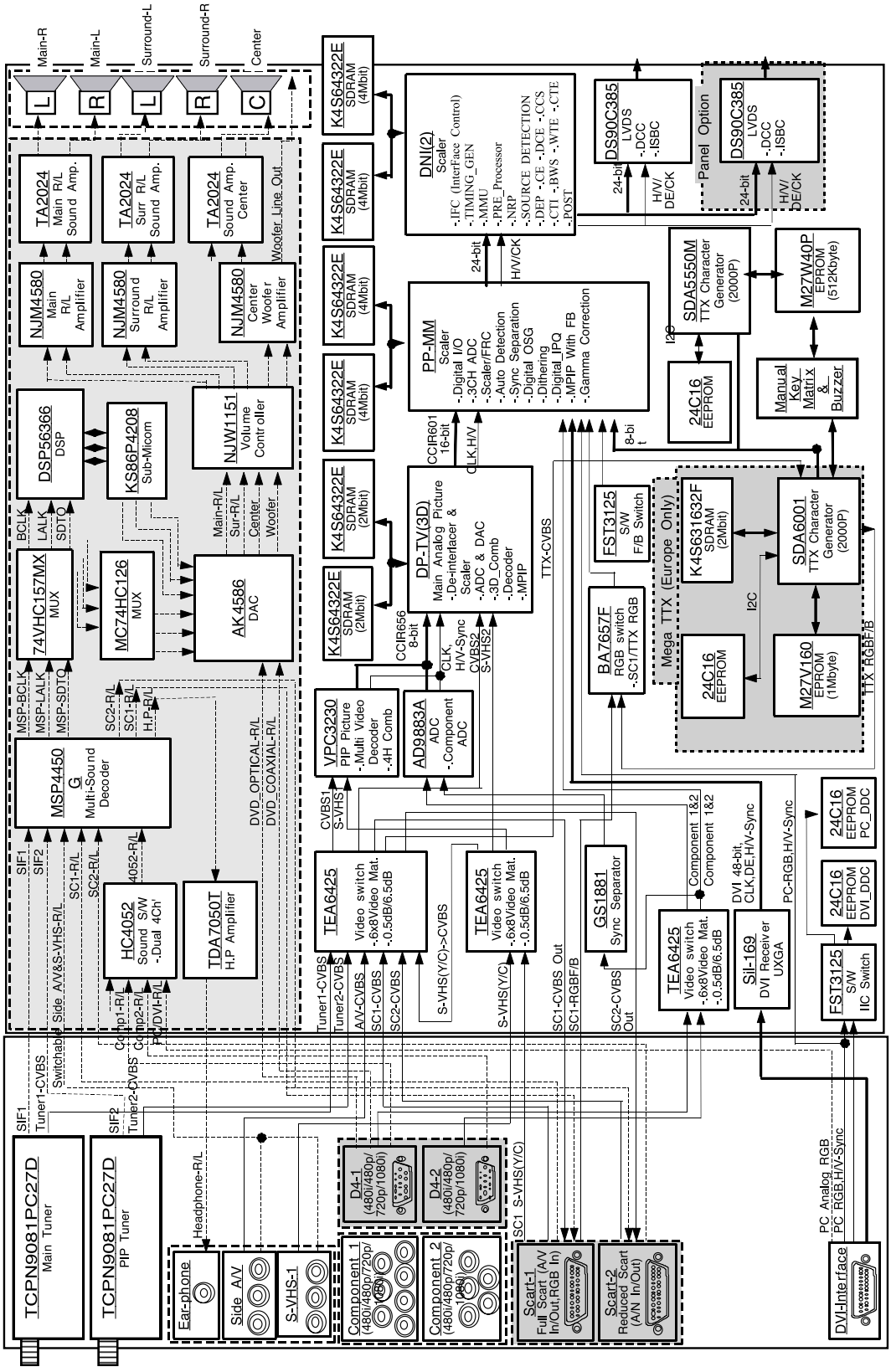
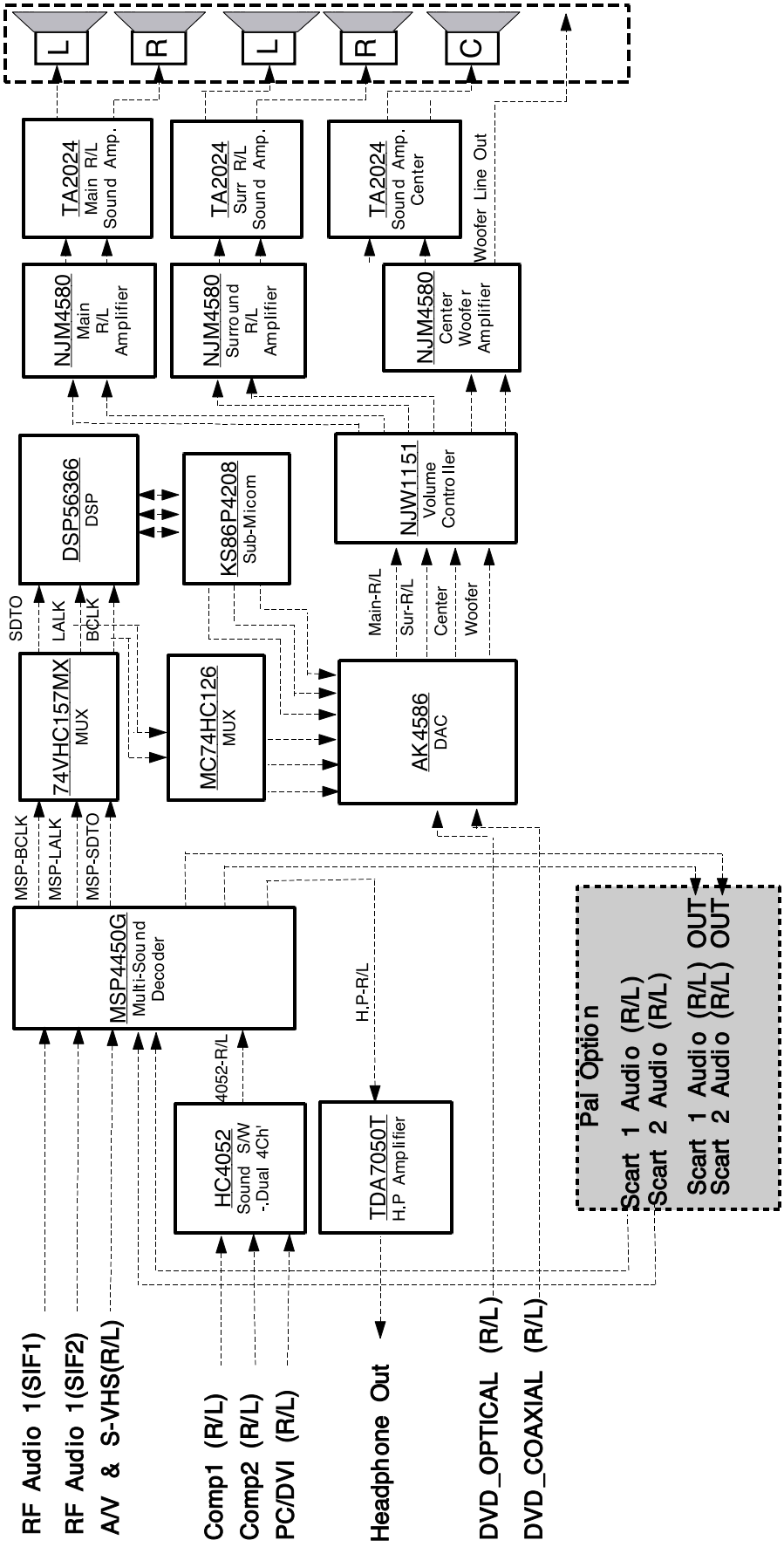
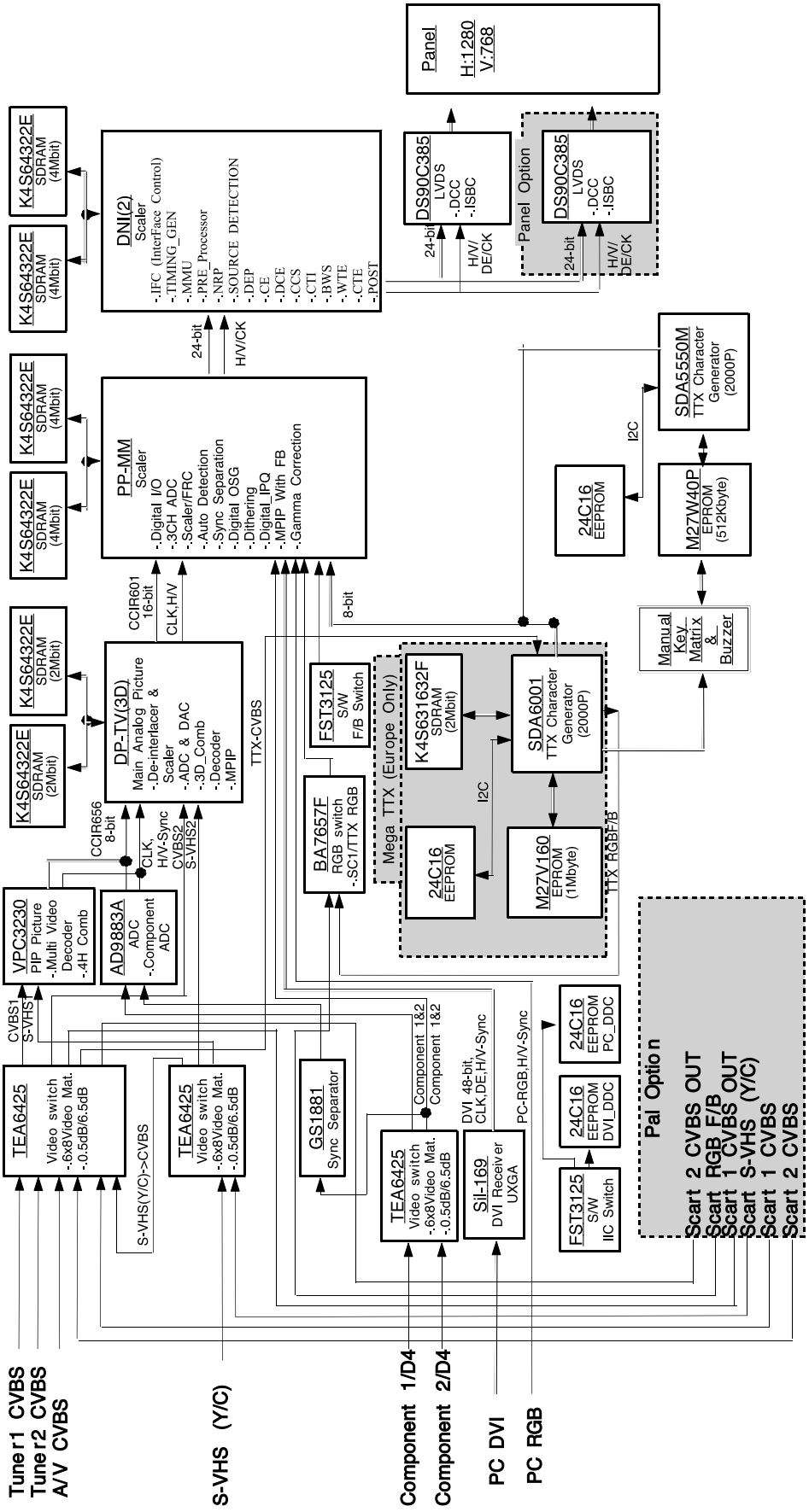
## Worldwide Full Multi-System Block diagram



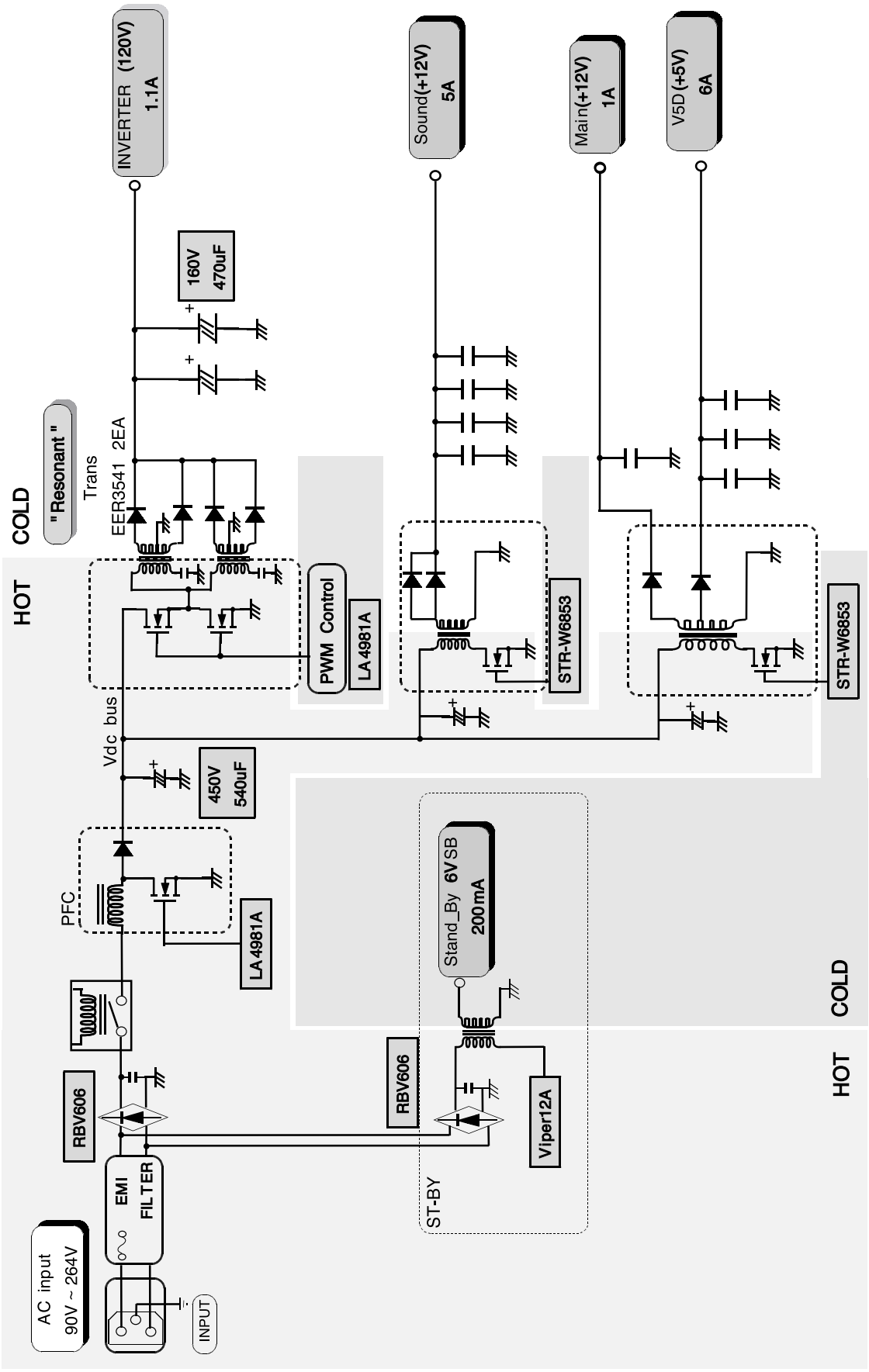
## Sound Block diagram



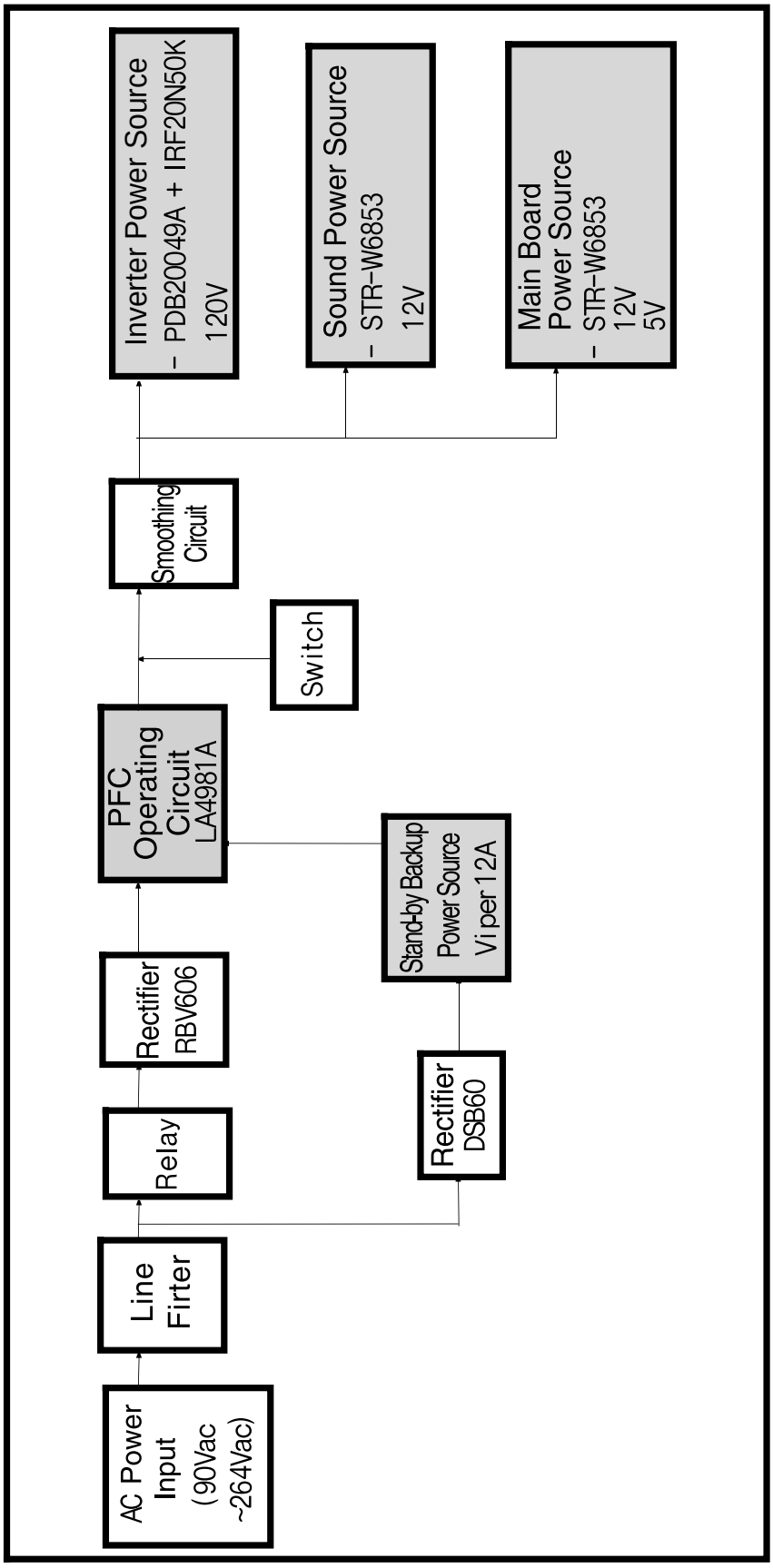
## Video Block diagram



## Power Block diagram

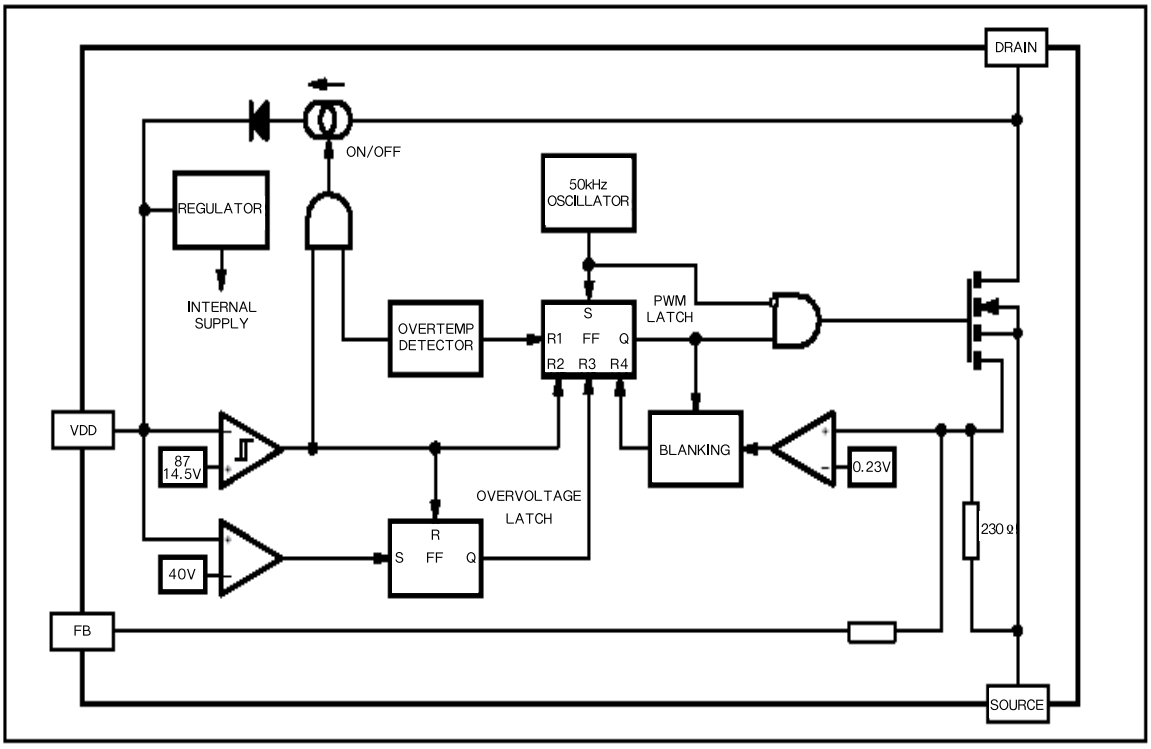


## LCD-TV 32”, 40” Power Block diagram



# Backup Power Source

## Viper 12A Block Diagram




## Pin Functions

| Name | function |
|---|---|
| VDD | For supplying power to the control circuit,dividing the charged current of the high-voltage current source connected to the drain during startup,and comparing VDD voltage hysteresis.<br>Divided into two threshold voltages VDDon to start switching and to disconnect the startup current source (normally 14.5V), and VDDoff to stop switching and to operate the startup current source (normally 8V) |
| SOURCE | Power MOSFET source and the circuit reference ground (GND) |
| DRAIN | Power MOSFET drain.Also used during startup as the internal high-voltage current source<br>until the external VDD capacitor is charged. |
| FB | Feedback input.Operating voltage range of 0V ~1V.Determined by the maximum MOSFET current value.<br>The current limit in due consideration of the maximum drain current is included in the FB pin that is connected to the source pin. |

# PFC Circuit

## Operating Principles

As the stand-by power circuit starts oscillating,the control IC of the PFC circuit (L4981) is applied with Vcc and starts oscillating. The oscillation frequency is determined by the resistance (RP824) connected to 17Pin and the condenser (CP816) connected to 18Pin. For regulation,the output voltage is divided by resistors and monitored by 14Pin. The 4Pin voltage, which is entered after dividing this voltage and the AC voltage by resistors, is calculated in the IC and the command value of the main FET is prepared. Therefore, the output voltage is controlled by the voltage determined by the dividing resistors, and the input current has the same waveform (sine wave) as the AC voltage, producing a power factor of almost 100%.

## Protections

1. Overvoltage

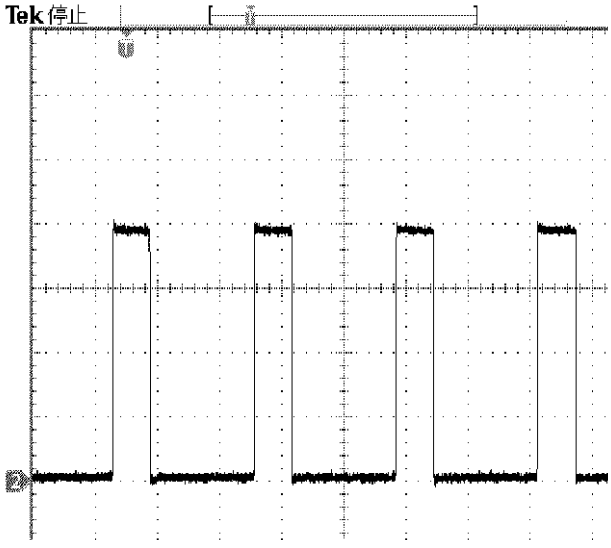
   The circuit has an overvoltage protection function of the voltage limit type. In the event of a sudden interruption of the input, of overshooting [overload?] during a sudden change of load,or non-control status, this function protects the circuit by narrowing the ON width of the FET and preventing the voltage from rising above the overvoltage setting. The overvoltage can be set with RP834, RP835, RP836 and RP840. (The power source is set to approximately 385V)

2. Overcurrent

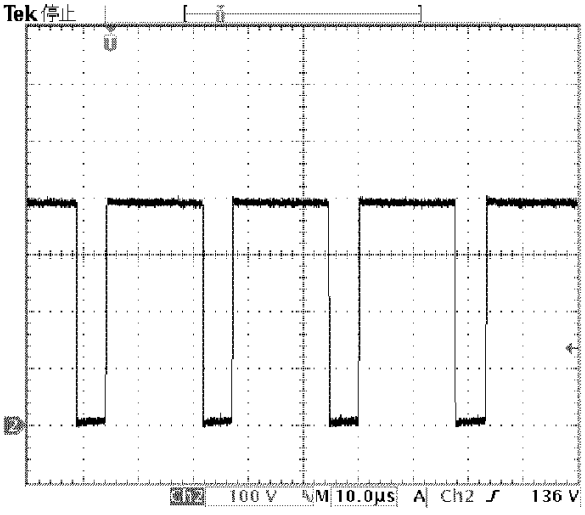
   The current is converted into the voltage value through RP831 and RP832,and monitored by 2 Pin and 8 Pin of the control IC. If the voltage of the detecting resistor rises above the set value due to an increase in current, the pulse width is narrowed to limit the output.

3. Thermal Shutdown

   Although the IC has a thermal shutdown function, a thermistor (TH) is installed on the heat-radiating fin of the main FET and the circuit is stopped if overheated by overload, etc.




FET VDS Waveform (Input of 100V)




FET VDS Waveform (Input of 230V)

# Resonance Circuit (Power Source for Inverter)

## Operating Principles

Explains the circuit of the power source for the inverter. With the operation of the MULTI block, a voltage is generated in the ancillary windings (4-5Pin) of T804S and is applied to 1 Pin (Vcc terminal) of the resonance circuit to start oscillation. High side FET (Q4) and low side FET (Q5) are turned on alternately, delivering energy to the secondary circuit. For voltage regulation, the output voltage is divided along resistors and monitored by the transistor (QI809), and the photo coupler (PC801S) is turned on or off. If the output , voltage rises, PC801S is turned on and draws current from 13 Pin of the resonance circuit. The switching frequency then increases, reducing the charge period of the resonance condenser (CI811) and thereby limiting the output voltage. On the other hand , if the output voltage decreases, no current is drawn from 13 Pin of the resonance circuit and the switching frequency decreases, extending the charge period of the resonance condenser and thereby raising the output voltage.

## Protections

1. Overvoltage

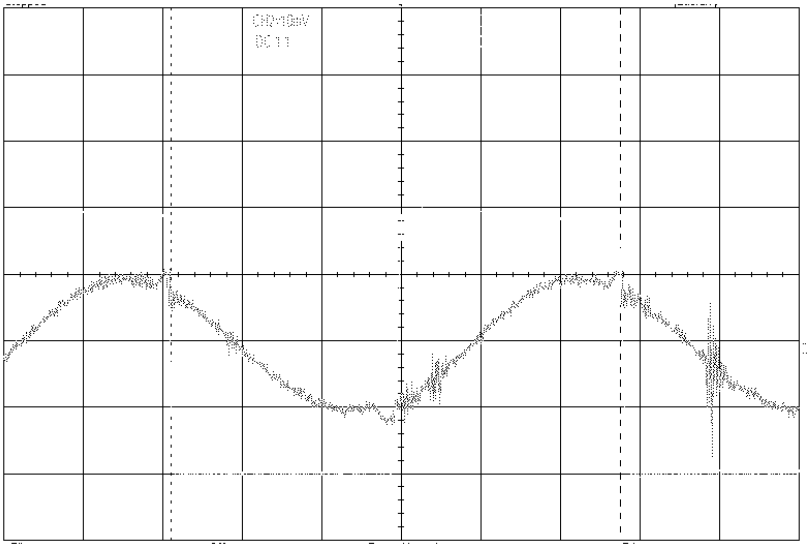
   The output voltage is divided along the resistors and monitored by QI810. If the output voltage rises, the QI810 voltage also rises, which triggers QO810 to turn PC802S on. This will increase the voltage at 5 Pin of the resonance IC, which stops oscillation in the latch mode.

2. Overcurrent

   The current flowing in the resonance condenser (CI811) is divided through CI808, converted into voltage at the resistors (RI809, RI816) and is monitored by 3 Pin of theresonance IC. If the output current rises, the current in the primary winding wire also rises, which triggers the voltage at 3 Pin of the IC to rise as well. If the voltage exceeds the set value, the pulse width is narrowed to limit the current.

3. Thermal Shutdown

   The resonance IC has a built-in thermal shutdown function and stops oscillation at over 125 ˚C



FET VDS Waveform of the resonance circuit

# Main Board Supply &Sound Exclusive IC of STR-W6853

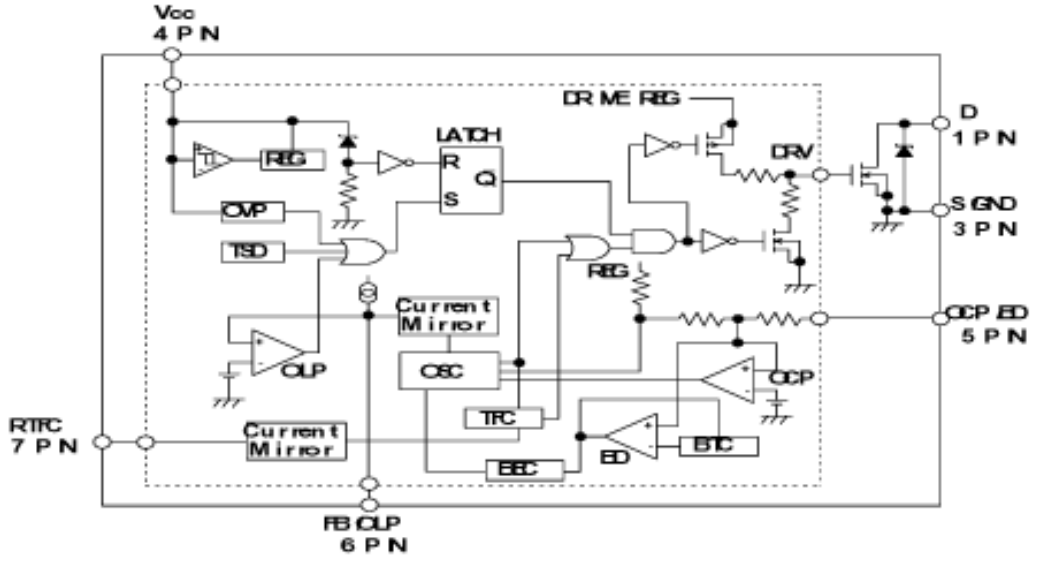
## Outlines

1. A new 7 Pin package has been developed from the existing 5 Pin package. High-power MOSFET is embedded in a small package to save space.
2. The distance between the pins of MOSFET drain & source has been widened to 1.8mm where high voltage is applied,allowing the loading of high anti-pressure MOSFET.
3. The operation mode changes in 3 stages according to the load applied, and saves power consumption. TFC, MBS, and pseudo-oscillation are available.

## Features

1. Improvement of power efficiency through automatic conversion of operation modes the controlling MIC part saves power consumption through a BCD processor. W6800 series changes the operation mode in 3 stages according to the load applied and saves power consumption.
   1) Pseudo-oscillation under load
   2) If MBS (Multi, Bottom, Skip) frequency exceeds 70 kHz under medium or small loads, the bottom is skipped while bottom, ON is maintained.
   3) If TFC (Time, Fix, Control)operation extends the ON time forcibly under St-By load, the OFF time is controlled to lower the oscillating frequency. In the event of compulsory ON, control by external resistors is possible.
2. Major Features
   1) Embedded overcurrent protection (OCP) of pulse by pulse
   2) Embedded overload protection (OLP) of latch shut down.
   3) Embedded thermal shutdown function.
   4) Embedded overvoltage protection for input voltage
   5) Adjustable frequency for TFC operation

# Block Diagram




## Terminal Functions

| Terminal Number | Symbol | Name and Functions |
|---|---|---|
| 1 | D | MOSFET Drain terminal |
| 2 | NC | Not Connect |
| 3 | S/GND | MOSFET Source / Ground terminal |
| 4 | Vcc | Control circuit power input terminal |
| 5 | OCD/BD | Overcurrent detection signal input terminal / Bottom detection signal input terminal |
| 6 | FB/OLP | Voltage control signal input terminal / Overload protection detection terminal |
| 7 | RTFC | Fixed ON time adjustment terminal |

## Other Functions

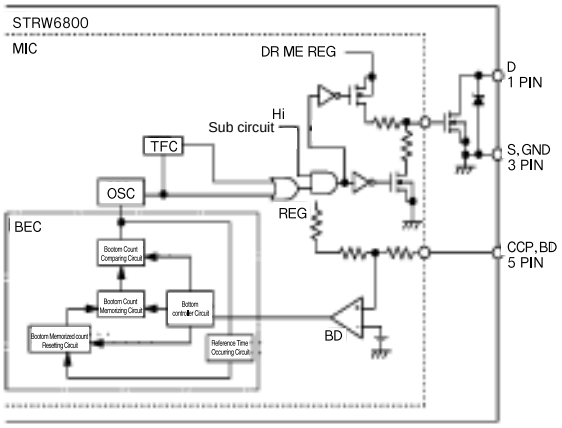
| Symbol | Functions |
|---|---|
| TSD | Thermal Shutdown Circuit |
| OVP | Overvoltage circuit |

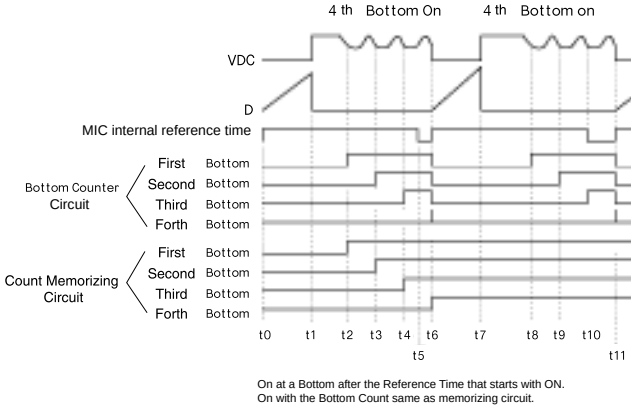
# Operation of W6853

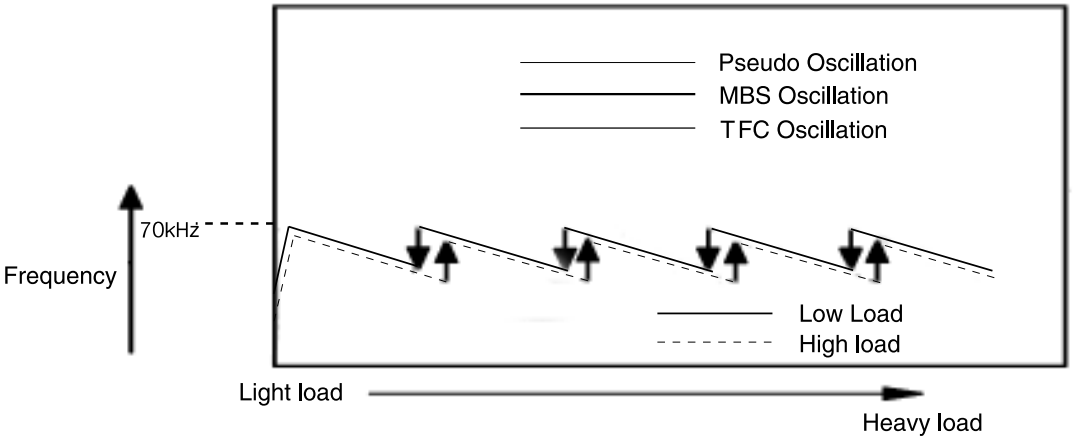
## Outlines

1. MBS : Multi bottom skip (medium load area)

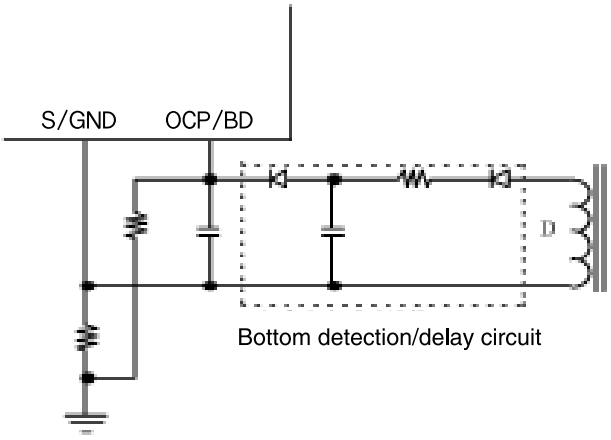
   The circuit has the PWM reference time T=14uS, 70 kHz internally and is designed to turn on at a bottom less than 14uS.

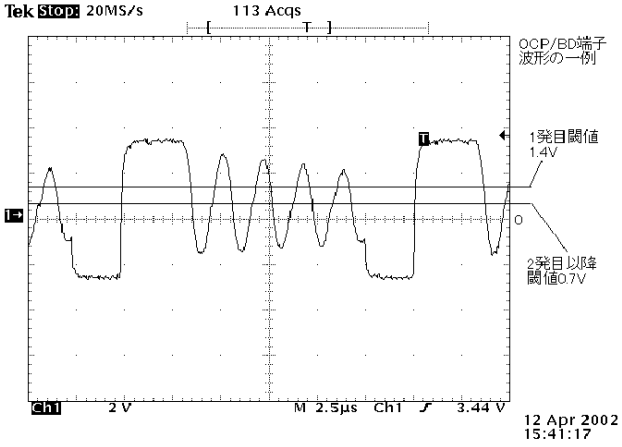


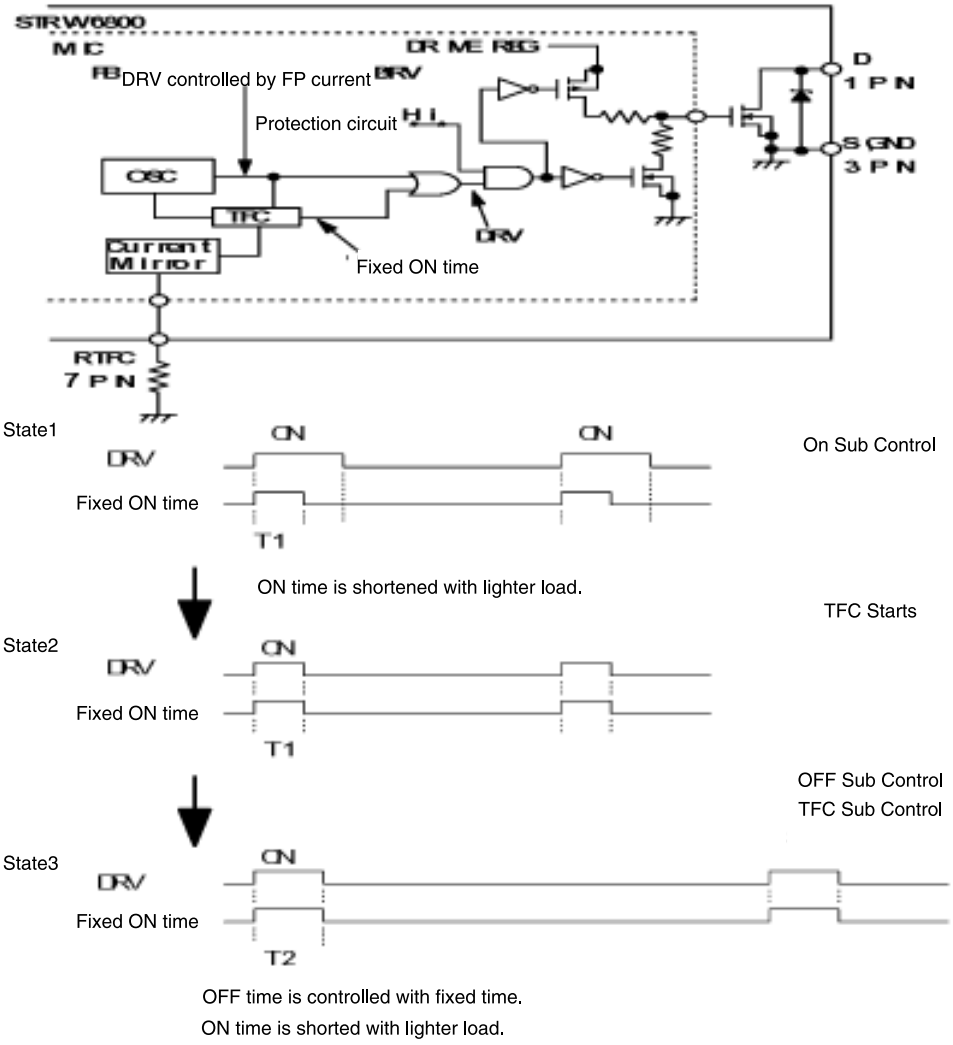




Note : MBS operations should not be counted in the overload, overcurrent area. (Bottom is not extended) If the overload condition continues, OLP will be triggered to shut down the operation. Normally ,it is not counted during startup, and if the down edge is detected only once after a count of 2, it is considered abnormal and the oscillation is stopped.

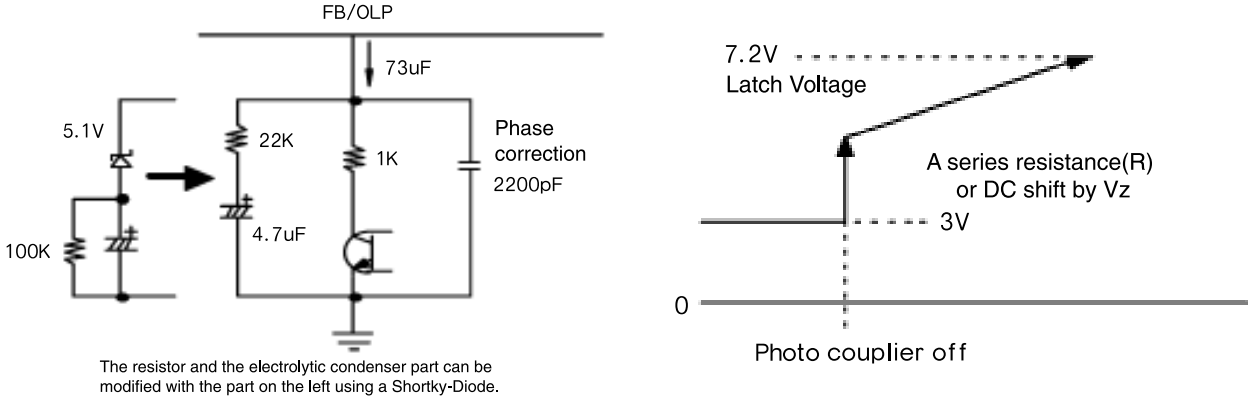


2. TFC : Time fix controller (Lighter load area during stand-by) TFC operation forcibly outputs to DRV an ON time (T2) that is longer than the fixed Ton (T1) inside the MIC to control the OFF time for stabilizing the output voltage. If MBS operation under light load moves toward the light load area again, the MBS operation is released at Ton=350 us and shifted to the TFS operation.

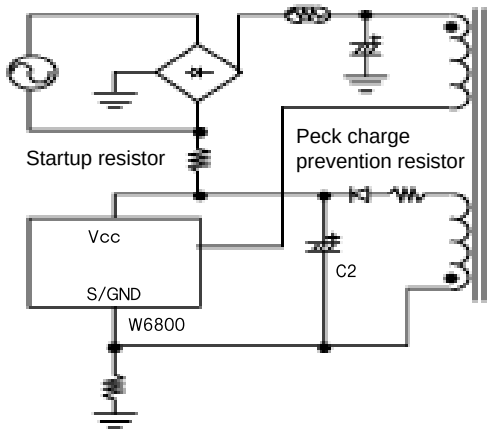


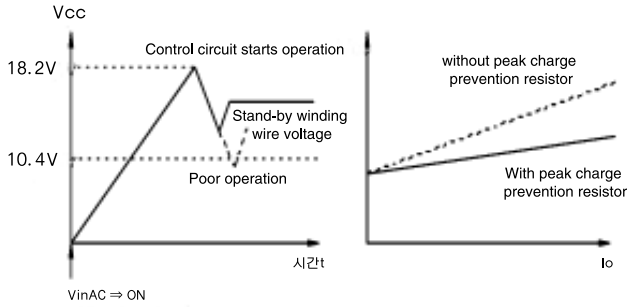

3. OLP



4. Vcc Terminal,Startup Circuit

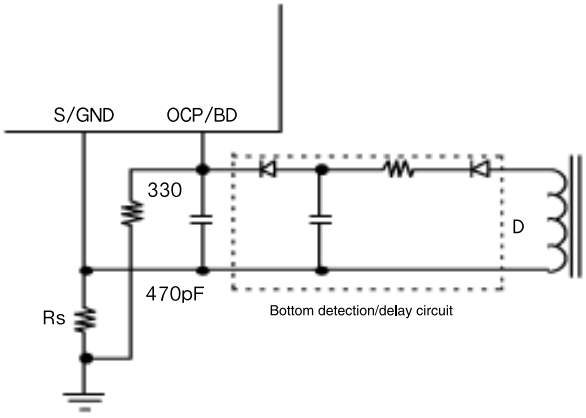
Startup is performed by the startup resistor and the condenser between Vcc and S/GND.
The startup voltage, Vcc is 18.2V (typ)and starts the circuit by charging C2 from the startup resistor.
After startup, operation continues with power supplied from the transistor drive winding wire .

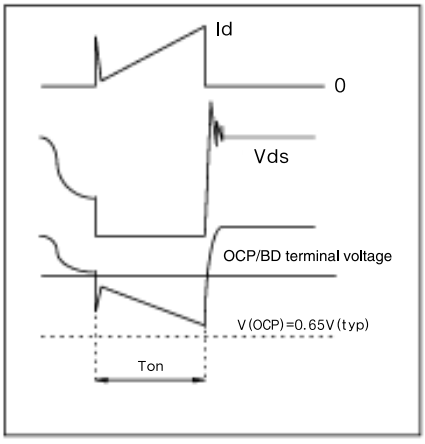


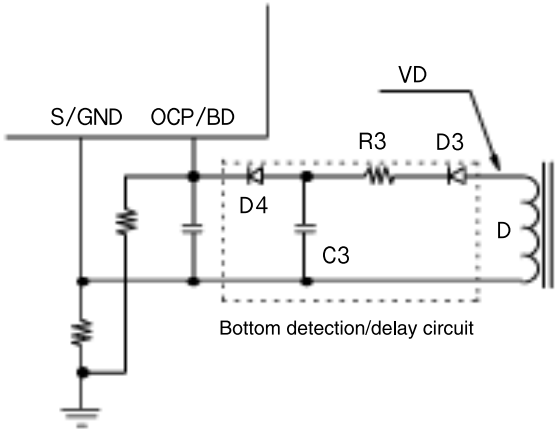

(Near the drive winding wire and stand-by power source;Startup of Vcc)

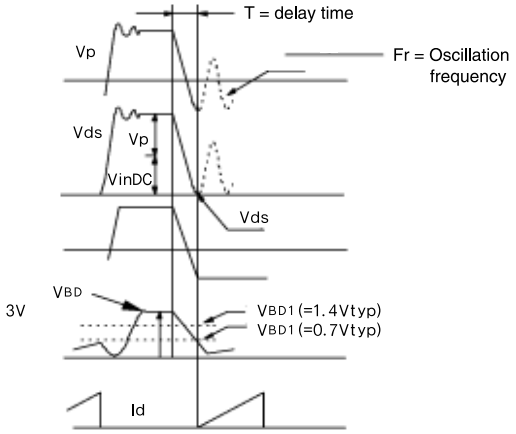
5. OCP / OLP



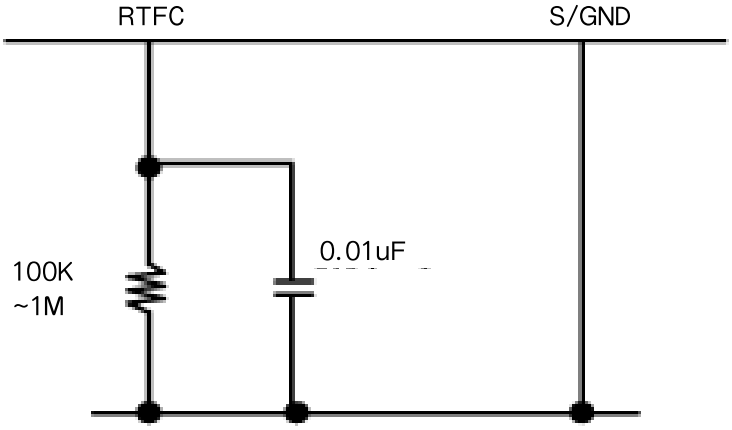

From the transistor design, under medium load with only one bottom left,it is possible for Id to exceed 50%of the normal pseudo oscillation duty.In particular,if there is still a bottom under the maximum load at VinAC (Min), confirming the condition is required. The following is an explanation of the pseudo oscillation signal input of the OCP/BD terminal.



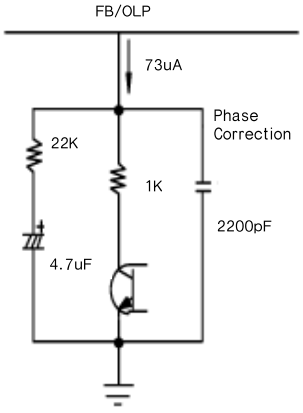




6. RTFC Terminal

Adjustment should be performed while checking the actual operation in the range of 100k to 1 M.During an IC examination, you may sometimes find minimum oscillating frequency at the RTFC resistor, but as the secondary circuit performs feedback control, Id determined by ton at RTFC shows changes in the peak value due to the primary inductance lp of the transistor and the winding ratio. If the load consumed by the secondary circuit is constant, the peak value of Id increases and the frequency decreases as lp becomes smaller and the ton setting becomes larger.




7. Phase Correction




When you have an unusual type of secondary feedback circuit and load specifications, if the phase correction of the error amp on the secondary circuit is not sufficient, due to the capacity of the smoothing input condenser being too small and the ripple voltage being too high, you can get a good result by adding a condenser between the FB/OLP terminal of W6800 and S/GND. The FB/OLP terminal is fitted with latch delay CR.If R is small, it may improve the shift start during startup,but may also cause extreme delay. Therefore ,care should be taken to avoid excessive response in changing the loads.

# Wiring Diagram

**CN510**

| | |
|---|---|
| 1 | VCC5I |
| 2 | VCC5P |
| 3 | VCC5P |
| 4 | VCC5P |
| 5 | VCC5P |
| 6 | GND_PANEL |
| 7 | GND_PANEL |
| 8 | GND_PANEL |
| 9 | PANEL_Y_DEC |
| 10 | PANEL_Y_INC |
| 11 | SW_ACCE |
| 12 | GND_PANEL |
| 13 | TXOUT 3+ |
| 14 | TXOUT 3- |
| 15 | GND_PANEL |
| 16 | TXCLKOUT+ |
| 17 | TXCLKOUT- |
| 18 | GND_PANEL |
| 19 | TXOUT 2+ |
| 20 | TXOUT 2- |
| 21 | GND_PANEL |
| 22 | TXOUT 1+ |
| 23 | TXOUT 1- |
| 24 | GND_PANEL |
| 25 | TXOUT 0+ |
| 26 | TXOUT 0- |
| 27 | GND_PANEL |
| 28 | SW_INVERTER |
| 29 | ANA_DIMMING |
| 30 | PWM_DIMMING |

**CN800**

| | |
|---|---|
| 1 | VCC12A |
| 2 | GND |
| 3 | VCC5A |
| 4 | VCC5A |
| 5 | VCC5A |
| 6 | GND |
| 7 | GND |
| 8 | GND |
| 9 | VCC12BS |
| 10 | VCC12BS |
| 11 | VCC12BS |
| 12 | GND_AMP |
| 13 | GND_AMP |
| 14 | GND_AMP |

**MAIN BOARD**

**CN505**

| | | | |
|---|---|---|---|
| 1 | SW_SMPS | 16 | AGND |
| 2 | GND | 17 | STD_VCC3B |
| 3 | STD_VCCGA | 18 | VCC5B |
| 4 | AGND | 19 | AGND |
| 5 | CH+_OUT | 20 | IR |
| 6 | VOL+_OUT | 21 | LED_GRN |
| 7 | BUZER_IN | 22 | LED_RED |
| 8 | AGND | 23 | AGND |
| 9 | CH-_OUT | 24 | AV_CVBS |
| 10 | VOL-_OUT | 25 | AGND |
| 11 | SOURCE_OUT | 26 | SVHS_Y |
| 12 | MENU_OUT | 27 | AGND |
| 13 | AGND | 28 | SVHS_C |
| 14 | STD_VCC5B | 29 | AGND |
| 15 | VCC5DDC | 30 | SC1_RGB_FB |

**CN506**

| | | | |
|---|---|---|---|
| 1 | SC1_R_SC1_SVHS_CI | 16 | AGND |
| 2 | SC1_G | 17 | Y_D1 |
| 3 | SC1_B_SC1_SVHS_CO | 18 | AGND |
| 4 | AGND | 19 | PB_D1 |
| 5 | SC1_CVBS_IN | 20 | PR_D1 |
| 6 | AGND | 21 | AGND |
| 7 | SC1_CVBS_OUT | 22 | Y_D2 |
| 8 | AGND | 23 | AGND |
| 9 | SC2_CVBS_IN | 24 | PB_D2 |
| 10 | AGND | 25 | PR_D2 |
| 11 | SC2_SVHS_CI | 26 | AGND |
| 12 | AGND | 27 | Y_COMP1 |
| 13 | SC2_CVBS_OUT | 28 | AGND |
| 14 | ANGD | 29 | PB_COMP1 |
| 15 | SC2_SVHS_CO | 30 | PR_COMP1 |

**CN509**

| | | | |
|---|---|---|---|
| 1 | Y_COMP2 | 16 | AGND |
| 2 | AGND | 17 | SC1_L_OUT |
| 3 | PB_COMP2 | 18 | SC1_R_OUT |
| 4 | PR_COMP2 | 19 | AGND |
| 5 | D4_1_CON1 | 20 | SC2_L_IN |
| 6 | D4_1_CONT2(SC1_S) | 21 | SC2_R_IN |
| 7 | D4_1_CONT3 | 22 | AGND |
| 8 | D4_2_CONT1 | 23 | SC2_L_OUT |
| 9 | D4_2_CONT2(SC2_S) | 24 | SC2_R_OUT |
| 10 | D4_2_CONT3 | 25 | AGND |
| 11 | AV_L | 26 | COMP1_L |
| 12 | AV_R | 27 | COMP1_R |
| 13 | GND | 28 | AGND |
| 14 | SC1_L_IN | 29 | COMP2_L |
| 15 | SC1_R_IN | 30 | COMP2_R |

**CN507**

| | | | |
|---|---|---|---|
| 1 | PC_L | 16 | DDC_DVI_SDAS |
| 2 | PC_R | 17 | IDENT_PC |
| 3 | AGND | 18 | RX0- |
| 4 | COAXIAL_IN | 19 | RX0+ |
| 5 | AGND | 20 | DGND |
| 6 | OPTICAL_IN | 21 | RX1- |
| 7 | AGND | 22 | RX1+ |
| 8 | PC_RED | 23 | DGND |
| 9 | PC_GREEN | 24 | RX2- |
| 10 | PC_BLUE | 25 | RX2+ |
| 11 | AGND | 26 | DGND |
| 12 | PC_DDC_HSYNC | 27 | RXC- |
| 13 | PC_DDC_VSYNC | 28 | RXC+ |
| 14 | AGND | 29 | DGND |
| 15 | DDC_DVI_SCLS | 30 | DDC_VCC5D |

**CN508**

| | | | |
|---|---|---|---|
| 1 | GND_AMP | 13 | MAIN_R_OUT1 |
| 2 | HP_IDENT | 14 | MAIN_R_OUT2 |
| 3 | GND_AMP | 15 | GND_AMP |
| 4 | HP_OUT_L | 16 | SUR_L_OUT1 |
| 5 | GND_AMP | 17 | SUR_L_OUT2 |
| 6 | HP_OUT_R | 18 | GND_AMP |
| 7 | GND_AMP | 19 | SUR_R_OUT1 |
| 8 | WOOFER_OUT | 20 | SUR_R_OUT2 |
| 9 | GND_AMP | 21 | GND_AMP |
| 10 | MAIN_L_OUT1 | 22 | CENTER_OUT1 |
| 11 | MAIN_L_OUT2 | 23 | CENTER_OUT2 |
| 12 | GND_AMP | 24 | GND_AMP |

# Schematic Diagrams

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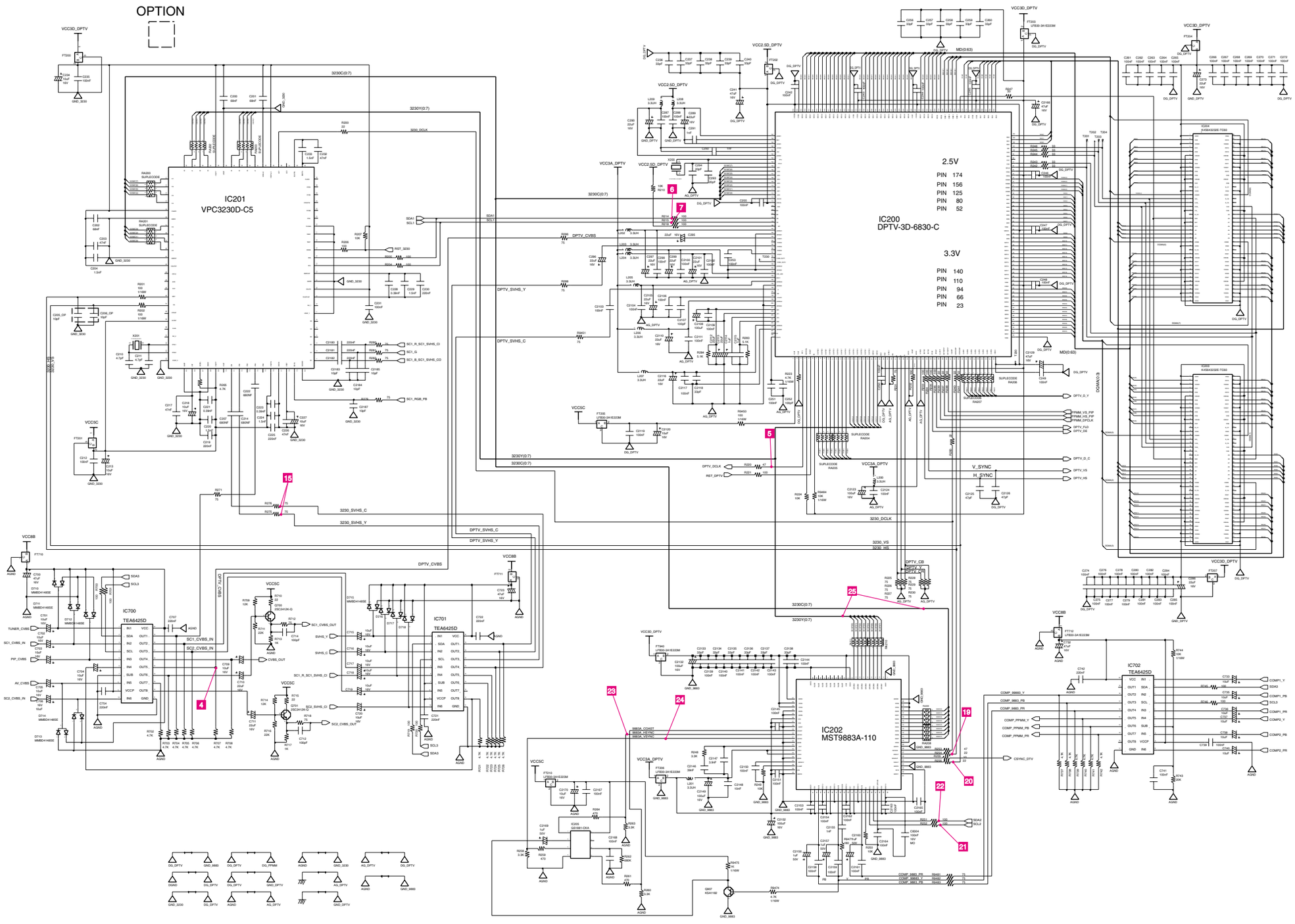
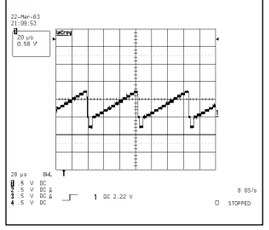
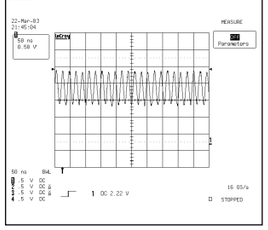
## DPTV, VPC3230, MST 9883 Block Schematic Diagram



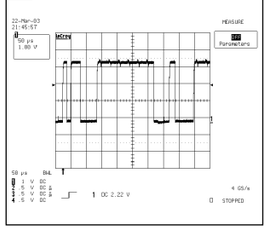
**4** CVBS Signal



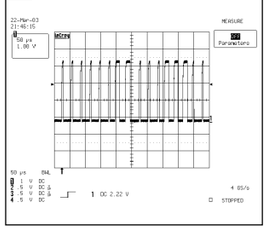
**5** IC200,#3 Clock Signal



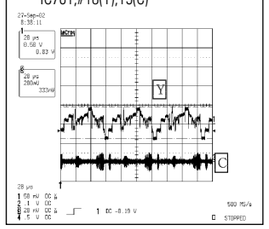
**6** IC200,#178 Communichion Data Signal



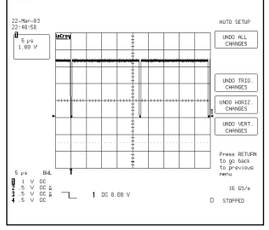
**7** IC200,#179 Communichion Clock Signal



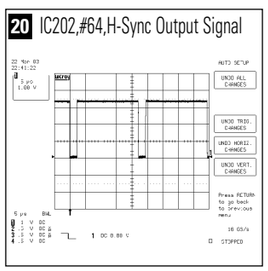
**15** S-Video signal,CN505,#26(Y),28(C), IC701,#18(Y),19(C)



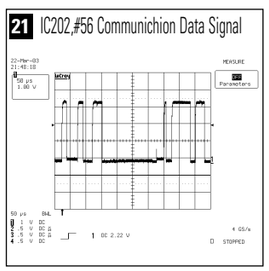

**19** IC202,#66,H-Sync Output Signal



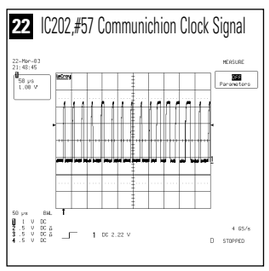
**20** IC202,#64,H-Sync Output Signal



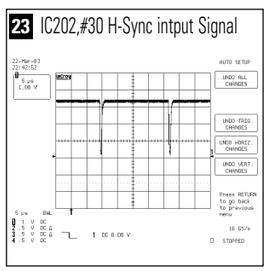
**21** IC202,#56 Communichion Data Signal



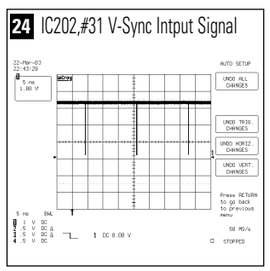
**22** IC202,#57 Communichion Clock Signal



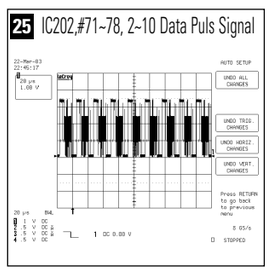
**23** IC202,#30 H-Sync intput Signal



**24** IC202,#31 V-Sync Intput Signal



**25** IC202,#71~78, 2~10 Data Puls Signal



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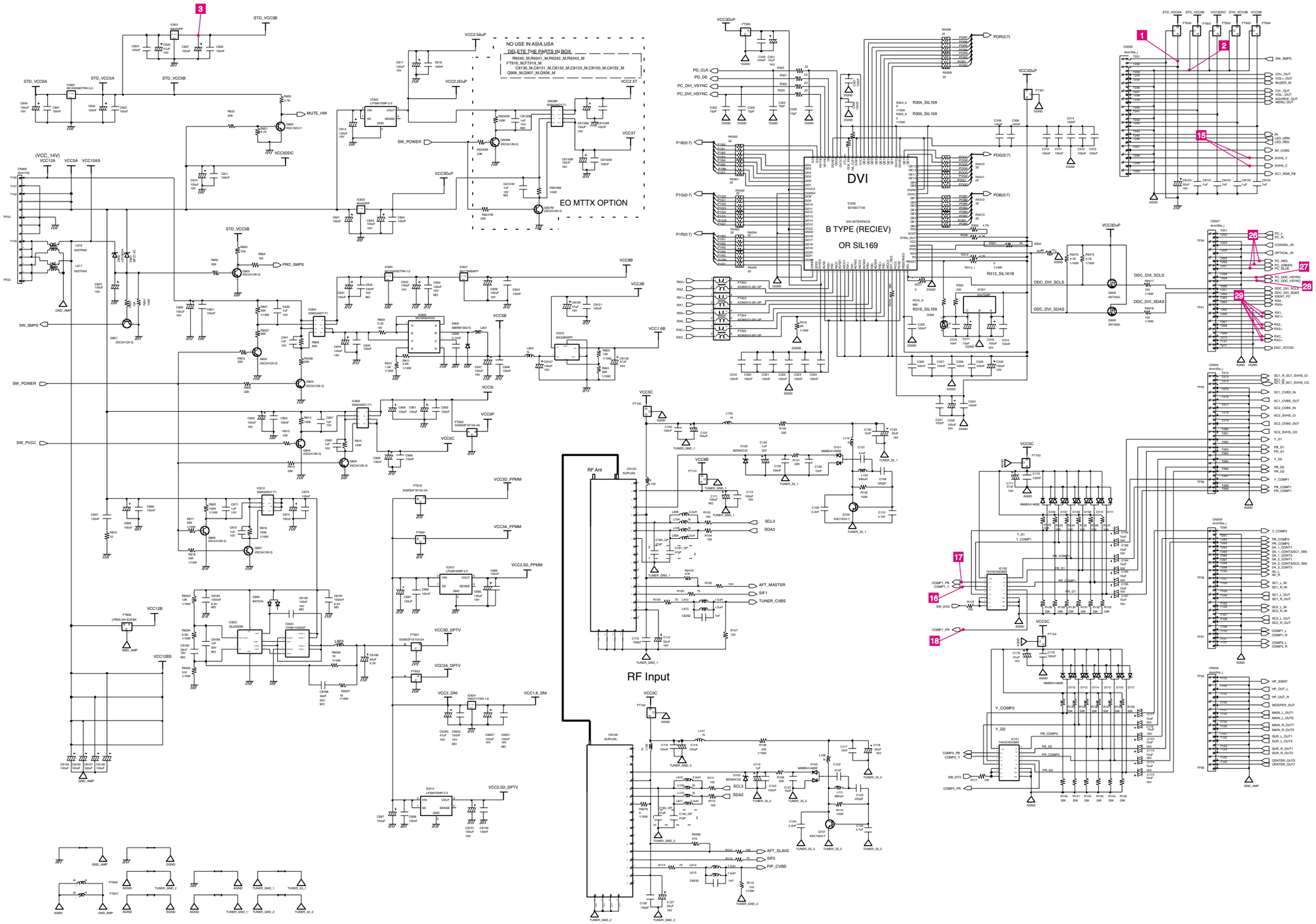
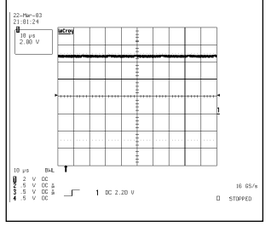
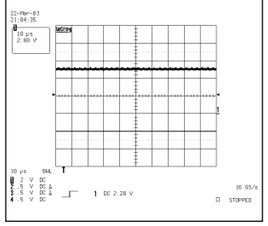
## Power, DVI, Tuner Block Schematic Diagram



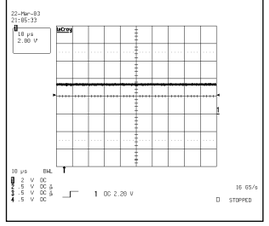
**1** DC 6V



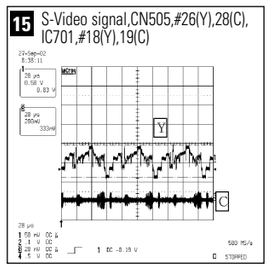
**2** DC 5V



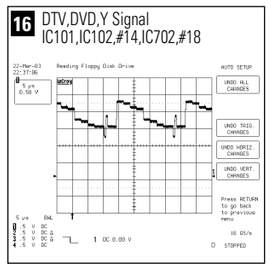
**3** DC 3V



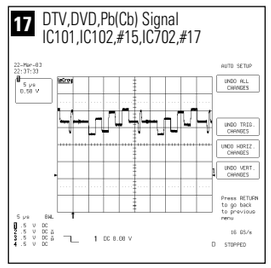
**15** S-Video signal,CN505,#26(Y),28(C), IC701,#18(Y),19(C)



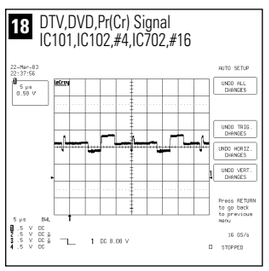

**16** DTV,DVD,Y Signal IC101,IC102,#14,IC702,#18



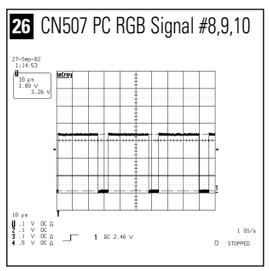
**17** DTV,DVD,Pb(Cb) Signal IC101,IC102,#15,IC702,#17



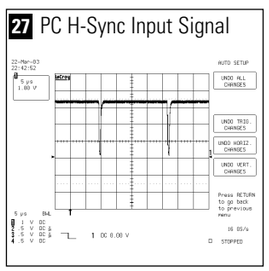
**18** DTV,DVD,Pr(Cr) Signal IC101,IC102,#4,IC702,#16



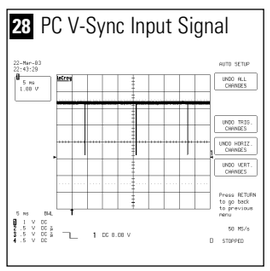
**26** CN507 PC RGB Signal #8,9,10



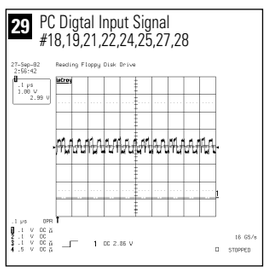
**27** PC H-Sync Input Signal



**28** PC V-Sync Input Signal



**29** PC Digtal Input Signal #18,19,21,22,24,25,27,28



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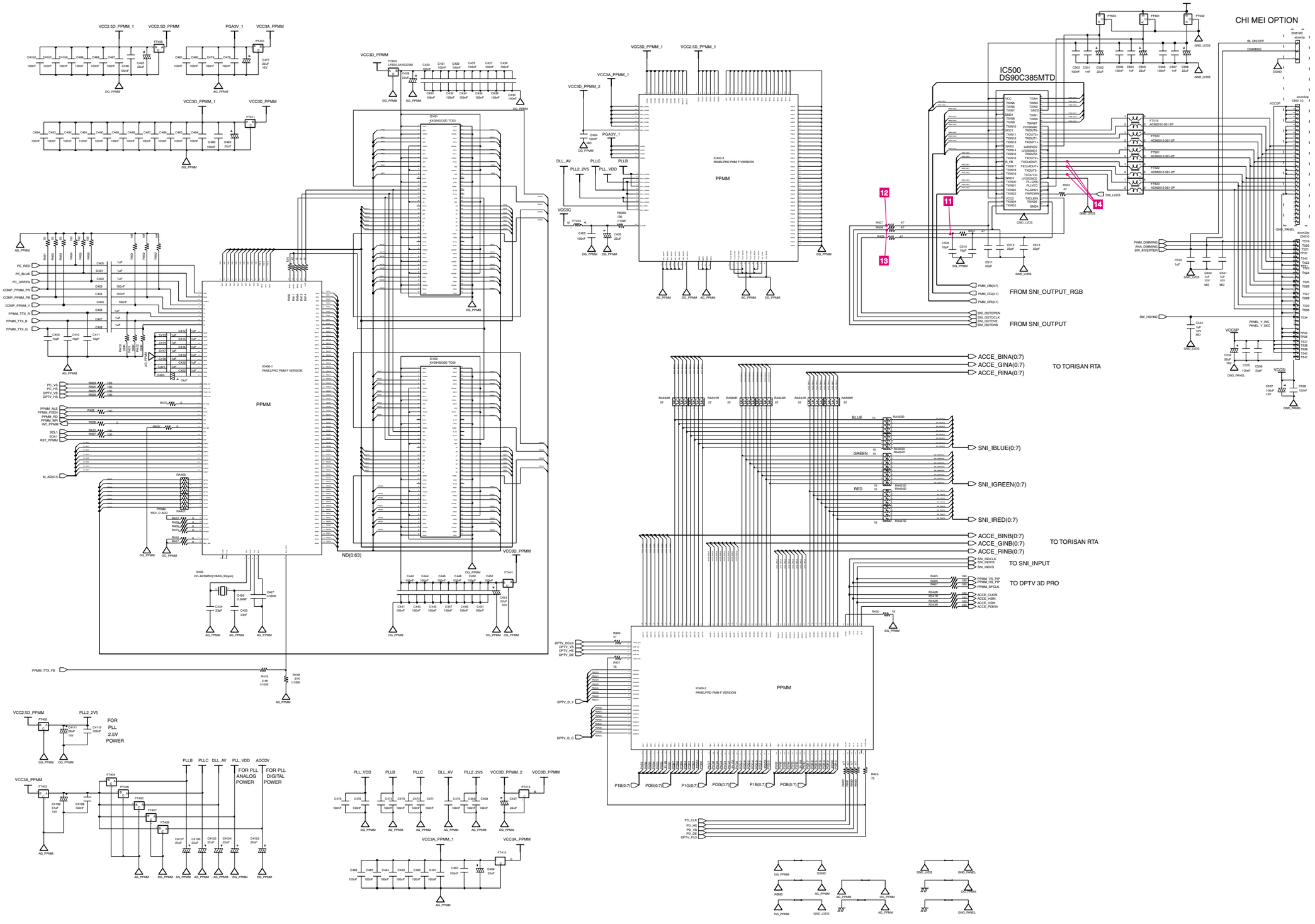
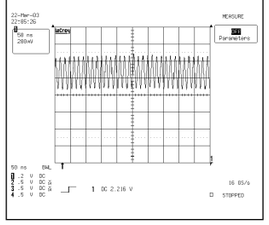
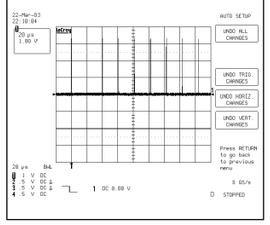
## PPMM (Sub Scaler) Block Schematic Diagram



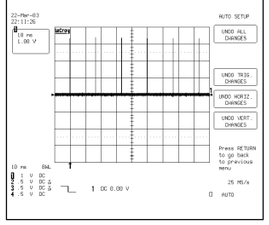
**11** IC500,#31 Clock Signal



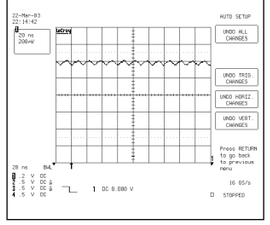

**12** IC500,#27 H-Sync




**13** IC500,#28 V-Sync




**14** IC500,#37,39,40 Clock Output Signal



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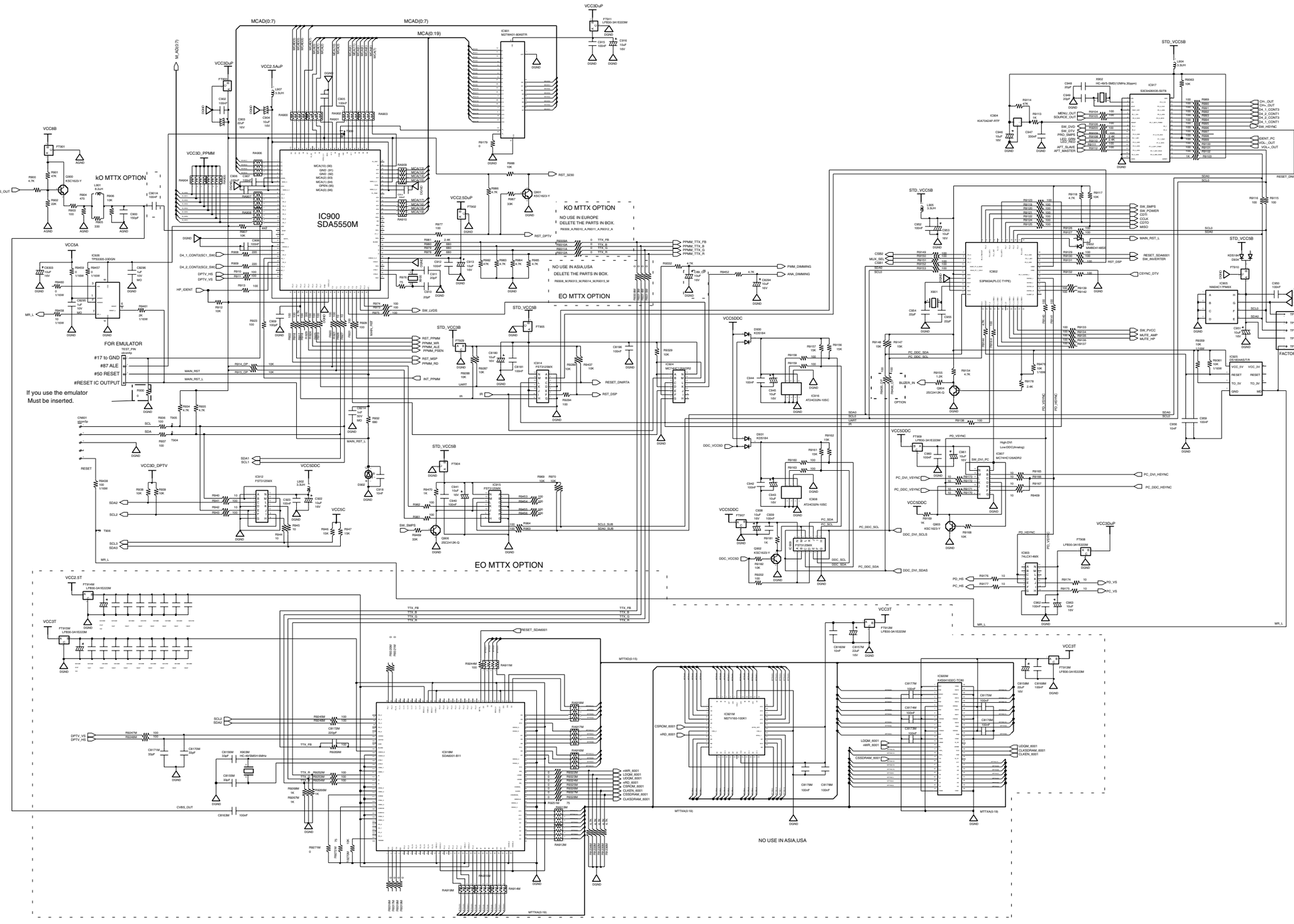
## MICIOM Block Schematic Diagram



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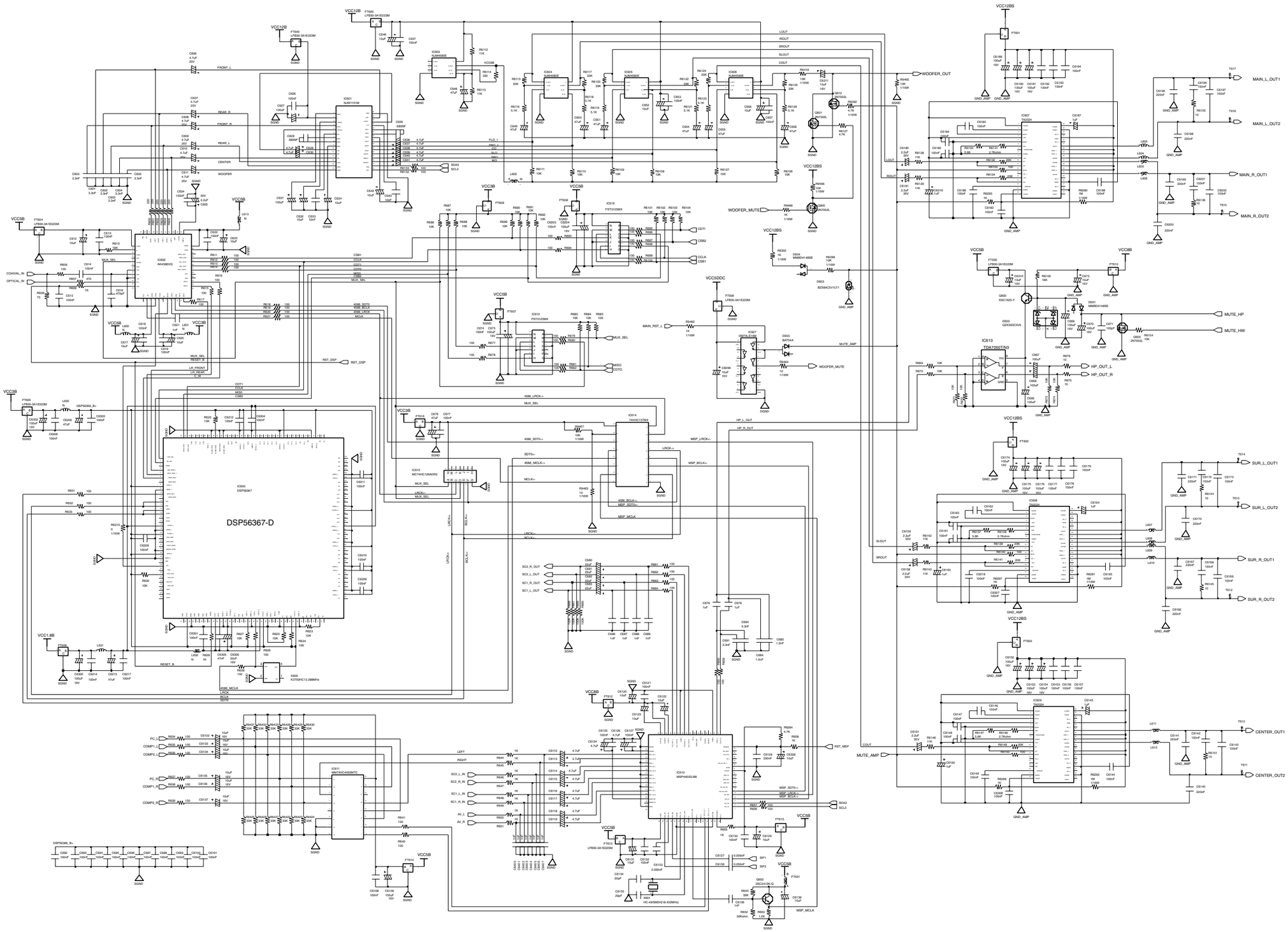
## Sound Block Schematic Diagram



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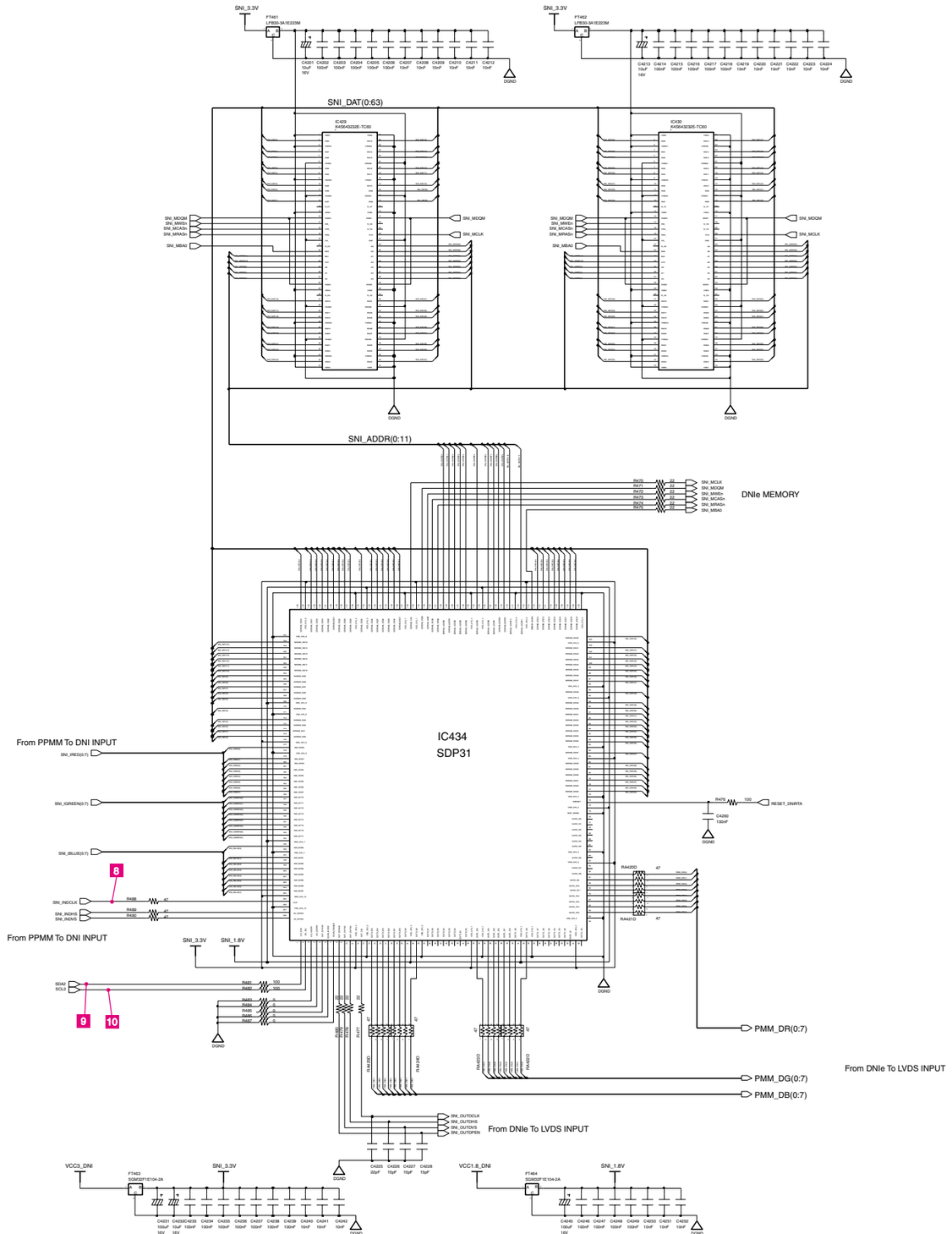
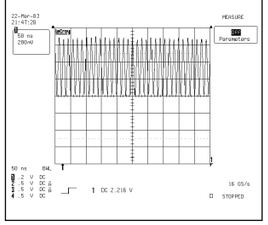
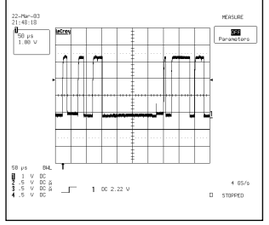
## DNIe Block Schematic Diagram



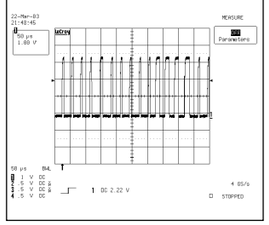
**8** IC434,#205 Clock Signal




**9** IC400,IC434 Communichion Data Signal




**10** IC400,IC434 Communichion Clock Signal



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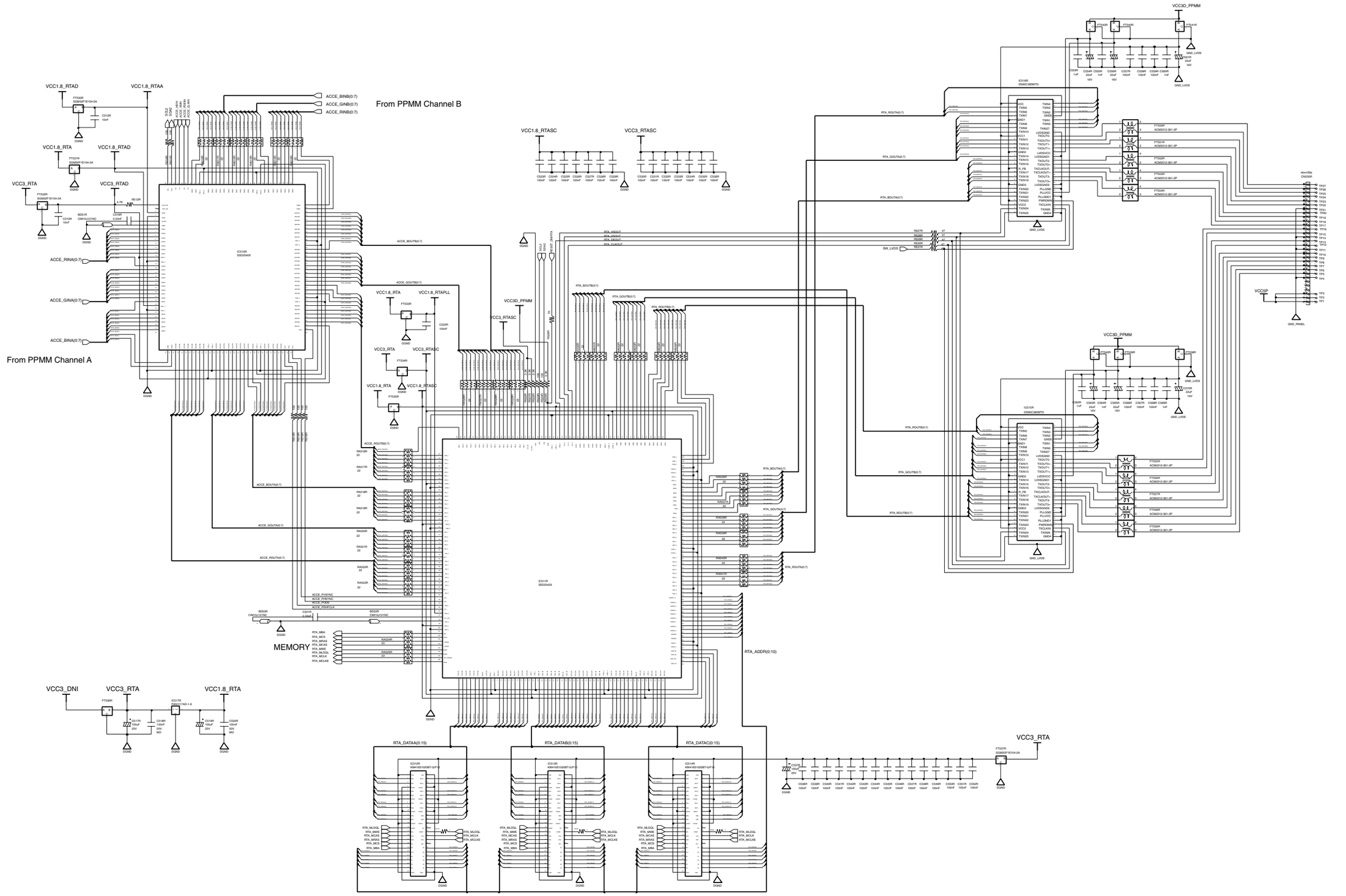
## RTA ACCE Option Block Schematic Diagram



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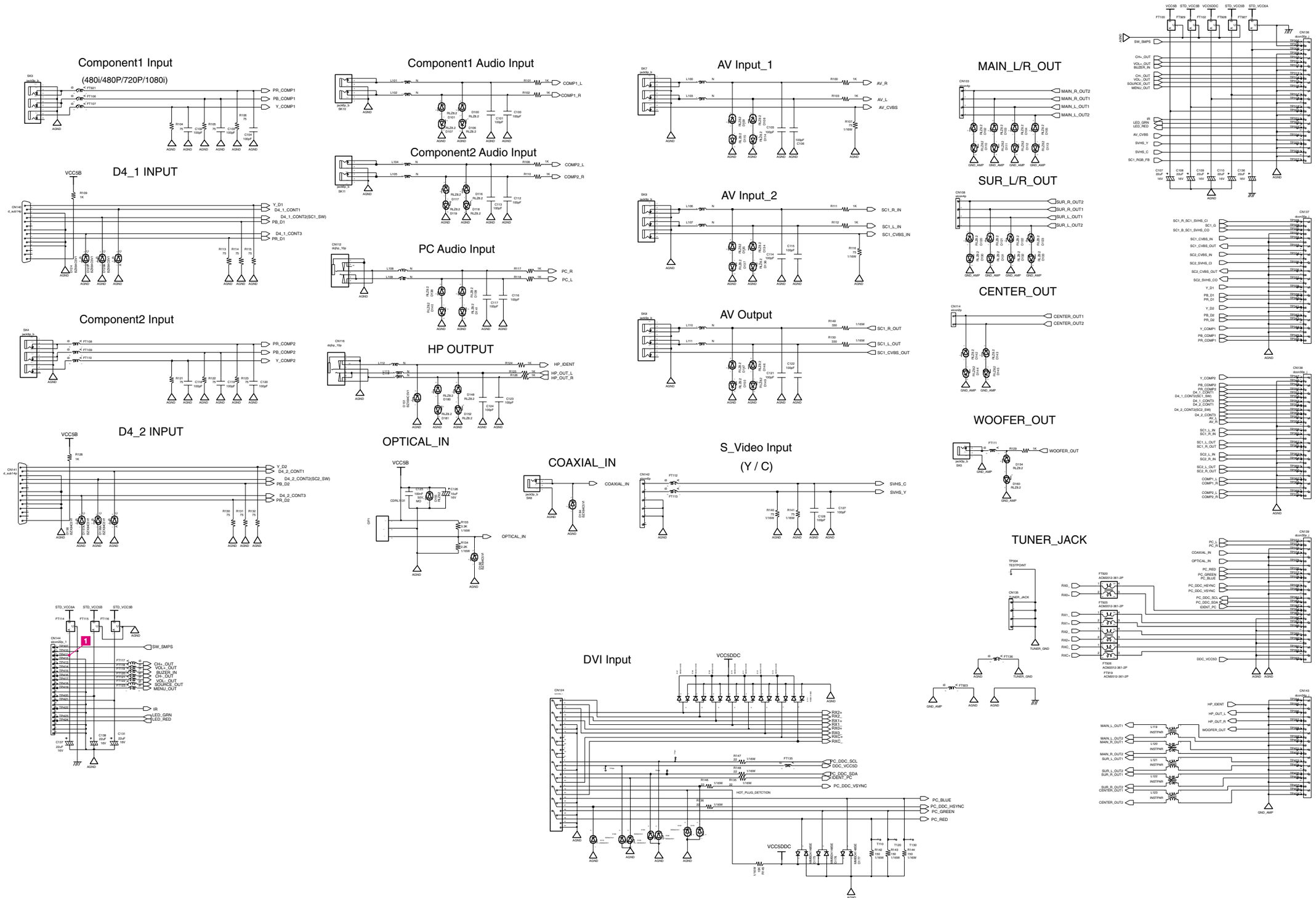
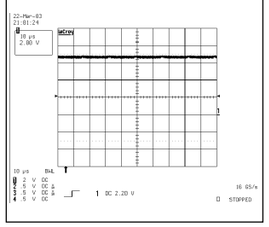
# Input Board Schematic Diagram



**1** DC 6V


22-Mar-03
21:01:24
10 µs
2.80 V
10 µs
BWL
2 V DC
5 V DC
5 V DC
5 V DC
1 DC 2.20 V
16 GS/s
STOPPED

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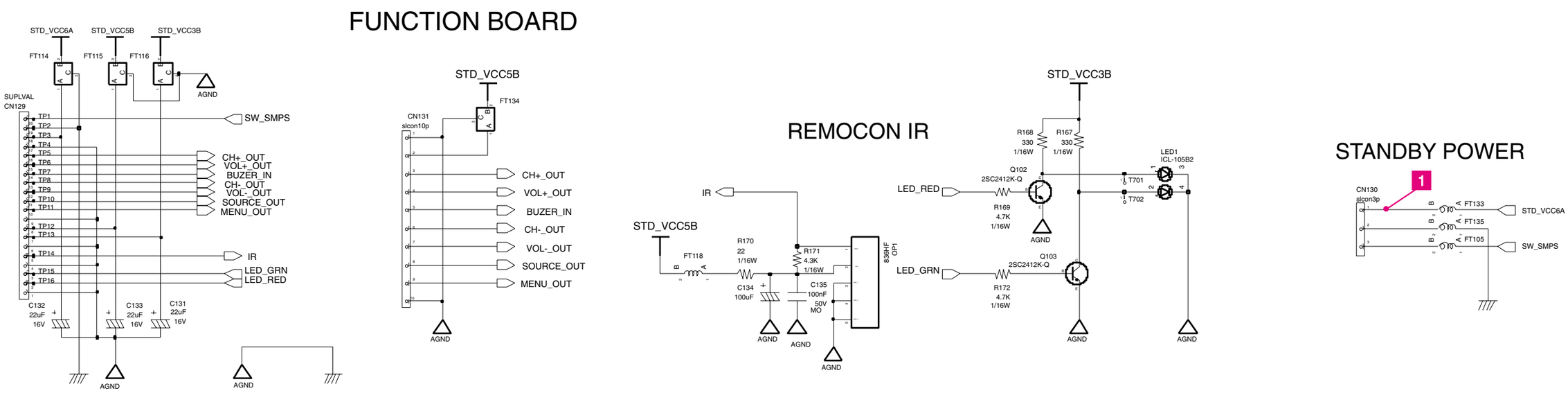
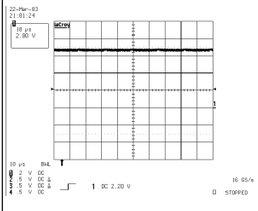
## Power Switch Schematic Diagram



**1** DC 6V


22-Mar-03
21:01:24
10 µs
2.80 V
10 µs
BWL
CH1 2 V DC
CH2 5 V DC
CH3 5 V DC
CH4 5 V DC
1 DC 2.20 V
16 GS/s
STOPPED

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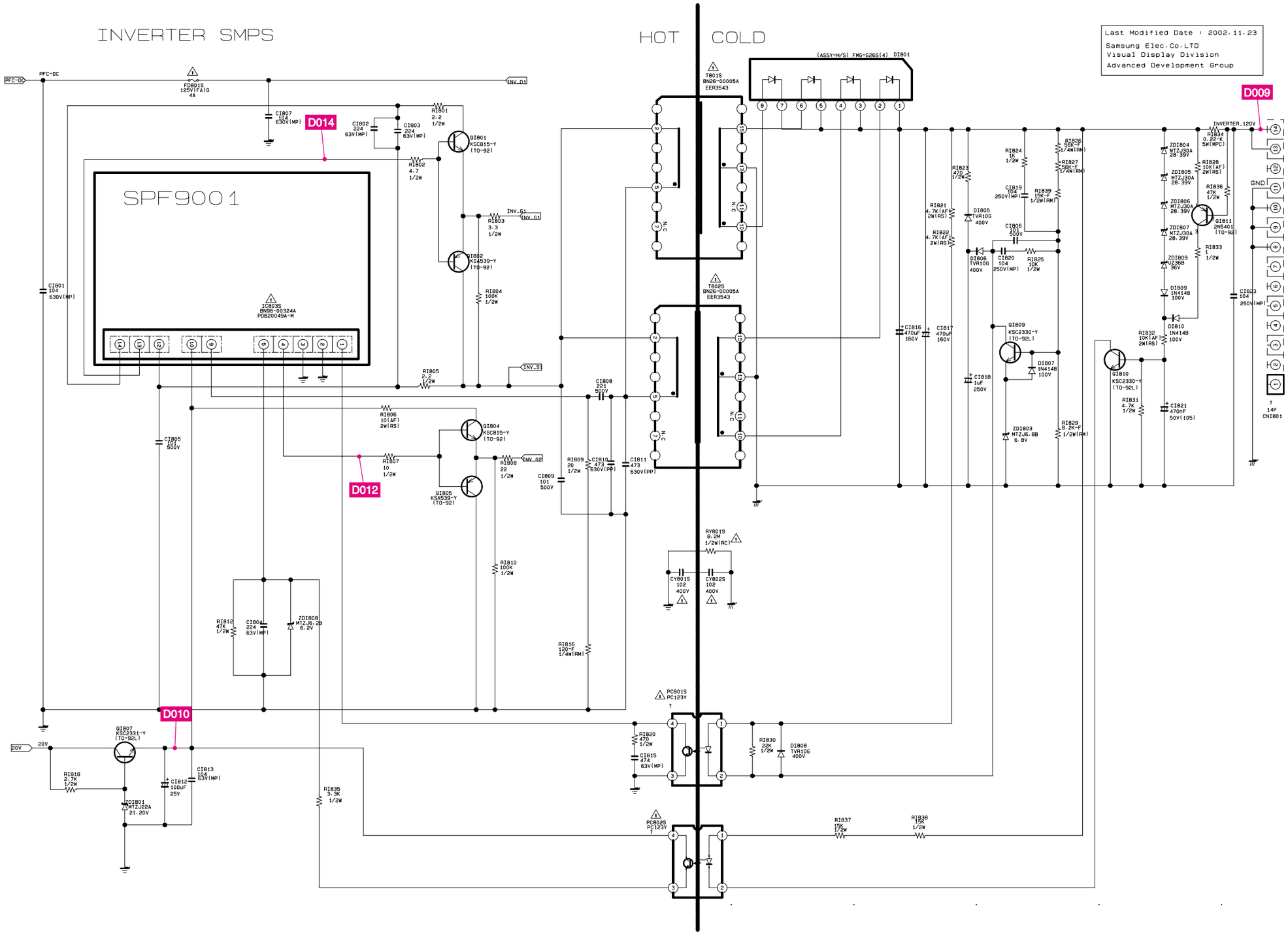
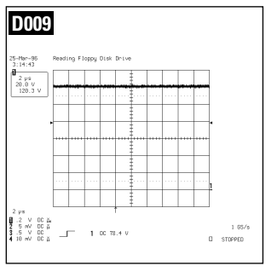
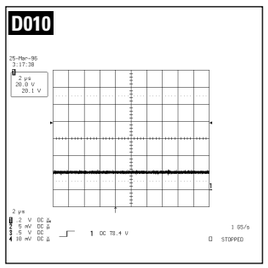
## Inverter Block Schematic Diagram



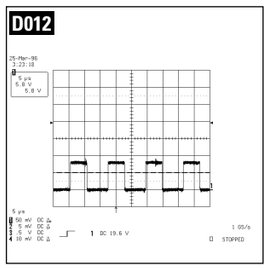
**D009**



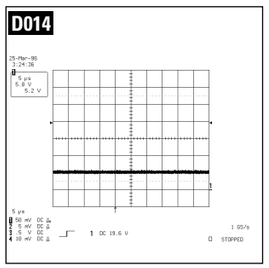

**D010**




**D012**




**D014**



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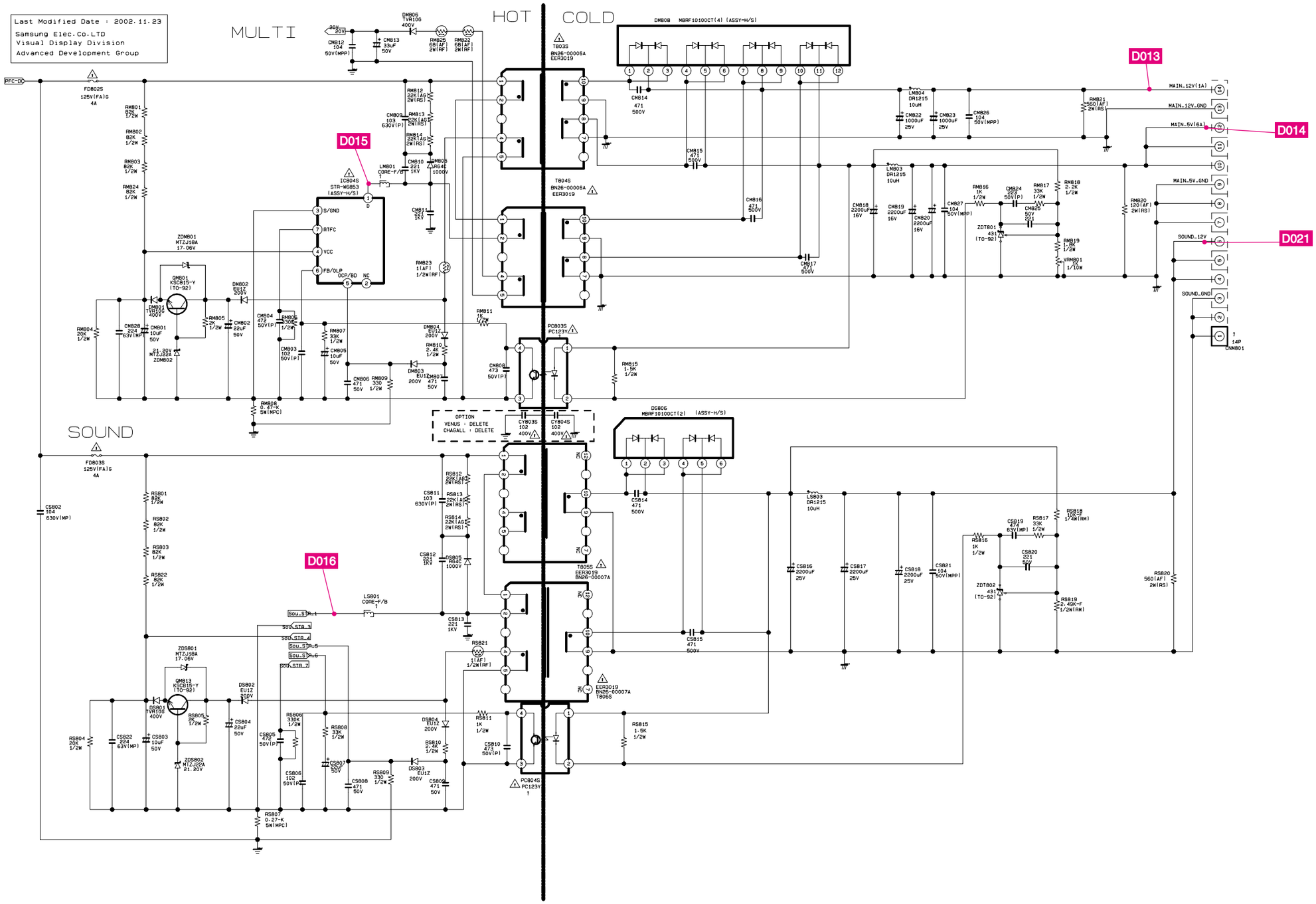
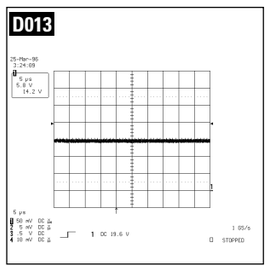
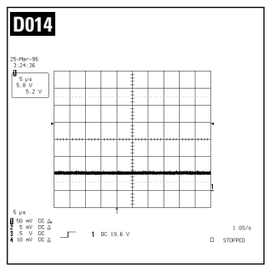
## Multi Block Schematic Diagram



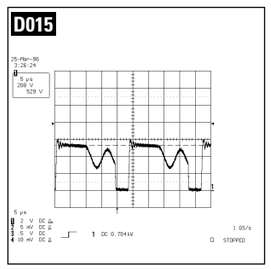
**D013**



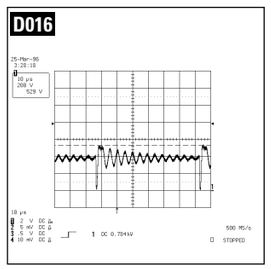
**D014**



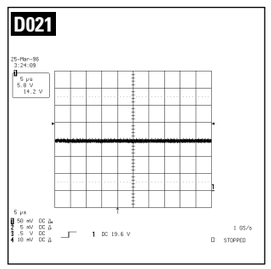
**D015**



**D016**



**D021**



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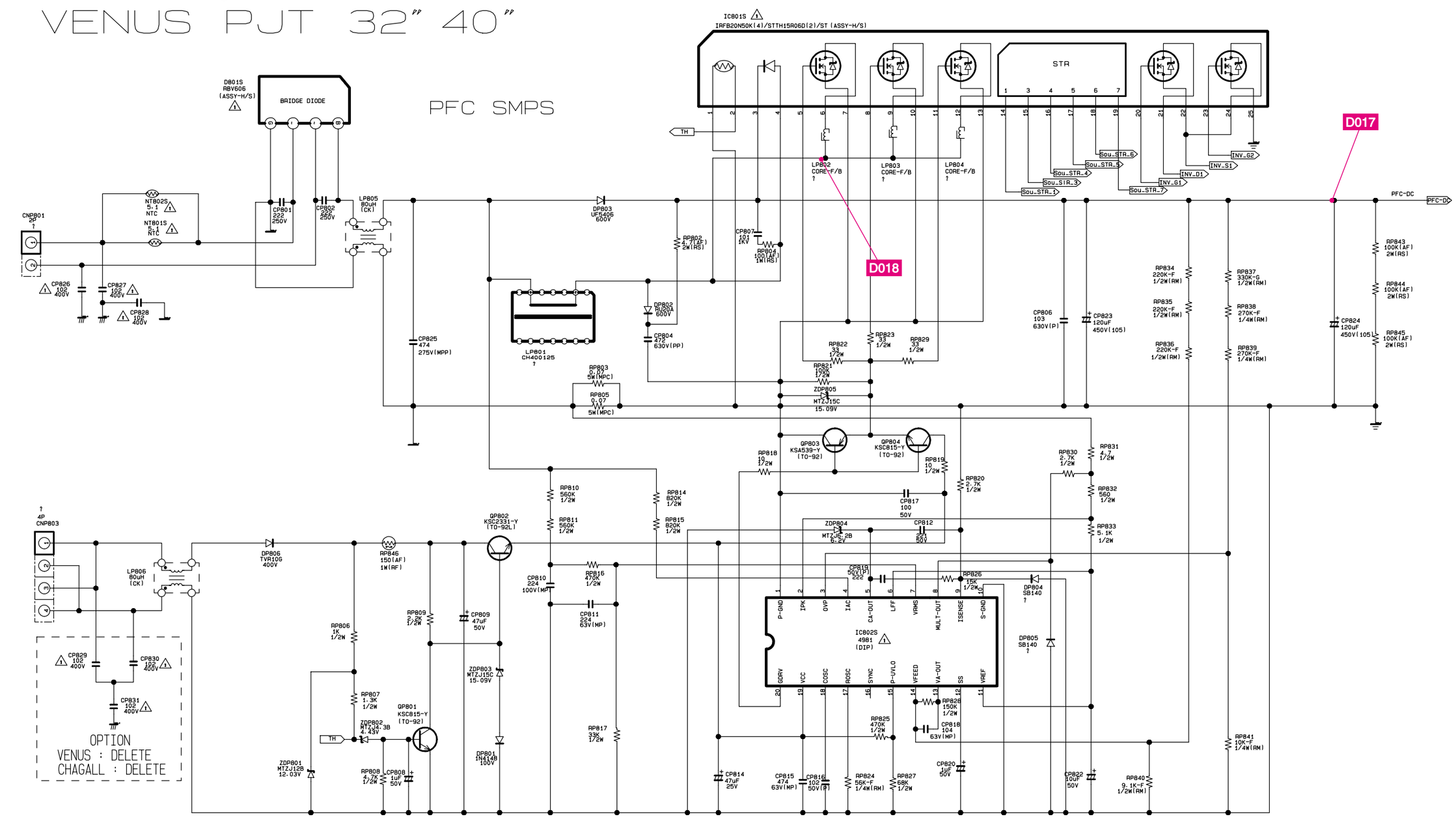
## PFC Block Schematic Diagram

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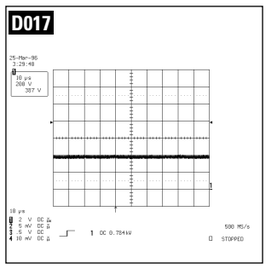
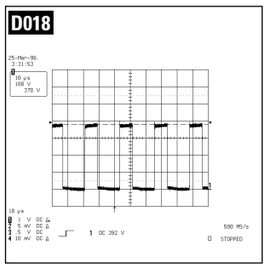
Visual Display Division
Advanced Development Group

**D017**


25-Mar-96
3:29:48
10 µs
200 V
387 V
10 µs
2 V DC
5 mV DC
5 V DC
10 mV DC
DC 0.784kV
500 MS/s
STOPPED

**D018**


25-Mar-96
3:31:53
10 µs
100 V
378 V
10 µs
1 V DC
5 mV DC
5 V DC
10 mV DC
DC 392 V
500 MS/s
STOPPED

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## SUB Block Schematic Diagram

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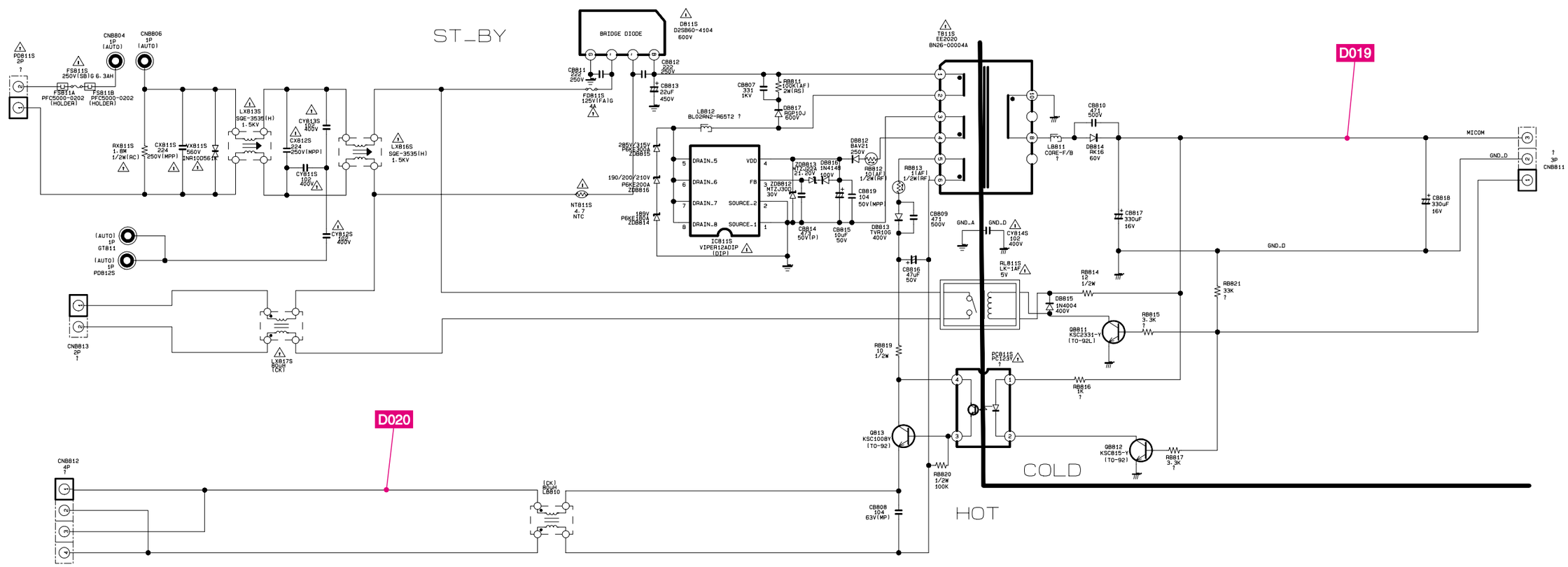
technical-document managing department is prohibited.

VENUS PJT 32" 40"



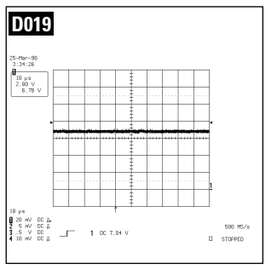

Last Modified Date 2003.02.04

Samsung Elec.Co.LTD

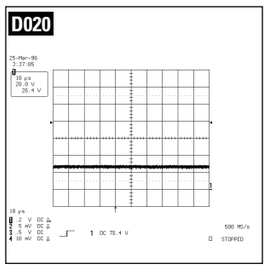
Visual Display Division

Advanced Development Group

**D019**


25-Mar-96
3:34:26
10 µs
2.80 V
8.78 V
10 µs
20 mV DC
5 mV DC
.5 V DC
10 mV DC
DC 7.84 V
500 MS/s
STOPPED

**D020**


25-Mar-96
3:37:05
10 µs
20.0 V
26.4 V
10 µs
2 V DC
5 mV DC
.5 V DC
10 mV DC
DC 78.4 V
500 MS/s
STOPPED