MODEL NAME : VAW00
PROJECT CODE : ANRVAW0000
PCB NO : LA-9104P (Thames XT)

DA60000VV00 LA-9104P M/B
DA40001FO00 LS-9101P POWER BUTTON/B
DA40001FP00 LS-9102P USB/B
DA40001FQ00 LS-9103P TP BUTTON/B

ZZZ R1@
PCB VAW00 LA-9104P LS-9101P/9102P/9103P
DAZ0SZ00200

ZZZ GCER3@
PCB VAW00 LA-9104P LS-9101P/9102P/9103P GOLD A31 !
DAZ0SZ00201

ZZZ TRIR3@
PCB VAW00 LA-9104P LS-9101P/9102P/9103P TRIPOD A31 !
DAZ0SZ00202

ZZZ HANNR3@
PCB VAW00 LA-9104P LS-9101P/9102P/9103P HANNSTARB A31 !
DAZ0SZ00203

ZZZ ZDTR3@
PCB VAW00 LA-9104P LS-9101P/9102P/9103P ZDT A31 !
DAZ0SZ00204

Dell / Compal Confidential

Schematic Document

Intel Chief River
Ivy Bridge(BGA) + Panther Point
OAK 15" UMA/DIS AMD Thames XT

2012-08-22

Rev: 1.0

46@ : for 46 level
@ : Nopop Component
CONN@ : Connector Component
KB9012@ : ENE KB9012 Implemented
UMA@ : Only for UMA
EMC@ : EMI/ESD parts

GCLK@ : Green CLK implemented
GCLKUMA@ : Green CLK for UMA
GCLKDIS@ : Green CLK for DIS
XTAL@ : X'tal implemented
XTALDIS@ : X'tal with DIS implemented

R1@ : R1 P/N
R3@ : R3 P/N

i3R1@ : CPU i3-3217 1.8G
i3VOSR1@ : CPU i3-2365 1.4G
i5R1@ : CPU i5-3317 1.7G
i7R1@ : CPU i7-3517 1.9G
CELR1@ : CPU Celeron 887 1.5G
PENR1@ : CPU Pentium 997 1.6G

DIS@ : Only for Discrete
TH@/THR1@ : Thames-XT
MS@/MSR1@ : Mars Pro
X76@ :
SPI-ROM & VRAM Group

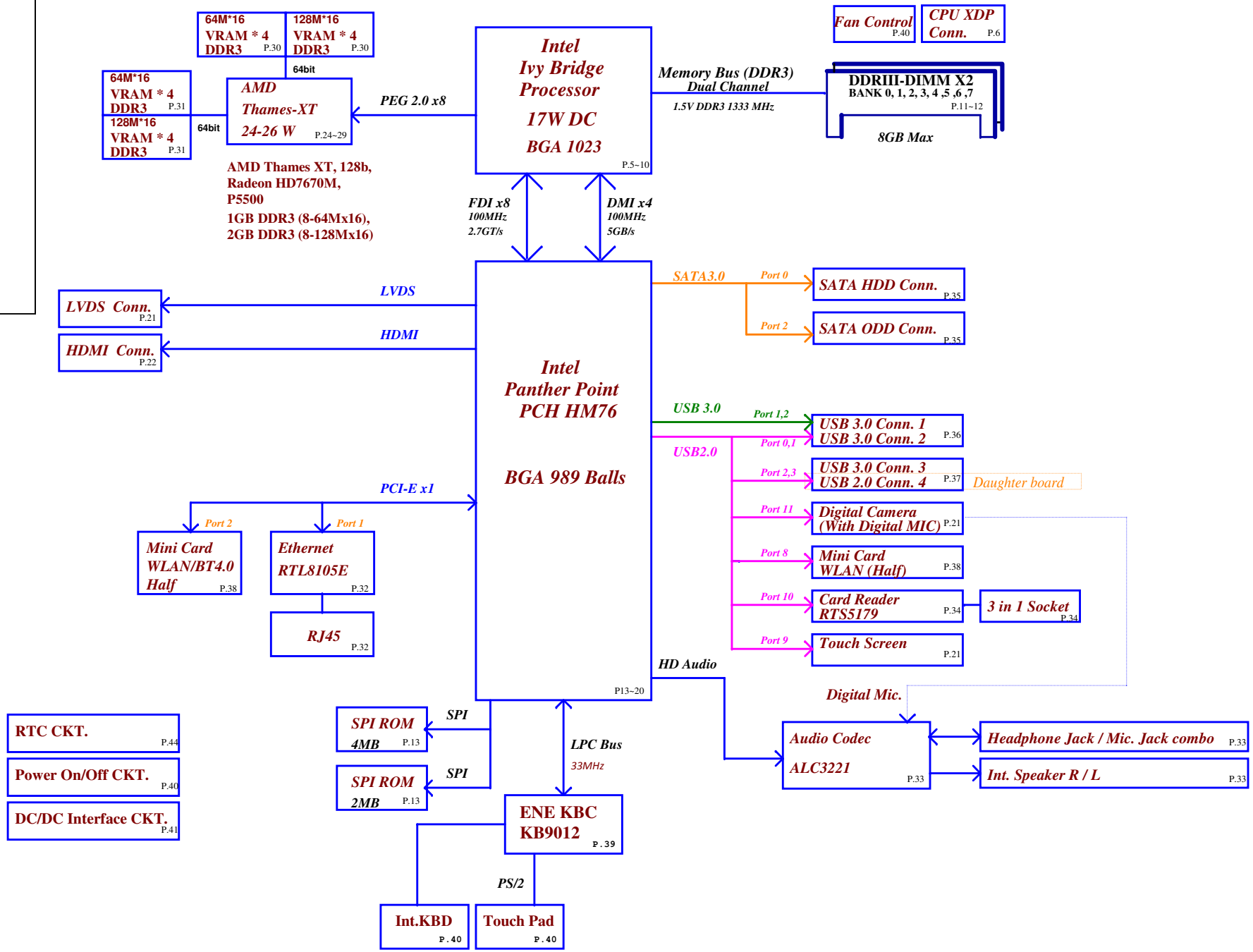
Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: Cover Page

Size: Custom | Document Number: LA-9104P | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 1 of 57

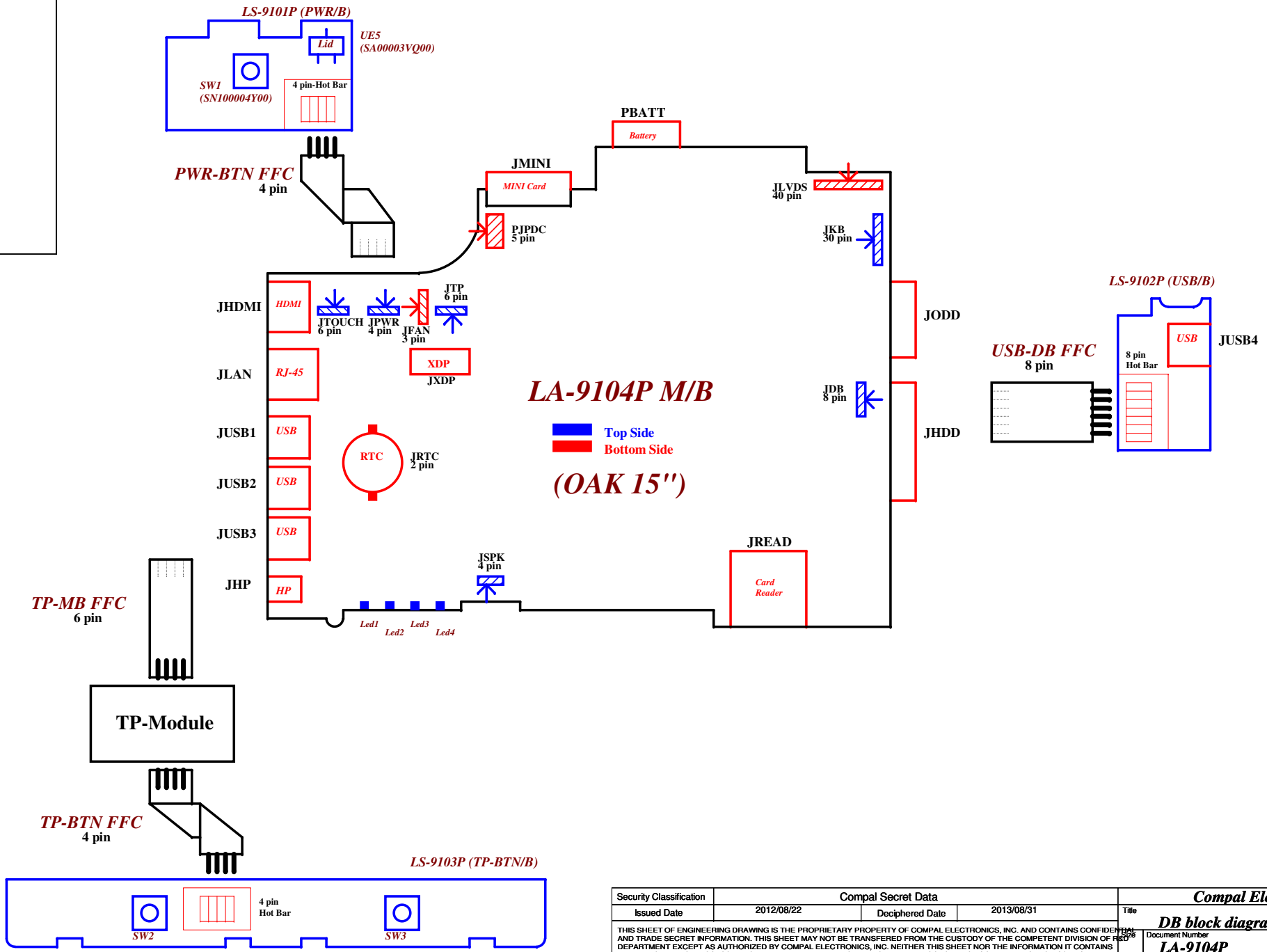


Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.			
Title	Block diagram		
Size	Document Number		Rev
	LA-9104P		1.0
Date:	Wednesday, August 29, 2012	Sheet	2 of 57

Compal Confidential

Project Code : VAW00
File Name : LA-9104P



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: **DB block diagram**

Size | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 3 of 57

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

ID	PCB Revision		
	UMA	THM	MARS
0	0.1		
1		0.1	0.1
2	0.2		
3		0.2	0.2
4	0.3		
5		0.3	0.3
6	1.0		
7		1.0	1.0

Project ID Table

ID	Project Revision
0	
1	
2	
3	
4	
5	UMA
6	DIS THAMES
7	DIS MARS PRO

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Express Card	Thermal Sensor	FFS	VGA Thermal Sensor	VGA	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V
EC_SMB_CK2 EC_SMB_DA2	KB9012								V	V		
PCH_SML0CLK PCH_SML0DATA	PCH											
PCH_SML1CLK PCH_SML1DATA	PCH											
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V	V		V			V	

Link

PCH	USB PORT#	DESTINATION
	0	USB conn.2
	1	USB conn.1
	2	USB conn.3
	3	USB conn.4 (DB)
	4	NC
	5	NC
	6	NC
	7	NC
	8	MINI CARD (WLAN)
	9	Touch Screen
	10	Card Reader
	11	Camera
	12	NC
	13	NC

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100 LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

Symbol Note :

: means Digital Ground

: means Analog Ground

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Issued Date	2012/08/22	Deciphered Date	2013/08/31

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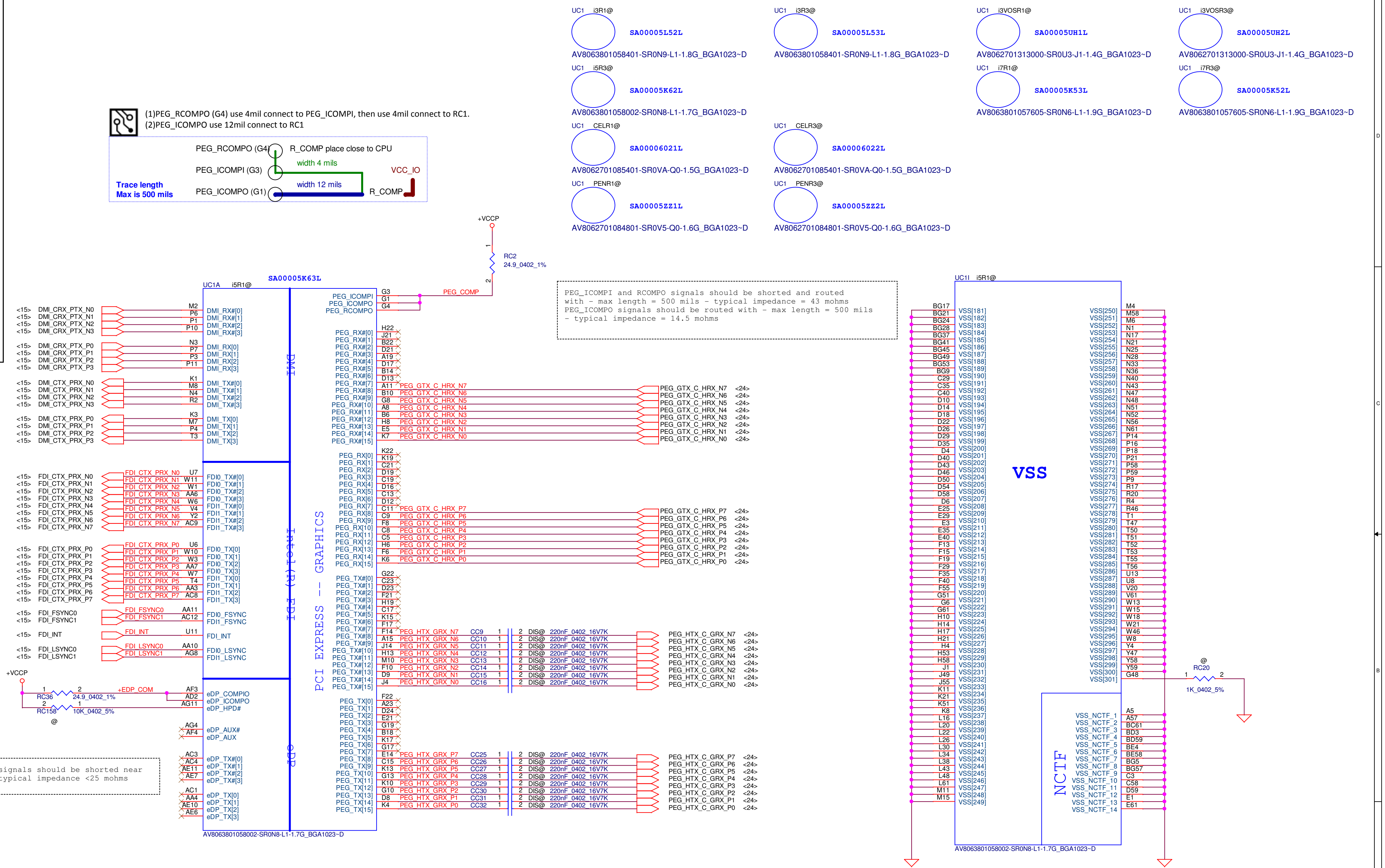
Title: Notes List

Size: B | Document Number: LA-9104P | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 4 of 57



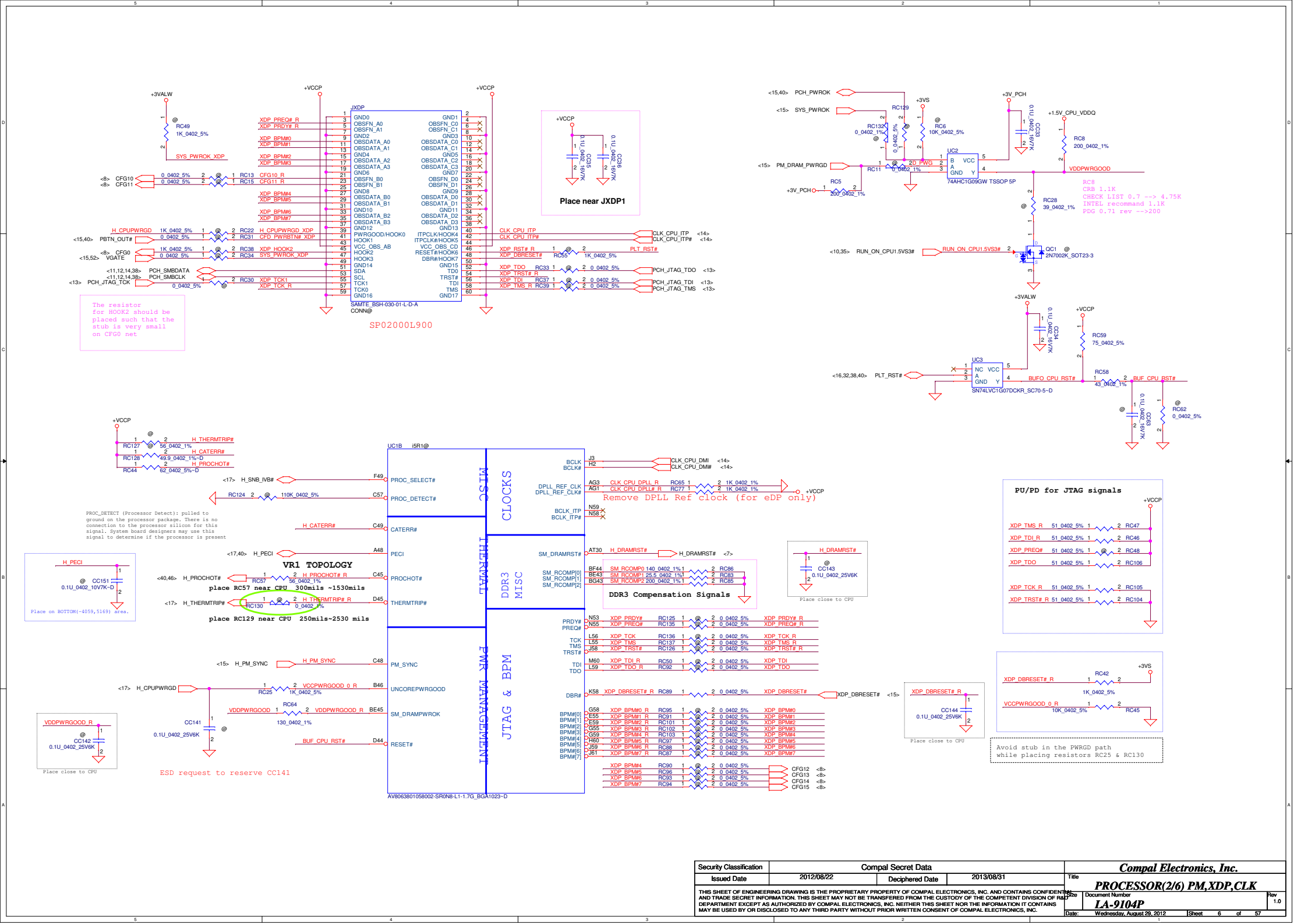
Security Classification	Compal Secret Data	
Issued Date	2012/08/22	Deciphered Date 2013/08/31

Compal Electronics, Inc.

Title: **PROCESSOR(1/6) DMI,FDI,PEG**

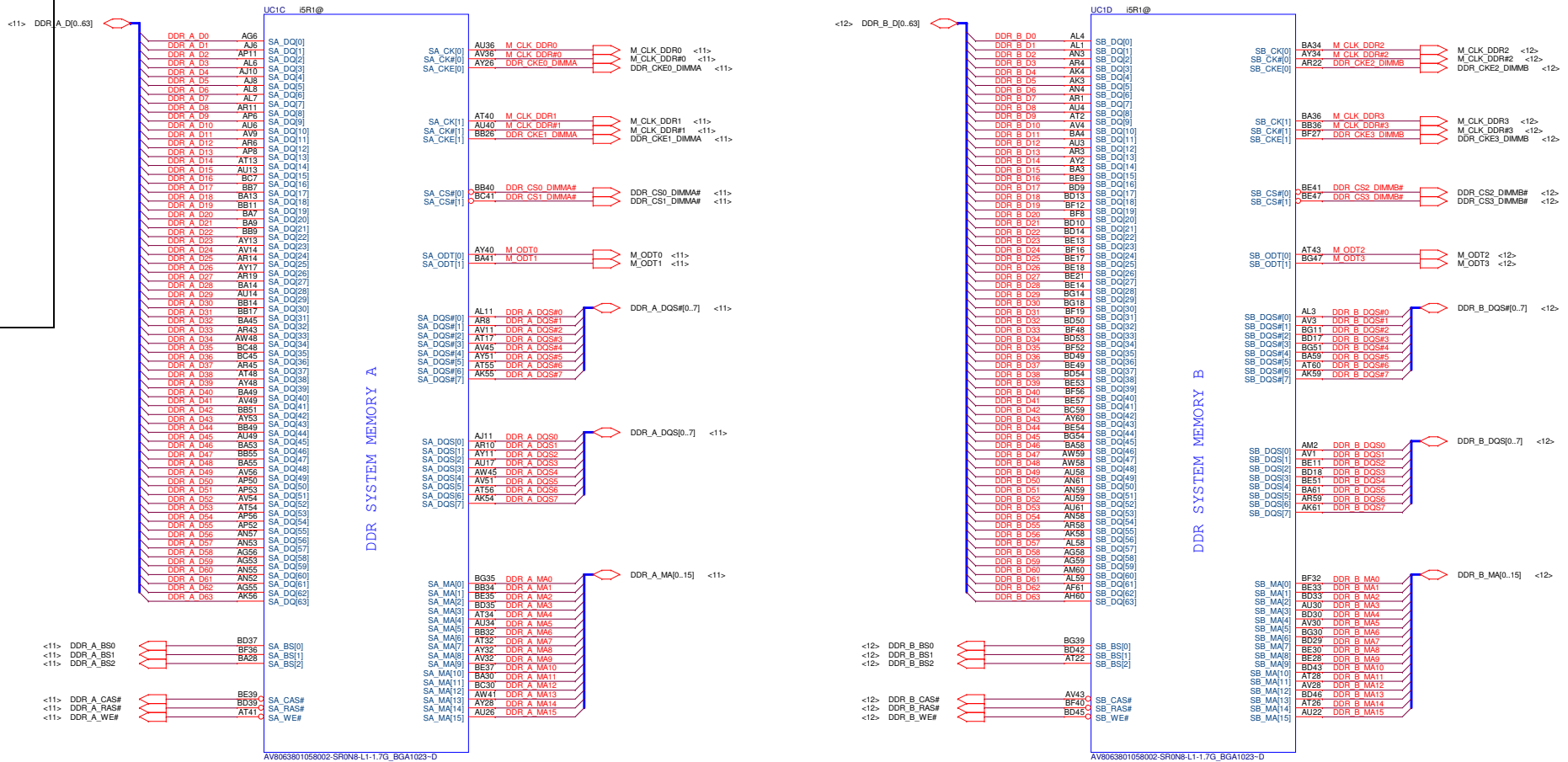
Size | Document Number: **LA-9104P** | Rev 1.0

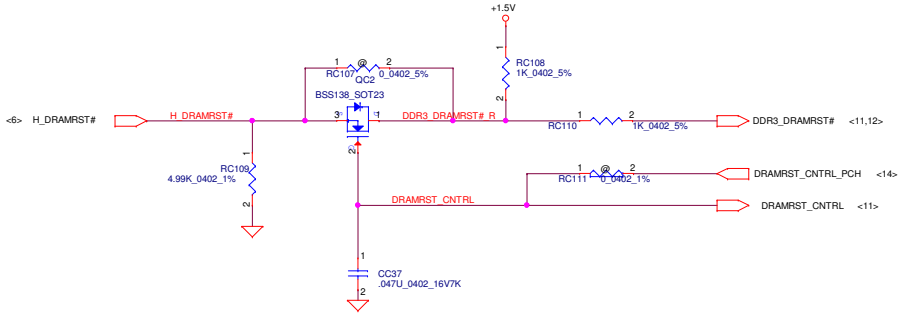
Date: Wednesday, August 29, 2012 | Sheet 5 of 57

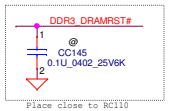


Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.			
Title: PROCESSOR(2/6) PM,XDP,CLK			
Size	Document Number: LA-9104P		Rev: 1.0
Date: Wednesday, August 29, 2012	Sheet 6 of 57		



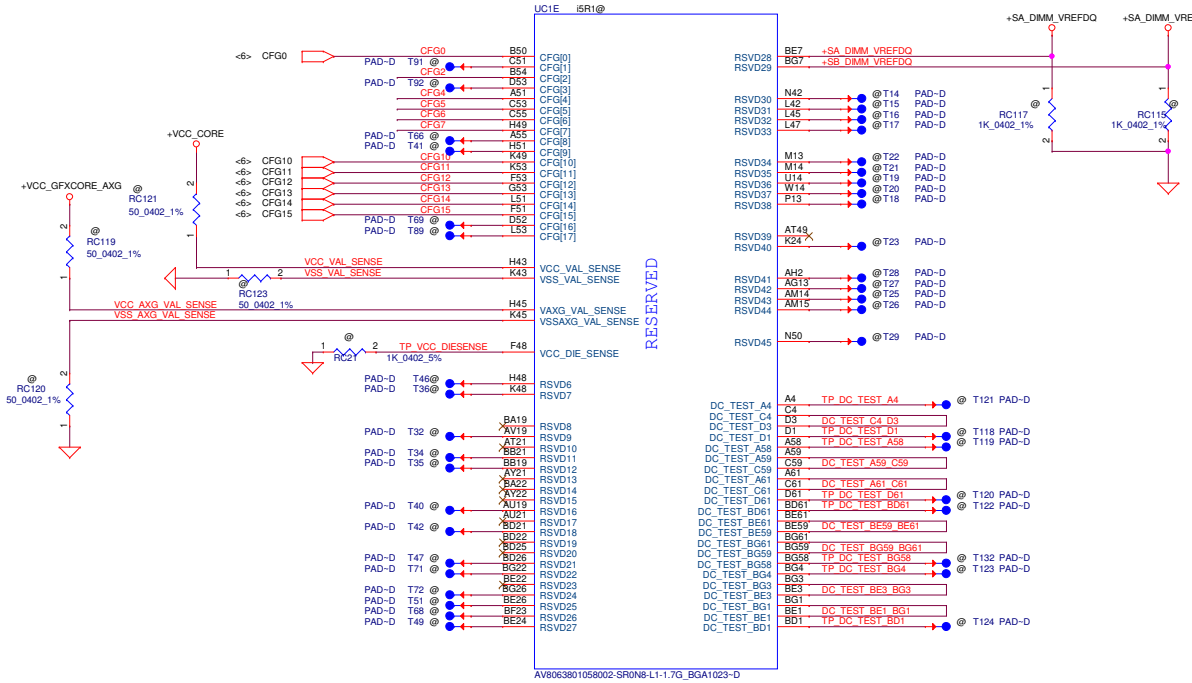


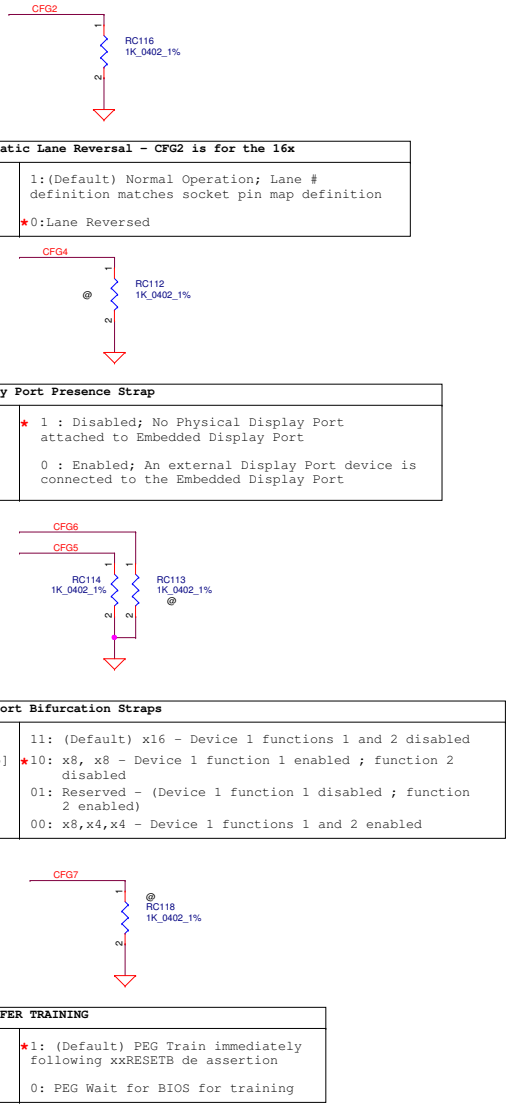


Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.			
Title: PROCESSOR(3/6) DDRIII			
Size	Document Number: LA-9104P		Rev: 1.0
Date: Wednesday, August 29, 2012	Sheet 7 of 57		

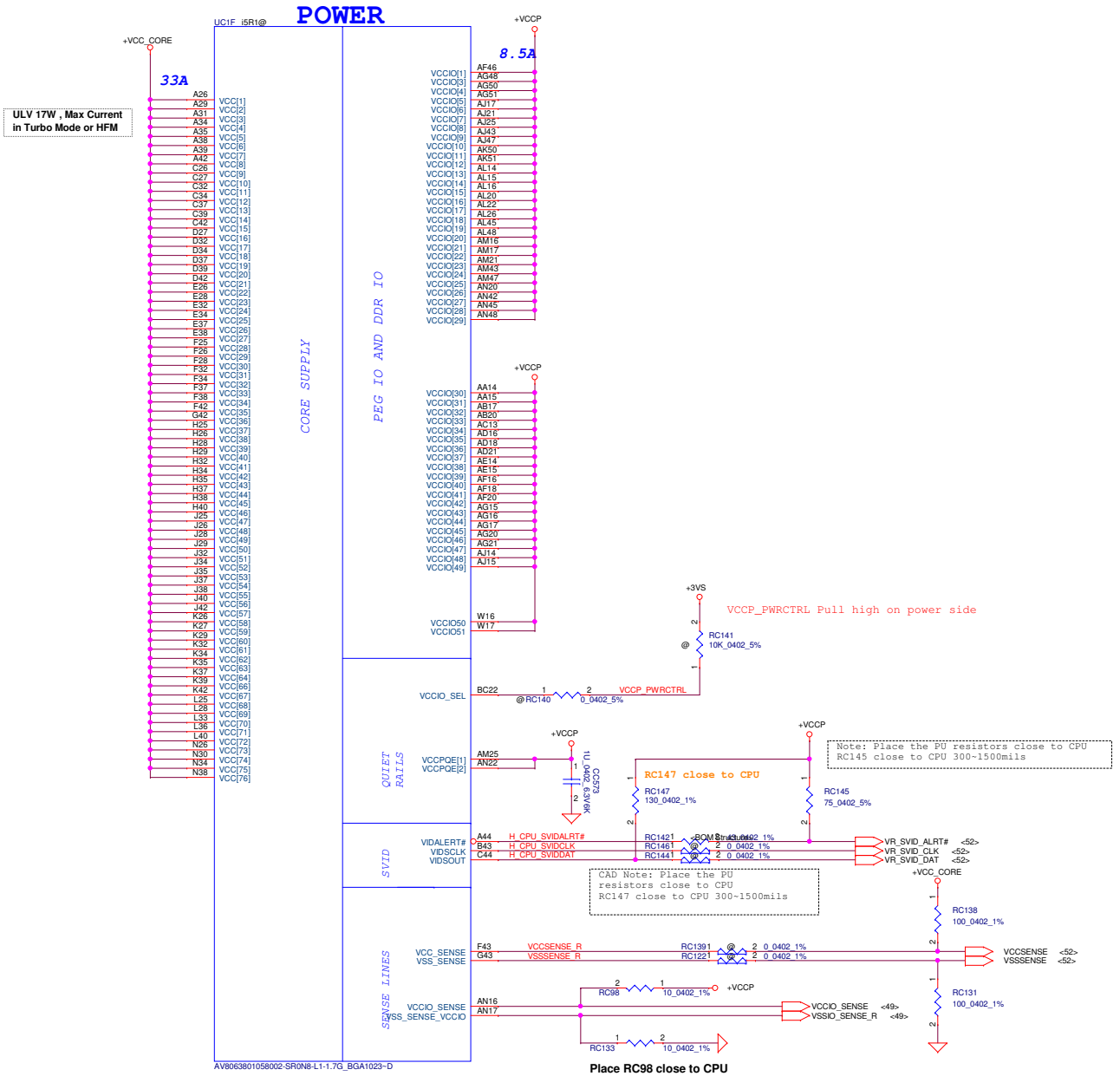
CFG Straps for Processor





Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.			
Title: PROCESSOR(4/6) RSVD,CFG			
Size	Document Number: LA-9104P		Rev: 1.0
Date: Wednesday, August 29, 2012	Sheet 8 of 57		



Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65~1.3	53
VCCIO	1.05/1	8.5
VAXG	0.0~1.1	33
VCCPLL	1.8	1.2
VDDQ	1.5	5
VCCSA	0.65~0.9	6
+1.5V_MEM	1.5	12~16 ★

★ Description

5A to Mem controller(+1.5V_CPU_VDDQ)
5~6A to 2 DIMMs/channel
2~5A to +1.5V_RUN & +0.75V_DDR_VTT

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.	
Title	PROCESSOR(5/6) PWR,BYPASS
Size	Document Number: LA-9104P
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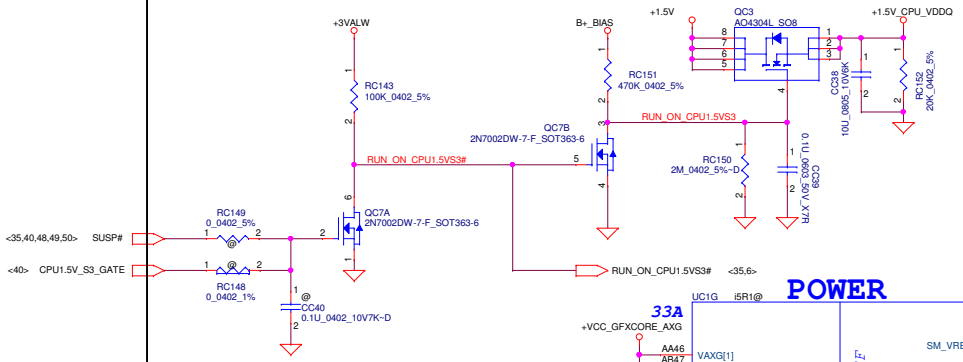
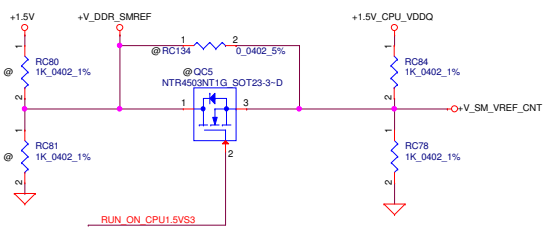
+1.5V_CPU_VDDQ Source





POWER

UC1G i5R1@

33A

+VCC_GFXCORE_AXG

AA46 AB47 AB50 AB51 AB52 AB53 AB55 AB56 AB58 AB59 AC61 AD47 AD48 AD50 AD51 AD52 AD53 AD55 AD56 AD58 AD59 AE46 N45 P47 P48 P50 P51 P52 P53 P55 P56 P61 T48 T58 T59 T61 U46 V47 V48 V50 V51 V52 V53 V55 V56 V58 V59 W50 W51 W52 W53 W55 W56 W61 Y48 Y61

VAXG[1] VAXG[2] VAXG[3] VAXG[4] VAXG[5] VAXG[6] VAXG[7] VAXG[8] VAXG[9] VAXG[10] VAXG[11] VAXG[12] VAXG[13] VAXG[14] VAXG[15] VAXG[16] VAXG[17] VAXG[18] VAXG[19] VAXG[20] VAXG[21] VAXG[22] VAXG[23] VAXG[24] VAXG[25] VAXG[26] VAXG[27] VAXG[28] VAXG[29] VAXG[30] VAXG[31] VAXG[32] VAXG[33] VAXG[34] VAXG[35] VAXG[36] VAXG[37] VAXG[38] VAXG[39] VAXG[40] VAXG[41] VAXG[42] VAXG[43] VAXG[44] VAXG[45] VAXG[46] VAXG[47] VAXG[48] VAXG[49] VAXG[50] VAXG[51] VAXG[52] VAXG[53] VAXG[54] VAXG[55] VAXG[56]

GRAPHICS

VREF

SM_VREF AY43

+V_SM_VREF_CNT

+V_SM_VREF should have 10 mil trace width

DDR3 - 1.5V RAILS

5A

+1.5V_CPU_VDDQ

VDDQ[1] VDDQ[2] VDDQ[3] VDDQ[4] VDDQ[5] VDDQ[6] VDDQ[7] VDDQ[8] VDDQ[9] VDDQ[10] VDDQ[11] VDDQ[12] VDDQ[13] VDDQ[14] VDDQ[15] VDDQ[16] VDDQ[17] VDDQ[18] VDDQ[19] VDDQ[20] VDDQ[21] VDDQ[22] VDDQ[23] VDDQ[24] VDDQ[25] VDDQ[26]

AJ28 AJ33 AJ36 AJ40 AL30 AL34 AL38 AL42 AM33 AM36 AM40 AN30 AN34 AN38 AR26 AR28 AR30 AR32 AR34 AR36 AR40 AV41 AW26 BA40 BB28 BG33

CC178 CC179 CC149 CC150 0.1U_0402_10V7K-D

6A +1.5V

10U_0603_6.3V6M CC181 CC180 CC161 CC162 CC163 CC164 CC165 CC166

330U_D2_2VM_R6M-D CC167

10U_0402_6.3V6K CC250 CC251 CC252 CC253 CC254 CC255 CC256 CC257 CC258 CC259

QUIET RAILS

+1.5V_CPU_VDDQ

VCCDQ[1] VCCDQ[2]

AM28 AN26

10U_0402_6.3V6K CC274

SENSE LINES

+VCC_GFXCORE_AXG

RC99 100_0402_1%

RC76 100_0402_1%

RC100 100_0402_1%

<52> VCC_AXG_SENSE

<52> VSS_AXG_SENSE

F45 G45

VAXG_SENSE VSSAXG_SENSE

1.2A

+1.8VS

330U_D2_2.5VM_R6M-D CC176

10U_0402_6.3V6K CC174

10U_0402_6.3V6K CC175

BB3 BC1 BC4

VCCPLL[1] VCCPLL[2] VCCPLL[3]

1.8V RAIL

VDDQ_SENSE BC43

VSS_SENSE_VDDQ BA43

SENSE LINES

VCCSA_SENSE U10 VCCSA_SENSE <51>

+VCCSA

330U_D2_2VM_R6M-D CC172

10U_0603_6.3V6M CC171 CC170 CC169 CC168 CC183 CC184

10U_0402_6.3V6K CC263 CC262 CC261 CC260

6A

L17 N16 N20 N22 P17 P20 R16 R18 R21 U15 V16 V17 V18 V21 W20

VCCSA[1] VCCSA[2] VCCSA[3] VCCSA[4] VCCSA[5] VCCSA[6] VCCSA[7] VCCSA[8] VCCSA[9] VCCSA[10] VCCSA[11] VCCSA[12] VCCSA[13] VCCSA[14] VCCSA[15] VCCSA[16]

SA RAIL

VCCSA VID lines

D48 D49

VCCSA_VID[0] VCCSA_VID[1]

VCCSA_VID0 <51>

VCCSA_VID1 <51>

AV8063801058002-SR0N8-L1-1.7G_BGA1023-D

UC1H i5R1@

VSS

A13 A17 A21 A25 A28 A33 A37 A40 A45 A49 A53 AA1 AA13 AA50 AA51 AA52 AA53 AA55 AA8 AB16 AB18 AB21 AB48 AB61 AC10 AC17 AC46 AC6 AD17 AD20 AD4 AD61 AE13 AE8 AF1 AF17 AF21 AF47 AF48 AF50 AF51 AF52 AF53 AF55 AF56 AF58 AF59 AG10 AG14 AG18 AG47 AG52 AG61 AG7 AH14 AH58 AJ13 AJ16 AJ20 AJ22 AJ26 AJ30 AJ34 AJ38 AJ42 AJ45 AJ48 AJ7 AK1 AK52 AL10 AL13 AL17 AL21 AL25 AL28 AL33 AL36 AL40 AL43 AL47 AL61 AM18 AM20 AM22 AM26 AM30 AM34

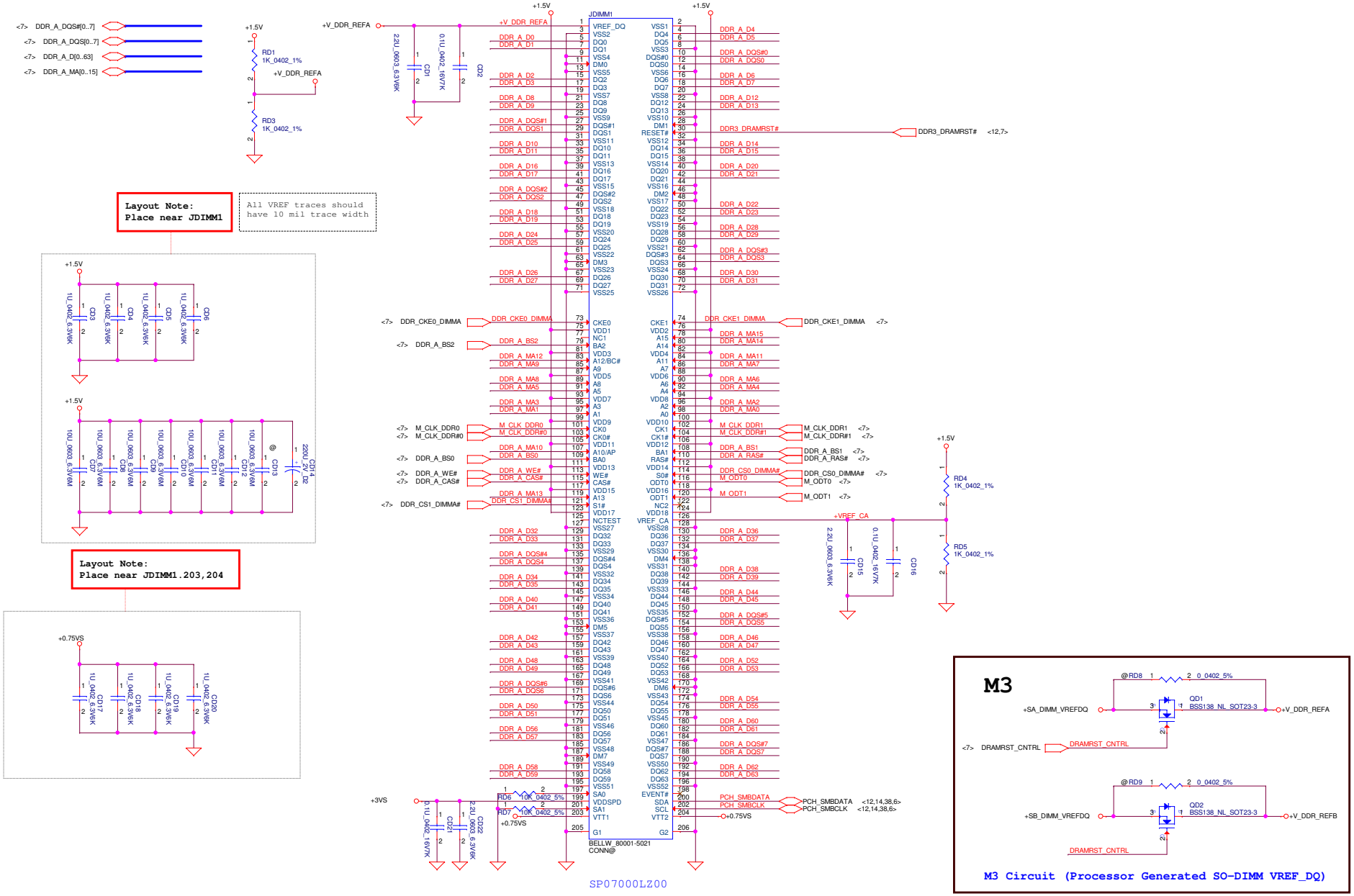
VSS[1] VSS[2] VSS[3] VSS[4] VSS[5] VSS[6] VSS[7] VSS[8] VSS[9] VSS[10] VSS[11] VSS[12] VSS[13] VSS[14] VSS[15] VSS[16] VSS[17] VSS[18] VSS[19] VSS[20] VSS[21] VSS[22] VSS[23] VSS[24] VSS[25] VSS[26] VSS[27] VSS[28] VSS[29] VSS[30] VSS[31] VSS[32] VSS[33] VSS[34] VSS[35] VSS[36] VSS[37] VSS[38] VSS[39] VSS[40] VSS[41] VSS[42] VSS[43] VSS[44] VSS[45] VSS[46] VSS[47] VSS[48] VSS[49] VSS[50] VSS[51] VSS[52] VSS[53] VSS[54] VSS[55] VSS[56] VSS[57] VSS[58] VSS[59] VSS[60] VSS[61] VSS[62] VSS[63] VSS[64] VSS[65] VSS[66] VSS[67] VSS[68] VSS[69] VSS[70] VSS[71] VSS[72] VSS[73] VSS[74] VSS[75] VSS[76] VSS[77] VSS[78] VSS[79] VSS[80] VSS[81] VSS[82] VSS[83] VSS[84] VSS[85] VSS[86] VSS[87] VSS[88] VSS[89] VSS[90]

VSS[91] VSS[92] VSS[93] VSS[94] VSS[95] VSS[96] VSS[97] VSS[98] VSS[99] VSS[100] VSS[101] VSS[102] VSS[103] VSS[104] VSS[105] VSS[106] VSS[107] VSS[108] VSS[109] VSS[110] VSS[111] VSS[112] VSS[113] VSS[114] VSS[115] VSS[116] VSS[117] VSS[118] VSS[119] VSS[120] VSS[121] VSS[122] VSS[123] VSS[124] VSS[125] VSS[126] VSS[127] VSS[128] VSS[129] VSS[130] VSS[131] VSS[132] VSS[133] VSS[134] VSS[135] VSS[136] VSS[137] VSS[138] VSS[139] VSS[140] VSS[141] VSS[142] VSS[143] VSS[144] VSS[145] VSS[146] VSS[147] VSS[148] VSS[149] VSS[150] VSS[151] VSS[152] VSS[153] VSS[154] VSS[155] VSS[156] VSS[157] VSS[158] VSS[159] VSS[160] VSS[161] VSS[162] VSS[163] VSS[164] VSS[165] VSS[166] VSS[167] VSS[168] VSS[169] VSS[170] VSS[171] VSS[172] VSS[173] VSS[174] VSS[175] VSS[176] VSS[177] VSS[178] VSS[179] VSS[180]

AM38 AM4 AM42 AM45 AM48 AM58 AN1 AN21 AN25 AN28 AN33 AN36 AN40 AN43 AN47 AN50 AN54 AP10 AP51 AP55 AP7 AR13 AR17 AR21 AR41 AR48 AR61 AR7 AT14 AT19 AT36 AT4 AT45 AT52 AT58 AU1 AU11 AU28 AU32 AU51 AU7 AV17 AV21 AV22 AV34 AV40 AV48 AV55 AW13 AW43 AW61 AW7 AY14 AY19 AY30 AY36 AY4 AY41 AY45 AY49 AY55 AY58 AY9 BA1 BA11 BA17 BA21 BA26 BA32 BA48 BA51 BB53 BC13 BC5 BC57 BD12 BD16 BD19 BD23 BD27 BD32 BD36 BD40 BD44 BD48 BD52 BD56 BD8 BE5 BG13

AV8063801058002-SR0N8-L1-1.7G_BGA1023-D

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title: PROCESSOR(6/6) PWR,VSS
Size	Document Number: LA-9104P			Rev: 1.0
Date: Wednesday, August 29, 2012	Sheet 10 of 57			



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

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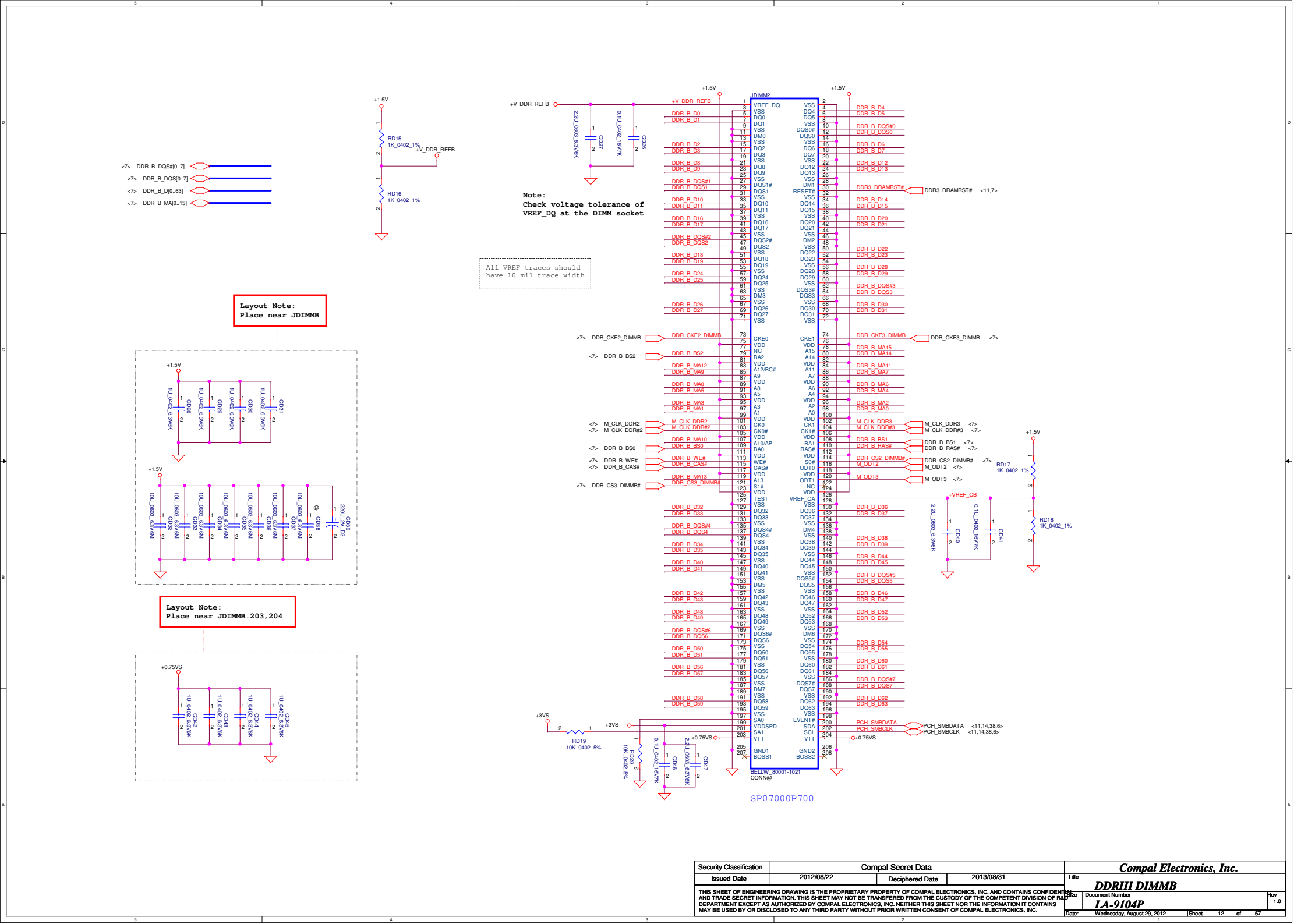
Compal Electronics, Inc.

Title: **DDRIII DIMMA**

Size | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 11 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

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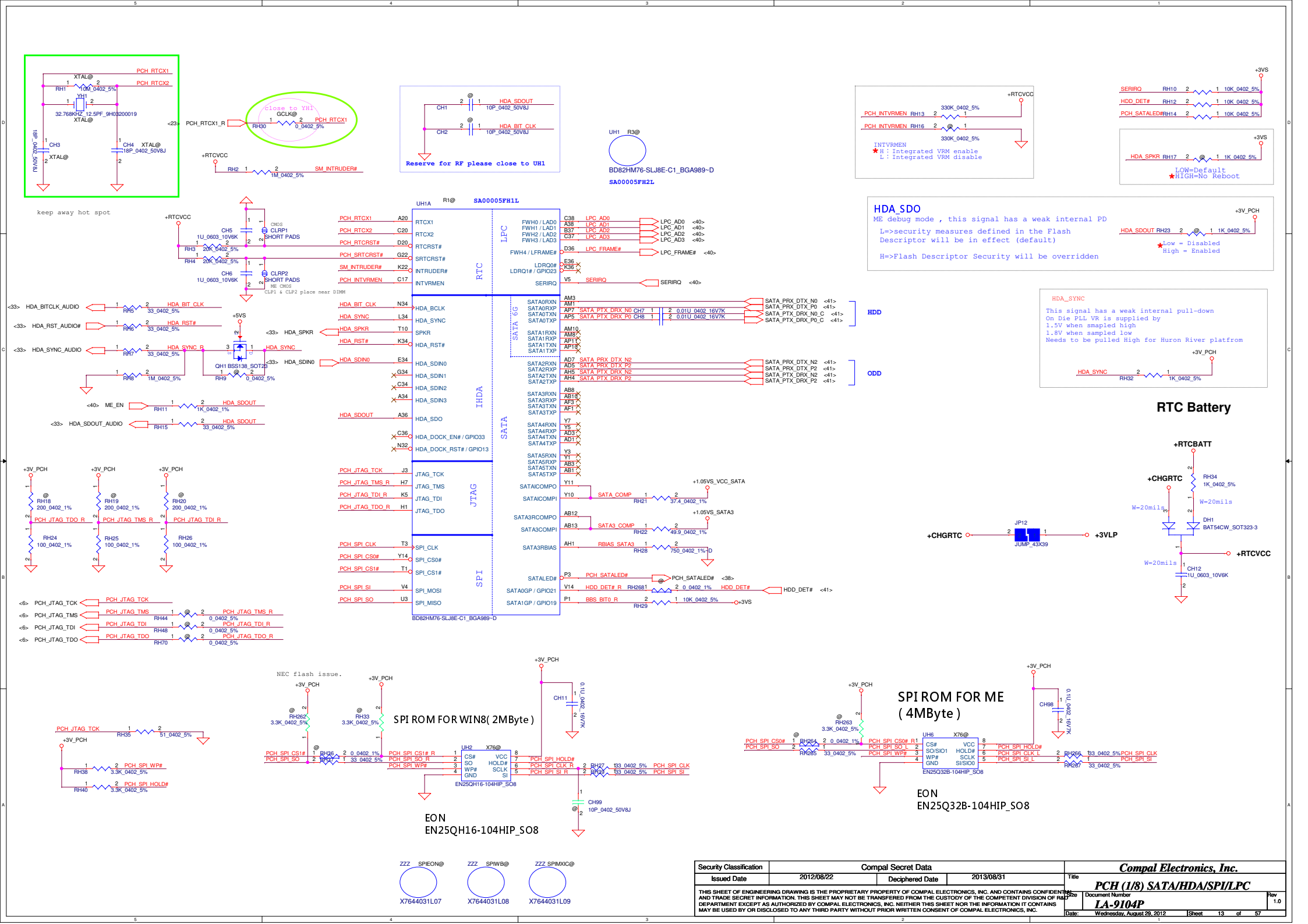
Compal Electronics, Inc.

Title: **DDRIII DIMMB**

Size | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 12 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

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Compal Electronics, Inc.

Title: **PCH (1/8) SATA/HDA/SPI/LPC**

Size: | Document Number: **LA-9104P** | Rev: 1.0

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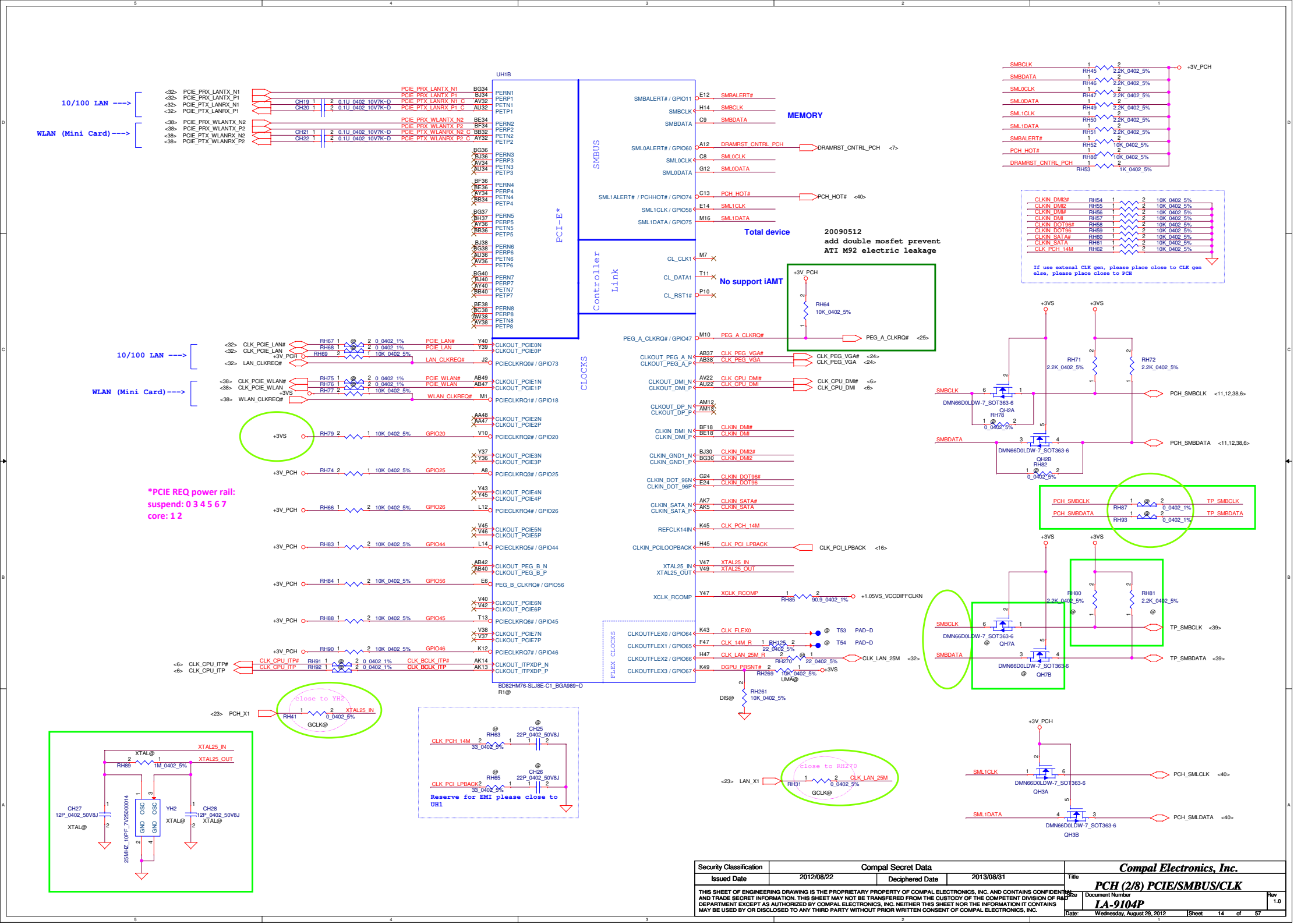

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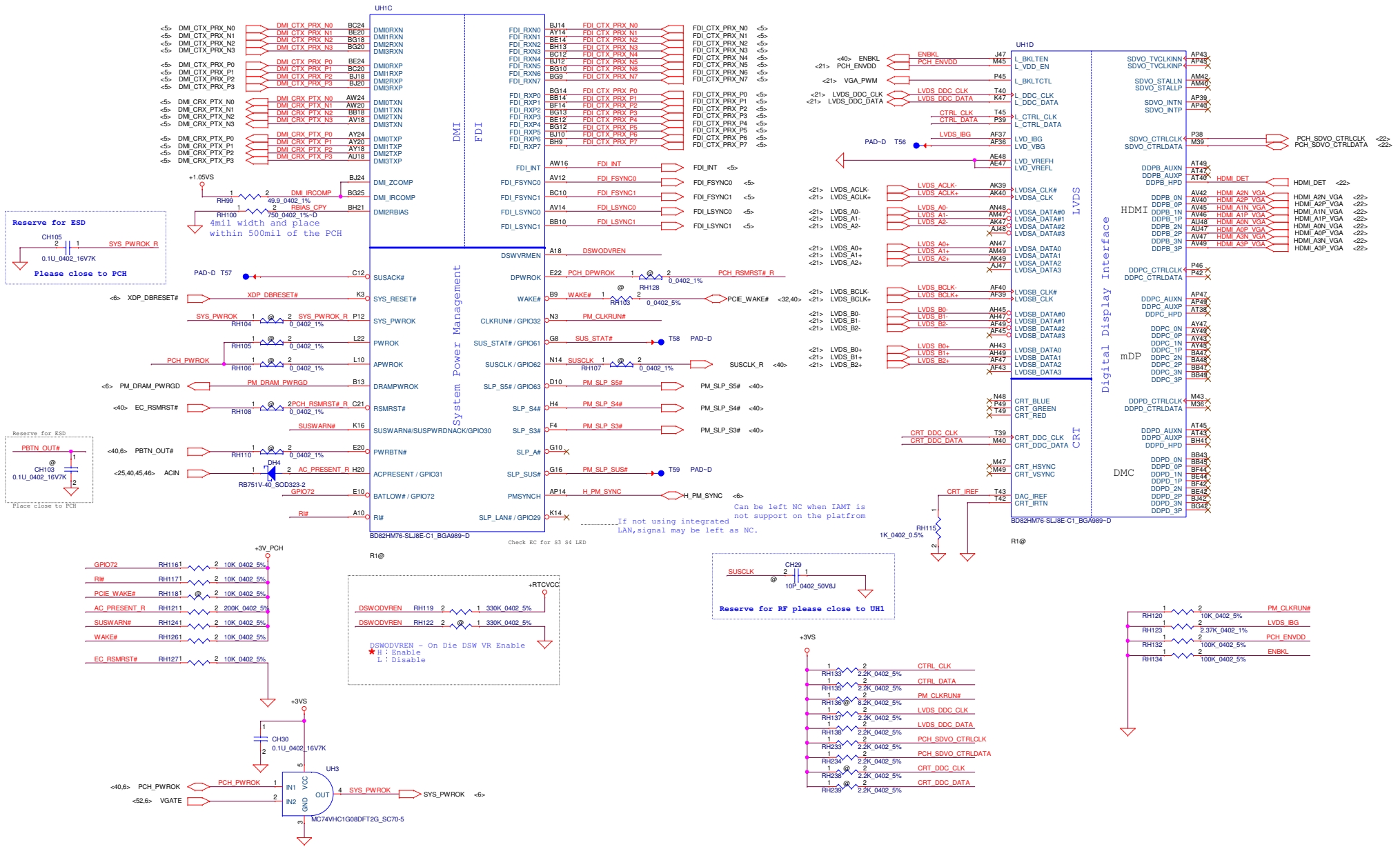
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: **PCH (2/8) PCIE/SMBUS/CLK**

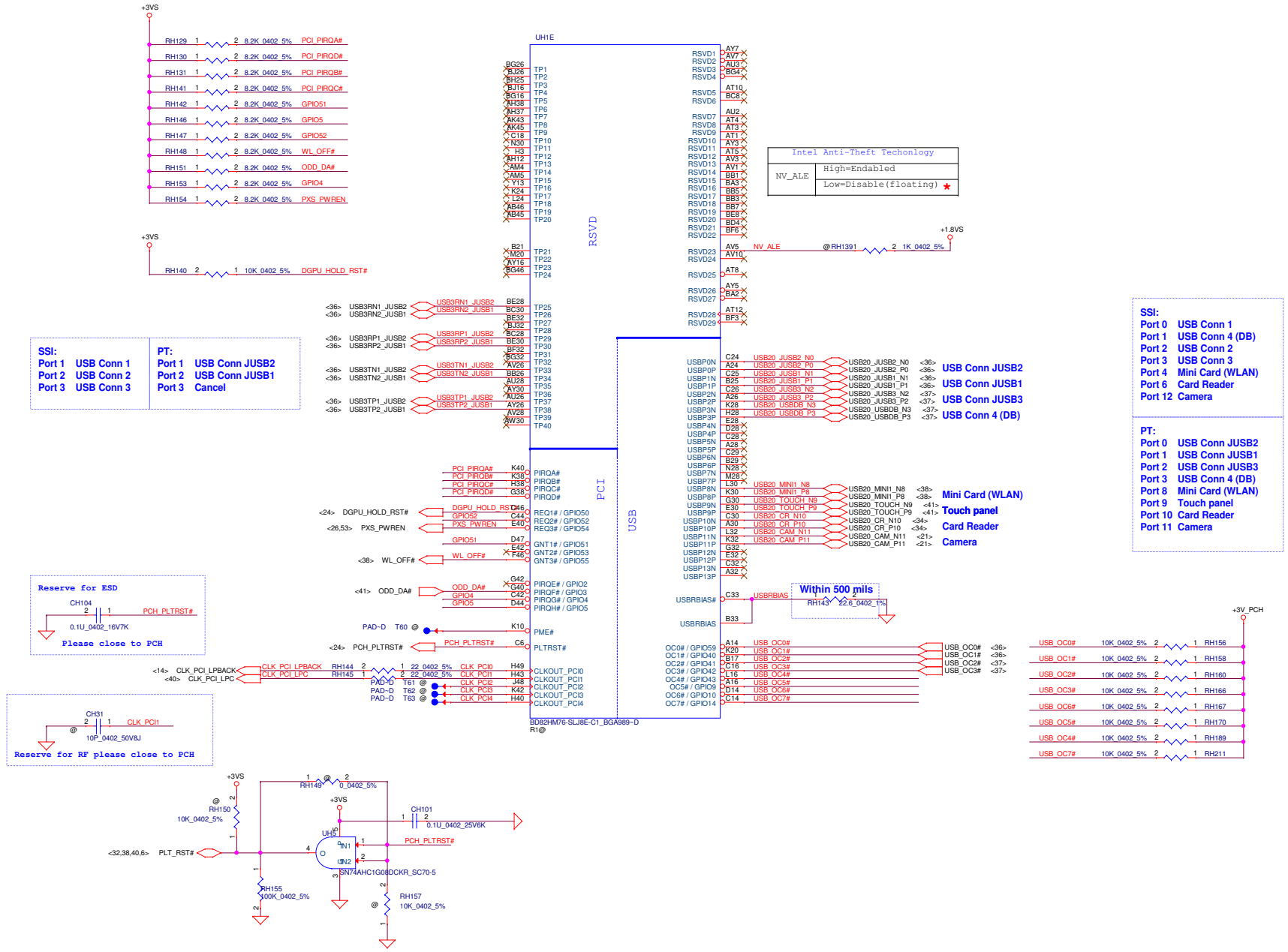
Size	Document Number	Rev
	LA-9104P	1.0

Date: Wednesday, August 29, 2012 Sheet 14 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.			
Title: PCH (3/8) DMI/FDI/PM/GFX/DP			
Size	Document Number: LA-9104P		Rev: 1.0
Date: Wednesday, August 29, 2012	Sheet 15 of 57		



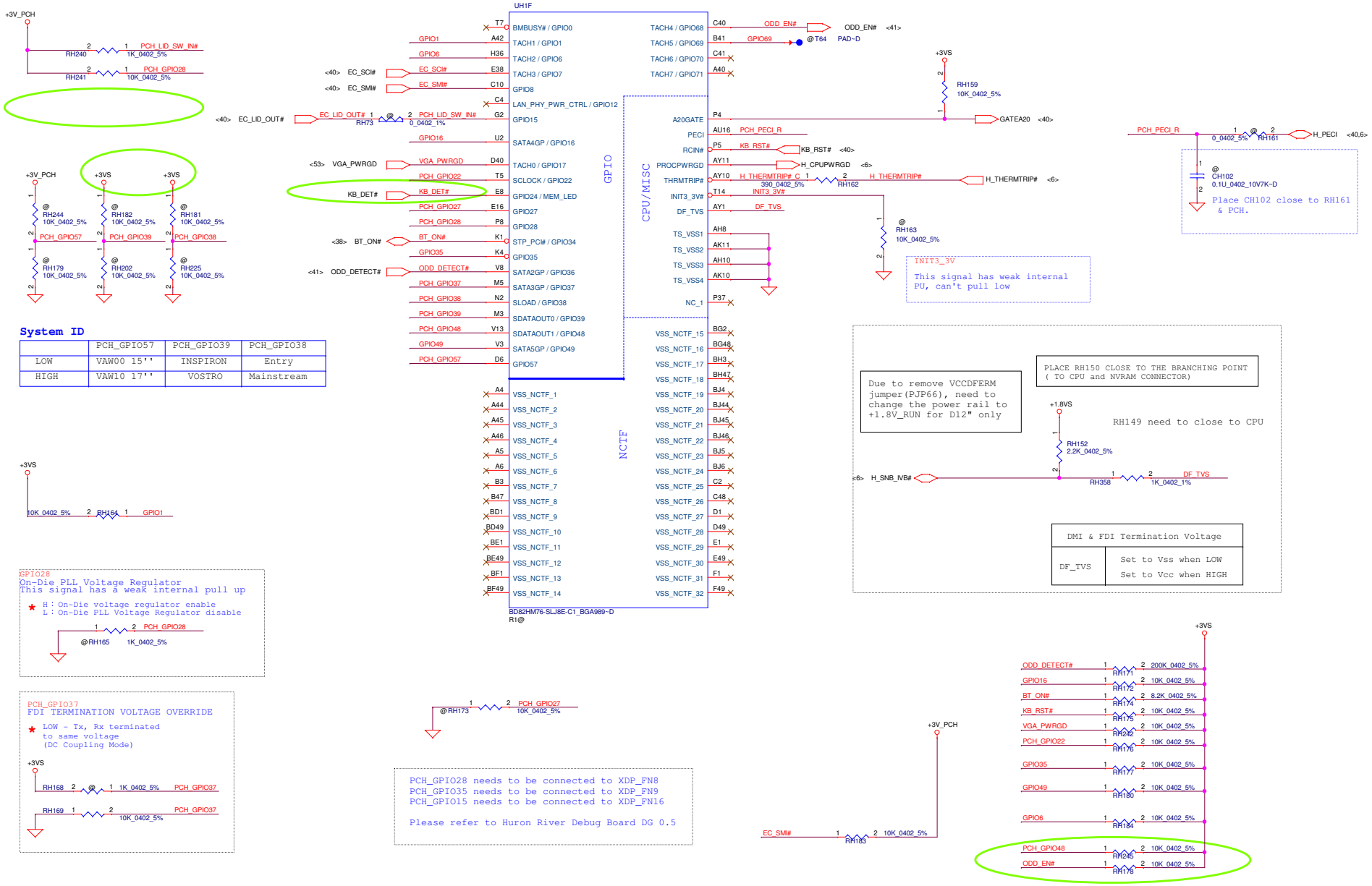
Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: PCH (4/8) PCI/USB/NVRAM

Size | Document Number: LA-9104P | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 16 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: **PCH (5/8) GPIO/CPU/MISC**

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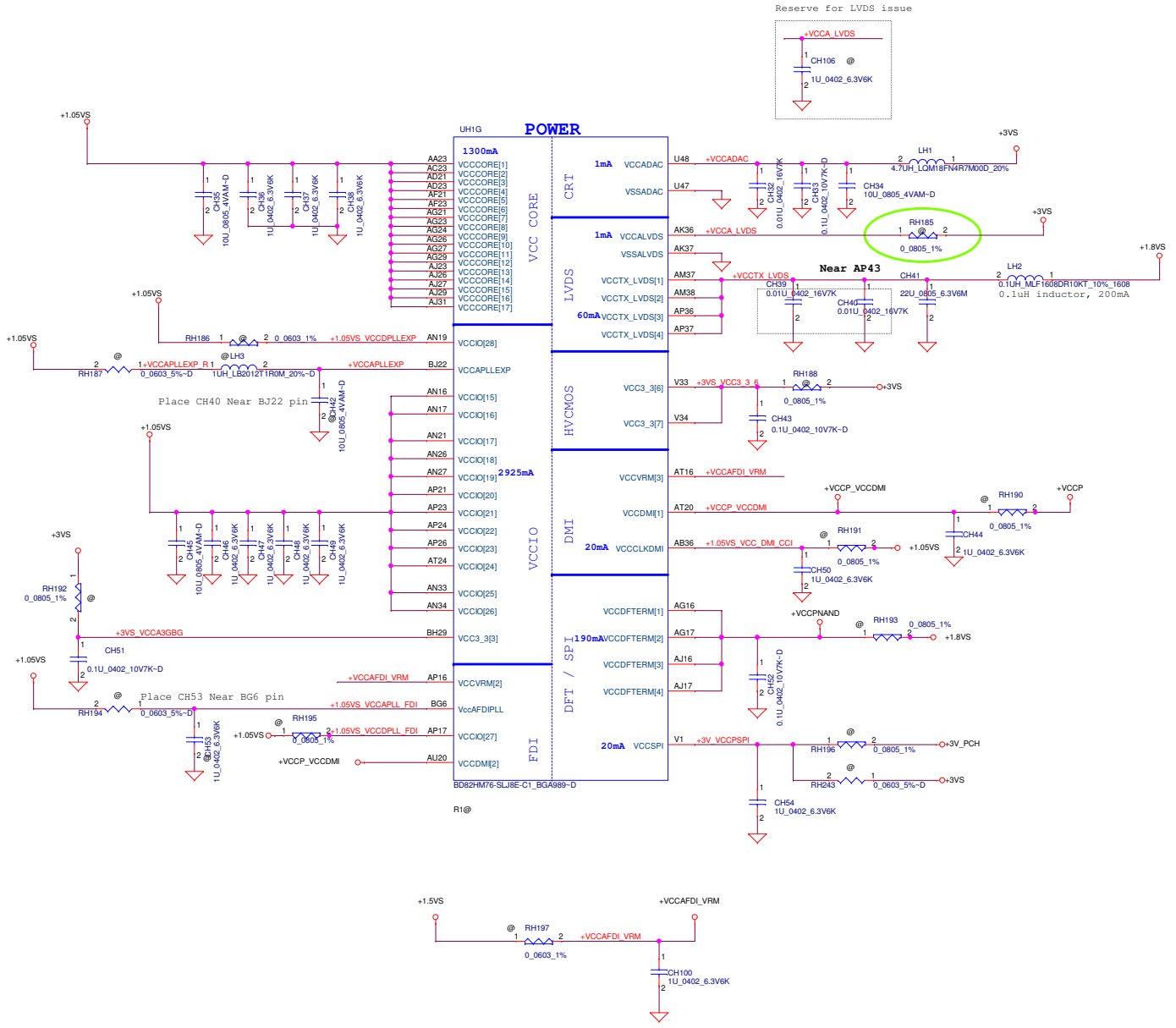
Date: Wednesday, August 29, 2012 | Sheet 17 of 57



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

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Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: PCH (6/8) PWR

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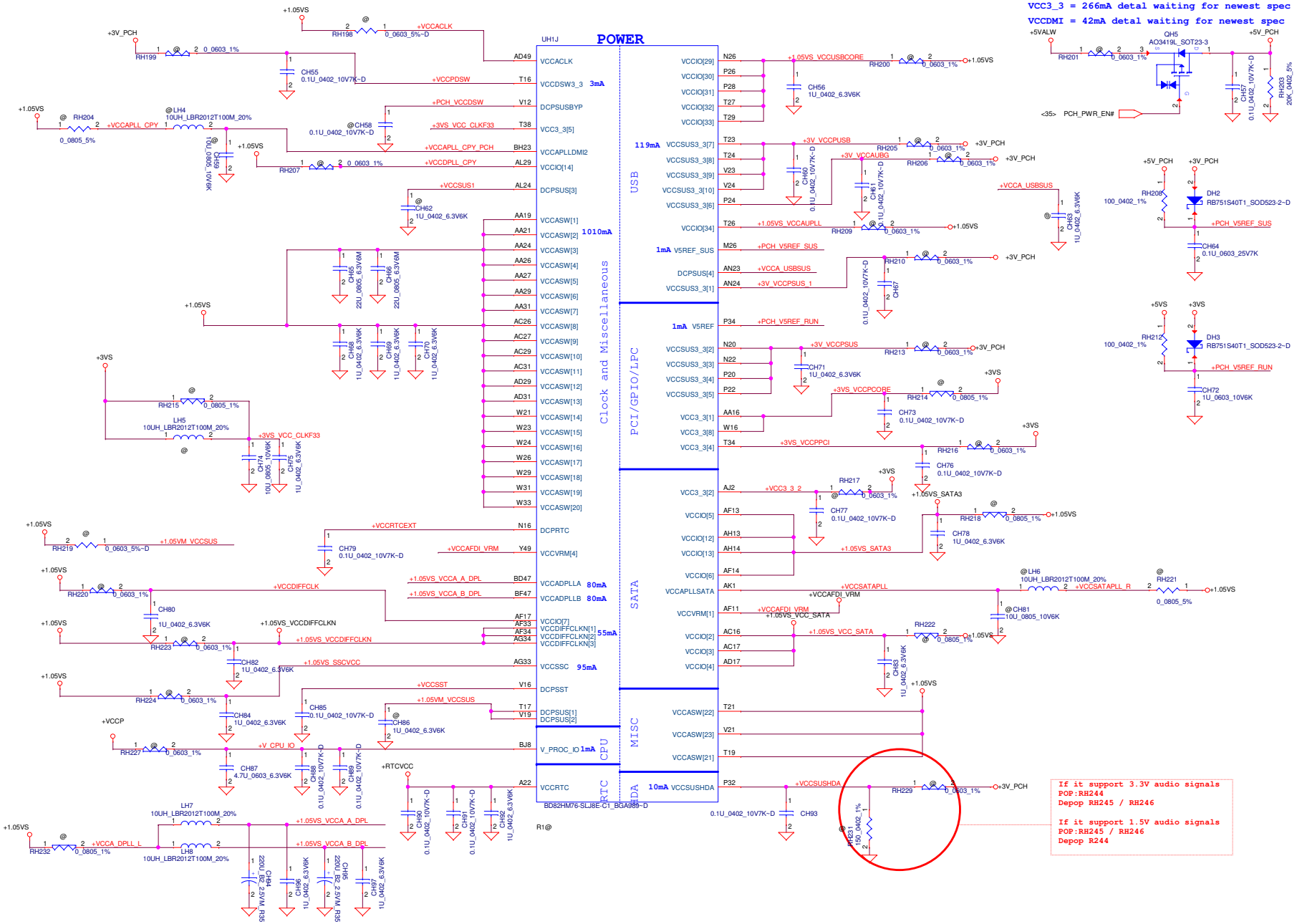

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Compal Electronics, Inc.

Title: **PCH (7/8) PWR**

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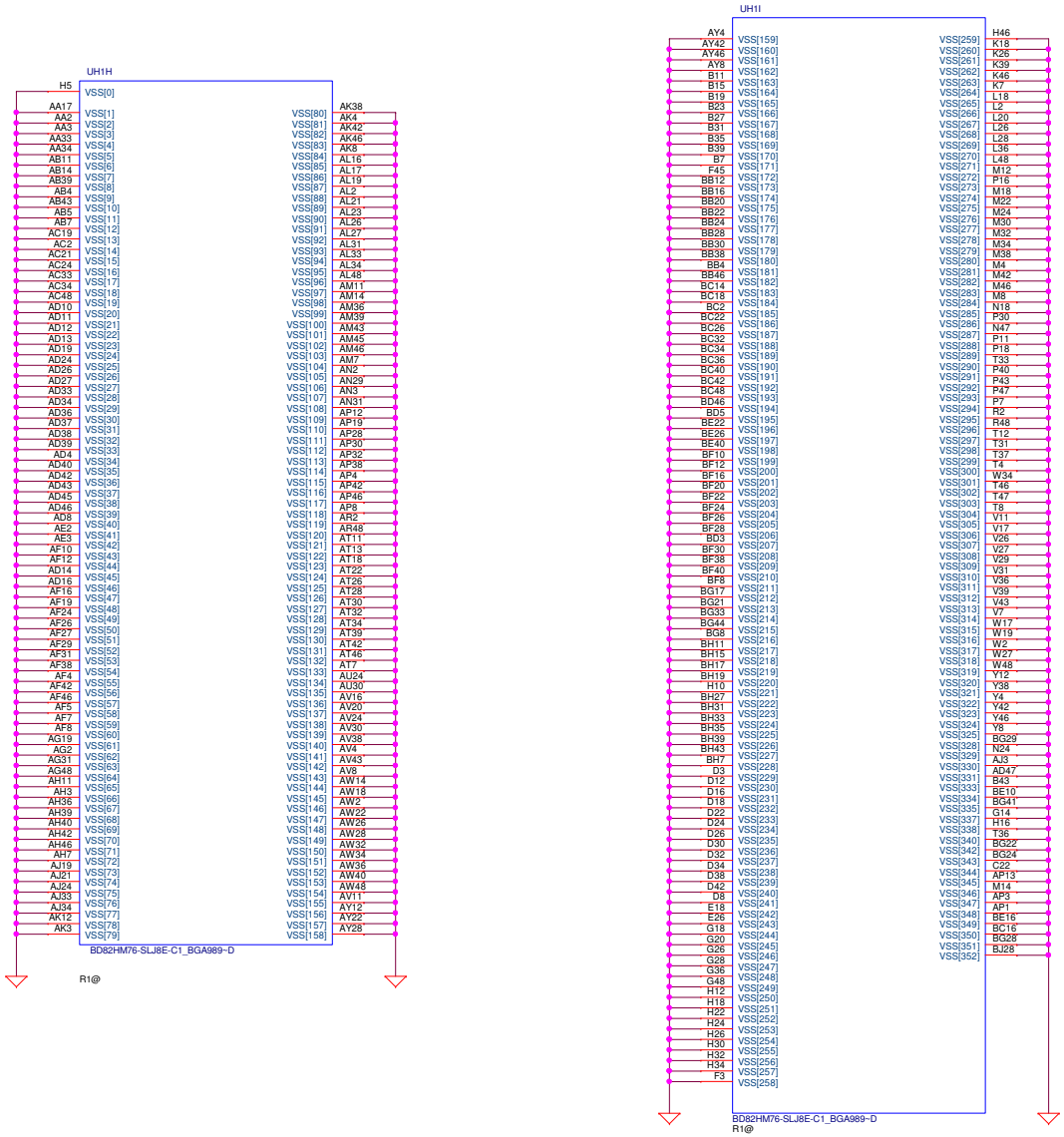

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Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

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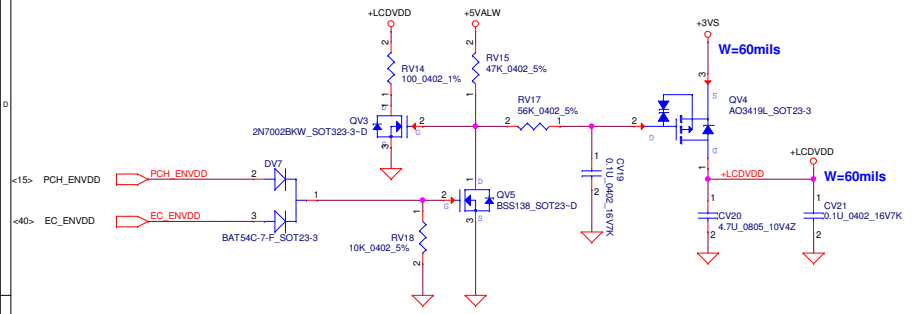
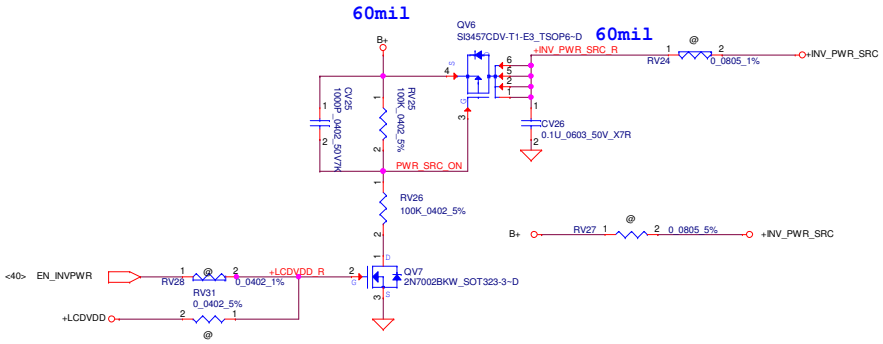
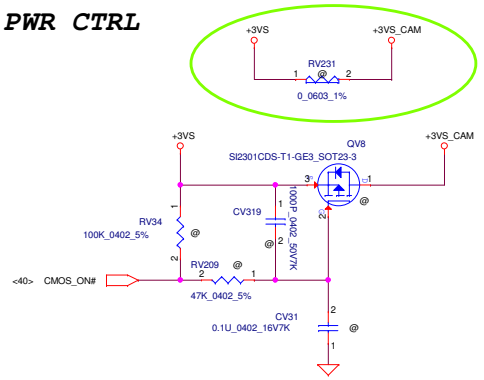
LCD PWR CTRL



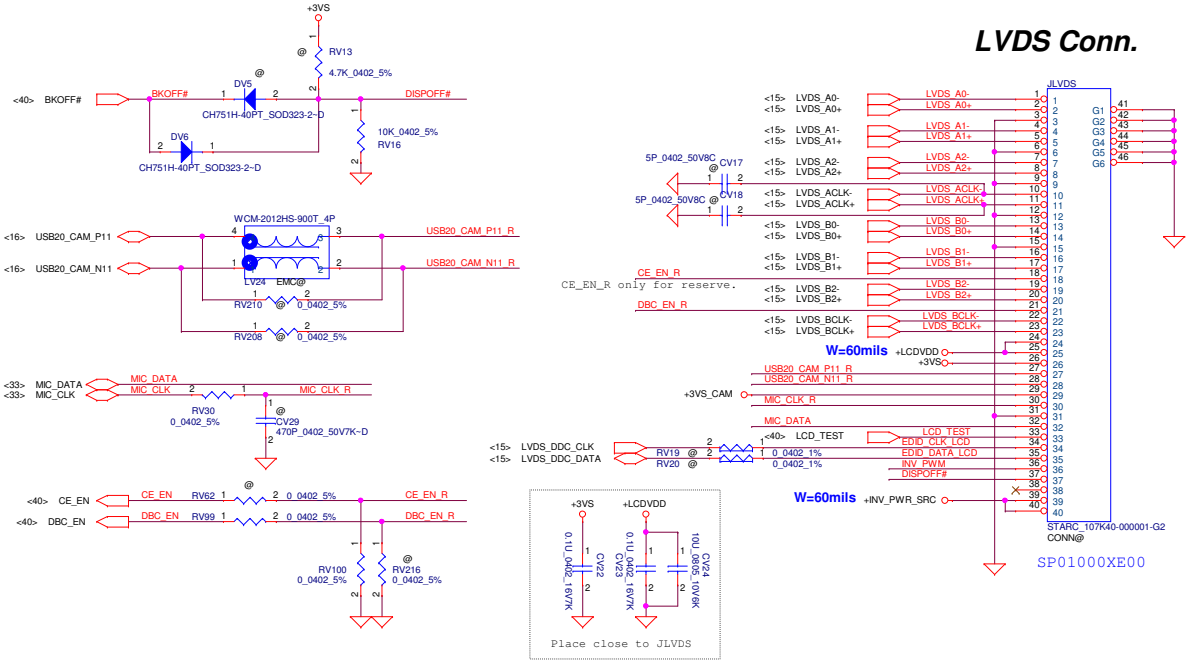
LCD backlight PWR CTRL

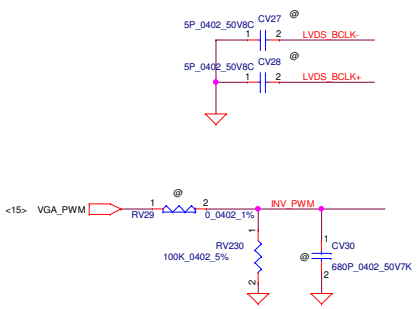


Webcam PWR CTRL

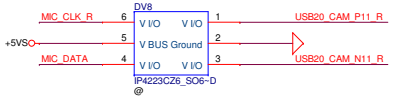


LVDS Conn.

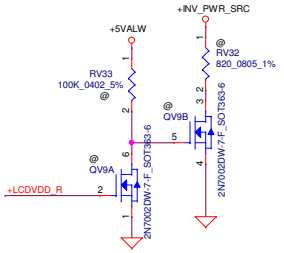




* Reserved for EMI/ESD/RF need to close to JLVDS



* Reserved for LCD sequence tuning



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Compal Electronics, Inc.

Title: LVDS/webcam

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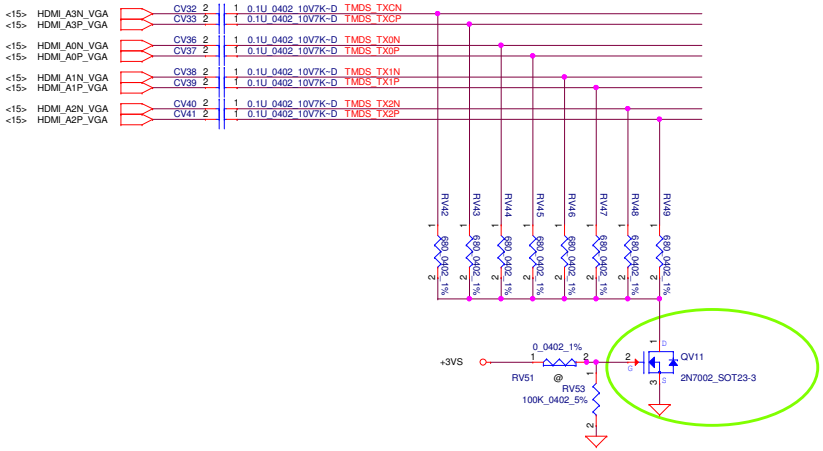
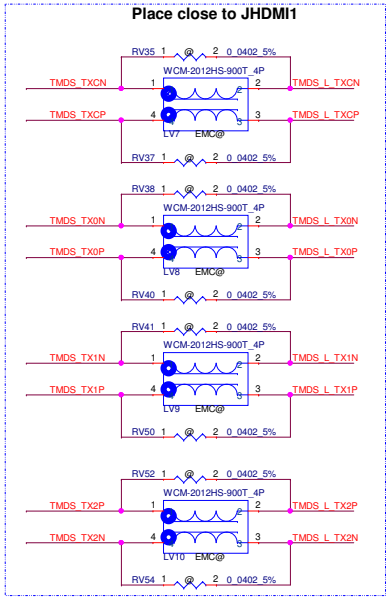
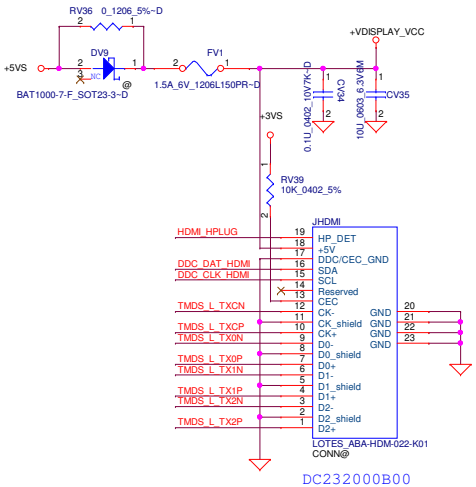
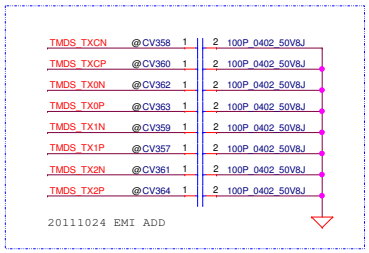
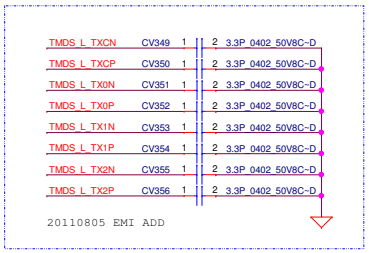
W=40mils

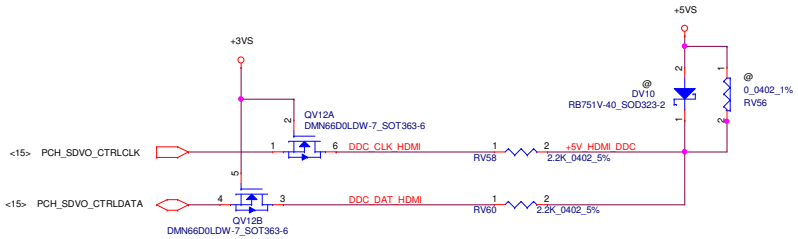


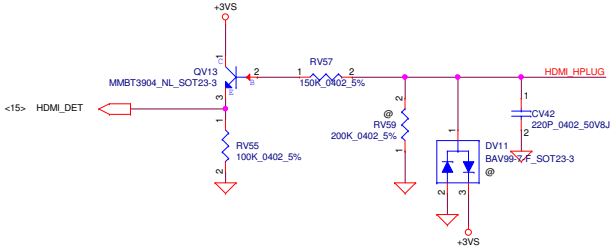












46@ ROYALTY HDMI W/LOGO

Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM

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Title: HDMI

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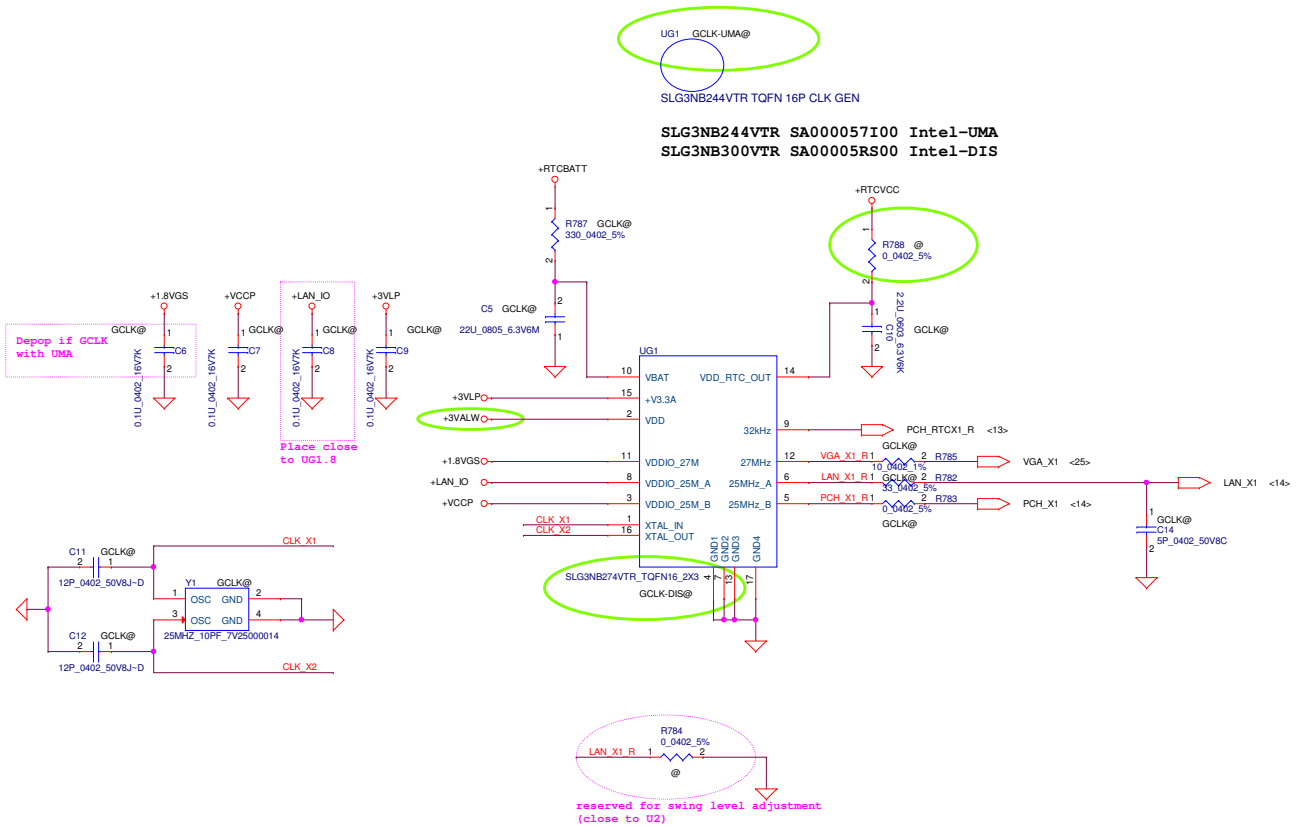

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Compal Electronics, Inc.

Title: GCLK

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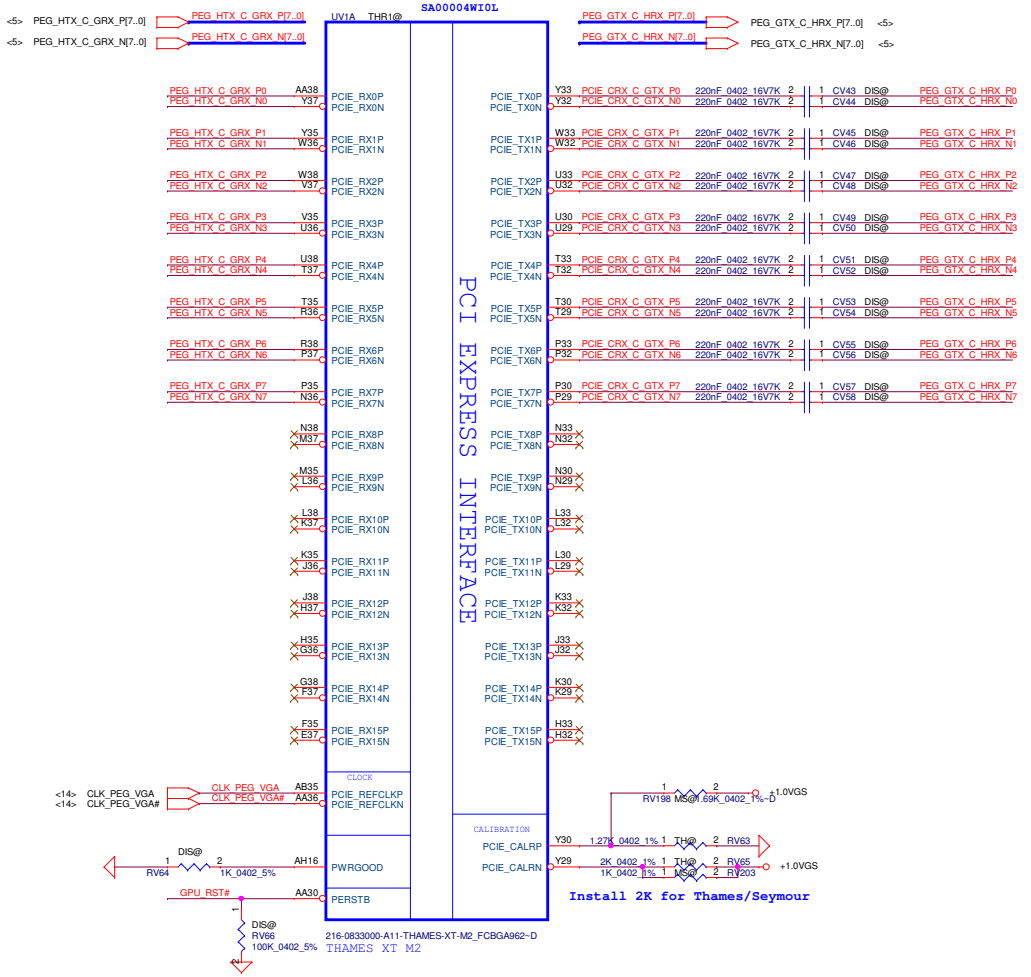
GFX PCIE LANE REVERSAL



UV1 THR3@ SA00004WI1L
216-0833000-A11-THAMES-XT-M2_FCBGA962~D

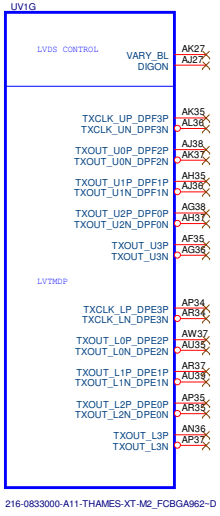
UV1 MSR1@ SA00005X10L
MARS-PRO_FCBGA962~D
MARS Pro

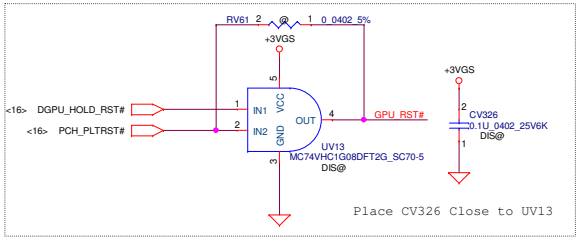
UV1 MSR3@ SA00005X10L
MARS-PRO_FCBGA962~D

UV1 CHR1@
Chelsea Pro

UV1 CHR3@
Chelsea Pro

LVDS Interface





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				Date: Wednesday, August 29, 2012 Sheet 24 of 57

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS		RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS	0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test	0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	RESERVED		0
BIF_VGA DIS	GPIO9	VGA ENABLED		0
RSVD	GPIO21	RESERVED		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT		XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS		0
RSVD	H2SYNC			0
RSVD	GENERICC			0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI		11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Samsung 1GB SA000004G5OL(R1) SA000004GS1L(R3)	RV68 0	RV69 1	RV72 0
Hynix 1GB SA000041S3L	RV67 1	RV70 0	RV72 0
Micron 1GB SA000004Y20L(R1) SA000004Y21L(R3)	RV67 1	RV69 1	RV71 1
Samsung 2GB SA000055H0L(R1) SA000055H1L(R3)	RV68 0	RV69 1	RV71 1
Hynix 2GB SA000003YO2L(R1) SA000003YO3L(R3)	RV67 1	RV70 0	RV71 1
Micron 2GB SA000005XB0L(R1) SA000005XB1L(R3)			

PT

Mars Pro MLPs	RV241	RV242	Bits [3:1]
Hynix	NC	4.75k	000
Samsung	8.45k	2k	001
Micron	4.75k	NC	111

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)

Add 12/6 for MLPS 0402 1% resistors are required.

NC_TSVSSQ should be tied to GND on Thames/Seymour

Add 12/6 for MLPS

Need to CHECK CIS symbol

Close to YV1

Internal VGA Thermal Sensor

VGA Thermal Sensor ADM1032ARMZ

Closed to GPU

Address:100_1101

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Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_Main_MSIC

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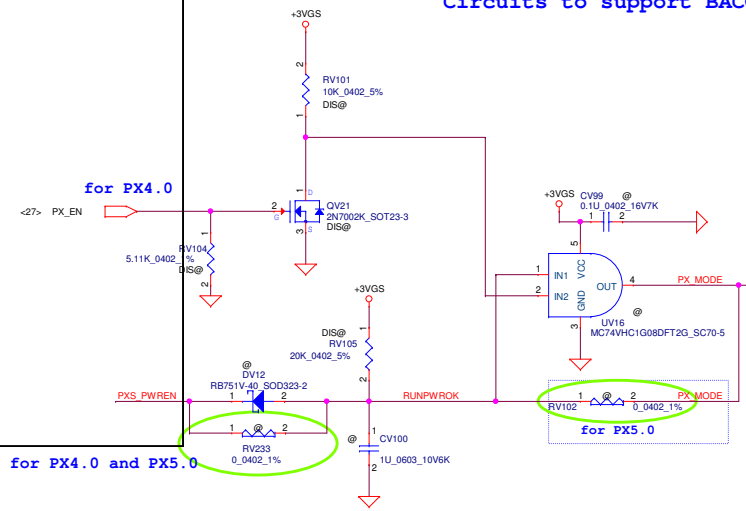
Circuits to support BACO

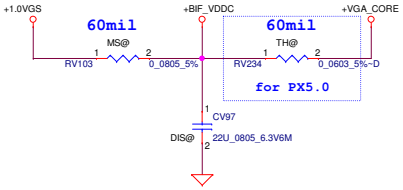
Switch circuits in BACO desingns for Thanes/Seymour only

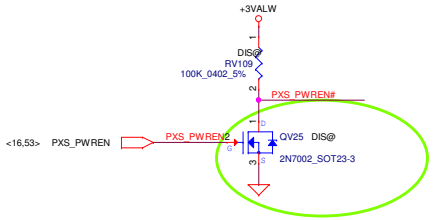
55mA@1.0V, in BACO mode



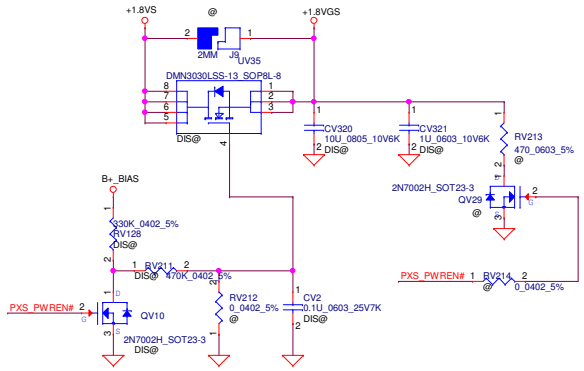
PX_MODE=1 for Normal Operation

PX_MODE=0 for BACO mode to shut down power rails expcept VDDR3,PCIE_VDDC and 1.8V rail

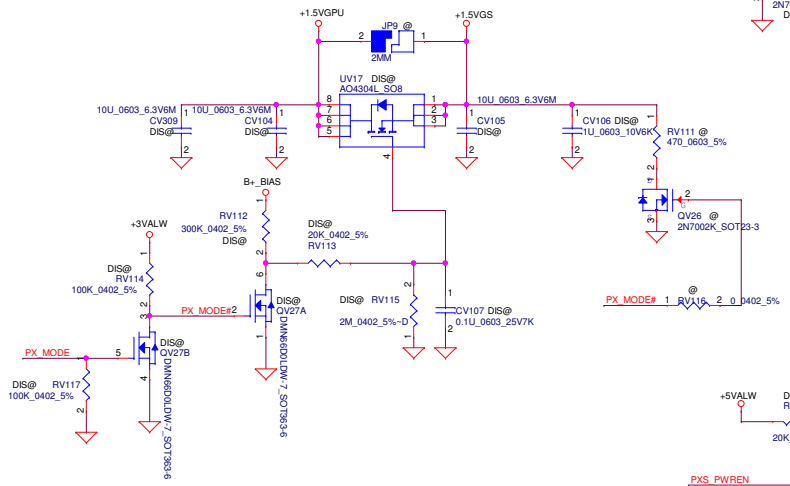




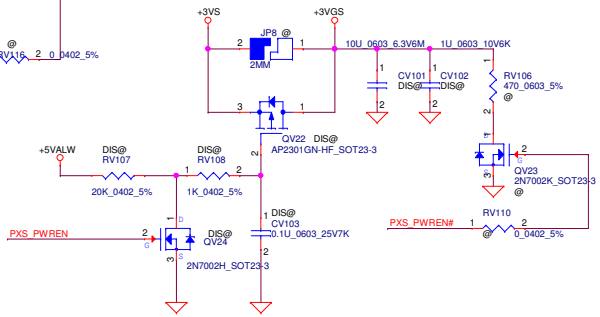
+1.8VS TO +1.8VGS



+1.5VGPU TO +1.5VGS



+3.3VS TO +3.3VGS



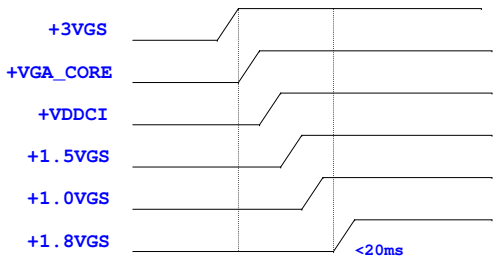
Note:

PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON

PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF

PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

Power Seguence of Thames and Mars Pro



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Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_BACO POWER

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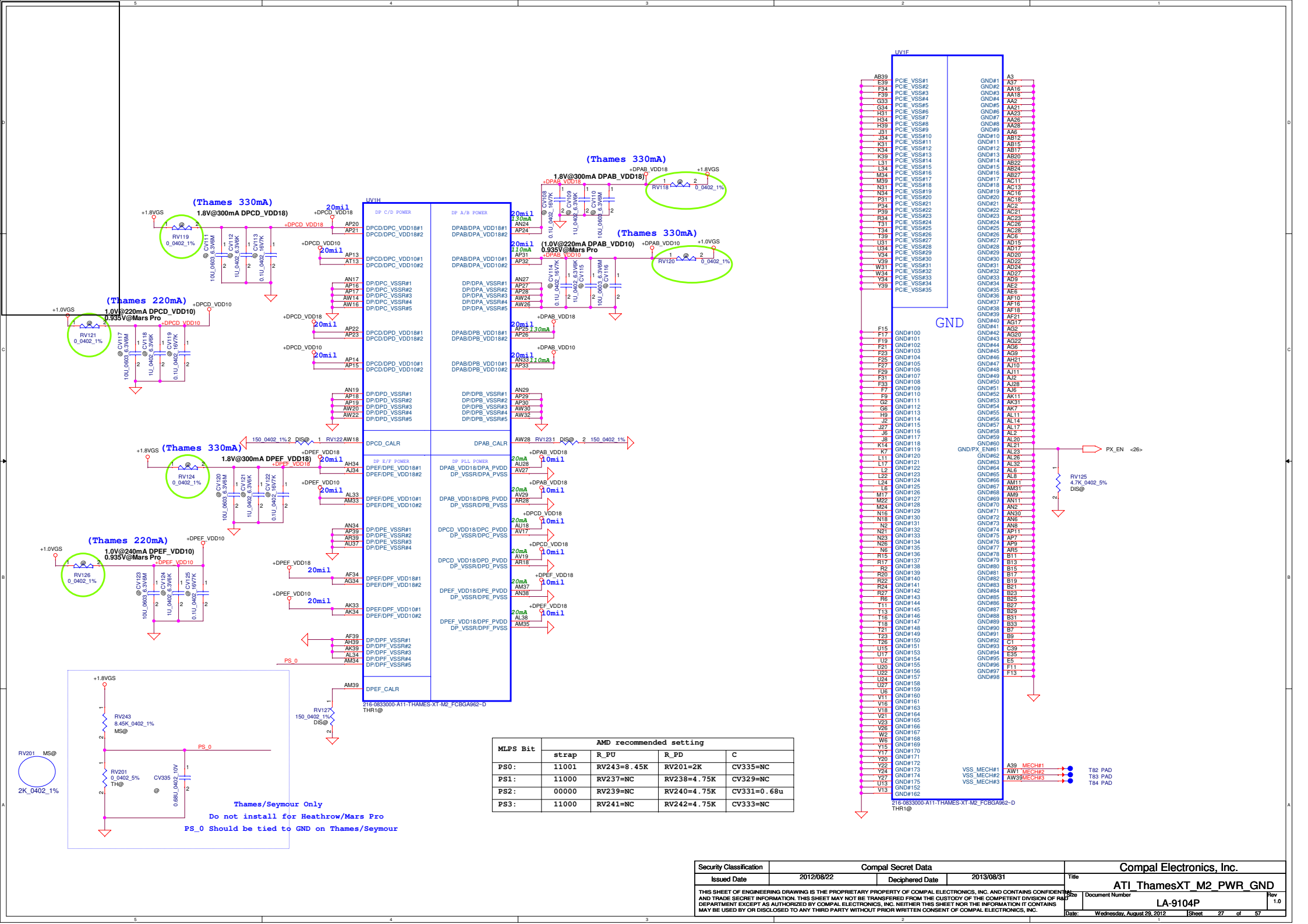

MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_PWR_GND

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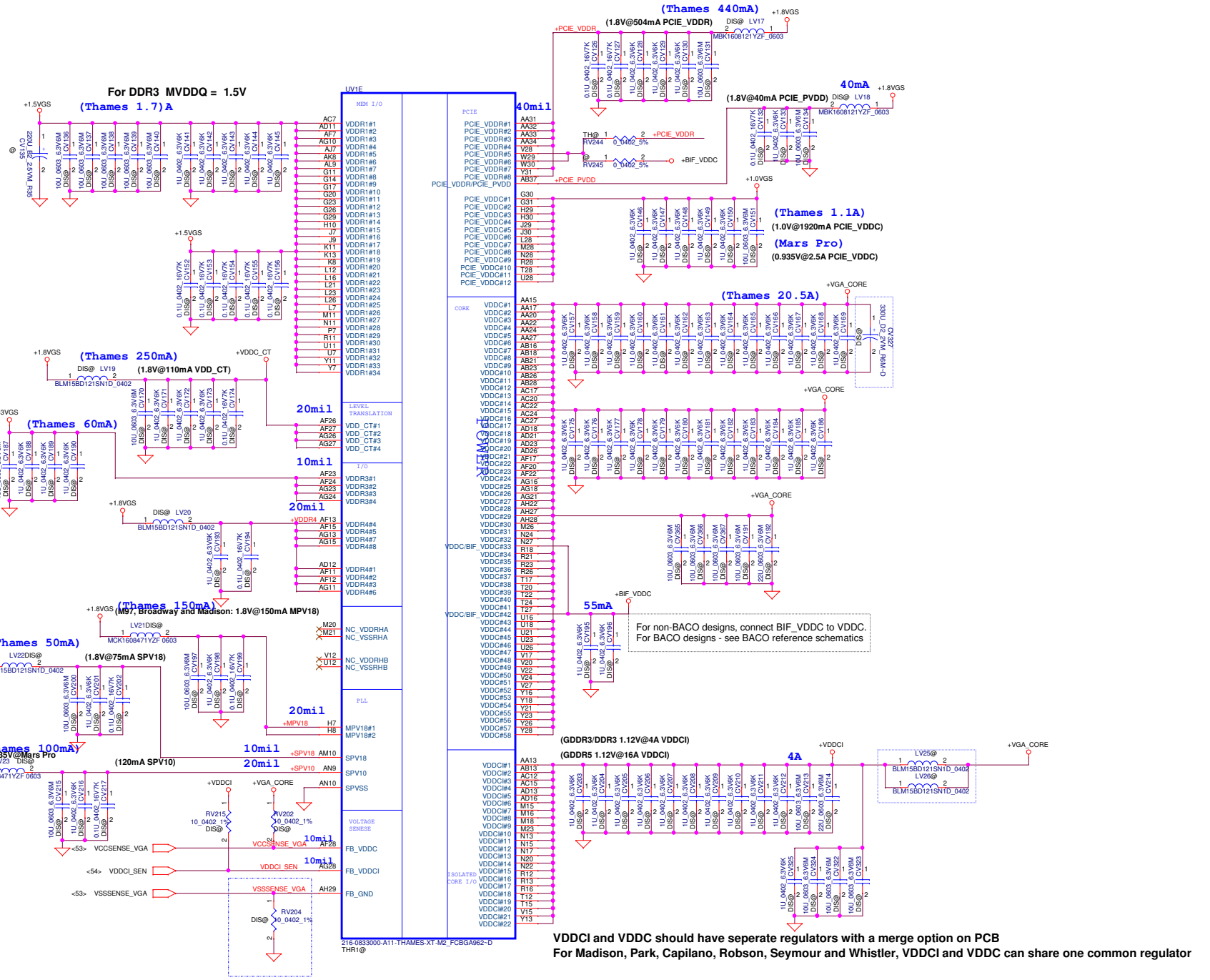

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Title: ATI_ThamesXT_M2_Power

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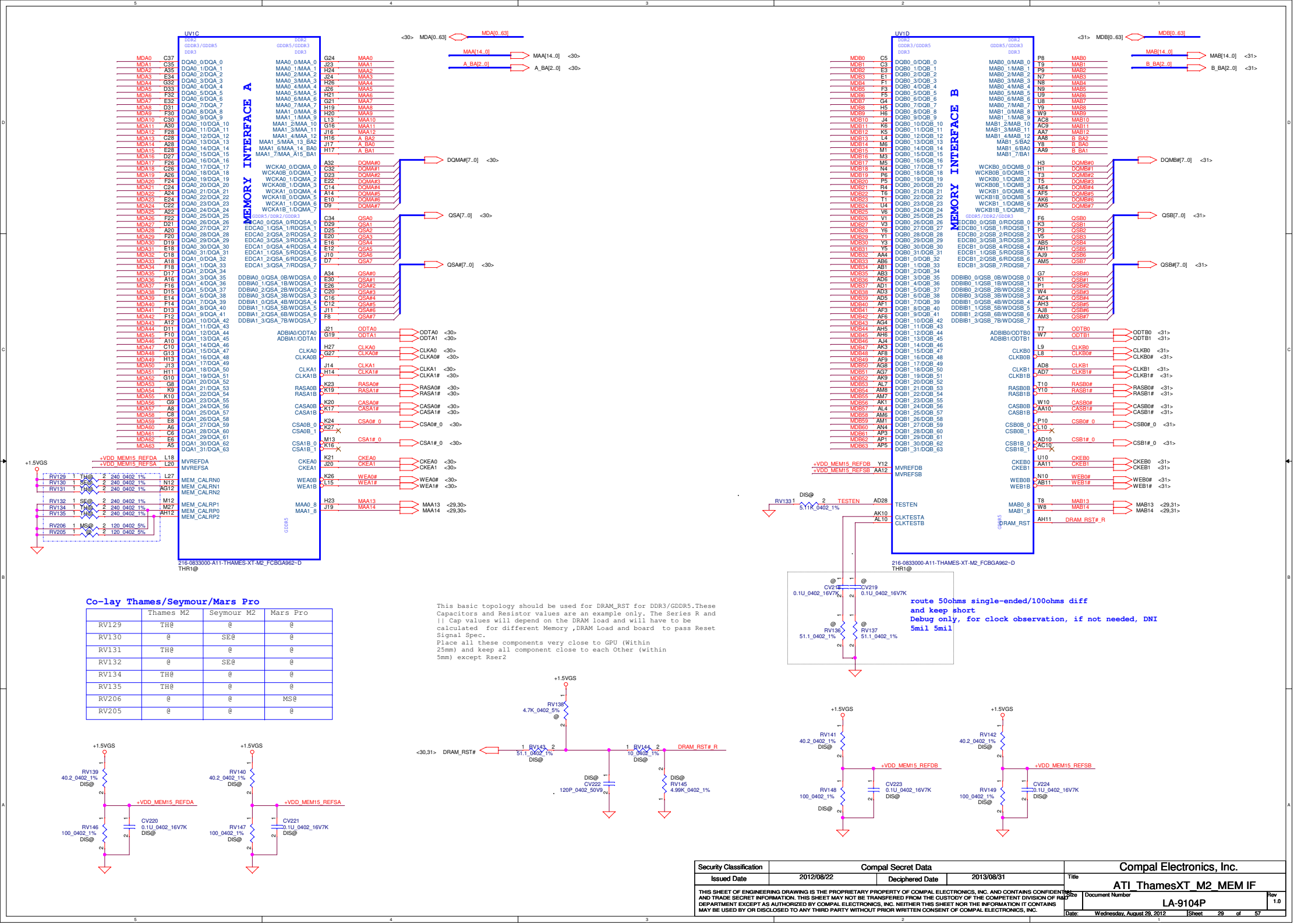

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Issued Date	2012/08/22	Deciphered Date	2013/08/31

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Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_MEM IF

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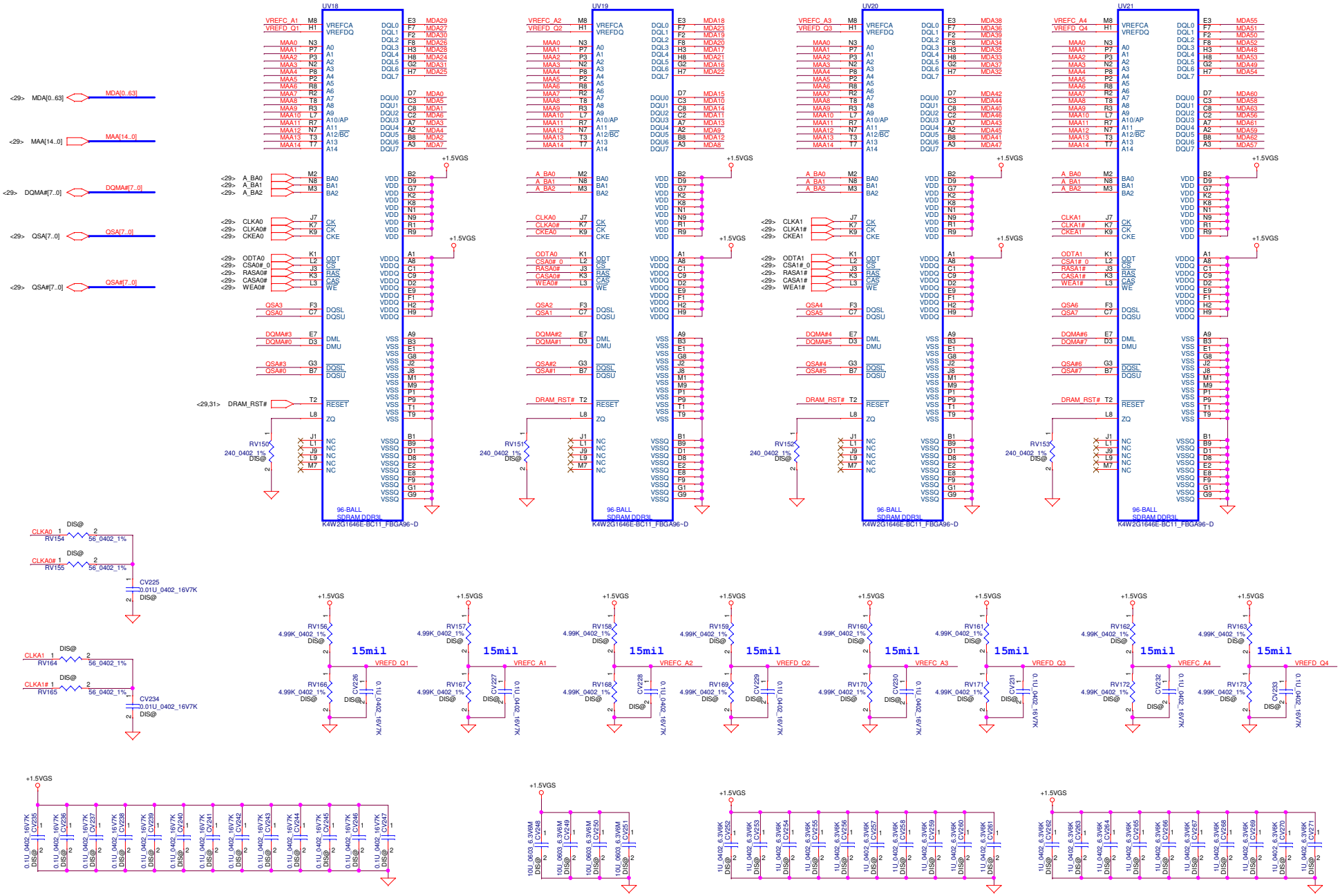
CHANNEL A: 256MB/512MB DDR3



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_VRAM_A

Size	Document Number	Rev
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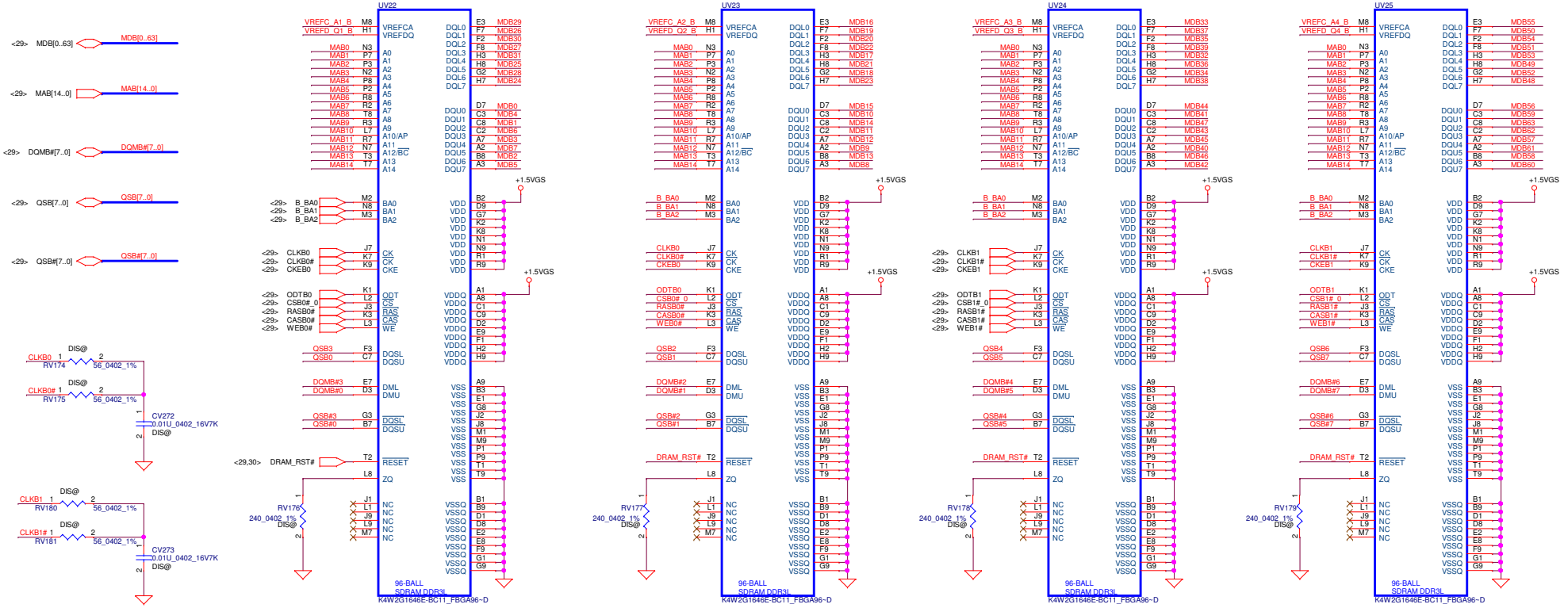
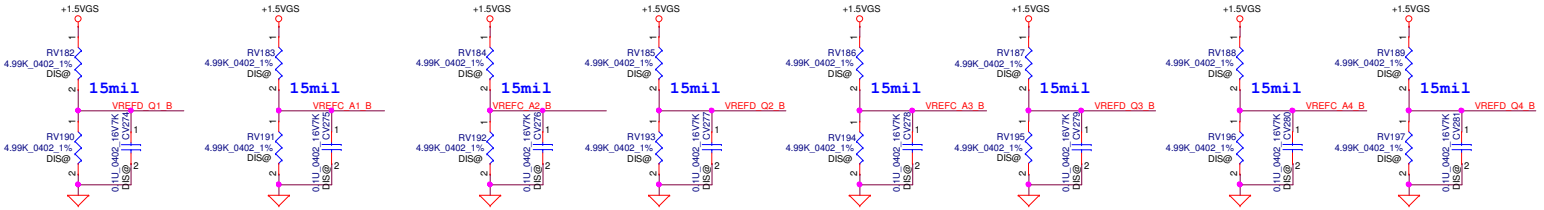
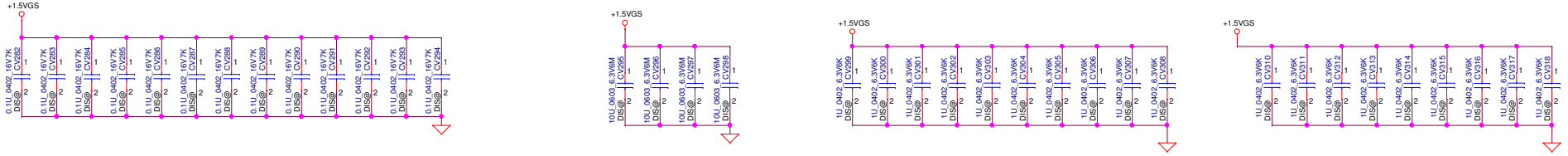
CHANNEL B: 256MB/512MB DDR3







Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_VRAM_B

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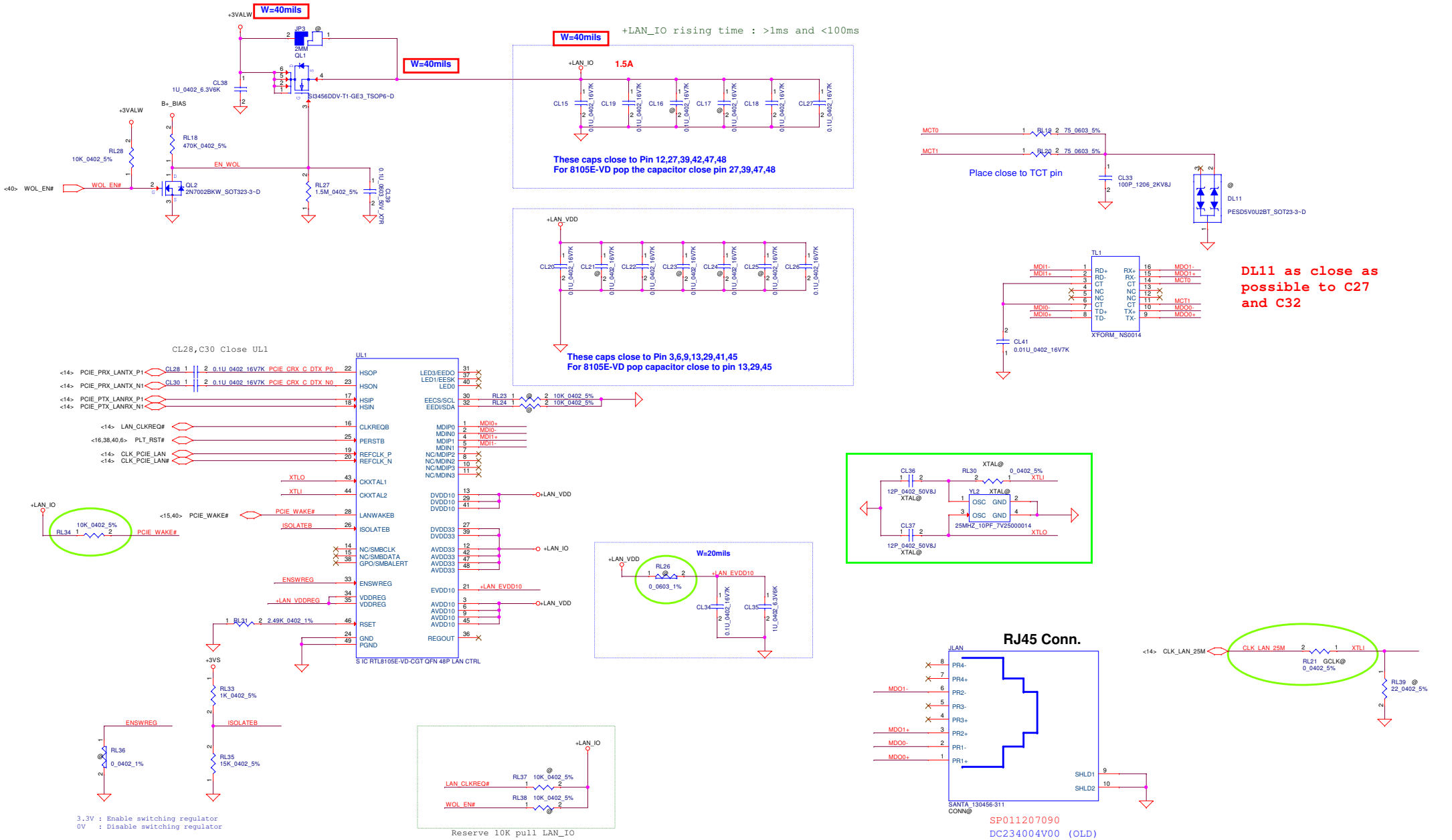
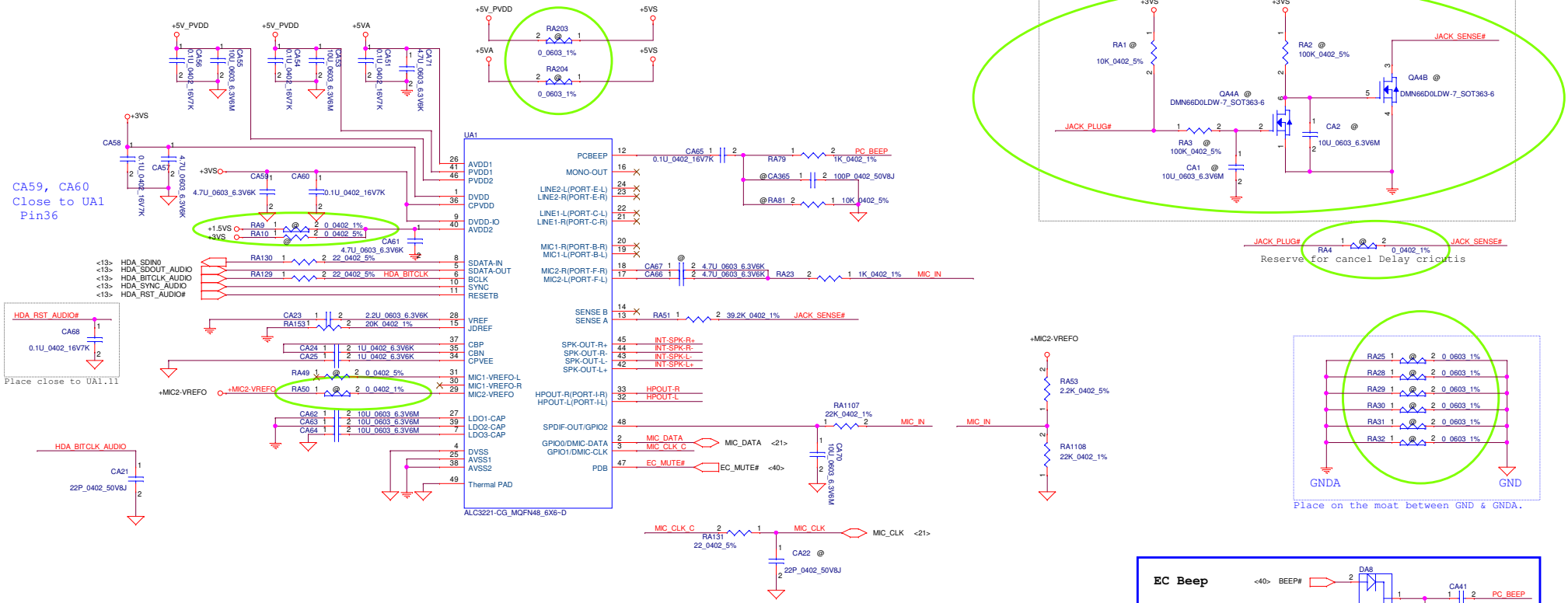
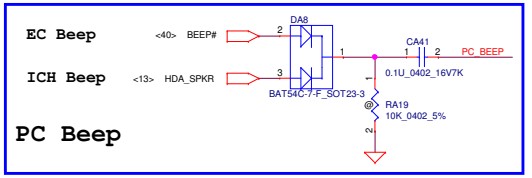


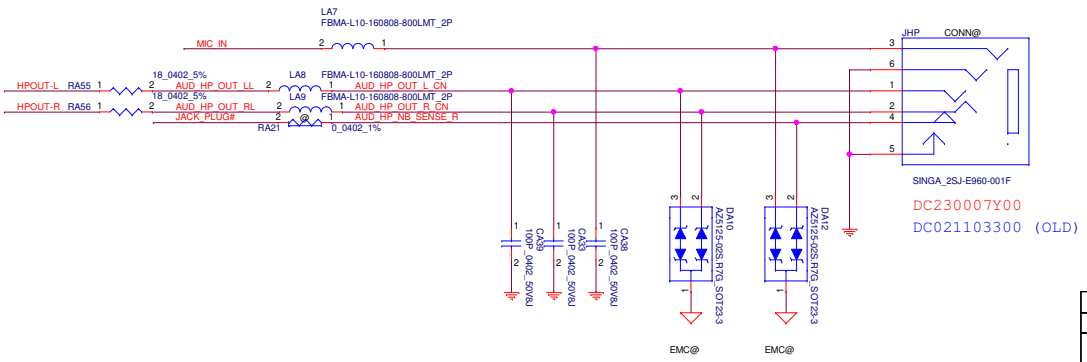
Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

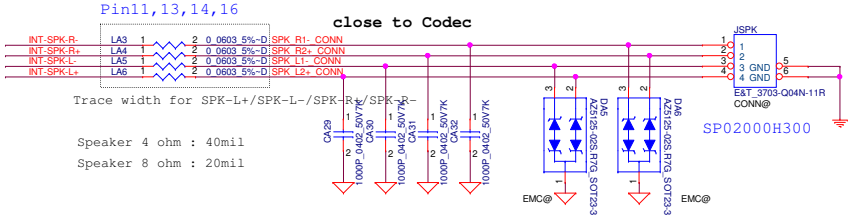
Compal Electronics, Inc.			
Title: LAN RTL8105E			
Size	Document Number: LA-9104P		Rev: 1.0
Date: Wednesday, August 29, 2012	Sheet 32 of 57		



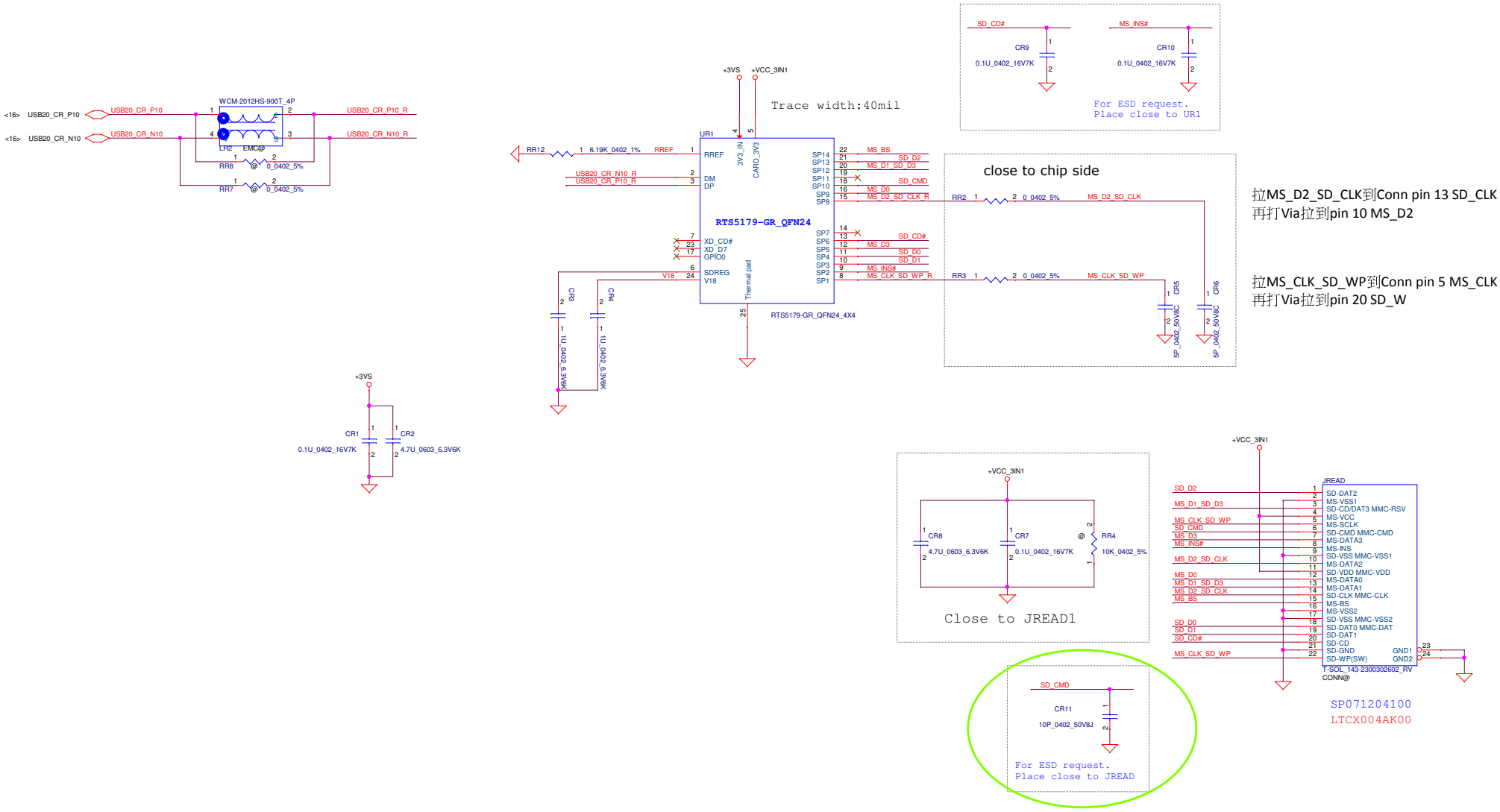


iPhone type Combo Jack





Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title: Audio Codec ALC3221
				Size: Document Number: LA-9104P Rev: 1.0
				Date: Wednesday, August 29, 2012 Sheet 33 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: **Card Reader RTS5179**

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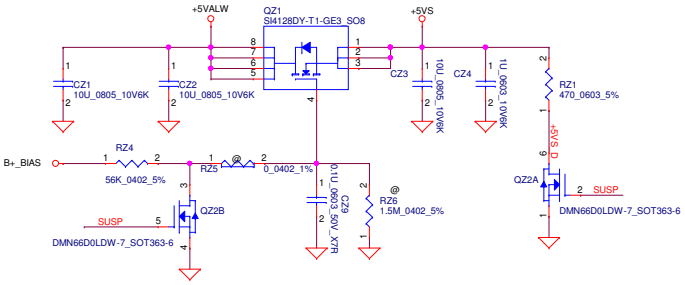
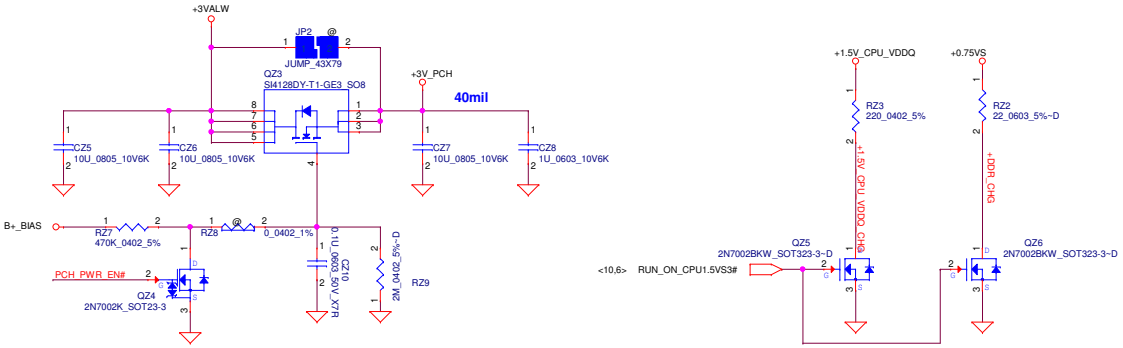
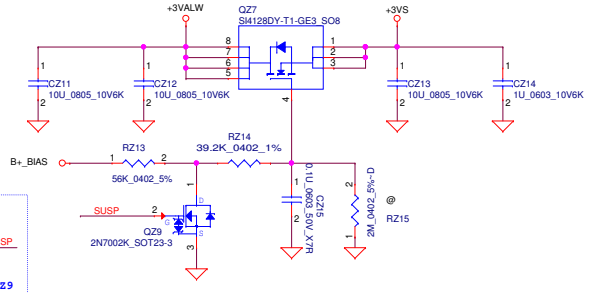
+5VALW to +5VS

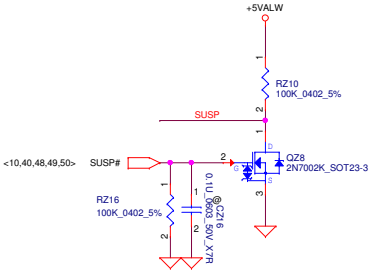


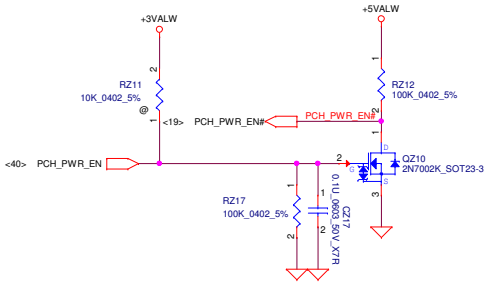
+3VALW to +3V_PCH



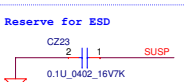
+3VALW to +3VS



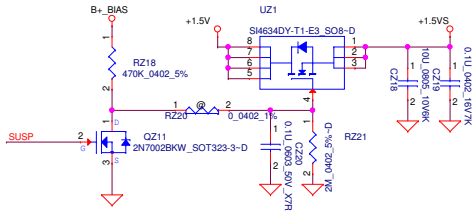


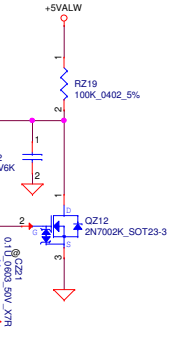


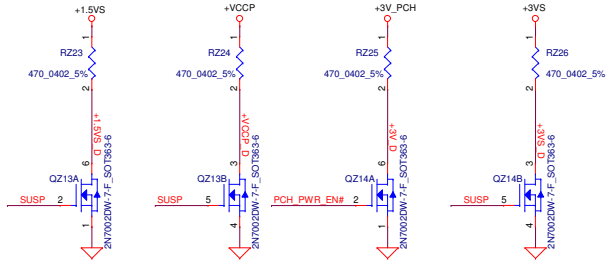
Reserve for ESD

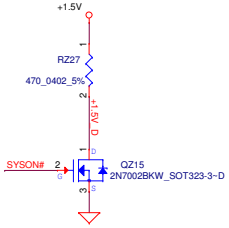


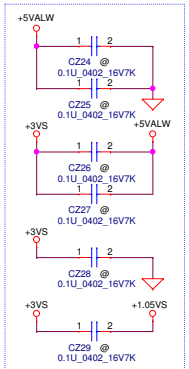
+1.5V To +1.5VS











Reserve for ESD

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: DC/DC Interface

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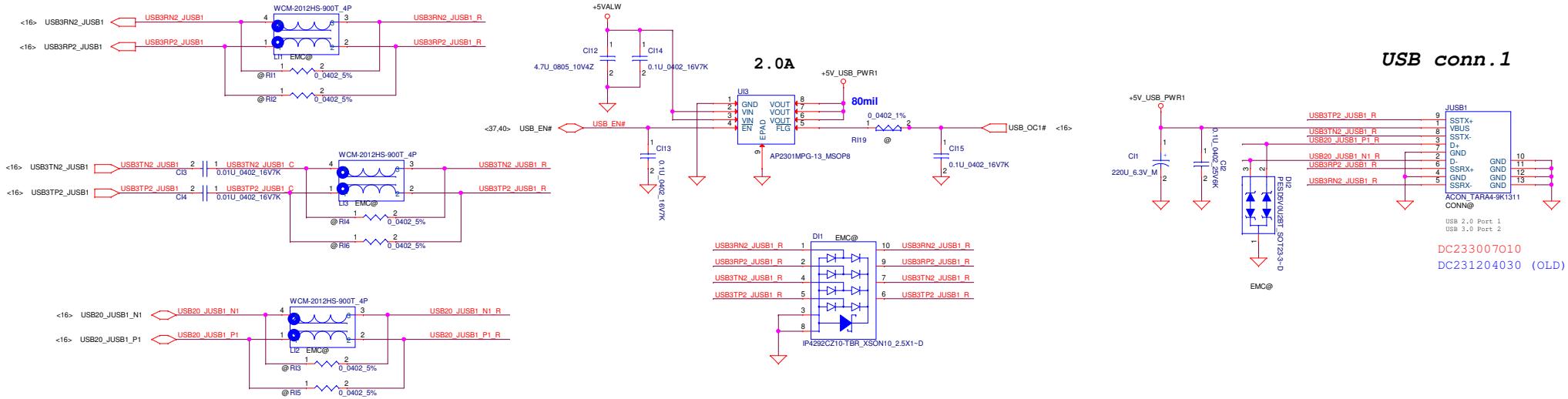
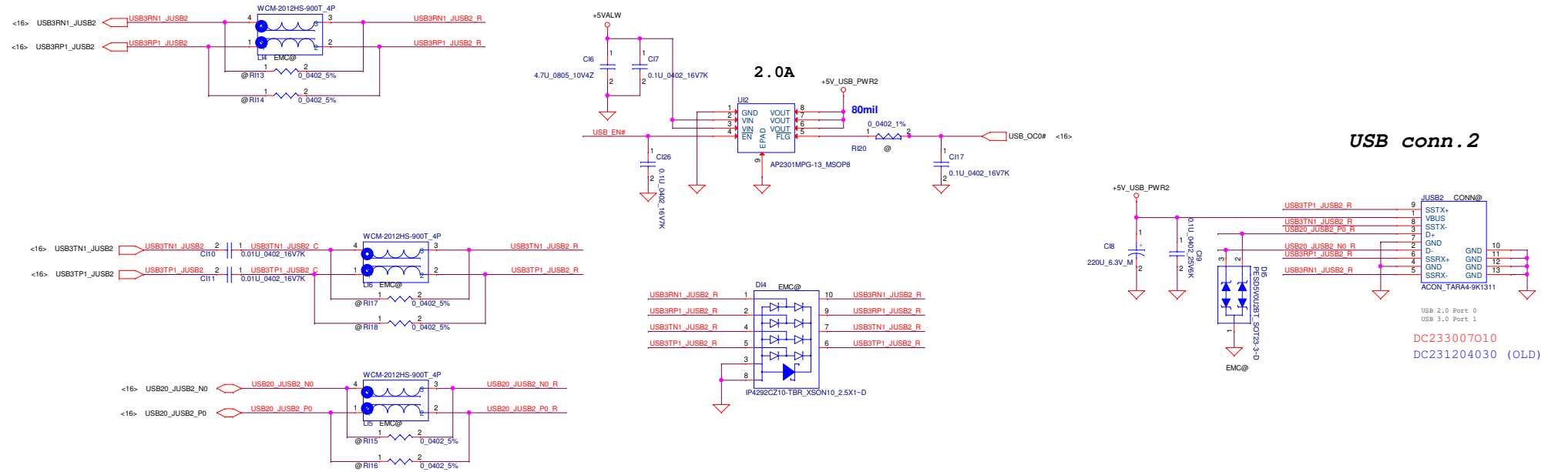


USB conn.1



USB conn.2

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: **USB3.0**

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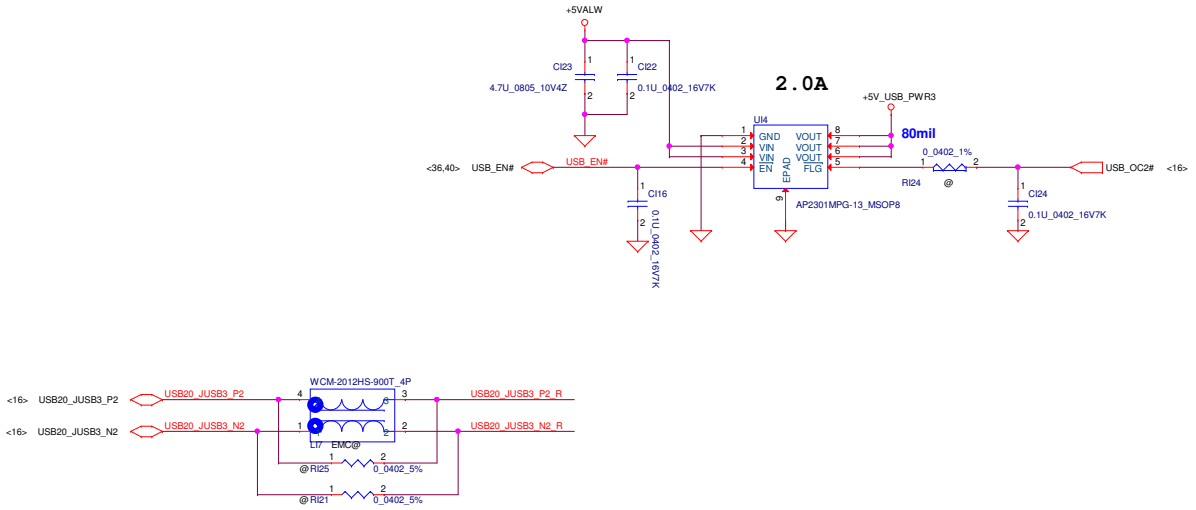
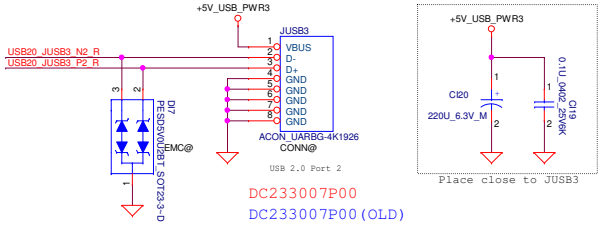
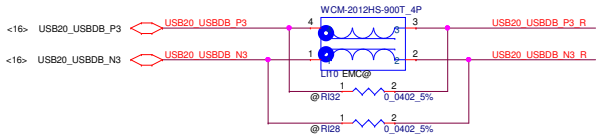
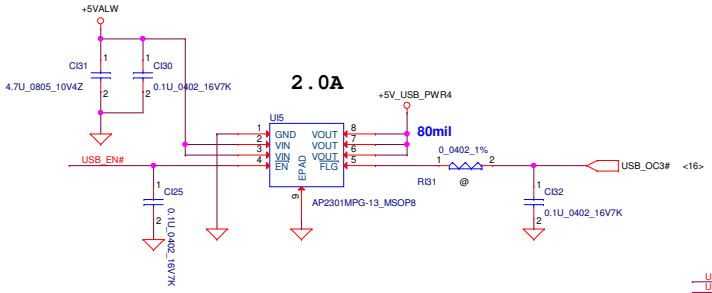


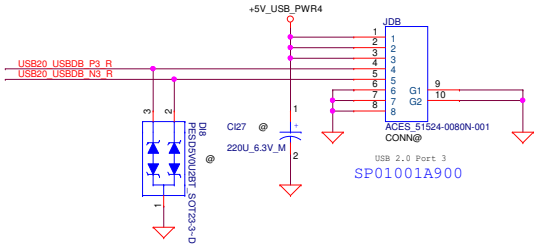
USB conn.3







USB conn.4



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Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.	
Title	MB to USB2.0 DB
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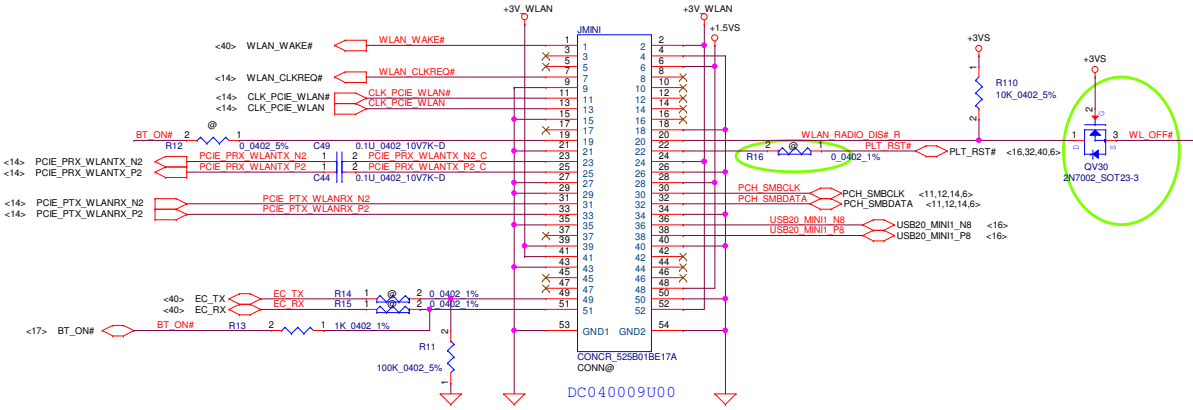
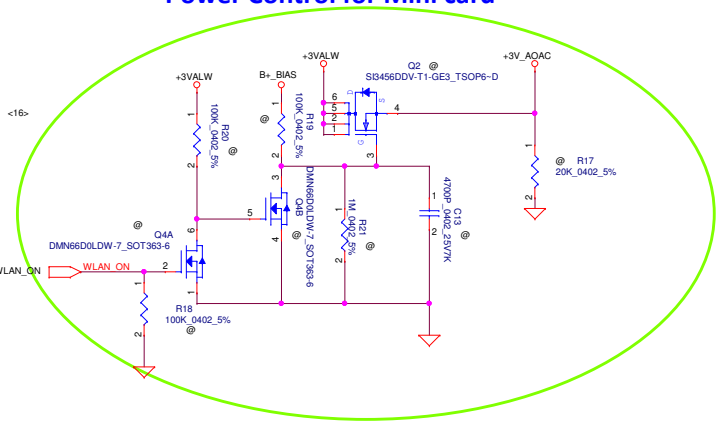
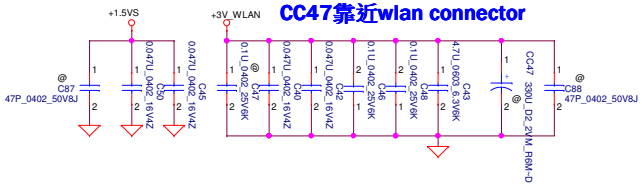
Mini WLAN/WIMAX H=6.7

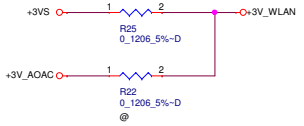


Power Control for Mini card

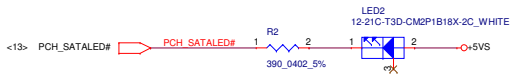


CC47靠近wlan connector

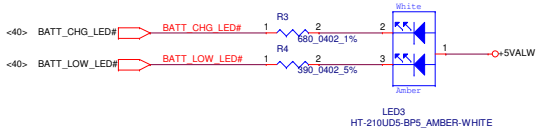




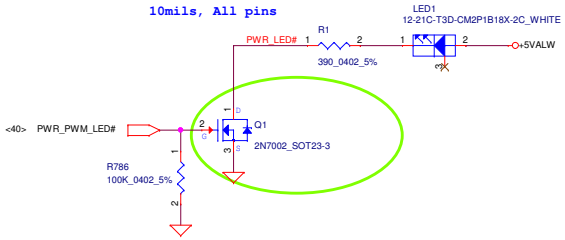
HDD LED



Battery LED



Power LED



Wireless LED

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Mini Card/LED

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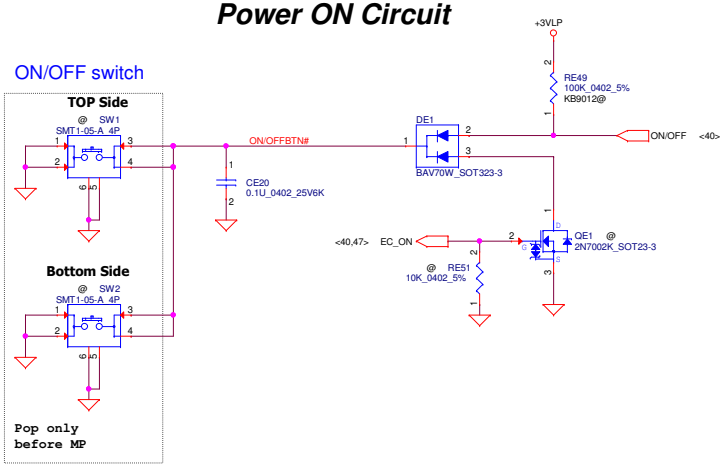
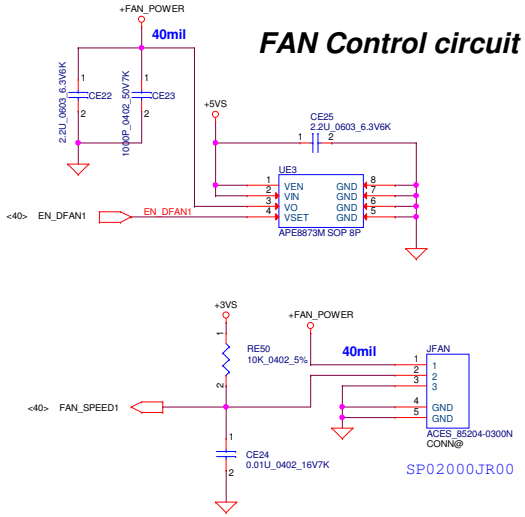
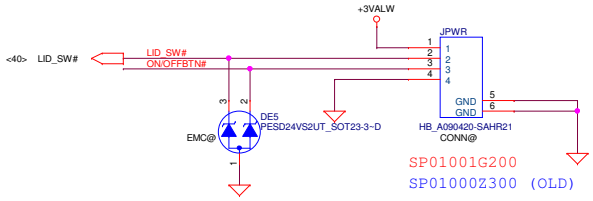
Power ON Circuit



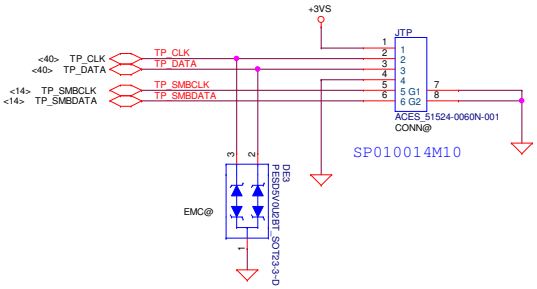
FAN Control circuit



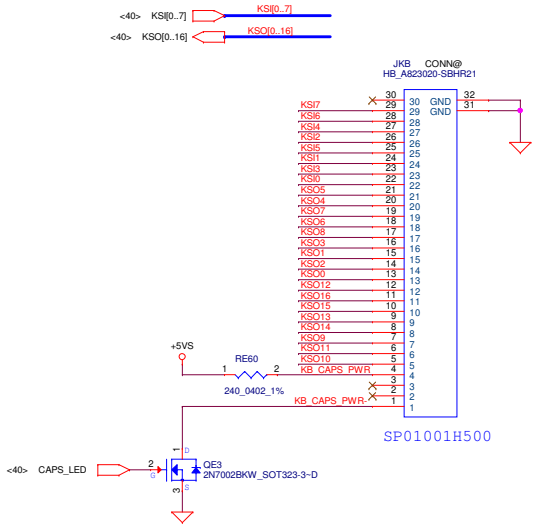
POWER/B



Touch pad



INT_KBD Conn.



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Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.			
Title	FAN/TP/KB/PWR SW		
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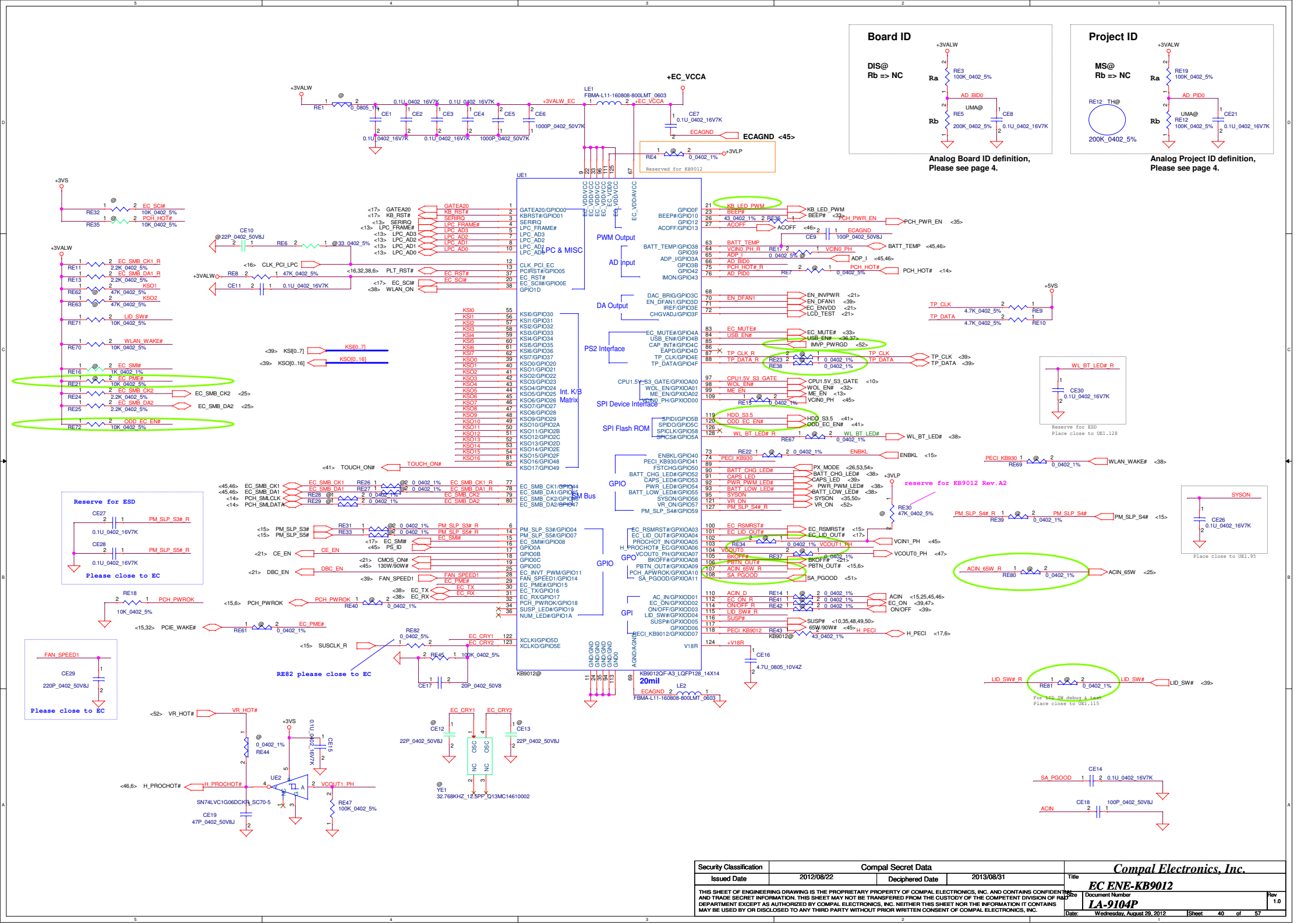
Board ID
DIS@
Rb => NC
Analog Board ID definition,
Please see page 4.
Project ID
MS@
Rb => NC
200K_0402_5%
Analog Project ID definition,
Please see page 4.
+EC_VCCA
ECAGND <45>
UE1
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
GPO
GPI
PC & MISC
SM Bus
KB9012@
KB9012QF-A3_LQFP128_14X14
20mil
reserve for KB9012 Rev.A2
Reserve for ESD
Please close to EC
RE82 please close to EC
Please close to EC
Reserve for ESD
Place close to UE1.128
Place close to UE1.95
For LID SW debug & test
Place close to UE1.115
SN74LVC1G06DCKR_SC70-5
32.768KHZ_12.5PF_Q13MC14610002
Security Classification
Compal Secret Data
Issued Date
2012/08/22
Deciphered Date
2013/08/31
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EC ENE-KB9012
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Document Number
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1.0
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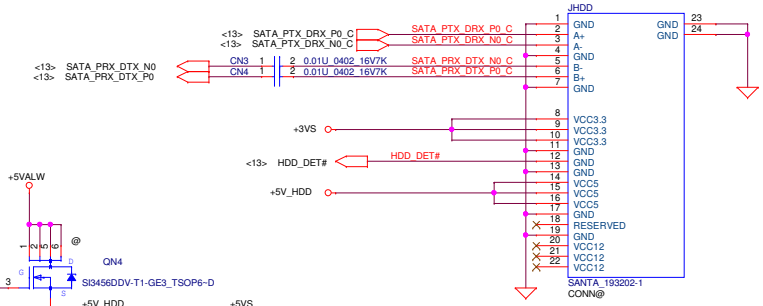
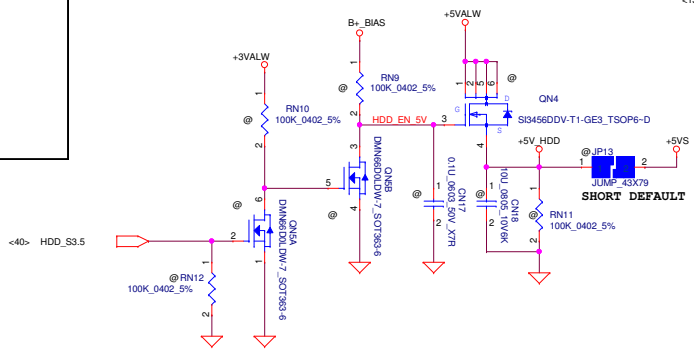
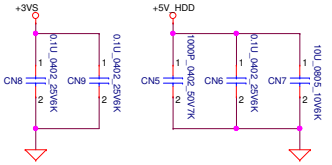
SATA HDD Conn.

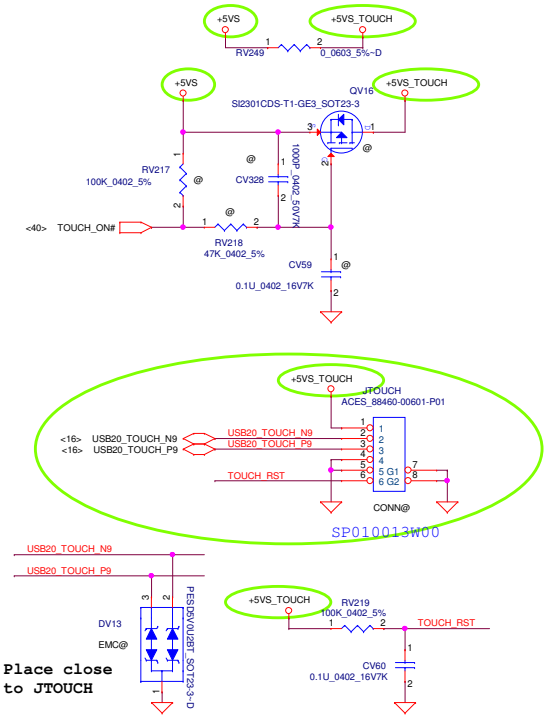


+5V_HDD Source

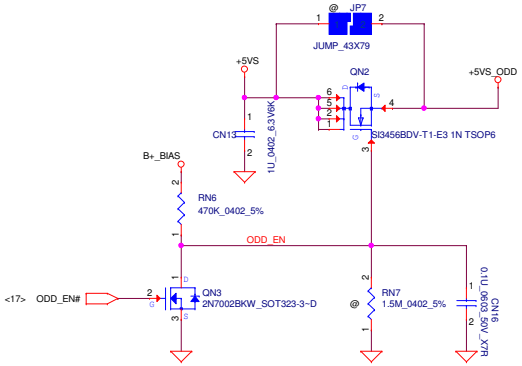


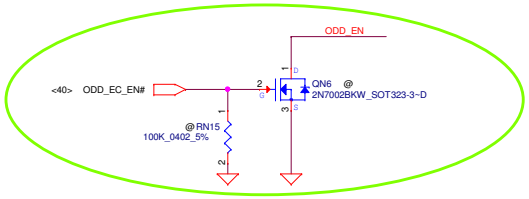


* Touch Screen Panel

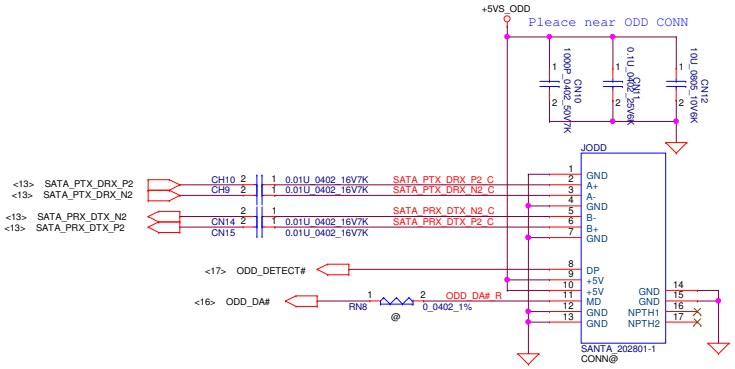


ODD Power Control





SATA ODD Conn.



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Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: HDD / ODD

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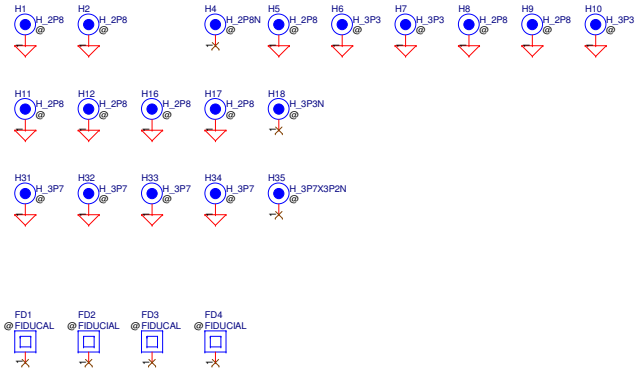
Screw Hole



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: Screw Hole

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Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	21,39	LVDS	2012/05/17	SED	Add FHD Panel CE_ENABLE, DBC_ENABLE function from SED request	Add CE_EN, DBC_EN control pin to EC	0.2
2	21	LVDS	2012/05/22	SED	Follow SED team request disable CE_EN function	Change RV62 to DE-POP and RV100 to POP for disable CE_EN function	0.2
3	33	Audio codec	2012/05/23	CODEC	Follow CODEC vendor suggestion	Add AUDIO JACK PLUG delay circuit, Spearate NET JACK_PLUG to => JACK_SENSE# & => JACK_PLUG#	0.2
4	16,21	Touch Screen	2012/05/29	HW	Add touch screen function	Add RV217, RV218, RV219, RV249, CV59, CV60, CV328, DV13, QV16, JTOUCH	0.2
5	39	Board ID	2012/05/30	HW	Board ID change for PT	Change RE5 from 8.2k_0402(SD028820180) to 33k_0402(SD028330280)	0.2
6	21,39	Touch Screen	2012/05/30	HW	Add touch screen function power control	Add NET "TOUCH_ON#" from JTOUCH to UE1.82(KB9012) for TOUCH SCREEN PANEL power control	0.2
7	33	Audio codec	2012/05/30	HW	Follow RealTek suggestion remove, delete reserve MUTE circuit	Delete D1,QA1,QA2,QA3,RA24,RA26,RA60,RA62,RA68,RA109,CA72,CA73	0.2
8	15,16, 39,41	ESD	2012/05/30	ESD	ESD ask CAP for reserve	Reserve 0.1u/0402 CH104,CZ23,CH105,CE27,CE29	0.2
9	14	Green CLK	2012/05/30	HW	For Green CLK test	Change RH31,RH41,RV232 0ohm form "GCLK@" to "@" for break the clock signal to device	0.2
10	10,26,41	DC/DC	2012/05/31	HW	Change "+1.5V_CPU_VDDQ", "+1.5VS", "+1.5VGS" derating	Change RC150 330K/0402 to 2M/0402, RC151 100K/0402 to 470K/0402, RZ18 100K/0402 to 470K/0402, RV115 0/0402 to 2M/0403	0.2
11	41	DC/DC	2012/05/31	HW	For power sequence trunning	Change RZ15 to DE-POP	0.2
12	06,15,16, 39,41	ESD	2012/05/31	ESD	Follow ESD team request	Change 0.1u/0402 from "@" to POP	0.2
13	32	Green CLK	2012/06/15	HW	Change for Green CLK bom control	Change RL21,RL30 from "@" to "GCLK@"	0.2
14	41	DC/DC	2012/06/15	HW	For WLAN card power sequence issue	Change RZ4,RZ13 from 470K/0402 56K/0403	0.2
15	35,41	Schematic page modify	2012/06/18	HW	Schematic page modify for easily maintain.	Swap Page. 35 & Page 41.	0.2
16	41	ODD	2012/06/18	HW	Change component location for easily maintain.	Move CH9,CH10 from Page.13 to Page.41	0.2
17	39	FAN	2012/06/29	HW	Fan speed noise issue	Reserve 220p/0402 CE24	0.2
18	6	CPU	2012/06/29	ESD	System boot-up shot down issue.	Change CC151 from POP to "@"	0.2
19	21,35, 39,40,41	Circuit adjuest	2012/07/01	HW	Circuit & page adjust for OAK 15" & OAK 17"	1. Swap P.35 & P.41and move touch screen circuit from P.21 to P.41. 2. Swap P.39 & P.40 page no	0.2
20	40	LID SW	2012/07/01	HW	LID SW need a trace for debug and switch.	Add RE81 for LID SW.	0.2
21	25	GPU	2012/07/01	HW	Follow AMD request, MarsPro will used MPLs.	Change RV75,RV76,RV81 from "DIS@" to "TH@"	0.2
22	29	GPU	2012/07/01	HW	Follow AMD request, MEM_CALRP2 is not need for Mars ASIC now.	Change RV205 from "MS@" to "@"	0.2
23	38	MINI card	2012/07/03	HW	Power Control for Mini card didn't need	Change R17 to "@"	0.2
24	6	XDP	2012/07/06	HW	S3 return hang issue	Change RC89 from "@" to POP	0.2
25	23	GREEN CLK	2012/07/09	HW	Follow Green CLK FAE suggestion	1. Change UG1.2(+3VLP) & UG1.8(+3VALW) connect to +LAN_IO 2. Add R787 connect from +RTCBATT to C5.2 & UG1.10 3. Change C14 from 0.1u to 5p/0402 4. Change C8 connect from +3V_ALW to +LAN_IO 5. Add R788 0ohm/0402 from +RTCVCC to UG1 for GCLK & DH1 select	0.2
26	35	MOAT	2012/07/09	ESD	For ESD request reserve CAP.	Reserve those CAP for ESD MOAT.	0.2
27	18	LVDS	2012/07/10	HW	Change RES and reserve CAP for LVDS issue	Change RH185 from 0ohm-short to 0ohm/0805, and reserve CH106 1U/0402	0.2
28	13	PCH	2012/07/11	ESD	Follow ESD team request	Add RH44,RH48,RH70 & NET PCH_JTAG_TMS_R, PCH_JTAG_TDI_R, PCH_JTAG_TDO_R for break signal trace	0.2
29	40	PCH	2012/07/11	ESD	Follow ESD team request	1.Change NET NAME "N59110727" to "WL_BT_LED#_R" 2. Reserve 0.1u/0402 on "WL_BT_LED#_R" for ESD	0.2
30	21	LVDS	2012/07/11	HW	Reserve for CE function for LVDS connector	Change CE_EN_R from dummy to JLVDS.18	0.2
31	32	Connector	2012/07/12	ME	For ME request	Change JLAN CPN from "DC234004V00" to "SP011207090"	0.2
32	40	FAN	2012/07/16	HW	For FAN_SPEED1 noise issue	Change CE29 from "@" to POP	0.2
33	14	Touch PAD	2012/07/17	SED	Change Touch PAD SMBUS port for SMBUS issue	Change Touch PAD SMBUS port for SMB0 to SMB	1.0
34	32	GREEN CLK	2012/07/19	HW	Follow Silego FAE request	Change RL21 from 510 ohm to 0 ohm/0402	1.0
35	41	Touch Screen	2012/08/07	SED	Follow SED team request change JTOUCH USB signal conatct.	Change JTOUCH Pin define.	1.0
36	34	Card Reader	2012/08/14	ESD	Follow ESD team request	Reserve CR11 100p/0402 close to JREAD	1.0
37	23	GREEN CLK	2012/08/16	HW	Fixed GCLK output abnormal issue	Change UG1.2(UG1/VDD) from +LAN_IO to+3VALW	1.0
38	33	CODEC	2012/08/16	HW	The issue already fixed by new CODEC.	Remove delay circuit and POP RA4	1.0
39	23	GREEN CLK	2012/08/17	HW	For RTC discharge issue	De-pop R788	1.0
40	32,34	LAN	2012/08/17	HW	For LAN Chip abnormal leakage issue	Pop RL34 and de-pop RE21	1.0
41	34	Card Reader	2012/08/20	ESD	Follow ESD team request	Change CR11 from 100p/0402 to 10p/0402 and POP	1.0

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Title: HW-PIR

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Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
42	41	Touch Screen	2012/08/20	SED	Follow SED team request	Change Touch screen power rail for +3VS to +5VS	1.0
43	38	LED	2012/08/20	HW	Change LED light	Change LED1,LED2,LED4 CPN from SC500006O00 to SC50000DC00	1.0
44	38	WLAN	2012/08/20	HW	Remove AOAC function power control	Change R18,R19,R20,R21,C13,Q2,Q4 component BOM structure to "@"	1.0
45	41	Touch Screen	2012/08/20	HW	Add EC control for Touch Screen function	Add RN15 & QN6 and relative circuit connect	1.0
46	40	BATMAN2	2012/08/21	HW	For BATMAN2	Add RE82 0ohm/0402 between trace SUSCLK_R & EC_CRY2	1.0
47	14,17	PCH	2012/08/21	HW	For SYSTEM S3 leakage issue	Change RH79.2 & RH245.2 connect from +3V_PCH to +3VS	1.0

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Title: HW-PIR

Size | Document Number: LA-9104P | Rev: 1.0

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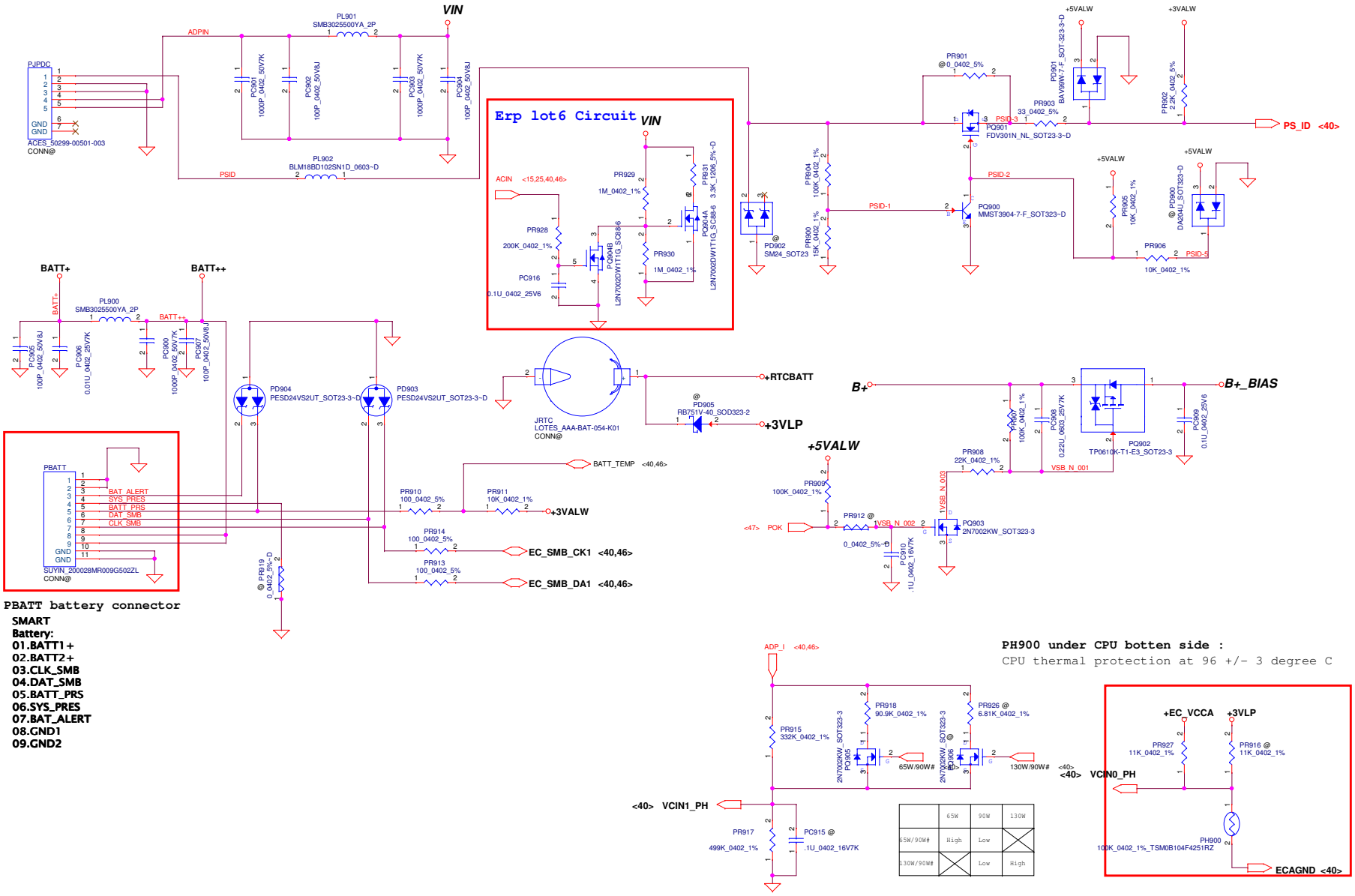

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.			
Title	PWR_DCIN/BATT CONN/OTP		
Size	Document Number		Rev
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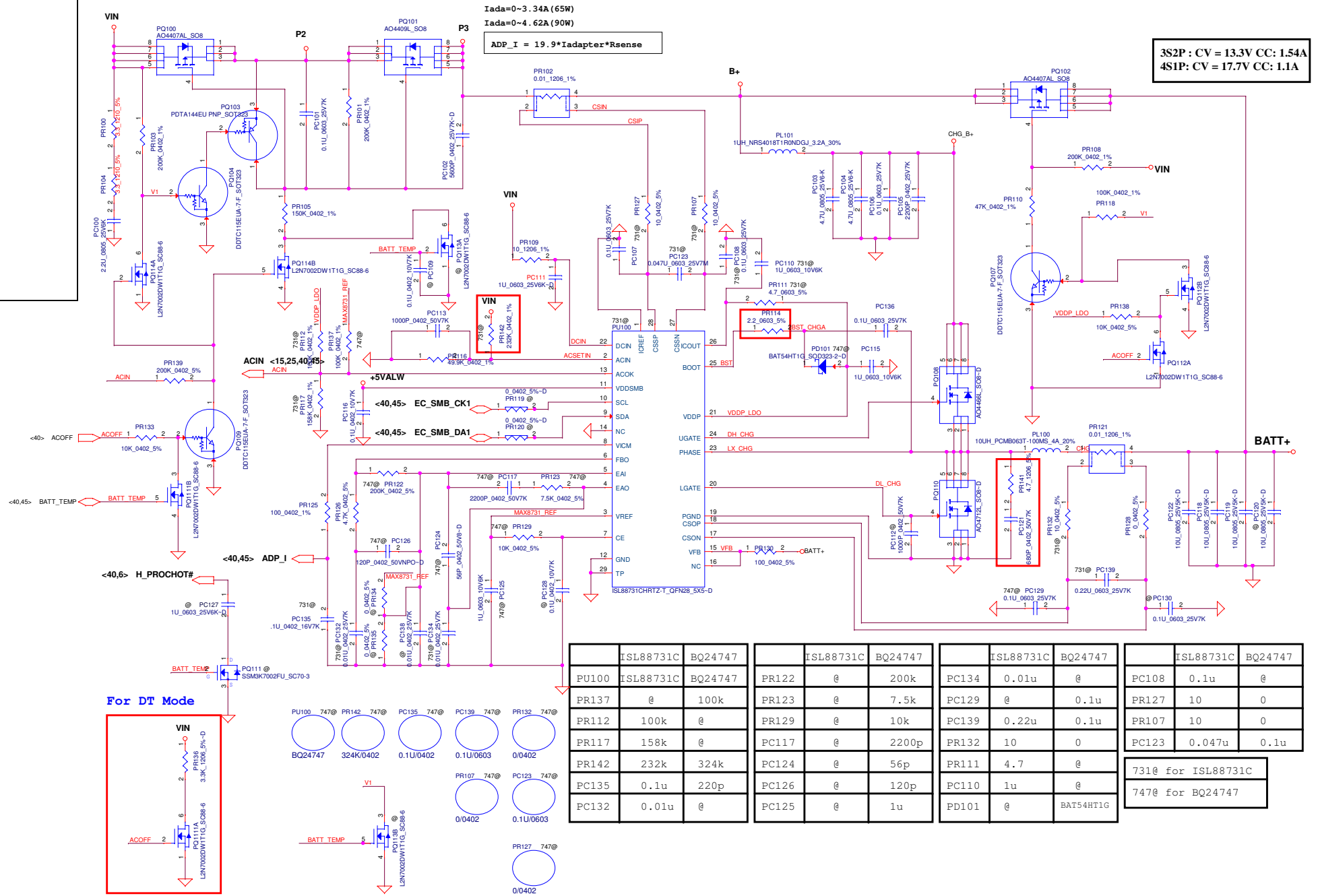

	ISL88731C	BQ24747
PU100	ISL88731C	BQ24747
PR137	@	100k
PR112	100k	@
PR117	158k	@
PR142	232k	324k
PC135	0.1u	220p
PC132	0.01u	@

	ISL88731C	BQ24747
PR122	@	200k
PR123	@	7.5k
PR129	@	10k
PC117	@	2200p
PC124	@	56p
PC126	@	120p
PC125	@	1u

	ISL88731C	BQ24747
PC134	0.01u	@
PC129	@	0.1u
PC139	0.22u	0.1u
PR132	10	0
PR111	4.7	@
PC110	1u	@
PD101	@	BAT54HT1G

	ISL88731C	BQ24747
PC108	0.1u	@
PR127	10	0
PR107	10	0
PC123	0.047u	0.1u

731@ for ISL88731C
747@ for BQ24747

Security Classification	Compal Secret Data	
Issued Date	2012/08/22	Deciphered Date 2013/08/31

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Title: PWR_CHARGER

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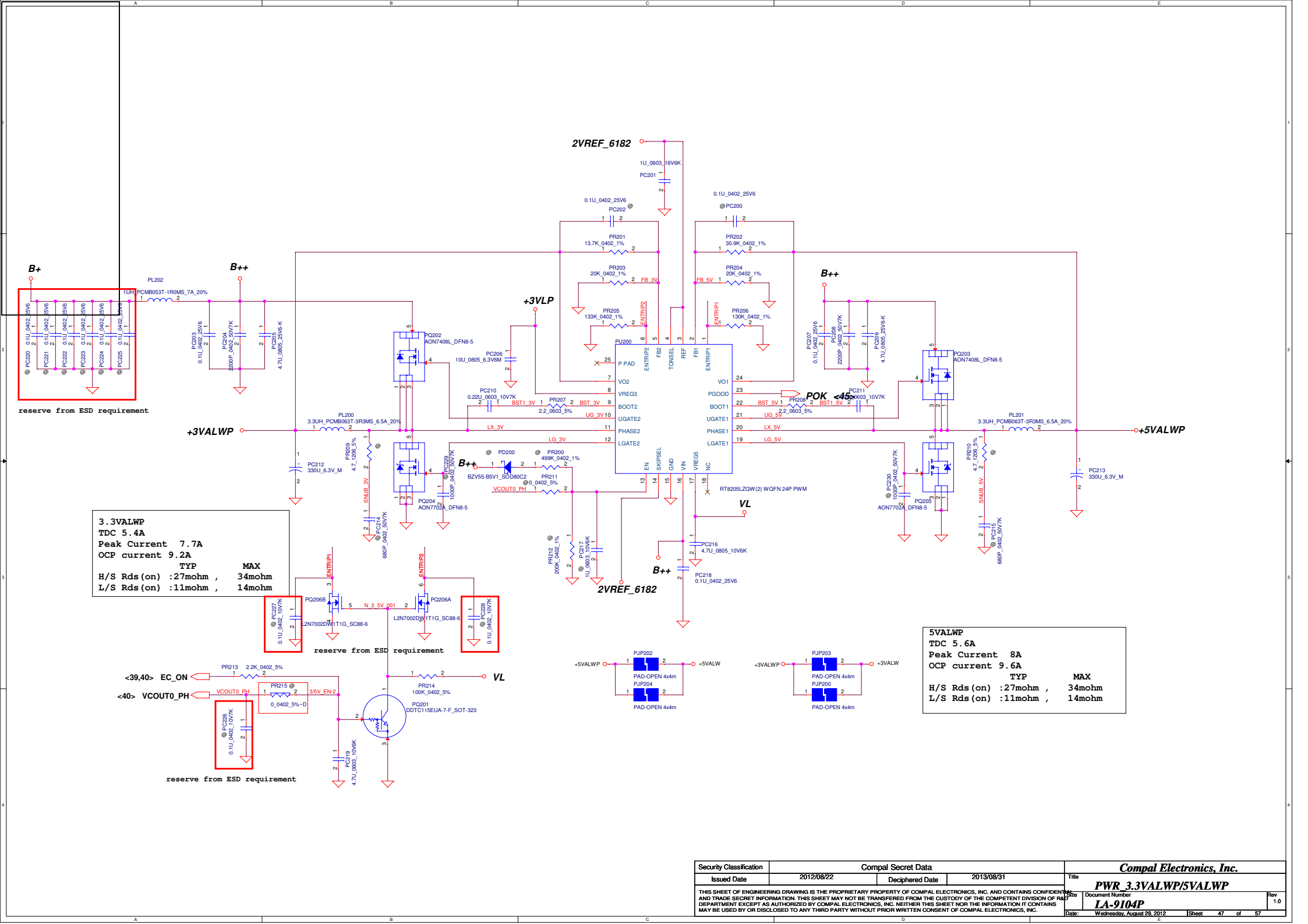

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

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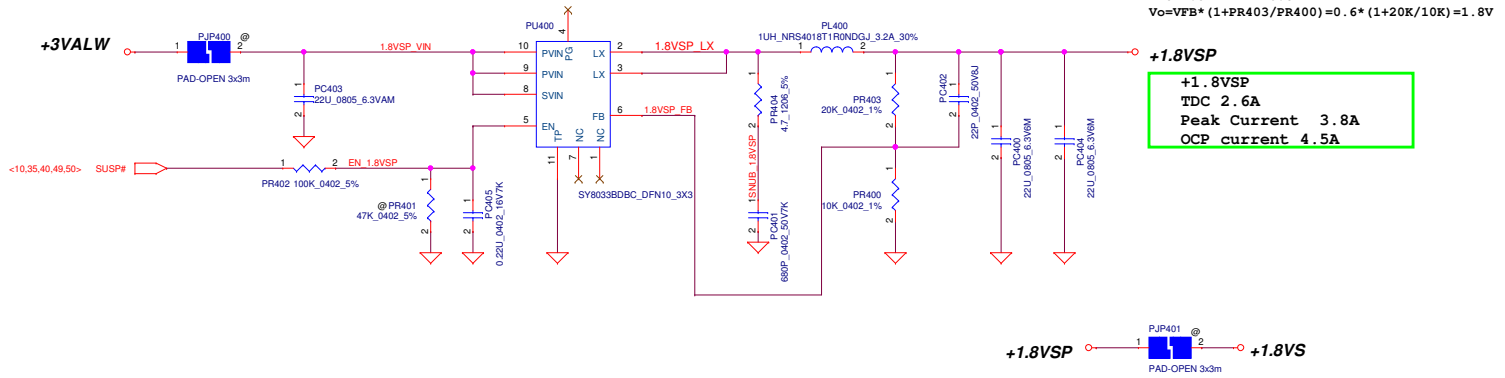

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Issued Date	2012/08/22	Deciphered Date	2013/08/31

Title	PWR_1.8VSP		
Size	Document Number		Rev
	LA-9104P		1.0
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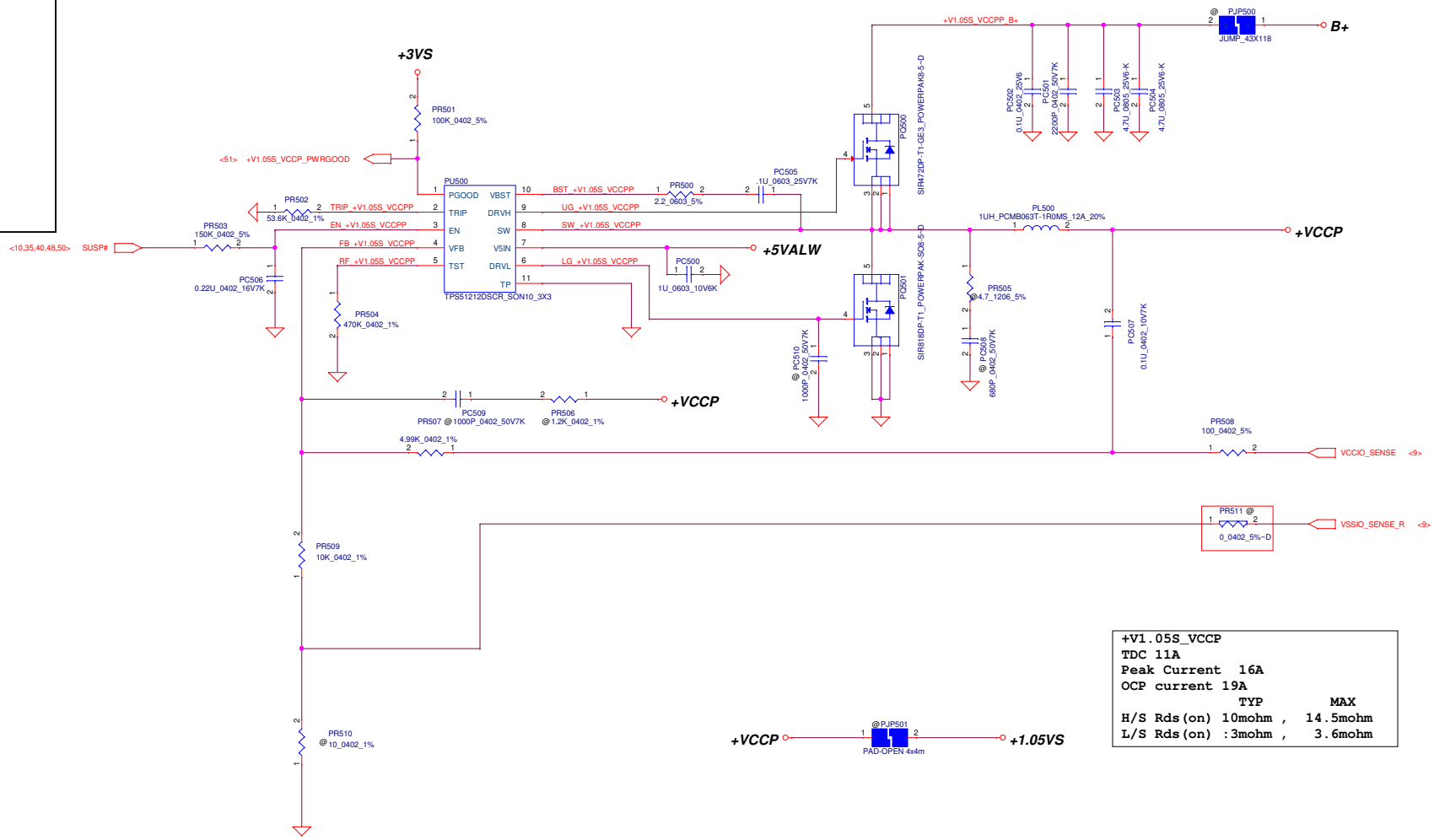

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.			
Title: PWR_+VCCIO			
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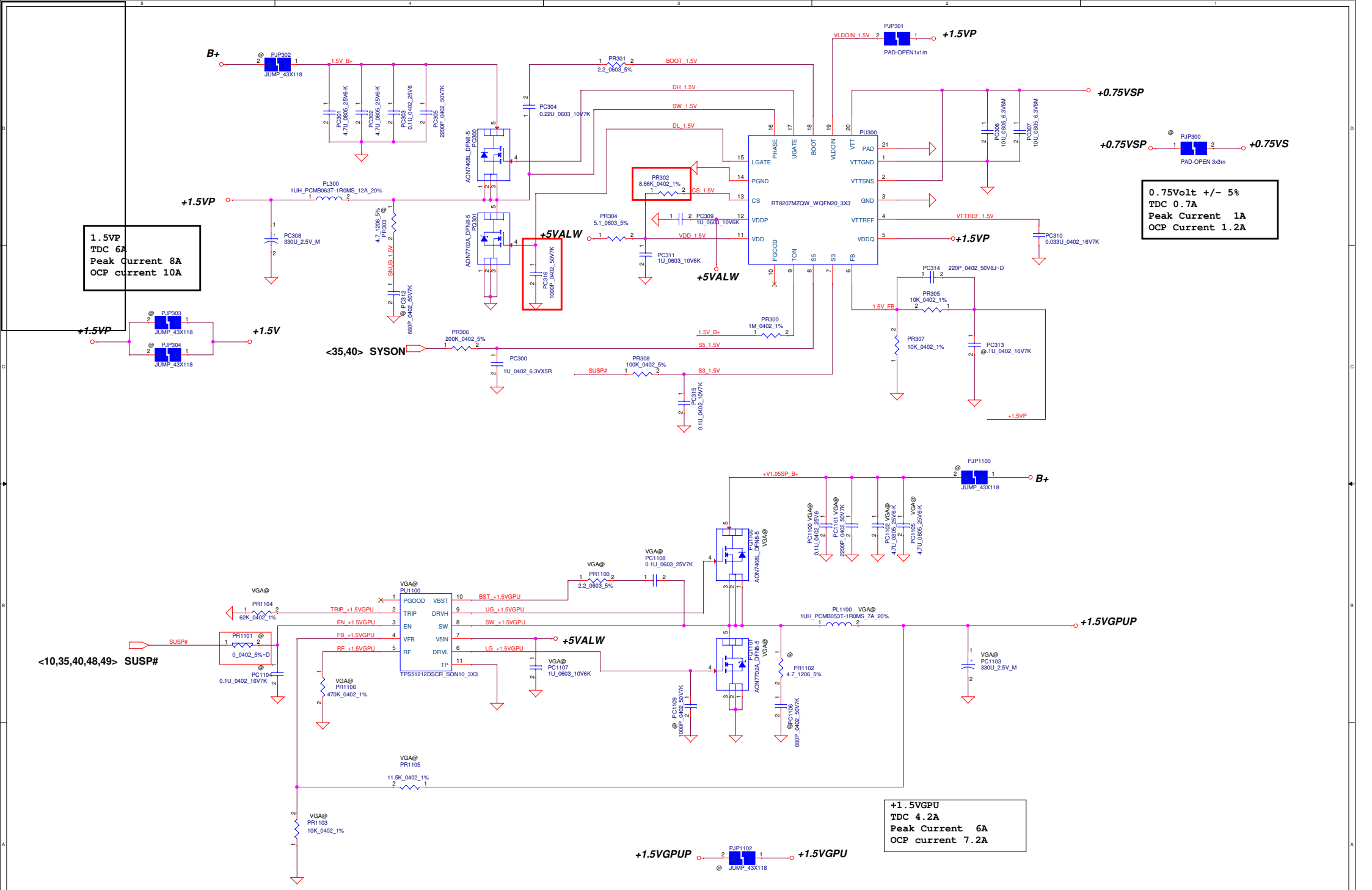

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: PWR_+1.5VP/+1.5VGPUP/0.75VSP

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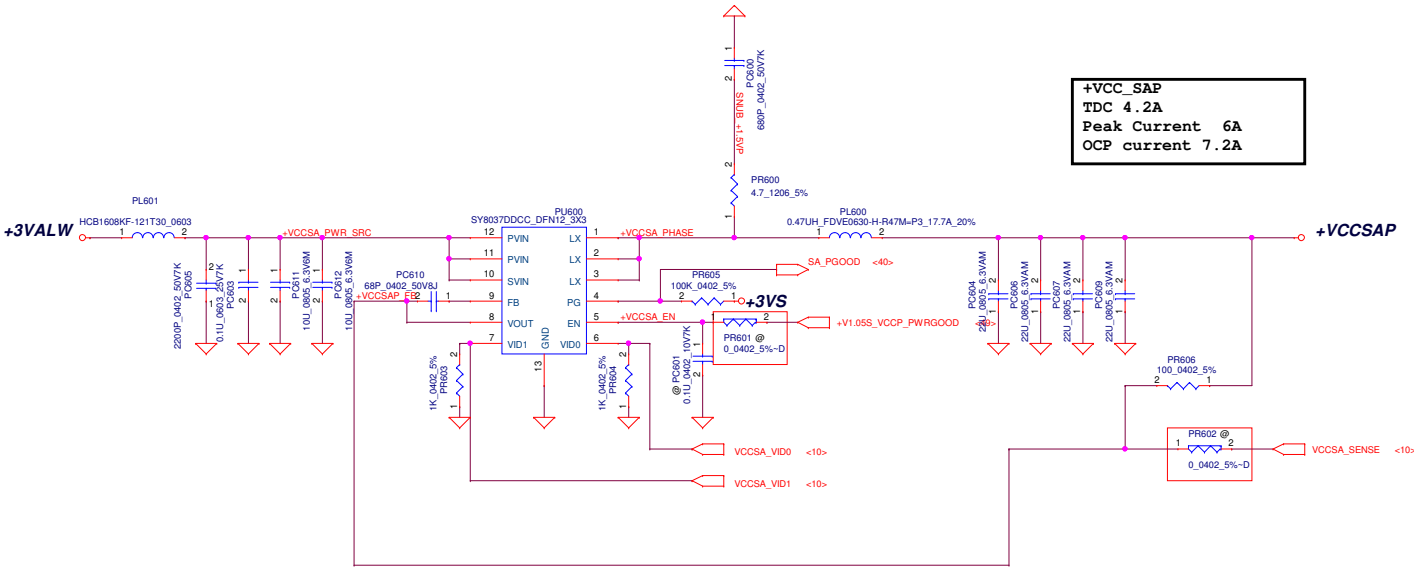
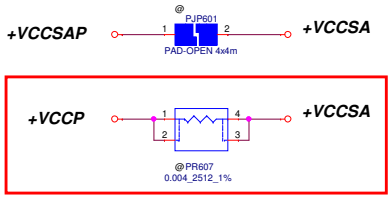
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A



The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



reserve for Pentium and Celeron only

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: PWR_+VCCSAP

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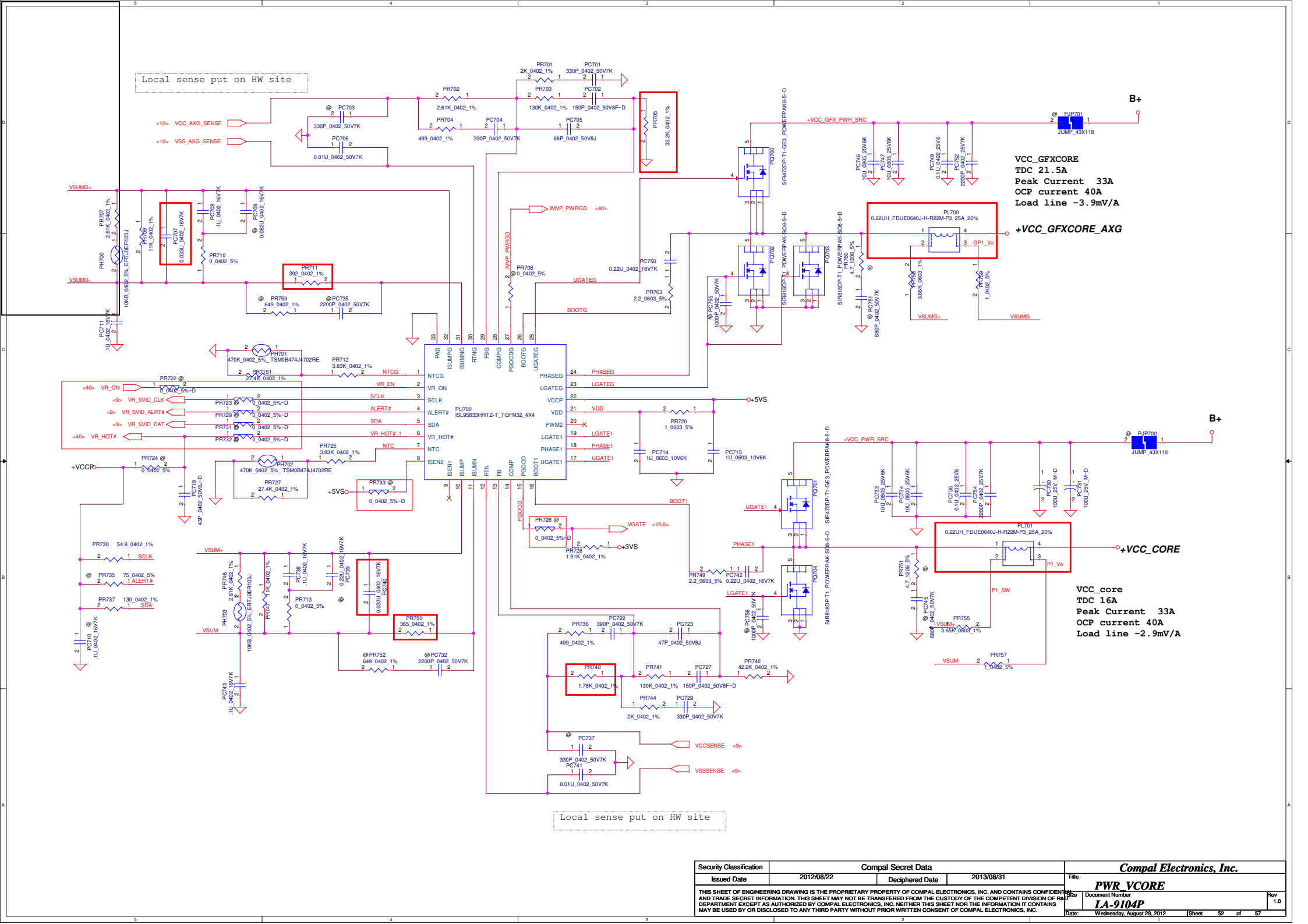

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: PWR_VCORE

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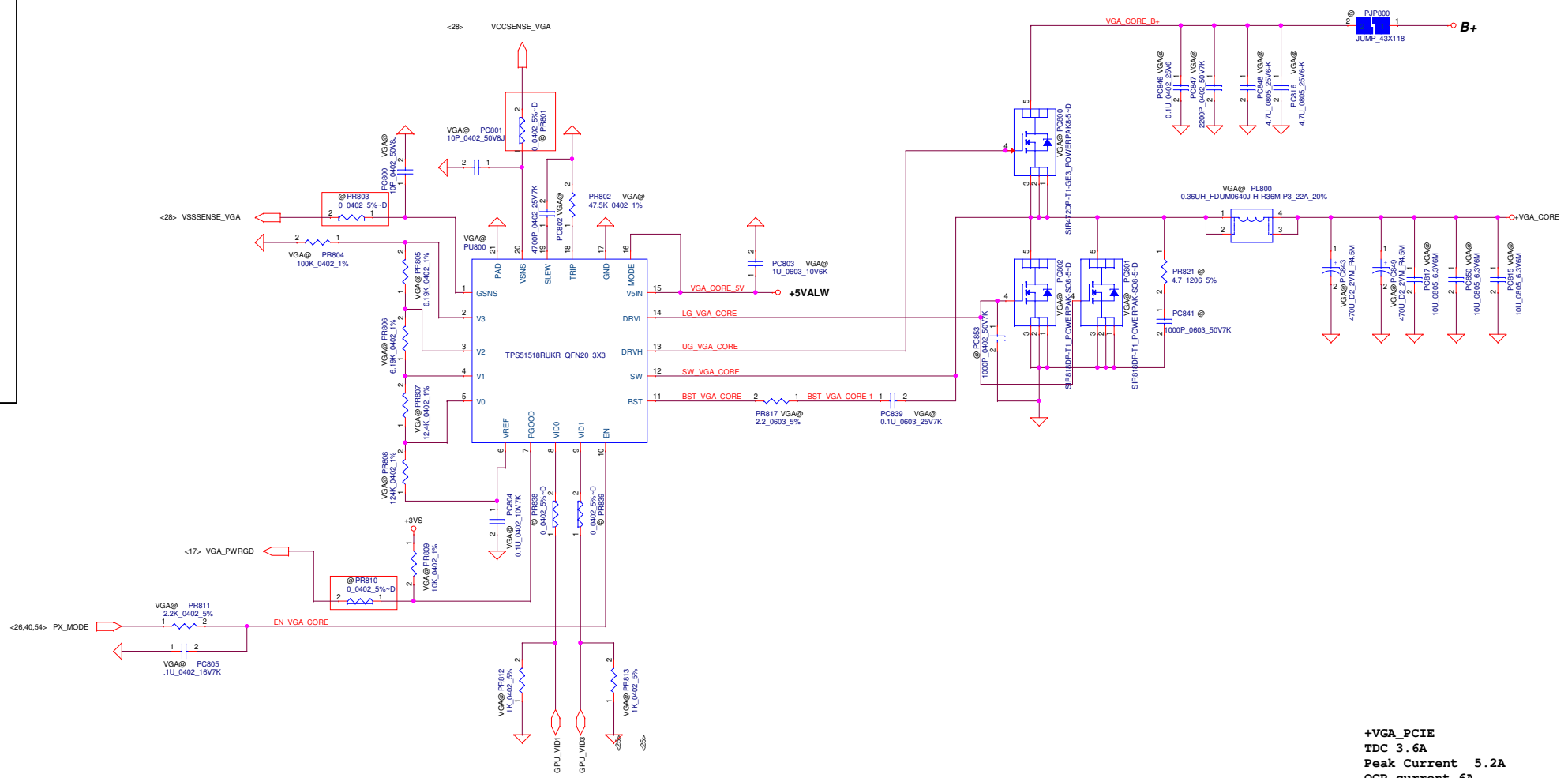
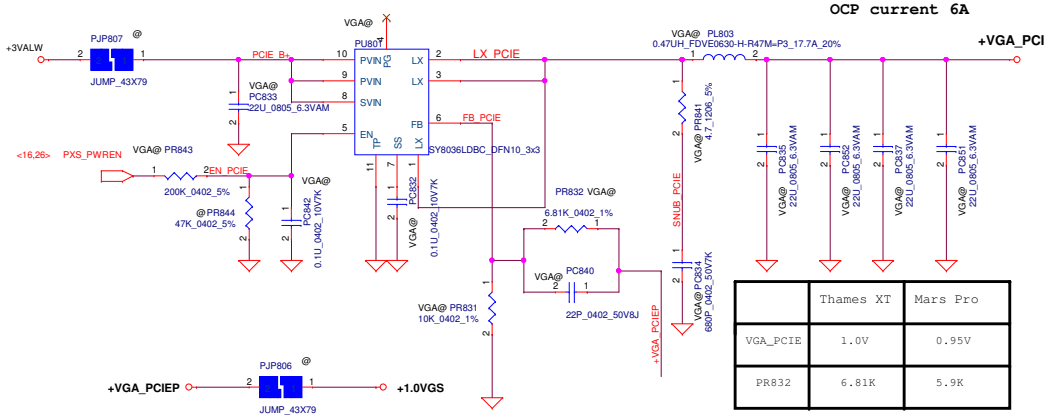


Thames XT

GPU_VID3 (GPIO15)	GPU_VID1 (GPIO20)	Core Voltage Level
1	1	0.8V
1	0	0.85V
0	1	0.9V
0	0	1.0V

+VGA_CORE
TDC 20A
Peak Current 30A
OCP current 36A
FSW=350kHz
DCR 1.4mohm +/-5%



+VGA_PCIE
TDC 3.6A
Peak Current 5.2A
OCP current 6A

	Thames XT	Mars Pro
VGA_PCIE	1.0V	0.95V
PR832	6.81K	5.9K

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: PWR_VGA_CORE/VGA_PCIE

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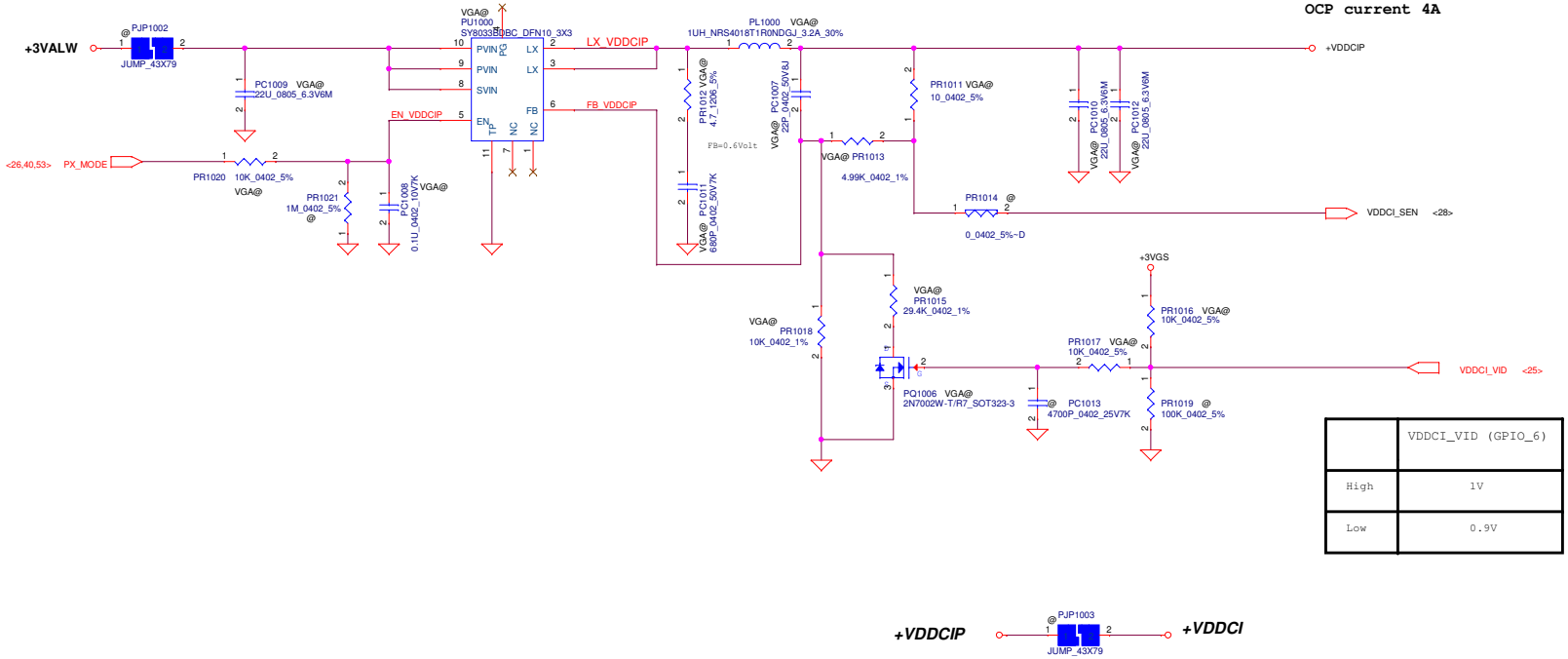
+VDDCI
TDC 2.2A
Peak Current 2.2A
OCP current 4A



	VDDCI_VID (GPIO_6)
High	1V
Low	0.9V

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Issued Date	2012/08/22	Deciphered Date	2013/08/31

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Title: PWR_+VDDCIP

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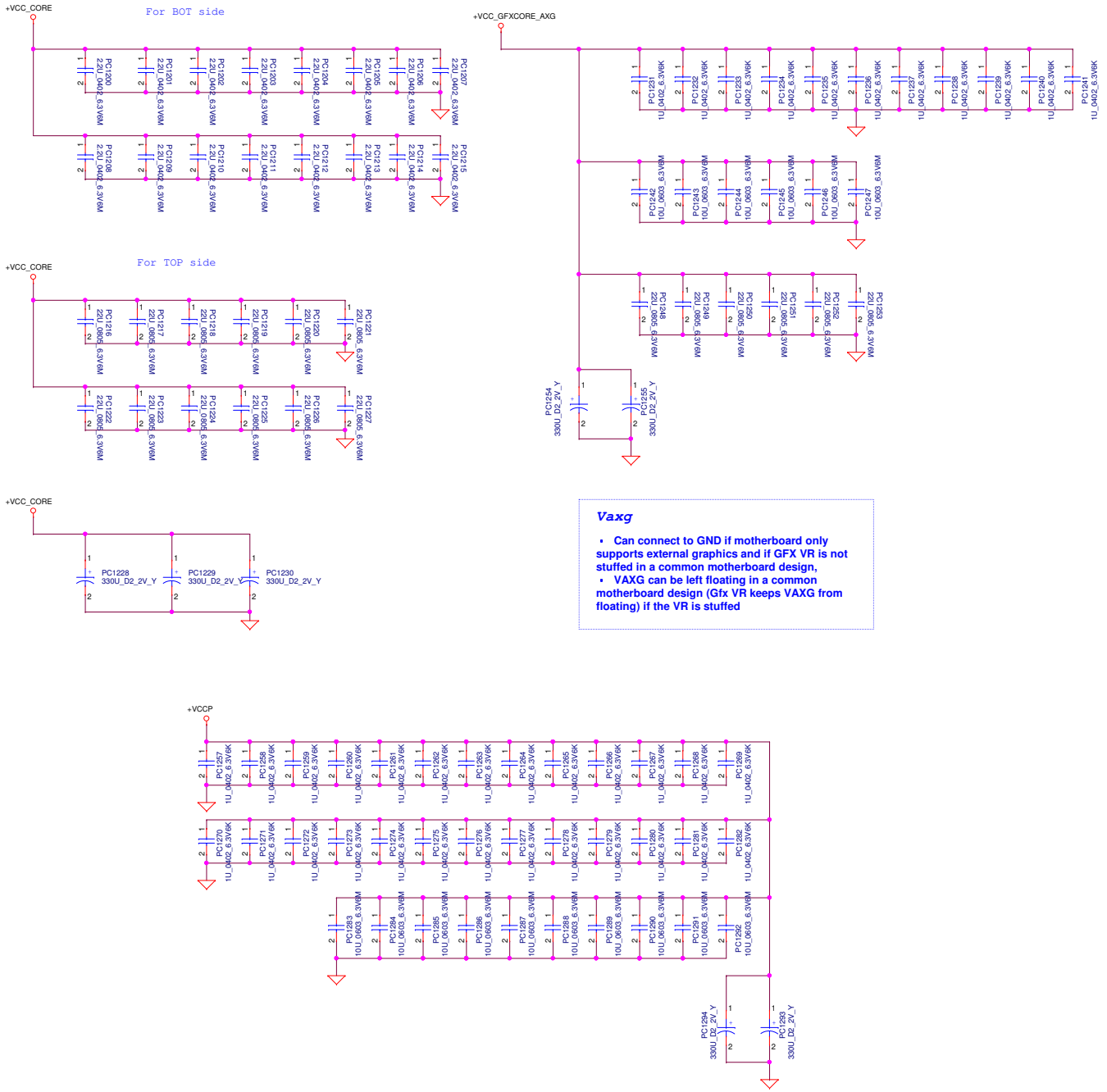

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: **PWR_PROCESSOR DECOUPLING**

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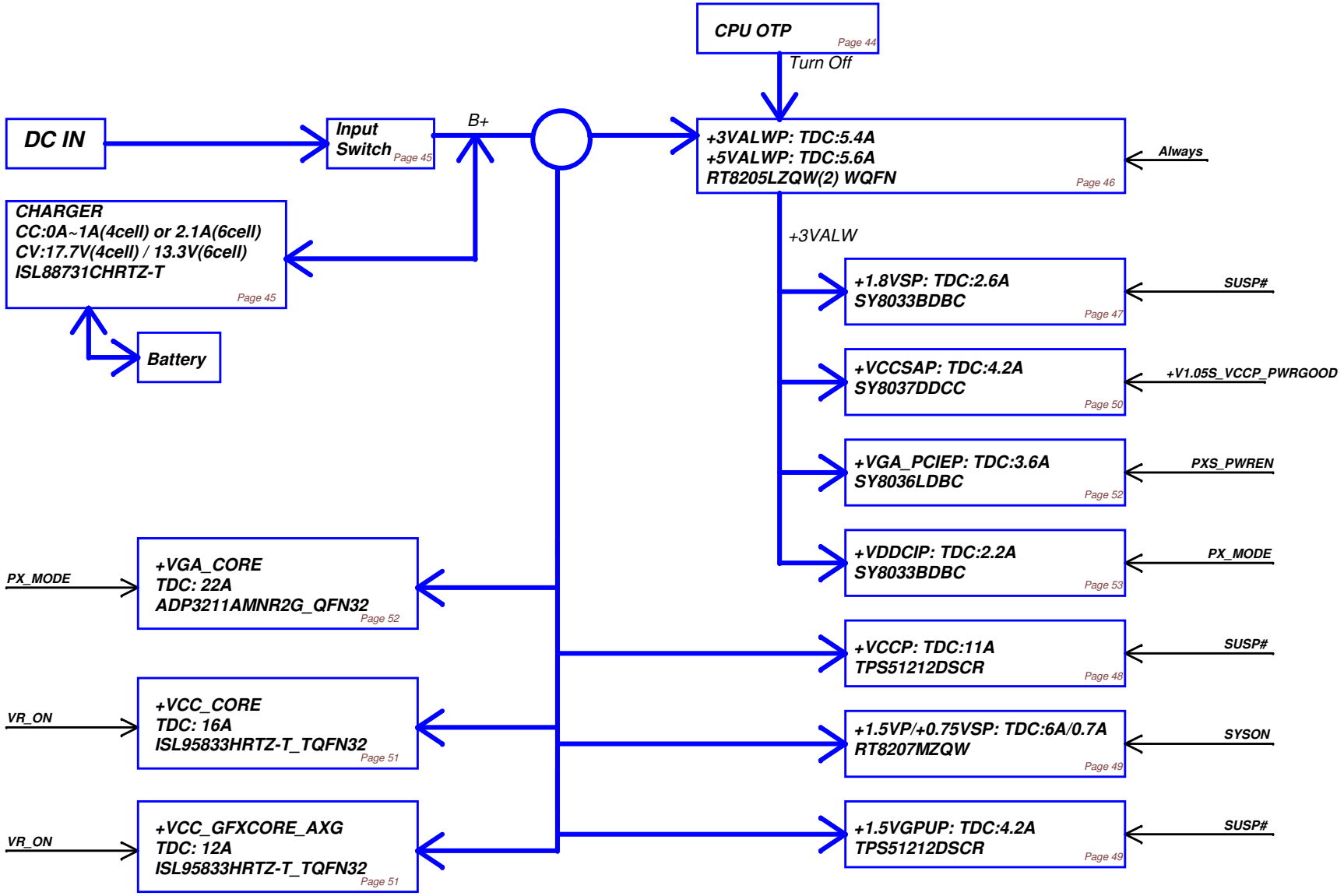
Power block



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.			
Title: PWR_POWER BLOCK DIAGRAM			
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	51	VCORE	12/05/11	Morris	adjust VR parameter	change PL700 and PL701 from 0.36u to 0.22u change PC707 and PC740 from 0.047u to 0.033u change PR750 from 649 to 365 change PR711 from 649 to 392 change PR740 from 1.91k to 1.78k change PR705 from 150k to 33.2k	X00
2	44 45 46	DCIN/BATT CONN/OTP CHARGER 3.3VALWP/5VALWP	12/05/11	Morris	follow SSI memo for part shortage issue	change PQ112,PQ114,PQ1111,PQ206,PQ904 from SB00000CQ00 to SB00000PV00	X00
3	49	+1.5VP/1.5VDGPU/0.75VSP	12/05/15	Morris	design change	change PR302 from 12k to 8.66k	X00
4	50	+VCCSAP	12/05/23	Morris	for Pentium and Celeron special BOM	add PR607 and reserve	X00
5	49	+1.5VP/1.5VDGPU/0.75VSP	12/07/06	Morris	design change to reduce low-side mosfet induce	add PC316 1000pf	X01
6	45	CHARGER	12/07/17	Morris	from EMI request	change PR114 from 0 to 2.2 add PR141 and PC121	X01
7	45	CHARGER	12/07/17	Morris	design change to solve Battery LED is still on after unplug AC when SUT in S3S4S5 issue	change PR142 from 210k to 232k for ISL88731C (X76) change PR142 from 309k to 324k for BQ24747 (X76)	X01
8	44	DCIN/BATT CONN/OTP	12/07/17	Morris	revise OTP setting to 96C from thermal request	change PR927 from 12.1k to 11k	X01

Compal Electronics, Inc.		
Title: PWR-PIR		
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