Data Sheet

BIT3715

High Performance PWM Controller

Preliminary
Version: 0.00

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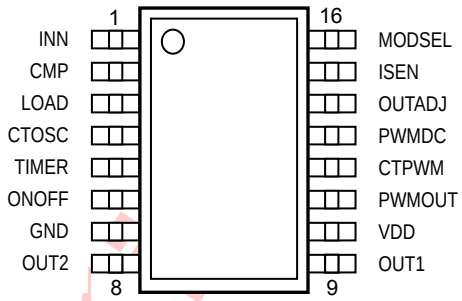
Features:

- **Near Zero Stand By Current**
- **4.5V ~ 8.0V operation**
- **Fixed High Frequency,**
  Voltage Mode PWM Control Topology
- **Latched Off Protection**
- **Build-In 2nd Low Frequency PWM Generator**
- **Build-In UVLO**
- **Low Power CMOS Process**
- **Totem Pole Output**
- **16 Pin Package**

Pin Layout:



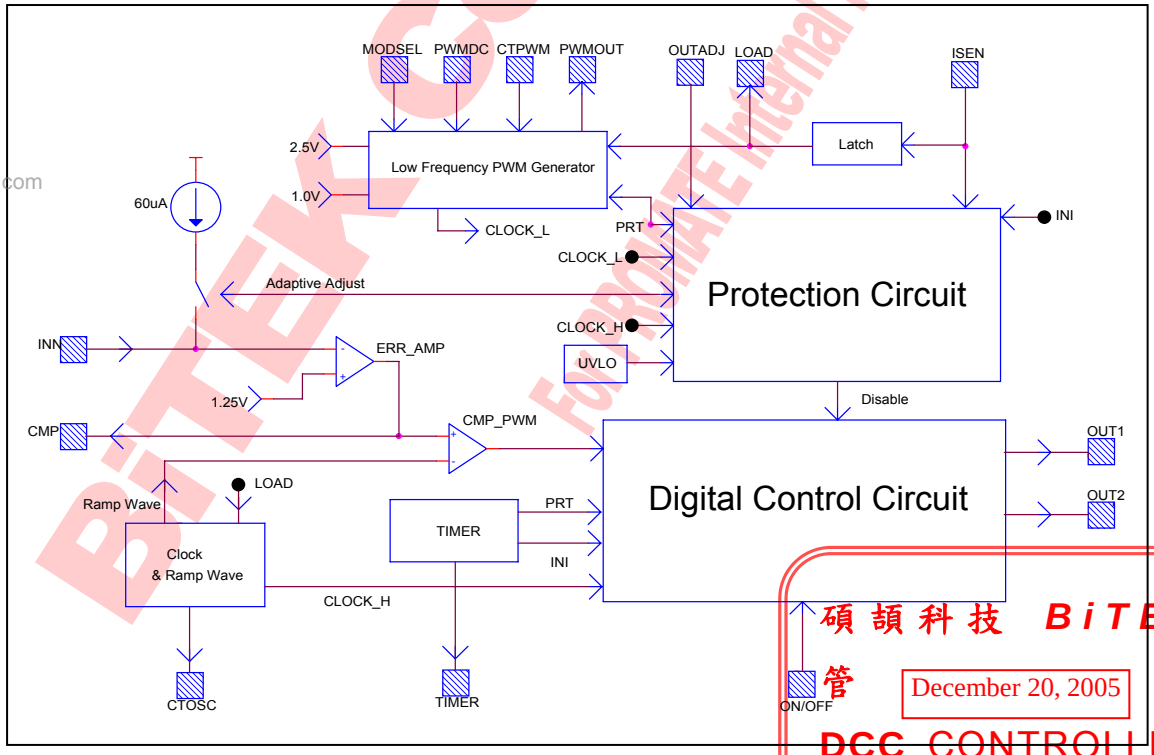
General Description:

BIT3715 integrated circuit provides the essential PWM features for DC/DC conversion purpose in a small low cost 16-pin package. Another built-in low frequency PWM generator provides user more flexible applications. BIT3715 provides latched off protection feature may make the system more reliable. CMOS process makes BIT3715 consumes less power while comparing to conventional bipolar products.

Recommended Operating Condition:

Supply Voltage……4.5 ~ 8.0V
Operating Ambient Temperature……..-20 ~ 85 ℃
Operating Frequency……50K ~ 400K Hz

Functional Block Diagram:



Pin Description:

Table 1

Pin No.	Symbol	I/O	Descriptions
1	INN	I	The inverting input of the error amplifier.
2	CMP	O	Output of the error amplifier.
3	LOAD	I/O	A switch that connected to the high frequency triangle wave generator. This switch is open while the voltage level of ISEN pin is lower than 1.3V. An external resistor connected here may change the operation frequency of CTOSC in open load situation.
4	CTOSC	I/O	An external capacitor connected here decides the frequency of high frequency PWM controller.
5	TIMER	I/O	With internal reference current and an external capacitor connected here, it decides the required period of starting and the timing of initialization. The controller is forced to the reset mode while the voltage level of TIMER is lower than 0.3V. During reset mode, the current about 60uA will flow into the INN pin to reduce the output level of the error amplifier CMP to turn off the controller. The protection function will be enabled after this node is charged to exceed 2.5V. The output current of this pin is 20uA when the level of TIMER is lower than 0.3V. The output current becomes 1uA when the level of TIMER is higher than 0.3V
6	ONOFF	I	The control pin of turning on or off the IC. 1V threshold with an internal 80K± 15% ohm pull-low resistor.
7	GND	I/O	The ground pin of the device.
8	OUT1	O	The active high output driver.
9	OUT2	O	The active low output driver.
10	VDD	I	The power supplies pin of the device.
11	PWMOUT	O	The output pin of low frequency PWM generator. A 2.5V or floating two state output is provided through this pin. The internal circuit limits the max. Duty-cycle to about 92%.
12	CTPWM	I/O	With the internal reference current and an external capacitor connected here can set the operation frequency of low frequency PWM generator with 1.0V ~ 2.5V triangle wave output.
13	PWMDC	I	Low frequency PWM controlling input. A PWM output comes out by comparing this DC input and the 1.0 ~ 2.5V triangle wave that is generated by CTPWM.
14	OUTADJ	I	Output regulation and protection. If a > 2.0 V voltage is detected. A ~ 60uA current will flow into the INN pin to adjust the output of the error amplifier pin CMP to regulate the output voltage.
15	ISEN	I	Load current detection pin, the open load situation is detected if a less than 1.3V input is sensed.
16	MODSEL	O	To set the output polarity of the low frequency PWM generator.

Functional Description:

The Power On Initialization: BIT3715 is in an "initial state" when TIMER pin voltage is less than 0.3V. An internal current source charges the external capacitor connected on TIMER pin determines the operation timing of BIT3715. This current provides about 20uA when TIMER pin voltage is less than 0.3V, or about 1uA when TIMER pin voltage is large than 0.3V. Table 2 lists the states of each key features during TIMER pin voltage is less than 0.3V.

Table 2 BIT3715 initial states

Pin Number	Pin Name	Status
4	CTOSC	Normally run
8	OUT1	Forced to GND level
9	OUT2	Forced to VDD level
11	PWMOUT	Floating
12	CTPWM	Normally run

To Set the Operation Frequency of the 1st High Frequency PWM Controller: An external capacitor C_{CTOSC} pin CTOSC determines the frequency as equation (1)

The frequency of the 1st high frequency PWM controller is:

$$F_{HFPWM} = \frac{K_{HF}}{C_{CTOSC}},\ K_{HF} = 8.2e-5 \quad .....(1)$$

Or a 100KHz operation PWM control system if an 820pF capacitor is connected to pin CTOSC. Equation (1) is valid only when VDD=6V, temperature=30ºC and frequency ≈ (80K ~ 120K)Hz. Fig. 1 shows the relationship between the frequency of the high frequency PWM and CTOSC capacitance.

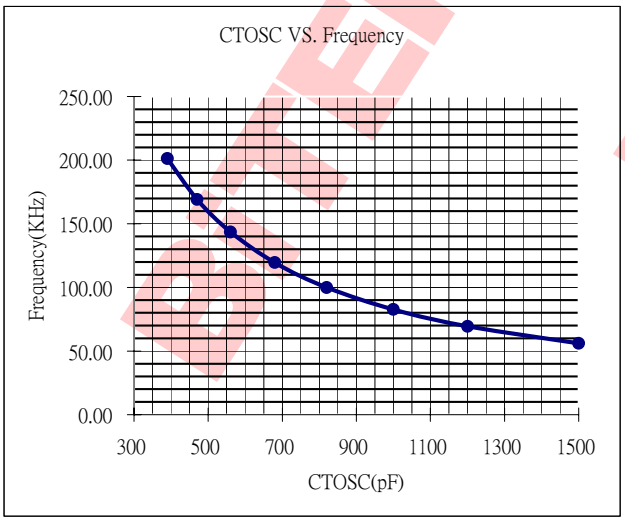


Fig.1

The 1st Latched Off Protection: The ISEN pin may be used for detecting if the operation is controlled stably during normal operation. For most of the applications, to define a "staring period" in which period no power deliver to the load side, are necessary. BIT3715 disable the latched off function when TIMER pin voltage < 2.5V. If "TIMER >2.5V and ISEN < 1.3V" for 32 cycles of the 2nd low frequency PWM, BIT3715 will shut down the output pins, OUT1 and OUT2 until the system is powered on again. The detail is as bellow:

During TIMER > 2.5V, the system operates normally when the ISEN > or < than 1.3V. The lathed off function performs when ISEN has continuously been kept < 1.3V for 32 cycles of the 2nd low frequency PWM.

The Output Adjustment and 2nd Latched Off Protection: The OUTADJ pin may be used for detecting if the PWM control system operates normally. An about 60uA current source will charge the INN pin to adjust the output of CMP while OUTADJ > 2.0V. The latched off abnormal protection performs while TIMER > 2.5V. If "TIMER > 2.5V and OUTADJ > 2.0V" for 32 cycles of the 1st high frequency PWM, BIT3715 will shut down the output pins, OUT1 and OUT2, until the system is powered on again. The detail is as bellow:

During TIMER > 2.5V, the system operates normally when the OUTADJ > or < than 2.0V. The lathed off function performs when OUTADJ has continuously been kept > 2.0V for 32 cycles of the 1st high frequency PWM.

Or, a pulse signal on OUTADJ pin with > 50KHz which may > 2.0V or < 2.0V. BIT3715 performs latched off function when TIMER > 2.5V and the pulse signal has continuously present on OUTADJ pin for 32 cycles of the 1st high frequency PWM.

To Set The Frequency Deviation of High Frequency PWM During Different Loading Condition: A connected between GND and LOAD resistor may increase the operation frequency of CTOSC. An internal switch of the LOAD pin is closed may be used to change the frequency of CTOSC before ISEN had been triggered to larger than 1.3V. In many cases, the resonance frequency of the load is varied while the load is changed. For obtaining the better performance, the operation frequency of the PWM controller must fit to the resonance frequency of the load. The following diagram shows how the load resistance changes the 100KHz operation frequency of CTOSC pin. In above case, CTOSC is connected by an 820pF capacitor. The normal operation frequency of high frequency PWM is 100KHz. If a different frequency says Fn is the set for normal operation. In BIT3715, the internal switch of the LOAD pin is "frozen" to "open" status when the ISEN > 1.3V.

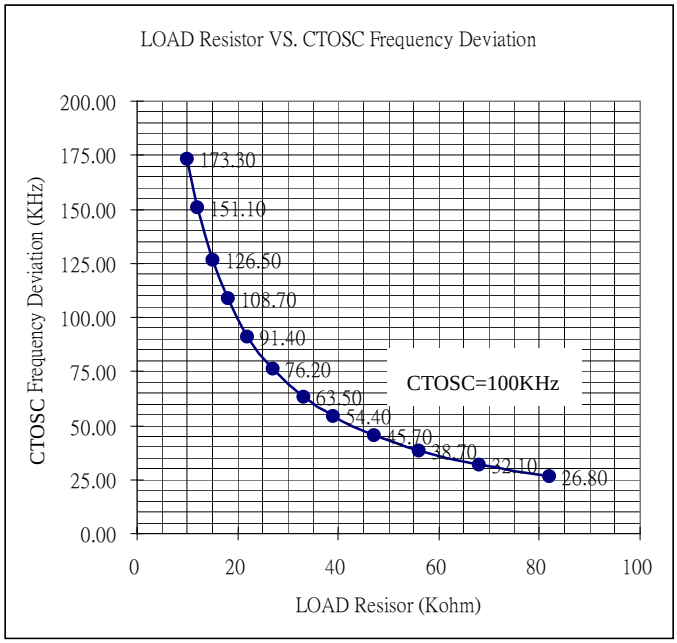


Fig.2

Then the frequency deviation can be calculated as Equation (2)

$$\Delta Fn = \frac{\Delta F100_{KHz} \times F_n}{100KHz} \text{.....(2)}$$

Setting the Frequency of the 2nd Low Frequency PWM Generator: A 2nd internal trimmed low frequency oscillator generates a ± 3% accurate frequency on CTPWM pin with external capacitors. The capacitor values versus operation frequencies are as bellow:

Note: Above equation (3) is valid only when operating frequency is between 150Hz ~ 1.5KHz

The logic high output of pin PWMOUT is made by a 2.5V DC voltage and the floating state makes the logic low

$$F_{LFPWM} = \frac{4512}{[C_{CTPWM} + 0.005]nF} \text{.....(3)}$$

portion. MODSEL pin provides the polarity selection of LF_PWM generator. If MODSEL pin is 0V, a 0% duty cycle is obtained when PWMDC < 1.0V. If this pin is pulled to IC VDD level, 0% duty cycle is obtained while PWMDC> 2.5V.

Note: BIT3715 limits the maximum duty cycle to about 92 %. PWMOUT sends the pulses when ISEN >1.3V or TIMER >2.5V.

UVLO: The under-voltage-lockout circuit turns the output driver off when supply voltage drops too low. Whole system includes the protection and timing circuits are reset (pin TIMER =0) in low VDD state.

DC/AC Characteristics:

Absolute Ratings:

Table 3

Parameter	Symbol	Ratings	Unit	Remarks
Supply Voltage	VDD	-0.3~+ 8.8	V	Ta=25°C
Ground	GND	±0.3	V	
Input pin Voltage		-0.3~ VDD+0.3	V	
Operating Ambit Temperature	Ta	-20 ~ +85	°C	
Operating Junction Temperature		+150	°C	
Storage Temperature		-55~+150	°C	

DC/AC Characteristics

Table 4

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltages					
Pin VDD input		4.0		8.0	V
Chip Consumed Current	8V Supply Voltage Ta=25°C		4		mA
Error Amplifier Reference Voltage					
Non-Inverting input of the error amplifier	Measure INN	1.2125	1.25	1.2875	V
Line regulation	VDD=4.0~8.0 V		2	20	mV
Under Voltage Look Out					
Positive Going Threshold	Ta=25°C Note3	3.8	4.0	4.2	V
Hysteresis		0.1	0.2	0.3	V
The 1st High Frequency Ramp Wave Generator					
Operating Frequency	Note1	50		400	KHz
Output peak(CTOSC)			2.25		V
Output valley(CTOSC)			0.5		V
Error Amplifier					
Input voltage	Note2	0.1		3	V
Open loop gain		60	80		dB
Unit gain band width		1	1.5		MHz
Power On Initialization and Latched Off Protection Enable					
Pin TIMER Output current Case1. TIMER <0.3V	VDD=6V, Ta=25°C Note 3		20		uA
Pin TIMER Output current Case1. TIMER > 0.3V			1		uA
Power On Reset/Initialization threshold on pin TIMER			0.3		V
Latched Off Protection enable threshold on pin TIMER			2.5		V
Load Detection					
Pin ISEN detection lower threshold	VDD=6V, Ta=25°C		1.3		V
Hysterisis			20		mV
Output Detection and Adaptive Adjusting					
Pin OUTADJ detection lower threshold	VDD=6V, Ta=25°C		2.0		V
Hysterisis			20		mV
INN pin pull-up current source			60		uA
The 2nd Low Frequency PWM Generator					
Ramp Wave Peak(CTPWM)	VDD=6V, Ta=25°C		2.5		V
Ramp Wave Valley(CTPWM)			1.0		V
PWM Frequency		10		100K	Hz
Control voltage of 0 % Duty cycle on pin PWMDC Case 1. MODSEL = 0V			1.0		V
Control voltage of 0 % Duty cycle on pin PWMDC Case 1. MODSEL = ICVDD			2.5		V
Output voltage of Pin PWMOUT for making the logic “high”.			2.5		V
Pin PWMOUT output for making the logic “low”			Floating		
Maximum Duty Cycle			92		%
Output of the 1st PWM (OUT1, OUT2)					
CMOS output impedance	(Note2, Note3)		50		ohm
Rising Time	VDD=6V, 2000pF(Note2, Note3)		110		nS
Falling Time			100		nS
Delay Time			600		nS

Note 1. The output driver frequency is the half of the ramp wave frequency.
Note 2. Only verified by simulation. Not 100% tested.
Note 3. The voltages of the output driver OUT1 is pulled to GND and OUT2 is pulled to VDD in each off states.

Timing Diagram

The timing of the 2nd low frequency PWM generator, ISEN and LOAD pin are as bellow: A 51Kohm pulled-low resistor is connected on PWMOUT pin in this example.

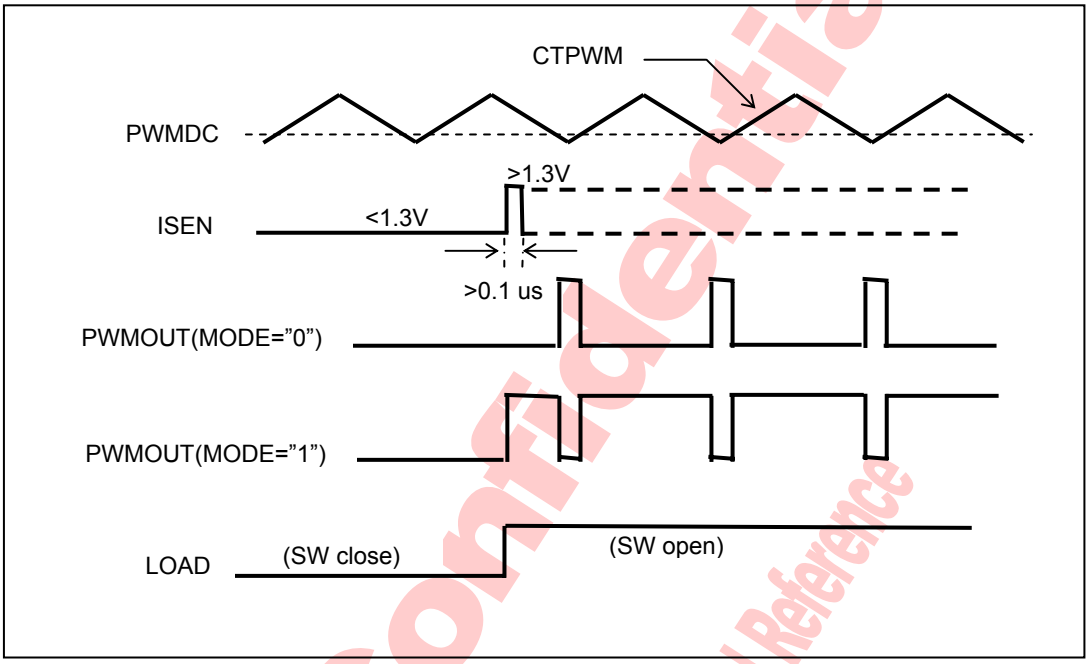


Fig. 3

BIT3715 uses fixed frequency driving methodology. The power switch is driven by fixed frequency PWM controlled signal. The detail timing relationship is shown as bellow: The maximum duty cycle of OUT1 and OUT1 are smaller than 50% with 180° phase difference.

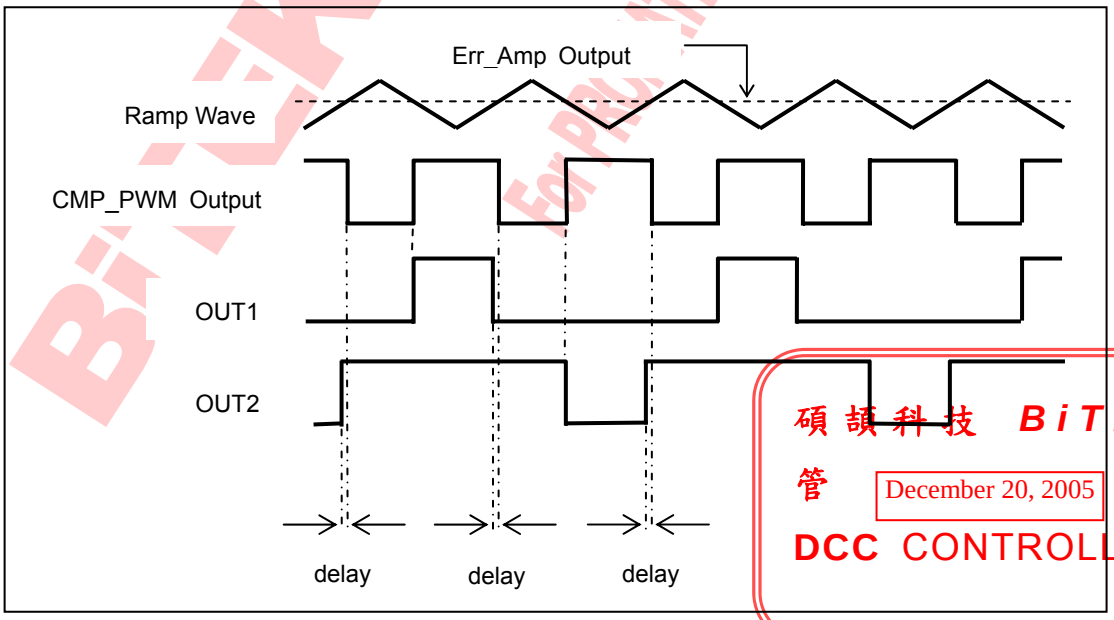


Fig. 4

Order Information:

BIT3715-S0

SO: SOP **SS:** SSOP

Part number

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Soldering Information

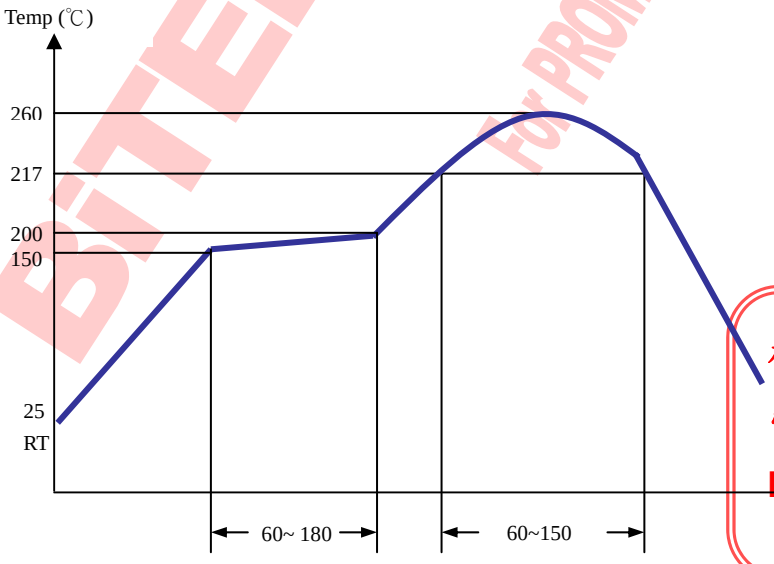
Reflow Soldering:

The choice of heating method may be influenced by plastic QFP package). If infrared or vapor phase heating is used and the package is not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement. Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferable be kept below 245 °C for thick/large packages (packages with a thickness ≧ 2.5 mm or with a volume ≧ 350 mm^3 so called thick/large packages). The top-surface temperature of the packages should preferable be kept below 260 °C for thin/small packages (packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called thin/small packages).

Stage	Condition	Duration
1'st Ram Up Rate	max3.0+/-2℃/sec	-
Preheat	150℃~200℃	60~180 sec
2'nd Ram Up	max3.0+/-2℃/sec	-
Solder Joint	217℃ above	60~150 sec
Peak Temp	260 +0/-5℃	20~40 sec
Ram Down rate	6℃/sec max	-



Wave Soldering:

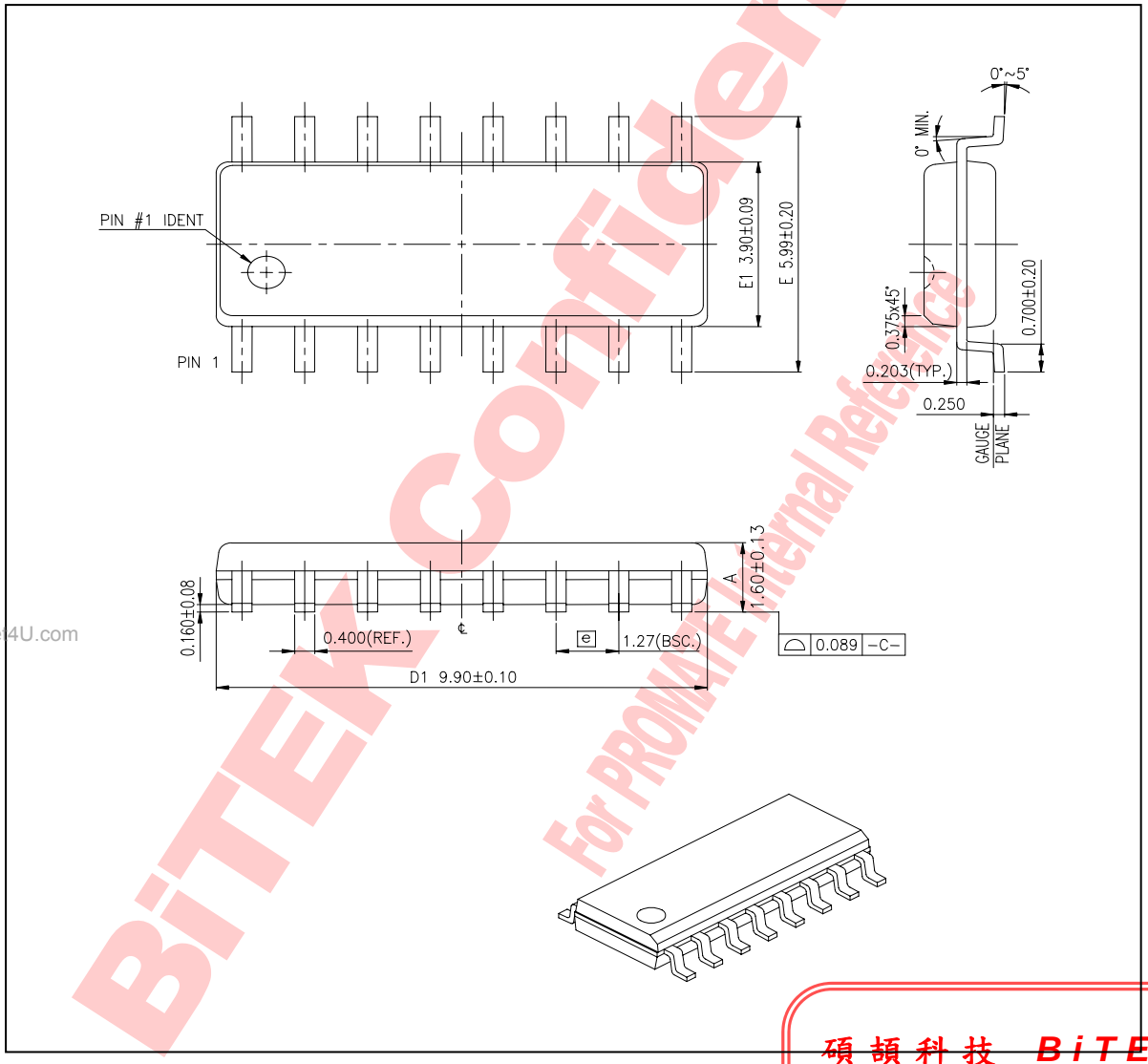
Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

Manual Soldering:

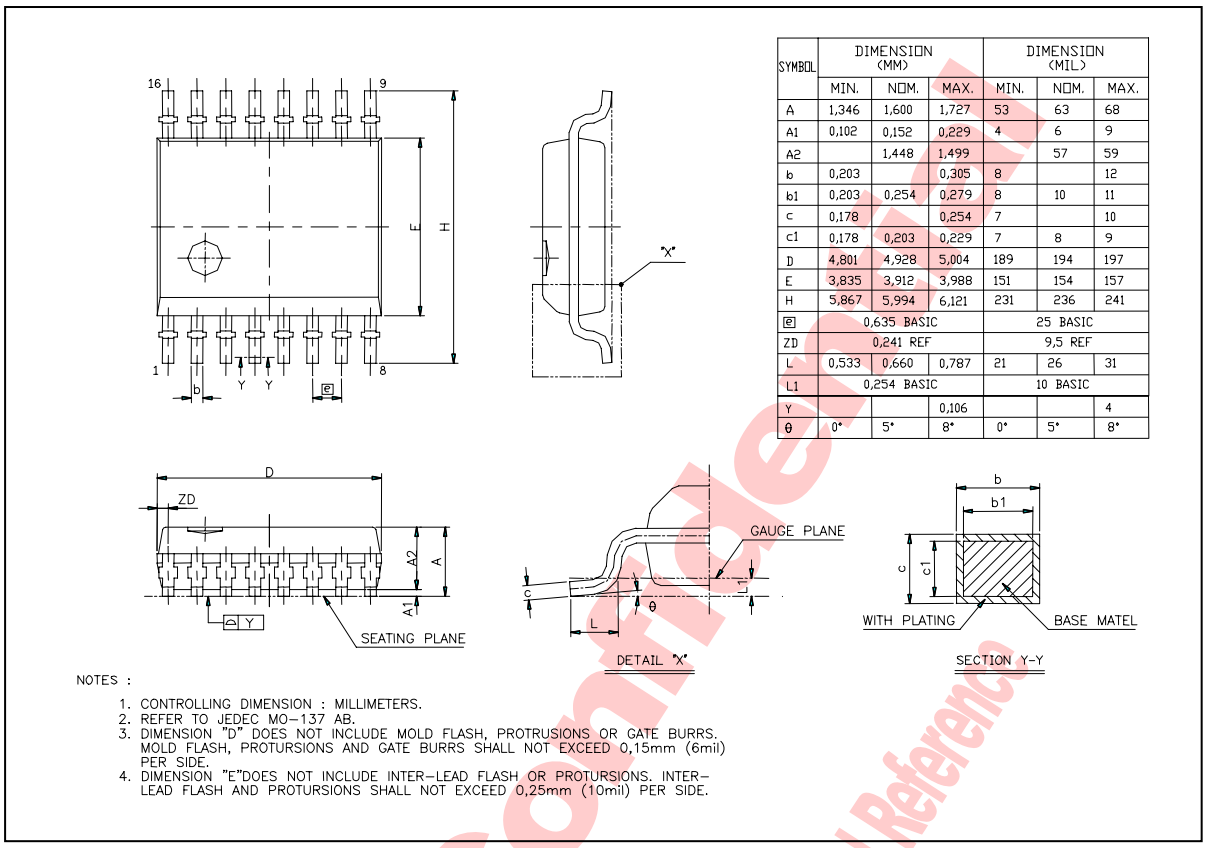
Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Package Information :

SOP type :



SSOP type :



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1,346	1,600	1,727	53	63	68
A1	0,102	0,152	0,229	4	6	9
A2		1,448	1,499		57	59
b	0,203		0,305	8		12
b1	0,203	0,254	0,279	8	10	11
c	0,178		0,254	7		10
c1	0,178	0,203	0,229	7	8	9
D	4,801	4,928	5,004	189	194	197
E	3,835	3,912	3,988	151	154	157
H	5,867	5,994	6,121	231	236	241
e	0,635 BASIC			25 BASIC		
ZD	0,241 REF			9,5 REF		
L	0,533	0,660	0,787	21	26	31
L1	0,254 BASIC			10 BASIC		
Y			0,106			4
θ	0°	5°	8°	0°	5°	8°

NOTES :

1. CONTROLLING DIMENSION : MILLIMETERS.
2. REFER TO JEDEC MO-137 AB.
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTURSIONS AND GATE BURRS SHALL NOT EXCEED 0,15mm (6mil) PER SIDE.
4. DIMENSION "E"DOES NOT INCLUDE INTER-LEAD FLASH OR PROTURSIONS. INTER-LEAD FLASH AND PROTURSIONS SHALL NOT EXCEED 0,25mm (10mil) PER SIDE.