2-3 Cell NVDC-1 Battery Charger Controller

Check for Samples: bq24715J

FEATURES

- **6-24V Input SMBus NVDC-1 2-3S Battery Charger Controller**
- **System Instant-on Operation with No Battery or Deeply Discharged Battery**
- **Ultra-Fast Transient Response of 100 µs**
- **Ultra-Low Quiescent Current of 500 µA and High PFM Light Load Efficiency 80% at 20mA load to Meet Energy Star and ErP Lot6**
- **Switching Frequency: 600 kHz, 800 kHz, 1MHz**
- **Programmable System/Charge Voltage (16 mV/step), Input/Charge Current (64 mA/step) with High Accuracy**
  - **±0.5% Charge Voltage Regulation**
  - **±3% Input/Charge Current Regulation**
  - **±2% 40x Input/16x Discharge Current Monitor Output**
- **Support Battery LEARN Function**
- **Maximize CPU Performance with Deeply Discharged Battery or No Battery**
- **Integrated NMOS ACFET and RBFET Driver**
- **20-pin 3.5 x 3.5 mm^2 QFN Package**

APPLICATIONS

- **Ultrabook, Notebook, and Tablet PC**
- **Industrial and Medical Equipment**
- **Portable Equipment**

DESCRIPTION

The bq24715J is a NVDC-1 synchronous battery charge controller with low quiescent current, high light load efficiency for 2S or 3S Li-ion battery charging applications, offering low component count.

The power path management allows the system to be regulated at battery voltage but does not drop below the programmable system minimum voltage.

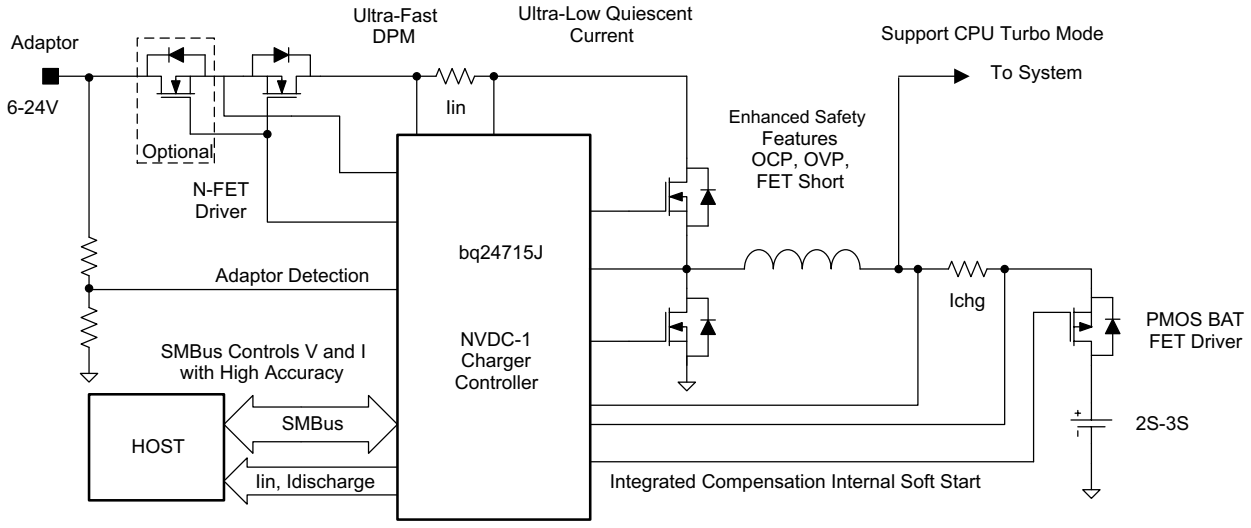
The device provides N-channel ACFET and RBFET drivers for the power path management. It also provides driver of the external P-channel battery FET. The loop compensation is fully integrated.

The device has programmable 11-bit charge voltage, 7-bit input/charge current and 6-bit minimal system voltage with very high regulation accuracies through the SMBus communication interface.

The device monitors adapter current or battery discharge current through the IOUT pin allowing the host to throttle down CPU speed when needed.

The device provides extensive safety features for over current, over voltage and MOSFET short circuit.

Simplified Application Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

PART NUMBER	IC MARKING	PACKAGE	ORDERING NUMBER (Tape and Reel)	QUANTITY
bq24715J	BQ715	20-PIN 3.5 × 3.5 mm^2 QFN	bq24715JRGRR	3000
			bq24715JRGRT	250

(1) For the most current package and ordering information see Package Option Addendum at the end of this document; or see the TI website at www.ti.com

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Voltage range	SRN, SRP, ACN, ACP, CMSRC, VCC	–0.3	30	V
		PHASE	–2.5	30	
		ACDET, SDA, SCL, LODRV, REGN, IOUT, ACOK, CELL	–0.3	7	
		LODRV (20ns)	–2.5	7	
		BTST, HIDRV, ACDRV	–0.3	36	
		HIDRV (20ns)	–2.5	36	
		$\overline{\text{BATDRV}}$	–0.3	30	
	Maximum difference voltage SRP–SRN, ACP–ACN		–0.5	0.5	V
T_J	Junction temperature range		–40	155	°C
T_{STG}	Storage temperature range		–55	155	°C
	ESD Human Body Model (HBM)			2000	V
	ESD Charged Device Model (CDM)			500	V

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.

THERMAL INFORMATION

THERMAL METRIC(1)		bq24715 QFN (20 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	34.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	49.3	
θ_{JB}	Junction-to-board thermal resistance(2)	12.5	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	12.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Voltage range	SRN, SRP, ACN, ACP, CMSRC, VCC	0	24	V
		PHASE	–2	24	V
		ACDET, SDA, SCL, LODRV, REGN, IOUT, ACOK, CELL	0	6.5	V
		BTST, HIDRV, ACDRV	0	30	V
		BATDRV	–0.3	16	V
	Maximum difference range	SRP–SRN, ACP–CAN	–0.2	0.2	V
T_J	Junction temperature range		–20	125	°C
T_A	Operating free-air temperature range		–20	85	°C

ELECTRICAL CHARACTERISTICS

6 V ≤ $V_{(VCC)}$ ≤ 24V, –20°C ≤ T_J ≤ 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT OPERATING CONDITIONS						
V_{VCC_OP}	VCC Input Voltage Operating Range		6		24	V
MIN SYSTEM VOLTAGE REGULATION (0x3E register)						
V_{SYSMIN_RNG}	MinSystem Voltage Regulation Range		4.096		14.5	V
V_{SYSMIN_REG} and $V_{SYSMIN\_REG\_ACC}$	Default minimum system voltage and accuracy at charge enable and battery voltage lower than V_{SYSMIN_REG}	MinsystemVoltage() = 0x2400H (3S)		9.216		V
			–2%		1.2%	
		MinsystemVoltage() = 0x1800H (2S)		6.144		V
			–3%		1.5%	
MAX SYSTEM VOLTAGE REGULATION (0x15 register charge disable)						
V_{SYSMAX_RNG}	MaxSystem Voltage Regulation Range		4.096		14.5	V
V_{SYSMAX_REG} and $V_{SYSMAX\_REG\_ACC}$	Default maximum system voltage and accuracy at charge disable	MaxChargeVoltage() = 0x34C0H (3S)		13.504		V
			–2%		1.2%	
		MaxChargeVoltage() = 0x2330H (2S)		9.008		V
			–3%		1.5%	
MAX CHARGE VOLTAGE REGULATION (0-85C; 0x15 register charge enable)						
$V_{BAT\_REG\_RNG}$	Battery voltage range		4.096		14.5	V
$V_{BAT\_REG\_ACC}$	Charge voltage regulation accuracy	MaxChargeVoltage() = 0x3130H	12.529	12.592	12.655	V
			–0.5%		0.5%	
		MaxChargeVoltage() = 0x20D0H	8.35	8.4	8.45	V
			–0.6%		0.6%	

ELECTRICAL CHARACTERISTICS (continued)

6 V ≤ $V_{(VCC)}$ ≤ 24V, –20°C ≤ T_J ≤ 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CHARGE CURRENT REGULATION (0-85°C)						
$V_{IREG\_CHG\_RNG}$	Charge current regulation differential voltage range R_{SNS} = 10mΩ	VIREG_CHG = VSRP - VSRN	0		81.28	mV
$I_{CHRG\_REG\_ACC}$	Charge current regulation accuracy 10mΩ current sensing resistor, VBAT>VSYSMIN	ChargeCurrent() = 0x1000H	3937	4096	4219	mA
			–3%		3%	
		ChargeCurrent() = 0x0800H	1946	2048	2150	mA
			–5%		5%	
		ChargeCurrent() = 0x0400H	921	1024	1127	mA
			–10%		10%	
		ChargeCurrent() = 0x0200H	410	512	614	mA
			–20%		20%	
		ChargeCurrent() = 0x0180H	288	384	480	
			–25%		25%	
		ChargeCurrent() = 0x0100H	172	256	340	mA
			–33%		33%	
		ChargeCurrent() = 0x00C0H	115	192	269	
			–40%		40%	
		ChargeCurrent() = 0x0080H	64	128	192	mA
			–60%		60%	
PRECHARGE CURRENT REGULATION (0-85°C)						
$I_{PRECHRG\_REG\_ACC}$	Charge current regulation accuracy 10mΩ current sensing resistor, VBAT<VSYSMIN, chargeoption(2)=1	ChargeCurrent() >= 0x0180H	268.8	384	499.2	
			–30%		30%	
		ChargeCurrent() = 0x0100H	153.6	256	358.4	mA
			–40%		40%	
		ChargeCurrent() = 0x00C0H	96	192	288	
			–50%		50%	
		ChargeCurrent() = 0x0080H	25.6	128	230.4	mA
			–80%		80%	
INPUT CURRENT REGULATION						
$V_{DPM\_REG\_RNG}$	Input current regulation differential voltage range R_{AC} = 10mΩ	V_{IREG_DPM} = V_{ACP} – V_{ACN}	0		80.64	mV
$I_{DPM\_REG\_ACC}$	Input current regulation accuracy 10 mΩ current sensing resistor	InputCurrent() = 0x1000H	3973	4096	4219	mA
			–3%		3%	
		InputCurrent() = 0x0800H	1946	2048	2150	mA
			–5%		5%	
		InputCurrent() = 0x0400H	870	1024	1178	mA
			–15%		15%	
		InputCurrent() = 0x0200H	358.4	512	665.6	mA
			–30%		30%	
INPUT CURRENT OR DISCHARGE CURRENT SENSE AMPLIFIER						
V_{ACP/N_OP}	Input common mode range	Voltage on ACP/ACN	4.5		24	V
V_{SRP/N_OP}	Output common mode range	Voltage on SRP/SRN			14.5	V
I_{IOUT}	IOUT Output current		0		40	uA
A_{IOUT}	Current sense amplifier gain	$V_{(IOUT)}/V_{(SRN-SRP)}$, 0x12H[15] = 1, 0x12H[4] = 1 and 0x12H[3] = 1		16		V/V
		$V_{(IOUT)}/V_{(ACP-ACN)}$, 0x12H[4] = 0 and 0x12H[3] = 1		40		V/V
$V_{SRN-SRP\_OFF}$	Input current amplifier offset voltage			1		mV
V_{IOUT_ACC}	Current sense output accuracy	$V_{(SRN-SRP)}$ or $V_{(ACP-ACN)}$ = 40.96 mV	-2%		2%	
		$V_{(SRN-SRP)}$ or $V_{(ACP-ACN)}$ = 20.48 mV	-3%		3%	
		$V_{(SRN-SRP)}$ or $V_{(ACP-ACN)}$ = 10.24 mV	-10%		10%	
		$V_{(SRN-SRP)}$ or $V_{(ACP-ACN)}$) = 5.12 mV	-25%		25%	

ELECTRICAL CHARACTERISTICS (continued)

6 V ≤ $V_{(VCC)}$ ≤ 24V, –20°C ≤ T_J ≤ 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
C_{IOUT_MAX}	Maximum output load capacitance	For stability with 0 to 1mA load			100	pF
REGN REGULATOR						
V_{REGN_REG}	REGN Regulator voltage	V_{VCC} > 6.5V, V_{ACDET} > 0.6V (0-50 mA load)	5.5	6	6.5	V
I_{REGN_LIM}	REGN Current limit	V_{REGN} = 0V, V_{VCC} > UVLO, Converter enabled and not in T_{SHUT}	50	75		mA
		V_{REGN} = 0V, V_{VCC} > UVLO, Converter disabled or in T_{SHUT}	7	14		mA
C_{REGN}	REGN Output capacitor required for stability	I_{LOAD} = 100 µA to 50 mA		1		µF
UNDER VOLTAGE LOCKOUT COMPARATOR (UVLO)						
V_{UVLO_VCC}	Under-voltage rising threshold	V_{VCC} rising	3	3.2	3.4	V
	Under-voltage hysteresis, falling	V_{VCC} falling		400		mV
V_{UVLO_BAT}	Under-voltage rising threshold	V_{SRN} rising	3	3.3	3.6	V
	Under-voltage hysteresis, falling	V_{SRN} falling		400		mV
QUIESCENT CURRENT						
$I_{BAT\_BATFET\_ON}$	Standby mode. System powered by battery. BATFET ON. $I_{SRN}+I_{SRP}+I_{PHASE}+I_{BTST}+I_{ACP}+I_{ACN}+I_{CMSRC}$	V_{BAT} = 12.6V, V_{SRN} > UVLO, BATFET turns on, ACDET < 0.6 V, T_J = –20°C to 85°C, 0x12[15] = 1 (low power mode enabled)		13.3	20	µA
		V_{BAT} = 12.6V, V_{SRN} > UVLO, BATFET turns on, ACDET < 0.6 V, T_J = –20°C to 85°C, 0x12[15] = 0 (low power mode disabled)		50	70	µA
$I_{STANDBY}$	Adapter standby quiescent current, $I_{VCC}+I_{ACP}+I_{ACN}+I_{CMSRC}$	ACN = ACP = CMSRC = VCC = 20 V, V_{BAT} = 12.6V, V_{ACDET}> 2.4V, CELL pull up, T_J = –20°C to 85°C. No switching.		540	700	µA
$I_{AC\_SWLIGHT}$	Adapter current, I_{VCC} + I_{ACP} + I_{ACN} + I_{CMSRC}	$I_{STANDBY}$ plus supply current in PFM, 200 mW output; Reg0x12[10] = 0; MOSFET Qg = 4 nC;		1.5		mA
		$I_{STANDBY}$ plus supply current in PFM, 200 mW output; Reg0x12[10] = 1; MOSFET Qg = 4 nC;		5		
I_{AC_SW}	Adapter current, I_{VCC} + I_{ACP} + I_{ACN} + I_{CMSRC}	Charge enable, 800kHz switching frequency MOSFET Qg = 4 nC		10		mA
ACOK COMPARATOR						
V_{ACOK_RISE}	ACOK Rising threshold	V_{VCC} > UVLO, V_{ACDET} rising	2.376	2.4	2.424	V
$V_{ACOK\_FALL\_HYS}$	ACOK Falling hysteresis	V_{VCC} > UVLO, V_{ACDET} falling	35	55	75	mV
$V_{ACOK\_RISE\_DEG}$	ACOK Rising deglitch (Specified by design)	V_{VCC} >UVLO, V_{ACDET} rising above 2.4V		2	3	ms
V_{WAKEUP_RISE}	WAKEUP Detect rising threshold	V_{VCC} > UVLO, V_{ACDET} rising		0.52	0.6	V
V_{WAKEUP_FALL}	WAKEUP Detect falling threshold	V_{VCC} > UVLO, V_{ACDET} falling	0.35	0.46		V
VCC to SRN COMPARATOR (VCC_SRN), SLEEP						
$V_{VCC\text{-}SRN\_FALL}$	VCC-SRN Falling threshold	V_{VCC} falling towards V_{SRN}	70	125	200	mV
$V_{VCC\text{-}SRN\_RHYS}$	VCC-SRN Rising hysteresis	V_{VCC} rising above V_{SRN}		150		mV
	VCC-SRN falling delay	V_{VCC} falling towards V_{SRN}	95	160	237	µs
	Resume time	V_{VCC} rising above V_{SRN}	0.76	1.28	1.9	ms
INPUT OVER-CURRENT COMPARATOR						
ACOC	ACP to ACN Rising Threshold, respect to input current().	ChargeOption() bit [7] = 1		330%		I_{DPM}
	ACOC floor			50		mV
	ACOC ceiling			180		mV
	Relax time, No latch.			300		ms
LIGHT LOAD COMPARATOR						
	ACP to ACN Falling Threshold, average	Converter CCM-DCM, current decrease		1.25		mV
	ACP to ACN Rising Threshold, average			2.5		mV
	Deglitch time, both side			10		µs

ELECTRICAL CHARACTERISTICS (continued)

6 V ≤ $V_{(VCC)}$ ≤ 24V, –20°C ≤ T_J ≤ 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CONVERTER OVER-CURRENT COMPARATOR (ILIM_HI), CYCLE-BY-CYCLE						
ILIM_HI	Converter over current limit, measure GND-PH	Chargeoption() bit [6] =0		250		mV
		Chargeoption() bit [6] =1 (default)		350		mV
CONVERTER UNDER-CURRENT COMPARATOR (ILIM_LOW) , CYCLE-BY-CYCLE						
	Converter over current limit, measure GND-PH		–2	0	6	mV
INPUT OVER-VOLTAGE (ACOVP)						
V_{ACOVP}	VCC Over-Voltage Rising Threshold	VCC rising	24	26	28	V
V_{ACOV_HYS}	VCC Over-Voltage Falling Hysteresis	VCC falling		1		V
	Rising deglitch	VCC rising		0.1		ms
	Falling deglitch	VCC falling		1		ms
BAT OVER-VOLTAGE COMPARATOR (BAT_OVP)						
V_{OVP_RISE}	Over-voltage rising threshold as percentage of VBAT_REG	V_{SRN} rising		102%		
V_{OVP_FALL}	Over-voltage falling threshold as percentage of VBAT_REG	V_{SRN} falling		101%		
	Discharge current during OVP, SRP pin	Charge enable, BATFET ON		4		mA
	Over voltage deglitch time to fully turn-off BATFET			1		ms
SYSTEM OVER-VOLTAGE COMPARATOR (SYS_OVP)						
$V_{SYSOVP\_RISE\_3S}$	3S System over-voltage rising threshold	V_{SRN} rising, chargeoption bit[12]=0 default		15.1		V
		V_{SRN} rising, chargeoption bit[12]=1		17.0		
$V_{SYSOVP\_FALL\_3S}$	3S System over-voltage falling threshold	V_{SRN} falling		13.2		V
$V_{SYSOVP\_RISE\_2S}$	2S System over-voltage rising threshold	V_{SRN} rising, chargeoption bit[12]=0 default		10.1		V
		V_{SRN} rising, chargeoption bit[12]=1		11.3		
$V_{SYSOVP\_FALL\_2S}$	2S System over-voltage falling threshold	V_{SRN} falling		8.8		V
t_{SYSOVP_DEG}	System over-voltage deglitch time to turn-off ACDRV			24		µs
	Discharge current during OVP			4		mA
THERMAL SHUTDOWN COMPARATOR (T_{SHUT})						
T_{SHUT}	Thermal shutdown rising temperature	Temperature rising		155		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis, falling	Temperature falling		20		°C
	Rising deglitch			100		µs
	Falling deglitch			10		ms
LOGIC INPUT (SDA, SCL)						
VIN_ LO	Input low threshold				0.8	V
VIN_ HI	Input high threshold		2.1			V
IIN_ LEAK	Input bias current	V = 7 V	–1		1	µA
LOGIC OUTPUT OPEN DRAIN (ACOK, SDA)						
VOUT_ LO	Output saturation voltage	5 mA drain current			500	mV
IOUT_ LEAK	Leakage current	V = 7 V	–1		1	µA
ANALOG INPUT (ACDET)						
IIN_ LEAK	Input bias current	V = 7 V	–1		1	µA
	Offset		–10		10	mV
ANALOG INPUT (CELL)						
	GND				1.0	V
	Float (2S setting)		1.2		1.8	V
	High (3S setting)		2.5			V
	Allowed max delay time to config CELL at POR		72	100	120	ms
	Internal pull up resistor to REGN			405		kΩ
	Internal pull down resistor to GND			141		kΩ

ELECTRICAL CHARACTERISTICS (continued)

6 V ≤ $V_{(VCC)}$ ≤ 24V, –20°C ≤ T_J ≤ 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
PWM OSCILLATOR						
F_{SW}	PWM Switching frequency	ChargeOption () bit [9:8] = 00	–10%	600	10%	kHz
		ChargeOption() bit [9:8] = 01 (Default)	–10%	800	10%	kHz
		ChargeOption() bit [9:8] = 10	–10%	1000	10%	kHz
F_{SW_min}	Audio frequency limit, PFM	ChargeOption() bit [10] = 1		40		kHz
ACFET GATE DRIVER (ACDRV)						
I_{ACFET}	ACDRV Charge pump current limit		40	60		µA
V_{ACFET}	Gate drive voltage on ACFET	V_{ACDRV} – V_{CMSRC} when V_{VCC} > UVLO	5.5	6.1	6.7	V
R_{ACDRV_LOAD}	Minimum load resistance between ACDRV and CMSRC		500			kΩ
R_{ACDRV_OFF}	ACDRV Turn-off resistance	I = 30 µA	5	6.2	7.4	kΩ
V_{ACFET_LOW}	ACDRV Turn-off when Vgs voltage is lower than V_{ACFET} (Specified by design)	The voltage below V_{ACFET}		0.2		V
BATTERY FET GATE DRIVER ($\overline{BATDRV}$)						
$R_{DS\_BAT\_OFF}$	BATFET Turn-off resistance	100 µA current into $\overline{BATDRV}$		2		kΩ
$R_{DS\_BAT\_ON}$	BATFET Turn-on resistance	100 µA current from $\overline{BATDRV}$		5		kΩ
V_{BATDRV_REG}	BATFET Drive voltage	V_{BATDRV_REG} =V_{SRN} – V_{BATDRV} when V_{AVCC} > 5 V and BATFET is on	4.2		8	V
PWM HIGH SIDE DRIVER (HIDRV)						
$R_{DS\_HI\_ON}$	High side driver turn-on resistance	V_{BTST} – VPH = 5.5 V, I = 10 mA		4	5.5	Ω
$R_{DS\_HI\_OFF}$	High side driver turn-off resistance	V_{BTST} – V_{PH} = 5.5 V, I = 10 mA		0.65	1.3	Ω
$V_{BTST\_REFRESH}$	Bootstrap refresh comparator threshold voltage	V_{BTST} – V_{PH} when low side refresh pulse is requested	3.85	4.15	4.7	V
PWM LOW SIDE DRIVER (LODRV)						
$R_{DS\_LO\_ON}$	Low side driver turn-on resistance	V_{REGN} = 6V, I = 10mA		4	6.2	Ω
$R_{DS\_LO\_OFF}$	Low side driver turn-off resistance	V_{REGN} = 6V, I = 10mA		0.9	1.4	Ω
PWM DRIVER TIMING						
t_{LOW_HIGH}	Driver dead time from low side to high side			20		ns
t_{HIGH_LOW}	Driver dead time from high side to low side			20		ns
INTERNAL SOFT START						
I_{STEP}	Soft start current step	In CCM mode 10 mΩ current sensing resistor		64		mA
	Soft start current step time			24		µs

SMBus TIMING CHARACTERISTICS

4.5 V ≤ $V_{(VCC)}$ ≤ 24 V, 0°C ≤ T_J ≤125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

		MIN	TYP	MAX	UNIT
t_R	SCLK/SDATA rise time			1	µs
t_F	SCLK/SDATA fall time			300	ns
$t_{W(H)}$	SCLK pulse width high	4		50	µs
$t_{W(L)}$	SCLK Pulse Width Low	4.7			µs
$t_{SU(STA)}$	Setup time for START condition	4.7			µs
$t_{H(STA)}$	START condition hold time after which first clock pulse is generated	4			µs
$t_{SU(DAT)}$	Data setup time	250			ns
$t_{H(DAT)}$	Data hold time	300			ns
$t_{SU(STOP)}$	Setup time for STOP condition	4			µs
$t_{(BUF)}$	Bus free time between START and STOP condition	4.7			µs
$F_{S(CL)}$	Clock Frequency	10		100	kHz
HOST COMMUNICATION FAILURE					
$t_{timeout}$	SMBus bus release timeout (1)	25		35	ms
t_{BOOT}	Deglitch for watchdog reset signal	10			ms
t_{WDI}	Watchdog timeout period, ChargeOption() bit [14:13] = 01 (2)	35	44	53	s
	Watchdog timeout period, ChargeOption() bit [14:13] = 10 (2)	70	88	105	
	Watchdog timeout period, ChargeOption() bit [14:13] = 11 (2) (Default)	140	175	210	

(1) Devices participating in a transfer will timeout when any clock low exceeds the 25ms minimum timeout period. Devices that have detected a timeout condition must reset the communication no later than the 35ms maximum timeout period. Both a master and a slave must adhere to the maximum value specified as it incorporates the cumulative stretch limit for both a master (10ms) and a slave (25ms).
(2) User can adjust threshold via SMBus ChargeOption() REG0x12.

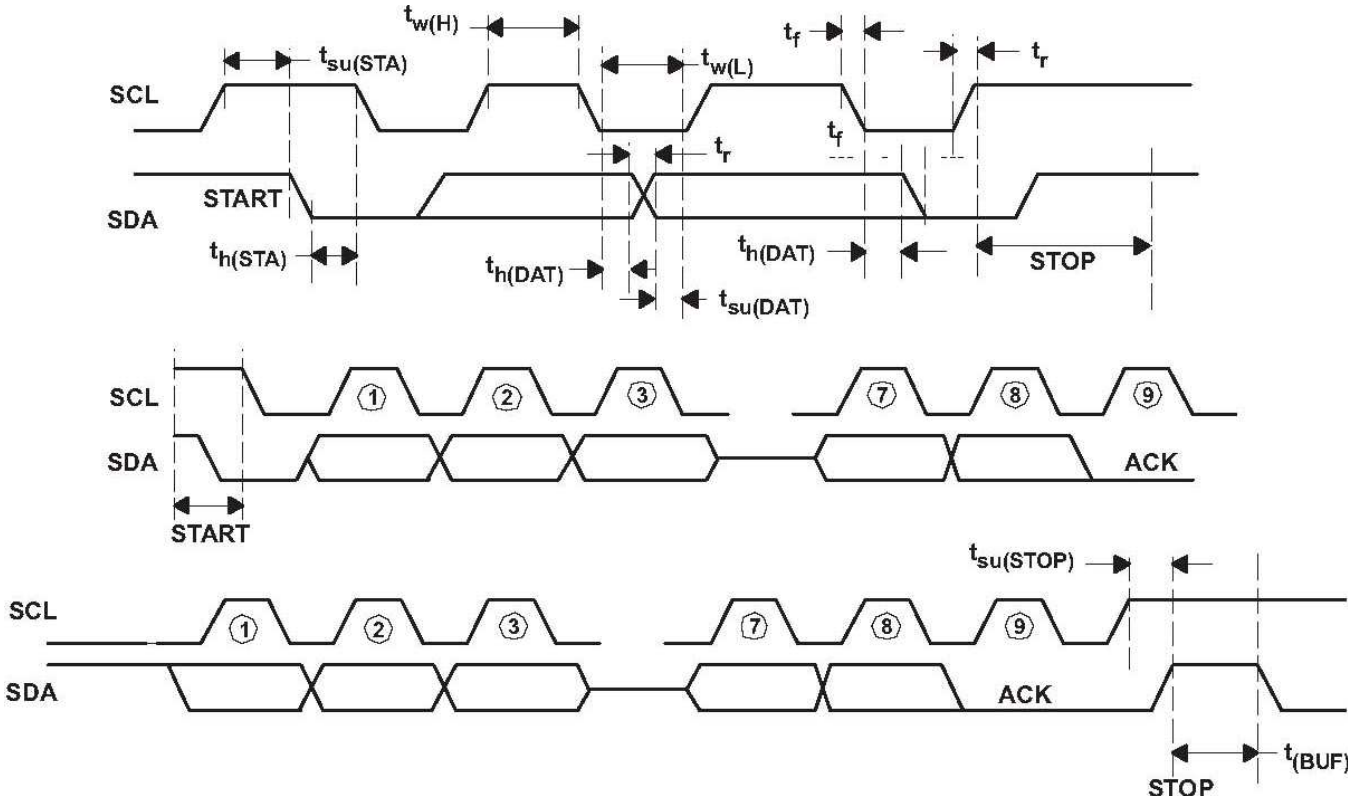
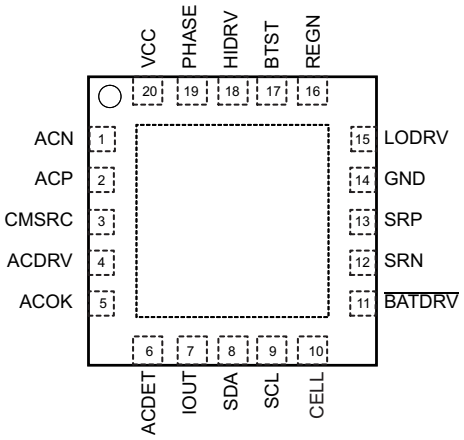


Figure 1. SMBus Communication Timing Waveforms

PIN CONFIGURATION

QFN PACKAGE
(TOP VIEW)



PIN DESCRIPTIONS

PIN	NAME	FUNCTION DESCRIPTION
1	ACN	Input current sense resistor negative input. Place an optional 0.1µF ceramic capacitor from ACN to GND for common-mode filtering. Place a 0.1µF ceramic capacitor from ACN to ACP to provide differential mode filtering.
2	ACP	Input current sense resistor positive input. Place a 1µF ceramic capacitor from ACP to GND for common-mode filtering. Place a 0.1µF ceramic capacitor from ACN to ACP to provide differential-mode filtering.
3	CMSRC	ACDRV charge pump source input. Place a 4kΩ resistor from CMSRC to the common source of ACFET (Q1) and RBFET (Q2) limits the in-rush current on CMSRC pin.
4	ACDRV	Charge pump output to drive both adapter input n-channel MOSFET (ACFET) and reverse blocking n-channel MOSFET (RBFET). ACDRV voltage is 6.1V above CMSRC when voltage on ACDET pin is higher than 2.4V, voltage on VCC pin is above UVLO but lower than 26V and voltage on VCC pin is 675mV above voltage on SRN pin so that ACFET and RBFET can be turned on to power the system by AC adapter. Place a 4kΩ resistor from ACDRV to the gate of ACFET and RBFET limits the in-rush current on ACDRV pin.
5	ACOK	AC adapter detection open drain output. It is pulled HIGH to external pull-up supply rail by external pull-up resistor when voltage on ACDET pin is above 2.4V, VCC above UVLO but lower than 26V and voltage on VCC pin is 675mV above voltage on SRN pin, indicating a valid adapter is present to start charge. If any one of the above conditions can not meet, it is pulled LOW to GND by internal MOSFET. Connect a 10kΩ pull up resistor from ACOK to the pull-up supply rail.
6	ACDET	Adapter detection input. Program adapter valid input threshold by connecting a resistor divider from adapter input to ACDET pin to GND pin. When ACDET pin is above 0.6V and VCC is above UVLO, REGN LDO is present, ACOK comparator and IOUT are both active.
7	IOUT	Buffered 40 times adapter or 16 times discharge current output - the differential voltage across sense resistor; selectable with SMBus command ChargeOption(). Place a 100pF or less ceramic decoupling capacitor from IOUT pin to GND.
8	SDA	SMBus open-drain data I/O. Connect to SMBus data line from the host controller or smart battery. Connect a 10kΩ pull-up resistor according to SMBus specifications.
9	SCL	SMBus open-drain clock input. Connect to SMBus clock line from the host controller or smart battery. Connect a 10kΩ pull-up resistor according to SMBus specifications.
10	CELL	Cell selection pin. For bq24715J, set CELL pin Float for 2-cell, and HIGH for 3-cell. Pulling CELL to GND will provide a hardware exit function from LEARN mode, disable the input DPM function, reset the bit[5] and bit[1] in chargeoption(), and reset Maxchargevoltage() to previous CELL pin default setting value and chargecurrent() to zero. Release CELL from GND, charger will recheck CELL pin voltage and lock the new CELL pin selection.
11	$\overline{\text{BATDRV}}$	P-channel battery FET gate driver output. This pin can go high to turn off the battery FET, go low to turn on the battery FET, or operate battery FET in linear mode to regulate the minimum system voltage when battery is depleted. Connect the source of the BATFET to the system load voltage node. Connect the drain of the BATFET to the battery pack positive node. There is an internal pull-down resistor of 50k on $\overline{\text{BATDRV}}$ to ground.
12	SRN	Charge current sense resistor negative input. SRN pin is for battery voltage sensing as well. Connect SRN pin with a 0.1µF ceramic capacitor to GND for common-mode filtering and connect to current sensing resistor. Connect a 0.1µF ceramic capacitor between current sensing resistor to provide differential mode filtering.

PIN DESCRIPTIONS (continued)

PIN	NAME	FUNCTION DESCRIPTION
13	SRP	Charge current sense resistor positive input. Connect a 0.1µF ceramic capacitor between current sensing resistor to provide differential mode filtering.
14	GND	IC ground. On PCB layout, connect to analog ground plane, and only connect to power ground plane through the power pad underneath IC.
15	LODRV	Low side power MOSFET driver output. Connect to low side n-channel MOSFET gate.
16	REGN	Linear regulator output. REGN is the output of the 6V linear regulator supplied from VCC. The LDO is active when voltage on ACDET pin is above 0.6V and voltage on VCC is above UVLO. Connect a 1µF ceramic capacitor from REGN to GND.
17	BTST	High side power MOSFET driver power supply. Connect a 0.047µF-0.1µF capacitor from BTST to PHASE. Connect a bootstrap Schottky diode from REGN to BTST.
18	HIDRV	High side power MOSFET driver output. Connect to the high side n-channel MOSFET gate.
19	PHASE	High side power MOSFET driver source. Connect to the source of the high side n-channel MOSFET.
20	VCC	Input supply. Use 10Ω resistor and 1µF capacitor to ground as low pass filter to limit inrush current.
PowerPad		Exposed pad beneath the IC. Analog ground and power ground star-connected only at the PowerPad plane. Always solder PowerPad to the board, and have vias on the PowerPad plane connecting to analog ground and power ground planes. It also serves as a thermal pad to dissipate the heat.

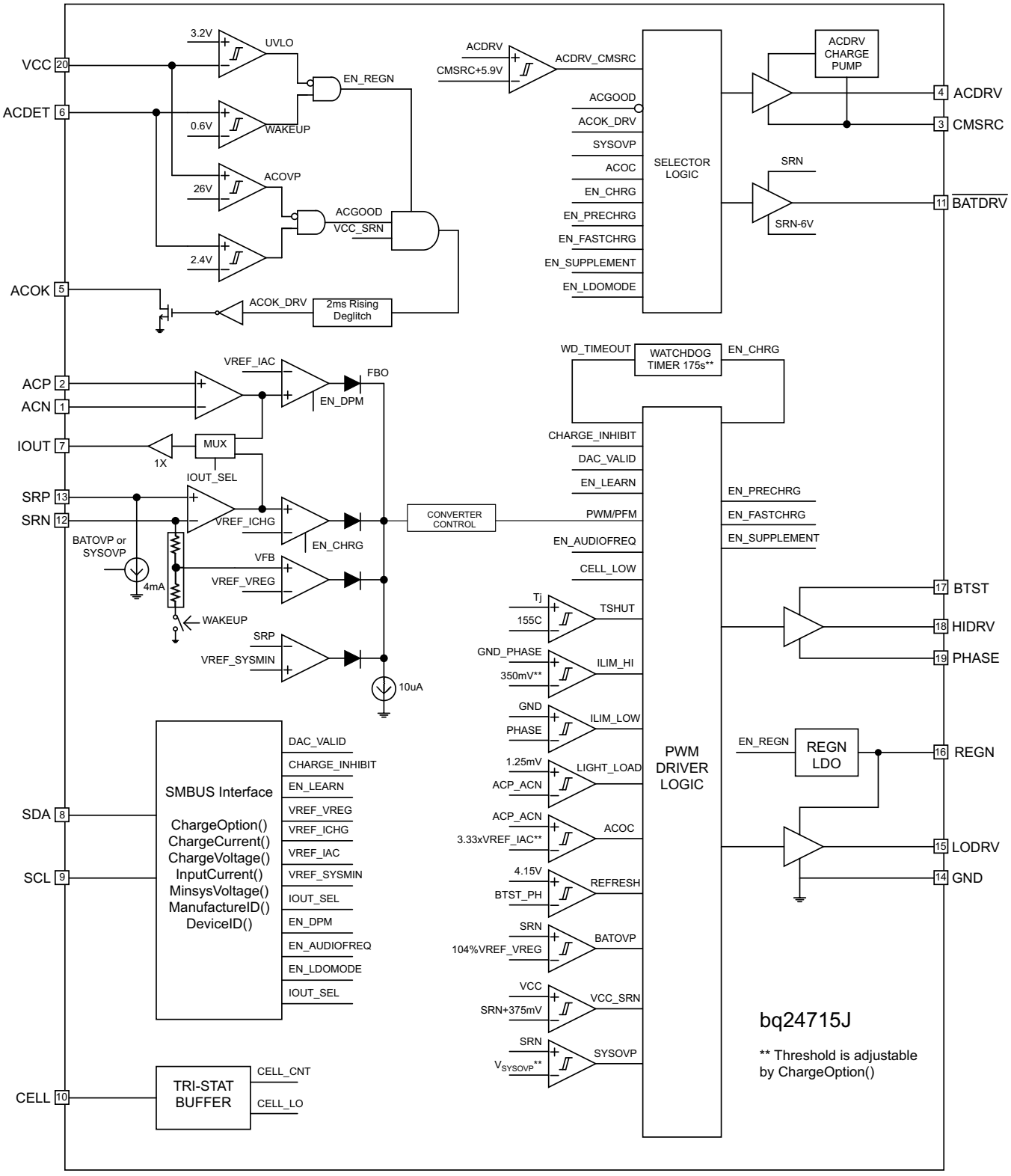
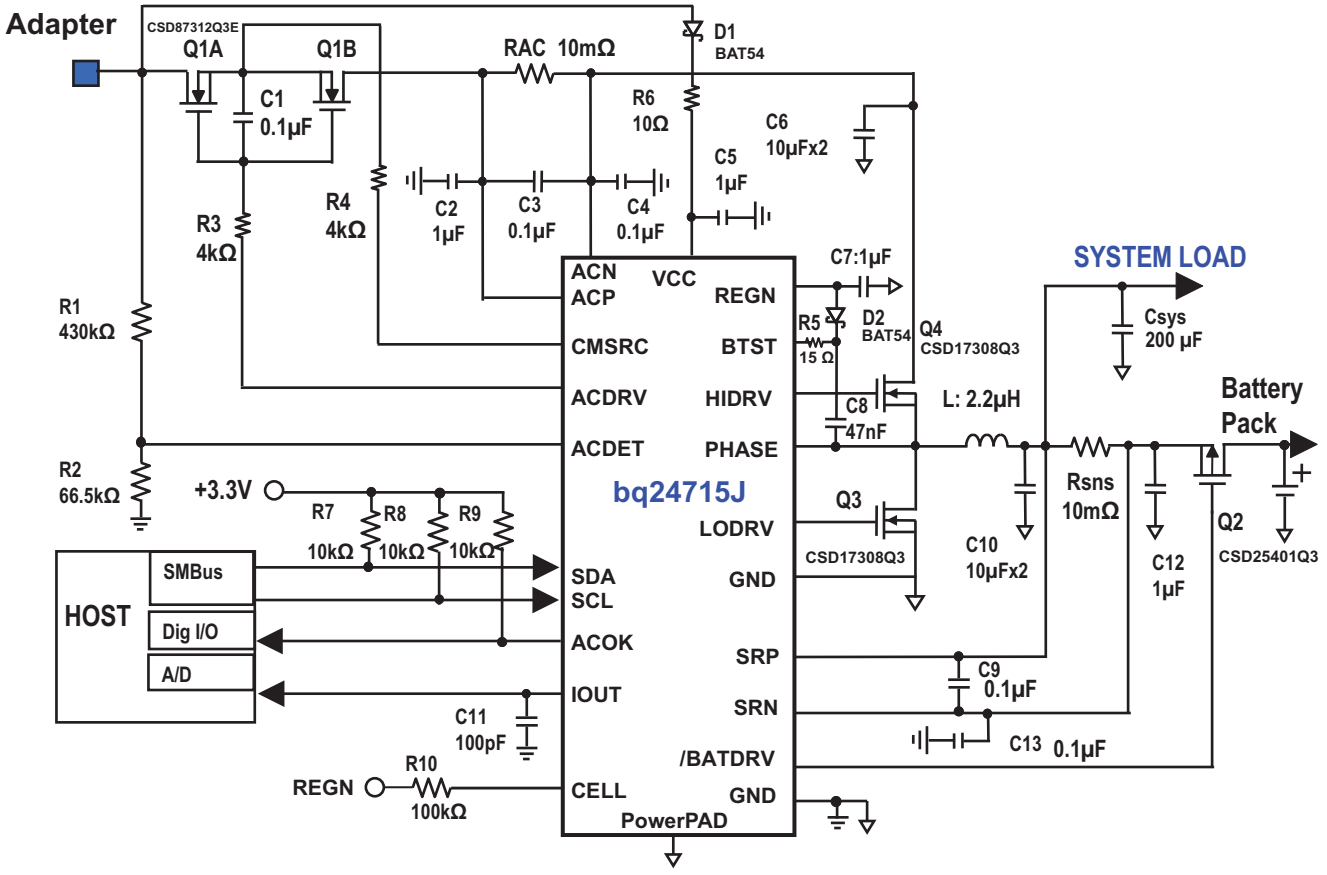


Figure 2. Block Diagram

TYPICAL APPLICATION DIAGRAM



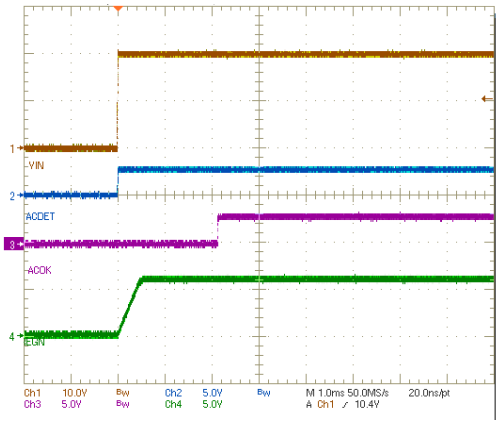
Fs = 800kHz, I_{ADPT} = 3.0A, I_{CHRG} = 2.944A, I_{SYSTEM} = 5A, V_{CHRG} = 12.592V, 65W adapter and 3S2P battery pack
Csys : 200 µF is lumped system bus capacitance

Figure 3. Typical Application Circuit

TYPICAL CHARACTERISTICS

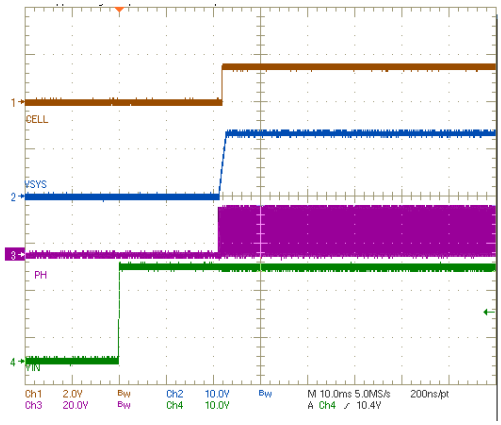
Table 1. Table of Graphs

	FIGURES
VCC, ACDET, REGN and ACOK Power Up	Figure 4
System Power Up	Figure 5
Charge Startup and Shutdown	Figure 6
PFM Mode Switching Waveforms	Figure 7
PwM Mode Switching Waveforms	Figure 8
CELL-GND in Learn Mode	Figure 9
0~3A System Load Transient (IDPM disable & Charge disable)	Figure 10
2~6A System Load Transient (IDPM disable & Charge disable)	Figure 11
0~3A System Load Transient (IDPM enable & Charge enable)	Figure 12
2~6A System Load Transient (IDPM enable & Charge enable)	Figure 13
LIGHT LOAD EFFICIENCY VS. SYSTEM CURRENT	Figure 14
Heavy Load Efficiency vs. System Current	Figure 15



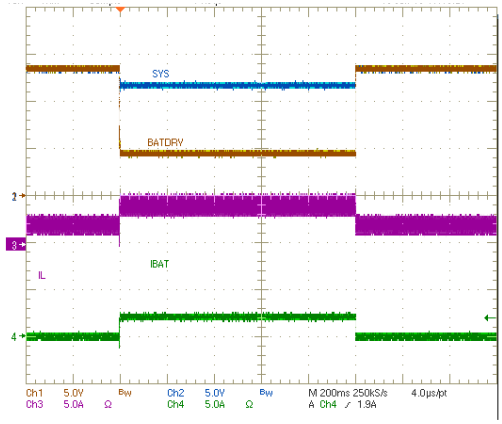
CH1: VCC/VIN, 10V/div, CH2: ACDET, 5V/div, CH3: ACOK, 5V/div, CH4: REGN, 5V/div, 1ms/div

Figure 4. VCC, ACDET, REGN and ACOK Power Up



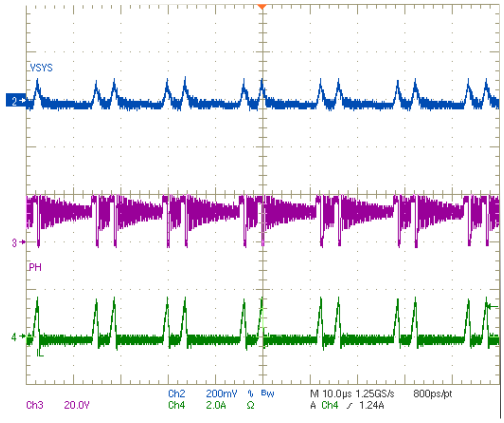
CH1: CELL, 2V/div; CH2: SRN, 10V/div; CH3: PHASE, 20V/div; CH4: VCC, 10/div, 10ms/div

Figure 5. System Power Up



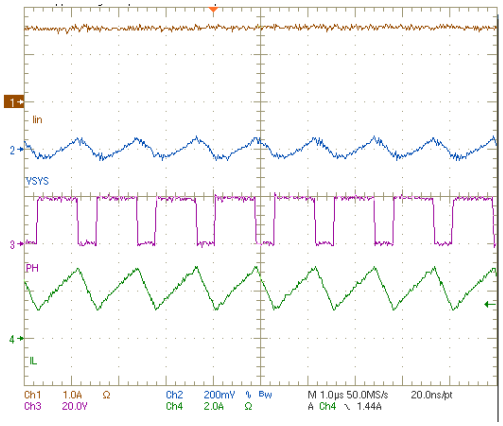
CH1: BATDRV, 5V/div; CH2: SRN, 5V/div; CH3: Inductor current, 5A/div; CH4: Charge current, 5A/div, 200ms/div

Figure 6. Charge Startup and Shutdown



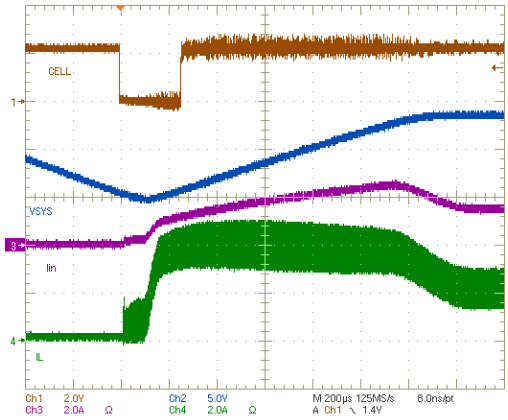
CH2: system voltage (AC), 200mV/div, CH3: PHASE, 20V/div, CH4: inductor current, 2A/div, 10µs/div

Figure 7. PFM Mode Switching Waveforms



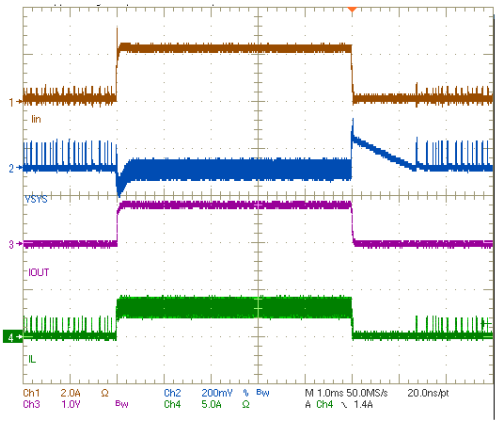
CH1: Input current, 1A/div; CH2: system voltage AC), 200mV/div, CH3: PHASE, 20V/div, CH4: (inductor current, 2A/div, 1µs/div

Figure 8. PWM Mode Switching Waveforms



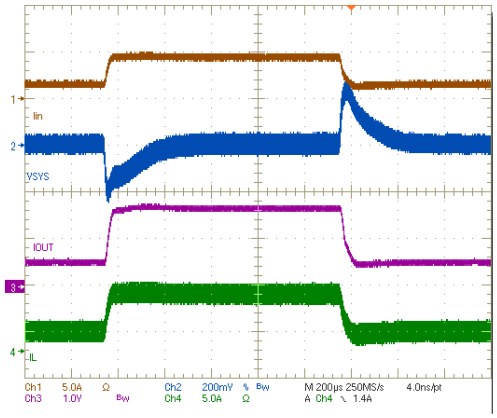
CH1: CELL, 2V/div, CH2: system voltage, CH3: input current, 2A/div, 5V/div, CH4: inductor current, 2A/div, 200µs/div

Figure 9. CELL-GND in Learn Mode



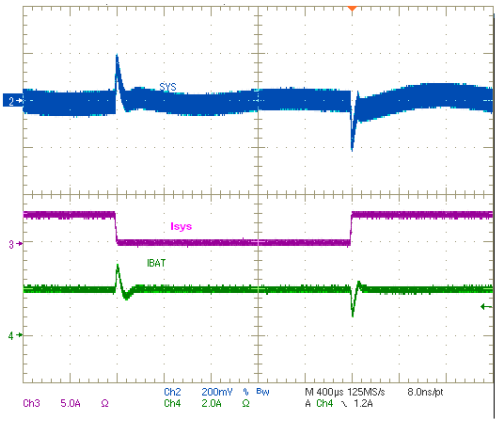
CH1: Input current, 2A/div; CH2: system load, 2A/div; CH3: IOUT, 1V/div; CH4: inductor current, 2A/div, 1ms/div

Figure 10. 0~3A System Load Transient (IDPM Disable and Charge Disable)



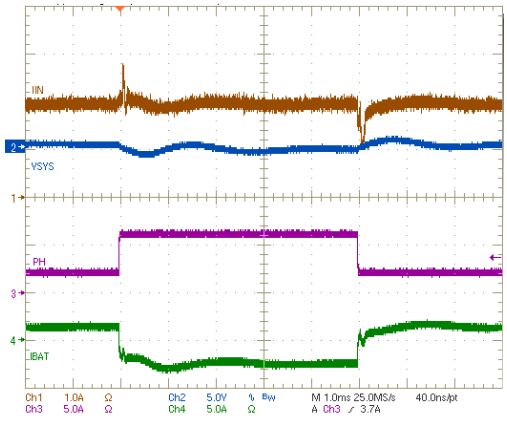
CH1: Input current, 2A/div; CH2: system load, 2A/div; CH3: IOUT, 1V/div; CH4: inductor current, 2A/div, 20µs/div

Figure 11. 2~6A System Load Transient (IDPM Disable and Charge Disable)



CH2: system voltage (AC), 200mV/div; CH3: system load current, 5A/div; CH4: battery charge current, 2A/div, 400us/div

Figure 12. 0~3A System Load Transient (IDPM Enable and Charge Enable)



CH1: input current, 1A/div; CH2: system voltage (AC), 5V/div; CH3: system load, 5A/div; CH4: battery charge current, 5A/div, 1ms/div

Figure 13. 2~6A System Load Transient (IDPM Enable and Charge Enable)

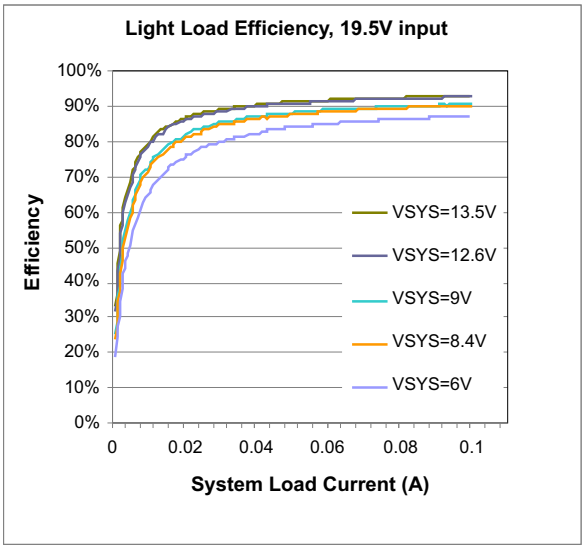


Figure 14. Light Load Efficiency vs. System Current

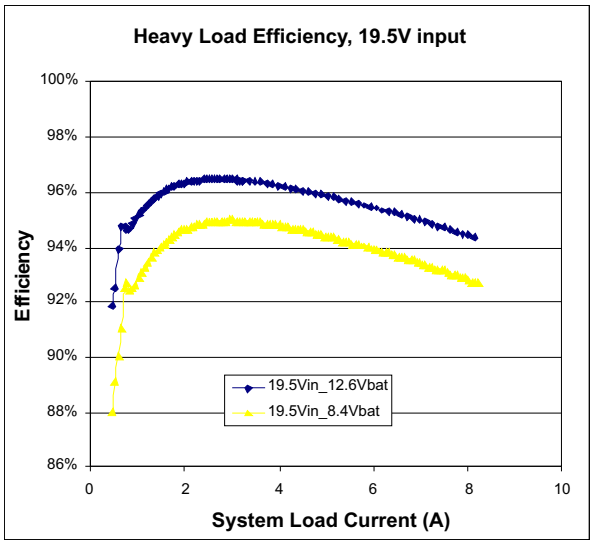


Figure 15. Heavy Load Efficiency vs. System Current

SMBus Communication

SMBus Interface

The bq24715J supports SMBus communication interface. Gas gauge broadcasting mode is supported.

The bq24715J operates as a slave, receiving control inputs from the embedded controller host through the SMBus interface. The bq24715J uses a simplified subset of the commands documented in System Management Bus Specification V1.1, which can be downloaded from www.smbus.org. The bq24715J uses the SMBus Read-Word and Write-Word protocols (Figure 16) to communicate with the smart battery. The bq24715J performs only as a SMBus slave device with address 0b00010010 (0x12H) and does not initiate communication on the bus. In addition, the bq24715J has two identification registers a 16-bit device ID register (0xFFH) and a 16-bit manufacturer ID register (0xFEH).

SMBus communication is enabled with the following conditions:

- V_{VCC} or V_{SRN} is above UVLO;

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors (10kΩ) for SDA and SCL to achieve rise times according to the SMBus specifications. Communication starts when the master signals a START condition, which is a high-to-low transition on SDA, while SCL is high. When the master has finished communicating, the master issues a STOP condition, which is a low-to-high transition on SDA, while SCL is high. The bus is then free for another transmission. Figure 17 and Figure 18 show the timing diagram for signals on the SMBus interface. The address byte, command byte, and data bytes are transmitted between the START and STOP conditions. The SDA state changes only while SCL is low, except for the START and STOP conditions. Data is transmitted in 8-bit bytes and is sampled on the rising edge of SCL. Nine clock cycles are required to transfer each byte in or out of the bq24715J because either the master or the slave acknowledges the receipt of the correct byte during the ninth clock cycle. The bq24715J supports the charger commands as described in Table 2.

a) Write-Word Format

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	ACK	P
	7 BITS	1b	1b	8 BITS	1b	8 BITS	1b	8 BITS	1b	
	MSB LSB	0	0	MSB LSB	0	MSB LSB	0	MSB LSB	0	

Preset to 0b0001001 **ChargeCurrent() = 0x14H** D7 D0 D15 D0
ChargeVoltage() = 0x15H
InputCurrent() = 0x3FH
MinSysVoltage() = 0x3EH
ChargeOption() = 0x12H

b) Read-Word Format

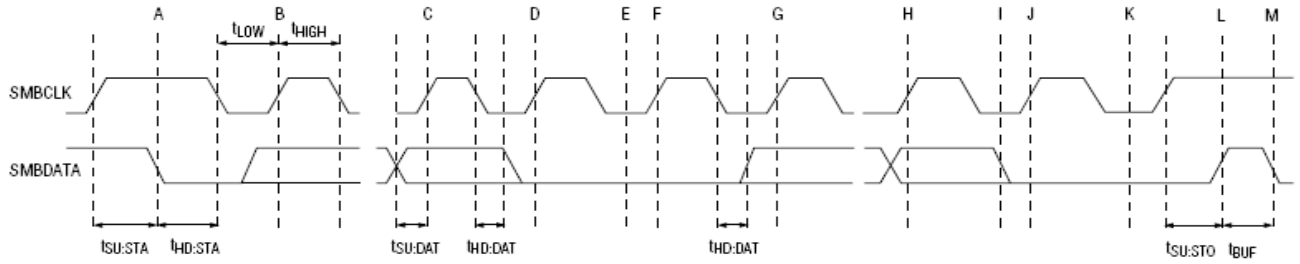
S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	S	SLAVE ADDRESS	R	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	NACK	P
	7 BITS	1b	1b	8 BITS	1b		8 BITS	1b	1b	8 BITS	1b	8 BITS	1b	
	MSB LSB	0	0	MSB LSB	0		MSB LSB	1	0	MSB LSB	0	MSB LSB	1	

Preset to 0b0001001 **DeviceID() = 0xFFH** Preset to 0b0001001 D7 D0 D15 D0
ManufactureID() = 0xFEH
ChargeCurrent() = 0x14H
ChargeVoltage() = 0x15H
InputCurrent() = 0x3FH
MinSysVoltage() = 0x3EH
ChargeOption() = 0x12H

LEGEND:
S = START CONDITION OR REPEATED START CONDITION
ACK = ACKNOWLEDGE (LOGIC-LOW)
W = WRITE BIT (LOGIC-LOW)
P = STOP CONDITION
NACK = NOT ACKNOWLEDGE (LOGIC-HIGH)
R = READ BIT (LOGIC-HIGH)

MASTER TO SLAVE
SLAVE TO MASTER

Figure 16. SMBus Write-Word and Read-Word Protocols



A = START CONDITION
B = MSB OF ADDRESS CLOCKED INTO SLAVE
C = LSB OF ADDRESS CLOCKED INTO SLAVE
D = R/$\overline{W}$ BIT CLOCKED INTO SLAVE
E = SLAVE PULLS SMBDATA LINE LOW
F = ACKNOWLEDGE BIT CLOCKED INTO MASTER
G = MSB OF DATA CLOCKED INTO SLAVE
H = LSB OF DATA CLOCKED INTO SLAVE
I = SLAVE PULLS SMBDATA LINE LOW
J = ACKNOWLEDGE CLOCKED INTO MASTER
K = ACKNOWLEDGE CLOCK PULSE
L = STOP CONDITION, DATA EXECUTED BY SLAVE
M = NEW START CONDITION

Figure 17. SMBus Writing Timing

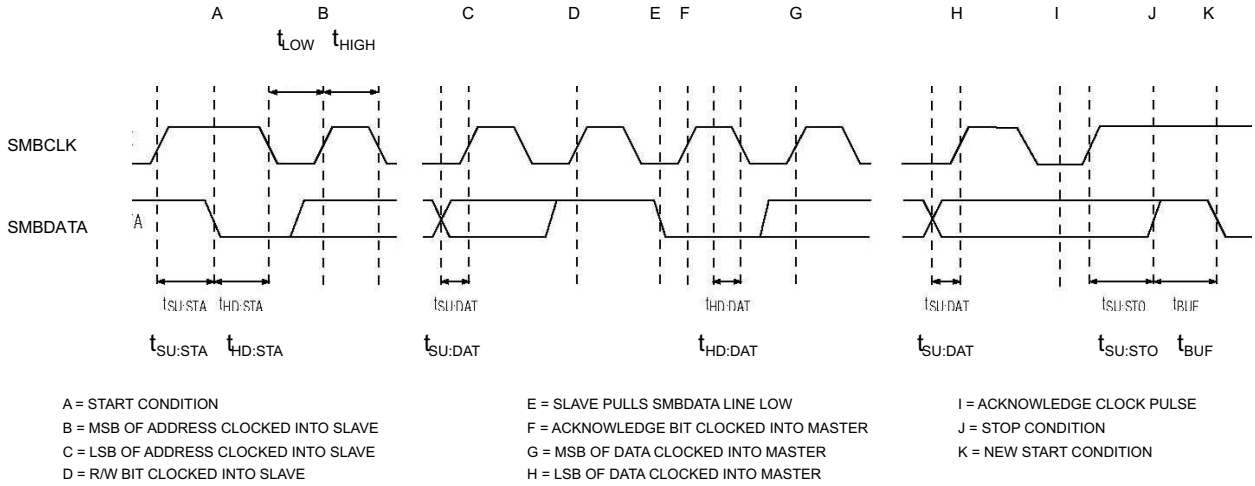


Figure 18. SMBus Read Timing

SMBus Commands

The bq24715J supports seven battery-charger commands that use either Write-Word or Read-Word protocols, as summarized in Table 2. ManufacturerID() and DeviceID() can be used to identify the bq24715J. The ManufacturerID() command always returns 0x0040H and the DeviceID() command always returns 0x0010H.

Table 2. Battery Charger Command Summary

REGISTER		READ/WRITE	DESCRIPTION	COMMENT
ADDRESS	NAME			
0x12H	ChargeOption()	Read or Write	Charger Options Control	● Default E144H
0x14H	ChargeCurrent()	Read or Write	7-Bit Charge Current Setting	● Default 0mA, 64mA Step ● Range:128mA -8.128A ● Bit [15] [14][13] value is ignored and counted as zero. Any value below 64mA results in zero. Write 64mA only is ignored ● 0mA disable charge
0x15H	MaxChargeVoltage()	Read or Write	11-Bit Charge Voltage Setting	● Default 2S-9V, 3S-13.5V; ● 16mV Step ● Range: 4.096V – 14.5V ● Any value below 4.096V results in 4.096V; not allow chargervoltage lower than minsystemvoltage
0x3EH	MinSystemVoltage()	Read or Write	6-Bit Minimum System Voltage Setting	● Default 2S-6.144V, 3S-9.216V; ● 256mV Step ● Range: 4.096V – 14.5V ● Any value out of range is ignored; not allow minsystemvoltage higher than chargervoltage.
0x3FH	InputCurrent()	Read or Write	7-Bit Input Current Setting	● Default 3.2A, 64mA Step ● Range:128mA -8.064A ● Any value out of range is ignored.
0xFEH	ManufacturerID()	Read Only	Manufacturer ID	0x0040H
0xFFH	DeviceID()	Read Only	Device ID	0x0010H

Setting Charger Options

By writing ChargeOption() command (0x12H or 0b00010010), bq24715J allows users to change several charger options after POR (Power On Reset) as shown in Table 3.

Table 3. Charge Options Register (0x12H)

BIT	BIT NAME	DESCRIPTION
[15]	LOWPOWER	Effective on BAT power only (ACDET<0.6 or VCC<UVLO) 0: turn on discharge current monitoring **1: lower quiescent current, discharge current monitoring are turned off <default @ POR>**
[14:13]	WATCHDOG Timer Adjust	Set maximum delay between consecutive SMBus Write charge voltage or charge current command. The charge will be suspended if IC does not receive write charge voltage or write charge current command within the watchdog time period and watchdog timer is enabled. The charge will be resumed after receive write charge voltage or write charge current command when watchdog timer expires and charge suspends. 00: Disable Watchdog Timer 01: Enabled, 44 sec 10: Enabled, 88 sec **11: Enable Watchdog Timer (175s) <default @ POR>**
[12]	SYSOVP	***Converter latch-off when sysovp is detected.*** ***0: 15.1V for 3s; 10.1V for 2s <default @ POR>*** *1:* 17.0V for 3s, 11.3V for 2s
[11]	SYSOVP status& clear	**0: not OVP (default; write 0 to clear the OVP status)** 1: OVP latch (read only)
[10]	Audio Frequency Limit	**0: No limit of switching frequency <default @ POR>** 1: Set minimum switching frequency to 40kHz to avoid audio noise
[9:8]	Switching Frequency Setting	00:600kHz **01:800kHz <default @ POR>** 10: 1MHz 11: 800 kHz
[7]	ACOC setting	ACOC protection threshold by detecting the ACP_ACN voltage. **0: function is disable <default @ POR>** 1: 333% IDPM
[6]	LSFET OCP threshold	When LSFET is ON, check the Rdson voltage drop, limit the current cycle-by-cycle 0: 250mV **1: 350mV <default>**
[5]	LEARN Enable	IC turns off buck converter (ACFET and RBFET still on), and turns on BATFET to support battery discharge mode. Set this bit 0 will stop LEARN mode and turn on buck converter back. Can be used to support battery LEARN mode **0: Disable LEARN Mode <default @ POR>** 1: Enable LEARN Mode
[4]	IOUT Selection	When bit[3]=1, bit[4] serve as input 0: IOUT is the 40x adapter current amplifier output 1: IOUT is the 16x discharge current amplifier output When bit[3]=0, bit[4] serve as output (indicate IOUT selection) **0: IOUT the 40x adapter current amplifier output; when IDPM is disabled <default @ POR>** 1: IOUT is the 16x discharge current amplifier output; when IDPM is enabled
[3]	FIX IOUT	**0: switch IOUT based on IDPM_EN <default @ POR>** 1: select IOUT based on bit[4]
[2]	LDO Mode Enable	0: Disable LDO mode. BATFET ON. Precharge current is set by battery pack LDO. **1: Enable LDO mode - Precharge current is set by ChargeCurrent() and clamped below 384mA <default@POR>**
[1]	IDPM_EN	**0: Disable <default @ POR>** 1: Enable
[0]	Charge Inhibit	**0: Enable Charge <default @ POR>** 1: Inhibit Charge

Setting the Charge Current

To set the charge current, write a 16bit ChargeCurrent() command (0x14H or 0b00010100) using the data format listed in Table 6. With 10mΩ sense resistor, the bq24715J provides a charge current range of 128mA to 8.128A, with 64mA step resolution. Sending ChargeCurrent() below 64mA clears the register and terminates charging. Upon POR, charge current is 0A. A 0.1µF capacitor between SRP and SRN for differential mode filtering is recommended, 0.1µF capacitor between SRN and ground for common mode filtering, and an optional 0.1µF capacitor between SRP and ground for common mode filtering.

The SRP and SRN pins are used to sense R_{SNS} with default value of 10mΩ. However, resistors of other values can also be used. For a larger sense resistor, a larger sense voltage is given, and a higher regulation accuracy; but, at the expense of higher conduction loss.

Because writing valid 0x14H will enable charge, even if 0x15H is not changed (0x15H has default value at start-up). EC needs write 0x15H – (charge voltage) first, then write 0x14H – (charge current). After enable charge, IC will regulate the charge voltage and current at 0x14H and 0x15H setting to reduce the risk for overcharging battery.

Table 4. Charge Current Register (0x14H), using 10mΩ sense resistor

BIT	BIT NAME	DESCRIPTION
0	—	Not used.
1	—	Not used.
2	—	Not used.
3	—	Not used.
4	—	Not used.
5	—	Not used.
6	Charge Current, DACICHG 0	0 = Adds 0mA of charger current. 1 = Adds 64mA of charger current.
7	Charge Current, DACICHG 1	0 = Adds 0mA of charger current. 1 = Adds 128mA of charger current.
8	Charge Current, DACICHG 2	0 = Adds 0mA of charger current. 1 = Adds 256mA of charger current.
9	Charge Current, DACICHG 3	0 = Adds 0mA of charger current. 1 = Adds 512mA of charger current.
10	Charge Current, DACICHG 4	0 = Adds 0mA of charger current. 1 = Adds 1024mA of charger current.
11	Charge Current, DACICHG 5	0 = Adds 0mA of charger current. 1 = Adds 2048mA of charger current.
12	Charge Current, DACICHG 6	0 = Adds 0mA of charger current. 1 = Adds 4096mA of charger current.
13	—	Not used.
14	—	Not used.
15	—	Not used.

Setting the Max Charge Voltage

To set the output charge regulation voltage, write a 16bit MaxChargeVoltage() command (0x15H or 0b00010101) using the data format listed in Table 5. The bq24715J provides charge voltage range from 4.096V to 9.6V (2S setting) or 14.5V (3S setting), with 16mV step resolution. Upon POR, Max charge voltage limit is 13.504V for 3S setting (CELL=HIGH) or 9.008V for 2S setting (CELL pin floating). Any value below 4.096V results in 4.096V.

If enable charge without writing any command to 0x15 register, the MaxChargeVoltage() is automatically changed to 8.4V (2S setting) or 12.6V (3S setting). If disable charge without writing any command to 0x15 register ever, the MaxChargeVoltage() automatically goes back to POR value. Once writing a valid number to 0x15 register, the MaxChargeVoltage() doesn't automatically change between enable charge and disable charge.

The SRN pin is used to sense the battery voltage for voltage regulation and should be connected as close to the battery as possible, and directly place a decoupling capacitor (0.1µF recommended) as close to IC as possible to decouple high frequency noise.

Table 5. Max Charge Voltage Register (0x15H)

BIT	BIT NAME	DESCRIPTION
0	—	Not used.
1	—	Not used.
2	—	Not used.
3	—	Not used.
4	Charge Voltage, DACV 0	0 = Adds 0mV of charger voltage. 1 = Adds 16mV of charger voltage.
5	Charge Voltage, DACV 1	0 = Adds 0mV of charger voltage. 1 = Adds 32mV of charger voltage.
6	Charge Voltage, DACV 2	0 = Adds 0mV of charger voltage. 1 = Adds 64mV of charger voltage.
7	Charge Voltage, DACV 3	0 = Adds 0mV of charger voltage. 1 = Adds 128mV of charger voltage.
8	Charge Voltage, DACV 4	0 = Adds 0mV of charger voltage. 1 = Adds 256mV of charger voltage.
9	Charge Voltage, DACV 5	0 = Adds 0mV of charger voltage. 1 = Adds 512mV of charger voltage.
10	Charge Voltage, DACV 6	0 = Adds 0mV of charger voltage. 1 = Adds 1024mV of charger voltage.
11	Charge Voltage, DACV 7	0 = Adds 0mV of charger voltage. 1 = Adds 2048mV of charger voltage.
12	Charge Voltage, DACV 8	0 = Adds 0mV of charger voltage. 1 = Adds 4096mV of charger voltage.
13	Charge Voltage, DACV 9	0 = Adds 0mV of charger voltage. 1 = Adds 8192mV of charger voltage.
14	Charge Voltage, DACV 9	0 = Adds 0mV of charger voltage. 1 = Adds 16384mV of charger voltage.
15	—	Not used.

Setting the Minimum System Voltage

To set the minimum system voltage, write a 16bit MinSystemVoltage() command (0x3EH or 0b00111110) using the data format listed in Table 6. The bq24715J provides minimum system voltage range from 4.096V up to maximum charge voltage, with 256mV step resolution. Any MinSystemVoltage() below 4.096V. Upon POR (set via CELL), charge voltage limit is 6.144V for 2S setting and 9.216V for 3S setting.

Table 6. Minimum System Voltage Register (0x3EH)

BIT	BIT NAME	DESCRIPTION
0	—	Not used.
1	—	Not used.
2	—	Not used.
3	—	Not used.
4	—	Not used.
5	—	Not used.
6	—	Not used.
7	—	Not used.
8	Minimum System Voltage, DACMINSV 0	0 = Adds 0mV of system voltage. 1 = Adds 256mV of system voltage.
9	Minimum System Voltage, DACMINSV 1	0 = Adds 0mV of system voltage. 1 = Adds 512mV of system voltage.
10	Minimum System Voltage, DACMINSV 2	0 = Adds 0mV of system voltage. 1 = Adds 1024mV of system voltage.
11	Minimum System Voltage, DACMINSV 3	0 = Adds 0mV of system voltage. 1 = Adds 2048mV of system voltage.
12	Minimum System Voltage, DACMINSV 4	0 = Adds 0mV of system voltage. 1 = Adds 4096mV of system voltage.
13	Minimum System Voltage, DACMINSV 5	0 = Adds 0mV of system voltage. 1 = Adds 8192mV of system voltage.
14	—	Not used.
15	—	Not used.

Setting Input Current

System current normally fluctuates as portions of the system are powered up or put to sleep. With the input current limit, the output current requirement of the AC wall adapter can be lowered, reducing system cost.

The total input current, from a wall cube or other DC source, is the sum of the system supply current and the current required by the charger. When the input current exceeds the set input current limit, the bq24715J decreases the charge current to provide priority to system load current. As the system current rises, the available charge current drops linearly to zero. Thereafter, all input current goes to system load and input current increases.

During DPM regulation, the total input current is the sum of the device supply current I_{BIAS}, the charger input current, and the system load current I_{LOAD}, and can be estimated as follows:

$$I_{INPUT} = \left[\frac{I_{LOAD} V_{SYS} + I_{BATTERY} \times V_{BATTERY}}{V_{IN} \times \eta} \right] + I_{BIAS} \quad (1)$$

where η is the efficiency of the charger buck converter (typically 85% to 95%).

To set the input current limit, write a 16-bit InputCurrent() command (0x3FH or 0b00111111) using the data format listed in Table 7. When using a 10mΩ sense resistor, the bq24715J provides an input-current limit range of 128mA to 8.064A, with 64mA resolution. Sending InputCurrent() below 128mA or above 8.064A will be ignored. Upon POR, default input current limit is 3.2A.

The ACP and ACN pins are used to sense R_{AC} with default value of 10mΩ. However, resistors of other values can also be used. For a larger sense resistor, larger sense voltage is given, and a higher regulation accuracy; but, at the expense of higher conduction loss.

Table 7. Input Current Register (0x3FH), using 10mΩ Sense Resistor

BIT	BIT NAME	DESCRIPTION
0	—	Not used.
1	—	Not used.
2	—	Not used.
3	—	Not used.
4	—	Not used.
5	—	Not used.
6	Input Current, DACIIN 0	0 = Adds 0mA of input current. 1 = Adds 64mA of input current.
7	Input Current, DACIIN 1	0 = Adds 0mA of input current. 1 = Adds 128mA of input current.
8	Input Current, DACIIN 2	0 = Adds 0mA of input current. 1 = Adds 256mA of input current.
9	Input Current, DACIIN 3	0 = Adds 0mA of input current. 1 = Adds 512mA of input current.
10	Input Current, DACIIN 4	0 = Adds 0mA of input current. 1 = Adds 1024mA of input current.
11	Input Current, DACIIN 5	0 = Adds 0mA of input current. 1 = Adds 2048mA of input current.
12	Input Current, DACIIN 6	0 = Adds 0mA of input current. 1 = Adds 4096mA of input current.
13	—	Not used.
14	—	Not used.
15	—	Not used.

Adapter Over-Voltage Protection (ACOVP)

The bq24715J uses a fixed ACOVP voltage (26V typ). When VCC pin voltage is higher than V_{ACOVP}, it is considered as adapter over voltage. ACOK will be pulled low, and charge will be disabled. ACFET will be turned off to disconnect high voltage adapter during ACOVP. BATFET will be turned on if turn-on conditions are valid. See the "ACFET/RBFET and BATFET Control" sections for detail.

When VCC pin voltage falls below 24V and ACDET above 2.4V, it is considered as adapter voltage returns back to normal voltage. ACOK will be pulled high by external pull up resistor. ACFET and RBFET will be turned on to power the converter from adapter.

Adapter Detect and ACOK Output

The bq24715J uses an ACOK comparator to determine the present of adapter on VCC pin. An external resistor voltage divider attenuates the adapter voltage before it goes to ACDET. The V_{ACOK_RISE} threshold should make the adapter voltage greater than the maximum battery voltage plus VCC_SRN (sleep) comparator rising threshold, but lower than the maximum allowed V_{ACOVP} voltage.

The open drain ACOK output requires external pull up resistor to system digital rail for a high level. It can be pulled to external rail under the following conditions:

- $V_{ACOVP} > V_{VCC} >$ UVLO;
- $V_{ACDET} > 2.4V$
- V_{VCC}-$V_{SRN} > 675mV$ (not in sleep mode);

ACFET/RBFET Control

The ACDRV drives a pair of common-source (CMSRC) n-channel power MOSFETs (ACFET: Q1A and RBFET: Q1B) between adapter and converter. The ACFET separates adapter from converter, and provides a limited di/dt when plugging in adapter by controlling the ACFET turn-on time. The RBFET provides battery discharge protection when adapter voltage is lower than battery, and minimizes system power dissipation with its low $R_{DS(on)}$ compared to a Schottky diode.

When adapter is not present, ACDRV is pulled to CMSRC to keep ACFET and RBFET off. And BATFET is turned on to discharge battery. After adapter is detected (ACDET pin voltage higher than 2.4V), adapter begins to provide power to system.

The gate drive voltage on ACFET and RBFET is V_{CMSRC}+6V. If the ACFET and RBFET have been turned on for 20ms, and the voltage across ACDRV and CMSRC is still 0.2V below V_{ACFET}, ACFET and RBFET will be turned off.

To limit the in-rush current on ACDRV pin and CMSRC pin, a 4kΩ resistor is recommended on each of the three pins.

To limit the adapter inrush current when ACFET is turned on to provide power converter from adapter, the external Cgs and Cgd capacitor of ACFET must be carefully selected. The larger the Cgs and Cgd capacitance, the slower turn on of ACFET will be and less inrush current of adapter. However, if Cgs and Cgd is too large, the ACDRV-CMSRC voltage may still be low after 20ms turn on time window is expired. To make sure ACFET will not be turned on when adapter is hot plug in, the Cgs value should be 20 times or higher of Cgd.

LDO MODE AND MINIMUM SYSTEM VOLTAGE

The $\overline{\text{BATDRV}}$ drives a p-channel BATFET between converter output (system node) and battery to provide a charge and discharge path for battery. When battery voltage is below the minimum system voltage setting, this BATFET works in linear mode as LDO (default chargeoption() bit[2]=1, the precharge current is set by ChargeCurrent() and clamped below 384mA) thus to keep system node voltage always higher than the minimum system voltage setting. If battery voltage reaches the minimum system voltage, BATFET fully turns on. This LDO function can be optionally disabled by set "LDO Mode Enable" bit low (chargeoption() bit[2]=0) and BATFET is fully turned on. At this condition, the battery pack internal circuit will maintain battery terminal voltage higher than system minimum voltage. And the precharge current also determined by battery pack internal circuit.

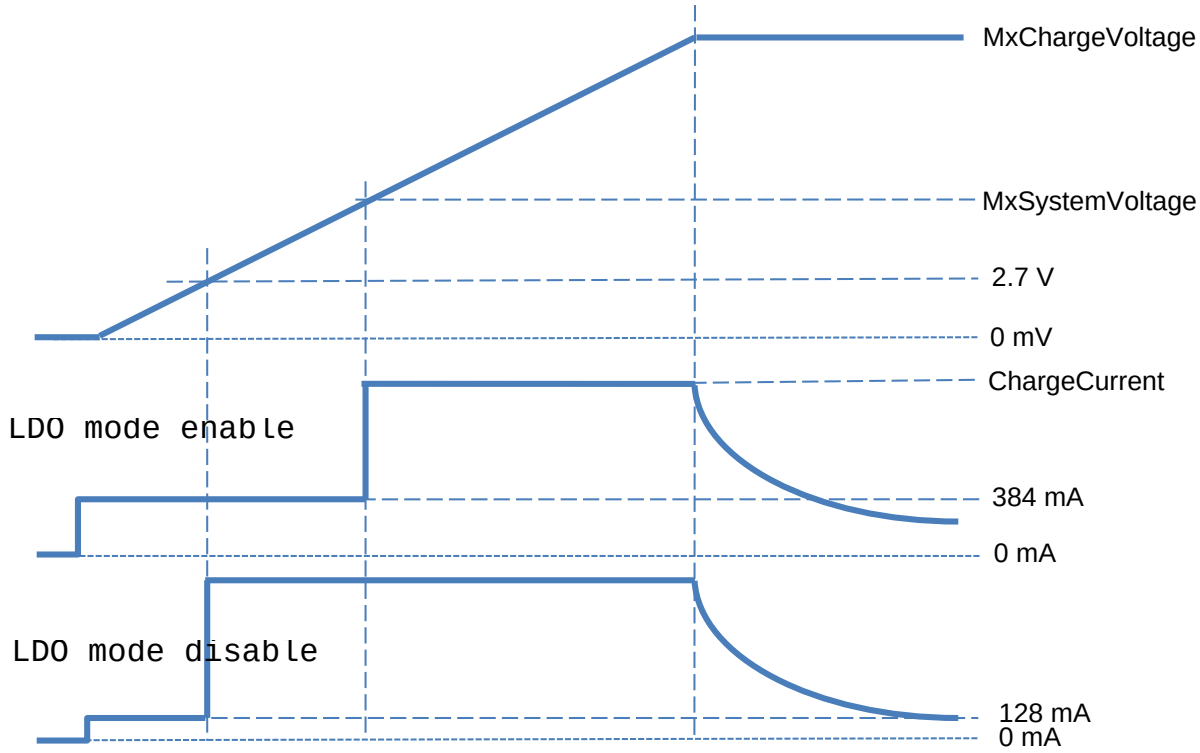


Figure 19. ChargeOption[2] (LDO Mode)

Register Setting

- ChargeOption 0x12H : 0x820E
- ChargeCurrent 0x14H: 0x0E80 (3712mA)
- MaxChargeVoltage 0x15H : 0x21D0 (8656mV)
- MinSystemVoltage 0x3EH : 0x1800 (6144mV)
- InputCurrent 0x3FH: 0x0C80

DPM

When the input current exceeds the input current limit setting and IPM_EN is enabled (ChargeOption() bit [1]=1), the bq24715J decreases the charge current to provide priority to system load current. As the system current rises, the available charge current drops linearly to zero. Higher systems loads can be drawn from the battery, battery discharges and BATFET is turned on when discharge current is higher than 256mA.

To reduce the risk for overcharging battery at battery insertion, please disable charge if the battery is absent.

Buck Converter Power up

After the ACFET is turned on, the converter is enabled and the HSFET and LSFET start switching. Every time the buck converter is started, the IC automatically applies soft-start (no soft-start when exit LEARN) on buck output current to avoid any overshoot or stress on the output capacitors or the power converter. The buck output current starts at 128mA, and the step size is 64mA in CCM mode for a 10mΩ current sensing resistor. Each step lasts around 24µs in CCM mode, until it reaches the programmed charge current limit. No external components are needed for this function.

When power up, converter output voltage is default value set by CELL pin configuration. After converter starts switching about 100ms, CELL pin setting is locked. If CELL pin is pulled to LOW when power-up, converter output is default 2S for bq24715J.

PWM Mode Converter Operation

The synchronous buck PWM converter uses a fixed frequency voltage control scheme and internal type III compensation network. The LC output filter gives a characteristic resonant frequency

$$f_o = \frac{1}{2\pi\sqrt{L_o C_o}} \quad (2)$$

The resonant frequency fo is used to determine the compensation to ensure there is sufficient phase margin for the target bandwidth. Suggested component value as charge current of 800Hz default switching frequency is shown in Table 8.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the output capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high output voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point.

Table 8. Suggested Component Value as Output Current of Default 800kHz Switching Frequency

Component	Recommended Value
Output Inductor Lo (µH)	3.3 or 2.2
System node capacitor (µF)	47- 350 (1)
SRN node Capacitor Co (µF)	0.1-1
Sense Resistor (mΩ)	10

(1) If system capacitance is higher than 350µF, please contact TI techniclal support.

The bq24715J/17 has four loops of regulation: input current, charge current, charge voltage and minimum system voltage. The four loops are brought together internally at the error amplifier. The maximum voltage of the four loops appears at the output of the error amplifier EAO. An internal saw-tooth ramp is compared to the internal error control signal EAO to vary the duty-cycle of the converter.

When the battery charge voltage approaches the input voltage, EAO signal is allowed to exceed the saw-tooth ramp peak in order to get a 100% duty-cycle. If voltage across BTST and PHASE pins falls below $V_{BTST\_REFRESH}$, a refresh cycle starts and low-side n-channel power MOSFET is turned on to recharge the BTST capacitor. It can achieve duty cycle of up to 99.5% with pulse skip.

Switching Frequency Adjust

The charger switching frequency can be adjusted ±25% to solve EMI issue via SMBus command. ChargeOption() bit [9:8] can be used to set switching frequency.

If frequency is reduced, the current ripple is increased. Inductor value must be carefully selected so that it will not trigger cycle-by-cycle peak over current protection even for the worst condition such as higher input voltage, 50% duty cycle, lower inductance and lower switching frequency.

Continuous Conduction Mode (CCM)

With sufficient charge current, the inductor current never crosses zero, which is defined as Continuous Conduction Mode. The controller starts a new cycle with ramp coming up from 200mV. As long as EAO voltage is above the ramp voltage, the high-side MOSFET (HSFET) stays on. When the ramp voltage exceeds EAO voltage, HSFET turns off and low-side MOSFET (LSFET) turns on. At the end of each switching cycle, ramp gets reset and LSFET turns off, ready for the next cycle. There is always break-before-make logic during transition to prevent cross-conduction and shoot-through. During the dead time when both MOSFETs are off, the body-diode of the low-side power MOSFET conducts the inductor current.

During CCM mode, the inductor current is always flowing and creates a fixed two-pole system. Having the LSFET turn-on keeps the power dissipation low, and allows safely at high output currents.

Discontinuous Conduction Mode (DCM)

When LSFET is turned on, the inductor current will decrease. If this current goes to zero, the converter enters Discontinuous Conduction Mode. Every cycle, when the voltage across ACP and ACN falls below 1.25mV (125mA on 10mΩ), the light-load comparator turns off LSFET to avoid negative inductor current, which may boost the system via the body diode of HSFET. There is also a cycle-by-cycle converter under-current comparator monitor the LFET current and prevent it goes negative.

During the DCM mode the loop response automatically changes. It changes to a single pole system and the pole is proportional to the load current.

PFM Mode

In order to improve converter light-load efficiency, the bq24715J switches to PFM control at light load with charge disable or charge in LDO mode. The effective switching frequency will decrease accordingly when system load decreases. The minimum frequency can be limit to 40kHz if set IDPM_EN bit high (ChargeOption() bit[10]=1). To have higher light load efficiency, set "Audio Frequency Limit" bit low (Chargeoption() bit[10]=0, default).

Learn Mode

A battery LEARN cycle can be activated via SMBus "LEARN Enable" command (ChargeOption() bit[5]=1 enable Learn Mode). When LEARN is enabled with an adapter connected, the system power switch to battery by turning off converter and keep ACFET/BATFET on. Learn mode allows the battery to discharge in order to calibrate the battery gas gauge over a complete discharge/charge cycle. When LEARN is disabled, the system power switch to adapter by turning on converter in a few hundreds µs.

bq24715J also supports hardware pin to exist LEARN mode by pulling CELL to GND. When Cell pin is pulled to GND, bq24715J resets "LEARN Enable" (ChargeOption() bit[5]) and IDPM_EN (ChargeOption() bit[1]), and reset chargevoltage() and chargecurrent().

I_{DPM} Disable at Battery Removal

CELL pull to GND can also be used to disable I_{DPM} function automatically when battery is removed.

When battery present, IOUT monitors discharge current and CPU can do throttling when IOUT is higher than battery discharge limit.

When battery is removed, CELL is pulled to GND. IC disables input DPM function and switch IOUT to monitor input current, thus CPU throttling when IOUT higher than limit.

After insert battery back, EC need set bit[1]=1 to enable IDPM function.

- Customer who has external discharge current monitor can set "FIX IOUT" ChargeOption() bit[3]=1 and "IOUT Selection" ChargeOption() bit[4]=0 to have fixed IOUT monitoring adapter current.
- Customer who has external adapter current monitor can set "FIX IOUT" ChargeOption() bit[3]=1 and "IOUT Selection" ChargeOption() bit[4]=1 to have fixed IOUT monitoring discharge current.

High Accuracy Current Sense Amplifiers

If LOWPOWER bit is zero (ChargeOption() bit[15] = 0), as an industry standard, high accuracy current sense amplifiers (CSA) are used to monitor the input current or the discharge current, selectable via SMBUS, see Table 3. Once VCC is above UVLO and ACDET is above 0.6V, input current CSA turns on and the IOUT output becomes valid. Once SRN is above UVLO and ChargeOption() bit[15] = 0, discharge current CSA turns on and the IOUT output becomes valid. The CSA senses voltage across the input sense resistor by a factor of 40 or across the output sense resistor by a factor of 16 through the IOUT pin. To lower the voltage on current monitoring, a resistor divider from IOUT to GND can be used and accuracy over temperature can still be achieved.

If LOWPOWER bit is "1" (ChargeOption() bit[15] = 1) and only a valid battery (BAT>UVLO) is connected to system with an input adaptor (ACDET<0.6V or VCC<UVLO), the IC enter low quiescent current mode, all current monitoring circuits are turned off.

A 100pF capacitor connected on the output is recommended for decoupling high-frequency noise. An additional RC filter is optional, if additional filtering is desired. Note that adding filtering also adds additional response delay.

Charger Timeout

The bq24715J includes a watchdog timer to terminate charging if the charger does not receive a write ChargeVoltage() or write ChargeCurrent() command within 175s (adjustable via ChargeOption() command). If a watchdog timeout occurs all register values keep unchanged but charge is suspended. Write ChargeVoltage() or write ChargeCurrent() commands must be re-sent to reset watchdog timer and resume charging. The watchdog timer can be disabled, or set to 44s, 88s or 175s via SMBus command (ChargeOption() bit[14:13]). If watchdog is in timeout, disabling watchdog timer by writing ChargeOption() bit[14:13] also resumes charging.

Input Over-Current Protection (ACOC)

If the input current exceeds the 3.33X of input current DAC set point, ACFET/RBFET is turned-off and charge is disabled. After 300ms, ACFET/RBFET will be turned on again.

The ACOC function threshold can be set to 3.33X of input DPM current (ChargeOption() bit [7]=1) or function disable(ChargeOption() bit [7]=0, default) via SMBus command

The bq24715J has a cycle-to-cycle peak over-current protection. It monitors the voltage across Rds_on of the LSFET or the input current sense resistor, and prevents the converter from over current condition. The high-side gate drive turns off when the over-current is detected, and resumes automatically when the over-current condition is gone.

Converter Over-Current Protection

When LODRV pulse is longer than 100ns blanking time, the LSFET OCP is active and the threshold is automatically set to 350mV (ChargeOption() bit [6]=1, default) or 250mV (ChargeOption() bit [6]=0) via SMBus command. The blanking time prevents noise when MOSFET just turn on.

When LODRV pulse is shorter than 100ns blanking time, bq24715J uses 2.5 times of InputCurrent() setting (minimum 45mV) as Vacp-acn protection threshold to turn off the high-side gate drive even the IDPM function is disabled (0x12[1]=0). Set InputCurrent() to a right value even IDPM is disabled.

Battery Over-Voltage Protection (BATOVP)

The bq24715J will not allow the BATFET to turn-on when the battery voltage at SRN exceeds 104% of the regulation voltage set-point. This allows quick response to an over-voltage condition – such as occurs when the load is removed or the battery is disconnected. A 4mA current sink from SRP to GND is on only during BATOVP and allows discharging the stored output inductor energy that is transferred to the output capacitors.

System Over-Voltage Protection (SYSOVP)

When system voltage is higher than maximum allowed voltage (V_{SYSOVP_RISE}), it is considered as system overvoltage. If SYSOVP is detected, it will latch off ACFET, RBFET, and buck converter to prevent any potential damage to the system due to unexpected short (e.g. high HFET short) or other conditions. Reading chargeoption bit[11]=1 reflect this latch-off protection and writing chargeoption bit[11]=0 clear the latch. Adapter replug-in can also clear the latch.

Thermal Shutdown Protection (T_{SHUT})

The QFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junctions temperatures low. As added level of protection, the charger converter turns off for self-protection whenever the junction temperature exceeds the 155°C. The charger stays off until the junction temperature falls below 135°C. During thermal shut down, the REGN LDO current limit is reduced to 16mA. Once the temperature falls below 135°C, charge can be resumed with soft start.

Component List for Typical Application Circuit

Table 9. Component List for Figure 3

PART DESIGNATOR	QTY	DESCRIPTION
C1, C3, C4, C9, C13,	5	Capacitor, Ceramic, 0.1µF, 25V, 10%, X7R, 0603
C2, C5, C7, C12	2	Capacitor, Ceramic, 1µF, 25V, 10%, X7R, 0603
C6, C10	4	Capacitor, Ceramic, 10µF, 25V, 10%, X7R, 1206
C8	1	Capacitor, Ceramic, 0.047µF, 25V, 10%, X7R, 0603
C11	1	Capacitor, Ceramic, 100pF, 25V, 10%, X7R, 0603
Csys	1	Capacitor, Electrolytic, 220µF, 25V
D1, D2	2	Diode, Schottky, 30V, 200mA, SOT-23, Fairchild, BAT54
Q1	1	Dual N-channel MOSFET, 30V, SON3.3X3.3, TI, CSD87312Q3E
Q2	1	P-channel MOSFET, -20V, SON3.3X3.3, TI, CSD25401Q3
Q3, Q4	2	N-channel MOSFET, 30V, SON3.3X3.3, TI, CSD17308Q3
L1	1	Inductor, SMT, 9.2A, 16.5mohm, Vishay, IHLP3232DZER3R3M01
R1	1	Resistor, Chip, 430kΩ, 1/10W, 1%, 0603
R2	1	Resistor, Chip, 66.5kΩ, 1/10W, 1%, 0603
R3, R4	2	Resistor, Chip, 4.02kΩ, 1/10W, 1%, 0603
R5	1	Resistor, Chip, 15Ω, 1/4W, 5%, 0603
R6	1	Resistor, Chip, 10Ω, 1/4W, 1%, 1206
R7, R8, R9	3	Resistor, Chip, 10.0kΩ, 1/10W, 1%, 0603
RAC, Rsns	2	Resistor, Chip, 0.01Ω, 1/2W, 1%, 1206
U1	1	Charger controller, 20 pin VQFN, TI, bq24715JRGR

APPLICATION INFORMATION

Inductor Selection

The bq24715J has three selectable fixed switching frequency. Higher switching frequency allows the use of smaller inductor and capacitor values. Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \quad (3)$$

The inductor ripple current depends on input voltage (V_{IN}), duty cycle ($D = V_{OUT}/V_{IN}$), switching frequency (f_S) and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{f_S \times L} \quad (4)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. For example, the battery charging voltage range is from 9V to 12.6V for 3-cell battery pack. For 20V adapter voltage, 10V battery voltage gives the maximum inductor ripple current. Another example is 2-cell battery, the battery voltage range is from 6V to 8.4V, and 8.4V battery voltage gives the maximum inductor ripple current.

Usually inductor ripple is designed in the range of (20-40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current occurs where the duty cycle is closest to 50% and can be estimated by Equation 5:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \quad (5)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25V rating or higher capacitor is preferred for 19-20V input voltage. 10-20µF capacitance is suggested for typical of 3-4A charging current.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the input capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high input voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point.

Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (6)$$

The preferred ceramic capacitor is 25V X7R or X5R for output capacitor. Capacitance of 47µF ~ 350µF is suggested for the output capacitor. Place the capacitors after charging current sensing resistor to get the best charge current regulation accuracy.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the output capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high output voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point.

Power MOSFETs Selection

Two external N-channel MOSFETs are used for a synchronous switching battery charger. The gate drivers are internally integrated into the IC with 6V of gate drive voltage. 30V or higher voltage rating MOSFETs are preferred for 19-20V input voltage.

Figure-of-merit (FOM) is usually used for selecting proper MOSFET based on a tradeoff between the conduction loss and switching loss. For the top side MOSFET, FOM is defined as the product of a MOSFET's on-resistance, $R_{DS(ON)}$, and the gate-to-drain charge, Q_{GD}. For the bottom side MOSFET, FOM is defined as the product of the MOSFET's on-resistance, $R_{DS(ON)}$, and the total gate charge, Q_G.

$$FOM_{top} = R_{DS(on)} \times Q_{GD};\ FOM_{bottom} = R_{DS(on)} \times Q_G \quad (7)$$

The lower the FOM value, the lower the total power loss. Usually lower $R_{DS(ON)}$ has higher cost with the same package size.

The top-side MOSFET loss includes conduction loss and switching loss. It is a function of duty cycle ($D=V_{OUT}/V_{IN}$), charging current (I_{CHG}), MOSFET's on-resistance ($R_{DS(ON)}$), input voltage (V_{IN}), switching frequency (f_S), turn on time (t_{on}) and turn off time (t_{off}):

$$P_{top} = D \times I_{CHG}^2 \times R_{DS(on)} + \frac{1}{2} \times V_{IN} \times I_{CHG} \times (t_{on} + t_{off}) \times f_s \quad (8)$$

The first item represents the conduction loss. Usually MOSFET $R_{DS(ON)}$ increases by 50% with 100°C junction temperature rise. The second term represents the switching loss. The MOSFET turn-on and turn-off times are given by:

$$t_{on} = \frac{Q_{SW}}{I_{on}},\quad t_{off} = \frac{Q_{SW}}{I_{off}} \quad (9)$$

where Q_{sw} is the switching charge, I_{on} is the turn-on gate driving current and I_{off} is the turn-off gate driving current. If the switching charge is not given in MOSFET datasheet, it can be estimated by gate-to-drain charge (Q_{GD}) and gate-to-source charge (Q_{GS}):

$$Q_{SW} = Q_{GD} + \frac{1}{2} \times Q_{GS} \quad (10)$$

Gate driving current can be estimated by REGN voltage (V_{REGN}), MOSFET plateau voltage (V_{plt}), total turn-on gate resistance (R_{on}) and turn-off gate resistance (R_{off}) of the gate driver:

$$I_{on} = \frac{V_{REGN} - V_{plt}}{R_{on}},\quad I_{off} = \frac{V_{plt}}{R_{off}} \quad (11)$$

The conduction loss of the bottom-side MOSFET is calculated with the following equation when it operates in synchronous continuous conduction mode:

$$P_{bottom} = (1 - D) \times I_{CHG}^2 \times R_{DS(on)} \quad (12)$$

When charger operates in non-synchronous mode, the bottom-side MOSFET is off. As a result all the freewheeling current goes through the body-diode of the bottom-side MOSFET. The body diode power loss depends on its forward voltage drop (V_F), non-synchronous mode charging current ($I_{NONSYNC}$), and duty cycle (D).

$$P_D = V_F \times I_{NONSYNC} \times (1 - D) \quad (13)$$

The maximum charging current in non-synchronous mode can be up to 0.25A for a 10mΩ charging current sensing resistor or 0.5A if battery voltage is below 2.5V. The minimum duty cycle happens at lowest battery voltage. Choose the bottom-side MOSFET with either an internal Schottky or body diode capable of carrying the maximum non-synchronous mode charging current.

Input Filter Design

During adapter hot plug-in, the parasitic inductance and input capacitor from the adapter cable form a second order system. The voltage spike at VCC pin maybe beyond IC maximum voltage rating and damage IC. The input filter must be carefully designed and tested to prevent over voltage event on VCC pin.

There are several methods to damping or limit the over voltage spike during adapter hot plug-in. An electrolytic capacitor with high ESR as an input capacitor can damp the over voltage spike well below the IC maximum pin voltage rating. A high current capability TVS Zener diode can also limit the over voltage level to an IC safe level. However these two solutions may not have low cost or small size.

A cost effective and small size solution is shown in Figure 20. The R1 and C1 are composed of a damping RC network to damp the hot plug-in oscillation. As a result the over voltage spike is limited to a safe level. D1 is used for reverse voltage protection for VCC pin. C2 is VCC pin decoupling capacitor and it should be place to VCC pin as close as possible. C2 value should be less than C1 value so R1 can dominant the equivalent ESR value to get enough damping effect. R2 is used to limit inrush current of D1 to prevent D1 getting damage when adapter hot plug-in. R2 and C2 should have 10us time constant to limit the dv/dt on VCC pin to reduce inrush current when adapter hot plug in. R1 has high inrush current. R1 package must be sized enough to handle inrush current power loss according to resistor manufacturer's datasheet. The filter components value always need to be verified with real application and minor adjustments may need to fit in the real application circuit.

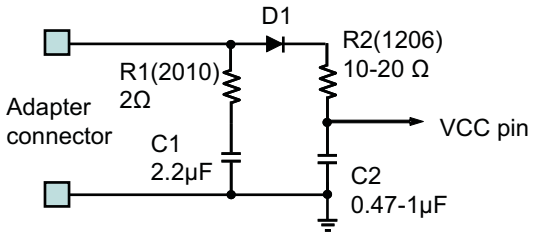


Figure 20. Input Filter

PCB Layout Guideline

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 21) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

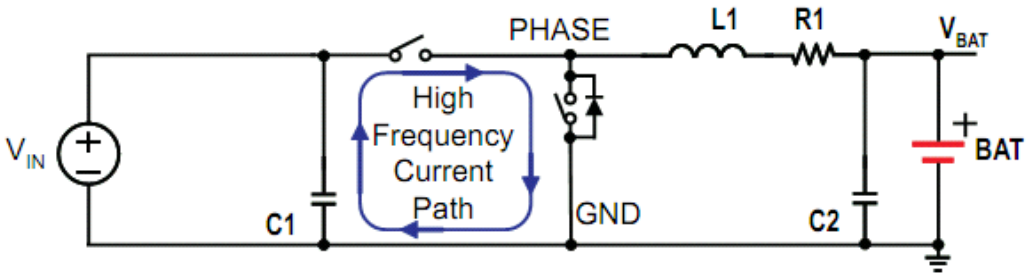


Figure 21. High Frequency Current Path

1. Place input capacitor as close as possible to switching MOSFET's supply and ground connections and use shortest copper trace connection. These parts should be placed on the same layer of PCB instead of on different layers and using vias to make this connection.
2. The IC should be placed close to the switching MOSFET's gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the other side of the PCB of switching MOSFETs.
3. Place inductor input terminal to switching MOSFET's output terminal as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
4. The charging current sensing resistor should be placed right next to the inductor output. Route the sense leads connected across the sensing resistor back to the IC in same layer, close to each other (minimize loop area) and do not route the sense leads through a high-current path (see Figure 21 for Kelvin connection for best current accuracy). Place decoupling capacitor on these traces next to the IC.

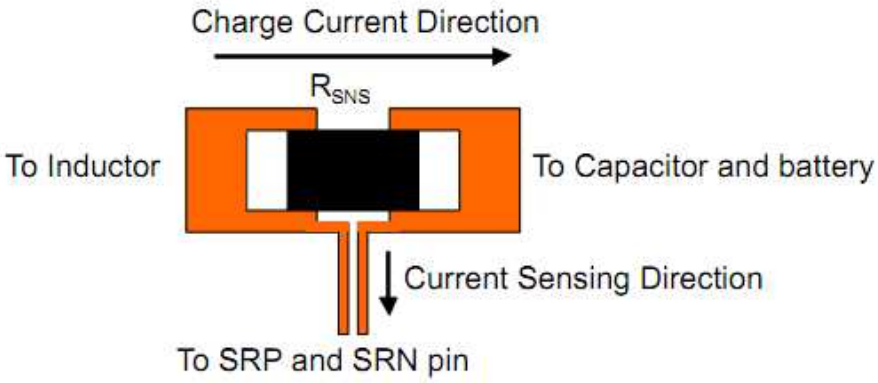


Figure 22. Sensing Resistor PCB Layout

5. Place output capacitor next to the sensing resistor output and ground.
6. Output capacitor ground connections need to be tied to the same copper that connects to the input capacitor ground before connecting to system ground.
7. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC use analog ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
8. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using power pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground (power pad should tie to

analog ground in this case if possible).

9. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.
10. It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
11. The via size and number should be enough for a given current path.

See the EVM design for the recommended component placement with trace and via locations. For the QFN information, refer to SCBA017 and SLUA271.

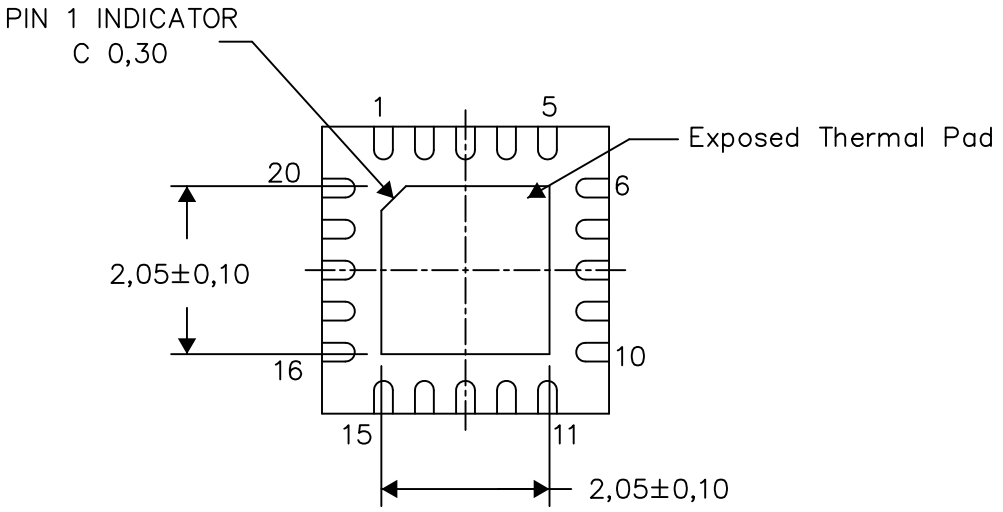
RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



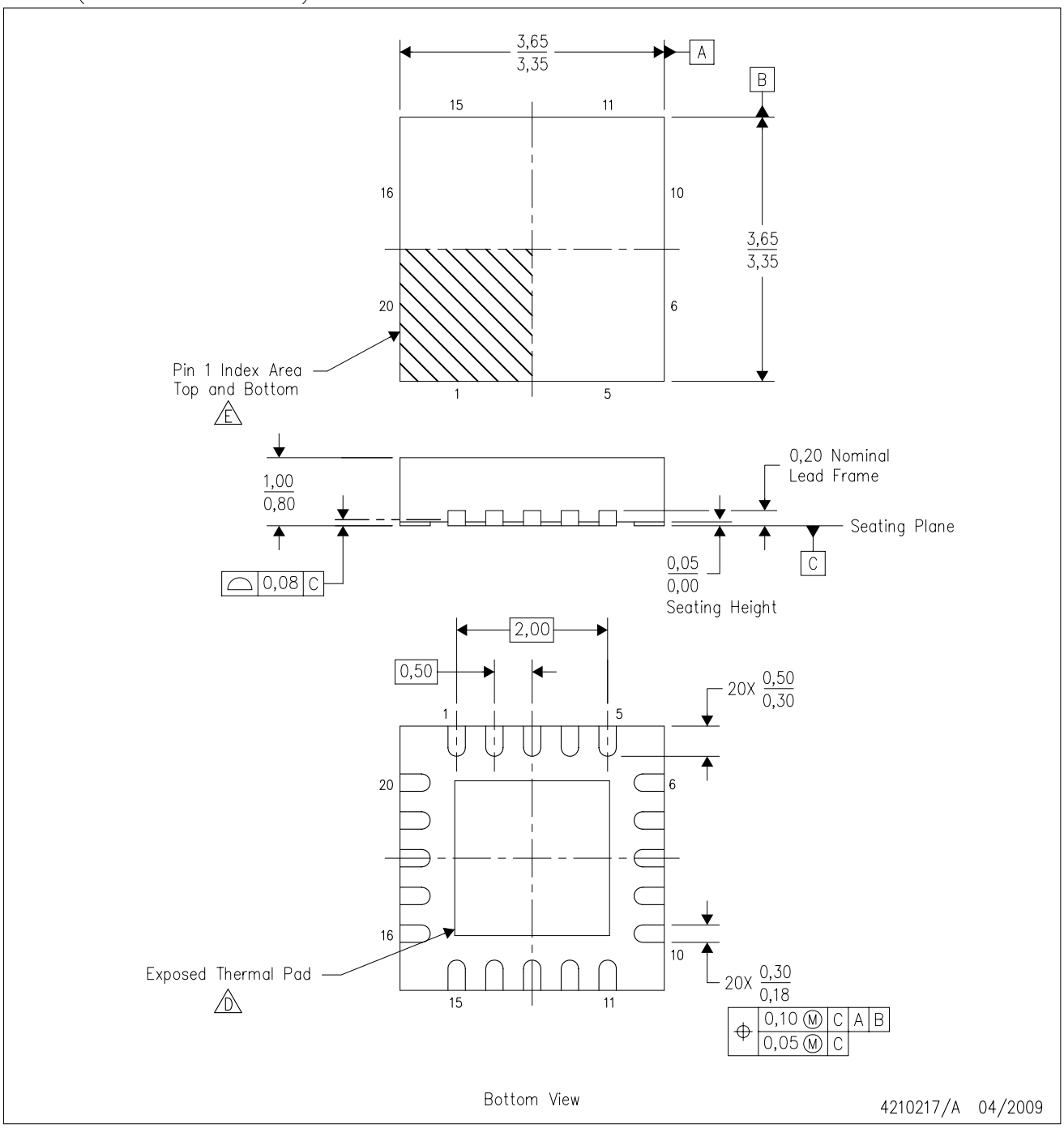
Bottom View

Exposed Thermal Pad Dimensions

4210218/D 02/13

NOTE: All linear dimensions are in millimeters

RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.