TEXAS INSTRUMENTS

bq21040

SLUSCE2A – APRIL 2016 – REVISED MAY 2016

bq21040 0.8-A, Single-Input, Single Cell Li-Ion and Li-Pol Battery Charger

1 Features

- Charging
  - 1% Charge Voltage Accuracy
  - 10% Charge Current Accuracy
  - Low Battery Leakage Current (1 μA)
  - Programmable Charge Current using External Resistor up to 800 mA
  - 4.2-V Li-Ion and Li-Pol Charger
- Protection
  - 30-V Input Rating; with 6.6-V Input Overvoltage Protection
  - Input Voltage Dynamic Power Management
  - 125°C Thermal Regulation; 150°C Thermal Shutdown Protection
  - OUT Short-Circuit Protection and ISET Short Detection
  - Overtemperature Sensing Protection Through NTC
  - Fixed 10-Hour Safety Timer
- System
  - Status Indication – Charging/Done
  - Available in Small SOT-23 Package

2 Applications

- EPOS
- Medical Endoscopes
- BLE Speaker and Headsets
- Low-Power Handheld Devices

3 Description

The bq21040 device is a highly integrated Li-Ion and Li-Pol linear battery charger device targeted at space-limited portable applications. The device operates from either a USB port or AC adapter. The high input voltage range with input overvoltage protection supports low-cost unregulated adapters.

The bq21040 has a single power output that charges the battery. A system load can be placed in parallel with the battery as long as the average system load does not keep the battery from charging fully during the 10 hour safety timer.

The battery is charged in three phases: conditioning, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.
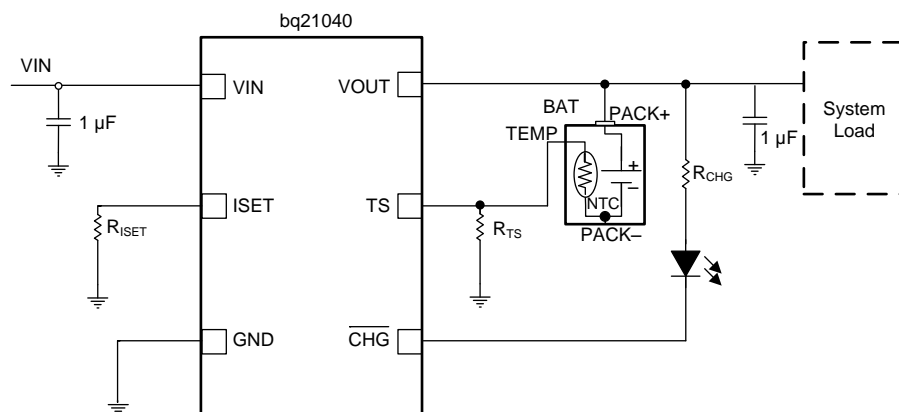
The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, charge status display, and charge termination. The pre-charge current and termination current threshold are fixed to 20% and 10%, respectively. The fast charge current value is programmable through an external resistor.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq21040	SOT-23 (6)	3.00 mm x 1.75 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

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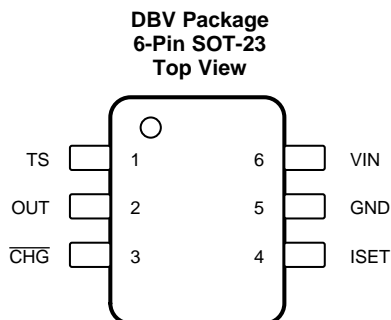
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2016) to Revision A   **Page**

5   Device Comparison

PART NO.	$V_{O(REG)}$	V_{OVP}	TS	PACKAGE
bq21040	4.20 V	6.6 V	TS	3.00 mm × 1.75 mm × 1.45 mm SOT-23

6   Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View

Pin Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
$\overline{CHG}$	3	O	Low (FET on) indicates charging and Open Drain (FET off) indicates no Charging or Charge complete.
GND	5	—	Ground terminal
ISET	4	I	Programs the Fast-charge current setting. External resistor from ISET to VSS defines fast charge current value. Range is 10.8kΩ (50mA) to 675Ω (800mA).
OUT	2	O	Battery connection. System load may be connected. Expected range of bypass capacitors 1μF to 10μF.
TS	1	I	Temperature sense terminal connected to bq21040 -10k at 25°C NTC thermistor, in the battery pack. Floating T terminal or pulling High puts part in TTDM "Charger" Mode and disable TS monitoring, Timers and Termination. Pulling terminal Low disables the IC. If NTC sensing is not needed, connect this terminal to VSS through an external 10 kΩ resistor. A 250kΩ from TS to ground will prevent IC entering TTDM mode when battery with thermistor is removed.
VIN	6	I	Input power, connected to external DC supply (AC adapter or USB port). Expected range of bypass capacitors 1μF to 10μF, connect from IN to V_{SS}.

7   Specifications

7.1   Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

		MIN	MAX	UNIT
Input voltage	IN (with respect to VSS)	−0.3	30	V
	OUT (with respect to VSS)	−0.3	7	V
	PRE-TERM, ISET, ISET2, TS, /CHG (with respect to VSS)	−0.3	7	V
Input current	IN		1.25	A
Output current (continuous)	OUT		1.25	A
Output sink current	$\overline{CHG}$		15	mA
Junction temperature, T_J		−40	150	°C
Storage temperature, T_{stg}		−65	150	°C

(1)   Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2)   All voltage values are with respect to the network ground terminal unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[1]	±250	

(1) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	IN voltage range	3.5		28	V
	IN operating voltage range, restricted by VDPM and VOVP	4.45		6.45	V
I_{IN}	Input current, IN terminal			0.8	A
I_{OUT}	Current, OUT terminal			0.8	A
T_J	Junction temperature	0		125	°C
R_{ISET}	Fast-charge current programming resistor	0.675		10.8	kΩ
R_{TS}	10k NTC thermistor range without entering TTDM	1.66		25.8	kΩ

7.4 Thermal Information

	THERMAL METRIC[1]	bq21040 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	31.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	45.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
UVLO	Undervoltage lockout exit	V_{IN}: 0 V to 4 V	3.15	3.3	3.45	V
$V_{HYS-UVLO}$	Hysteresis on V_{UVLO_RISE} falling	V_{IN}: 0 V to 4 V, V_{UVLO_FALL} = V_{UVLO_RISE} – $V_{HYS-UVLO}$	175	227	280	mV
V_{IN-DT}	Input power good detection threshold is $V_{OUT}+VIN-DT$	(Input power good if $V_{IN} > V_{OUT} + V_{IN-DT}$); V_{OUT} = 3.6 V, V_{IN}: 3.5 V to 4 V	30	80	145	mV
$V_{HYS-INDT}$	Hysteresis on V_{IN-DT} falling	V_{OUT} = 3.6 V, VIN: 4 V to 3.5 V		31		mV
V_{OVP}	Input overvoltage protection threshold	V_{IN}: 5 V to 12 V	6.5	6.65	6.8	V
$V_{HYS-OVP}$	Hysteresis on OVP	V_{IN}: 11 V to 5 V		95		mV
V_{IN-DPM}	Adaptor low input voltage protection. Restricts Iout at VIN-DPM	Feature active in adaptor mode; Limit Input Current to 50 mA; V_{OUT} = 3.5 V; R_{ISET} = 825	4.24	4.3	4.46	V
ISET SHORT CIRCUIT TEST						
R_{ISET_SHORT}	Highest resistance considered a fault (short). Monitored for I_{OUT}>90mA	R_{ISET}: 250 Ω to 540 Ω, Iout latches off. Cycle power to reset			500	Ω
I_{OUT_CL}	Maximum OUT current limit regulation (clamp)	V_{IN} = 5 V, V_{OUT} = 3.6 V, R_{ISET}: 250 Ω to 540 Ω, Iout latches off after $t_{DGL-SHORT}$	1.05		1.4	A

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY SHORT PROTECTION						
$V_{OUT(SC)}$	OUT terminal short-circuit detection threshold/precharge threshold	Vout:3V to 0.5V, no deglitch	0.75	0.8	0.85	V
$V_{OUT(SC-HYS)}$	OUT terminal short hysteresis	Recovery ≥ $V_{OUT(SC)}$ + $V_{OUT(SC-HYS)}$; Rising, no deglitch		77		mV
$I_{OUT(SC)}$	Source current to OUT terminal during short-circuit detection		10	15	20	mA
QUIESCENT CURRENT						
$I_{OUT(PDWN)}$	Battery current into OUT terminal	V_{IN} = 0V			1	µA
$I_{OUT(DONE)}$	OUT pin current, charging terminated	V_{IN} = 6 V, V_{BAT} > $V_{BAT(REG)}$, net current is into OUT pin			6	µA
$I_{IN(STDBY)}$	Standby current into IN pin	TS = Low, V_{IN} ≤ 6 V			125	µA
I_{CC}	Active supply current, IN pin	TS = Low, V_{IN} = 6 V, no load on OUT pin, V_{BAT} > $V_{BAT(REG)}$			1000	µA
BATTERY CHARGER FAST-CHARGE						
$V_{OUT(REG)}$	Battery regulation voltage	V_{REG} = 4.2 V, I_L = 25 mA, V_{IN} = 5.5 V	4.16	4.2	4.23	V
$I_{OUT(RANGE)}$	Programmed output fast charge current range	$V_{OUT(REG)}$ > V_{OUT} > V_{LOWV}; V_{IN} = 5 V, R_{ISET} = 0.675 to 52 kΩ	10		800	mA
$V_{DO(IN-OUT)}$	Drop-Out, V_{IN} – V_{OUT}	Adjust V_{IN} down until I_{OUT} = 0.5 A, V_{OUT} = 4.15 V, R_{ISET} = 1.08kΩ		325	550	mV
I_{OUT}	Output fast charge formula	$V_{OUT(REG)}$ > V_{OUT} > V_{LOWV}; V_{IN} = 5 V	KISET/ RISET	KISET/ RISET	KISET/ RISET	A
K_{ISET}	Fast charge current factor	R_{ISET} = K_{ISET} / I_{OUT}; 50 < I_{OUT} < 800 mA	510	540	570	AΩ
		R_{ISET} = K_{ISET} / I_{OUT}; 25< I_{OUT} < 50 mA	480	527	600	
		R_{ISET} = K_{ISET} / I_{OUT}; 10 < I_{OUT} < 25 mA	350	520	680	
PRECHARGE						
V_{LOWV}	Pre-charge to fast-charge transition threshold		2.4	2.5	2.6	V
Pre-charge	Default pre-charge current	V_{BAT} < V_{LOWV}, I_{CHG} = 50 mA	18	20	22	%ISET
TERMINATION						
%TERM	Termination Threshold Current, default setting	V_{OUT} > V_{RCH}; R_{ISET} = 1 kΩ	9	10	11	%IOUT-CC
RECHARGE OR REFRESH						
V_{RCH}	Recharge detection threshold	V_{IN} = 5 V, V_{TS} = 0.5 V, V_{OUT} = 4.25 V to V_{RCH}	$V_{O(REG)}$ - 120 mV	$V_{O(REG)}$ - 95 mV	$V_{O(REG)}$ - 70 mV	mV
BATT DETECT						
V_{REG-BD}	VOUT Reduced regulation during battery detect	V_{IN} = 5 V, V_{TS} = 0.5 V, battery absent	$V_{O(REG)}$ - 450 mV	$V_{O(REG)}$ - 400 mV	$V_{O(REG)}$ - 350 mV	mV
$I_{BD-SINK}$	Sink current during VREG-BD		7		10	mA
V_{BD-HI}	High battery detection threshold	V_{IN} = 5 V, V_{TS} = 0.5 V, battery absent	$V_{O(REG)}$ - 150 mV	$V_{O(REG)}$ - 100 mV	$V_{O(REG)}$ - 50 mV	V
V_{BD-LO}	Low battery detection threshold		VREG-BD+0.50	VREG-BD+0.1	VREG-BD+0.15	V
BATTERY-PACK NTC MONITOR						
$I_{NTC\,50µA}$	NTC bias current		48	50	53	µA
$I_{NTC-DIS-10K}$	10K NTC bias current when charging is disabled	V_{TS} = 0 V	27	30	34	µA
$I_{NTC-FLDBK\,-10K}$	INTC is reduced prior to entering TTDM to keep cold thermistor from entering TTDM	V_{TS} = 1.525 V	4	5	6.5	µA

Product Folder Links: *bq21040*

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

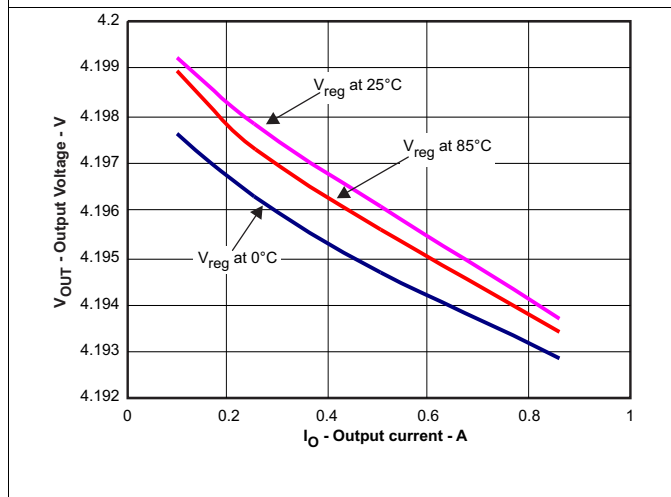| PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TTDM(TS)}$	Termination and timer disable mode-Threshold-Enter	V_{TS}: 0.5 V to 1.7 V; timer held in reset	1550	1600	1650	mV
$I_{HYS-TTDM(TS)}$	Hysteresis exiting TTDM	V_{TS}: 1.7 V to 0.5 V; timer enabled		100		mV
$V_{CLAMP(TS)}$	TS maximum voltage clamp	V_{TS} = Open (float)	1800	1950	2000	mV
$V_{TS\_I-FLDBK}$	TS voltage where INTC is reduce to keep thermistor from entering TTDM	INTC adjustment (90 to 10%; 45 to 6.6 µs) takes place near this spec threshold. V_{TS}: 1.425 V to 1.525 V		1475		mV
C_{TS}	Optional capacitance – ESD			0.22		µF
V_{TS-0C}	Low temperature CHG pending	Low temperature charging to pending; V_{TS}: 1 V to 1.5 V	1220	1250	1280	mV
V_{HYS-0C}	Hysteresis at 0°C	Charge pending to low temperature charging; V_{TS}: 1.5 V to 1 V		100		mV
V_{TS-45C}	High temperature CHG disable	High temperature charging to pending; V_{TS}: 0.5 V to 0.2 V	260	275	290	mV
$V_{HYS-45C}$	Hysteresis at 45°C	Charge pending to high temperature charging; V_{TS}: 0.2 V to 0.5 V		20		mV
$V_{TS-EN-10K}$	Charge enable threshold (10k NTC)	V_{TS}: 0 V to 0.175 V	80	88	96	mV
$V_{TS-DIS\_HYS-10K}$	HYS below VTS-EN-10k to disable (10k NTC)	V_{TS}: 0.125 V to 0 V		12		mV
THERMAL REGULATION						
$T_{J(REG)}$	Temperature regulation limit			125		
$T_{J(OFF)}$	Thermal shutdown temperature			155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		
CHG INDICATION						
V_{OL}	Output Low Voltage-CHG FET on - first charge after power-up	I_{SINK} = 5 mA			0.4	V
I_{LEAK}	Leakage current into IC	$V_{\overline{CHG}}$ = 5 V			1	µA

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
INPUT						
$t_{DGL(OVP\_SET)}$	Input over-voltage blanking time	V_{IN}: 5 V to 12 V		113		µs
$t_{DGL(OVP\_REC)}$	Deglitch time exiting OVP	Time measured from VIN: 12V to 5V		30		µs
ISET SHORT CIRCUIT TEST						
t_{DGL_SHORT}	Deglitch time transition from ISET short to IOUT disable	Clear fault by disconnecting IN or cycling (high / low) TS		1		ms
PRECHARGE – SET INTERNALLY						
$t_{DGL1(LOWV)}$	Deglitch time on pre-charge to fast-charge transition			70		µs
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to pre-charge transition			32		ms
TERMINATION						
$t_{DGL(TERM)}$	Deglitch time, termination detected			29		ms
RECHARGE OR REFRESH						
$t_{DGL1(RCHG)}$	Deglitch time, recharge threshold detected	V_{IN} = 5 V, V_{TS} = 0.5 V, VOUT: 4.25 V to 3.5 V in 1 µs; $t_{DGL(RCHG)}$ is time to ISET ramp		29		ms
BATTERY DETECT ROUTINE						
$t_{DGL(HI/LOW REG)}$	Regulation time at VREG or VREG-BD			25		ms
BATTERY-PACK NTC MONITOR; TS TERMINAL						
$t_{DGL(TS)}$	Deglitch for TS thresholds: 0/45C.	Battery charging		30		ms

7.7 Typical Operational Characteristics (Protection Circuits Waveforms)

SETUP: bq21040 typical applications schematic; V_{IN} = 5V, V_{BAT} = 3.6V (unless otherwise indicated)

Figure 1. Kiset for Low and High Currents

Figure 2. Line Regulation

Figure 3. Load Regulation Over Temperature

Figure 4. Load Regulation

Figure 5. Line Regulation

Figure 6. Current Regulation Over Temperature

Product Folder Links: *bq21040*
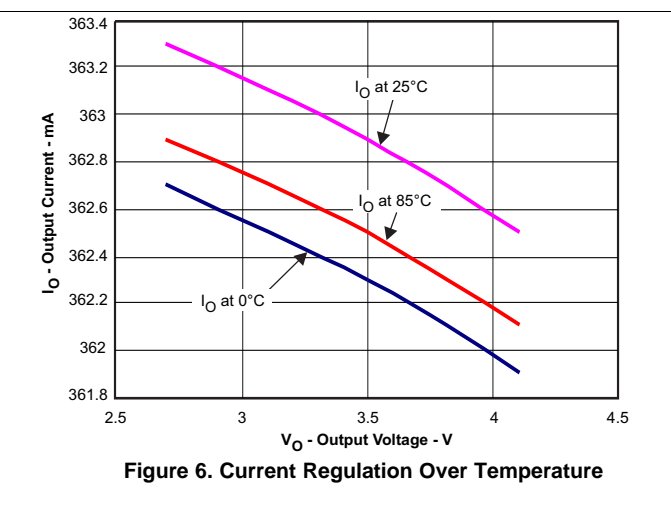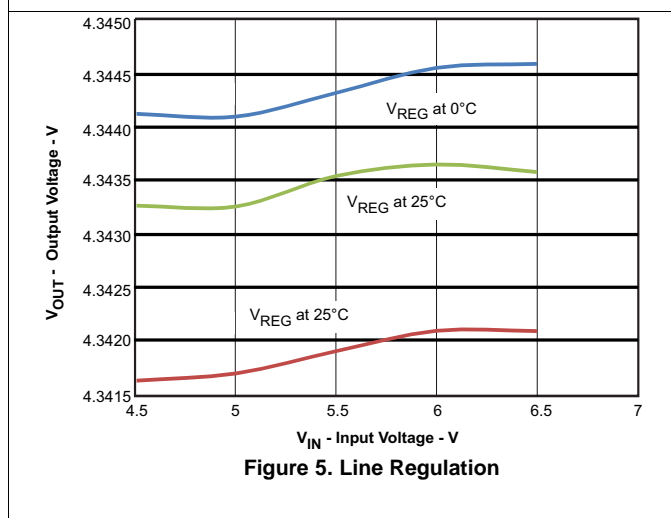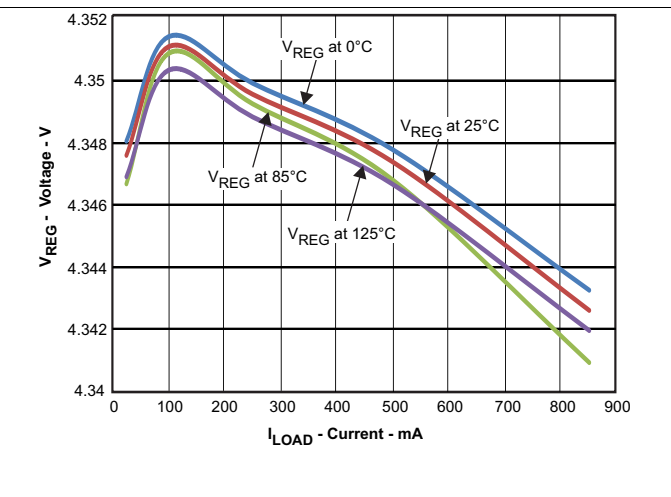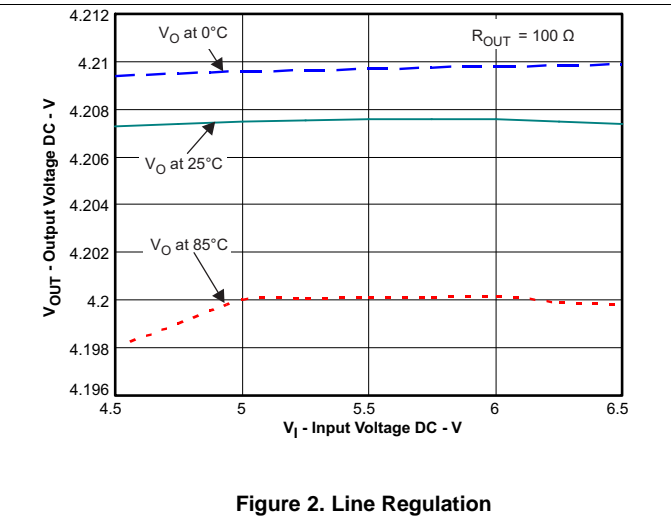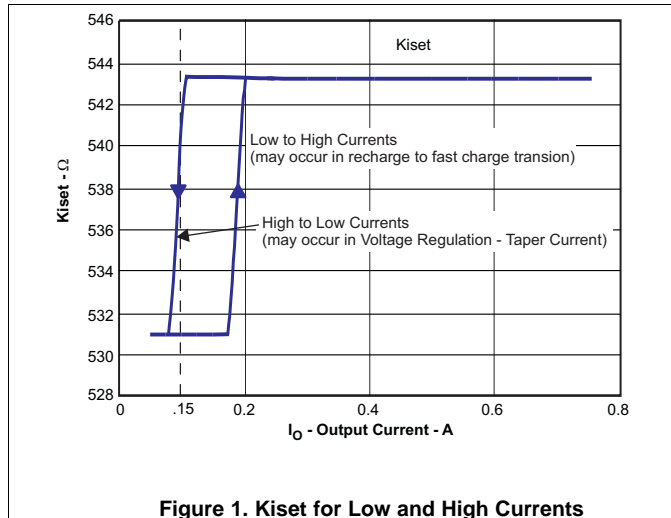
8 Detailed Description

8.1 Overview

The bq21040 is a highly integrated single cell Li-Ion and Li-Pol charger. The charger can be used to charge a battery, power a system or both. The charger has three phases of charging: Pre-charge to recover a fully discharged battery, fast-charge constant current to supply the buck charge safely and voltage regulation to safely reach full capacity. The charger is very flexible, allowing programming of the fast-charge current. This charger is designed to work with a USB connection or Adaptor (DC out). The charger also checks to see if a battery is present.

The charger also comes with a full set of safety features: Temperature Sensing Standard, Over-Voltage Protection, DPM-IN, Safety Timers, and ISET short protection. All of these features and more are described in detail below.

The charger is designed for a single power path from the input to the output to charge a single cell Li-Ion or Li-Pol battery pack. Upon application of a 5VDC power source the ISET and OUT short checks are performed to assure a proper charge cycle.

If the battery voltage is below the LOWV threshold, the battery is considered discharged and a preconditioning cycle begins. The amount of the current goes into the battery during this phase is called pre-charge current. It is fixed to 20% of the fast charge current.

Once the battery voltage has charged to the VLOWV threshold, fast charge is initiated and the fast charge current is applied. The fast charge constant current is programmed using the ISET terminal. The constant current provides the bulk of the charge. Power dissipation in the IC is greatest in fast charge with a lower battery voltage. If the IC reaches 125°C the IC enters thermal regulation, slows the timer clock by half and reduce the charge current as needed to keep the temperature from rising any further. Figure 7 shows the charging profile with thermal regulation. Typically under normal operating conditions, the IC's junction temperature is less than 125°C and thermal regulation is not entered.

Once the cell has charged to the regulation voltage the voltage loop takes control and holds the battery at the regulation voltage until the current tapers to the termination threshold. The termination current is set to 10% of the fast charge current. The CHG terminal is low (LED on) during the first charge cycle only and turns off once the termination threshold is reached, regardless if termination, for charge current, is enabled or disabled.
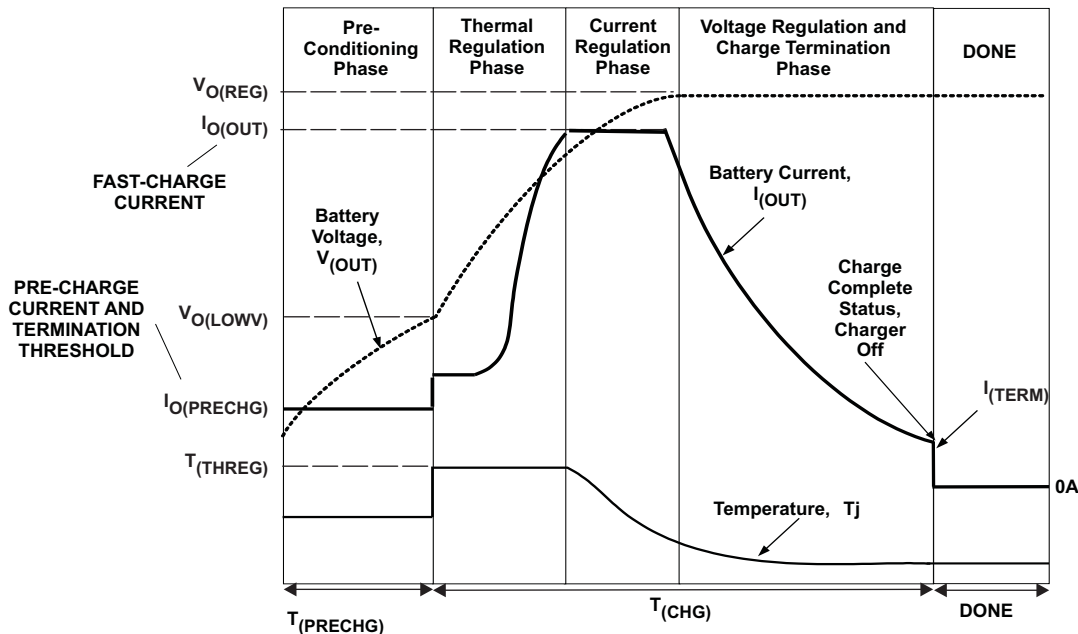
8.2 Functional Block Diagram
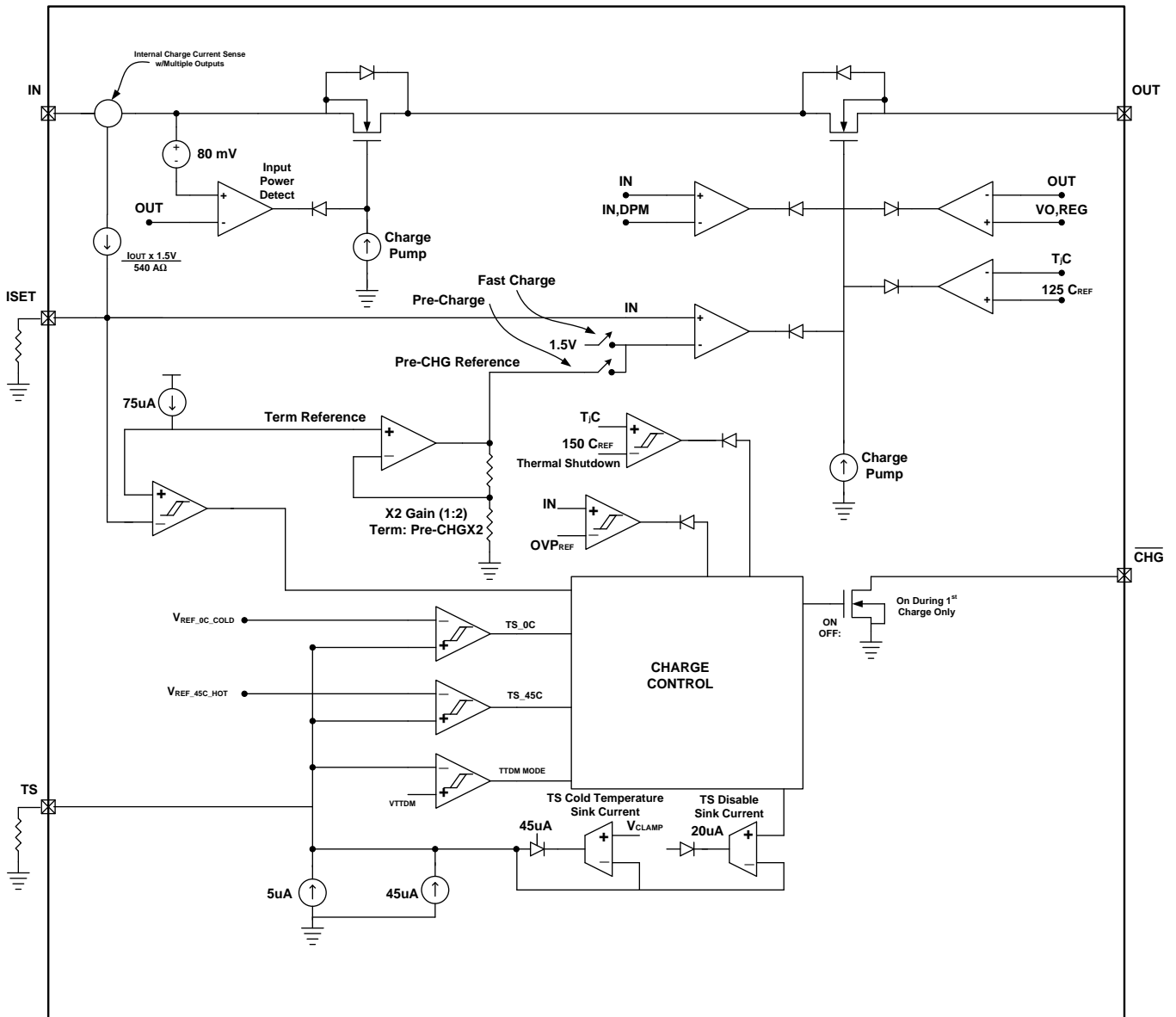
8.3 Feature Description

Figure 7. Charging Profile With Thermal Regulation

8.3.1 Power-Down or Undervoltage Lockout (UVLO)

The bq21040 is in power-down mode if the IN terminal voltage is less than UVLO. The part is considered "dead" and all the terminals are high impedance. Once the IN voltage rises above the UVLO threshold the IC will enter Sleep Mode or Active mode depending on the OUT terminal (battery) voltage.
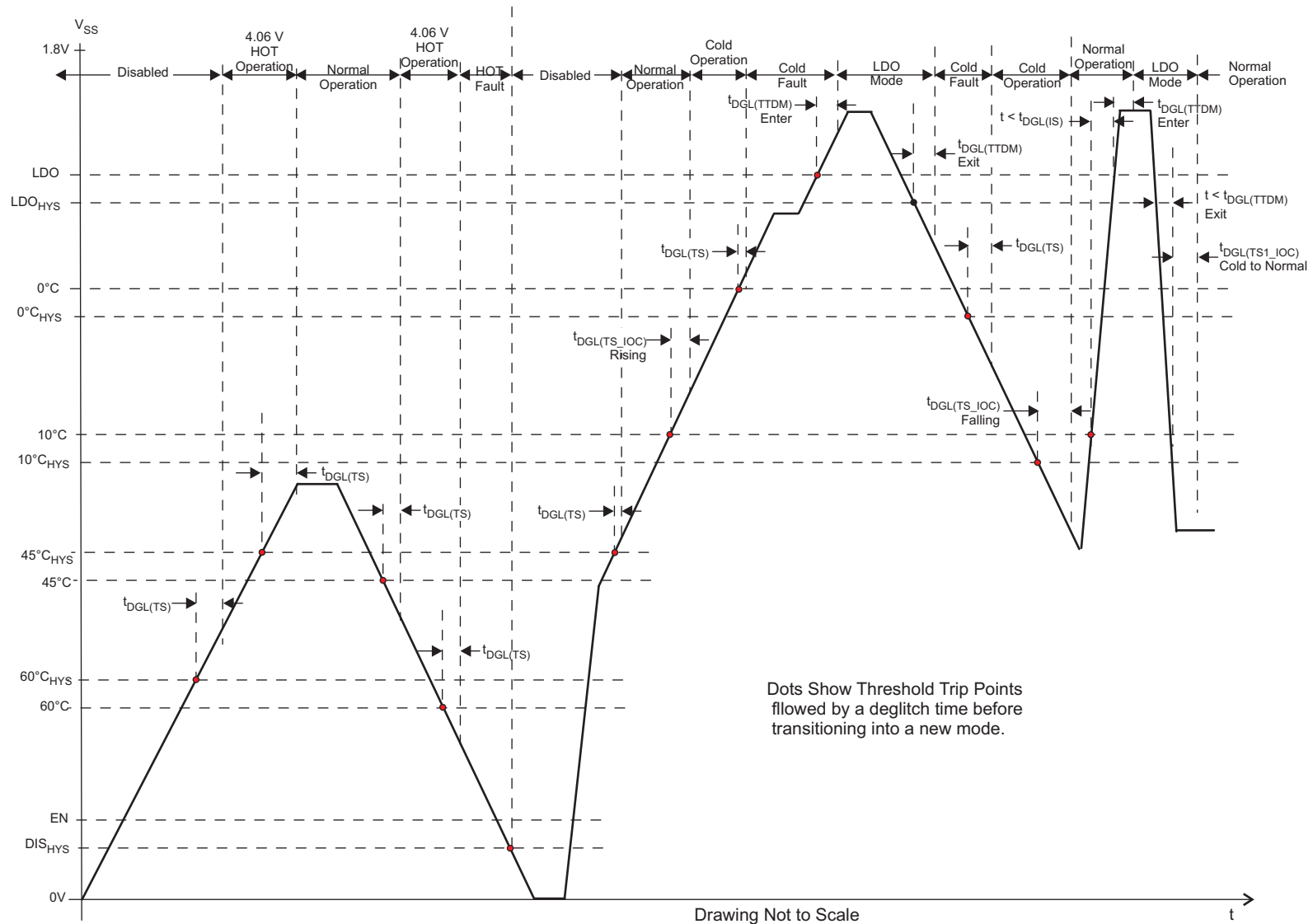
8.3.2 Power-up

The IC is alive after the IN voltage ramps above UVLO (see sleep mode), resets all logic and timers, and starts to perform many of the continuous monitoring routines. Typically the input voltage quickly rises through the UVLO and sleep states where the IC declares power good, starts the qualification charge at 100mA starts the safety timer and enables the $\overline{\text{CHG}}$ terminal. See Figure 8.

8.3.3 Sleep Mode

If the IN terminal voltage is between than $V_{OUT}+V_{DT}$ and UVLO, the charge current is disabled, the safety timer counting stops (not reset) and the $\overline{\text{CHG}}$ terminal is high impedance. As the input voltage rises and the charger exits sleep mode, the safety timer continues to count, charge is enabled and the $\overline{\text{CHG}}$ terminal returns to its previous state. See Figure 9.

8.3.4 New Charge Cycle

A new charge cycle is started when a good power source is applied, performing a chip disable/enable (TS terminal), exiting Termination and Timer Disable Mode (TTDM), detecting a battery insertion or the OUT voltage dropping below the VRCH threshold. The $\overline{\text{CHG}}$ terminal is active low only during the first charge cycle, therefore exiting TTDM or a dropping below VRCH will not turn on the $\overline{\text{CHG}}$ terminal FET, if the $\overline{\text{CHG}}$ terminal is already high impedance.

Product Folder Links: *bq21040*

Figure 8. TS Battery Temperature Bias Threshold and Deglitch Timers

A.   JEITA timing does not apply to bq21040
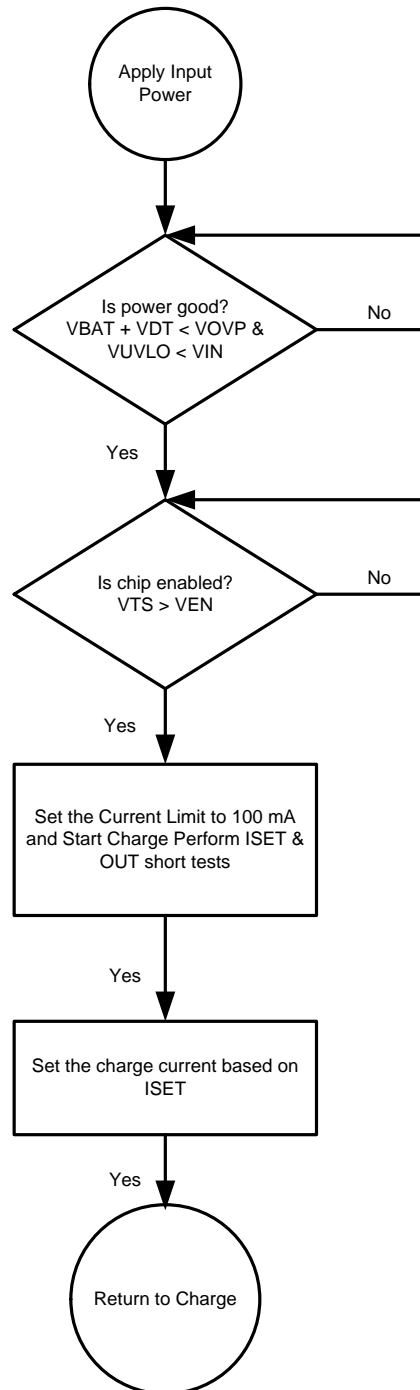
Figure 9. bq21040 Power-Up Flow Diagram

8.3.5 Overvoltage-Protection (OVP) – Continuously Monitored

If the input source applies an overvoltage, the pass FET, if previously on, turns off after a deglitch, $t_{BLK(OVP)}$. The timer ends and the $\overline{CHG}$ terminal goes to a high impedance state. After the overvoltage returns to a normal voltage, the timer continues, charge continues, and the $\overline{CHG}$ terminal goes low after a 25ms deglitch.

8.3.6 $\overline{\text{CHG}}$ Terminal Indication

The charge terminal has an internal open drain FET which is on (pulls down to V_{SS}) during the first charge only (independent of TTDM) and is turned off once the battery reaches voltage regulation and the charge current tapers to the termination threshold set by the PRE-TERM resistor. The bq21040 does not terminate charge, however, the $\overline{\text{CHG}}$ terminal will turn off once the battery current reaches 10% of the programmed charge current.

The charge terminal is high impedance in sleep mode and OVP and returns to its previous state once the condition is removed.

Cycling input power, pulling the TS terminal low and releasing or entering pre-charge mode causes the $\overline{\text{CHG}}$ terminal to go reset (go low if power is good and a discharged battery is attached) and is considered the start of a first charge.

8.4 Device Functional Modes

8.4.1 $\overline{\text{CHG}}$ LED Pull-up Source

For host monitoring, a pullup resistor is used between the STATUS terminal and the V_{CC} of the host and for a visual indication a resistor in series with an LED is connected between the STATUS terminal and a power source. If the $\overline{\text{CHG}}$ source is capable of exceeding 7 V, a 6.2-V Zener should be used to clamp the voltage. If the source is the OUT terminal, note that as the battery changes voltage, and the brightness of the LEDs vary.

Table 1. Charging States and $\overline{\text{CHG}}$ LED

CHARGING STATE	$\overline{\text{CHG}}$ FET/LED
First charge after VIN applied	ON
Refresh charge	OFF
OVP	
SLEEP	
TEMP FAULT	ON for 1st Charge

8.4.2 IN-DPM (V_{IN}-DPM or IN-DPM)

The IN-DPM feature is used to detect an input source voltage that is folding back (voltage dropping), reaching its current limit due to excessive load. When the input voltage drops to the V_{IN-DPM} threshold the internal pass FET starts to reduce the current until there is no further drop in voltage at the input. This would prevent a source with voltage less than V_{IN-DPM} to power the out terminal. This works well with current limited adaptors and USB ports as long as the nominal voltage is above 4.3 V. This is an added safety feature that helps protect the source from excessive loads.

8.4.3 OUT

The Charger's OUT terminal provides current to the battery and to the system, if present. This IC can be used to charge the battery plus power the system, charge just the battery or just power the system (TTDM) assuming the loads do not exceed the available current. The OUT terminal is a current limited source and is inherently protected against shorts. If the system load ever exceeds the output programmed current threshold, the output will be discharged unless there is sufficient capacitance or a charged battery present to supplement the excessive load.

8.4.4 ISET

An external resistor is used to Program the Output Current (50 to 800 mA) and can be used as a current monitor.

$$R_{ISET} = K_{ISET} / I_{OUT}$$

where

- I_{OUT} is the desired fast charge current;
- K_{ISET} is a gain factor found in the electrical specification (1)

For greater accuracy at lower currents, part of the sense FET is disabled to give better resolution. Figure 1 shows the transition from low current to higher current. Going from higher currents to low currents, there is hysteresis and the transition occurs around 0.15 A.

The ISET resistor is short protected and will detect a resistance lower than ≠340 Ω. The detection requires at least 80mA of output current. If a "short" is detected, then the IC will latch off and can only be reset by cycling the power. The OUT current is internally clamped to a maximum current between 1.05 A and 1.4 A and is independent of the ISET short detection circuitry, as shown in Figure 10. Also, see Figure 25 and Figure 26.
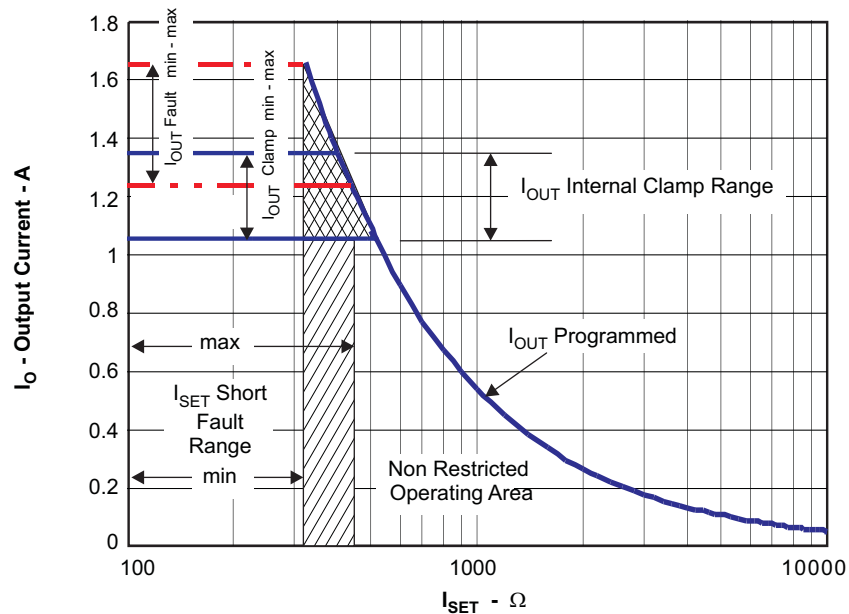
Figure 10. Programmed/Clamped Out Current

8.4.5 TS

The TS function is designed to follow the temperature sensing standard for Li-Ion and Li-Pol batteries. There are two thresholds, 45°C and 0°C. Normal operation occurs between 0°C and 45°C.

The TS feature is implemented using an internal 50µA current source to bias the thermistor (designed for use with a 10k NTC β = 3370 (SEMITEC 103AT-2 or Mitsubishi TH05-3H103F) connected from the TS terminal to V_{SS}. If this feature is not needed, a fixed 10kΩ can be placed between TS and V_{SS} to allow normal operation. This may be done if the host is monitoring the thermistor and then the host would determine when to pull the TS terminal low to disable charge.

The TS terminal has two additional features, when the TS terminal is pulled low or floated/driven high. A low disables charge (similar to a high on the $\overline{BAT\_EN}$ feature) and a high puts the charger in TTDM.

Above 45°C or below 0°C the charge is disabled. Once the thermistor reaches ≠–10°C the TS current folds back to keep a cold thermistor (between –10°C and –50°C) from placing the IC in the TTDM mode. If the TS terminal is pulled low into disable mode, the current is reduce to ≠30µA, see Figure 8. Since the I_{TS} curent is fixed along with the temperature thresholds, it is not possible to use thermistor values other than the 10k NTC (at 25°C).

8.4.6 Termination and Timer Disable Mode (TTDM) - TS Terminal High

The battery charger is in TTDM when the TS terminal goes high from removing the thermistor (removing battery pack/floating the TS terminal) or by pulling the TS terminal up to the TTDM threshold.

When entering TTDM, the 10 hour safety timer is held in reset and termination is disabled. A battery detect routine is run to see if the battery was removed or not. If the battery was removed then the $\overline{CHG}$ terminal will go to its high impedance state if not already there. If a battery is detected the $\overline{CHG}$ terminal does not change states until the current tapers to the termination threshold, where the $\overline{CHG}$ terminal goes to its high impedance state if not already there (the regulated output will remain on).

The charging profile does not change (still has pre-charge, fast-charge constant current and constant voltage modes). This implies the battery is still charged safely and the current is allowed to taper to zero.

When coming out of TTDM, the battery detect routine is run and if a battery is detected, then a new charge cycle begins and the $\overline{\text{CHG}}$ LED turns on.

If TTDM is not desired upon removing the battery with the thermistor, one can add a 237k resistor between TS and V_{SS} to disable TTDM. This keeps the current source from driving the TS terminal into TTDM. This creates ≠0.1°C error at hot and a ≠3°C error at cold.

8.4.7 Timers

The pre-charge timer is set to 30 minutes. The pre-charge current, can be programmed to off-set any system load, making sure that the 30 minutes is adequate. The bq21040 does not have a safety timer.

The fast charge timer is fixed at 10 hours and can be increased real time by going into thermal regulation, IN-DPM or if in USB current limit. The timer clock slows by a factor of 2, resulting in a clock than counts half as fast when in these modes. If either the 30 minute or ten hour timer times out, the charging is terminated and the $\overline{\text{CHG}}$ terminal goes high impedance if not already in that state. The fast charge timer is reset by disabling the IC, cycling power or going into and out of TTDM.

8.4.8 Termination

Once the OUT terminal goes above VRCH, (reaches voltage regulation) and the current tapers down to the termination threshold (10% of the fast charge current), the $\overline{\text{CHG}}$ terminal goes high impedance and a battery detect route is run to determine if the battery was removed or the battery is full. If the battery is present, the charge current will terminate. If the battery was removed along with the thermistor, then the TS terminal is driven high and the charge enters TTDM. If the battery was removed and the TS terminal is held in the active region, then the battery detect routine will continue until a battery is inserted.

8.4.9 Battery Detect Routine

The battery detect routine should check for a missing battery while keeping the OUT terminal at a useable voltage. Whenever the battery is missing the $\overline{\text{CHG}}$ terminal should be high impedance.

The battery detect routine is run when entering and exiting TTDM to verify if battery is present, or run all the time if battery is missing and not in TTDM. On power-up, if battery voltage is greater than V_{RCH} threshold, a battery detect routine is run to determine if a battery is present.

The battery detect routine is disabled while the IC is in TTDM, or has a TS fault. See Figure 11 for the Battery Detect Flow Diagram.

8.4.10 Refresh Threshold

After termination, if the OUT terminal voltage drops to V_{RCH} (100mV below regulation) then a new charge is initiated, but the $\overline{\text{CHG}}$ terminal remains at a high impedance (off).

8.4.11 Starting a Charge on a Full Battery

The termination threshold is raised by ≠14%, for the first minute of a charge cycle so if a full battery is removed and reinserted or a new charge cycle is initiated, that the new charge terminates (less than 1 minute). Batteries that have relaxed many hours may take several minutes to taper to the termination threshold and terminate charge.
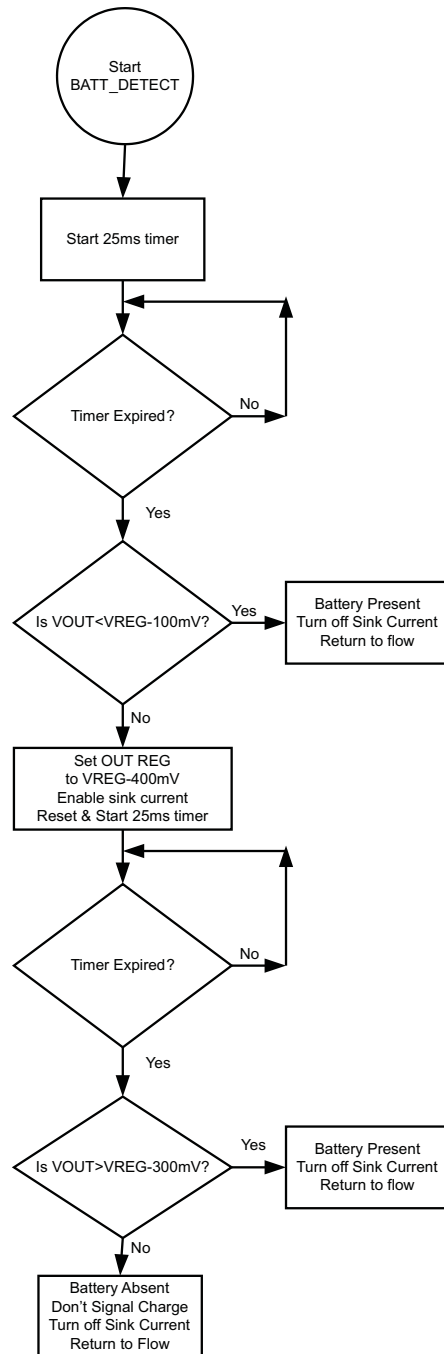
Figure 11. Battery Detect Routine (bq21040)

# 9 Application and Implementation

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NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq21040 device is a highly integrated Li-Ion and Li-Pol linear charger device targeted at space-limited portable applications. The device operates from either a USB port or AC adapter. The high input voltage range with input overvoltage protection supports low-cost unregulated adapters. This device has a single power output that charges the battery. A system load can be placed in parallel with the battery as long as the average system load does not keep the battery from charging fully during the 10 hour safety timer.

9.2 Typical Application

$I_{OUT\_FAST\_CHG}$ = 540mA; $I_{OUT\_PRE\_CHG}$ = 108mA; I_{OUT_TERM} = 54mA
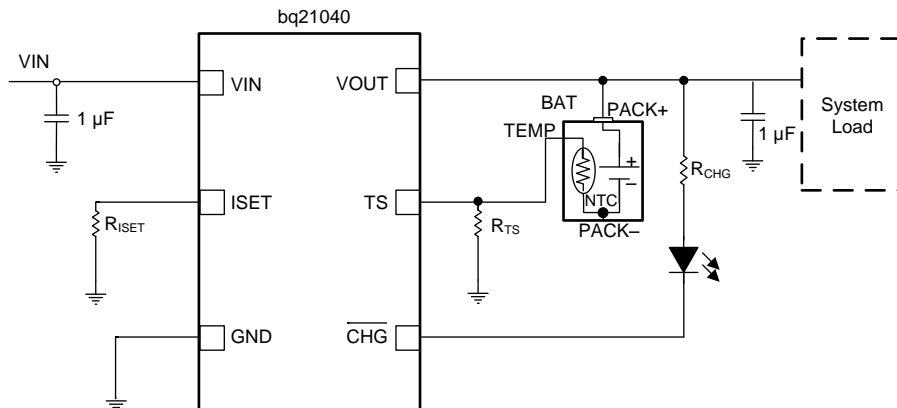
Copyright © 2016, Texas Instruments Incorporated

Figure 12. Typical Application Circuit

9.2.1 Design Requirements

- Supply voltage = 5 V
- Fast charge current: I_{OUT-FC} = 540 mA; ISET-terminal 2
- Termination Current Threshold: $\%_{IOUT-FC}$ = 10% of Fast Charge or about 54mA
- Pre-Charge Current by default is twice the termination Current or about 108mA
- TS – Battery Temperature Sense = 10k NTC (103AT)

Typical Application (continued)

9.2.2 Detailed Design Procedure

9.2.2.1 Calculations

9.2.2.1.1 Program the Fast Charge Current, ISET:

$$R_{ISET} = [K_{(ISET)} / I_{(OUT)}] \tag{2}$$

From the *Electrical Characteristics* table:

- $K_{(SET)}$ = 540AΩ
- R_{ISET} = [540AΩ/0.54A] = 1.0 kΩ

Selecting the closest standard value, use a 1.0 kΩ resistor between ISET (terminal 16) and Vss.

9.2.2.1.2 Pre-Charge and Termination Current Thresholds, ITERM, and PRE-CHG

$$TERM = I_{(OUT)} \times 10\% I_{OUT-FC} \tag{3}$$
$$TERM = 540mA \times 10\% = 54mA \tag{4}$$

One can calculate the pre-charge current by using 20% of the fast charge current (factor of 2 difference).

$$PRE\text{-}Charge = I_{(OUT)} \times 20\% I_{OUT-FC} \tag{5}$$
$$PRE\text{-}Charge = 540mA \times 20\% = 108mA \tag{6}$$

9.2.2.1.3 TS Function

Use a 10k NTC thermistor in the battery pack (103AT).

To Disable the temp sense function, use a fixed 10k resistor between the TS (terminal 1) and Vss.

9.2.2.1.4 $\overline{CHG}$

LED Status: connect a 1.5kΩ resistor in series with a LED between the OUT terminal and the $\overline{CHG}$ terminal.

Processor Monitoring: Connect a pull-up resistor between the processor's power rail and the $\overline{CHG}$ terminal.

9.2.2.2 Selecting In and Out Terminal Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor (ceramic) on the power terminal, input and output terminals. Using the values shown on the application diagram, is recommended. After evaluation of these voltage signals with real system operational conditions, one can determine if capacitance values can be adjusted toward the minimum recommended values (DC load application) or higher values for fast high amplitude pulsed load applications. Note if designed for high input voltage sources (bad adaptors or wrong adaptors), the capacitor needs to be rated appropriately. Ceramic capacitors are tested to 2x their rated values so a 16V capacitor may be adequate for a 30V transient (verify tested rating with capacitor manufacturer).

Typical Application (continued)

9.2.3 Application Curves

SETUP: bq21040 typical applications schematic; V_{IN} = 5V, V_{BAT} = 3.6V (unless otherwise indicated)
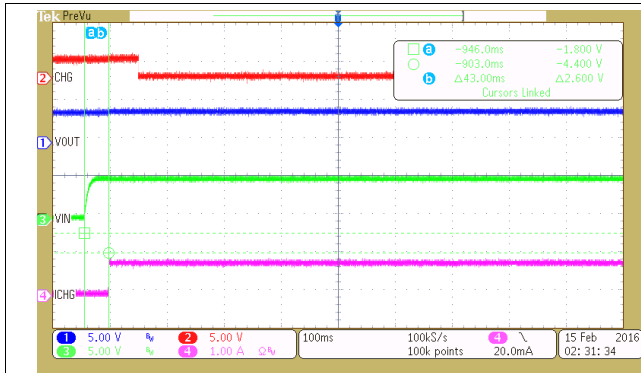
Figure 13. Power-Up Timing
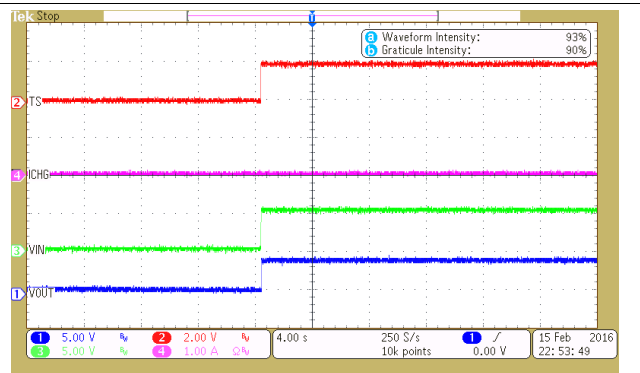
Figure 14. Power-Up Timing – No Battery or Load in TTDM
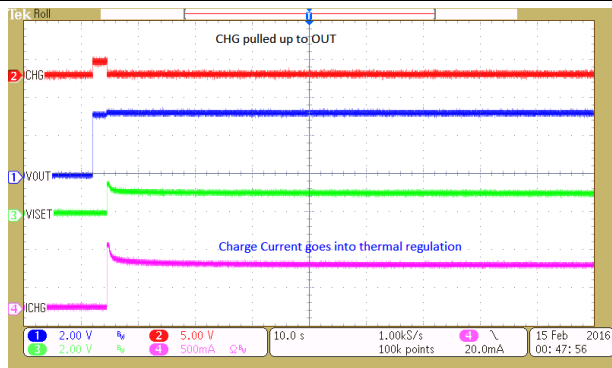
Figure 15. Start-Up in Thermal Regulation
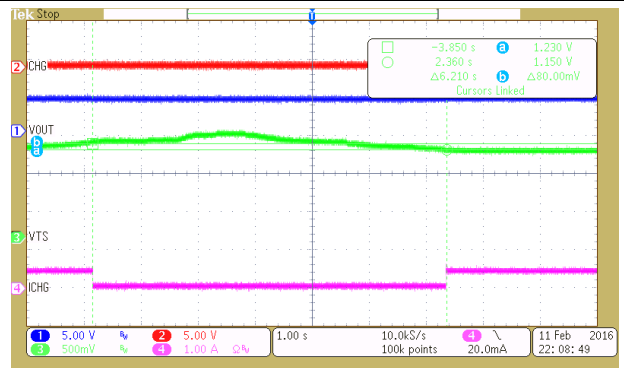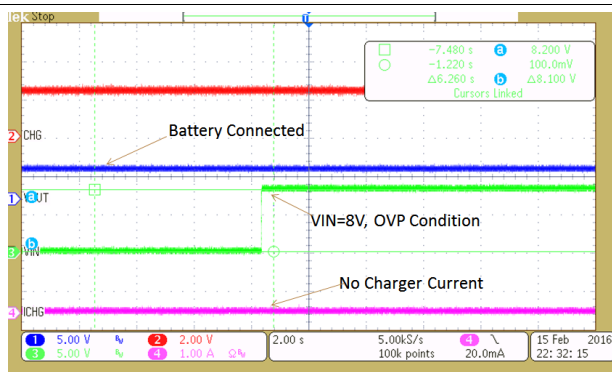

Figure 16. TS Entering and Leaving Cold Temperature
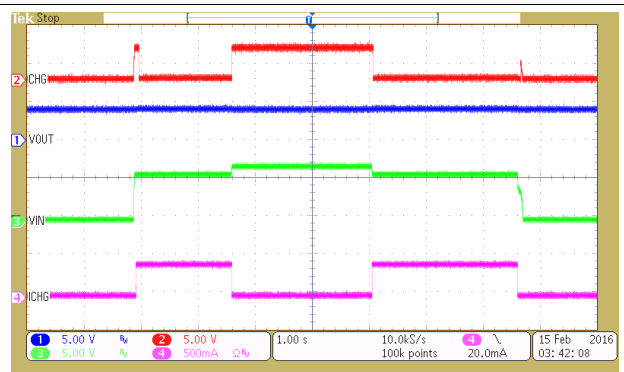

Figure 17. OVP 8-V Adaptor — Hot Plug

Figure 18. OVP From Normal Power-Up Operation – V_{IN} 0 V → 6 V → 7 V → 6 V→ 0 V

Typical Application (continued)
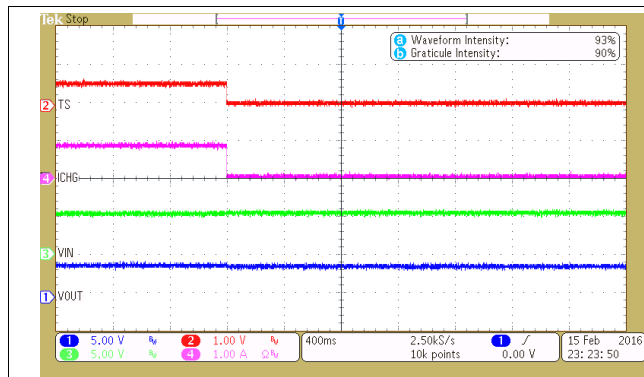
Figure 19. TS Enable and Disable
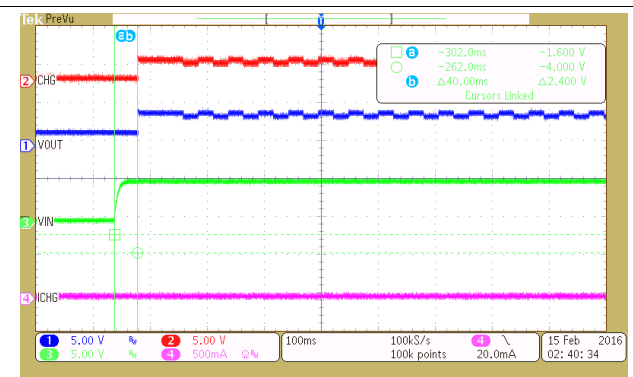
Fixed 10kΩ resistor, between TS and GND.

Figure 20. Power-Up Timing with No Battery and No Load – Battery Detection
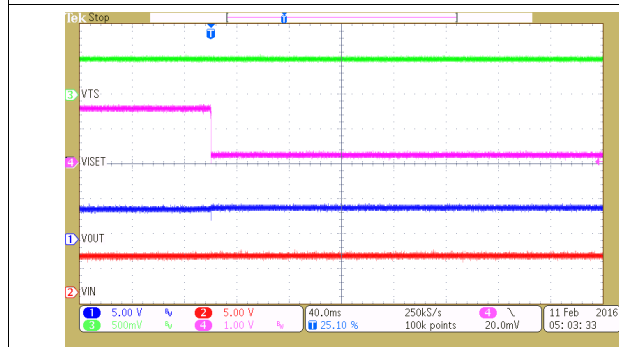
Figure 21. Battery Removal – GND Removed 1st, 42-Ω Load
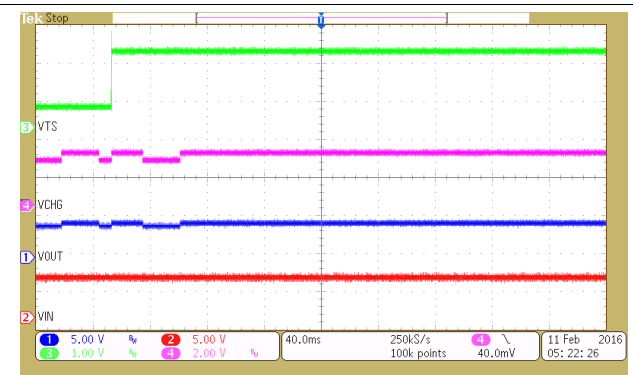
Figure 22. Battery Removal With OUT and TS Disconnect 1st, With 100-Ω Load
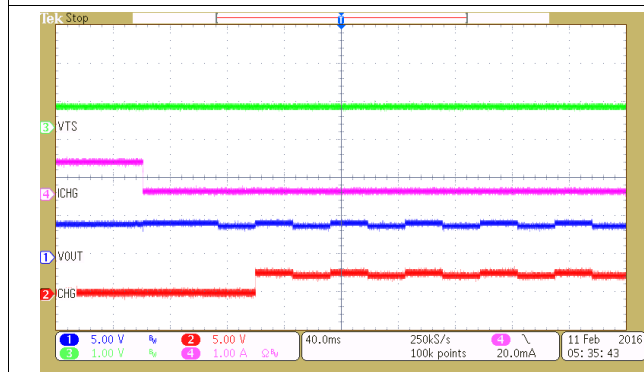
Continuous battery detection when not in TTDM

Figure 23. Battery Removal With Fixed TS = 0.5 V
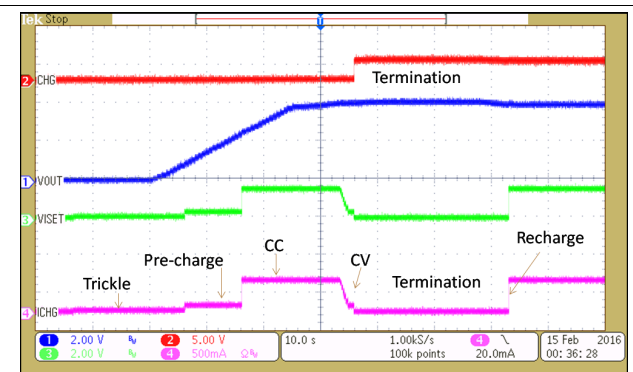
CH4: I_{OUT} (1A/Div)
Battery voltage swept from 0V to 4.25V to 3.9V.

Figure 24. Battery Charge Profile

Product Folder Links: *bq21040*

Typical Application (continued)
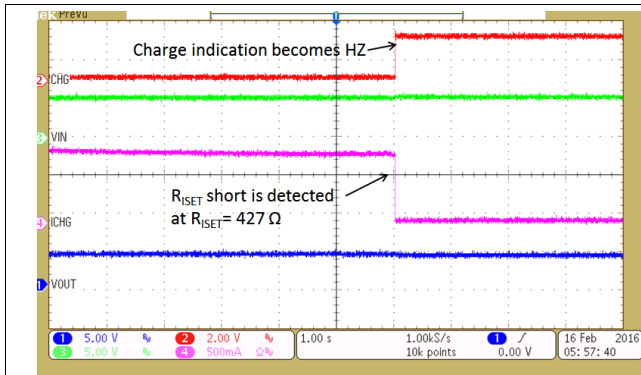
CH4: I$_{OUT}$ (1A/Div)

Figure 25. ISET Shorted During Normal Operation
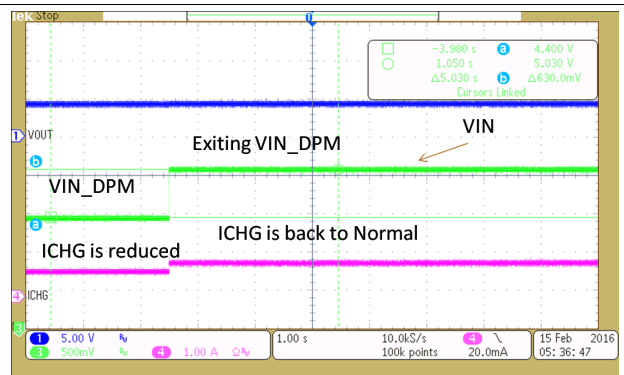
CH4: I$_{OUT}$ (0.2A/Div)

Figure 26. ISET Shorted Prior to USB Power-up
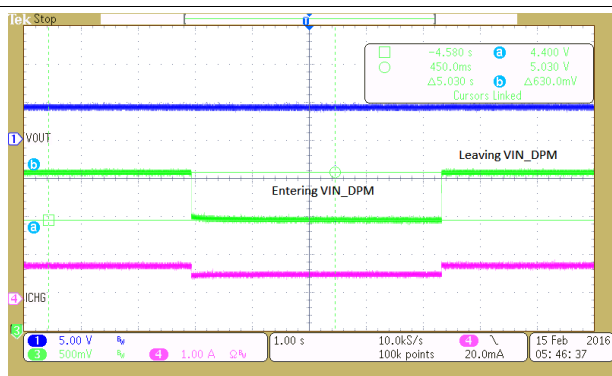
CH4: I$_{OUT}$ (0.2A/Div)

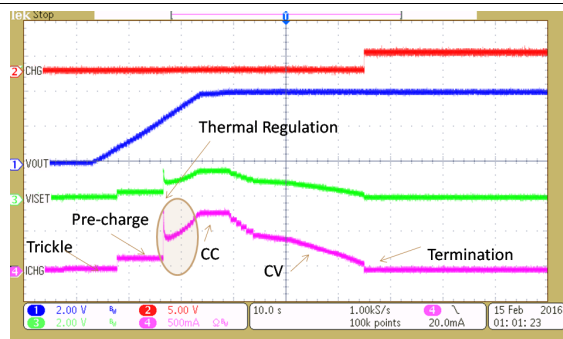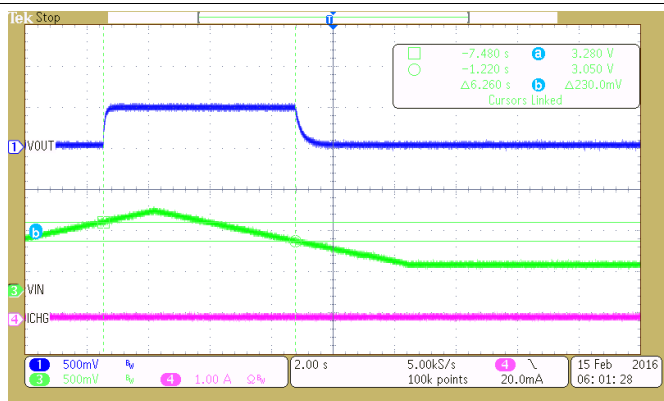**Figure 27. DPM – Adaptor Current Limits – VIN Regulated**
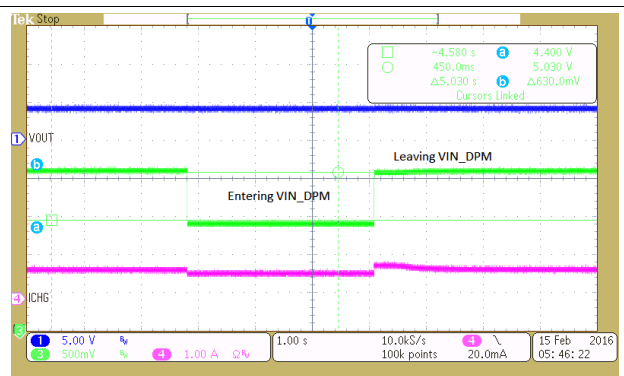
Figure 28. DPM – USB Current Limits – VIN Regulated to 4.4 V

The IC temperature rises to 125°C and enters thermal regulation. Charge current is reduced to regulate the IC at 125°C. VIN is reduced, the IC temperature drops, the charge current returns to the programmed value

.

Figure 29. Charge Cycle With Thermal Regulation

V$_{IN}$ swept from 5 V to 3.9 V to 5 V   V$_{BAT}$ = 4 V

Figure 30. Entering and Exiting UVLO

Product Folder Links: *bq21040*

10 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 3.5 V and 28 V and current capability of at least the maximum designed charge current. This input supply should be well regulated. If located more than a few inches from the bq21040 IN and GND terminals, a larger capacitor is recommended.
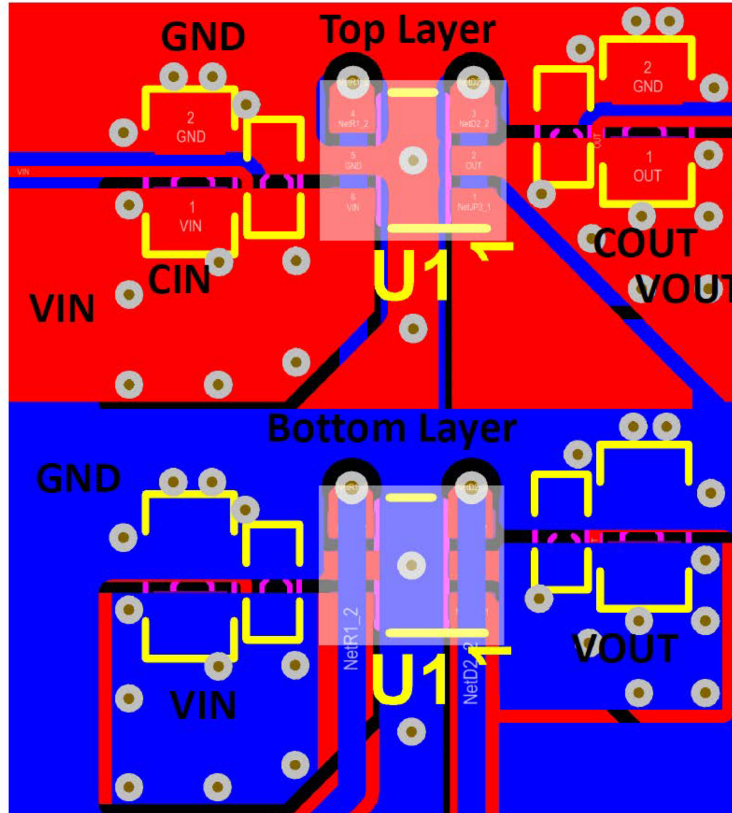
11 Layout

11.1 Layout Guidelines

To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the bq21040, with short trace runs to both IN, OUT, and GND (thermal pad).

- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into IN terminal and from the OUT terminal must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces
- The bq21040 is packaged in a thermally-enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. It is best to use multiple 10mil vias in the power pad of the IC and close enough to conduct the heat to the bottom ground plane. The bottom ground place should avoid traces that "cut off" the thermal path. The thinner the PCB the less temperature rise. The EVM PCB has a thickness of 0.031 inches and uses 2 oz. (2.8mil thick) copper on top and bottom, and is a good example of optimal thermal performance.

11.2 Layout Example

Figure 31. Board Layout

11.3 Thermal Considerations

The bq21040 is packaged in a thermally-enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). The power pad should be directly connected to the VSS terminal. The most common measure of package thermal performance is thermal impedance ($R_{\theta JA}$) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for ψ_{JT} is:

$$\psi_{JT} = (T_J - T) / P$$

where

- T_J = Chip junction temperature
- P = Device power dissipation
- T = Case temperature   (7)

Factors that can influence the measurement and calculation of ψ_{JT} include:

1. Whether or not the device is board mounted
2. Trace size, composition, thickness, and geometry
3. Orientation of the device (horizontal or vertical)
4. Volume of the ambient air surrounding the device under test and airflow
5. Whether other surfaces are in close proximity to the device being tested

Due to the charge profile of Li-Ion and Li-Pol batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. Typically after fast charge begins the pack voltage increases to ≠3.4V within the first 2 minutes. The thermal time constant of the assembly typically takes a few minutes to heat up so when doing maximum power dissipation calculations, 3.4V is a good minimum voltage to use. This is verified, with the system and a fully discharged battery, by plotting temperature on the bottom of the PCB under the IC (pad should have multiple vias), the charge current and the battery voltage as a function of time. The fast charge current will start to taper off if the part goes into thermal regulation.

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged:

$$P = [V_{(IN)} - V_{(OUT)}] \times I_{(OUT)} + [V_{(OUT)} - V_{(BAT)}] \times I_{(BAT)}$$ (8)

The thermal loop feature reduces the charge current to limit excessive IC junction temperature. It is recommended that the design not run in thermal regulation for typical operating conditions (nominal input voltage and nominal ambient temperatures) and use the feature for non typical situations such as hot environments or higher than normal input source voltage. With that said, the IC will still perform as described, if the thermal loop is always active.

11.3.1 Leakage Current Effects on Battery Capacity

To determine how fast a leakage current on the battery will discharge the battery is an easy calculation. The time from full to discharge can be calculated by dividing the Amp-Hour Capacity of the battery by the leakage current. For a 0.75AHr battery and a 10µA leakage current (750 mAHr / 0.010 mA = 75000 hours), it would take 75k hours or 8.8 years to discharge. In reality the self discharge of the cell would be much faster so the 10µA leakage would be considered negligible.

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ21040DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 125	130E	Samples
BQ21040DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	0 to 125	130E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ21040DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
BQ21040DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ21040DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
BQ21040DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0

DBV (R−PDSO−G6)   PLASTIC SMALL−OUTLINE PACKAGE

6   4

Pin 1
Index Area

DETAIL:
OPTIONAL ORIENTATION
MARKING

1   3

0,95

6X $\frac{0,50}{0,25}$ $\boxed{\oplus}$ $\boxed{0,20}$ Ⓜ

6   4

$\frac{1,75}{1,45}$ $\frac{3,00}{2,60}$

Pin 1
Index Area
(See Detail)

1   3

$\frac{3,05}{2,75}$

$\frac{0,22}{0,08}$

Gage Plane

$\boxed{0,25}$

0°−8°

$\frac{0,60}{0,30}$

1,45 MAX

$\frac{0,15}{0,00}$

Seating Plane

$\boxed{0,10}$

4073253−5/N 12/14

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
         E.   Falls within JEDEC MO−178 Variation AB, except minimum lead width.

DBV (R−PDSO−G6)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

1,00

0,55

2,7

2,7

0,95

0,95

0,6

Solder Mask Opening

1,05

Pad Geometry

0,07
All Around

4209593−4/C 08/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D.   Publication IPC−7351 is recommended for alternate designs.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
              metal load solder paste. Refer to IPC−7525 for other stencil recommendations.