The Future of Analog IC Technology

Nu-Pulse™, Half-Bridge and Push-Pull CCFL Inverter Controller

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

MPS CONFIDENTIAL AND PROPRIETARY INFORMATION – INTERNAL USE ONLY

DESCRIPTION

The MP1009 is a fixed operating frequency inverter controller that controls two external power MOSFETs in Nu-Pulse ™, Half-Bridge or Push-Pull configuration for powering one or more cold cathode fluorescent lamps (CCFL) to backlight liquid crystal displays (LCD).

The MP1009 offers cost effective solutions with minimized external components. The controller provides high efficiency power conversion of unregulated DC input voltages to nearly pure sine waves. The featured fault detection and protection scheme (patent pending) includes open lamp regulation, open lamp protection and short lamp protection.

Burst mode dimming is controlled with either an external analog or digital signal. Lamp voltages and lamp currents are continuously regulated under any operating conditions.

The MP1009 is available in a 16-pin SOIC package.

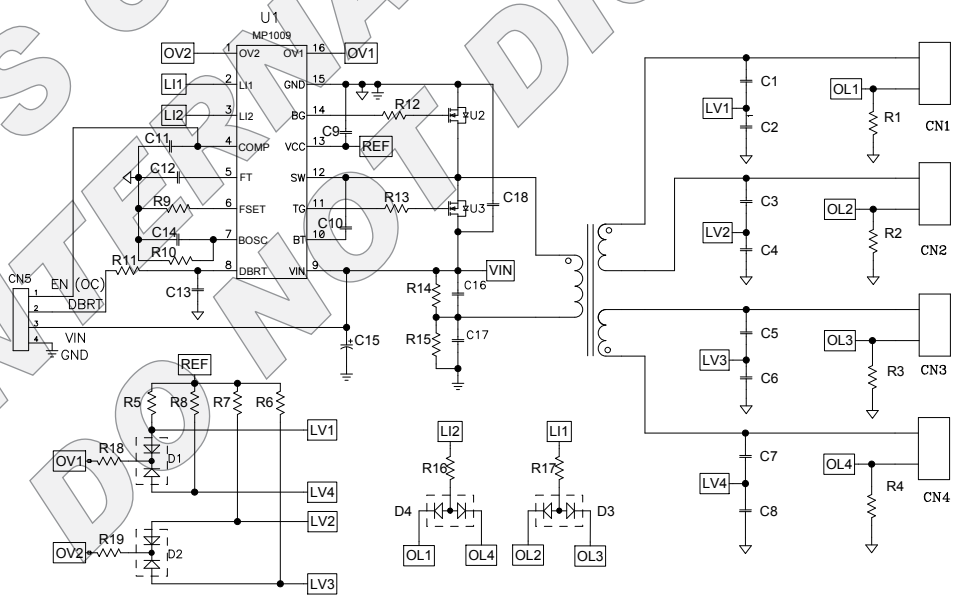
FEATURES

- Drives Two External, Low Cost, N-Channel MOSFETs
- Fixed Operating Frequency
- Input Voltage Range of 8V to 30V
- Lamp Current and Voltage Regulation
- Burst Mode Dimming Control
- Integrated Burst Mode Oscillator and Modulator
- Soft-On and Soft-Off Burst Envelope
- Open Lamp & Short circuit Protection
- Fault Timer and Indicator
- Available in SOIC 16 Package

APPLICATIONS

- Desktop LCD Flat Panel Displays
- Flat Panel Video Displays
- LCD TVs and Monitors

TYPICAL APPLICATION

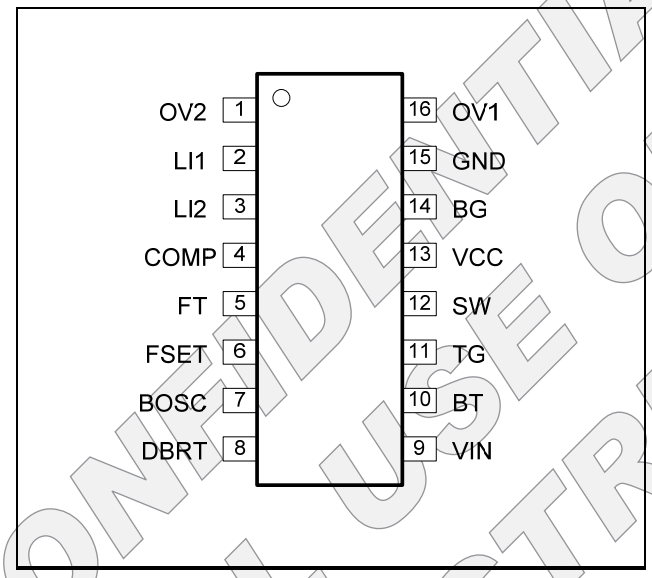


ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP1009ES	SOIC16	MP1009ES	-20°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP1009ES–Z).
For RoHS Compliant packaging, add suffix –LF (e.g. MP1009ES–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage VIN 34V
BT and TG ..... -0.3V to VIN+VCC
SW. ..... -0.3V to VIN
VCC and BG ..... -0.3V to +6.5V
Logic Inputs ..... -0.3V to +6.5V
LI1 and LI2 Inputs ..... -5.8V to +5.8V
OV1 and OV2 inputs ..... -0.3V to +14.5V
Continuous Power Dissipation (T_A = +25°C) (2)
..... 1.56W
Junction Temperature ..... 150°C
Power Dissipation 0.6W
Lead Temperature (Solder) ..... 260°C
Operating Frequency 150kHz
Storage Temperature ..... -55°C to +150°C

Recommended Operating Conditions (3)

Input Voltage V_{IN} ..... 8V to 30V
Digital Brightness Voltage V_{DBRT} ..... 0V to 1.2V
Operating Frequency ..... 20kHz to 100kHz
Operating Frequency (Typical) 50kHz
Operating Junct. Temp (T_J) .... –20°C to + 125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
SOIC16	80	30 °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 17.5V, T_A = +25°C, unless otherwise noted.

Parameter Sy	mbol	Condition	Min	Typ	Max	Units
Gate drive TG, BG						
Gate Pull-Down	R_{GD}			1.6		Ω
Gate Pull-Up	R_{GU}			5		Ω
Brightness Control Range						
DBRT Full Scale	V_{DBRT}	DC burst dimming	1.1	1.2	1.3	V
DBRT Logic Input Threshold		PWM dimming	1.6	1.9	2.2	V
DBRT Logic Input Hysterisis		PWM dimming		0.3		V
Burst Rate Generator						
Source Current	$I_{SRC(BRS)}$	V_{BRS} = 2V	120	150	180	µA
Lower Threshold	$V_{V(BRS)}$		2.20	2.40	2.60	V
Upper Threshold	$V_{P(BRS)}$		3.3	3.55	3.8	V
Supply Current						
Supply Current (Enabled)	I_{PR} No	Switching		1.7	3	mA
Supply Current (Disabled)	I_{PR}			7	15	µA
Operating Frequency	f_O 100	kΩ FSET to GND	44	48	52	kHz
Frequency Set Voltage	V_{SWS}		1.1	1.2	1.3	V
Lamp Current Feedback (LI1 and LI2)						
Pull Up Current Source	I_{source}			55		µA
Open Lamp Detect Threshold	V_{TH_OL}		0.9	1.1	1.3	V
Protection Delay	T_{D_SC}			220		µs
Magnitude |V	$_{LI}$|		2.87	3.05	3.23	V
Lamp Voltage Feedbacks (OV1 and OV2)						
Open La mp Voltage Feedback Threshold (Peak)	V_{TH}		10.7	11.5	12.3	V
Input Resistance		OV1, OV2 pin to GND		300		kΩ
Short Circuit Detect Threshold	V_{TH_SC}	DC bias 6V	4.5	4.9	5.3	V
Protection Delay	T_{D_SC}			300		µs
Fault Indicator						
Threshold	$V_{t(FT)}$		1.15	1.21	1.27	V
Sink Current	$I_{SINK(FT)}$			–1		µA
Open Lamp Source Current	$I_{PU\_OL(FT)}$			1		µA
Short Lamp Source Current	$I_{PU\_SL(FT)}$			100		µA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 17.5V, T_A = +25°C, unless otherwise noted.

Parameter Sy	mbol	Condition	Min	Typ	Max	Units
Comp						
IC On Threshold (Used as EN Function)	V_{ON_TH}	Rising threshold	0.55	0.65	0.75	V
Enable Hysteresis				150		mV
Clamp Voltage	V_{COMP}		0.8	0.9	1	V
Reference Current	I_{COMP+}			20		µA
Decay Current	I_{COMP-}	End of Burst		12		µA
Output (VCC)						
Voltage V	CC		5.6	5.9	6.2	V
Current I	CC			5		mA

PIN FUNCTIONS

Pin #	Name	Description
1	OV2	Open lamp voltage feedback input 2. Connect this pin to the tap of a cap divider and a bias resistor to VCC for lamp voltage feedback. In multi-lamp application, connect this pin through a diode in “or” relationship to all lamp voltage feedback points, which are AC in phase. If the peak voltage value at OV2 pin exceeds +11.5V, the controller treats this as lamp over-voltage condition. A pulse of current will pull-down the COMP pin voltage to regulate the lamp voltage. The burst dimming signal is ignored and the Fault Timer starts ramping up. This signal is also used for short circuit protection. If the voltage at OV2 is always above 4.9V, the controller will treat this as a short circuit condition after a certain delay. The Fault Timer will start ramping up. In single lamp application, connect OV1and OV2 pins together.
2	LI1	Lamp current feedback 1. Connect this pin to the current sense resistor. In multi-lamp application, connect this pin through a diode in “and” relationship to all lamp current feedback points, which are AC in phase. Combined with the lamp current feedback signal from LI2, the signal is fed to the internal error amplifier. Selecting the feedback resistors can easily program the lamp current. The signal is also used for open lamp protection. If the voltage at LI1 is always below 1.1V, the controller treats this as an open lamp condition after a certain delay. The burst dimming signal is ignored and the Fault Timer starts ramping up. In single lamp application, short LI1 to LI2 pin and connect to the lamp current feedback resistor through a small RC filter.
3	LI2	Lamp current feedback 2. The function of this pin is same as LI1. In multi-lamp application, this pin is used for lamp current feedback which is out-of-phase of LI1.
4	COMP	Feedback Compensation Node. Connect a compensation capacitor from this pin to GND. This pin is also used for IC enable control. A logic low (below 0.5V) input turns off the IC. The enable logic input signal should have open collector (OC) structure.
5	FT	Fault Indicator. Connect a capacitor from this pin to GND to program the open lamp and short lamp protection delay time. When the voltage on this pin reaches 1.2V, the IC is shutdown until it is enabled again.
6	FSET	Switching Frequency Set. Connect a resistor from this pin to GND. This resistor sets the operating frequency of the MP1009.
7	BOSC	Burst Repetition Rate Setting. For DC input internal burst dimming, connect a resistor and a capacitor from this pin to GND. The burst dimming frequency and minimum dimming duty is programmed by the resistor and capacitor values. For external logic PWM input dimming, connect BOSC to VCC and apply the logic signal to the DBRT pin.
8	DBRT	Burst-Mode (Digital) Brightness Control Input. For DC input internal burst dimming, the voltage range of 0V to 1.2V at DBRT linearly sets the burst-mode duty cycle from minimum to 100%. For external logic PWM input dimming, drive DBRT pin higher than 2.2V and lower than 1.6V to directly control the inverter dimming duty. If burst dimming is not used, connect DBRT to VCC.
9	VIN	Input Power Rail. Decouple this pin to GND with >1μF ceramic capacitor. It is desirable to add a 10Ω resistor between VIN pin and the input bus.
10	BT	Output Bootstrap. BT provides gate driver bias for the high-side MOSFET. Connect a capacitor from BT to SW.
11	TG	High-Side MOSFET Gate Output. Connect TG to the gate of the high-side, external power MOSFET.
12	SW	Bridge Output. Connect SW to the source of the high-side MOSFET and the drain of the low-side MOSFET.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
13	VCC	Voltage Rail Output. VCC provides power supply for the low-side gate driver and the internal control circuitry. Bypass VCC to GND with a ceramic capacitor.
14	BG	Low-Side MOSFET Gate Output. Connect BG to the gate of the low-side MOSFET.
15 GND		Circuit Ground. Connect power GND and analog GND of the PCB to this pin. The power GND for power switches and the analog GND for the control signals is desired to be separated and only connected at this pin.
16 OV1		Open lamp voltage feedback input 1. The function of this pin is same as OV2. In multi-lamp application, this pin is used for lamp voltage feedback which is out-of-phase of OV2.

BLOCK DIAGRAM

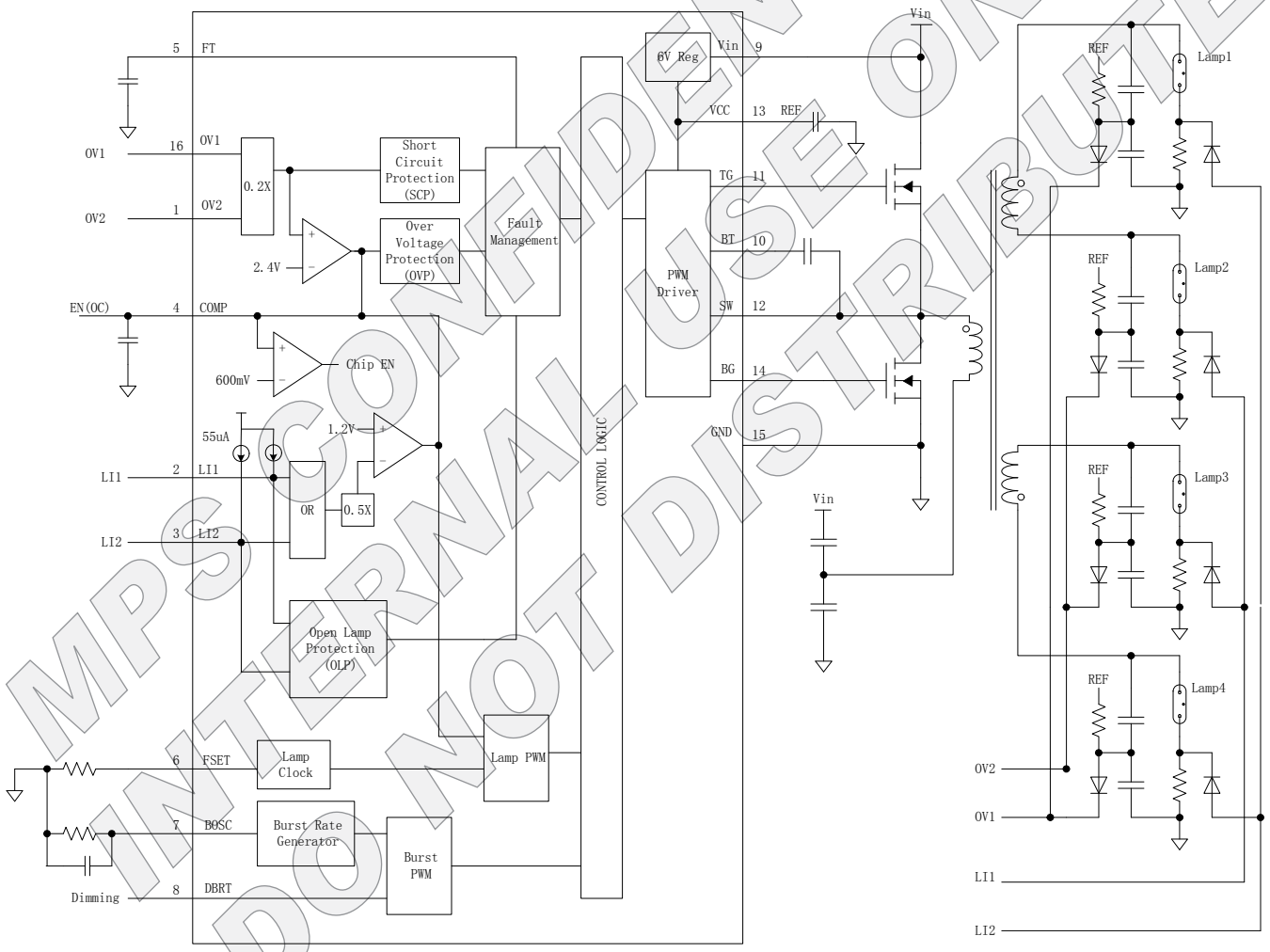


Figure 1—Functional Block Diagram

OPERATION

The MP1009 is a fixed frequency inverter controller for CCFL application, especially optimized for multi-lamp applications. The MP1009 has an integrated bootstrap driver stage which offers the advantage of adopting low cost N-MOSFET as the upper switch.

EN Function

The MP1009 has integrated EN function with the feedback compensation pin COMP. A logic low (typical below 0.5V) turns off the IC. An open collector (OC) signal is required as EN signal which connected to COMP.

Lamp Current/Voltage Regulation

The MP1009 features two current and two voltage feedback pins to achieve: lamp current regulation, lamp over-voltage regulation and protection. When the lamp is lit, the duty cycles of the power devices are regulated to maintain the lamp current feedback. In open or unstuck lamp conditions the peak value of the lamp voltage is similarly regulated via the lamp voltage feedback.

Both pairs of feedback signals are simultaneously functional during operation. In multi-lamp applications, the in-phase and out-of-phase signal current and voltage signals can be connected to separate pins, which dramatically simplify the external circuit. In addition the MP1009 derives Fault conditions via these feedback pins, further simplifying external circuitry.

Switching Frequency

The switching frequency is set by the resistance from the FSET pin to ground.

At open lamp condition, the internal open lamp control circuit adopts the adaptive frequency control method based on the input, output condition, which sets the open lamp frequency automatically. The adaptive frequency control method can guarantee the striking voltage at any temperature, which is also not sensitive to the parameters variation in practical production. The maximum frequency under this operation mode is set to be 1.4 times of normal frequency.

Fault Protection

When the lamp is open, the voltage feedback on OV1 and OV2 pin is used to regulate the lamp voltage. The voltage feedback on OV1 and OV2 is scaled down with an internal 0.2 gain stage. If the peak value exceeds 2.4V after the gain stage, the COMP pin will be pulled down by a 20μA current pulse. At the same time, the FT timer will be charged by the 1μA current. If the FT voltage exceeds 1.2V, the controller will shut-down.

Also, the lamp current feedback pin LI1 and LI2 can be used for open lamp protection. In open lamp condition, the corresponding current feedback signal will be zero, which will trigger the internal FT timer.

When the lamp is shorted, the related lamp voltage feedback will be zero, which will change the waveform fed into OV1/ OV2 pin. If the voltage signal is always above 4.9V, the short circuit detector will trigger the FT timer, and the FT timer will be charged by a 100uA current source.

Burst Dimming

MP1009 implements burst dimming (digital brightness) control to the lamp. Burst mode operation dims the lamp by modulating the duty cycle of a burst of AC lamp current and features soft-on/soft-off control of the lamp current envelope. Burst dimming can be achieved by either a DC voltage input or an external PWM signal. The MP1009 has a built-in burst oscillator which can generate a triangle waveform on the BOSC pin. A DC voltage can be applied on the DBRT pin and it linearly controls the burst dimming duty cycle. If the BOSC pin is tied to VCC (6V), the DBRT pin can be directly driven with an external PWM dimming signal (100Hz - 500Hz).

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at excedingly high temperatures. When the silicon die temperature is higher than 150°C, it shuts down the whole chip. When the temperature is lower than its lower threshold, typically 145°C, the chip is enabled again.

APPLICATION INFORMATION

The typical 4-lamp half bridge application circuit is used as an example to describe the design procedure.

Pin 2 (LI1) & Pin 3 (LI2): Lamp Current Regulation and Open Lamp Protection

R1~R4 is used to set the current for each lamp. For multi-lamp application, the lamps can be divided into two groups, in-phase group and out-of-phase group. LI1 and LI2 can be used for these two groups separately. In each group, the lamp current feedback signal is connected to LI1/LI2 pin via a diode, which forms an AND gate with an internal 55uA pull up current source.

The lamp current signal on LI1 and LI2 is combined in a full wave rectifier and scale down with an internal resistor divider, the gain is 0.5. The internal reference is 1.2V for average value, For the 4 lamp application with diode on LI pin, the lamp current sense resistor can be calculated as:

$$R1 \approx 2.7V / I_{(LAMP)rms}$$

Where $I_{(LAMP)rms}$ is the lamp rms current. For 7.4mA rms, R1~R4 is 374Ω.

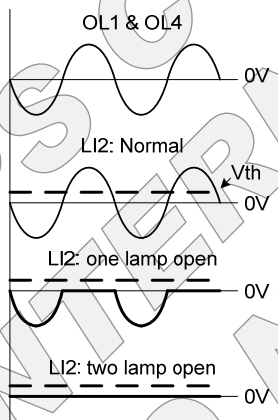


Figure2—Open lamp protection with LI1/LI2

Also, the lamp current feedback signal on LI1/LI2 pin is compared to internal 1.1V reference before the internal resistor divider. In normal operation, the voltage waveform should be sinusoidal wavefo rms. In open lamp condition, the positive half cycle will be missed as shown in Figure 2, which will trigger the open lamp protection.

Pin1 (OV2) & Pin 16 (OV1): Lamp Voltage Regulation and Short Circuit Protection

OV1 and OV2 are used for lamp voltage feedback and short circuit protection with the unique protection method (patent protected).

In multi-lamp application, the lamps should also be divided into two groups, i.e. in-phase group and out-of-phase group. OV1 and OV2 pin can be used for these two groups separately, which is just the same as lamp current feedback. Also, if the lamps are all in-phase, they can be divided into two groups equally.

A DC bias (REF, 6V) is added to lamp voltage feedback for short circuit protection. An internal resistor divider with 0.2X gain scales down the input signal.

In normal operation, the OV1 and OV2 waveforms should be sinusoidal with 6V DC bias as shown in Figure 3. In the short circuit condition, the negative half cycle will be missed, which will trigger the internal protection circuit. The protection threshold for OV1/ OV2 pin is 4.9V.

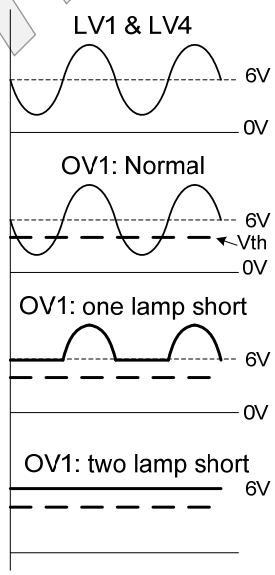


Figure3— Short Circuit protection with OV1/OV2

The regulated open lamp voltage is proportional to the ratio of C1 to C2 (also, C3 to C4, C5 to C6 and C7 to C8).

C1 has to be rated at 3kV and is typically between 5pF to 22pF. The value of C2 is set by

customer to program the required open lamp voltage. The value of DC bias resistors (R5~R8) is typically 10kΩ.

For safety operation, V_{PP} for normal operation should be at least 3V, thus the maximum open lamp voltage ratio (open lamp voltage to normal operation lamp voltage) is 4:1.

Pin 4 (COMP): C11
C11 is the feedback compensation capacitor (connected between COMP and analog GND). A 1.5nF~4.7nF (X7R ceramic) cap is recommended. The value of C11 affects the soft-on rising time and soft-off falling time of the lamp current at each burst dimming cycle by changing the comp voltage slew rate.

The EN function is also combined with COMP pin. If the COMP pin is pulled down below 0.5V, the IC will turn off. The EN signal connected to COMP pin should have the open collector (OC) structure to avoid any affecting in COMP pin under normal operation. If the EN signal from system is not an OC signal, an extra NPN transistor is required to get the OC structure. Be careful, if the extra NPN transistor is used, the polarity of EN is reversed (Active at low input).

Pin 5 (FT): C12
The capacitor C12 from FT to GND sets the fault timer. This capacitor will determine the time MP1009 takes to react the fault threshold (1.2V). User can choose the capacitor value to program the protection delay time.

Pin 6 (FSET): R9
R9 is used to set the lamp operating clock. The value for R9 is calculated by:

$$R9 = 100k\Omega \times \frac{48kHz}{f_S}$$

For R9 = 100kΩ, the operating clock will be 48 kHz.

For open lamp:

C12=T(open lamp)*(1uA)/1.2V

For a C12=820nF, then the time out for open lamp is 0.98s.

For short circuit:

The internal current for short circuit protection is 100uA instead of 1uA for open lamp protection, the off time will be approximately 100 times faster than open lamp time. To reduce the short turn off timer further, the connection at FT node can be modified to:

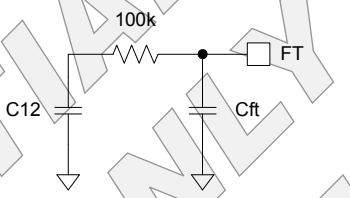


Figure 4— Turn off time Adjustment

Cft can be used to adjust the short circuit turn off time.

Pin 7 (BOSC): C14, R10
BOSC is used to set the Burst Repetition Rate. C14 and R10 will set the burst repetition frequency (f_{BURST}) and the minimum burst on time (t_{MIN}) as shown in Figure 5.

Set t_{MIN} to achieve the minimum required system brightness and ensure that t_{MIN} is long enough so that the lamp does not extinguish. These values are determined as follows:

Select a Minimum Burst Duty Cycle (D_{MIN}) where:

$$D_{MIN} = t_{MIN} \times f_{BURST}$$

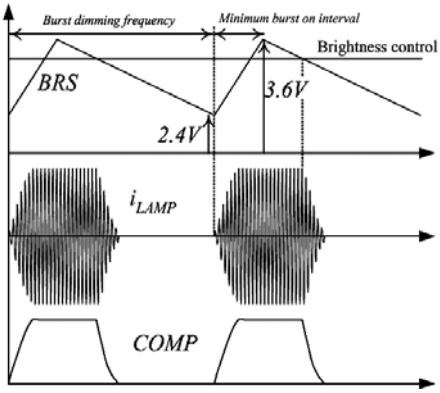


Figure 5—Burst Mode with DC input voltage at DBRT pin.

R10 and C14 can be estimated by the following equations:

$$R10 \approx 21.16k\Omega \left(\frac{1}{D_{MIN}} - 1 \right) + 21.43k\Omega$$

$$C14 = \frac{1 - D_{MIN}}{f_{BURST} \times 10 \quad 0.405}$$

For D_{MIN}=0.1, f_b=200Hz, we get R10=212kΩ, C14=52nF.

If the burst dimming is to be controlled by an external logic signal, connect BOSC to VCC and apply the logic signal to the DBRT pin.

Table 1—Function Mode

Function	Pin Connection	
	DBRT	BOSC
Burst Mode with DC Input Voltage	0V to 1.2V	C14, R10
Burst Mode with External Source	PWM V	CC

Burst Brightness Polarity: 100% duty cycle at DBRT voltage 1.2V.

Pin 8 (DBRT): R11, C13
DBRT is used for burst brightness control. The DC voltage on this pin will control the burst percentage on the output. The signal should be locally filtered for optimal operation. A voltage ranging from 0V to 1.2V on DBRT will correspond to a Burst Duty Cycle from minimum to 100%, respectively. R11 and C13 form a low pass filter to reduce the noise of the input DC voltage. Recommended values are 10kΩ and 0.1μF.

For direct Pulse Width Modulation of the burst signal, connect BOSC to VCC and drive DBRT with a logic level PWM signal. A logic-High is Burst-On and a logic-Low is Burst-Off.

Pin 9 (VIN): C15, C18 Input Power Rail
An electrolytic capacitor and a ceramic capacitor are recommended between VIN and power ground. The ceramic capacitor C18 should be placed close to the MOSFETs to supply the high frequency energy and attenuate the switching noise. Note that the loop are a formed by U2, U3 and C18 must be minimized.

Pin 10 (BT): C10
BT is the bias supply for the level shift of the upper MOSFETs. C10 should be large enough to supply the energy required for driving the MOSFET. A 100nF capacitor of X7R ceramic material is recommended.

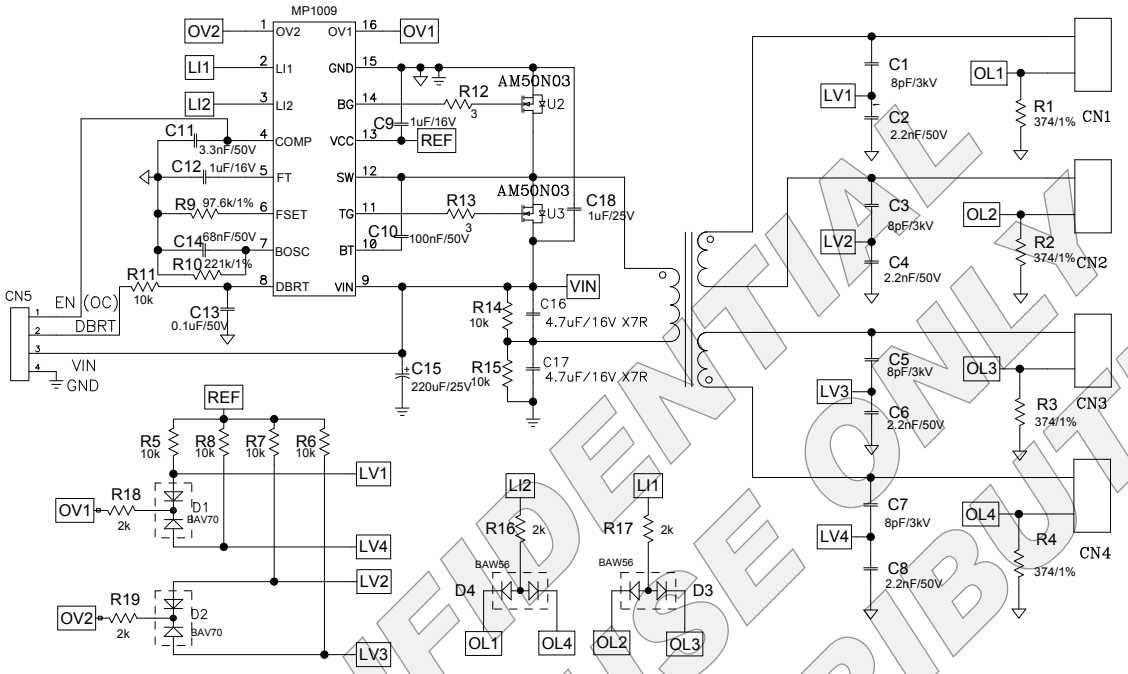
Pin 11 (TG), Pin 14 (BG): R12, R13
These pins are used to drive the MOSFETs. A 0Ω~15Ω series gate resistor is optional to reduce the switching noise.

Pin 12 (SW)
This pin connects to the source of the high-side MOSFET and the drain of the low-side MOSFET in the output bridge. One end of the primary transformer is also connected to this pin.

Another end of the transformer is connected to a capacitor divider as shown in Figure 1. The capacitors C16 and C17 should be ceramic and have a ripple current rating greater than the primary current. X7R type of capacitors are preferred. Their value is typically in a range of 2.2μF~6.3μF. R14 and R15 are used to ensure the voltages across the capacitors are zero at start up. Typically, R14 and R15 are 10kΩ.

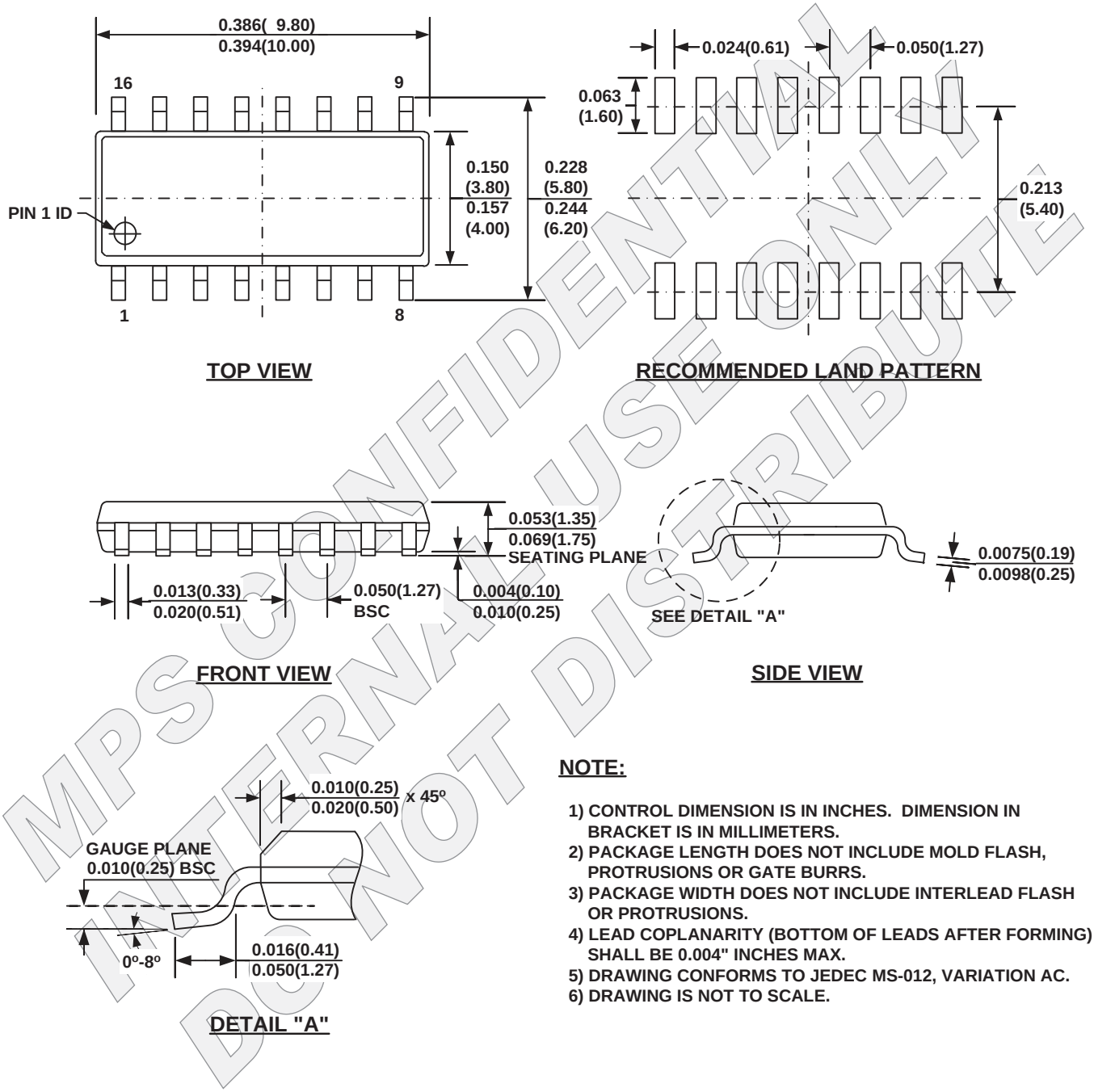
Pin 13 (VCC): C9
This capacitor bypasses the 6V gate supply for the low-side switches. It also supplies power to the internal logic circuit of MP1009. This pin should be bypassed with a ceramic X7R capacitor. The recommended value is 1uF.

TYPICAL APPLICATION CIRCUIT



PACKAGE INFORMATION

SOIC16



NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AC.
6) DRAWING IS NOT TO SCALE.