OZ9932

LCD Monitor CCFL Inverter Controller

FEATURES

- Built-in intelligence to ignite positive impedance CCFLs
- Universal panel interface
- Enhanced output drive capability
- Over 200 steps dimming control
- Low cost LCD TV inverter solution
- Constant operating frequency
- Operating frequency can be synchronized with external signal
- Integrated synchronized PWM dimming control with wide dimming range
- Built-in intelligence for ignition and normal operation of CCFLs
- Built-in open-lamp protection and over-voltage protection
- Optimized soft-start function
- Shutdown delay for input voltage brownout
- Supports multiple CCFLs

ORDERING INFORMATION

Part Number	Temp Range	Package
OZ9932G	0°C to 70°C	8-pin SOIC
OZ9932GN	0°C to 70°C	8-pin SOIC, Lead-Free
OZ9932D	0°C to 70°C	8-pin PDIP
OZ9932DN	0°C to 70°C	8-pin PDIP, Lead-Free

GENERAL DESCRIPTION

The patent pending OZ9932 is a cost-effective CCFL (Cold Cathode Fluorescent Lamp) Power Management controller designed for CCFL, Liquid Crystal Display (LCD) applications.

The OZ9932 provides two drive signals for most power conversion topologies, such as push-pull, half-bridge, full-bridge or Class-D inverters while maintaining high-efficiency operation. The controller converts unregulated DC voltages into nearly sinusoidal lamp voltage and current waveforms. The highly integrated controller encompasses current and voltage regulation, soft-start operation, over-voltage protection and an external enabling function while maintaining a high-degree of design flexibility.

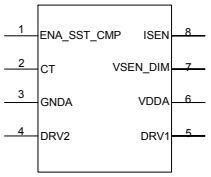
OZ9932 operates at a constant operating frequency. The operating frequency can be synchronized with an external signal that eliminates any undesired interference between the controller and LCD panel. OZ9932 drives all types of CCFLs and is able to ignite positive impedance CCFLs. OZ9932 provides a shutdown delay feature for input voltage brownout condition.

The controller provides a wide dimming range by converting an external analog control input into a low-frequency Pulse Width Modulation (LPWM) dimming function. The control logic provides a regulated ignition voltage and appropriate protection for over-voltage or over-current conditions.

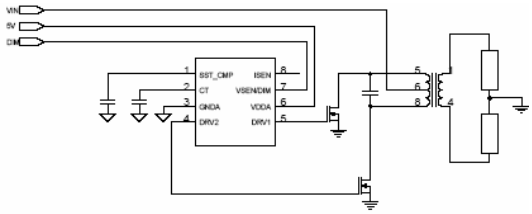
The OZ9932 offers a high level of integration, while maintaining flexibility and high-efficiency operation that reduces component heating. This results in higher reliability and longer CCFL life. The proprietary (patent pending) design technique provides a simpler, lower-cost system solution.

With its enhanced output drive capability, OZ9932 is ideal for LCD monitor and LCD TV applications.

PIN DESCRIPTION



SIMPLIFIED APPLICATION DIAGRAM



PIN DESCRIPTION

Names	Pin No.	Description
ENA_SST_CMP	1	Enable, Soft Start Time and Compensation
CT	2	Timing Capacitor to Set Striking, Operating and LPWM Frequency
GNDA	3	Ground
DRV2	4	N MOSFET Drive Output
DRV1	5	N MOSFET Drive Output
VDDA	6	Supply Voltage
VSEN_DIM	7	Voltage Sense_Dimming Voltage
ISEN	8	Current–Sense Feedback

ABSOLUTE MAXIMUM RATINGS(1)

Input Voltage VDDA	7.0V
GNDA	+/- 0.3V
Signal Inputs	-0.3V to VDDA +0.3V

Operating Temp.	OZ9932
	0^{o}C to $+70^{o}$C

Operating Junction Temp.	125^{o}C
Storage Temp.	-55^{o}C to 150^{o}C

RECOMMENDED OPERATING RANGE

VDDA - Input Voltage	4.5V to 5.5V
f_{op} - Operating Frequency	30KHz to 150KHz
Thermal Impedance (θ_{J-A}) - 8-pin SOIC	113^{o}C/W
Thermal Impedance (θ_{J-A}) - 8-pin PDIP	74^{o}C/W

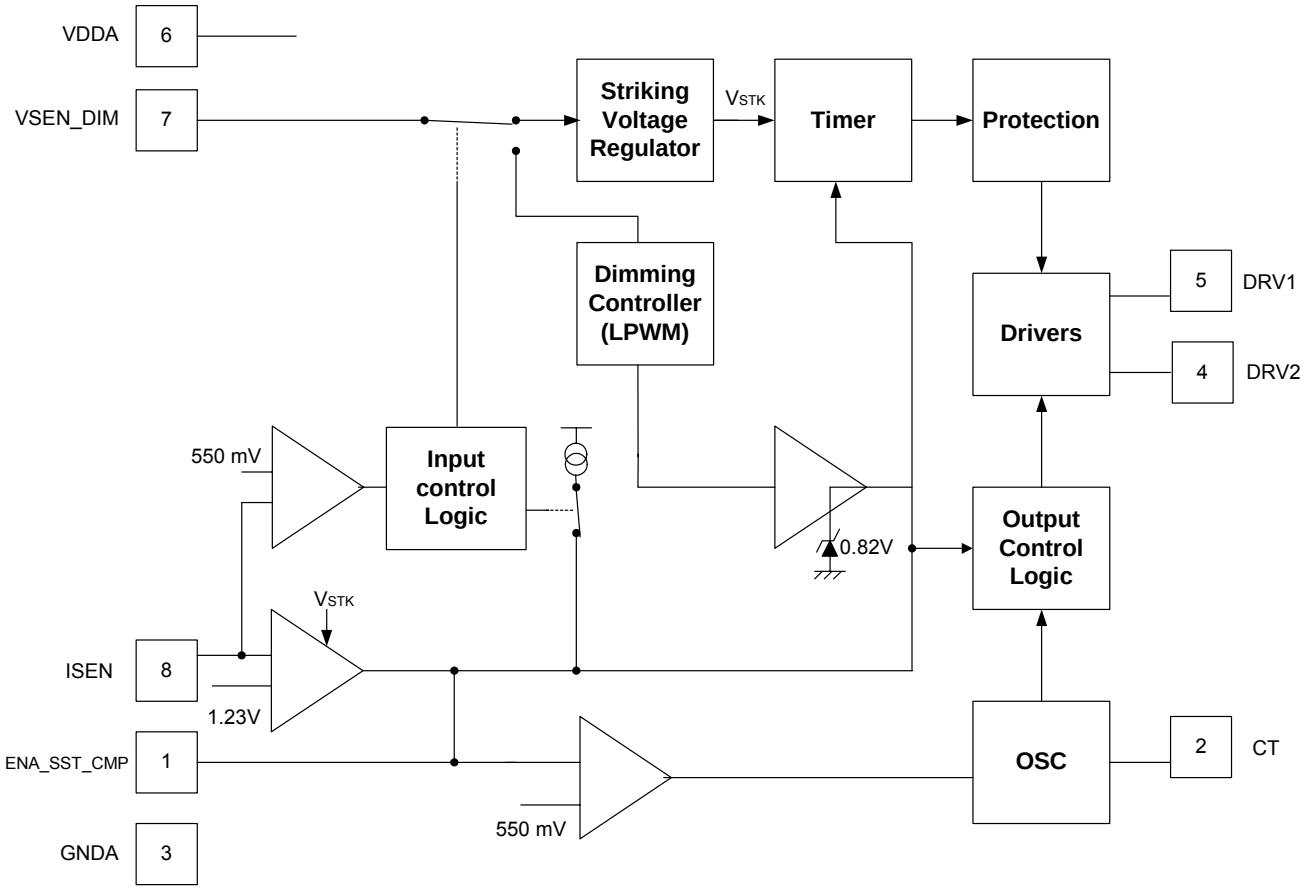
Note (1): The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The "Electrical Characteristics" table defines the conditions for actual device operation. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Conditions		Limits		Unit
		VDDA=5V; C_T=357pF; C_{SST}=12.1nF, Ta=25 °C	Min	Typ	Max	
Supply Current						
Stand By	I_{dds}	V_1=0V; V_8=0V	-	350	500	μA
Operating	I_{dd}	V_1=2V; V_8=0V Capacitance at DRV1 & DRV2=500pF	-	2.5	4.2	mA
Soft Start Current Source	I_{SST}	V_1=0V; V_8=0V; V_7=0V	1.7	2.7	4.0	μA
Under Voltage Lockout	UVLO	V_1=1.2V; VDDA from 0V to 5V	3.22	3.6	4.25	V
ENA_SST_CMP Pin - Low	V_{CMP}		0.77	0.83	0.88	V
CT Pin Peak Valley						
CT Pin Peak	Vpeak	V_1=2V; V_8=660mV; V_7=2.8V	2.87	3.03	3.20	V
CT Pin Valley	Vvalley	V_1=2V; V_8=660mV; V_7=2.8V	0.98	1.05	1.12	V
Operating Frequency on DRV1 & DRV2 Pin	fop	V_1=1.2V; V_8=660mV; V_7=2.8V	48.7	50.2	51.7	kHz
		Thermal Coefficiency	-	350	-	ppm/ °C
LPWM Frequency	f_{LF}	V_1=1.2V; V_8=660mV; V_7=1.5V	428	449	470	Hz
		Thermal Coefficiency	-	360	-	ppm/ °C
Dimming						
LPWM Duty Cycle	LPWM	V_7=0.22V	-	10	-	%
LPWM Duty Cycle	LPWM	V_7=2.2V	-	-	99	%
LPWM Duty Cycle	LPWM	V_7=2.41V	100	-	-	%
Duty Cycle on DRV1 & DRV2 (active high)						
Maximum		V_1=3.5V; V_8=0V; V_7=0V	44	-	-	%
Over Voltage Protection Threshold	OVP (V_7)	V_1=1.5V; V_8=0V	2.93	3.10	3.25	V
Open Lamp Protection Threshold	OPLAMP (V_1)	V_8=0V; V_7=0V; VDDA from 4.5V to 5.5V	VDDA - 1.6	-	VDDA - 0.8	V
Ignition Time		V_8=0V	1.7	2.0	2.3	sec
Open Lamp Shutdown Delay Time		V_1=VDDA	2.21	2.60	2.99	sec
Lamp Current Reference Voltage	ISEN		1.189	1.235	1.278	V
		Thermal Coefficiency	-	275	-	ppm/ °C
V_1 (ENA_SST_CMP Pin) Threshold	ENA		400	550	700	mV
Drivers						
DRV1	Ron	For Iout= 70 mA; Tamb=25°C	3	6	10	Ω
DRV2	Ron	For Iout= 70 mA; Tamb=25°C	3	6	10	Ω

Note: Vx denotes voltage at Pinx

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

1. Power Conversion

The power train can be selected from the standard half-bridge, full-bridge, push-pull or Class-D topologies to provide symmetrical drive pulses to the tank circuit that includes the transformer(s), output capacitors and the CCFL/panel load, to yield quasi-sinusoidal CCFL voltage and current waveforms. High-efficiency operation of the OZ9932 yields lower heat dissipation for the inverter system resulting in higher reliability. Reference Application Circuits for Push-Pull and Half-Bridge topologies are illustrated in Figure 2 & 3 on pages 7 & 8.

OZ9932 controller provides a low system cost.

To illustrate the controller functions, refer to Figures 1 2, and 3 on pages 4, 7 and 8, respectively for the following sections. Other topologies can be found in the OZ9RR Application Note.

2. Enable

The OZ9932 is enabled when the voltage on Pin 1 is greater than 0.55V.

3. Soft Start (SST)

Connecting an external capacitor to Pin 1 provides the SST function. A charging current is provided to capacitor C5. At Start-up, as capacitor C5 charges, the voltage level controls the gradual increase in power to the transformer. This reduces in-rush current and provides reliable operation to the CCFL.

4. Ignition

The ignition process requires a higher striking frequency to strike the CCFL. The striking frequency is approximately 1.3 times the normal operating frequency. The striking frequency is determined by CT (Pin 2), external capacitors C9 and C11.

OZ9932 built-in intelligence ensures successful ignition of all types of CCFLs and is able to ignite positive high impedance CCFLs.

5. Normal Operation

Once the CCFL is ignited and current is sensed at Pin 8 (ISEN), the control loop regulates the CCFL current. The operating frequency is determined by the external capacitors (C9 & C11) connected to CT (Pin 2), where the approximate operating frequency is calculated by the following equation.

$$f_{op} = \frac{18.0 \times 10^3}{C_T\ [pF]} \quad [kHz]$$

6. Over-Voltage Protection

The control logic protects the transformer from an abnormal high voltage at the secondary output.

Once the IC is enabled, an internal timer is activated to provide sufficient time for CCFL ignition (turn-on) and VSEN_DIM (pin 7) senses the voltage at the transformer secondary. The internal timer provides approximately 2.0 seconds, to ensure successful ignition. Within the ~2.0 second ignition period, once the voltage at VSEN_DIM pin reaches ~3.0V, the output voltage is regulated. Conversely, if no current is sensed after approximately ~2.0 seconds (open/damaged lamp), OZ9932 immediately shuts down. Toggling the enable signal from high to low will reinitiate IC start-up.

7. Open Lamp Protection

OZ9932 provides a shutdown delay feature if the lamp current is not regulated. The inverter module will remain in normal operation for ~2-3 seconds if the input voltage suddenly drops and subsequently resumes to a normal level.

When a CCFL is removed or damaged during normal operation, the OZ9932 shuts off the output drives after the shutdown delay timer expires. When the damaged lamp is replaced, toggling the enable pin from low to high resumes normal operation.

8. Aged CCFL Ignition

During the ignition process, the controller senses the voltage at the CCFL. For an open-circuit condition, the power train delivers a regulated voltage at the CCFL for approximately two seconds. This is to ensure that any aged, slow-turn-on CCFL is provided with sufficient voltage and time to ignite.

9. Dimming Control

The OZ9932 internal LPWM dimming control circuitry provides a wide low-frequency dimming range. The input to Pin 7 (VSEN_DIM) is an analog voltage of 0.2V to 2.3V that produces a LPWM duty cycle of 10% to 100%.
The output of the LPWM signal has a duty cycle proportional to the input dimming signal command (VDIM). A resistive network (R1, R2 and R3) is inserted between the external dimming input and Pin 7 to provide user flexibility for different dimming input voltage ranges, such as 0V to 3V or 0V to 5V.

A wide dimming range is achieved by utilizing LPWM control method, via the low-frequency PWM generator circuitry. OZ9932 operates in a constant frequency mode, in which the frequency is set by external capacitors C9 and C11 connected to CT (Pin 2). The operating and LPWM frequencies are internally synchronized. The operating frequency can also be synchronized to the LCD monitor system by providing an external signal to pin 2. This eliminates any undesired interference between the controller and LCD panel, as the interference is usually associated with variable-frequency design. Interference may result in a poor user experience because of “waterfall” display distortion and other poor display appearance.
The approximate dimming frequency (low frequency) is internally generated and calculated using the following equation:

$$f_{LF} = \frac{161 \times 10^3}{C_T\,[pF]}\,[Hz]$$

REFERENCE APPLICATION CIRCUIT: PUSH-PULL TOPOLOGY

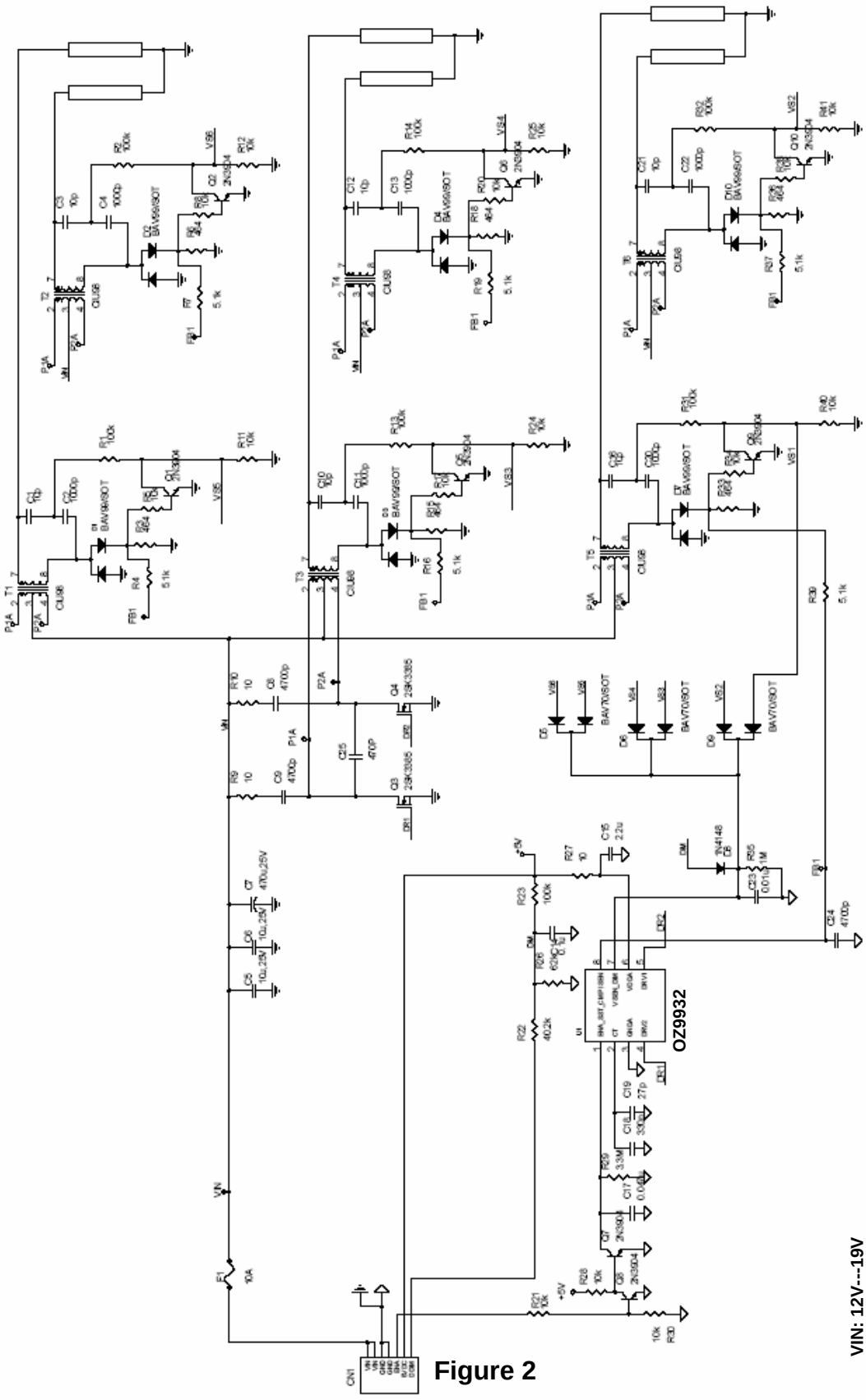


Figure 2

REFERENCE APPLICATION CIRCUIT: HALF-BRIDGE TOPOLOGY

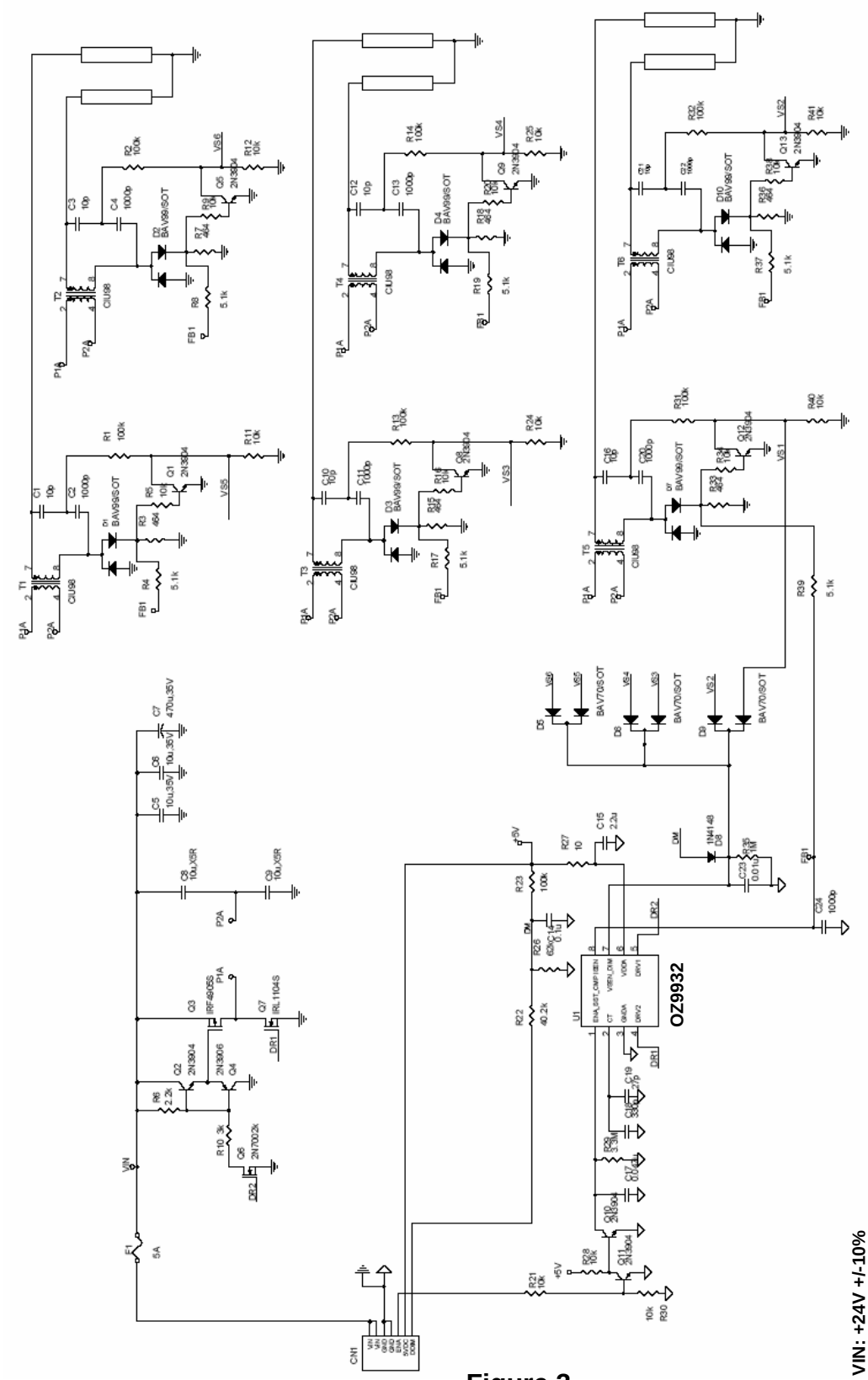
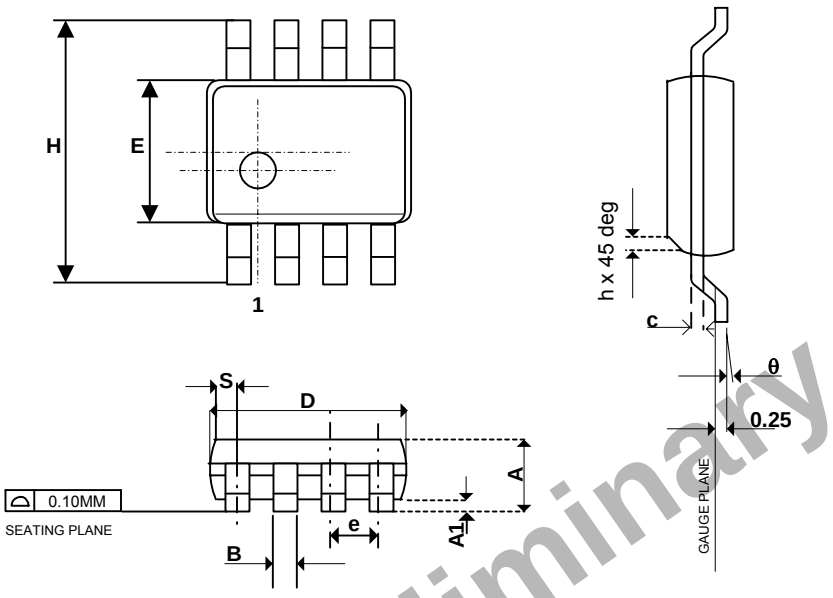


Figure 3

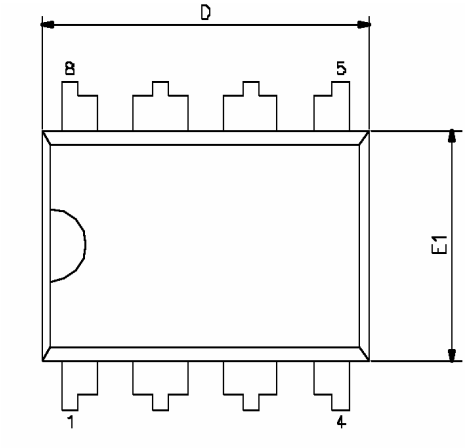
PACKAGE INFORMATION – 8-PIN SOIC: OZ9932G

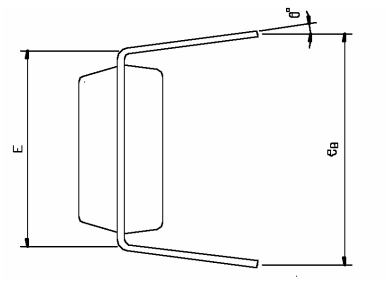


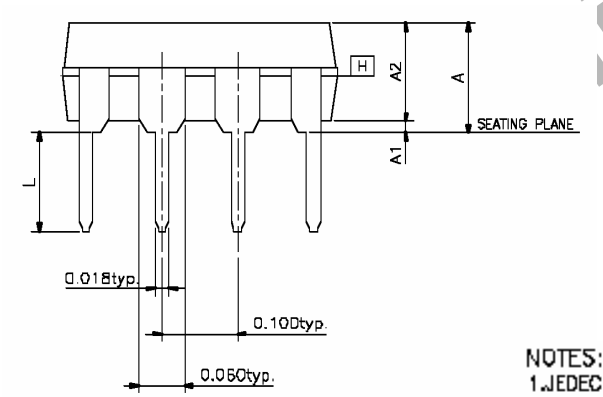
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
c	0.008	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050 BSC.		1.27 BSC.	
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
S	0.0155	0.0255	0.394	0.648
θ	0°	8°	0°	8°
D	-	-	4.80	5.00
JEDEC	MS-012AA			

Notes:
1. Controlling dimensions are in millimeter (mm).
2. Pin #1 count orientation shall be in counterclockwise direction as viewed in live-bug position.

PACKAGE INFORMATION – 8-PIN PDIP: OZ9932D







SYMBOLS	MIN	MIN	MAX
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	0.355	0.365	0.400
E	0.300 BSC		
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ	0	7	15

NOTES:

1. JEDEC OUTLINE : MS-001 BA
2. "D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINIMUM.
6. DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

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