STR2A100 Series Application Note (Rev.0.3)

The contents in this application note are preliminary, and are subject to changes without notice.

SANKEN ELECTRIC CO., LTD.
http://www.sanken-ele.co.jp

Contents

1. General Descriptions

The STR2A100 series are power ICs for switching power supplies, incorporating a power MOSFET and a current mode PWM controller IC in one package. Including a startup circuit and a standby function in the controller, the product achieves low power consumption, low standby power and high cost-effectiveness power supply systems with few external components.

2. Features and Production lineup

Features and benefits include the following

- DIP8 package, connecting one side (pin5 to pin8) with a power MOSFET drain.
  The distance between high voltage terminal and low voltage terminal is 0.762mm (0.3inches), and the wider drain trace is available to enhance thermal dissipation of the IC.
- Current Mode PWM control
- Built-in Random Switching Function, reducing EMI noise, and simplifying EMI filters, by the slight random change of PWM frequency, f_{OSC}.
- Auto Standby Function (Input Power, P_{IN} < 25mW at no load)
  Normal load operation ---------- PWM mode
  Light load operation ---------- Standby mode (Burst oscillation)
- Built-in Audible Noise Suppression Function for standby mode
- Built-in Startup Circuit, reducing power consumption in standby operation, and eliminating external components.
- Bias Assist Function, improving startup operation, suppressing V_{CC} voltage drop in operation, and allowing use of smaller V_{CC} capacitor.
  Soft Start Function, reducing stress of a power MOSFET and secondary rectifiers at startup
- Built-in Leading Edge Blanking Function
- Built-in Slope Compensation Function, avoiding subharmonic oscillation.
- Two Chip Structure, with a controller and a power MOSFET guaranteed Avalanche Energy which is available to simplify surge absorber circuits
- Protection Functions
  −Overcurrent Protection Function (OCP) ---------- Pulse-by-pulse, built-in compensation circuit to minimize OCP point variation for AC input voltage
  −Overload Protection Function (OLP) ---------- Auto restart, built-in delay timer to reduce temperature rise
  −Overvoltage Protection Function (OVP) ---------- Shutdown with latch mode
  −Thermal Shutdown Protection Function (TSD) ---------- Shutdown with latch mode

Product Lineup

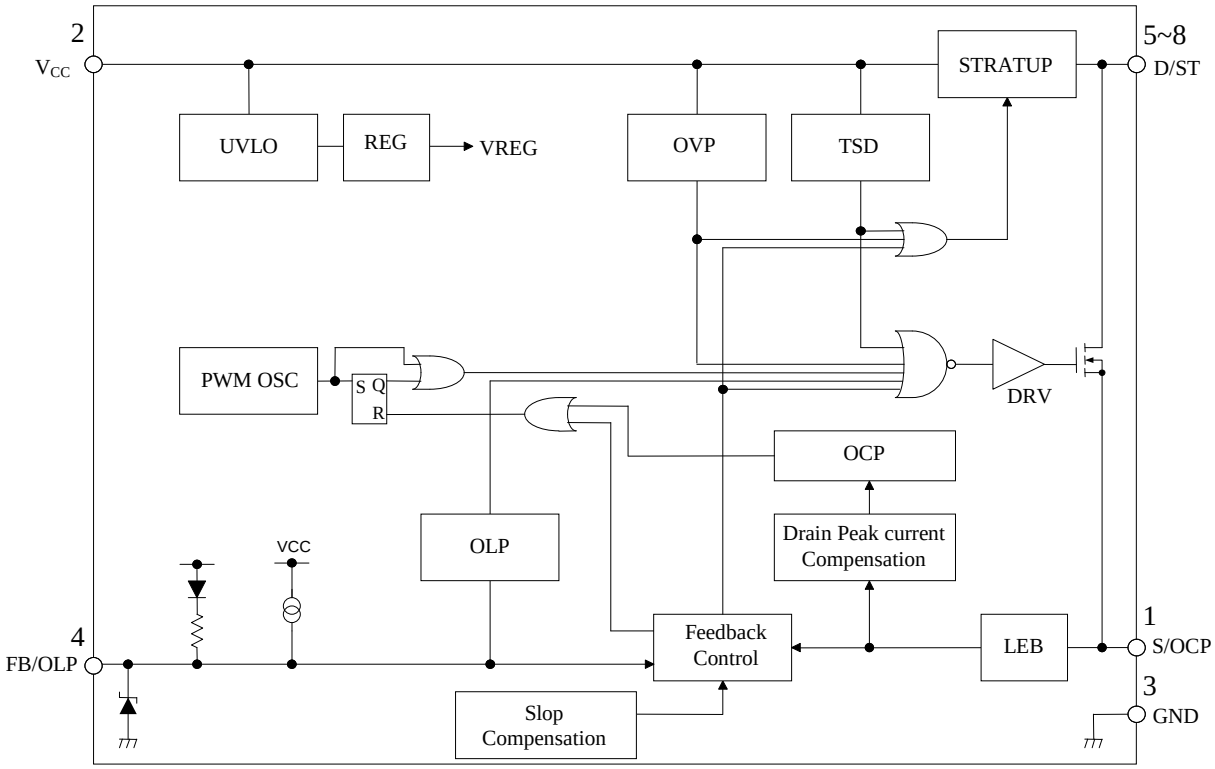
Part Number	f_{OSC} (kHz)	MOSFET V_{DSS} MIN (V)	$R_{DS(ON)}$ ※2 MAX	P_{OUT} ※1 ※2 230VAC/85VAC to 265VAC	Status
STR2A152	67	650	3.0Ω	30W / 23W	Planning
STR2A153			1.9Ω	36W / 30W	Sample available
STR2A155			1.1Ω	43W / 35W	Planning

※1 The open frame conditions.
The listed output power is based on the thermal ratings, and the peak output power is obtained by 120 to 140% of the value stated here. In low output voltage and narrow ON-duty cycle, the output power may be less than the value stated here.

※2 The preliminary values on IC development

3. Functional Block Diagram and Terminal List

Functional Block Diagram

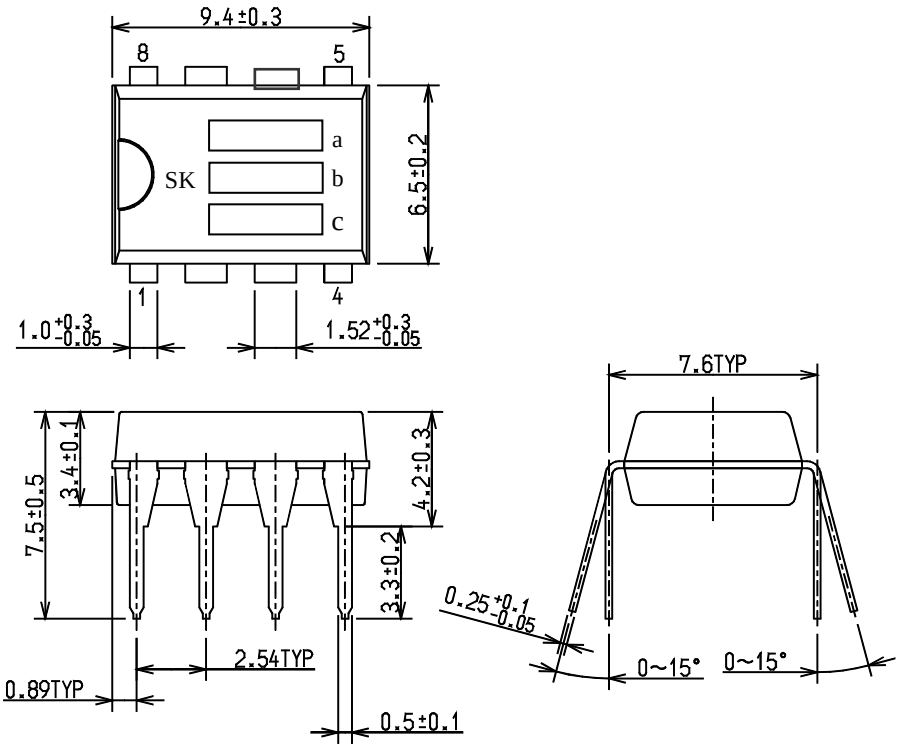


Terminal List Table

Number	Name	Functions
1	S/OCP	MOSFET source / Overcurrent protection control pulse input
2	V_{CC}	Power supply input for control circuit
3	GND	Ground
4	FB/OLP	Constant voltage control signal input / Overload protection signal input
5	D/ST	MOSFET drain / Startup current input
6		
7		
8		

4. Package Information

- DIP8 package



Material of terminal: Cu
Treatment of terminal: solder plating
Weight: Approx. 0.51g
Unit: mm

a. Type Number : 2AXXX
b. Lot Number
1st letter : The last digit of year
2nd letter : Month
1 to 9 for Jan. to Sept.
O for Oct.
N for Nov.
D for Dec.
3rd letter : Week
1st～10th : 1
11th～20th : 2
21st～31st : 3
c. Sanken Registration Number

5. Electrical Characteristics

- The STR2A153 of STR2A100 series is used as an example.
- Certain details vary among the individual products.
- The preliminary values at IC development

5.1 Absolute Maximum Ratings

T_a= 25°C, unless otherwise specified

Parameter	Terminal	Symbol	Ratings	Unit	Notes
Drain peak current ※1	8−1	I_{DPEAK}	4.4	A	Single Pulse
Avalanche energy ※1	8−1	E_{AS}	72	mJ	Single Pulse V_{DD}=99V, L=20mH
		I_{LPEAK}	2.46	A	
S/OCP terminal voltage	1−3	V_{OCP}	−2～6	V	—
Controller IC (MIC) input voltage	2−3	V_{CC}	32	V	—
FB/OLP terminal voltage	4−3	V_{FB}	−0.3～14	V	—
FB/OLP terminal sink current	4−3	I_{FB}	1.0	mA	—
MOSFET power dissipation ※1 ※2	8−1	P_{D1}	1.76	W	—
Controller IC (MIC) power dissipation	2−3	P_{D2}	1.3	W	—
Operating ambient temperature	—	T_{OP}	−20～+115	°C	Recommended internal frame temperature T_F= 115°C(Max)
Storage temperature	—	T_{stg}	−40～+125	°C	—
Channel temperature	—	T_{ch}	+150	°C	—

※1 Refer to individual product datasheet for details because these values differ among the various product types.

※2 The condition mounted on 15mm×15mm printed circuit board.

※ Current characteristics are defined based on IC as Sink:+, Source:−.

5.2 MOSFET Electrical Characteristics

Ta= 25°C, unless otherwise specified

Parameter	Terminal	Symbol	Ratings			Unit
			MIN	TYP	MAX	
Drain-to-Source breakdown voltage ※1	8−1	V_{DSS}	650	—	—	V
Drain leakage current	8−1	I_{DSS}	—	—	300	μA
On-resistance ※1	8−1	$R_{DS(ON)}$	—	—	1.9	Ω
Switching time	8−1	t_f	—	—	250	ns
Thermal resistance ※1 ※3	—	θ_{ch-F}	—	—	20	°C/W
		θ_{ch-C}	—	—	30	

※3 θ_{ch-F} is the thermal resistance between channel and internal frame.
θ_{ch-C} is the thermal resistance between channel and case. Case temperature (T_C) is measured at the center of the marking side.

5.3 Electrical Characteristics

Ta= 25°C, V_{CC}= 18 V, unless otherwise specified

Parameter	Terminal	Symbol	Ratings			Unit
			MIN	TYP	MAX	
Operation start voltage	2－3	$V_{CC(ON)}$	13.8	15.3	16.8	V
Operation stop voltage ※4	2－3	$V_{CC(OFF)}$	7.3	8.1	8.9	V
Circuit current in operation	2－3	$I_{CC(ON)}$	—	—	2.5	mA
Minimum startup voltage	8－3	$V_{ST(ON)}$	—	40	—	V
Startup current	8－3	Istartup	−3.9	−2.5	−1.1	mA
Startup current supply threshold ※4	2－3	$V_{CC(BIAS)}$	8.5	9.5	10.5	V
Average switching frequency	8－3	$f_{OSC(AVE)}$	60	67	74	kHz
Frequency modulation deviation	8－3	△f	—	5	—	kHz
Maximum on-duty cycle	8－3	D_{MAX}	65	74	83	%
Leading edge blanking time	—	t_{BW}	—	350	—	ns
OCP compensation coefficient	—	D_{PC}	—	17	—	mV/μs
OCP compensation duty cycle limit	—	D_{DPC}	—	36	—	%
OCP threshold voltage at zero duty cycle	1－3	$V_{OCP(L)}$	0.69	0.78	0.87	V
OCP threshold voltage at 36% duty cycle	1－3	$V_{OCP(H)}$	0.79	0.88	0.97	V
Maximum feedback current	4－3	$I_{FB(MAX)}$	−280	−170	−90	μA
Minimum feedback current	4－3	$I_{FB(MIN)}$	−30	−15	−7	μA
Oscillation stop FB/OLP voltage	4－3	$V_{FB(OFF)}$	1.05	1.15	1.25	V
OLP threshold voltage	4－3	$V_{FB(OLP)}$	7.3	8.1	8.9	V
Operation current after OLP	2－3	$I_{CC(OLP)}$	—	230	—	μA
OLP delay time	—	t_{OLP}	54	68	82	ms
FB/OLP terminal clamp voltage	4－3	$V_{FB(CLAMP)}$	11	12.8	14	V
OVP threshold voltage	2－3	$V_{CC(OVP)}$	26	29	32	V
Thermal shutdown operating temperature	—	$T_{j(TSD)}$	135	—	—	℃

※4 The relationship between $V_{CC(BIAS)}$ and $V_{CC(OFF)}$ consists of $V_{CC(OFF)} < V_{CC(BIAS)}$.

※ Current characteristics are defined based on IC as Sink:+, Source:－.

6. Typical Application Circuit

A typical application circuit is shown below. The following design features should be considered:

- D/ST terminals (pin 5 to pin8) are on one side of the IC. The PCB traces from them should be as wide as possible, in order to enhance thermal dissipation.
- In applications having a power supply specified such that V_{DS} voltage between D/T terminal and S/OCP terminal has large transient surge voltages, a clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added between both sides of a winding P, or a damper snubber circuit of a capacitor (C) or a resistor-capacitor (C, RC) combination should be added between D/ST terminal and S/OCP terminal.

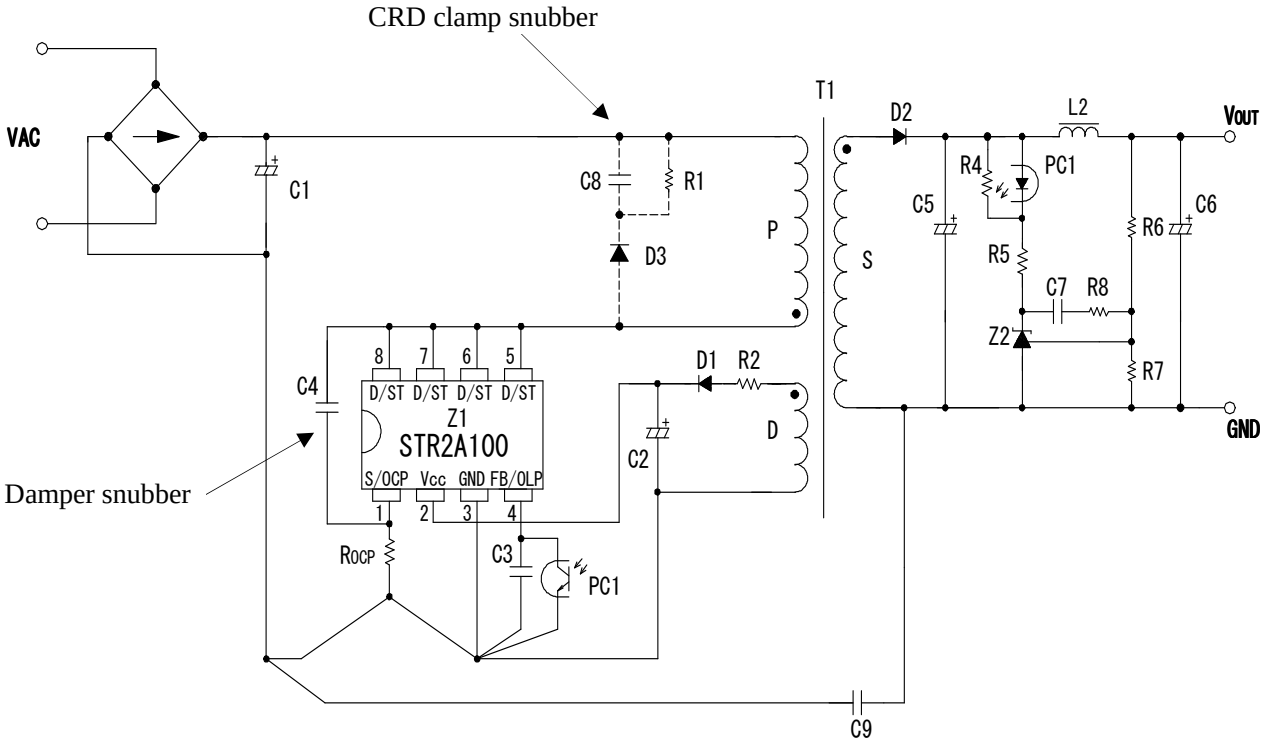


Figure 6 Typical application circuit example

7. Functional Descriptions

The parameter values in this section are based on the STR2A153 specification, unless otherwise specified.
The polarity of current is shown as "+"for sink current and "−" for source current based on IC

7.1 Startup Operation

The startup circuit is connected to D/ST terminal.
During the startup process, the constant current, $I_{STARTUP}$= −2.5mA(TYP), charges C2 at V_{CC} terminal in figure 7-1, and when V_{CC} terminal voltage increases to $V_{CC(ON)}$= 15.3V(TYP), the control circuit starts switching operation. After switching operation begins, the startup circuit turns off automatically, to zero its current consumption.
The approximate startup time, t_{START}, is calculated as follows

$$t_{START} = C2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{|I_{STARTUP}|} \qquad \text{------(1)}$$

where t_{START} is in sec,
and $V_{CC(INT)}$ is the initial voltage on V_{CC} terminal, in V.

C2 value is 10 to 47μF for general power supply applications.

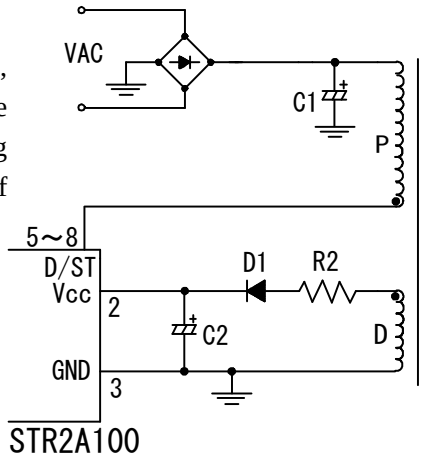


Figure 7-1 V_{CC} peripheral circuit

Figure 7-2 shows the relationship of V_{CC} and I_{CC}.
When V_{CC} terminal voltage increases to $V_{CC(ON)}$= 15.3V(TYP), the control circuit starts switching operation and the circuit current, I_{CC}, increases. In operation, when V_{CC} terminal voltage decreases to $V_{CC(OFF)}$= 8.1V(TYP), the control circuit stops operation by UVLO (Undervoltage Lockout) circuit, and reverts to the state before startup.
The voltage from the auxiliary winding D in figure 7-1 becomes a power source to the control circuit in operation. The auxiliary winding voltage needs to be adjusted to about 15 to 20 V, taking account of the winding turns of the winding D so that V_{CC} terminal voltage should become as follows within the specification of input voltage range and the output load range of power supply.

$$V_{CC(BIAS)} = 10.5V(MAX) < V_{CC} < V_{CC(ON)} = 26.0V(MIN)$$

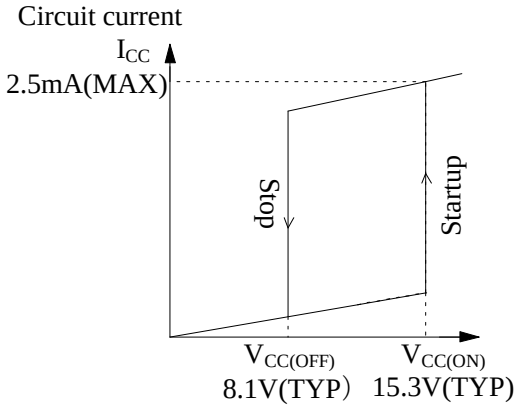


Figure 7-2 Relationship of V_{CC} and I_{CC} at startup and shutdown

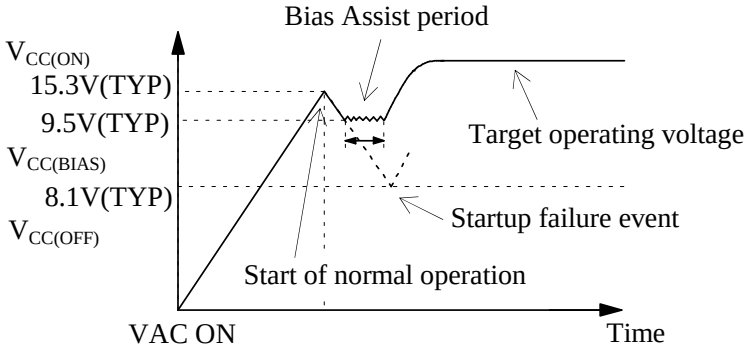


Figure 7-3 V_{CC} behavior during startup

Figure 7-3 shows V_{CC} terminal voltage behavior during the startup period. After V_{CC} terminal voltage increases to $V_{CC(ON)}$ at startup, the auxiliary winding voltage on the winding D does not rise to the target operating voltage immediately (which is set by the transformer ratio between the auxiliary winding and the secondary winding), and may fall down. When V_{CC} terminal voltage decreases to $V_{CC(BIAS)}$= 9.5V(TYP), Bias Assist Function is activated so that the decrease of V_{CC} terminal voltage is suppressed by $I_{STARTUP}$ provided from the startup circuit.
In addition, Bias Assist Function allows C2 value to be reduced and allows the startup time to be shorter, and this function allows the response of overvoltage detection in V_{CC} terminal to be faster.

In actual power supply circuits, V_{CC} voltage often fluctuates according to the output currents of power supply as shown in figure 7-4. This happens because C2 is charged to a peak voltage on the winding D, which is caused by the transient surge voltage coupled from the primary winding when a power MOSFET turns off.

Suppressing C2 peak charging, it is effective to add R2, of several ohms to several tenths of an ohm, in series with D1 as shown in figure 7-5. The optimum value of R2 should be determined on actual operation with a transformer matching the power supply application, because the variation of the auxiliary winding voltage is determined by the transformer structure design.
The variation becomes worse on the following conditions,

- The coupling between the primary winding and the secondary winding of transformer get worse, for example, a transformer for power supply specifications with low output voltage and/or large output current.
- The coupling between the auxiliary winding D and the stabilizing output winding (which is controlled as a constant voltage) gets worse.

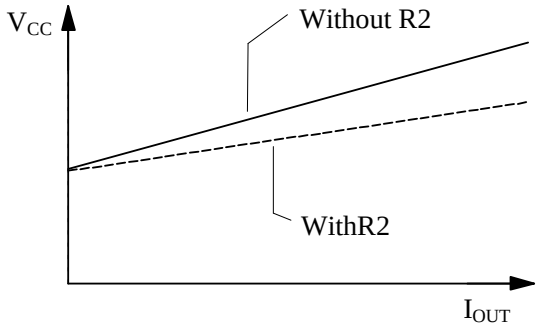


Figure 7-4 Variation of V_{CC} terminal voltage and power supply output current with / without R2 resistor

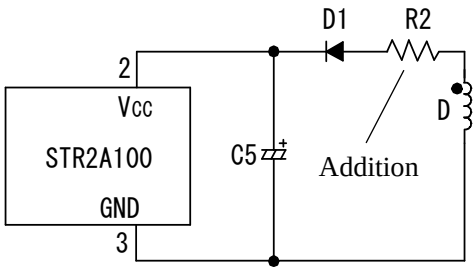
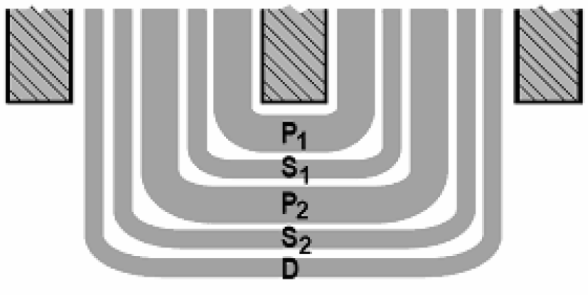


Figure 7-5 V_{CC} external circuit that is not susceptible to fluctuation in power supply output current

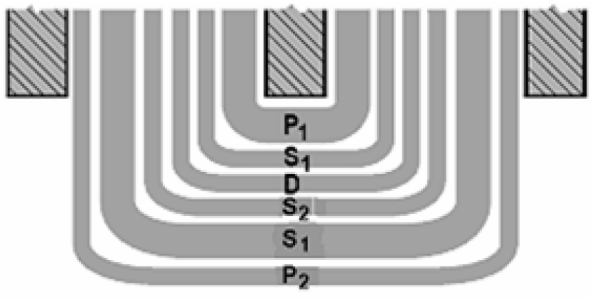
Figure 7-6 and figure 7-7 show alternative designs for the location of auxiliary winding D as examples of transformer structural designs.

- Auxiliary winding D is away from the primary windings P1and P2 (sandwich structure) as shown in figure 7-6 (Transformer structure example ①).
- Auxiliary winding D is within a stabilizing winding S1 (which is controlled as a constant voltage) as shown in figure 7-7 (Transformer structure example ②).



P1, P2: Primary winding
P1, P2 are sandwich structure winding
S1: Secondary control winding
S2: Secondary output winding
D: Auxiliary winding

Figure 7-6 Transformer structure example ①



P1, P2: Primary winding
P1, P2 are sandwich structure winding
S1: Secondary control winding
S2: Secondary output winding
D: Auxiliary winding

Figure 7-7 Transformer structure example ②

7.2 Constant Output Voltage Control

The constant output voltage control of the power supply uses the current-mode control method (the peak current-mode), which enhances response speed and provides stable operation.

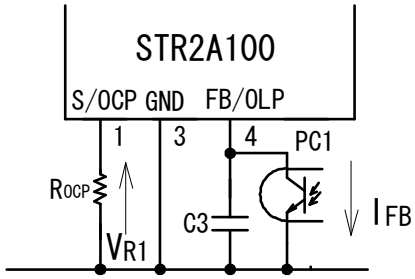


Figure 7-8 FB/OLP peripheral circuit

When load conditions become smaller, the output voltage, V_{OUT}, rises, and a feedback current from an error amplifier on the secondary side also rises. This current corresponded to the feedback current is sunk by a photo-coupler at FB/OLP terminal as shown in figure 7-8, and thus FB/OLP terminal voltage decreases.

This voltage is fed to Feedback Control block in "3. Functional Block Diagram and Terminal List" section, and is added the slope compensation signal to create the target voltage, V_{SC}, in figure 7-9. V_{SC} is fed to the negative input of FB comparator.

The peak detection signal, V_{R1}, converted from Drain current, I_D, with R_{OCP} is fed to the positive input of FB comparator.

The control circuit performs to decrease the peak current of I_D so that V_{R1} comes close to V_{SC}.

And this control prevents the output voltage from increasing.

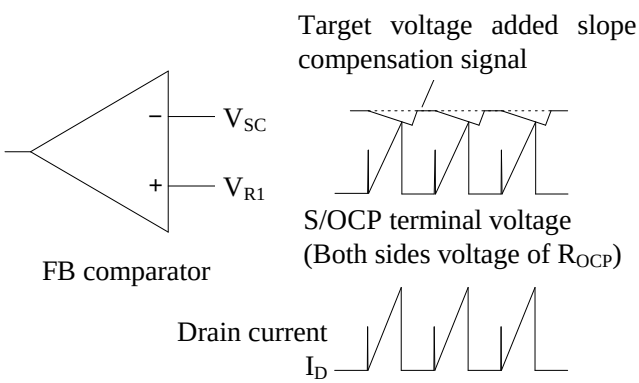


Figure 7-9 Drain current, I_D, and FB comparator in steady operation

When load conditions become bigger, the control circuit performs reverse operations to the former, and increases the peak current of I_D so that V_{R1} comes close to V_{SC}.

And this control prevents the output voltage from decreasing.

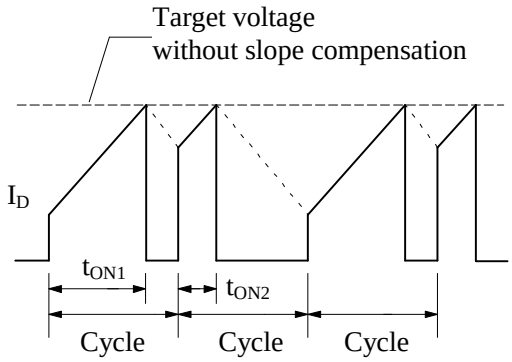


Figure 7-10 Drain current waveform in subharmonic oscillation

Generally, in the current-mode control method, some subharmonic oscillations shown in figure 7-10 occur theoretically. It is called the subharmonic phenomenon.

When the drain current waveform becomes a trapezoid in continuous operating mode, the ON-duty cycle can not become stable in each cycle, and thus subharmonic oscillations occur in multiples of the fundamental operating frequency, according to the initial value of drain current, even if the peak current level set by the target voltage is constant.

In order to avoid this, the IC incorporates Slope Compensation Function.

Because the target voltage, V_{SC}, in figure 7-9 is added the down-slope compensation signal, the wider the ON-duty cycle becomes, the smaller the peak drain current becomes to suppress subharmonic oscillations..

Even if subharmonic oscillations occur when the IC has some excess supply being out of feedback control, such as during startup and load shorted, this does not affect performance during normal operation.

In the current-mode control method, FB comparator and/or OCP comparator may respond to the surge voltage resulting from the drain surge current in turning on a power MOSFET, and may turn off the power MOSFET irregularly.

Leading Edge Blanking, t_{BW}= 350ns(TYP), is built-in to prevent OCP comparator from malfunction caused by surge voltage in turning on the power MOSFET.

7.3 Soft-Start Function

Figure 7-11 shows the operation image waveform at startup.

Soft-Start Function is built-in to reduce stress of voltage and current of a power MOSFET, secondary rectifiers and so on. The period of Soft-Start Function is fixed to 7ms internally. In this period, OCP threshold voltages increase with five steps.

It is necessary to check or adjust the followings at startup;

- V_{CC} terminal voltage should be more than $V_{CC(OFF)}$,
- The period when FB/OLP terminal voltage increases to OLP threshold voltage, $V_{FB(OLP)}$= 8.1V(TYP), should be shorter enough than OLP delay time, t_{OLP}=68ms(TYP).

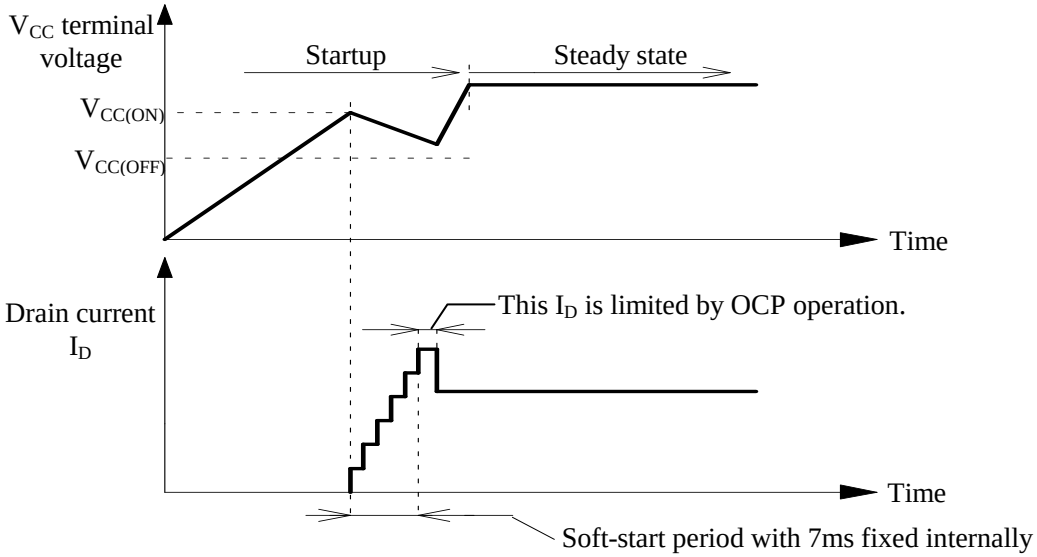


Figure 7-11 Operation image waveform at startup

7.4 Automatic Standby Mode Function

Automatic Standby Mode is activated automatically when the drain current, I_D, reduces in light load condition and S/OCP terminal voltage decreases to less than 15% to 20% of the voltage of the maximum drain current (it is overcurrent protection state). And this operation becomes the burst-oscillation as shown in figure 7-12.

The burst-oscillation reduces switching losses and improves power supply efficiency because there are interval periods.

Generally the frequency of the burst-oscillation is set at just a few kHz, such frequencies are in the range of human hearing, to improve the efficiency in light load condition, and thus it may cause audible noises from a transformer.

Because the IC series limit the drain current to less than 15% to 20% during the burst-oscillation, audible noises are well-suppressed.

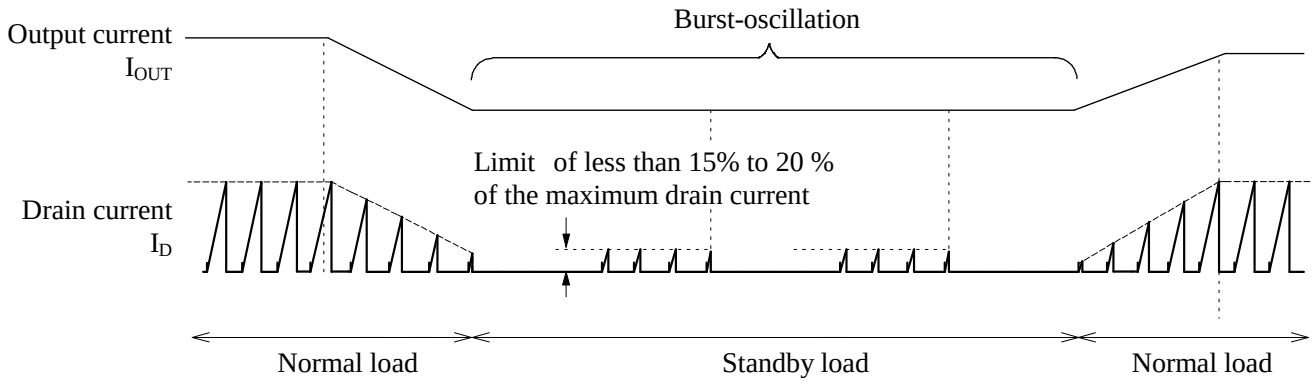


Figure 7-12 Automatic standby mode operation

During the transition to the burst-oscillation, if V_{CC} terminal voltage decreases to $V_{CC(BIAS)}$= 9.5V(TYP), Bias Assist Function is activated and stabilizes the standby mode operation, because $I_{STARTUP}$ is provided to V_{CC} terminal so that V_{CC} terminal voltage does not decrease to $V_{CC(OFF)}$.

However, if Bias Assist Function is always activated during standby mode, the power loss increases. Therefore V_{CC} terminal voltage should be more than $V_{CC(BIAS)}$, for example, by adjusting the turns ratio between auxiliary winding and secondary winding and/or R2 in figure 7-5.

7.5 Random Switching Function

The IC modulates its switching frequency randomly within △f= 5kHz of Average Switching Frequency, $f_{OSC(AVE)}$ = 67kHz(TYP), by superposing the modulating frequency on $f_{OSC(AVE)}$ in normal operation.

The conduction noise with this function is smaller than that without this function, and this function simplifies noise filtering of the input lines of power supply.

7.6 Latch Function

The latch function stops switching operation and a protection state is latched when OVP and/or TSD protection functions activate.

After stopping switching operation with latch mode, V_{CC} terminal voltage drops. When V_{CC} terminal voltage decreases to $V_{CC(BIAS)}$= 9.5V(TYP), Bias Assist Function is activated to prevent V_{CC} terminal voltage from reaching $V_{CC(OFF)}$, and then the latch function is maintained.

Releasing the latch function can be done when V_{CC} terminal voltage reaches $V_{CC(OFF)}$ or less by simply turning off the AC input.

7.7 Overcurrent Protection Function (OCP)

Overcurrent Protection Function (OCP) detects each drain peak current level of a power MOSFET on pulse-by-pulse basis, and limits the output power. This function incorporates AC Input Compensation Function to reduce OCP point variation for AC input voltage, without any additional external components.

This OCP function detects the drain current by a current detection resistor, R_{OCP}, which is connected between S/OCP terminal and GND terminal. When the voltage drop on both sides of R_{OCP} increases to internal OCP threshold voltage, the power MOSFET is turned off.

PWM control ICs usually have some detection delay time on OCP detection. The steeper the slope of actual drain current in high AC input voltage is, the longer the actual detection point is, compared with internal OCP threshold voltage. And thus the actual OCP point limited the output current usually has some variation depending on AC input voltage as shown in figure 7-13.

The IC incorporates a built-in Input Compensation Function that superposes a signal with a defined slope to the detection signal on S/OCP terminal as shown in figure 7-14.

When AC input voltage is lower and the ON-duty cycle is wider, the OCP compensation level increases. And thus the OCP point in low AC input voltage increases to minimize the difference of OCP points between low AC input voltage and high AC input voltage.

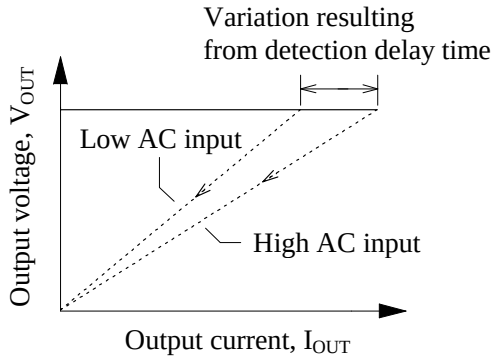


Figure 7-13 Output current at OCP without input compensation

Because the compensation signal level is designed to depend upon ON Time, OCP threshold voltage after compensation, $V_{OCP(ONTime)}$, is calculated as follows.

$$V_{OCP(ONTime)}(V) = V_{OCP(L)}(V) + D_{PC}(mV/\mu s) \times ONTime(\mu s) \quad \text{------(2)}$$

where D_{PC} is OCP compensation coefficient shown in Electrical Characteristics table.

However, in the ON Time when ON-duty cycle becomes 36% or more, OCP threshold voltage after compensation remains $V_{OCP(H)}$= 0.88V(TYP) constantly.

For example, when AC input voltage is 85VAC and the transformer is designed to become ON-duty cycle of 36% on maximum load condition, ON Time becomes about 5.6μs. And thus OCP threshold after compensation, $V_{OCP(5.6\mu s)}$, becomes about 0.88V, resulting from the equation (2).

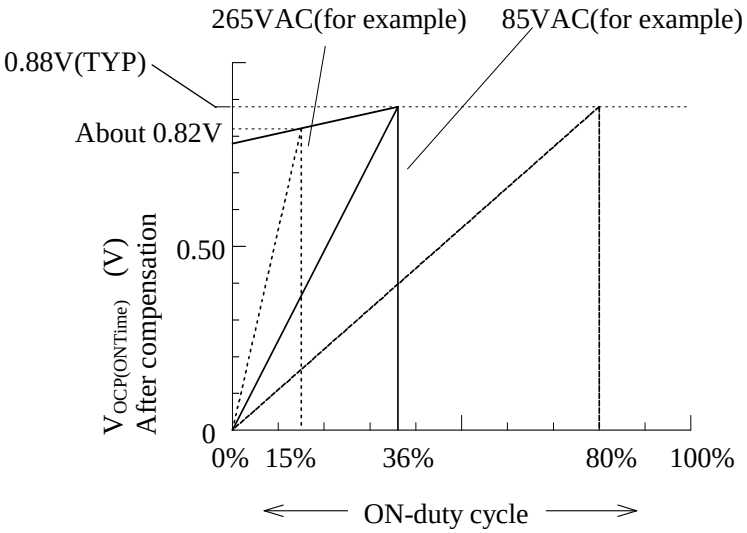


Figure 7-14 Relationship of ON-duty cycle and $V_{OCP(ONTime)}$ at $f_{OSC(AVE)}$= 67kHz(TYP)

7.8 Overvoltage Protection Function (OVP)

When a voltage between V_{CC} terminal and GND terminal increases to $V_{CC(OVP)}$= 29V(TYP) or more, OVP Function is activated and stops switching operation by Latch Function.

When the auxiliary winding provides V_{CC} terminal voltage, OVP Function is available to detect the overvoltage of the output voltage, such as the detection circuit for output control is open in the secondary side, because V_{CC} terminal voltage is proportional to the output voltage.

The output voltage of the secondary side at OVP operation, $V_{OUT(OVP)}$, is calculated approximately as follows.

$$V_{OUT(OVP)} \fallingdotseq \frac{V_{OUT} \text{ terminal voltage at normal operation}}{V_{CC} \text{ terminal voltage at normal operation}} \times 29\text{V}(TYP) \quad \text{-----(3)}$$

7.9 Overload Protection Function (OLP)

When the drain peak current is limited by OCP operation, the output voltage, V_{OUT}, decreases and the feedback current from the secondary photo-coupler becomes zero. As a result, FB/OLP terminal voltage increases.

When FB/OLP terminal voltage increases to $V_{FB(OLP)}$= 8.1V(TYP) or more and remains for OLP delay time, t_{OLP}= 68ms or more, OLP function is activated, stops switching operation and reduce stress of a power MOSFET, secondary rectifiers and so on.

Each waveform on OLP Function is shown in figure 7-15.

When OLP Function is activated, Bias Assist Function is disabled and thus V_{CC} terminal voltage decreases to $V_{CC(OFF)}$= 8.1V(TYP). After that, the IC reverts to the initial state by UVLO (Undervoltage Lockout) circuit, and the IC starts operation when V_{CC} terminal voltage increases to $V_{CC(ON)}$= 15.3V(TYP).

And thus the intermittent operation by UVLO is repeated. This operation reduces power dissipation because the switching period in this intermittent operation is short.

When such an abnormal condition is removed, the IC returns to normal operation automatically.

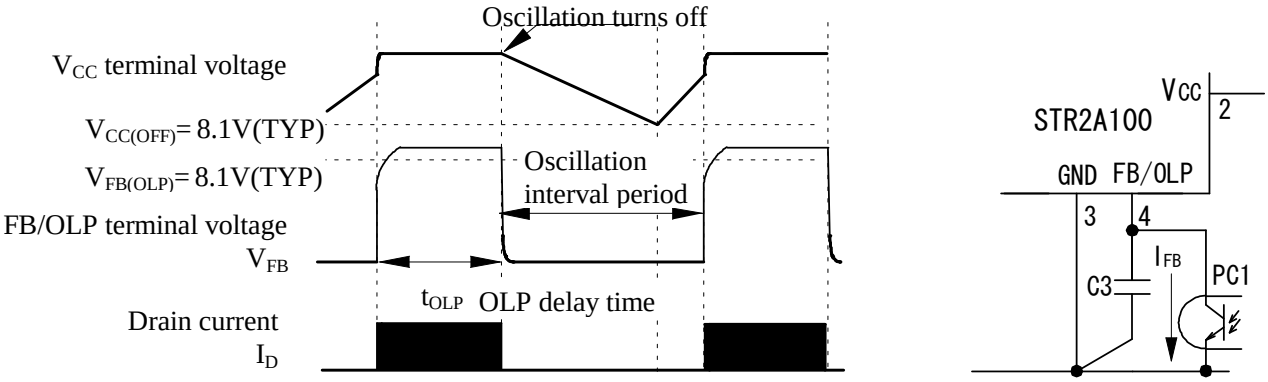


Figure 7-15 Each waveform on OLP operation and FB/OLP peripheral circuit

7.10 Thermal Shutdown Protection Function (TSD)

When the temperature of the control part (MIC) of the IC increases to $T_{j(TSD)}$= 135°C(MIN) or more, Thermal Shutdown Protection Function is activated and stops switching operation by Latch Function.

8. Design Notes

8.1 Peripheral Components

Take care to use properly rating and proper type of components.

- Input and output electrolytic capacitors
  Apply proper design margin to ripple current, voltage and temperature rise. Use of high ripple current and low impedance types, designed for switch mode power supplies, is recommended.
- Transformer
  Apply proper design margin to temperature rise by core loss and copper loss.
  Because switching currents contain high frequency currents, the some temperature rise may result from the skin-effect. If the influence of skin-effect can not be minimized, choose suitable wire gauge in consideration of RMS current in the current density of about 3 to 4A/mm^2.
  If measures to further reduce temperature is still necessary, use paralleled wires or litz wires to increase surface area of wires.
- Current detection resistor, R_{OCP}
  A high frequency switching current flows to R_{OCP}, and may cause poor operation if a high inductance resistor is used. Choose a low inductance and surge-proof type.

8.2 Phase Compensation

A typical error amplifier circuit with a shunt regulator (Z2) of secondary side is shown in figure 8-1.
C7 is recommended about 0.047 to 0.47μF, and should be adjusted on actual operation.
C3 between FB/OLP terminal and GND terminal shown in figure 8-2 is for high frequency noise reduction and phase compensation. C3 is recommended about 470pF to 0.01μF.
C3 should be connected close to FB/OLP terminal and GND terminal, and should be adjusted on actual operation.

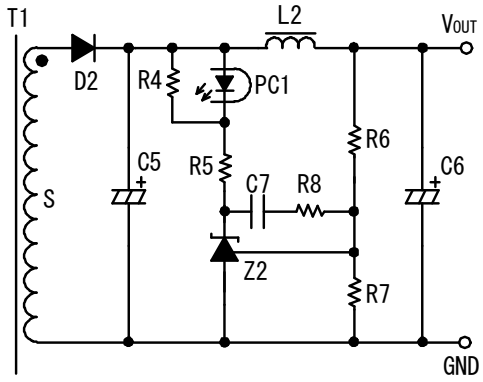


Figure 8-1 Peripheral circuit around secondary shunt regulator

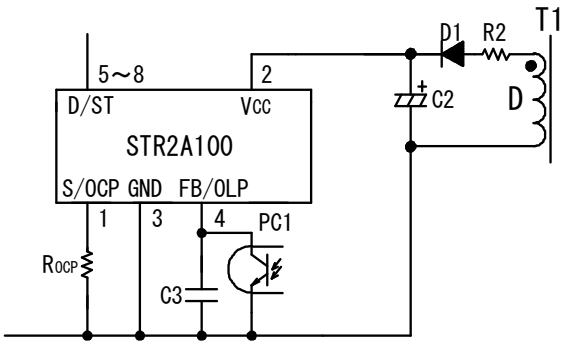


Figure 8-2 FB/OLP peripheral circuit

8.3 EMI Measure of the secondary rectifier

A general EMI measure of the secondary rectifier is shown in figure 8-3.

A snubber capacitor, C_{di}, in parallel to the secondary rectifier, is for noise reduction.

If ringing waveforms occur on the drain current, it is recommended to connect a damper resistor, R_{di}, in series to C_{di} as shown in figure 8-4, in order to reduce ringing waveforms, and to stabilize switching operation.

It is necessary to check temperature rise of R_{di} and C_{di}.

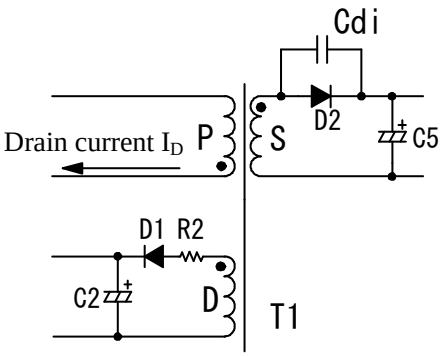


Figure 8-3 Rectifier measure example

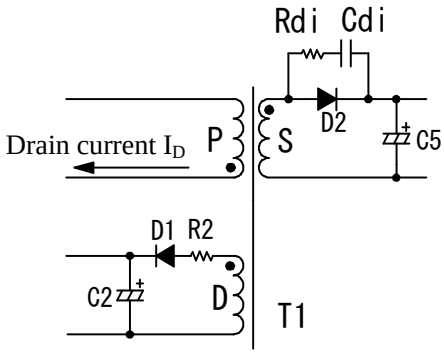


Figure 8-4 Damper resistor example

8.4 PCB trace layout and Component placement

PCB circuit trace design and component layout affect proper functioning during operation. Unless they are proper, mal-function, large noise and large power dissipation may occur.

Circuit loop traces flowing high frequency current, as shown in figure 8-5, should be designed as wide, short and small as possible to reduce trace impedance.

In addition, earth ground traces affect radiation noise, and thus it should be designed as wide and short as possible.

Switching mode power supplies consist of current traces with high frequency and high voltage, and thus trace design and component layout should be done to comply with all safety guidelines.

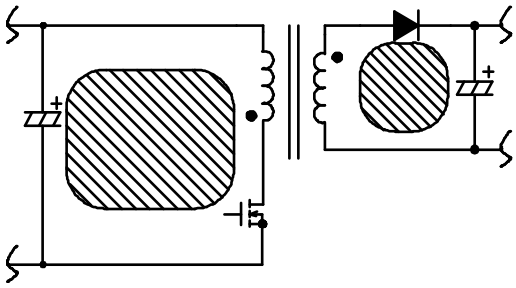


Figure 8-5 High frequency current loops (hatched areas)

Furthermore, because an integrated power MOSFET is being used as the switching device, take account of the positive thermal coefficient of $R_{DS(ON)}$ for thermal design.

Figure 8-6 shows a circuit layout design example.

(1) S/OCP Trace Layout: S/OCP terminal to R_{OCP} to C1 to T1 (winding P) to D/ST terminal

This is the main trace containing switching currents, and thus it should be as wide and short as possible.

If the trace distance between C1 and the IC is lengthy, an additional capacitor near the IC or the transformer is recommended to reduce impedance of high frequency current loop, and is recommended either electrolytic or film type capacitors, around 0.1μF, in the withstand voltage suitable for an applied maximum voltage.

(2) GND Trace Layout: GND terminal to C2 (negative terminal) and T1 (winding D) to R2 to D1 to C2 (positive terminal) to V_{CC} terminal

This trace also needs to be as wide and short as possible.

If the trace distance between C2 and the IC is lengthy, placing a capacitor around 0.1μF to 1uF (50V) with high frequency property is recommended close to V_{CC} terminal and GND terminal.

(3) R_{OCP} Trace Layout

R_{OCP} should be placed as close as possible to S/OCP terminal. The connection between the power ground of main trace and the control circuit ground should be connected by a single point (“A” mark in figure 8-6) to remove common impedance, and to avoid interference of the control circuit resulting from switching currents.

Figure 8-6 also shows a circuit layout design example for the secondary side.

(1) Secondary Smoothing Circuit Trace Layout: T1 (winding S) to D2 to C5

This trace should be as wide and short as possible.

If the loop length is lengthy, surge voltage may increase at turning off a power MOSFET because leakage inductance resulting from the long loop may increase.

Taking the secondary trace layout into account is available to increase the voltage strength margin of the power MOSFET, and to reduce stress and power dissipation of the clamp snubber circuit.

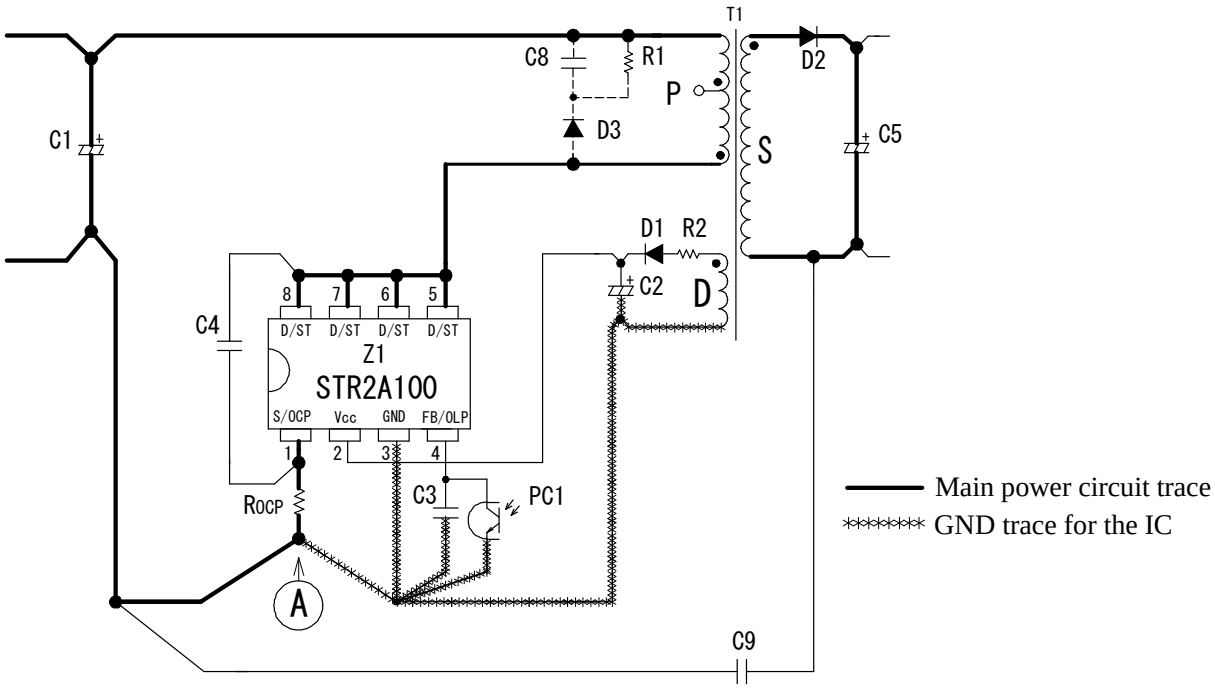


Figure 8-6 Peripheral circuit example around the IC