



TS4995

1.2W fully differential audio power amplifier with selectable standby and 6db fixed gain

Features

- Differential inputs
- 90dB PSRR @ 217Hz with grounded inputs
- Operating from $V_{CC} = 2.5V$ to $5.5V$
- 1.2W rail to rail output power @ $V_{CC}=5V$, THD+N=1%, F=1kHz, with 8Ω load
- 6dB integrated fixed gain
- Ultra-low consumption in standby mode (10nA)
- Selectable standby mode (active low or active high)
- Ultra-fast startup time: 10ms typ. at $V_{CC}=3.3V$
- Available in 9-bump flip-chip (300mm bump diameter)
- Ultra-low pops&clicks

Description

The TS4995 is an audio power amplifier capable of delivering 1.2W of continuous RMS output power into an 8Ω load at 5V. Thanks to its differential inputs, it exhibits outstanding noise immunity.

An external standby mode control reduces the supply current to less than 10nA. A STBY MODE pin allows the standby pin to be active HIGH or LOW. An internal thermal shutdown protection is also provided, making the device capable of sustaining short-circuits.

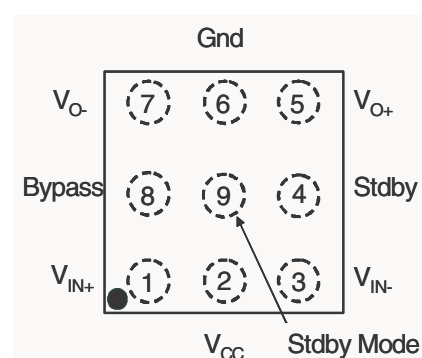
The TS4995 features an internal fixed gain at 6dB which reduces the number of external components on the application board.

Device summary table

Part Number	Temperature Range	Package	Packing	Marking
TS4995EIJT	-40°C to +85°C	Lead free flip-chip9	Tape & Reel	95

TS4995 - Flip-Chip9

Pin connections (top view)



The device is equipped with Common Mode Feedback circuitry allowing outputs to be always biased at $V_{CC}/2$ regardless of the input common mode voltage.

The TS4995 has been designed for high quality audio applications such as mobile phones and requires few external components.

Applications

- Mobile phones (cellular / cordless)
- PDAs
- Laptop / notebook computers
- Portable audio devices

Contents

1	Absolute maximum ratings & operating conditions	3
2	Typical application schematic	4
3	Electrical characteristics	5
4	Application information	16
4.1	Differential configuration principle	16
4.2	Common mode feedback loop limitations	16
4.3	Low frequency response	16
4.4	Power dissipation and efficiency	17
4.5	Decoupling of the circuit	18
4.6	Wake-up Time: TWU	19
4.7	Shutdown time	19
4.8	Pop performance	19
4.9	Single-ended input configuration	19
5	Package mechanical data	21
5.1	9-bump flip-chip package	21
6	Revision history	23

1 Absolute maximum ratings & operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	6	V
V_i	Input voltage ⁽²⁾	G_{ND} to V_{CC}	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient ⁽³⁾	200	°C/W
P_{diss}	Power dissipation	Internally limited	W
ESD	Machine model	200	V
	Human body model	1.5	kV
Latch-up	Latch-up immunity	200	mA
-	Lead temperature (soldering, 10sec)	260	°C

1. All voltage values are measured with respect to the ground pin.

2. The magnitude of input signal must never exceed $V_{CC} + 0.3V$ / $G_{ND} - 0.3V$.

3. Device is protected in case of over temperature by a thermal shutdown activated at 150°C.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.5 to 5.5	V
V_{SM}	Standby Mode Voltage Input:		
	Standby Active LOW Standby Active HIGH	$V_{SM}=G_{ND}$ $V_{SM}=V_{CC}$	V
V_{STB}	Standby Voltage Input:		
	Device ON ($V_{SM}=G_{ND}$) or Device OFF ($V_{SM}=V_{CC}$) Device OFF ($V_{SM}=G_{ND}$) or Device ON ($V_{SM}=V_{CC}$)	$1.5 \leq V_{STB} \leq V_{CC}$ $G_{ND} \leq V_{STB} \leq 0.4$ ⁽¹⁾	V
T_{SD}	Thermal Shutdown Temperature	150	°C
R_L	Load Resistor	≥ 8	Ω
R_{thja}	Thermal Resistance Junction to Ambient	100	°C/W

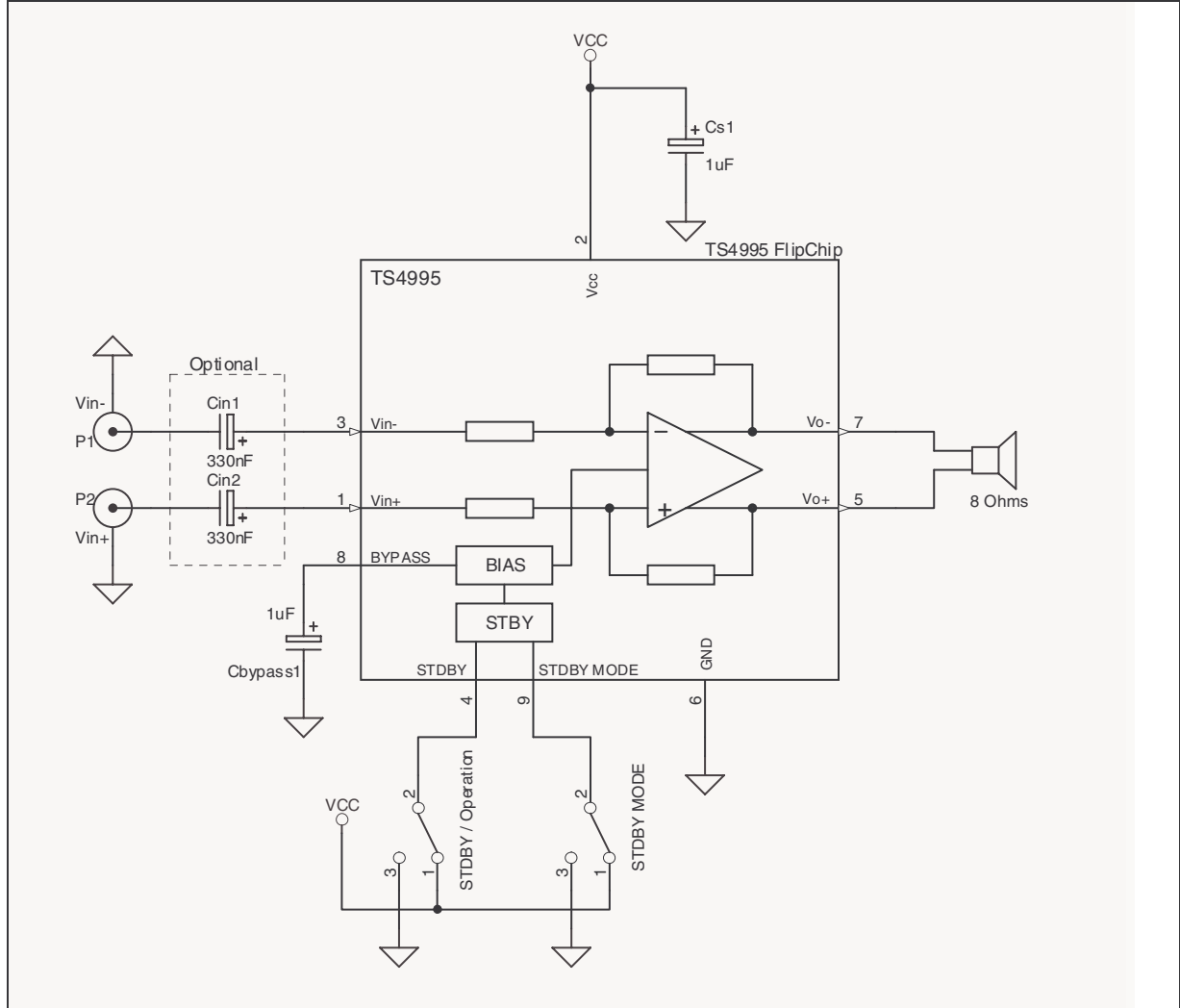
1. The minimum current consumption ($I_{STANDBY}$) is guaranteed when $V_{STB} = G_{ND}$ or V_{CC} (i.e. supply rails) for the whole temperature range.

2 Typical application schematic

Table 3. External components descriptions

Components	Functional description
C_s	Supply Bypass capacitor which provides power supply filtering.
C_b	Bypass capacitor which provides half supply filtering.
C_{in}	Optional input capacitor making a high pass filter together with R_{in} . ($f_{cl} = 1 / (2 \times \pi \times R_{in} \times C_{in})$).

Figure 1. Typical application



3 Electrical characteristics

Table 4. $V_{CC} = +5V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current	No input signal, no load		4	7	mA
$I_{STANDBY}$	Standby Current	No input signal, $V_{stdby} = V_{SM} = G_{ND}$, $R_L = 8\Omega$ No input signal, $V_{stdby} = V_{SM} = V_{CC}$, $R_L = 8\Omega$		10	1000	nA
V_{OO}	Differential Output Offset Voltage	No input signal, $R_L = 8\Omega$		0.1	10	mV
V_{IC}	Input Common Mode Voltage	-	0		4.5	V
P_o	Output Power	THD = 1% Max, $F = 1kHz$, $R_L = 8\Omega$	0.8	1.2		W
THD + N	Total Harmonic Distortion + Noise	$P_o = 850mW$ rms, $20Hz \leq F \leq 20kHz$, $R_L = 8\Omega$		0.5		%
$PSRR_{IG}$	Power Supply Rejection Ratio with Inputs Grounded ⁽¹⁾	$F = 217Hz$, $R = 8\Omega$, $C_{in} = 4.7\mu F$, $C_b = 1\mu F$ $V_{ripple} = 200mV_{PP}$	75 ⁽²⁾	90		dB
CMRR	Common Mode Rejection Ratio	$F = 217Hz$, $R_L = 8\Omega$, $C_{in} = 4.7\mu F$, $C_b = 1\mu F$ $V_{ic} = 200mV_{PP}$		60		dB
SNR	Signal-to-Noise Ratio	A Weighted Filter $R_L = 8\Omega$, THD + N < 0.7%, $20Hz \leq F \leq 20kHz$		100		dB
GBP	Gain Bandwidth Product	$R_L = 8\Omega$		2		MHz
V_N	Output Voltage Noise	20Hz $\leq F \leq 20kHz$, $R_L = 8\Omega$ Unweighted A weighted Unweighted, Standby A weighted, Standby		11 7 3.5 1.5		μV_{RMS}
Z_{in}	Input impedance	-	15	20	25	k Ω
-	Gain mismatch	-	5.5	6	6.5	dB
T_{WU}	Wake-Up Time ⁽³⁾	$C_b = 1\mu F$		15		mS

1. Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. Vripple is the super-imposed sinus signal relative to Vcc.

2. Guaranteed by design and evaluation.

3. Transition time from standby mode to fully operational amplifier.

Table 5. $V_{CC} = +3.3V$ (all electrical values are guaranteed with correlation measurements at 2.6V and 5V), $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current	No input signal, no load		3	7	mA
$I_{STANDBY}$	Standby Current	No input signal, $V_{stdby} = V_{SM} = G_{ND}$, $R_L = 8\Omega$ No input signal, $V_{stdby} = V_{SM} = V_{CC}$, $R_L = 8\Omega$		10	1000	nA
V_{OO}	Differential Output Offset Voltage	No input signal, $R_L = 8\Omega$		0.1	10	mV
V_{IC}	Input Common Mode Voltage	-	0.4		2.3	V
P_o	Output Power	THD = 1% Max, $F = 1kHz$, $R_L = 8\Omega$	300	500		mW
THD + N	Total Harmonic Distortion + Noise	$P_o = 300mW$ rms, $20Hz \leq F \leq 20kHz$, $R_L = 8\Omega$		0.5		%
$PSRR_{IG}$	Power Supply Rejection Ratio with Inputs Grounded ⁽¹⁾	$F = 217Hz$, $R = 8\Omega$, $C_{in} = 4.7\mu F$, $C_b = 1\mu F$ $V_{ripple} = 200mV_{PP}$	75 ⁽²⁾	90		dB
CMRR	Common Mode Rejection Ratio	$F = 217Hz$, $R_L = 8\Omega$, $C_{in} = 4.7\mu F$, $C_b = 1\mu F$ $V_{ic} = 200mV_{PP}$		60		dB
SNR	Signal-to-Noise Ratio	A Weighted Filter $R_L = 8\Omega$, THD + N < 0.7%, $20Hz \leq F \leq 20kHz$		100		dB
GBP	Gain Bandwidth Product	$R_L = 8\Omega$		2		MHz
V_N	Output Voltage Noise	$20Hz \leq F \leq 20kHz$, $R_L = 8\Omega$ Unweighted A weighted Unweighted, Standby A weighted, Standby		11 7 3.5 1.5		μV_{RMS}
Z_{in}	Input impedance	-	15	20	25	k Ω
-	Gain mismatch	-	5.5	6	6.5	dB
T_{WU}	Wake-Up Time ⁽³⁾	$C_b = 1\mu F$		10		mS

1. Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. Vripple is the super-imposed sinus signal relative to V_{CC} .

2. Guaranteed by design and evaluation.

3. Transition time from standby mode to fully operational amplifier.

Table 6. $V_{CC} = +2.6V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current	No input signal, no load		3	7	mA
$I_{STANDBY}$	Standby Current	No input signal, $V_{stdby} = V_{SM} = G_{ND}$, $R_L = 8\Omega$ No input signal, $V_{stdby} = V_{SM} = V_{CC}$, $R_L = 8\Omega$		10	1000	nA
V_{OO}	Differential Output Offset Voltage	No input signal, $R_L = 8\Omega$		0.1	10	mV
V_{IC}	Input Common Mode Voltage	-	0.6		1.5	V
P_o	Output Power	THD = 1% Max, $F = 1kHz$, $R_L = 8\Omega$	200	300		mW
THD + N	Total Harmonic Distortion + Noise	$P_o = 225mW$ rms, $20Hz \leq F \leq 20kHz$, $R_L = 8\Omega$		0.5		%
$PSRR_{IG}$	Power Supply Rejection Ratio with Inputs Grounded ⁽¹⁾	$F = 217Hz$, $R = 8\Omega$, $C_{in} = 4.7\mu F$, $C_b = 1\mu F$ $V_{ripple} = 200mV_{PP}$	75 ⁽²⁾	90		dB
CMRR	Common Mode Rejection Ratio	$F = 217Hz$, $R_L = 8\Omega$, $C_{in} = 4.7\mu F$, $C_b = 1\mu F$ $V_{ic} = 200mV_{PP}$		60		dB
SNR	Signal-to-Noise Ratio	A Weighted Filter $R_L = 8\Omega$, THD + N < 0.7%, $20Hz \leq F \leq 20kHz$		100		dB
GBP	Gain Bandwidth Product	$R_L = 8\Omega$		2		MHz
V_N	Output Voltage Noise	20Hz ≤ F ≤ 20kHz, $R_L = 8\Omega$ Unweighted A weighted Unweighted, Standby A weighted, Standby		11 7 3.5 1.5		μV_{RMS}
Z_{in}	Input impedance	-	15	20	25	k Ω
-	Gain mismatch	-	5.5	6	6.5	dB
T_{WU}	Wake-Up Time ⁽³⁾	$C_b = 1\mu F$		10		mS

1. Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. Vripple is the super-imposed sinus signal relative to Vcc.

2. Guaranteed by design and evaluation.

3. Transition time from standby mode to fully operational amplifier.

Figure 2. THD+N vs. output power

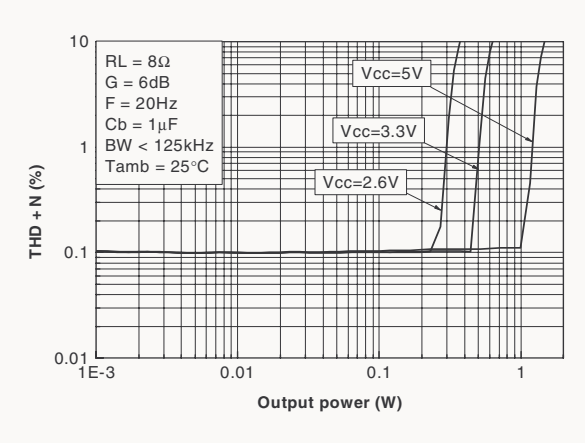


Figure 3. THD+N vs. output power

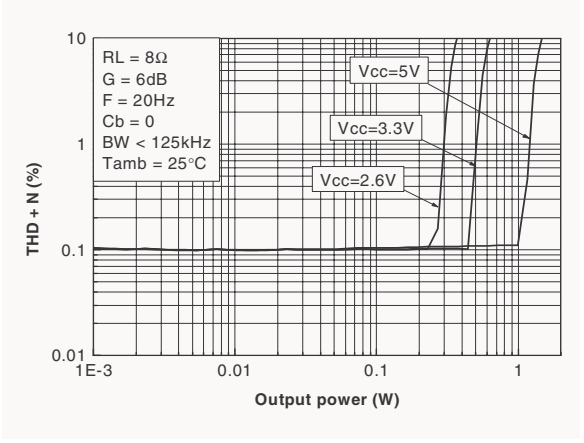


Figure 4. THD+N vs. output power

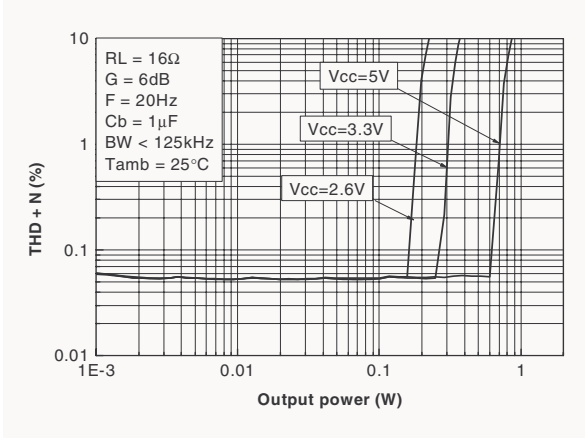


Figure 5. THD+N vs. output power

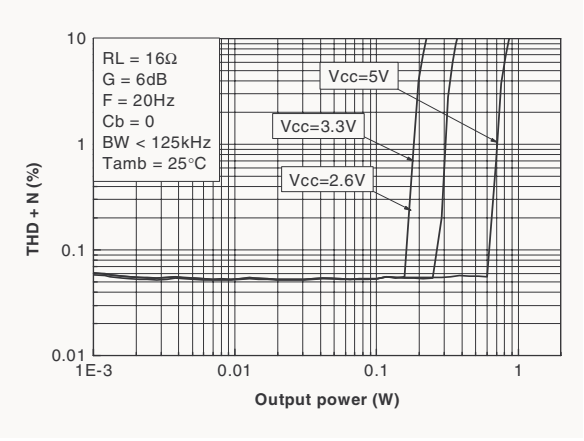


Figure 6. THD+N vs. output power

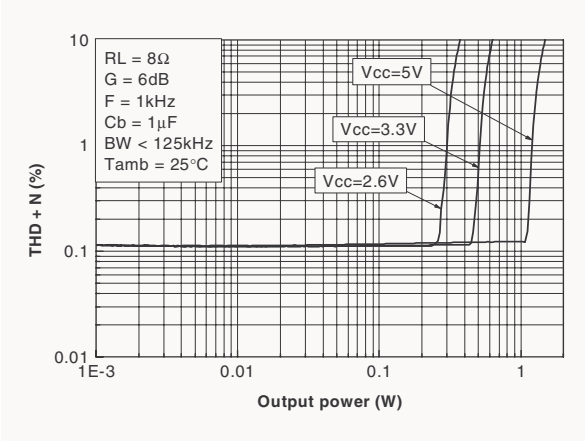


Figure 7. THD+N vs. output power

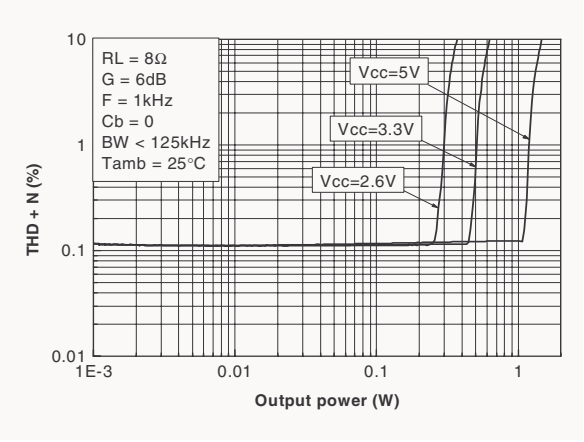


Figure 8. THD+N vs. output power

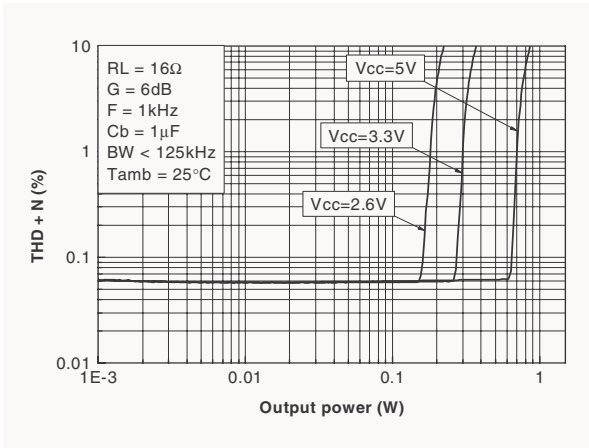


Figure 9. THD+N vs. output power

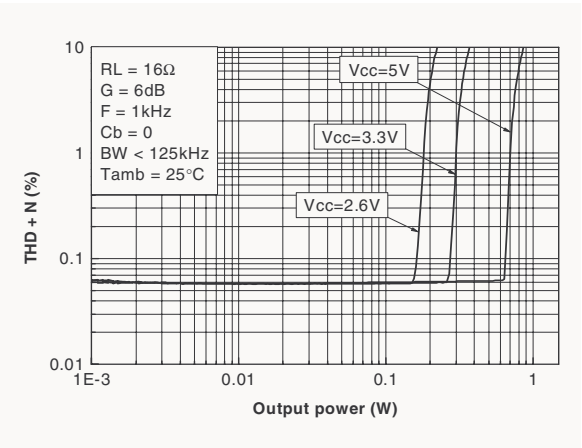


Figure 10. THD+N vs. output power

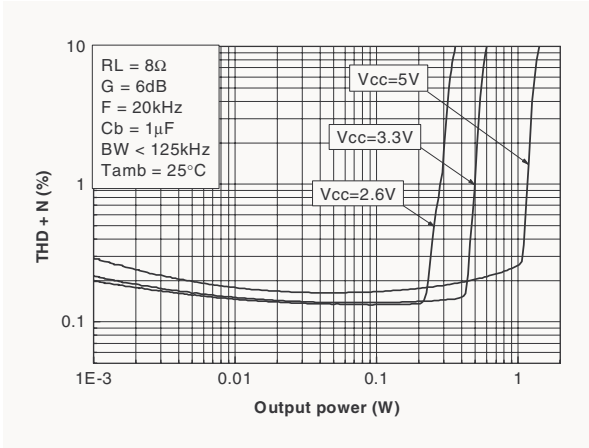


Figure 11. THD+N vs. output power

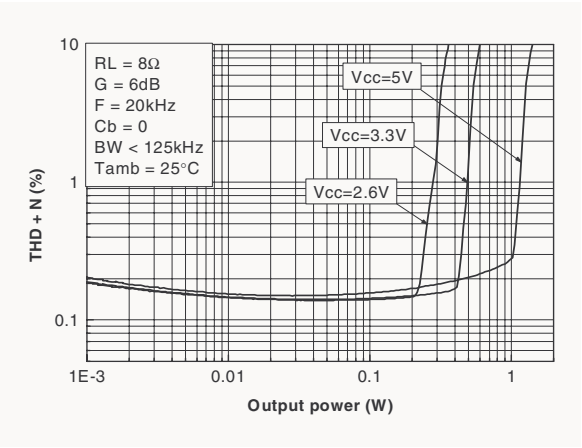


Figure 12. THD+N vs. output power

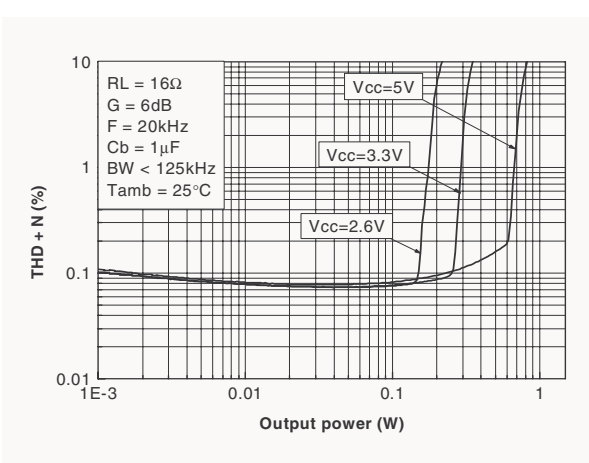


Figure 13. THD+N vs. output power

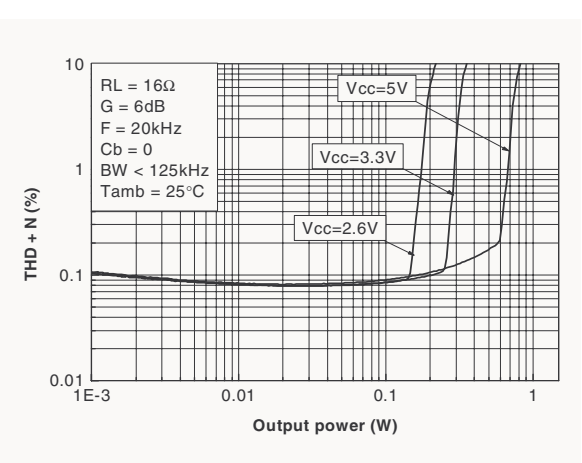


Figure 14. THD+N vs. frequency

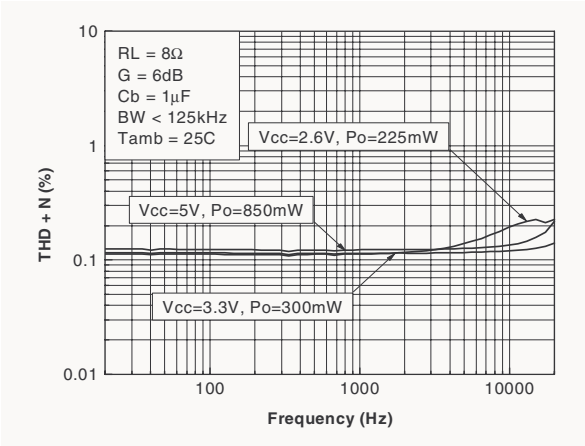


Figure 15. THD+N vs. frequency

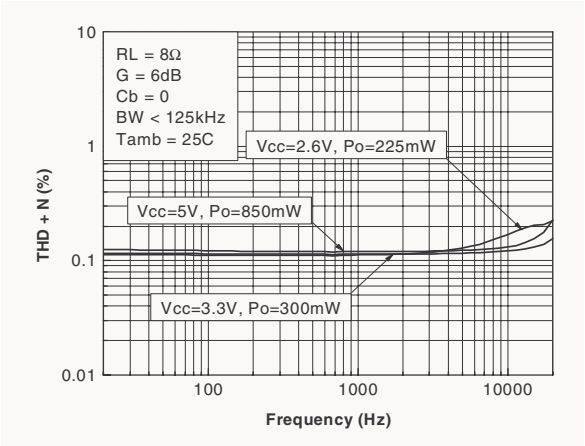


Figure 16. THD+N vs. frequency

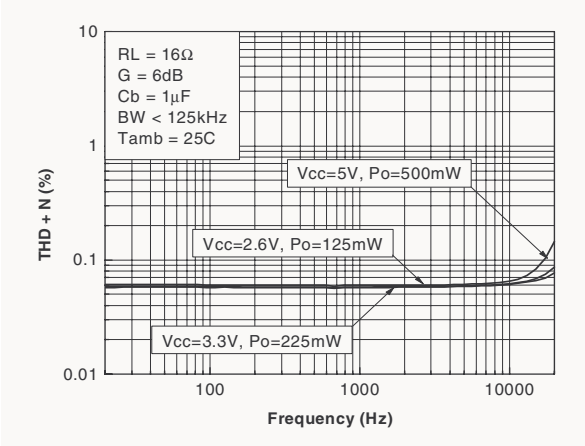


Figure 17. THD+N vs. frequency

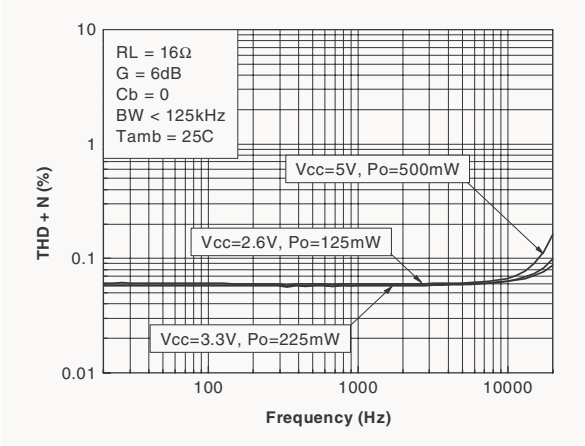


Figure 18. Output power vs. power supply voltage

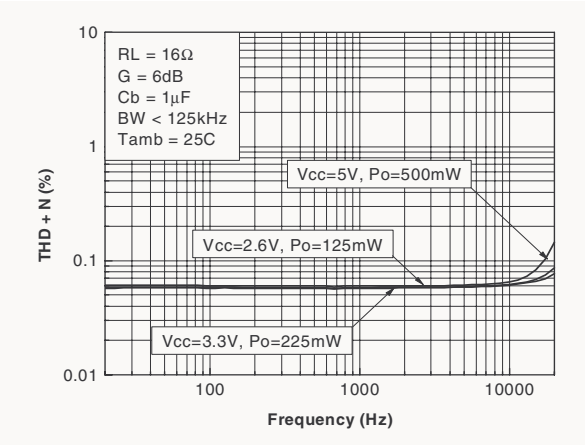


Figure 19. Output power vs. power supply voltage

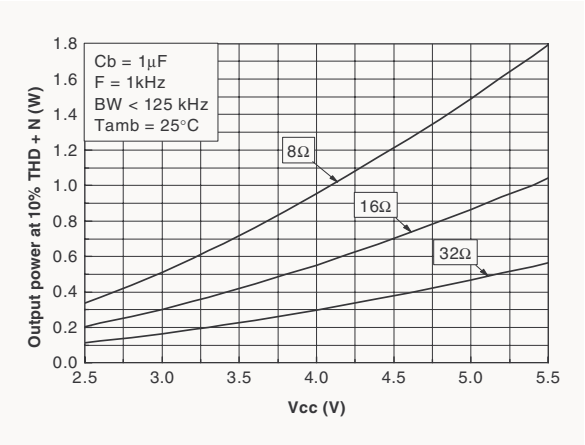


Figure 20. Output power vs. load resistance

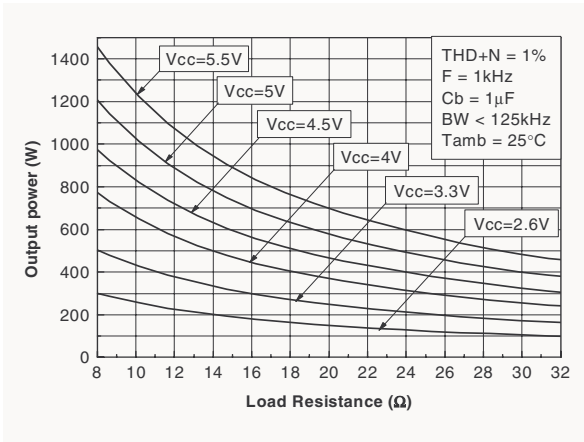


Figure 21. Power dissipation vs. output power

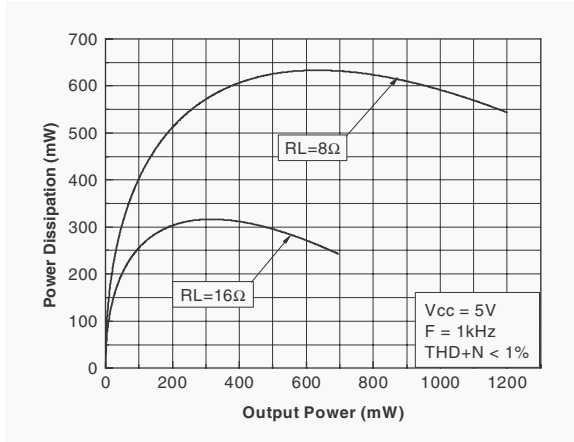


Figure 22. Power dissipation vs. output power

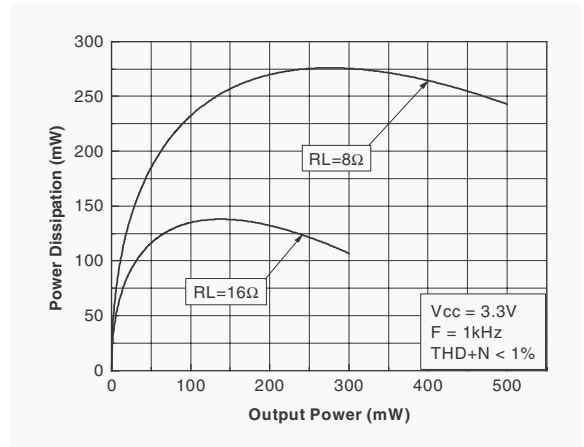


Figure 23. Power dissipation vs. output power

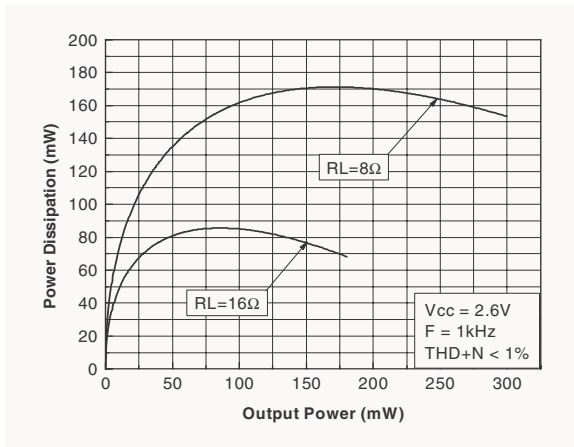


Figure 24. PSSR vs. frequency

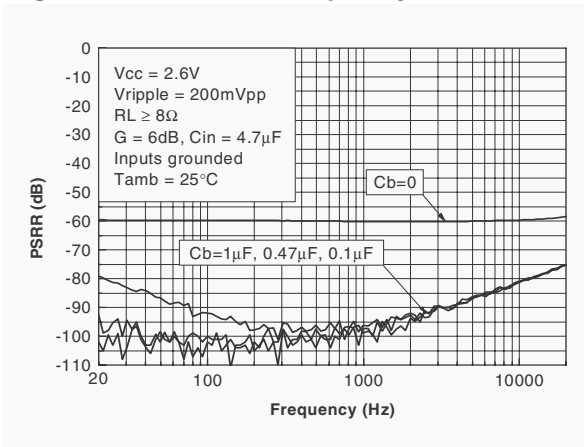


Figure 25. PSSR vs. frequency

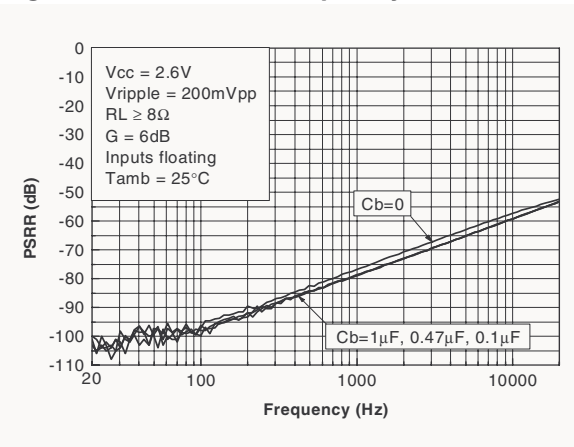


Figure 26. PSSR vs. frequency

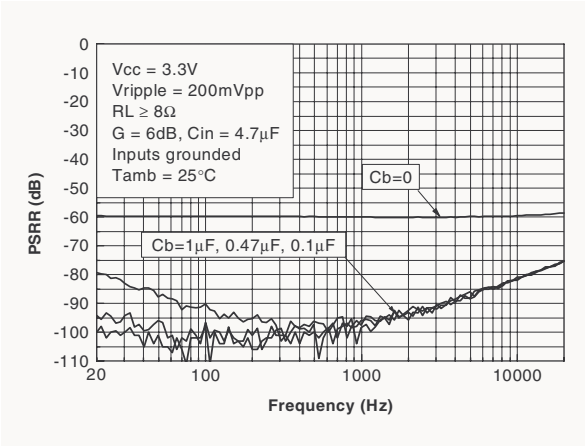


Figure 27. PSSR vs. frequency

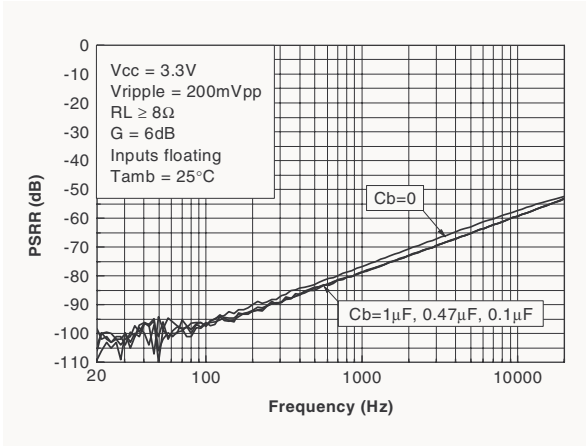


Figure 28. PSSR vs. frequency

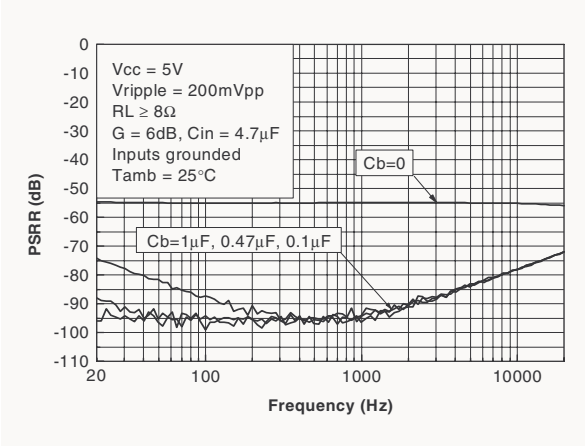


Figure 29. PSSR vs. frequency

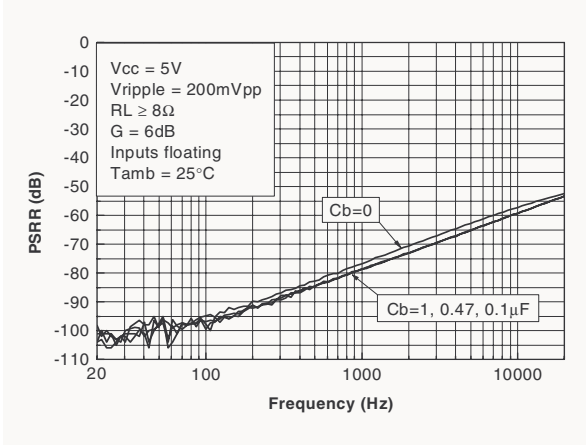


Figure 30. PSSR vs. common mode input voltage

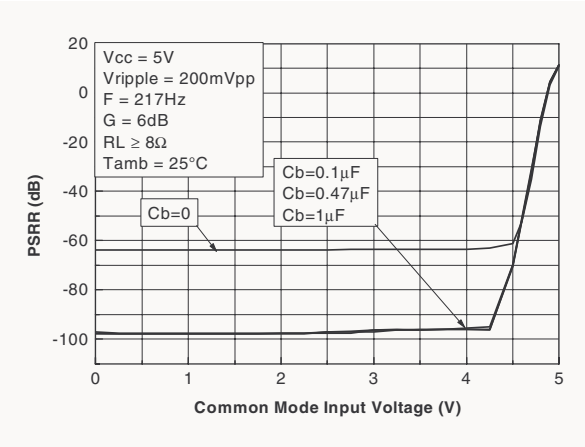


Figure 31. PSSR vs. common mode input voltage

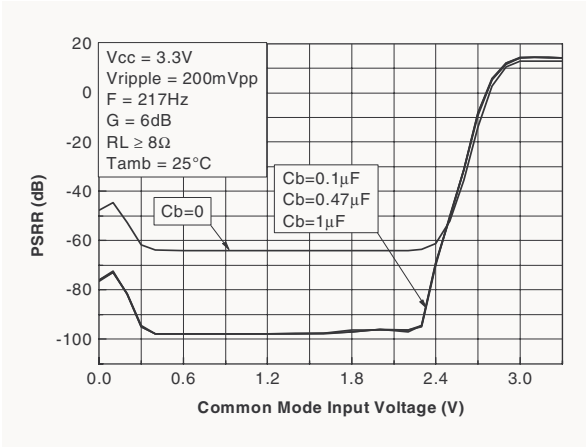


Figure 32. PSSR vs. common mode input voltage

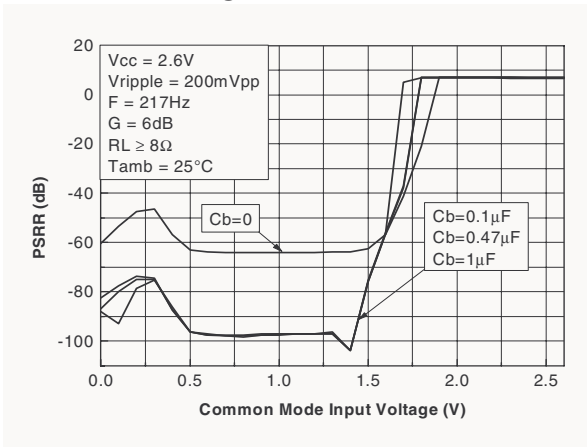


Figure 33. CMRR vs. frequency

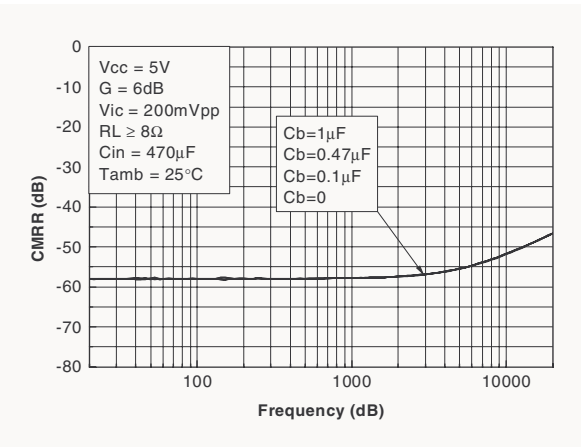


Figure 34. CMRR vs. frequency

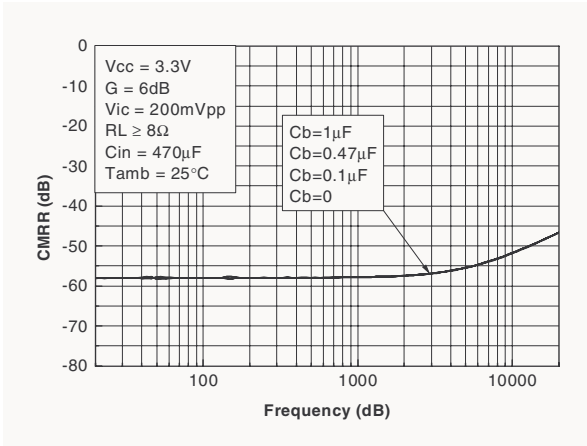


Figure 35. CMRR vs. frequency

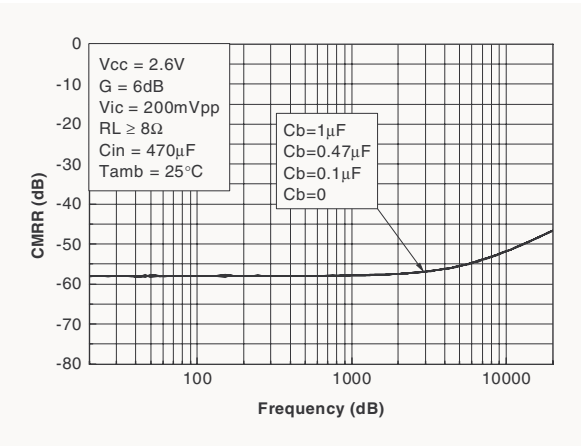


Figure 36. CMRR vs. common mode input voltage

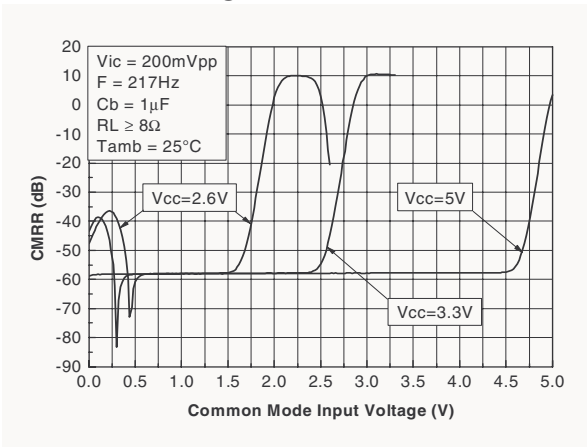


Figure 37. CMRR vs. common mode input voltage

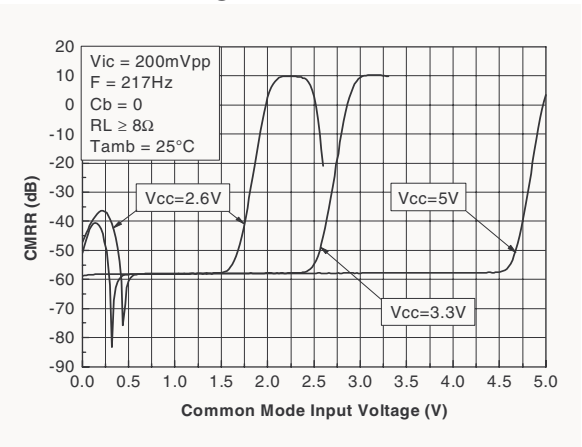


Figure 38. Current consumption vs. power supply voltage

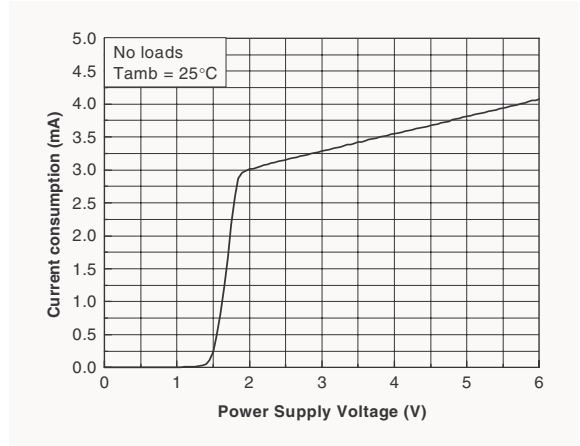


Figure 39. Differential DC output voltage vs. common mode input voltage

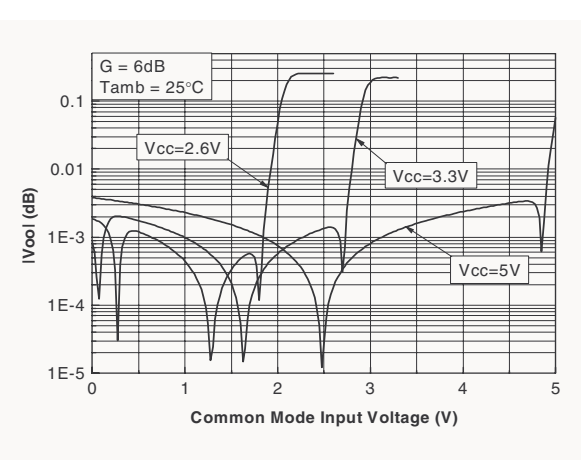


Figure 40. Current consumption vs. standby voltage

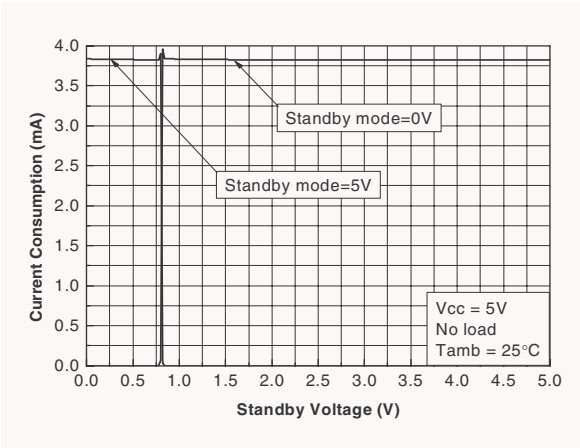


Figure 41. Current consumption vs. standby voltage

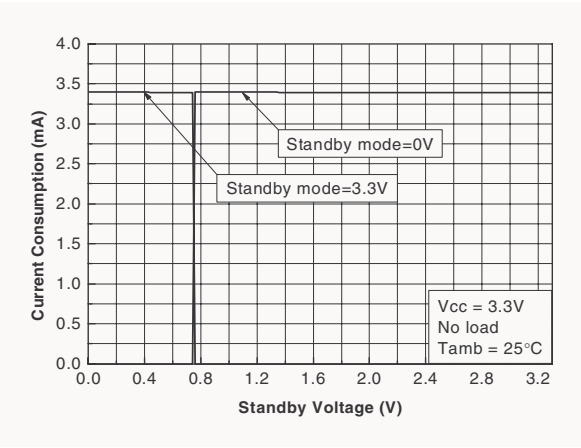


Figure 42. Current consumption vs. standby voltage

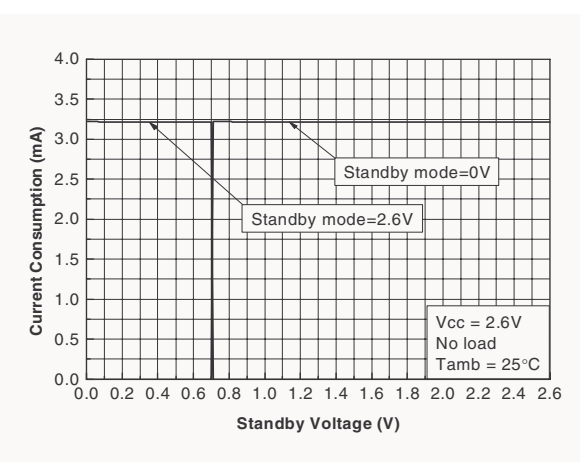


Figure 43. Frequency response

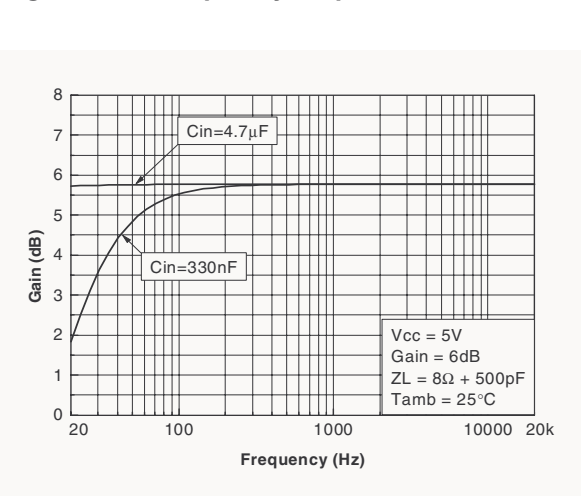


Figure 44. Frequency response

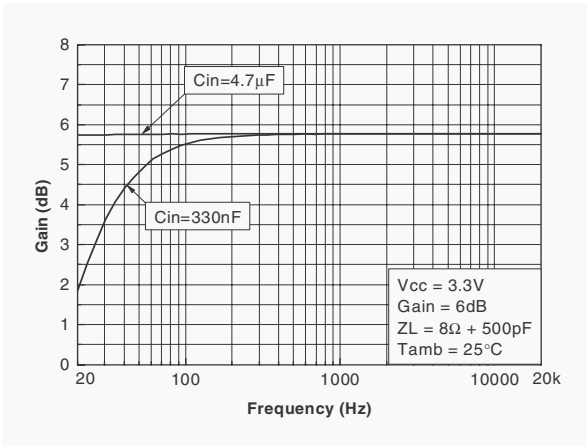


Figure 45. Frequency response

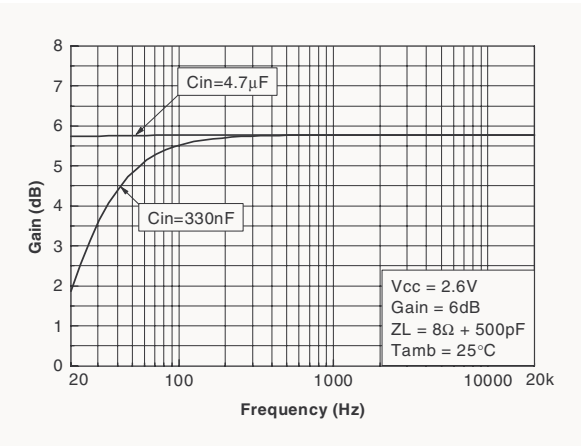


Figure 46. SNR vs. power supply voltage with unweighted filter

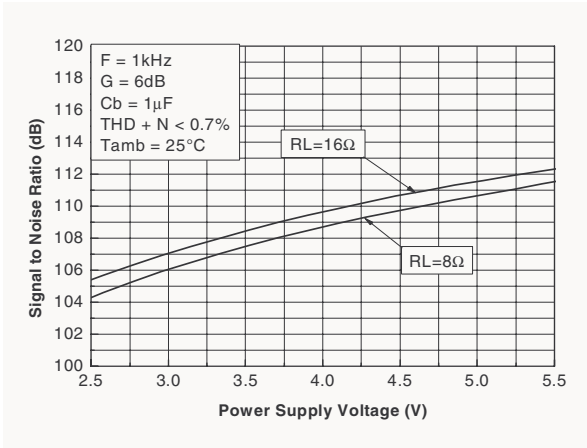


Figure 47. SNR vs. power supply voltage with A-weighted filter

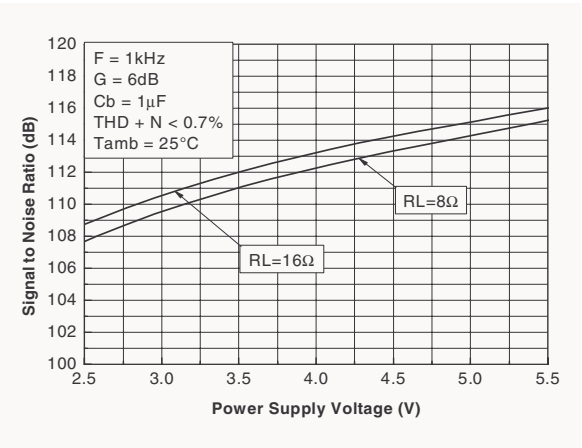
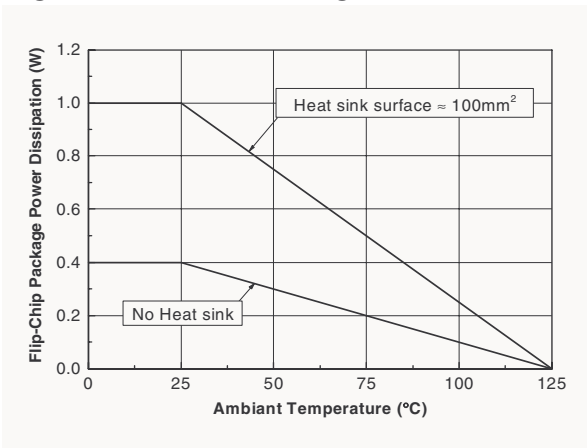


Figure 48. Power derating curves



4 Application information

4.1 Differential configuration principle

The TS4995 is a monolithic full-differential input/ output power amplifier with fixed +6 dB gain. The TS4995 also includes a common mode feedback loop that controls the output bias value to average it at $V_{CC}/2$ for any DC common mode input voltage. This allows maximum output voltage swing, and therefore, maximize the output power. Moreover, as the load is connected differentially instead of single-ended, output power is four times higher for the same power supply voltage.

The **advantages** of a full-differential amplifier are:

- very high PSRR (Power Supply Rejection Ratio),
- high common mode noise rejection,
- virtually no pops&clicks without additional circuitry, giving a faster start-up time compared to conventional single-ended input amplifiers,
- easier interfacing with differential output audio DAC,
- no input coupling capacitors required thanks to common mode feedback loop.

In theory, the filtering of the internal bias by an external bypass capacitor is not necessary. However to reach maximum performance in all tolerance situations, it is recommended to keep this option.

4.2 Common mode feedback loop limitations

As explained previously, the common mode feedback loop allows the output DC bias voltage to be averaged at $V_{CC}/2$ for any DC common mode bias input voltage.

Due to VIC limitation of the input stage (see [Table 4 on page 5](#)), the common mode feedback loop can ensure its role only within defined range.

4.3 Low frequency response

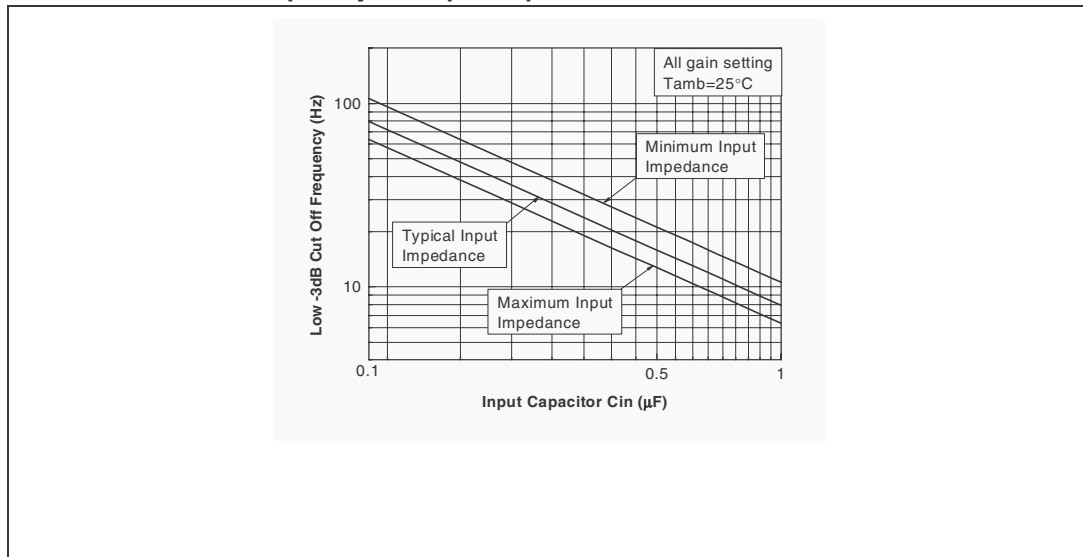
The input coupling capacitors block the input signal DC part at the amplifier inputs. C_{in} and R_{in} form a first-order high pass filter with -3 dB cut-off frequency.

$$F_{CL} = \frac{1}{2 \times \pi \times R_{in} \times C_{in}} \quad (\text{Hz})$$

Note: The Input impedance for the TS4995 is typically 20 k Ω and there is tolerance around this value.

From [Figure 49](#), one can easily establish the C_{in} value required for a -3 dB cut-off frequency.

Figure 49. -3dB lower cut-off frequency vs. input capacitance



4.4 Power dissipation and efficiency

Assumptions:

- load voltage and current are sinusoidal (V_{out} and I_{out})
- supply voltage is a pure DC source (V_{CC})

Regarding the load we have:

$$V_{out} = V_{PEAK} \sin \omega t \text{ (V)}$$

and

$$I_{out} = \frac{V_{out}}{R_L} \text{ (A)}$$

and

$$P_{out} = \frac{V_{PEAK}^2}{2R_L} \text{ (W)}$$

Therefore, the average current delivered by the supply voltage is:

$$I_{CC\,AVG} = 2 \frac{V_{PEAK}}{\pi R_L} \text{ (A)}$$

The power delivered by the supply voltage is:

$$P_{supply} = V_{CC} I_{CC\,AVG} \text{ (W)}$$

Then, the **power dissipated by each amplifier** is

$$P_{diss} = P_{supply} - P_{out} \text{ (W)}$$

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}} \sqrt{P_{out}} - P_{out}$$

and the maximum value is obtained when:

$$\frac{\partial P_{\text{diss}}}{\partial P_{\text{out}}} = 0$$

and its value is:

$$P_{\text{dissmax}} = \frac{2V_{\text{CC}}^2}{\pi^2 R_L} \text{ (W)}$$

Note: This maximum value is only dependent on power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply

$$\eta = \frac{P_{\text{out}}}{P_{\text{supply}}} = \frac{\pi V_{\text{PEAK}}}{4V_{\text{CC}}}$$

The maximum theoretical value is reached when $V_{\text{peak}} = V_{\text{CC}}$, so

$$\frac{\pi}{4} = 78.5\%$$

The maximum die temperature allowable for the TS4995 is 125°C. However, in case of overheating, a thermal shutdown set to 150°C, puts the TS4995 in standby until the temperature of the die is reduced by about 5°C.

To calculate the maximum ambient temperature T_{AMB} allowable, we need to know:

- power supply voltage value, V_{CC}
- load resistor value, R_L
- the package type, R_{THJA}

Example: $V_{\text{CC}}=5\text{V}$, $R_L=8\Omega$, $R_{\text{THJA}}\text{Flip-Chip}=100^\circ\text{C/W}$ (100mm² copper heatsink).

We calculate $P_{\text{dissmax}} = 633\text{mW}$.

with

$$T_{\text{AMB}} = 125^\circ\text{C} - R_{\text{THJA}} \times P_{\text{diss}} \quad (^\circ\text{C})$$

$$T_{\text{AMB}} = 125 - 100 \times 0.633 = 61.7^\circ\text{C}$$

4.5 Decoupling of the circuit

Two capacitors are needed to correctly bypass the TS4995: a power supply bypass capacitor C_S and a bias voltage bypass capacitor C_B .

Capacitor C_S has particular influence on THD+N at high frequency (above 7kHz) and an indirect influence on power supply disturbances. With a value for C_S of 1μF, one can expect THD+N performance similar to that shown in the datasheet.

In the high frequency region, if C_S is lower than 1μF, then THD+N increases and disturbances on the power supply rail are less filtered.

On the other hand, if C_S is larger than 1μF, then those disturbances on the power supply rail are more filtered.

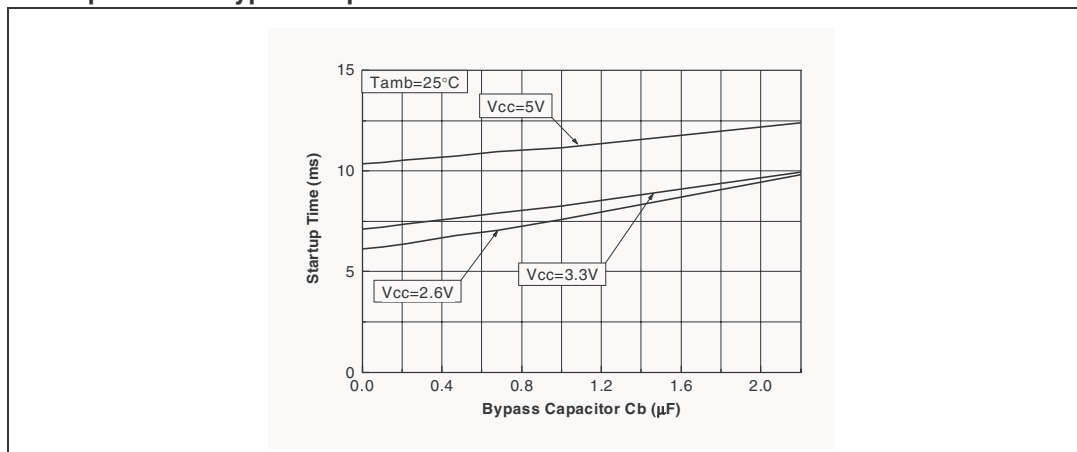
Capacitor C_B has an influence on THD+N at lower frequencies, but also impacts PSRR performance (with grounded input and in the lower frequency region).

4.6 Wake-up Time: T_{WU}

When the standby is released to put the device ON, the bypass capacitor C_b will not be charged immediately. As C_b is directly linked to the bias of the amplifier, the bias will not work properly until the C_b voltage is correct. The time to reach this voltage is called the wake-up time or T_{WU} and is specified in [Table 4 on page 5](#), with $C_b=1\mu\text{F}$. During the wake-up time phase, the TS4995 gain is close to zero. After the wake-up time period, the gain is released and set to its nominal value.

If C_b has a value different than $1\mu\text{F}$, then refer to the graph in [Figure 50](#) to establish the corresponding wake-up time value.

Figure 50. Startup time vs. bypass capacitor



4.7 Shutdown time

When the standby command is set, the time required to put the two output stages in high impedance and the internal circuitry in shutdown mode is a few microseconds.

Note: In shutdown mode, the Bypass pin and V_{in+} , V_{in-} pins are shorted to ground by internal switches. This allows a quick discharge of C_b and C_{in} .

4.8 Pop performance

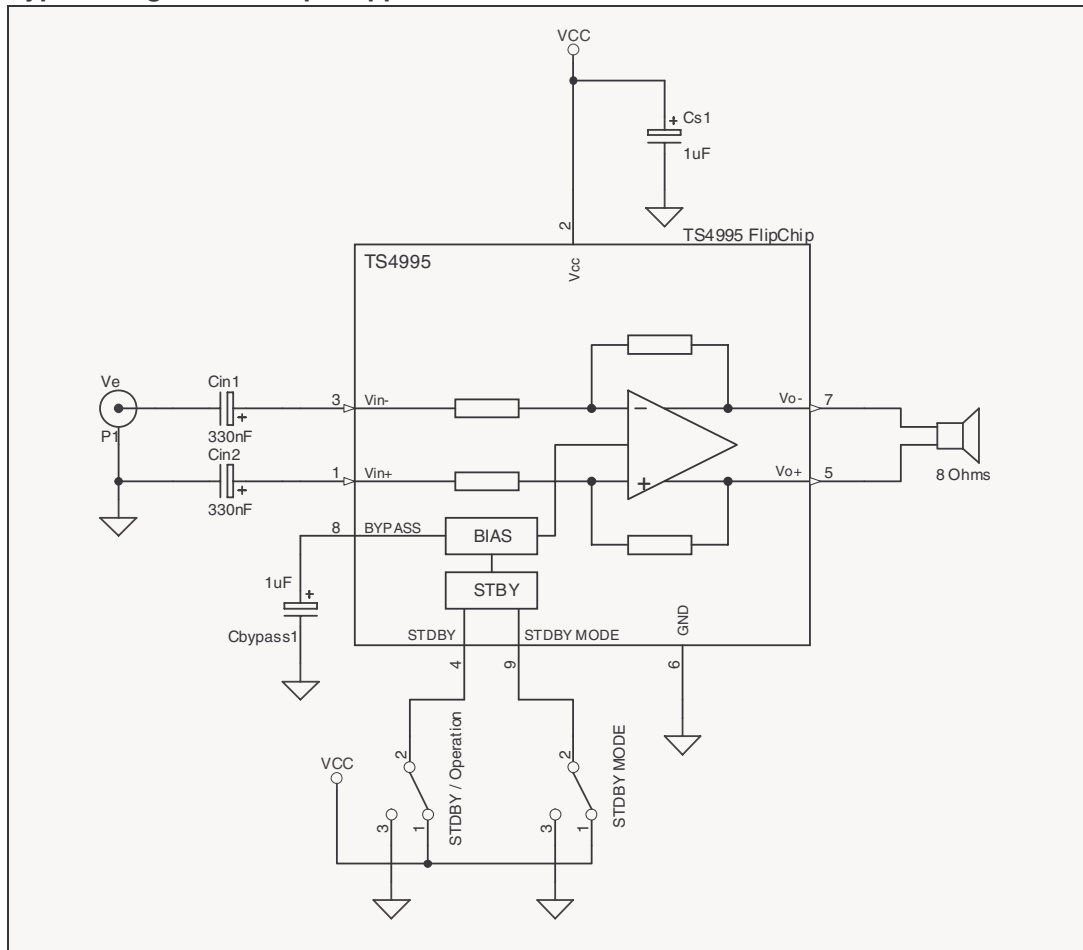
In theory, due to a fully differential structure, the TS4995 pop performance should be perfect. However, due to R_{in} , R_{feed} , and C_{in} mismatching, some startup noise could remain. In the TS4995 a built-in pop reduction circuitry allows to reach the theoretical pop (with mismatched components). With this circuitry, the TS4995 is close to zero pop for all common applications possible.

In addition, when the TS4995 is set in standby, due to the high impedance output stage configuration in this mode, no pop is possible.

4.9 Single-ended input configuration

It is possible to use the TS4995 in a single-ended input configuration. However, input coupling capacitors are needed in this configuration. The schematic in [Figure 51](#) shows this configuration as example.

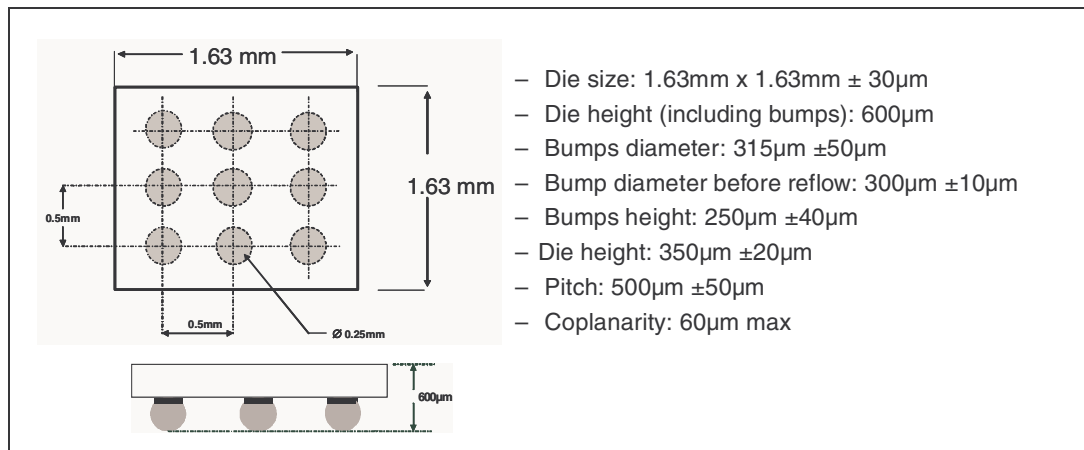
Figure 51. Typical single-ended input application



5 Package mechanical data

To meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

5.1 9-bump flip-chip package



5.2 Tape & reel schematic (top view)

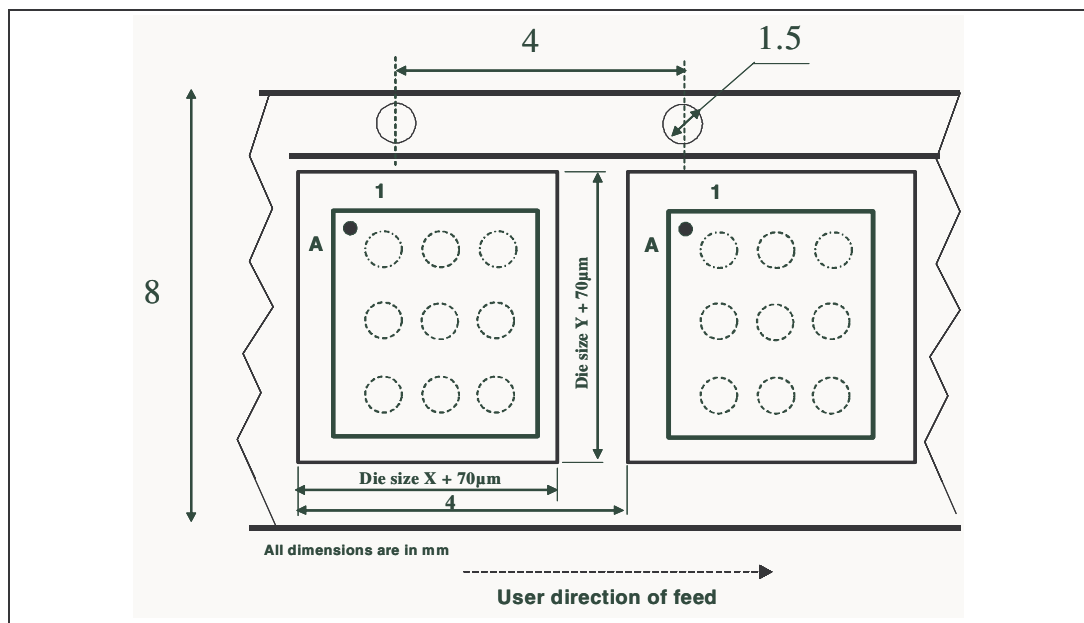


Figure 52. Pin out (top view)

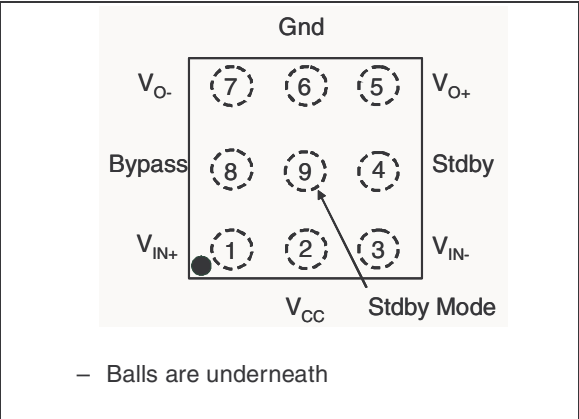


Figure 53. Marking (top view)

