INTEGRATED CIRCUITS

DATA SHEET

TDA3615J

Multiple voltage regulator

Preliminary specification
File under Integrated Circuits, IC01

1998 Jun 23

Philips
Semiconductors

PHILIPS

FEATURES

General

- Six voltage regulators
- Five microprocessor controlled regulators (regulators 2 to 6)
- Regulator 1 and reset operate during load dump and thermal shutdown
- Low reverse current of regulator 1
- Very low quiescent current when regulators 2 to 6 and power switches are switched off ($V_{I(ig)}$ = 0 V)
- Reset output
- Adjustable display regulator
- High ripple rejection
- Three power switches
- Low noise for regulators 2 to 6.

Protections

- Reverse polarity safe (down to –18 V without high reverse current)
- Able to withstand voltages up to 18 V at the output (supply line may be short-circuited)
- ESD protected on all pins
- Thermal protection
- Load dump protection
- Foldback current limit protection (except for regulator 2)
- The regulator outputs and the power switches are DC short-circuited safe to ground and V_{bat}.

GENERAL DESCRIPTION

The TDA3615J is a multiple output voltage regulator with power switches, intended for use in car radios with or without a microprocessor. It contains:

- One fixed voltage regulator (regulator 1) intended to supply a microprocessor, that also operates during load dump and thermal shutdown
- 5 power regulators supplied by $V_{I(ig)}$
- 3 power switches with protections
- 3 enable inputs for selecting regulators 2 to 6 and the three power switches
- Very low quiescent current of typical 110 μA.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3615J	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{bat/I(ig)}$	supply voltage					
	operating	regulators on	11	14.4	18	V
	operating	regulator 1 on	3.5	14.4	18	V
	jump start	$t \leq 10$ minutes	–	–	30	V
	load dump protection	$t \leq 50$ ms; $t_r \geq 2.5$ ms	–	–	50	V
I_q	quiescent supply current	V_{bat} = 14.4 V; $V_{I(ig)}$ < 1 V; note 1	–	110	250	μA
		V_{bat} = $V_{I(ig)}$ = 14.4 V; selector inputs 0,0,0 (state 3 in Table 1); note 1	–	125	–	μA
Voltage regulators						
$V_{O(REG1)}$	output voltage regulator 1 (5 V standby)	0.5 mA ≤ I_{REG1} ≤ 50 mA	4.75	5.0	5.25	V
$V_{O(REG2)}$	output voltage regulator 2 (filament)	0.5 mA ≤ I_{REG2} ≤ 300 mA	2.7	2.85	3.0	V
$V_{O(REG3)}$	output voltage regulator 3 (5 V logic)	0.5 mA ≤ I_{REG3} ≤ 450 mA	4.75	5.0	5.25	V
$V_{O(REG4)}$	output voltage regulator 4 (synthesizer)	0.5 mA ≤ I_{REG4} ≤ 100 mA	9.0	9.5	10.0	V
$V_{O(REG5)}$	output voltage regulator 5 (AM)	0.5 mA ≤ I_{REG5} ≤ 150 mA	9.0	9.5	10.0	V
$V_{O(REG6)}$	output voltage regulator 6 (FM)	0.5 mA ≤ I_{REG6} ≤ 150 mA	9.0	9.5	10.0	V
Power switches						
V_{d1}	drop-out voltage switch 1 (antenna)	I_{SW1} = 0.55 A	0.1	0.45	1.6	V
I_M	peak current switch 1	t < 1 s	1.7	1.9	–	A
V_{d2}	drop-out voltage switch 2 (media)	I_{SW2} = 1 A	–	0.5	1.0	V
V_{clamp2}	clamping voltage switch 2		–	15.0	16	V
V_{d3}	drop-out voltage switch 3 (display)	I_{SW3} = 0.35 A	–	0.5	1.0	V
V_{clamp3}	clamping voltage switch 3		–	15.2	16	V

Note

1. The quiescent current is measured when $R_L = \infty$.

BLOCK DIAGRAM

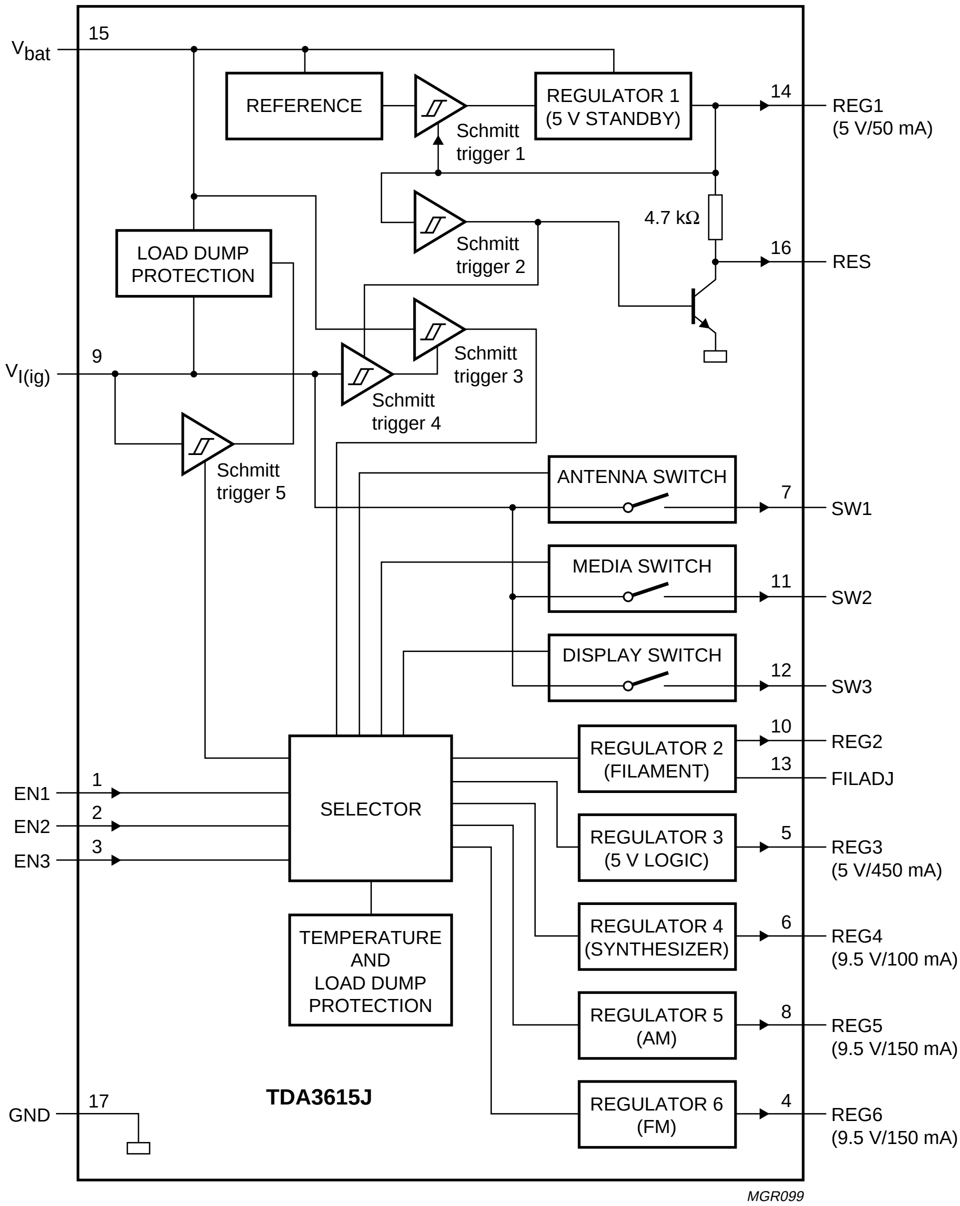


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
EN1	1	enable input 1
EN2	2	enable input 2
EN3	3	enable input 3
REG6	4	regulator 6 output, FM
REG3	5	regulator 3 output, 5 V logic
REG4	6	regulator 4 output, synthesizer
SW1	7	switch 1 output, antenna
REG5	8	regulator 5 output, AM
$V_{I(ig)}$	9	ignition input voltage
REG2	10	regulator 2 output, filament
SW2	11	switch 2 output, media
SW3	12	switch 3 output, display
FILADJ	13	filament adjustment
REG1	14	regulator 1 output, 5 V standby
V_{bat}	15	battery input voltage
RES	16	reset output
GND	17	ground

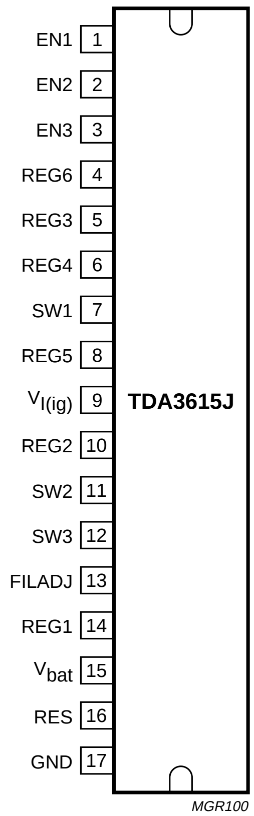


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA3615J is a multiple voltage regulator intended to supply a microprocessor (e.g. in car radio applications). Because of low-voltage operation of the application, a low-voltage drop regulator is used in the TDA3615J.

Regulator 1 (5 V standby) will switch on when the supply voltage exceeds 7.2 V for the first time and will switch off again when the output voltage of the regulator drops below 3.5 V.

Reset is used to indicate that the regulator output voltage is within its voltage range. This start-up feature is built-in to secure a smooth start-up of the microprocessor at first connection, without uncontrolled switching of the standby regulator during the start-up sequence.

All other regulators and switches can be switched on and off by using the three control input pins. This is only possible when both supply voltages (V_{bat} and $V_{I(ig)}$) are within their voltage range. Table 1 shows all possible states.

The filament regulator output voltage of the TDA3615J can be adjusted with pin FILADJ.

All output pins are fully protected. The regulators are protected against load dump and short-circuit (foldback current protection, except the filament regulator output). At load dump all regulator outputs will go LOW except the 5 V standby regulator output.

The antenna switch and the media switch can withstand ‘loss of ground’. This means that the ground pin is disconnected and the switch output is connected to ground (V_{bat} and $V_{I(ig)}$ are normally connected to the right pin).

Selector settings

Table 1 Possible states of outputs depending on inputs

STATE	INPUTS					OUTPUTS								
	V_{bat}	$V_{I(ig)}$	EN1	EN2	EN3	REG1	REG2	REG3	REG4	REG5	REG6	SW1	SW2	SW3
1	0	X(1)	X(1)	X(1)	X(1)	0	0	0	0	0	0	0	0	0
2	1	0	X(1)	X(1)	X(1)	1	0	0	0	0	0	0	0	0
3	1	1	0	0	0	1	0	0	0	0	0	0	0	0
4	1	1	0	0	1	1	1	1	1	0	1	1	0	1
5	1	1	0	1	0	1	1	1	1	1	0	1	0	1
6	1	1	0	1	1	1	1	1	0	0	0	0	1	1
7	1	1	1	0	0	1	1	1	0	0	0	0	0	1
8	1	1	1	0	1	1	1	1	1	0	1	1	1	1
9	1	1	1	1	0	1	1	1	1	1	0	1	1	1
10	1	1	1	1	1	1	1	1	1	0	0	1	1	1

Note

1. X = don’t care.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{bat/I(ig)}$	supply voltage				
	operating	regulators on	–	18	V
	jump start	$t \leq 10$ minutes	–	30	V
	load dump protection	$t \leq 50$ ms; $t_r \geq 2.5$ ms	–	50	V
V_{rp}	reverse polarity voltage	non-operating	–	–18	V
P_{tot}	total power dissipation	$T_{amb} = 25$ °C	–	62.5	W
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C
T_j	junction temperature	operating	–40	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case		2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W

QUALITY SPECIFICATION

Quality specification is in accordance with *“SNW-FQ-611E”*.

CHARACTERISTICS

$V_{bat} = V_{I(ig)} = 14.4$ V; $T_{amb} = 25$ °C; see Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{bat/I(ig)}$	supply voltage					
	operating	regulators on	11	14.4	18	V
	jump start	t ≤ 10 minutes	–	–	30	V
	load dump protection	t ≤ 50 ms; t_r ≥ 2.5 ms	–	–	50	V
I_q	quiescent supply current	V_{bat} = 14.4 V; $V_{I(ig)}$ < 1 V; note 1	–	110	250	μA
		$V_{bat} = V_{I(ig)}$ = 14.4 V; selector inputs 0,0,0; note 1	–	125	–	μA
Reset buffer						
$I_{sink(L)}$	LOW-level sink current		2	15	–	mA
$R_{pu(int)}$	internal pull-up resistance		3.7	4.7	5.7	kΩ
Selector control inputs						
V_{IL}	LOW-level input voltage		–0.5	–	+0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	–	V
I_{IH}	HIGH-level input current	V_{IH} > 2 V	–	–	1.0	mA
I_{IL}	LOW-level input current	V_{IL} < 0.8 V	–1.0	–	–	mA
Regulator 1 for 5 V standby (I_{REG1} = 1 mA unless otherwise specified)						
$V_{O(REG1)}$	output voltage	0.5 mA ≤ I_{REG1} ≤ 50 mA	4.75	5.0	5.25	V
		6.5 V ≤ V_{bat} ≤ 18 V; note 2	4.75	5.0	5.25	V
		18 V ≤ V_{bat} ≤ 50 V; load dump; I_{REG1} = 30 mA	4.75	5.0	5.25	V
ΔV_{LN}	line voltage regulation	7 V ≤ V_{bat} ≤ 18 V	–	3	50	mV
ΔV_L	load voltage regulation	0.5 mA ≤ I_{REG1} ≤ 50 mA	–	–	60	mV
SVRR	supply voltage ripple rejection	f_i = 120 Hz; $V_{i(p-p)}$ = 2 V	60	72	–	dB
V_d	drop-out voltage	V_{bat} = 5 V; note 3	–	0.27	1	V
I_l	current limit	V_{REG1} > 4.5 V	60	170	–	mA
I_{sc}	short-circuit current	R_L ≤ 0.5 Ω; note 5	15	60	–	mA
Regulator 2 for filament (I_{REG2} = 5 mA unless otherwise specified)						
$V_{O(REG2)}$	output voltage	0.5 mA ≤ I_{REG2} ≤ 300 mA	2.7	2.85	3.0	V
		7.5 V ≤ V_{bat} ≤ 16.9 V	2.7	2.85	3.0	V
		adjust control	1.1	adjust	$V_{I(ig)}$	V
ΔV_{LN}	line voltage regulation	7.5 V ≤ V_{bat} ≤ 16.9 V	–	–	50	mV
ΔV_L	load voltage regulation	5 mA ≤ I_{REG2} ≤ 300 mA	–	–	70	mV
SVRR	supply voltage ripple rejection	f_i = 120 Hz; $V_{i(p-p)}$ = 2 V	60	80	–	dB
I_{sc}	short-circuit current	R_L ≤ 0.5 Ω	0.35	0.66	–	A

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Regulator 3 for 5 V logic (I_{REG3} = 5 mA unless otherwise specified)						
$V_{O(REG3)}$	output voltage	0.5 mA ≤ I_{REG3} ≤ 450 mA	4.75	5.0	5.25	V
		7.5 V ≤ V_{bat} ≤ 16.9 V	4.75	5.0	5.25	V
ΔV_{LN}	line voltage regulation	7.5 V ≤ V_{bat} ≤ 16.9 V	–	–	50	mV
ΔV_L	load voltage regulation	5 mA ≤ I_{REG3} ≤ 450 mA	–	–	60	mV
SVRR	supply voltage ripple rejection	f_i = 120 Hz; $V_{i(p-p)}$ = 2 V	60	80	–	dB
I_l	current limit	V_{REG3} > 3.5 V	0.5	0.85	–	A
I_{sc}	short-circuit current	R_L ≤ 0.5 Ω; note 5	20	125	–	mA
Regulator 4 for synthesizer (I_{REG4} = 5 mA unless otherwise specified)						
$V_{O(REG4)}$	output voltage	0.5 mA ≤ I_{REG4} ≤ 100 mA	9.0	9.5	10.0	V
		10.75 V ≤ V_{bat} ≤ 16.9 V	9.0	9.5	10.0	V
ΔV_{LN}	line voltage regulation	10.75 V ≤ V_{bat} ≤ 16.9 V	–	–	50	mV
ΔV_L	load voltage regulation	5 mA ≤ I_{REG4} ≤ 100 mA	–	–	70	mV
SVRR	supply voltage ripple rejection	f_i = 120 Hz; $V_{i(p-p)}$ = 2 V	60	70	–	dB
V_d	drop-out voltage	I_{REG4} = 0.1 A; V_{bat} = 9 V; note 4	–	0.18	0.5	V
I_l	current limit	V_{REG4} > 7 V	0.35	0.57	–	A
I_{sc}	short-circuit current	R_L ≤ 0.5 Ω; note 5	20	160	–	mA
Regulator 5 for AM (I_{REG5} = 5 mA unless otherwise specified)						
$V_{O(REG5)}$	output voltage	0.5 mA ≤ I_{REG5} ≤ 150 mA	9.0	9.5	10.0	V
		10.75 V ≤ V_{bat} ≤ 16.9 V	9.0	9.5	10.0	V
ΔV_{LN}	line voltage regulation	10.75 V ≤ V_{bat} ≤ 16.9 V	–	–	50	mV
ΔV_L	load voltage regulation	5 mA ≤ I_{REG5} ≤ 150 mA	–	–	70	mV
SVRR	supply voltage ripple rejection	f_i = 120 Hz; $V_{i(p-p)}$ = 2 V	60	70	–	dB
V_d	drop-out voltage	I_{REG5} = 0.15 A; V_{bat} = 9 V; note 4	–	0.35	1	V
I_l	current limit	V_{REG5} > 7 V	0.2	0.37	–	A
I_{sc}	short-circuit current	R_L ≤ 0.5 Ω; note 5	50	130	–	mA
Regulator 6 for FM (I_{REG6} = 5 mA unless otherwise specified)						
$V_{O(REG6)}$	output voltage	0.5 mA ≤ I_{REG6} ≤ 150 mA	9.0	9.5	10.0	V
		10.75 V ≤ V_{bat} ≤ 16.9 V	9.0	9.5	10.0	V
ΔV_{LN}	line voltage regulation	10.75 V ≤ V_{bat} ≤ 16.9 V	–	–	50	mV
ΔV_L	load voltage regulation	5 mA ≤ I_{REG6} ≤ 150 mA	–	–	70	mV
SVRR	supply voltage ripple rejection	f_i = 120 Hz; $V_{i(p-p)}$ = 2 V	60	70	–	dB
V_d	drop-out voltage	I_{REG6} = 0.15 A; V_{bat} = 9 V; note 4	–	0.4	1	V
I_l	current limit	V_{REG6} > 7 V	0.2	0.37	–	A
I_{sc}	short-circuit current	R_L ≤ 0.5 Ω; note 5	50	125	–	mA
Power switch 1 (antenna)						
V_{d1}	drop-out voltage	I_{SW1} = 0.55 A; note 4	0.1	0.45	1.6	V
V_{clamp1}	clamping voltage		–	15.2	16	V
I_M	peak current	t < 1 s	1.7	1.9	–	A

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power switch 2 (media)						
V_{d2}	drop-out voltage	I_{SW2} = 1 A; note 4	–	0.5	1.0	V
V_{clamp2}	clamping voltage		–	15.0	16	V
Power switch 3 (display)						
V_{d3}	drop-out voltage	I_{SW3} = 0.35 A; note 4	–	0.5	1.0	V
V_{clamp3}	clamping voltage		–	15.2	16	V
Schmitt trigger 1 for regulator						
V_{thr}	rising threshold voltage	selector inputs 0,0,0 (state 3 in Table 1); I_{REG1} = 10 mA	6.2	7.2	7.8	V
V_{thf}	falling threshold voltage	selector inputs 0,0,0 (state 3 in Table 1); I_{REG1} = 10 mA	3.2	3.5	3.7	V
V_{hys}	hysteresis voltage		–	3.7	–	V
Schmitt trigger 2 for reset; note 6						
V_{thr}	rising threshold voltage	I_{REG1} = 10 mA	4.28	4.45	4.73	V
V_{thf}	falling threshold voltage	I_{REG1} = 10 mA	4.2	4.35	4.5	V
V_{hys}	hysteresis voltage		–	0.1	–	V
Schmitt trigger 3 for battery sense						
V_{thr}	rising threshold voltage	$V_{I(ig)}$ = 14.4 V; R_L = 1 kΩ	6.8	7.35	7.9	V
V_{thf}	falling threshold voltage	$V_{I(ig)}$ = 14.4 V; R_L = 1 kΩ	5.5	5.95	6.4	V
V_{hys}	hysteresis voltage		–	1.4	–	V
Schmitt trigger 4 for ignition sense						
V_{thr}	rising threshold voltage	V_{bat} = 14.4 V; R_L = 100 Ω	7.2	7.6	8.0	V
V_{thf}	falling threshold voltage	V_{bat} = 14.4 V; R_L = 100 Ω	6.0	6.3	6.8	V
V_{hys}	hysteresis voltage		–	1.3	–	V
Schmitt trigger 5 for load dump						
V_{thr}	rising threshold voltage	selector inputs 1,0,1 (state 8 in Table 1); note 7	17.5	18.5	19.5	V
V_{thf}	falling threshold voltage	selector inputs 1,0,1 (state 8 in Table 1); note 7	17	V_{thr} – 0.3	V_{thr} – 0.1	V

Notes

1. The quiescent current is measured when $R_L = \infty$.
2. Only if V_{bat} has exceeded 7.2 V.
3. The drop-out voltage of regulator 1 is measured between V_{bat} and V_{REGx}.
4. The drop-out voltage of regulators 2 to 6 and power switches 1, 2 and 3 are measured between $V_{I(ig)}$ and V_{REGx} or between $V_{I(ig)}$ and V_{SWx}.
5. The foldback current protection limits the dissipation power at short-circuit.
6. The voltage of regulator 1 sinks as a result of a supply voltage drop.
7. Only when one of the control pins is HIGH.

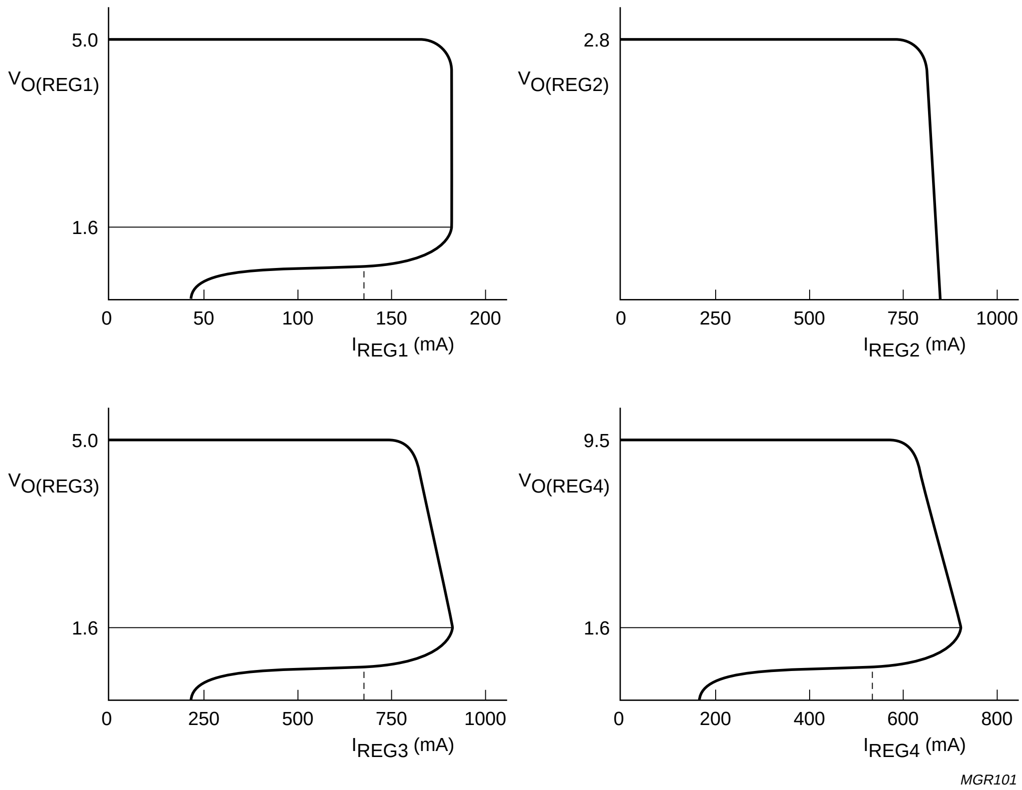


Fig.3 Typical foldback current protection behaviour.

TEST AND APPLICATION INFORMATION

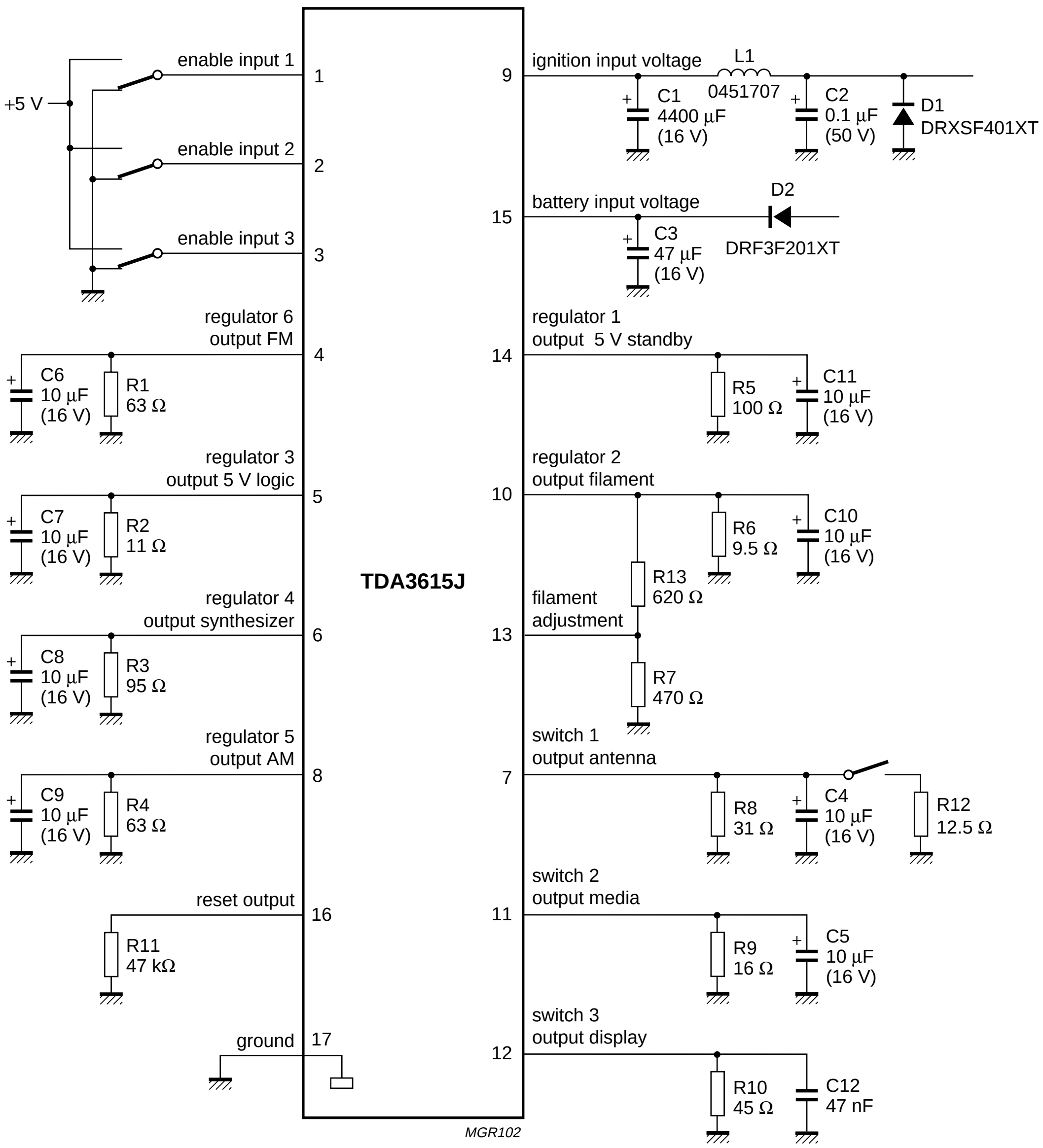


Fig.4 Typical application circuit.

Application information

NOISE

Table 2 Noise figures

REGULATOR	NOISE FIGURE (μV)(1)		
	C_o = 10 μF	C_o = 47 μF	C_o = 100 μF
1	175	145	100
2	125	98	85
3	180	150	125
4	290	260	190
5	290	260	190
6	290	260	190

Note

1. Measured at a bandwidth of 1 MHz.

The regulator outputs for regulators 2 to 6 are designed in such a way that the noise is very low and the stability is very good. The noise output voltages are depending on the output capacitors. Table 2 describes the influence of the output capacitors on the output noise.

STABILITY

The regulators are made stable with the external connected output capacitors.

With almost any output capacitor, stability can be guaranteed (see Figs 5, 6 and 7).

When only an electrolytic capacitor is used, the temperature behaviour of this output capacitor can cause oscillations at extreme low temperature. The next 2 examples show how an output capacitor value is selected. Oscillation problems can be avoided by adding a 47 nF capacitor in parallel with the electrolytic capacitor.

Example 1 (regulator 1)

Regulator 1 is made stable with an electrolytic output capacitor of 10 μF (ESR = 3.1 Ω). At –30 °C the capacitor value is decreased to 3 μF and the ESR is increased to 22 Ω. The regulator will remain stable at –30 °C (see Fig.5).

Example 2 (regulator 5)

Regulator 5 is made stable with a 2.2 μF electrolytic capacitor (ESR = 8 Ω). At –30 °C the capacitor value is decreased to 0.8 μF and the ESR is increased to 56 Ω. Using Fig.6, the regulator will be instable at –30 °C.

Even when only a small MKT capacitor of 47 nF is used as output capacitor, regulator 5 will remain stable over all temperatures.

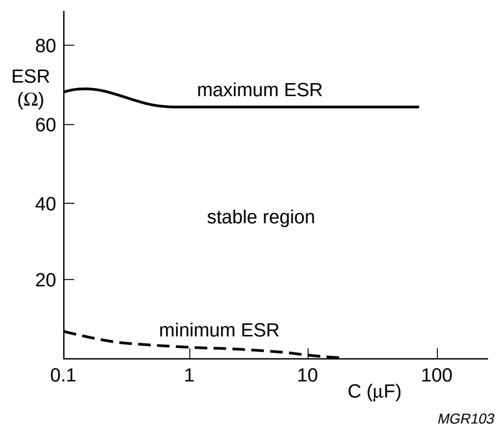


Fig.5 Stability curve of regulator 1 (5 V standby).

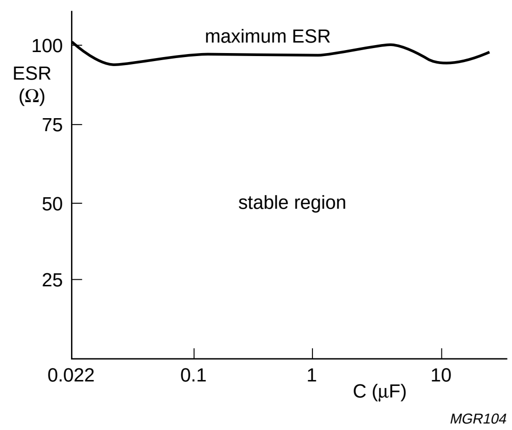


Fig.6 Stability curve of regulator 5 (AM).

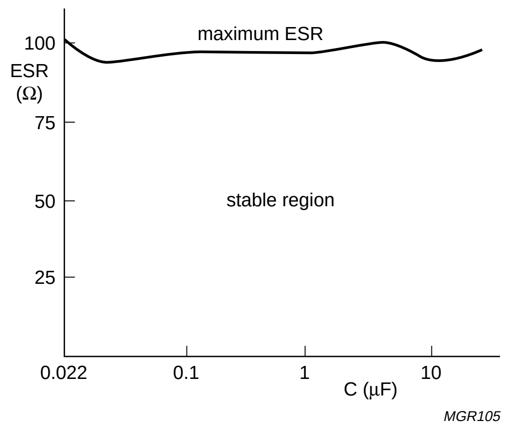


Fig.7 Stability curve of regulator 3 (5 V logic).

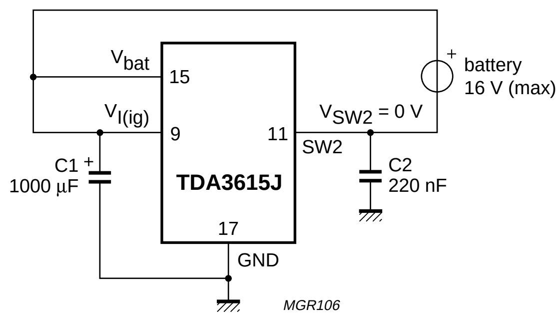


Fig.8 Loss of ground test circuit.

LOSS OF GROUND PROTECTION

Two power switches (media and antenna) are protected for loss of ground. The loss of ground situation is depicted in Fig.8. The ground terminal of the battery is connected to the output of the media switch. Two problems occur:

1. At first connection a high charge current will flow through C1 to the ground terminal (pin 17) of the TDA3615J and out of the switch output (pin 11). The media and antenna switches are protected to limit this current.
1. When the switch is enabled, a short-circuit current will flow out of the power switch output (pin 11) because the output of the switch is shortened below substrate potential.

A special protection is built-in to avoid the media and antenna switches from being damaged during a loss of ground condition.

In practice, this condition can occur when the ground terminal of the total application is connected to the switch output due to a bad wiring.

CAPACITIVE LOADS ON POWER SWITCHES

Power switches can deliver a large current to the connected loads. When a supply voltage ripple is applied, large load currents will flow when capacitive loads are used in parallel with normal loads.

When the output of a power switch is forced above $V_{I(ig)}$ an internal protection is activated to switch off the switch as long as the fault is present.

The display switch in particular is sensitive to capacitive loads.

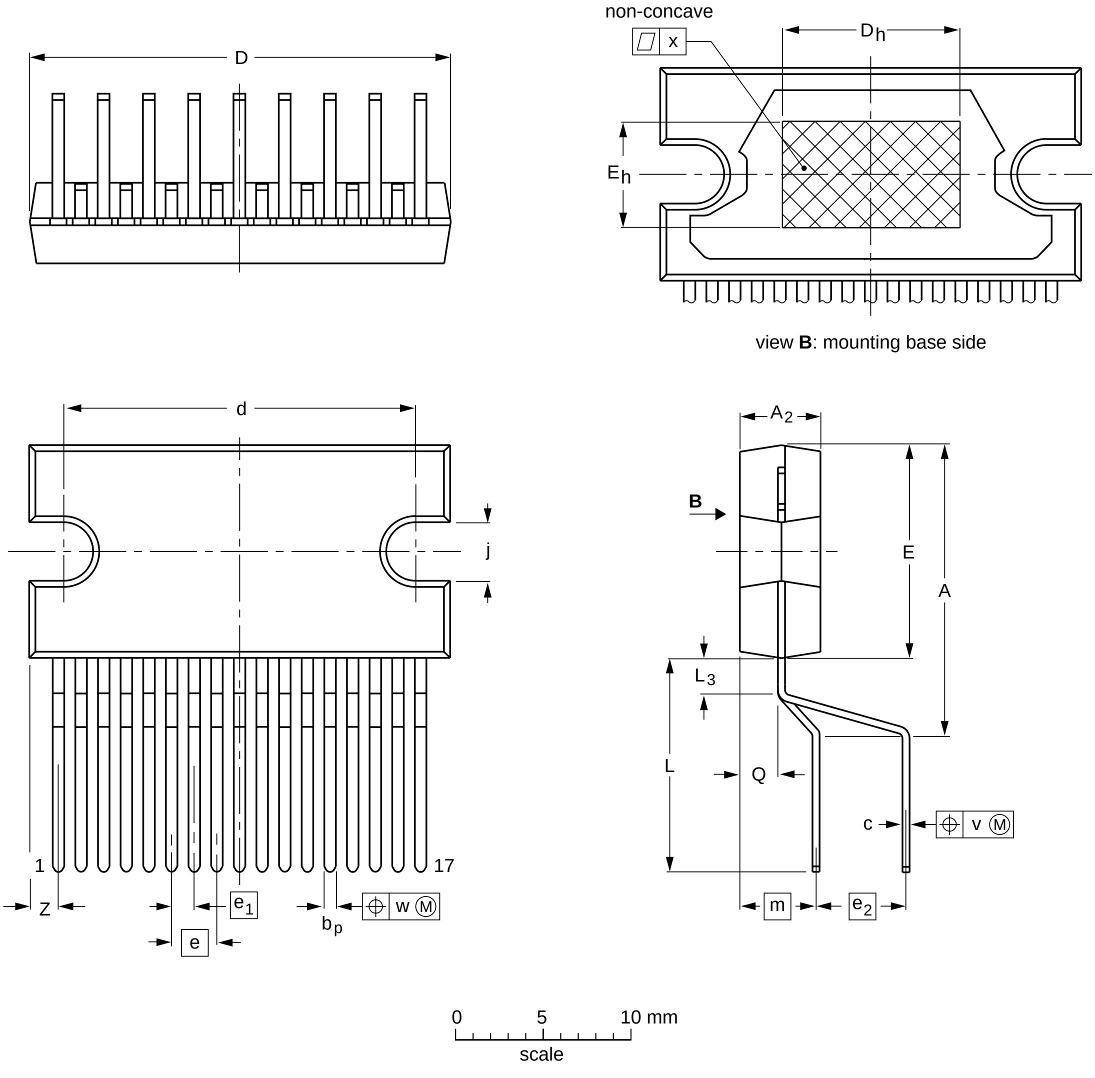
We therefore strongly advise:

- Use only a 47 nF output capacitor on the display switch
- Use a 10 μF capacitor on the outputs of the antenna and media switch.

On the outputs of regulators 2 to 6 a capacitor of 47 nF can be used; larger values are possible but not necessary to guarantee stability (see Figs 5, 6 and 7).

PACKAGE OUTLINE

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm) **SOT243-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT243-1						~~95-03-11~~ 97-12-16

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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