DATA SHEET

TDA3755
PAL/NTSC/SECAM synchronization processor for video recorders

Product specification
File under Integrated Circuits, IC02

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Philips Semiconductors

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PAL/NTSC/SECAM synchronization processor for video recorders

TDA3755

GENERAL DESCRIPTION

The TDA3755 is a monolithic integrated circuit for PAL/NTSC SECAM synchronization processing in VHS video recorders.

Features

- Adaptive sync separator
- Internal vertical sync pulse integrator
- Composite sync and vertical pulse output
- Current controlled oscillator (CCO) with 320/321 times horizontal frequency
- Horizontal phase detector with current output
- Video identification and mute circuit
- Burst gating pulse output (externally adjustable phase relationship)
- Test-picture output
- Subcarrier frequency output switched in phase in accordance with VHS standard
- Fast phase correction of subcarrier frequency
- Selection input to force PAL or NTSC function
- Still picture input

QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_P = V_{13\text{-}15}$	typ.	10	V
Supply current (pin 13)	$I_P = I_{13}$	typ.	24	mA
Sync separator				
Sync pulse input voltage				
(peak-to-peak value)	$V_{3\text{-}15(p\text{-}p)}$	typ.	300	mV
Sync pulse output voltage				
(peak-to-peak value)	$V_{1\text{-}15(p\text{-}p)}$	min.	7,3	V
Vertical sync pulse				
Output voltage				
(peak-to-peak value)	$V_{18\text{-}15(p\text{-}p)}$	min.	2,7	V
Phase detector				
Catching range	Δf	min.	$\pm$ 3,0	%
Oscillator				
Oscillator frequency				
PAL	f_{osc}	typ.	5,02	MHz
NTSC	f_{osc}	typ.	5,04	MHz
Output frequency				
PAL	f_o	typ.	627	kHz
NTSC	f_o	typ.	629	kHz
Output sinewave				
(peak-to-peak value)	$V_{8\text{-}15(p\text{-}p)}$	typ.	3	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102); SOT102-1; 1996 December 11.

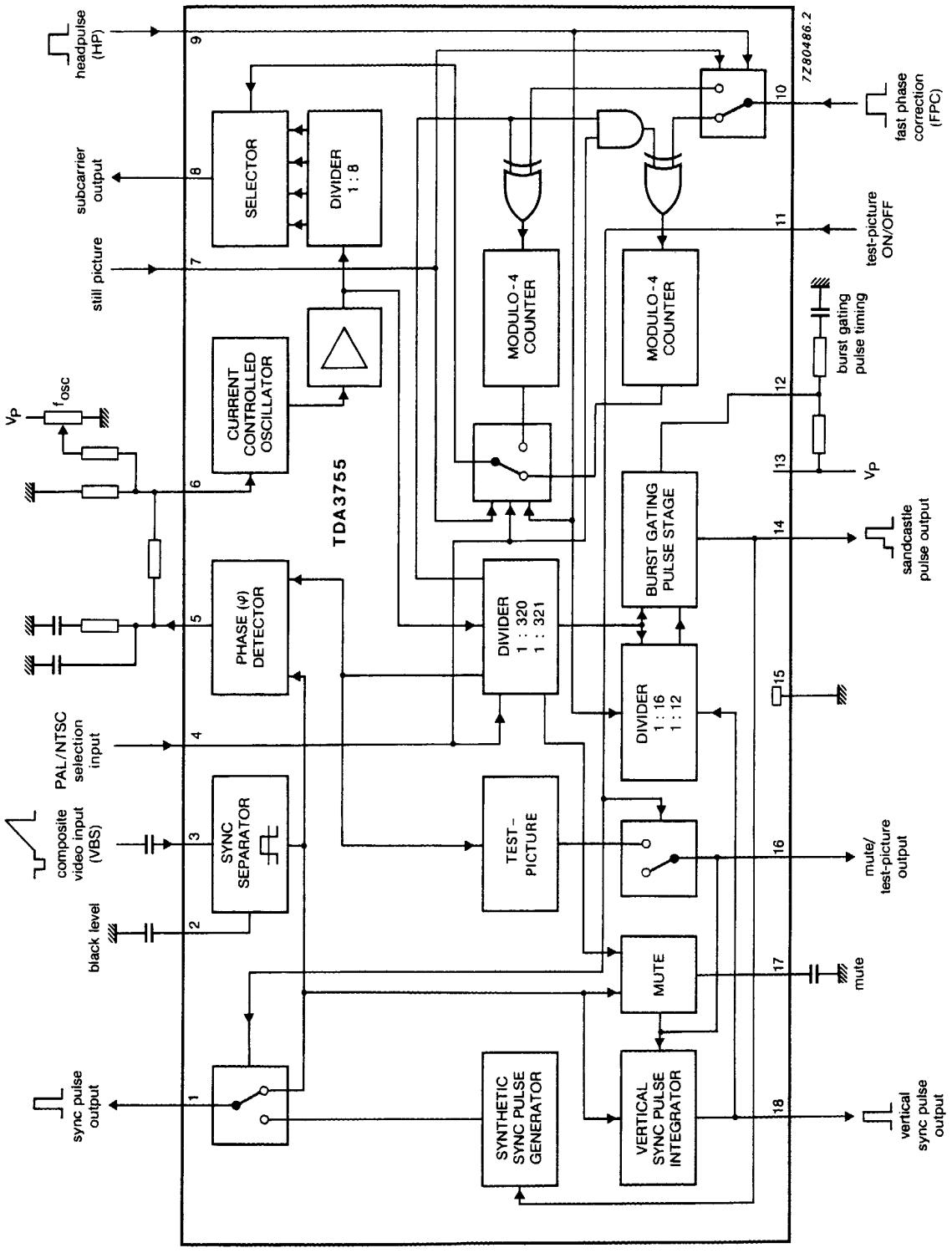


Fig.1 Block diagram

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13-15}$	max. 13,2	V
Voltage range at pins 2, 3, 4, 7, 9, 10, 11, 17 to pin 15 (ground)	V_{n-15}	0 to V_P	V
Voltage range at pin 12	V_{12-15}	min. 0	V
Voltage range at pin 6	V_{6-15}	max. 8	V
Currents			
at pins 1, 5, 8, 14, 16, 18	$\pm I_n$	max. 5	mA
at pin 6	$-I_6$	max. 1	mA
at pin 12	I_{12}	max. 2	mA
Total power dissipation	P_{tot}	max. 1	W
Storage temperature range	T_{stg}	−25 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

CHARACTERISTICS

V_P = 10 V; T_{amb} = 25 °C; measured in Fig.4; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply (pin 13)					
Supply voltage range	$V_P = V_{13-15}$	9,6	–	13,2	V
Supply current	$I_P = I_{13}$	–	24	–	mA
Sync separator (pin 3)					
Colour composite video input voltage (note 2) (peak-to-peak value)	$V_{3-15(p-p)}$	–	1	–	V
Sync pulse amplitude (peak-to-peak value)	$V_{3-15(p-p)}$	75	–	600	mV
Slicing level, relative to sync pulse amplitude (note 3)		–	50	–	%
Internal resistance of video source	R_G	–	–	1	kΩ
Sync output voltage HIGH at $-I_1$ = 1 mA	V_{1-15}	7,8	–	–	V
Sync output voltage LOW at I_1 = 1 mA	V_{1-15}	–	–	0,5	V
Delay between signal at input pin 3 and sync pulse at output pin 1	t_d	–	0,2	–	µs
Vertical sync pulse (pin 18; note 4)					
Output voltage HIGH at $-I_{18}$ = 1 mA	V_{18-15}	2,7	–	5,0	V
Output voltage LOW at I_{18} = 1,6 mA	V_{18-15}	–	–	0,5	V
Duration of HIGH state of internally generated output pulse	t_p	–	190	–	µs
Delay between leading edge of input signal at pin 3 and leading edge of output pulse at pin 18	t_d	32	–	64	µs
Selection input (pin 4)					
Input voltage for NTSC state	V_{4-15}	–	–	0,3	V
Input current at V_{4-15} = 0 V	$-I_4$	–	–	20	µA
Input voltage for PAL state pin 4 open circuit	V_{4-15}	2	–	–	V

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Test picture/mute/synthetic sync pulse					
Minimum voltage at pin 11 for test picture mode active (note 5)	$V_{11\text{-}15}$	4,8	–	–	V
Maximum voltage at pin 11 for test picture mode inactive	$V_{11\text{-}15}$	–	–	3,8	V
Output voltage at pin 16					
at test picture “black” or at mute	$V_{16\text{-}15}$	–	2,75	–	V
at test picture “white”	$V_{16\text{-}15}$	–	4,50	–	V
at “in sync condition”	$V_{16\text{-}15}$	–	–	0,5	V
Input current (pin 11)	$-I_{11}$	–	–	25	µA
Oscillator/phase detector					
Oscillator frequency (note 6)					
PAL	f_{osc}	–	5,02	–	MHz
NTSC	f_{osc}	–	5,04	–	MHz
Oscillator conversion gain	k_o	–	16,13	–	MHz/mA
D.C. control voltage	$V_{6\text{-}15}$	–	2,1	–	V
Input current for f = 5,016 MHz	$-I_{16}$	–	310	–	µA
Holding range (note 7)	Δf	$\pm$ 3,2	–	–	%
Catching range (note 7)	Δf	$\pm$ 3,0	–	–	%
Control loop gain	k_v	–	380 $\times 10^3$	–	s^{-1}
Output of lower subcarrier (note 8)					
(peak-to-peak value)	$V_{8\text{-}15(p\text{-}p)}$	–	3	–	V
Output current	I_8	–	–	2	mA
D.C. output voltage	$V_{8\text{-}15}$	–	3,1	–	V
2nd harmonic suppression without switching	α_{2nd}	20	–	–	dB
Switching position prior to centre of sync pulse (pin 3)	t_s	–	2	–	µs
Output peak current of phase detector during sync pulse	$\pm I_5$	–	3,78	–	mA
Output voltage range (note 9)	$V_{5\text{-}15}$	1,4	–	2,8	V

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Sandcastle pulse (pin 14; note 10)					
Output voltage HIGH (note 11)					
at $-I_{14}$ =1 mA	V_{14-15}	7,8	–	–	V
Output voltage INTERMEDIATE					
at $-I_{14}$ = 1 mA	V_{14-15}	2,3	3,0	3,7	V
Output voltage LOW					
at I_{14} =1 mA	V_{14-15}	–	–	0,5	V
Lower part is starting prior to the					
centre of sync pulse at pin 3	t_{14-3}	–	2,6	–	µs
and ending with the upper part					
Fast phase correction/head pulse					
Threshold voltage					
for fast phase correction (note 12)	V_{10-15}	–	7,2	–	V
Input current	$-I_{10}$	–	–	20	µA
Threshold voltage					
of head pulse input	V_{9-15}	–	1,4	–	V
Input current	$-I_9$	–	–	20	µA
D.C. input voltage	V_{7-15}	–	5,6	–	V
Input resistance	R_{7-15}	3	–	–	kΩ
Subcarrier phase switching (note 13)					
Phase switching of subcarrier phase					
in accordance with head pulse	V_{7-15}	–	5,6(1)	–	V
LOW state of still picture input	V_{7-15}	–	–	0,5	V
Continuous phase switching					
voltage	V_{7-15}	–	V_P	–	V

Notes to the characteristics

1. Or not connected.
2. The sync separator input signal is shown in Fig.2.
3. The black level and the top sync level are detected internally and stored in capacitors at pin 2 and pin 3 respectively.
4. The vertical sync pulse output is disabled by mute.
5. In test picture mode the synthetic sync pulse is fed to output pin 1 and the vertical pulse consists of an uninterrupted block pulse of 192 μs triggering at every transition of head pulse (HP) at pin 9. The timing of test picture and synthetic sync pulse is shown in Fig.3.
6. Oscillator adjustment during test picture mode made only, at $V_{11\text{-}15} > 4{,}8$ V, $V_{7\text{-}15} = 0$ V and $V_{4\text{-}15} > 2$ V or open circuit; measurement is $f_{osc} / 8$ at output pin 8.
7. The holding range and catching range are both determined by the resistor connected between pin 5 and pin 6.
8. The phase of the lower subcarrier is switched in accordance with the VHS standard. PNP emitter follower, internal resistive load of 10 kΩ (typ.) to V_P.
9. The output voltage at pin 5 is disabled during test picture mode.
10. The burst gating pulse is superimposed on an uninterrupted horizontal pulse. It is suppressed 16 times starting with every transition of the head pulse at pin 9. If a vertical pulse is detected during that time the burst gating pulses are additionally suppressed until line 12 and line 324 respectively. In any event the number of suppressed burst gating pulses is even.
11. The timing of the upper part of the sandcastle pulse is determined by the components connected to pin 12 (Fig.4) and is independent of supply voltage variations.
12. The fast phase correction pulses have to be in the burst gating reference pulse. For any HIGH to LOW transitions of the correction pulse the phase is corrected by –90° if the head pulse input is LOW and by +90° if the head pulse input is HIGH.
13. Subcarrier phase switching is detailed in Table 1.
    Subcarrier is $40{,}000 \times f_H$ for NTSC state and $40{,}125 \times f_H$ for PAL state.

Table 1 Subcarrier phase switching

STILL	PAL		NTSC	
PICTURE INPUT	HP = HIGH	HP = LOW	HP = HIGH	HP = LOW
HIGH	–90°	–90°	–90°	–90°
not connected	0°	–90°	+90°	–90°
LOW	0°	0°	+90°	+90°

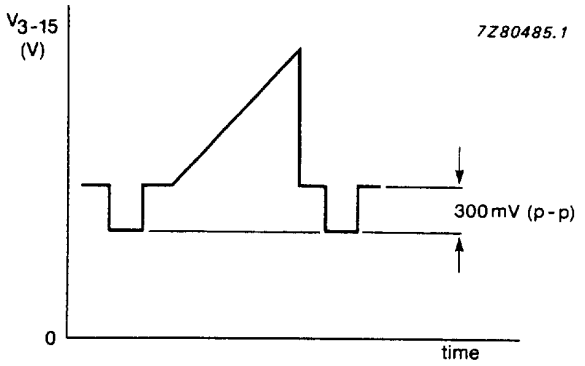
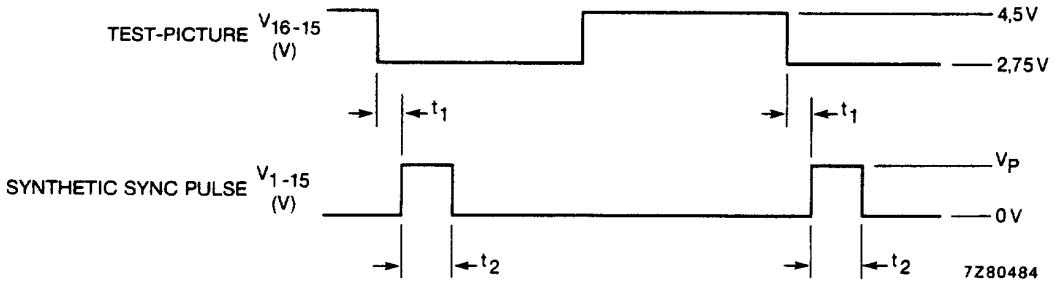


Fig.2 Colour composite video input signal at pin 3.



Where: The value of t_1 is dependent upon adjustment of the burst gating pulse delay.
Time t_2 is the burst gating pulse duration.

Fig.3 Timing of test picture and synthetic sync pulse.

APPLICATION INFORMATION

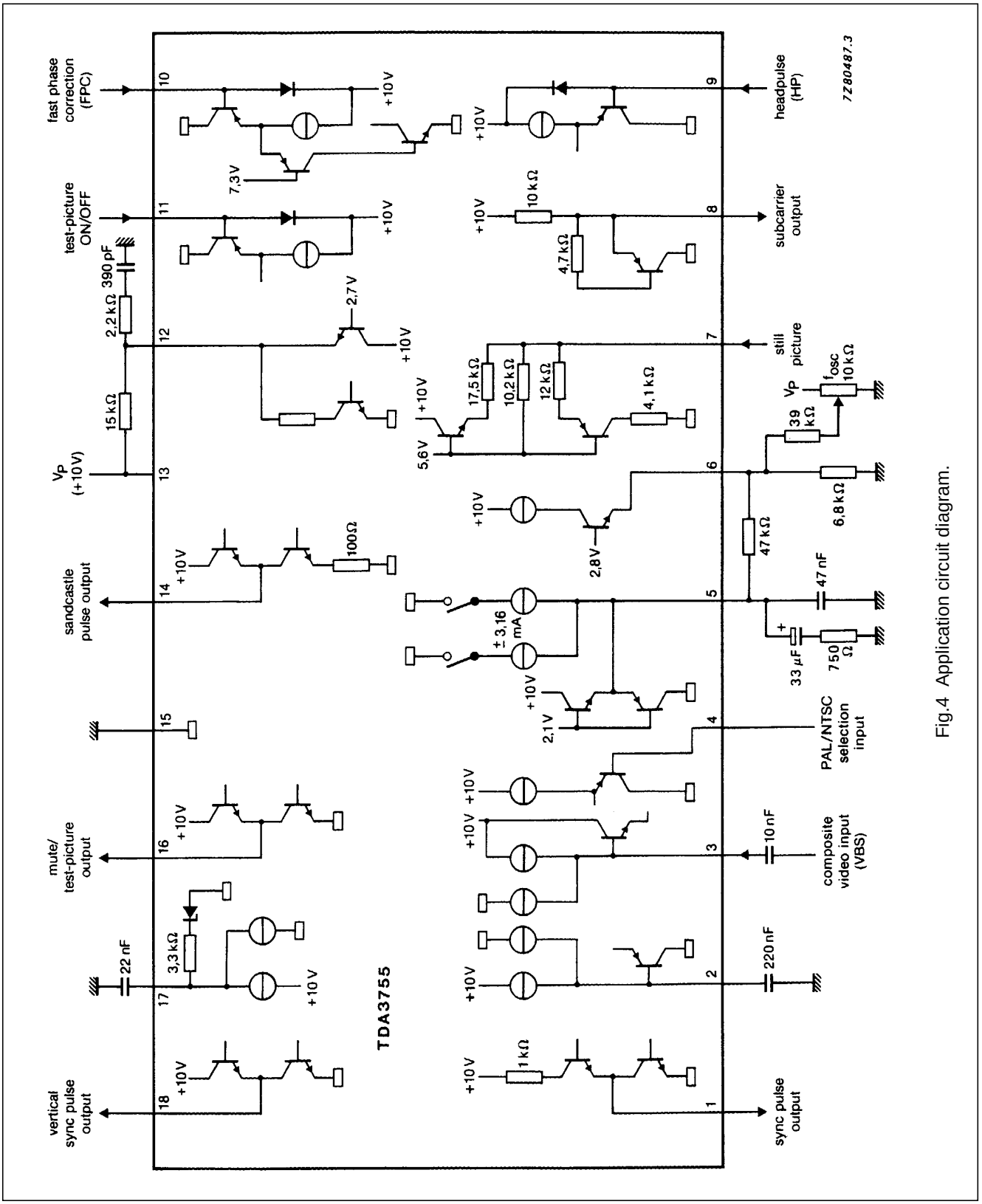
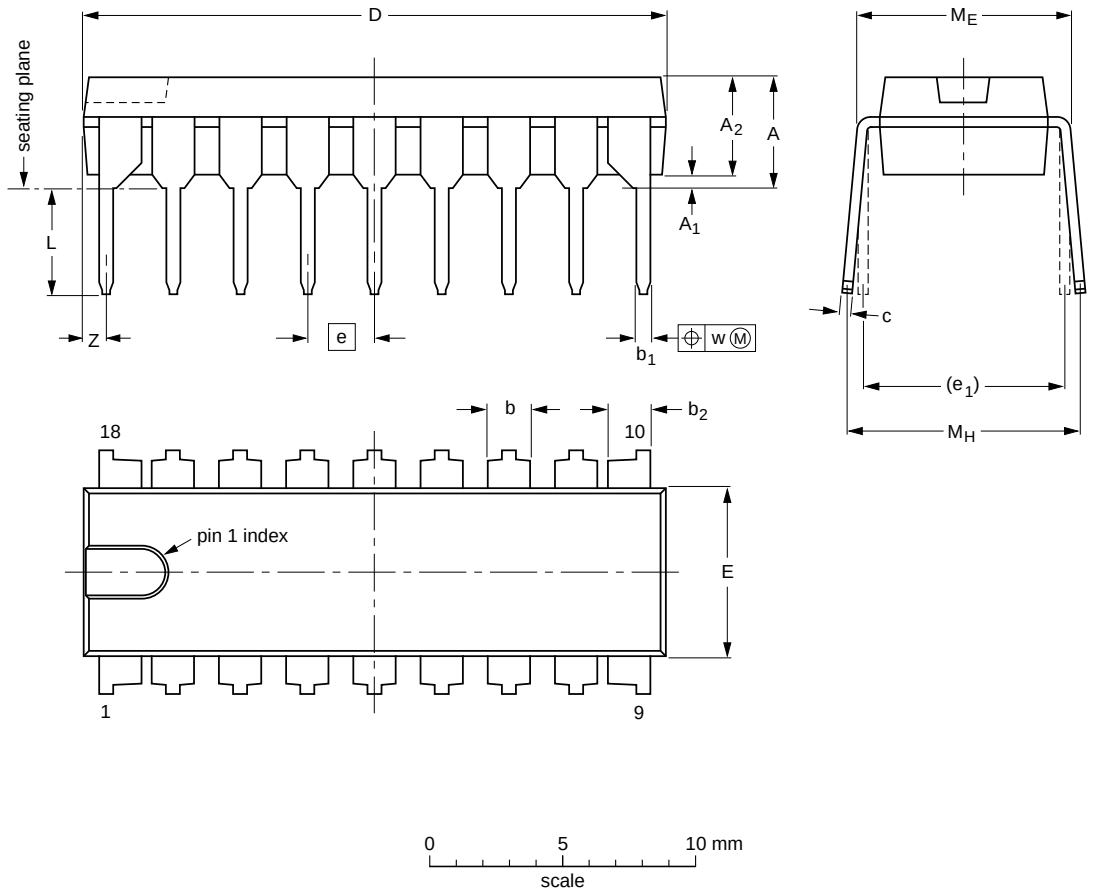


Fig.4 Application circuit diagram.

PACKAGE OUTLINE

DIP18: plastic dual in-line package; 18 leads (300 mil) **SOT102-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	1.40 1.14	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	0.85
inches	0.19	0.020	0.15	0.055 0.044	0.021 0.015	0.055 0.044	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.033

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT102-1						~~93-10-14~~ 95-01-23

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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