DATA SHEET

TDA4663T
Baseband delay line

Product specification
Supersedes data of September 1993
File under Integrated Circuits, IC02

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Philips
Semiconductors

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Baseband delay line TDA4663T

FEATURES

- Two delay lines, using the switched-capacitor technique, for a delay time of one horizontal line (1H) minus 55 ns (64 μs – 55 ns)
- Adjustment-free application
- Handles negative or positive colour-difference input signals
- Clamping of AC-coupled input signals [mostly colour-difference signals ±(R–Y) and ±(B–Y)]
- VCO without external components
- 3 MHz internal clock signal derived from a 6 MHz CCO, line-locked by the sandcastle pulse (64 μs line)
- Sample-and-hold circuits and low-pass filters to suppress the 3 MHz clock signal
- Output buffer amplifiers.

GENERAL DESCRIPTION

The TDA4663T is an integrated baseband delay line circuit with a delay time of one horizontal line (1H) minus 55 ns (64 μs – 55 ns).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{P1}	analog supply voltage (pin 9)	4.75	5	5.25	V
V_{P2}	digital supply voltage (pin 1)	4.75	5	5.25	V
$I_{P(tot)}$	total supply current	–	5.9	7.0	mA
$V_{i(p-p)}$	input signal PAL/NTSC (peak-to-peak value)				
	±(R–Y); pin 16	–	1.3	–	V
	±(B–Y); pin 14	–	1.3	–	V
G_v	gain $\frac{V_o}{V_i}$ of colour-difference output signals for PAL and NTSC				
	$\frac{V_{11}}{V_{16}}$	–1	0	+1	dB
	$\frac{V_{12}}{V_{14}}$	–1	0	+1	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4663T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

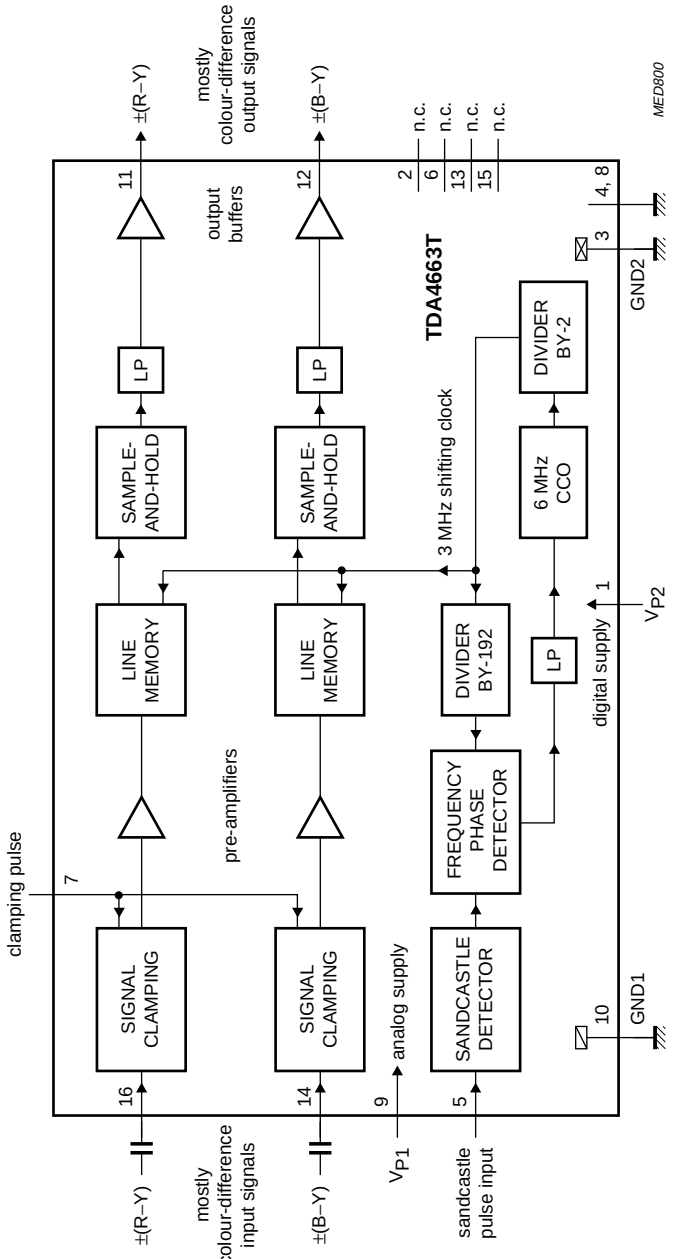


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P2}	1	supply voltage for digital part (+5 V)
n.c.	2	not connected
GND2	3	ground for digital part (0 V)
i.c.	4	internally connected
SAND	5	sandcastle pulse input
n.c.	6	not connected
V_{CL}	7	clamping pulse input
i.c.	8	internally connected
V_{P1}	9	supply voltage for analog part (+5 V)
GND1	10	ground for analog part (0 V)
$V_{o(R-Y)}$	11	±(R–Y) output signal
$V_{o(B-Y)}$	12	±(B–Y) output signal
n.c.	13	not connected
$V_{i(B-Y)}$	14	±(B–Y) input signal
n.c.	15	not connected
$V_{i(R-Y)}$	16	±(R–Y) input signal

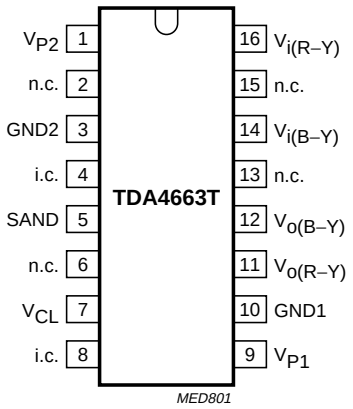


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). Ground pins 3 and 10 connected together.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 9)		–0.5	+7	V
V_{P2}	supply voltage (pin 1)		–0.5	+7	V
V_5	voltage on pin 5		–0.5	V_P + 1.0	V
V_n	voltage on pins 7, 11, 12, 14 and 16		–0.5	V_P	V
I_n	current on pins 7, 11 and 12		–	20	mA
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		–20	+70	°C
P_{tot}	total power dissipation		–	100	mW
V_{es}	electrostatic handling for all pins	note 1	–	±500	V

Note

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	220	K/W

CHARACTERISTICS

V_P = 5.0 V; input signals as specified in characteristics with 75% colour bars; super-sandcastle frequency of 15.625 kHz; T_{amb} = 25 °C; measurements taken in Fig.3; unless otherwise specified.

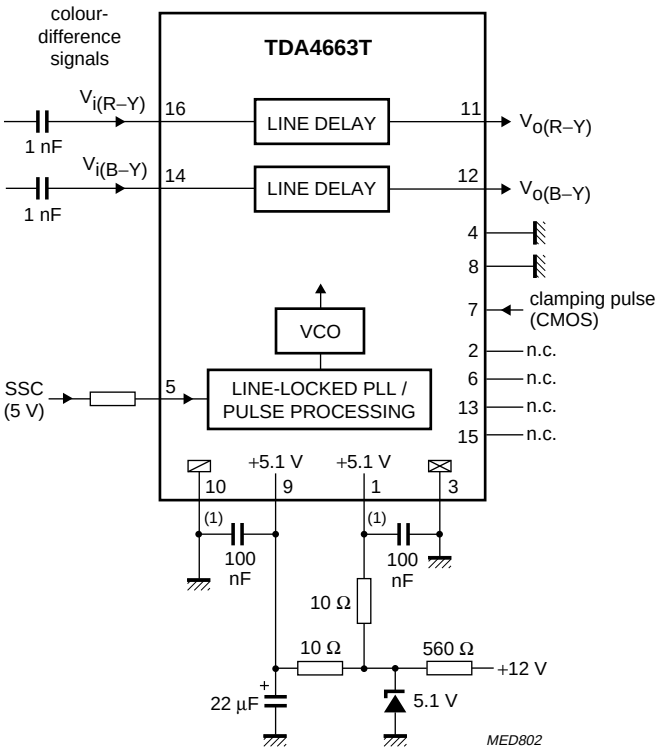
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	analog supply voltage (pin 9)		4.75	5	5.25	V
V_{P2}	digital supply voltage (pin 1)		4.75	5	5.25	V
I_{P1}	supply current		–	5.1	5.9	mA
I_{P2}	supply current		–	0.8	1.1	mA
Colour-difference input signals						
$V_{i(p-p)}$	input signal (peak-to-peak value)					
	pin 16		–	1.3	–	V
	pin 14		–	1.3	–	V
$V_{i(max)(p-p)}$	maximum symmetrical input signal (peak-to-peak value)					
	pin 16	before clipping	1.6	–	–	V
	pin 14	before clipping	1.6	–	–	V
$I_{14, 16}$	input leakage current (during picture content)		0.06	0.085	0.1	µA
$R_{14, 16}$	input resistance during clamping		–	–	40	kΩ
$C_{14, 16}$	input capacitance		–	–	10	pF
$V_{14, 16}$	input clamping voltage	proportional to V_P	1.3	1.5	1.7	V
Colour-difference output signals						
$V_{o(p-p)}$	output signal (peak-to-peak value)					
	pin 11		–	1.3	–	V
	pin 12		–	1.3	–	V
V_{11}/V_{12}	ratio of output amplitudes at equal input signals	$V_{i14, 16}$ = 665 mV (p-p)	–0.4	0	+0.4	dB
$V_{11, 12}$	DC output voltage	proportional to V_P	2.5	2.9	3.3	V
$R_{11, 12}$	output resistance		–	300	400	Ω
G_v	voltage gain $\frac{V_o}{V_i}$		–1	0	+1	dB
$V_{n(rms)}$	noise voltage (RMS value; pins 11 and 12)	$V_{i14, 16}$ = 0 V; note 1	–	–	1.2	mV
S/N(W)	weighted signal-to-noise ratio (pins 11 and 12)	V_o = 1 V (p-p); note 1	–	54	–	dB
t_j	jitter of output signal to external sandcastle reference V_5		–	–	20	ns
$\alpha_{ct(11, 12)}$	crosstalk between channels	V_{14} = 0 V; R_S = 300 Ω; V_{11} = 1.35 V (p-p)	30	–	–	dB
$\alpha_{ct(12, 11)}$	crosstalk between channels	V_{16} = 0 V; R_S = 300 Ω; V_{12} = 1.35 V (p-p)	30	–	–	dB
$\alpha_{ct(14, 12)}$	crosstalk direct from input to output signal	V_{16} = 0 V; R_S = 300 Ω; V_{14} = 1.35 V (p-p)	30	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\alpha_{ct(16, 11)}$	crosstalk direct from input to output signal	V_{14} = 0 V; R_S = 300 Ω; V_{16} = 1.35 V (p-p)	30	–	–	dB
SVRR	supply voltage ripple rejection $\Delta V_{11, 12}/V_R$	V_R = 100 mV (p-p); f_R = 10 Hz to 1 kHz; $V_{11, 12}$ = 1.35 V (p-p)	34	–	–	dB
$V_{11, 12(p-p)}$	clamping offset during H-clamp (peak-to-peak value)	$V_{14} = V_{16}$ = 0 V; R_S = 300 Ω	–	–	5	mV
$V_{11, 12(p-p)}$	unwanted signals (line-locked) (peak-to-peak value)	$V_{14} = V_{16}$ = 0 V; active video; R_S = 300 Ω				
	residual clock (3 MHz)		–	–	6.25	mV
	meander		–	–	1.5	mV
	needles		–	–	2.5	mV
t_d	line delay time	for PAL signals	64 – 0.125	64 – 0.055	64 + 0.015	µs
		for NTSC signals	63.555 – 0.125	63.555 – 0.055	63.555 + 0.015	µs
Sandcastle pulse input (pin 5)						
f_{BK}	burst-key frequency/sandcastle frequency		14.2	15.625	17.0	kHz
V_5	top pulse voltage	note 2	4.0	–	V_P + 1.0	V
t_{BK}	top pulse duration		–	2.5	–	µs
V_{slice}	internal slicing level		V_5 – 1.0	–	V_5 – 0.5	V
I_i	input current		–	–	10	µA
C_i	input capacitance		–	–	10	pF
t_{li}	lock-in time for PLL		–	–	1	ms
Clamping pulse input (pin 7)						
V_{clamp}	clamping pulse ON		3.5	V_P – 0.1	V_P	V
	clamping pulse OFF		–0.5	+0.1	+1.5	V
I_i	input current		–	–	10	µA
C_i	input capacitance		–	–	10	pF
t_{clamp}	clamping pulse duration		0.1	2	3	µs
t_r	rise time		10	–	–	ns
t_f	fall time		10	–	–	ns

Notes

1. Noise voltage at f = 10 kHz to 1 MHz; R_S < 300 Ω.
2. The leading edge of the burst-key pulse or H-blanking pulse is used for timing.

APPLICATION INFORMATION

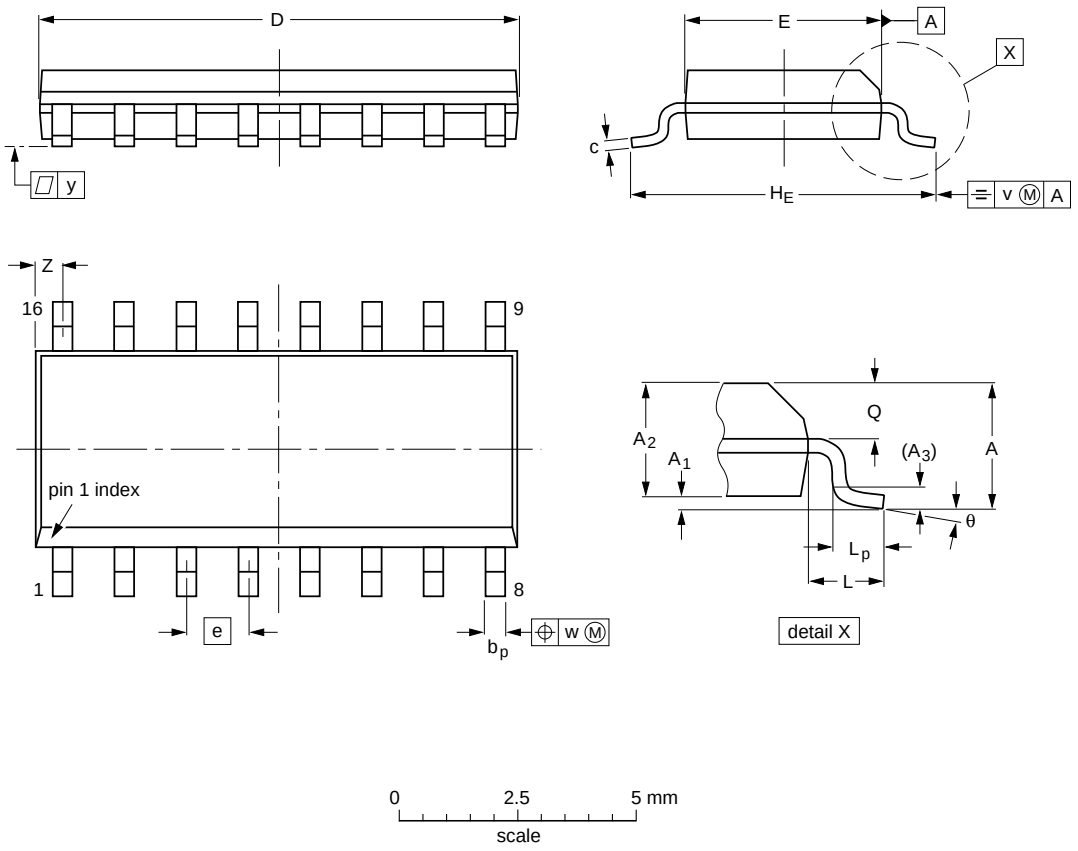


(1) Positioned close to pins.

Fig.3 Application circuit.

PACKAGE OUTLINE

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23