DATA SHEET

TDA4665
Baseband delay line

Product specification
Supersedes data of 1995 Oct 30
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

Baseband delay line TDA4665

FEATURES

- Two comb filters, using the switched-capacitor technique, for one line delay time (64 μs)
- Adjustment-free application
- No crosstalk between SECAM colour carriers (diaphoty)
- Handles negative or positive colour-difference input signals
- Clamping of AC-coupled input signals (±(R–Y) and ±(B–Y))
- VCO without external components
- 3 MHz internal clock signal derived from a 6 MHz CCO, line-locked by the sandcastle pulse (64 μs line)
- Sample-and-hold circuits and low-pass filters to suppress the 3 MHz clock signal
- Addition of delayed and non-delayed output signals
- Output buffer amplifiers
- Comb filtering functions for NTSC colour-difference signals to suppress cross-colour.

GENERAL DESCRIPTION

The TDA4665 is an integrated baseband delay line circuit with one line delay. It is suitable for decoders with colour-difference signal outputs ±(R–Y) and ±(B–Y).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{P1}	analog supply voltage (pin 9)	4.5	5	6	V
V_{P2}	digital supply voltage (pin 1)	4.5	5	6	V
$I_{P(tot)}$	total supply current	–	5.5	7.0	mA
$V_{i(p-p)}$	±(R–Y) input signal PAL/NTSC (peak-to-peak value; pin 16)	–	525	–	mV
	±(B–Y) input signal PAL/NTSC (peak-to-peak value; pin 14)	–	665	–	mV
	±(R–Y) input signal SECAM (peak-to-peak value; pin 16)	–	1.05	–	V
	±(B–Y) input signal SECAM (peak-to-peak value; pin 14)	–	1.33	–	V
G_v	gain V_o / V_i of colour-difference output signals				
	V_{11} / V_{16} for PAL and NTSC	5.3	5.8	6.3	dB
	V_{12} / V_{14} for PAL and NTSC	5.3	5.8	6.3	dB
	V_{11} / V_{16} for SECAM	–0.6	–0.1	+0.4	dB
	V_{12} / V_{14} for SECAM	–0.6	–0.1	+0.4	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4665	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
TDA4665T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

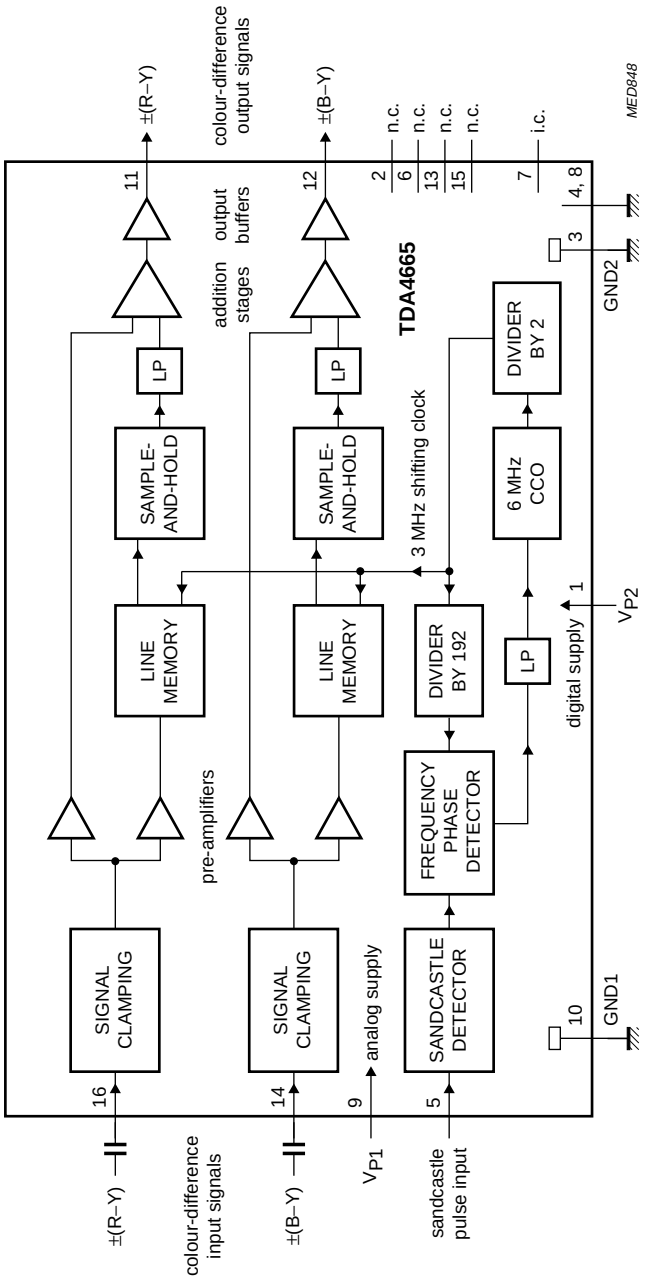


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P2}	1	+5 V supply voltage for digital part
n.c.	2	not connected
GND2	3	ground for digital part (0 V)
i.c.	4	internally connected
SAND	5	sandcastle pulse input
n.c.	6	not connected
i.c.	7	internally connected
i.c.	8	internally connected
V_{P1}	9	+5 V supply voltage for analog part
GND1	10	ground for analog part (0 V)
$V_{o(R-Y)}$	11	±(R–Y) output signal
$V_{o(B-Y)}$	12	±(B–Y) output signal
n.c.	13	not connected
$V_{i(B-Y)}$	14	±(B–Y) input signal
n.c.	15	not connected
$V_{i(R-Y)}$	16	±(R–Y) input signal

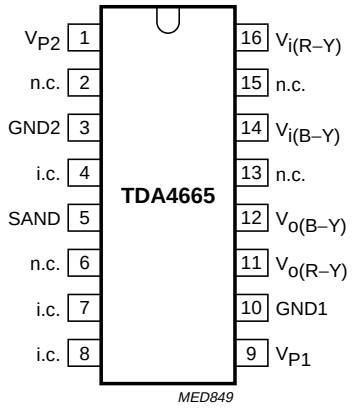


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). Ground pins 3 and 10 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	analog supply voltage (pin 9)	–0.5	+7	V
V_{P2}	digital supply voltage (pin 1)	–0.5	+7	V
V_5	voltage on pin 5	–0.5	V_P + 1.0	V
V_n	voltage on pins 11, 12, 14 and 16	–0.5	V_P	V
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	0	70	°C
V_{ESD}	electrostatic handling for all pins; note 1	–	±500	V

Note

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air		
	SOT38-4	75	K/W
	SOT109-1	220	K/W

CHARACTERISTICS

V_P = 5.0 V; input signals as specified in characteristics with 75% colour bars; super-sandcastle frequency of 15.625 kHz; T_{amb} = 25 °C; measurements taken in Fig.3; unless otherwise specified.

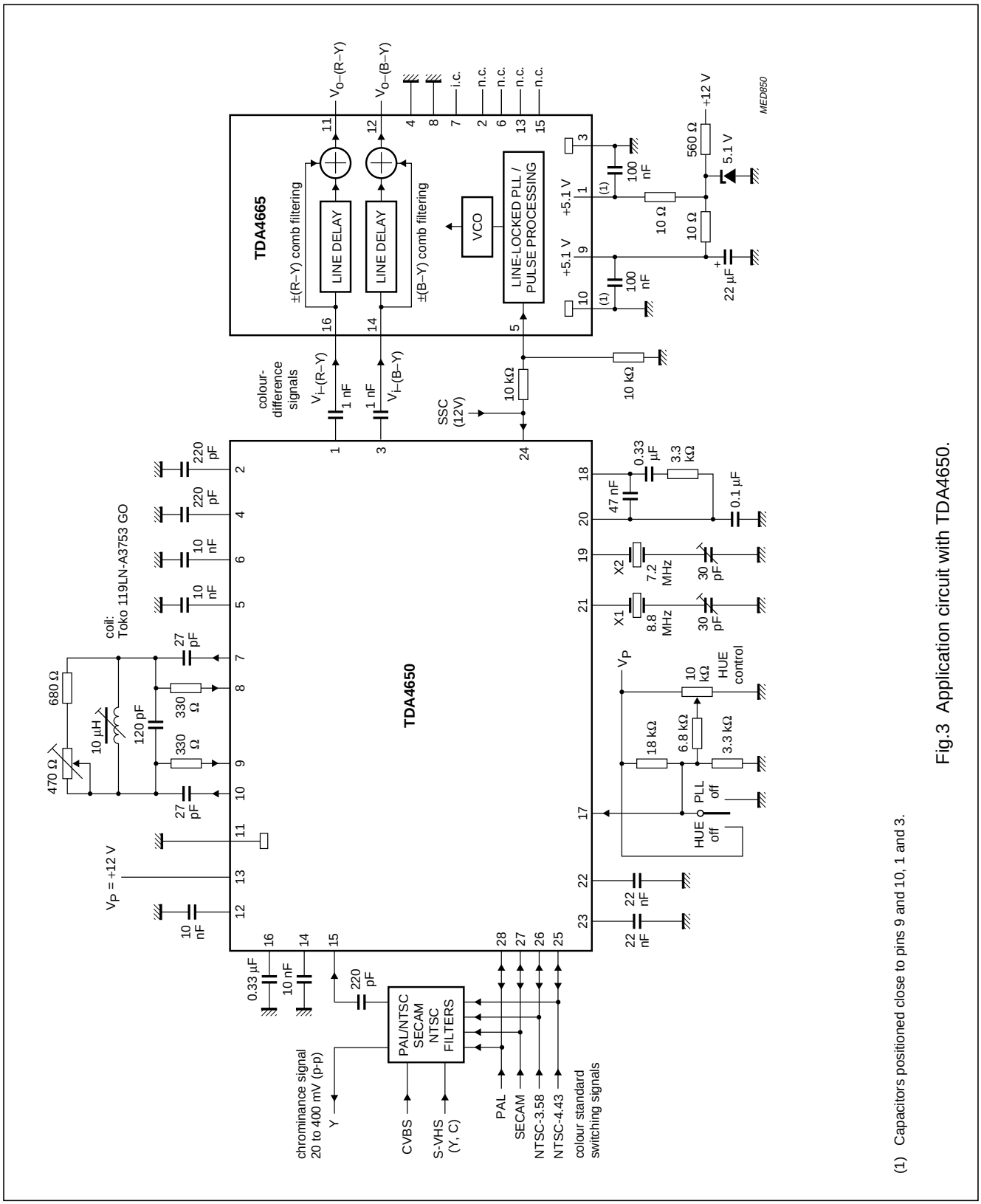
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{P1}	analog supply voltage (pin 9)		4.5	5	6	V
V_{P2}	digital supply voltage (pin 1)		4.5	5	6	V
I_{P1}	analog supply current		–	4.8	6.0	mA
I_{P2}	digital supply current		–	0.7	1.0	mA
Colour-difference input signals						
$V_{i(p-p)}$	input signal (peak-to-peak value)	note 1				
	±(R–Y) PAL and NTSC (pin 16)		–	525	–	mV
	±(B–Y) PAL and NTSC (pin 14)		–	665	–	mV
	±(R–Y) SECAM (pin 16)		–	1.05	–	V
	±(B–Y) SECAM (pin 14)		–	1.33	–	V
$V_{i(max)(p-p)}$	maximum symmetrical input signal (peak-to-peak value)					
	±(R–Y) or ±(B–Y) for PAL and NTSC	before clipping	1	–	–	V
	±(R–Y) or ±(B–Y) for SECAM	before clipping	2	–	–	V
$R_{14, 16}$	input resistance during clamping		–	–	40	kΩ
$C_{14, 16}$	input capacitance		–	–	10	pF
$V_{14, 16}$	input clamping voltage	proportional to V_P	1.3	1.5	1.7	V
Colour-difference output signals						
$V_{o(p-p)}$	output signal (peak-to-peak value)					
	±(R–Y) on pin 11	all standards	–	1.05	–	V
	±(B–Y) on pin 12	all standards	–	1.33	–	V
V_{11}/V_{12}	ratio of output amplitudes at equal input signals	$V_{i(14,16)(p-p)}$ = 1.33 V	–0.4	0	+0.4	dB
$V_{11, 12}$	DC output voltage	proportional to V_P	2.5	2.9	3.3	V
$R_{11, 12}$	output resistance		–	330	400	Ω
G_v	gain for PAL and NTSC	ratio V_o/V_i	5.3	5.8	6.3	dB
	gain for SECAM	ratio V_o/V_i	–0.6	–0.1	+0.4	dB
V_n/V_{n+1}	ratio of delayed to non-delayed output signals (pins 11 and 12)	$V_{i(14,16)(p-p)}$ = 1.33 V; SECAM signals	–0.1	0	+0.1	dB
$V_{n(rms)}$	noise voltage (RMS value; pins 11 and 12)	$V_{i(14,16)}$ = 0 V; note 2	–	–	1.2	mV
$V_{(11,12)(p-p)}$	unwanted signals (line-locked) (peak-to-peak value)	$V_{i(14,16)}$ = 0 V; active video; R_S = 300 Ω				
	meander		–	–	5	mV
	spikes		–	–	10	mV
S/N(W)	weighted signal-to-noise ratio (pins 11 and 12)	$V_{o(p-p)}$ = 1 V; note 2	–	54	–	dB
Δt_d	time difference between non-delayed and delayed output signals (pins 11 and 12)		63.94	64	64.06	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_d	delay of non-delayed signals		40	60	80	ns
t_{tr}	transient time of delayed signal on pins 11 respectively 12	300 ns transient of SECAM signal	–	350	–	ns
	transient time of non-delayed signal on pins 11 respectively 12	300 ns transient of SECAM signal	–	320	–	ns
Sandcastle pulse input (pin 5)						
f_{BK}	burst-key frequency/sandcastle frequency		14.2	15.625	17.0	kHz
V_5	top pulse voltage	note 3	4.0	–	V_P + 1.0	V
V_{slice}	internal slicing level		V_5 – 1.0	–	V_5 – 0.5	V
I_5	input current		–	–	10	μA
C_5	input capacitance		–	–	10	pF

Notes

1. For SECAM the signal must be blanked line-sequentially. The blanking level must be equal to the non-colour signal. For SECAM, PAL and NTSC the input signal must be equal to the non-colour signal during the internal clamping of TDA4665 (3 to 1 μs before the leading edge of the top pulse of V_5).
2. Noise voltage at f = 10 kHz to 1 MHz; R_S < 300 Ω.
3. The leading edge of the burst-key pulse or top pulse is used for timing.

APPLICATION INFORMATION

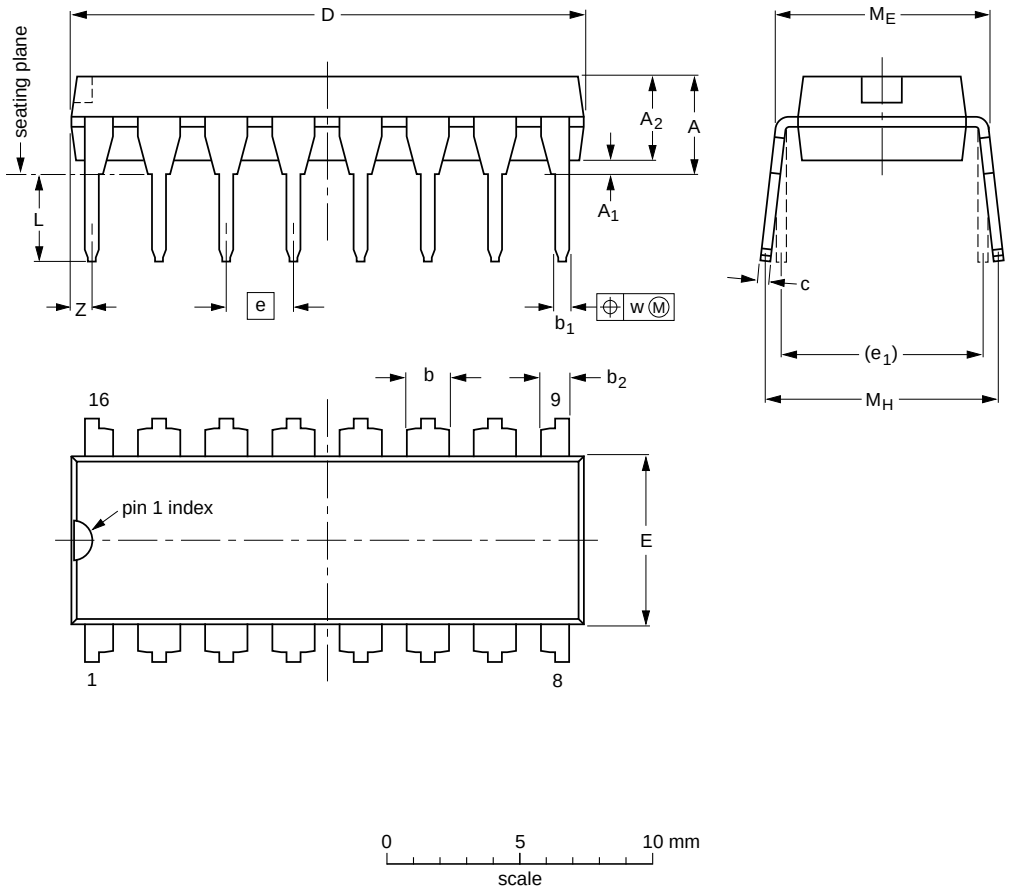


(1) Capacitors positioned close to pins 9 and 10, 1 and 3.

Fig.3 Application circuit with TDA4650.

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil) SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

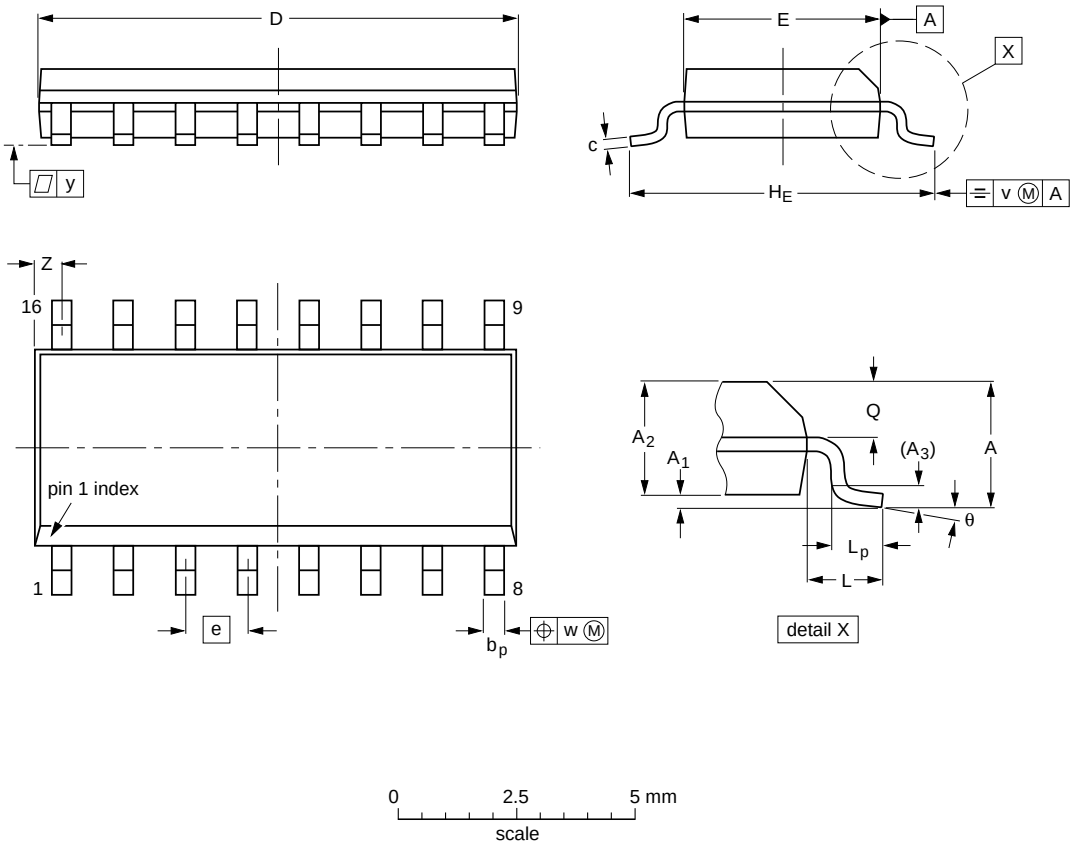
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23