DATA SHEET

TDA4685
Video processor with automatic cut-off control

Preliminary specification
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PHILIPS

Video processor with automatic cut-off control

TDA4685

FEATURES

- Operates from an 8 V DC supply
- Black level clamping of the colour difference, luminance and RGB input signals with coupling-capacitor DC level storage
- Two analog RGB inputs, selected either by fast switch signals or the I²C-bus; brightness and contrast control of these RGB inputs
- Saturation, contrast, brightness and white adjustment via I²C-bus
- Same RGB output black levels for Y/CD and RGB input signals
- Timing pulse generation from either a 2- or 3-level sandcastle pulse for clamping, vertical synchronization and cut-off timing pulses
- Automatic cut-off control or clamped output selectable via I²C-bus
- Automatic cut-off control with picture tube leakage current compensation
- Cut-off measurement pulses after end of the vertical blanking pulse or end of an extra vertical flyback pulse
- Two switch-on delays to prevent discolouration before steady-state operation
- Average beam current and peak drive limiting
- PAL/SECAM or NTSC matrix selection via I²C-bus
- Emitter-follower RGB output stages to drive the video output stages
- I²C-bus controlled DC output e. g. for hue-adjust of NTSC (multistandard) decoders

GENERAL DESCRIPTION

The TDA4685 is a monolithic, integrated circuit with a luminance and a colour difference interface for video processing in TV receivers.

Its primary function is to process the luminance and colour difference signals from a colour decoder which is equipped e. g. with the multistandard decoder TDA4655 or TDA9160 plus delayline TDA4661 and the Picture Signal Improvement (PSI) IC TDA467X or from a Feature Module. The required input signals are:

- luminance and negative colour difference signals
- 2- or 3-level sandcastle pulse for internal timing pulse generation
- I²C-bus data and clock signals for microprocessor control.

Two sets of analog RGB colour signals can also be inserted, e.g. one from a peritelevision connector and the other from an on-screen display generator. The TDA4685 has I²C-bus control of all parameters and functions with automatic cut-off control of the picture tube cathode currents. It provides RGB output signals for the video output stages.

The TDA4685 is a simplified, pin compatible (except pin 18) version of the TDA4680. The module address via the I²C-bus can be used for both ICs; where a function is not included in the TDA4685 then the I²C-bus command is not executed. The differences with the TDA4680 are:

- no automatic white level control; the white levels are determined directly by the I²C-bus data
- RGB reference levels for automatic cut-off control are not adjustable via I²C-bus
- clamping delay is fixed
- only contrast and brightness adjust for the RGB input signals
- the measurement lines are triggered either by the trailing edge of the vertical component of the sandcastle pulse or by the trailing edge of an optional external vertical flyback pulse (on pin 18), according to which occurs first.

The TDA4686 is like TDA4685 but intended for double line frequency application.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)	7.2	8.0	8.8	V
I_P	supply current (pin 5)	–	60	–	mA
$V_{8(p-p)}$	luminance input (peak-to-peak value)	–	0.45	–	V
$V_{6(p-p)}$	−(B−Y) input (peak-to-peak value)	–	1.33	–	V
$V_{7(p-p)}$	−(R−Y) input (peak-to-peak value)	–	1.05	–	V
V_{14}	three-level sandcastle pulse				
	H +V	–	2.5	–	V
	H	–	4.5	–	V
	BK	–	8.0	–	V
	two-level sandcastle pulse				
	H + V	–	2.5	–	V
	BK	–	4.5	–	V
V_i	RGB input signals at pins 2, 3, 4, 10, 11 and 12 (black-to-white value)	–	0.7	–	V
$V_{o(p-p)}$	RGB outputs at pins 24, 22 and 20 (peak-to-peak value)	–	2.0	–	V
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4685	28	DIL	plastic	SOT117(1)

Note

1. SOT117-1; 1996 November 25.

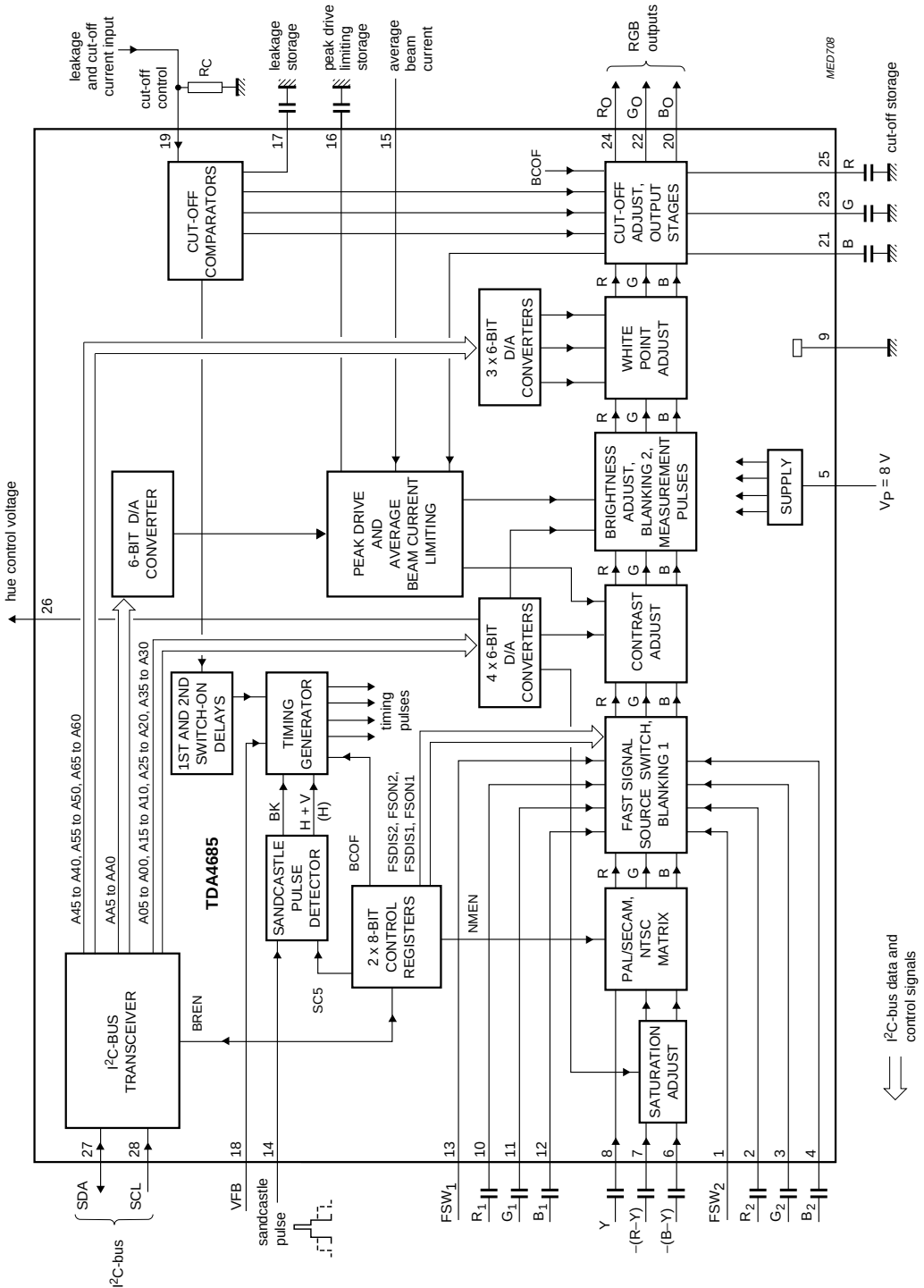


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FSW_2	1	fast switch 2 input
R_2	2	red input 2
G_2	3	green input 2
B_2	4	blue input 2
V_P	5	supply voltage
–(B–Y)	6	colour difference input –(B–Y)
–(R–Y)	7	colour difference input –(R–Y)
Y	8	luminance input
GND	9	ground
R_1	10	red input 1
G_1	11	green input 1
B_1	12	blue input 1
FSW_1	13	fast switch 1 input
SC	14	sandcastle pulse input
BCL	15	average beam current limiting input
C_{PDL}	16	storage capacitor for peak drive limiting
C_L	17	storage capacitor for leakage current
V_{FB}	18	vertical flyback pulse input
CI	19	cut-off measurement input
B_O	20	blue output
C_B	21	blue cut-off storage capacitor
G_O	22	green output
C_G	23	green cut-off storage capacitor
R_O	24	red output
C_R	25	red cut-off storage capacitor
HUE	26	hue control output
SDA	27	I^2C-bus serial data input / acknowledge output
SCL	28	I^2C-bus serial clock input

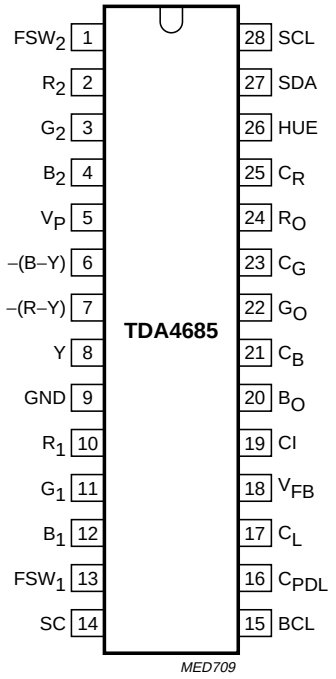


Fig.2 Pin configuration.

I²C-BUS CONTROL

The I²C-bus transmitter provides the data bytes to select and adjust the following functions and parameters:

- brightness adjust
- saturation adjust
- contrast adjust
- DC output e. g. for hue control
- RGB gain adjust
- peak drive limiting level adjust
- selects either 3-level or 2-level (5 V) sandcastle pulse
- enables cut-off control / enables output clamping
- selects either PAL/SECAM or NTSC matrix
- enables/disables synchronization of the execution of I²C-bus commands with the vertical blanking interval
- enables Y-CD, RGB1 or RGB2 input.

I²C-BUS TRANSMITTER AND DATA TRANSFER

I²C-bus specification

The I²C-bus is a bi-directional, two-wire, serial data bus for intercommunication between ICs in an equipment. The microcontroller transmits data to the I²C-bus receiver in the TDA4685 over the serial data line SDA (pin 27) synchronized by the serial clock line SCL (pin 28).
Both lines are normally connected to a positive voltage supply through pull-up resistors. Data is transferred when the SCL line is LOW. When SCL is HIGH the serial data line SDA must be stable. A HIGH-to-LOW transition of the SDA line when SCL is HIGH is defined as a start bit.
A LOW-to-HIGH transition of the SDA line when SCL is HIGH is defined as a stop bit. Each transmission must start with a start bit and end with a stop bit. The bus is busy after a start bit and is only free again after a stop bit has been transmitted.

I²C-bus receiver

(microcontroller write mode)
Each transmission to the I²C-bus receiver consists of at least three bytes following the start bit. Each byte is acknowledged by an acknowledge bit immediately following each byte. The first byte is the Module ADdress (MAD) byte, also called slave address byte. This includes the module address, 1000100_2 for the TDA4685. The TDA4685 is a slave receiver ($R/\overline{W} = 0$), therefore the module address byte is 10001000_2 (88 Hex), see Fig.3.
The length of a data transmission is unrestricted, but the module address and the correct sub-address must be transmitted before the data byte(s). The order of data transmission is shown in Fig.4 and Fig.5. Without auto-increment (BREN = 0 or 1) the Module ADdress (MAD) byte is followed by a Sub-ADdress (SAD) byte and one data byte only (Fig.4).

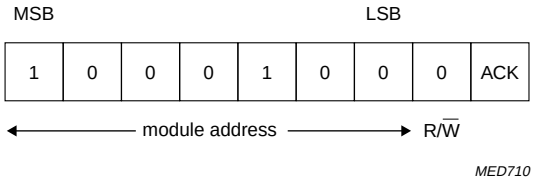


Fig.3 The module address byte.

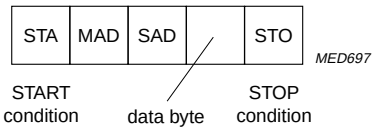


Fig.4 Data transmission without auto-increment (BREN = 0 or 1).

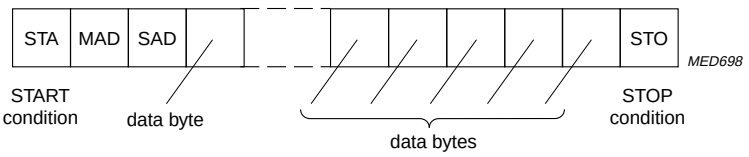


Fig.5 Data transmission with auto-increment (BREN = 0).

Auto-increment

The auto-increment format enables quick slave receiver initialization by one transmission, when the I^2C-bus control bit BREN = 0 (see control register bits of Table 1). If BREN = 1 auto-increment is not possible. If the auto-increment format is selected, the MAD byte is followed by an SAD byte and by the data bytes of consecutive sub-addresses (Fig.5).
All sub-addresses from 00 to 0F are automatically incremented, the sub-address counter wraps round from 0F to 00. Reserved sub-addresses 07, 08, 09, 0B, 0E and 0F are treated as legal but have no effect. Sub-addresses outside the range 00 and 0F are not acknowledged by the device. The sub-addresses are stored in the TDA4685 to address the following parameters and functions, see Table 1:

- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- peak drive limiting adjust
- control register functions.

The data bytes (D7-D0 of Table 1) provide the data of the parameters and functions for video processing.

Control register 1

NMEN (NTSC-Matrix ENable):
0 = PAL/SECAM matrix
1 = NTSC matrix.

BREN (Buffer Register ENable):
0 = new data is executed as soon as it is received
1 = data is stored in buffer registers and is transferred to the data registers during the next vertical blanking interval.
The I^2C-bus receiver does not accept any new data until this data is transferred into the data registers.

SC5 (SandCastle 5 V):
0 = 3-level sandcastle pulse
1 = 2-level (5 V) sandcastle pulse.

Control register 2

FSON2 - Fast Switch 2 ON
FSDIS2 - Fast Switch 2 DISable
FSON1 - Fast Switch 1 ON
FSDIS1 - Fast Switch 1 DISable
The RGB input signals are selected by FSON2 and FSON1 or FSW_2 and FSW_1:

- FSON2 has priority over FSON1;
- FSW_2 has priority over FSW_1;
- FSDIS1 and FSDIS2 disable FSW_1 and FSW_2 (see Table 2).

BCOF - Black level Control OFf:
0 = automatic cut-off control enabled
1 = automatic cut-off control disabled; RGB outputs are clamped to fixed DC levels.

When the supply voltage has dropped below approximately 6.0 V (usually occurs when the TV receiver is switched on or the supply voltage is interrupted) all data and function bits are set to $01_{Hex.}$

Table 1 Sub-address (SAD) and data bytes(1).

FUNCTION	SAD	MSB			DATA BYTE				LSB
	(HED)	7	6	5	4	3	2	1	0
Brightness	00	0	0	A05	A04	A03	A02	A01	A00
Saturation	01	0	0	A15	A14	A13	A12	A11	A10
Contrast	02	0	0	A25	A24	A23	A22	A21	A20
Hue control voltage	03	0	0	A35	A34	A33	A32	A31	A30
Red gain	04	0	0	A45	A44	A43	A42	A41	A40
Green gain	05	0	0	A55	A54	A53	A52	A51	A50
Blue gain	06	0	0	A65	A64	A63	A62	A61	A60
Reserved	07	0	0	x	x	x	x	x	x
Reserved	08	0	0	x	x	x	x	x	x
Reserved	09	0	0	x	x	x	x	x	x
Peak drive limit	0A	0	0	AA5	AA4	AA3	AA2	AA1	AA0
Reserved	0B	x	x	x	x	x	x	x	x
Control register 1	0C	SC5	x	BREN	x	NMEN	x	x	x
Control register 2	0D	x	x	x	BCOF	FSDIS2	FSON2	FSDIS1	FSON1
Reserved	0E	x	x	x	x	x	x	x	x
Reserved	0F	x	x	x	x	x	x	x	x

Note to Table 1

1. X is ‘don’t care’, but for software compatibility with other or future video ICs it is recommended to set all ‘X’ to ‘0’.

Table 2 Signal input selection by the fast source switches(1).

I^2C-BUS CONTROL BITS				ANALOG SWITCH SIGNALS		INPUT SELECTED		
FSON2	FSDIS2	FSON1	FSDIS1	FSW_2 (pin 1)	FSW_1 (pin 13)	RGB_2	RGB_1	Y/CD
L	L	L	L	L	L			ON
				L	H		ON	
				H	X	ON		
L	L	L	H	L	X			ON
				H	X	ON		
L	L	H	X	L	X		ON	
				H	X	ON		
L	H	L	L	X	L			ON
				X	H		ON	
L	H	L	H	X	X			ON
L	H	H	X	X	X		ON	
H	X	X	X	X	X	ON		

Note to Table 2

1. Where L is a logic LOW (< 0.4 V), H is a logic HIGH (> 0.9 V), X is ‘don’t care’, and ON is the selected input signal.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 5)	–	8.8	V
V_I	input voltage (pins 1 to 8, 10 to 13, 16, 21, 23 and 25)	–0.1	V_P	V
	input voltage (pins 15, 18 and 19)	–0.7	V_P+ 0.7	V
	input voltage (pins 27 and 28)	–0.1	8.8	V
V_{14}	sandcastle pulse voltage	–0.7	V_P+5.8	V
I_{AV}	average current (pins 20, 22 and 24)	–10	4	mA
I_M	peak current (pins 20, 22 and 24)	–20	4	mA
I_{26}	output current	–8	0.6	mA
T_{stg}	storage temperature	–20	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
P_{tot}	total power dissipation	–	1.2	W

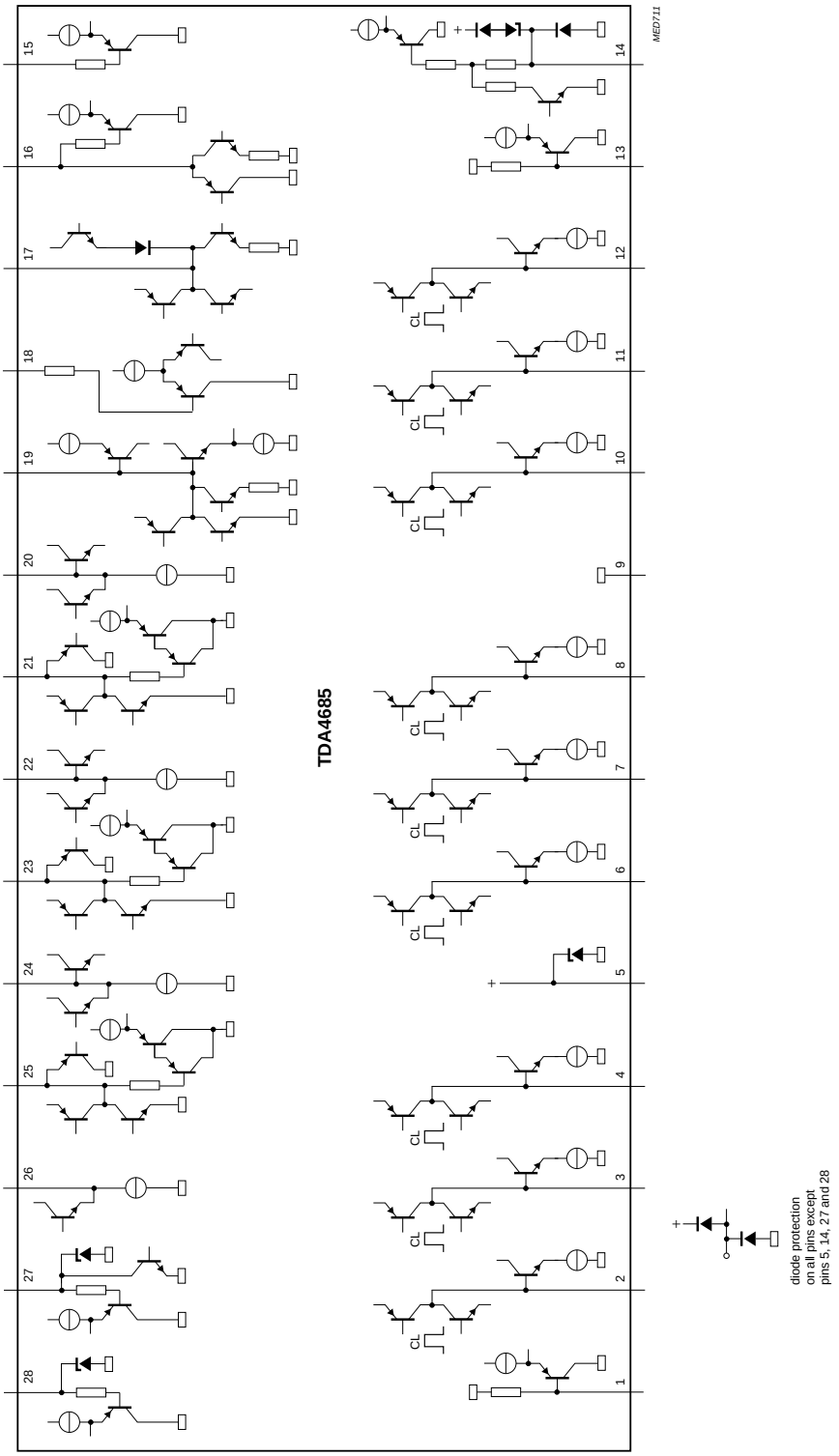


Fig.6 Internal circuits.

CHARACTERISTICS

All voltages are measured in test circuit of Fig.7 with respect to GND (pin 9); V_P = 8.0 V; T_{amb} =+25 °C:
- at nominal signal amplitudes (black-to-white) at output pins 24, 22 and 20,
- at nominal settings of brightness, contrast, saturation and white level control,
- without beam current or peak drive limiting; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)		7.2	8.0	8.8	V
I_P	supply current (pin 5)		–	60	–	mA
Colour difference inputs						
$V_{6(p-p)}$	–(B–Y) input (peak-to-peak value)	notes 1 and 2	–	1.33	–	V
$V_{7(p-p)}$	–(R–Y) input (peak-to-peak value)	notes 1 and 2	–	1.05	–	V
$V_{6,7}$	internal DC bias voltage	at black level clamping	–	4.1	–	V
$I_{6,7}$	input current	during line scan	–	–	±0.1	µA
		at black level clamping	±100	–	–	µA
$R_{6,7}$	input resistance		10	–	–	MΩ
Luminance/sync (VBS)						
$V_{i(p-p)}$	luminance input at pin 8 (peak-to-peak value)	note 2	–	0.45	–	V
V_8	internal DC bias voltage	at black level clamping	–	4.1	–	V
I_8	input current	during line scan	–	–	±0.1	µA
		at black level clamping	±100	–	–	µA
R_8	input resistance		10	–	–	MΩ
R_1,G_1 and B_1 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 10, 11 and 12 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{10/11/12}$	internal DC bias voltage	at black level clamping	–	5.7	–	V
$I_{10/11/12}$	input current	during line scan	–	–	±0.1	µA
		at black level clamping	±100	–	–	µA
$R_{10/11/12}$	input resistance		10	–	–	MΩ
R_2, G_2 and B_2 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 2, 3 and 4 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{2/3/4}$	internal DC bias voltage	at black level clamping	–	5.7	–	V
$I_{2/3/4}$	input current	during line scan	–	–	±0.1	µA
		at black level clamping	±100	–	–	µA
$R_{2/3/4}$	input resistance		10	–	–	MΩ
PAL/SECAM and NTSC matrix (note 3)						
	PAL/SECAM matrix	control bit NMEN = 0				
	NTSC matrix	control bit NMEN = 1				

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fast signal switch FSW_1 to select Y, CD or R_1, G_1, B_1 inputs control bits FSDIS1, FSON1 (see Table 2)						
V_{13}	voltage to select Y and CD		–	–	0.4	V
	voltage range to select R_1, G_1, B_1		0.9	–	5.0	V
R_{13}	internal resistance to ground		–	4.0	–	kΩ
Δt	difference between transit times for signal switching and signal insertion		–	–	10	ns
Fast signal switch FSW_2 to select Y, CD / R_1, G_1, B_1 or R_2, G_2, B_2 inputs control bits FSDIS2, FSON2 (see Table 2)						
V_1	voltage to select Y, CD/R_1, G_1, B_1		–	–	0.4	V
	voltage range to select R_2, G_2, B_2		0.9	–	5.0	V
R_1	internal resistance to ground		–	4.0	–	kΩ
Δt	difference between transit times for signal switching and signal insertion		–	–	10	ns
Saturation adjust acts on –(R–Y) and –(B–Y) signals under I^2C-bus control, sub-address 01_{Hex} (bit resolution 1.5% of maximum saturation); data byte $3F_{Hex}$ for maximum saturation; data byte 23_{Hex} for nominal saturation; data byte 00_{Hex} for minimum saturation						
d_s	saturation below maximum	at 23_{Hex}	–	5	–	dB
		at 00_{Hex}; f = 100 kHz	–	50	–	dB
Contrast adjust acts on internal RGB signals under I^2C-bus control, sub-address 02_{Hex} (bit resolution 1.5% of maximum contrast); data byte $3F_{Hex}$ for maximum contrast; data byte 22_{Hex} for nominal contrast; data byte 00_{Hex} for minimum contrast						
d_c	contrast below maximum	at 22_{Hex}	–	5	–	dB
		at 00_{Hex}	–	22	–	dB
Brightness adjust acts on internal RGB signals under I^2C-bus control, sub-address 00_{Hex} (bit resolution 1.5% of maximum brightness); data byte $3F_{Hex}$ for maximum brightness; data byte 26_{Hex} for nominal brightness; data byte 00_{Hex} for minimum brightness						
d_{br}	black level shift of nominal signal amplitude referred to cut-off measurement level	at $3F_{Hex}$	–	30	–	%
		at 00_{Hex}	–	–50	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
White potentiometers, under I²C-bus control, sub-addresses 04_{Hex} (red), 05_{Hex} (green) and 06_{Hex} (blue); note 4. data byte $3F_{Hex}$ for maximum gain data byte 19_{Hex} for nominal gain data byte 00_{Hex} for minimum gain						
ΔG_v	relative to nominal gain:					
	increase of gain	at $3F_{Hex}$	–	50	–	%
	decrease of gain	at 00_{Hex}	–	50	–	%
RGB outputs pins 24, 22 and 20 (positive going output signals; peak drive limiter set = $3F_{Hex}$); note 5.						
$V_{o(b-w)}$	nominal output signal amplitudes (black-to-white value)		–	2	–	V
	maximum output signal amplitudes (black-to-white value)		3.0	–	–	V
ΔV_o	spread between RGB output signals		–	–	10	%
V_o	minimum output voltages		–	–	0.8	V
	maximum output voltages		6.8	–	–	V
$V_{24,22,20}$	voltage of cut-off measurement line = voltage during ultra-black	BCOF = 1 (output clamping)	2.3	2.5	2.7	V
I_{int}	internal current sources		–	5.0	–	mA
R_o	output resistance		–	20	–	Ω
Frequency response						
d	frequency response of Y path (from pin 8 to pins 24, 22, 20)	f = 10 MHz	–	–	3	dB
	frequency response of CD path (from pins 7 to 24 and 6 to 20)	f = 8 MHz	–	–	3	dB
	frequency response of RGB_1 path (from pins 10 to 24, 11 to 22 and 12 to 20)	f = 10 MHz	–	–	3	dB
	frequency response of RGB_2 path (from pins 2 to 24, 3 to 22 and 4 to 20)	f = 10 MHz	–	–	3	dB
Sandcastle pulse detector (control bit SC5 = 0) three level; notes 6 and 7						
V_{14}	required voltage range					
	for H and V blanking pulses		2.0	2.5	3.0	V
	for H pulses (line count)		4.0	4.5	5.0	V
	for burst key pulses (clamping)		7.6	–	V_P +5.8	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sandcastle pulse detector (control bit SC5 = 1) two level; notes 6 and 7						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	for burst key pulses		4.0	4.5	V_P+5.8	V
Sandcastle pulse detector						
I_{14}	output current	V_{14} = 0 V	–	–	–100	µA
t_d	leading edge delay of the clamping pulse		–	1.5	–	µs
VFB (note 7)						
V_{18}	vertical flyback pulse	for LOW	–	–	2.5	V
		for HIGH	4.5	–	–	V
	internal voltage	pin 18 open-circuit; note 8	–	5.0	–	V
I_{18}	input current		–	–	5	µA
Average beam current limiting (note 9)						
$V_{c(15)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(15)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(15)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(15)}$	voltage difference for full brightness reduction		–	–1.6	–	V
Peak drive limiting voltage (note 10) internal peak drive limiting level (V_{pdl}) acts on RGB outputs I^2C-bus control, sub-address $0A_{Hex}$						
$V_{20/22/24}$	level for minimum RGB outputs	at byte 00_{Hex}	–	–	3.0	V
	level for maximum RGB outputs	at byte $3F_{Hex}$	7.0	–	–	V
I_{16}	charge current		–	–1	–	µA
	discharge current	during peak white	–	5	–	mA
V_{16}	internal voltage limitation		4.5	–	–	V
$V_{c(16)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(16)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(16)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(16)}$	voltage difference for full brightness reduction		–	–1.6	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic cut-off control (notes 7, 11, 12 and 13) see Fig.9						
V_{19}	external voltage		–	–	V_P - 1.4	V
I_{19}	output current		–	–	–60	µA
	input current		150	–	–	µA
	additional input current	switch-on delay 1	–	0.5	–	mA
$V_{24,22,20}$	monitor pulse amplitude (under I^2C-bus control, sub-address $0A_{Hex}$)	switch-on delay 1; note 12	–	V_{pdl} – 1.0	–	V
V_{19}	voltage threshold for picture tube cathode warm-up	switch-on delay 1	–	4.5	–	V
	internally controlled voltage (V_{REF})	during leakage measurement period	–	2.7	–	V
ΔV_{19}	voltage difference between V_{MEAS} (cut-off measurement voltage) and V_{REF}		–	1.0	–	V
Cut-off storage						
$I_{21/23/25}$	charge and discharge currents	during cut-off measurement lines	–	±0.3	–	mA
	current	outside measurement	–	–	±0.1	µA
Leakage storage						
I_{17}	charge and discharge currents	during leakage measurement period	–	±0.4	–	mA
	current	outside measurement	–	–	±0.1	µA
V_{17}	threshold voltage for reset to switch-on state		–	2.5	–	V
Hue control (note 14) under I^2C-bus control, sub-address 03_{Hex} data byte $3F_{Hex}$ for maximum voltage data byte 20_{Hex} for nominal voltage data byte 00_{Hex} for minimum voltage						
V_{26}	output voltage	at byte $3F_{Hex}$	4.8	–	–	V
		at byte 20_{Hex}	–	3.0	–	V
		at byte 00_{Hex}	–	–	1.2	V
I_{int}	current of the internal current source at pin 26		500	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus receiver clock SCL (pin 28)						
f_{SCL}	input frequency range		0	–	100	kHz
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	6.0	V
I_{IL}	LOW level input current		–	–	–10	µA
I_{IH}	HIGH level input current		–	–	10	µA
t_d	pulse delay time LOW		4.7	–	–	µs
	pulse delay time HIGH		4.0	–	–	µs
t_r	rise time		–	–	1.0	µs
t_f	fall time		–	–	0.3	µs
I²C-bus receiver data input/output SDA (pin 27)						
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	6.0	V
I_{IL}	LOW level input current		–	–	–10	µA
I_{IH}	HIGH level input current		–	–	10	µA
I_{OL}	LOW level output current		3.0	–	–	mA
t_r	rise time		–	–	1.0	µs
t_f	fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		0.25	–	–	µs

Notes to the characteristics

1. The values of the –(B–Y) and –(R–Y) colour difference input signals are for a 75% colour-bar signal.
2. The pins are capacitively coupled to a low ohmic source, with a recommended maximum output impedance of 600 Ω.
3. PAL/SECAM signals are matrixed by the equation: $V_{G-Y} = -0.51V_{R-Y} - 0.19V_{B-Y}$
   NTSC signals are matrixed by the equations (hue phase shift of –5 degrees):
   $V_{R-Y*} = 1.57V_{R-Y} - 0.41V_{B-Y}$; $V_{G-Y}* = -0.43V_{R-Y} - 0.11V_{B-Y}$; $V_{B-Y}* = V_{B-Y}$
   In the matrix equations: V_{R-Y} and V_{B-Y} are conventional PAL demodulation axes and amplitudes at the output of the NTSC demodulator. $V_{G-Y}*$, $V_{R-Y}*$ and $V_{B-Y}*$ are the NTSC-modified colour difference signals; this is equivalent to the following demodulator axes and amplification factors:

	NTSC	PAL
(B–Y)* demodulator axis	0°	0°
(R–Y)* demodulator axis	115°	90°
(R–Y)* amplification factor	1.97	1.14
(B–Y)* amplification factor	2.03	2.03

   $V_{G-Y}* = -0.27V_{R-Y}* - 0.22V_{B-Y}*$.
4. The white potentiometers affect the amplitudes of the RGB output signals.
5. The RGB outputs at pins 24, 22 and 20 are emitter followers with current sources.

6. Sandcastle pulses are compared with internal threshold voltages independent of V_P. The threshold voltages separate the components of the sandcastle pulse. The particular component is generated when the voltage on pin 14 exceeds the defined internal threshold voltage. The internal threshold voltages (control bit SC5 = 0) are:

   1.5 V for horizontal and vertical blanking pulses (H and V blanking pulses),

   3.5 V for horizontal pulses,

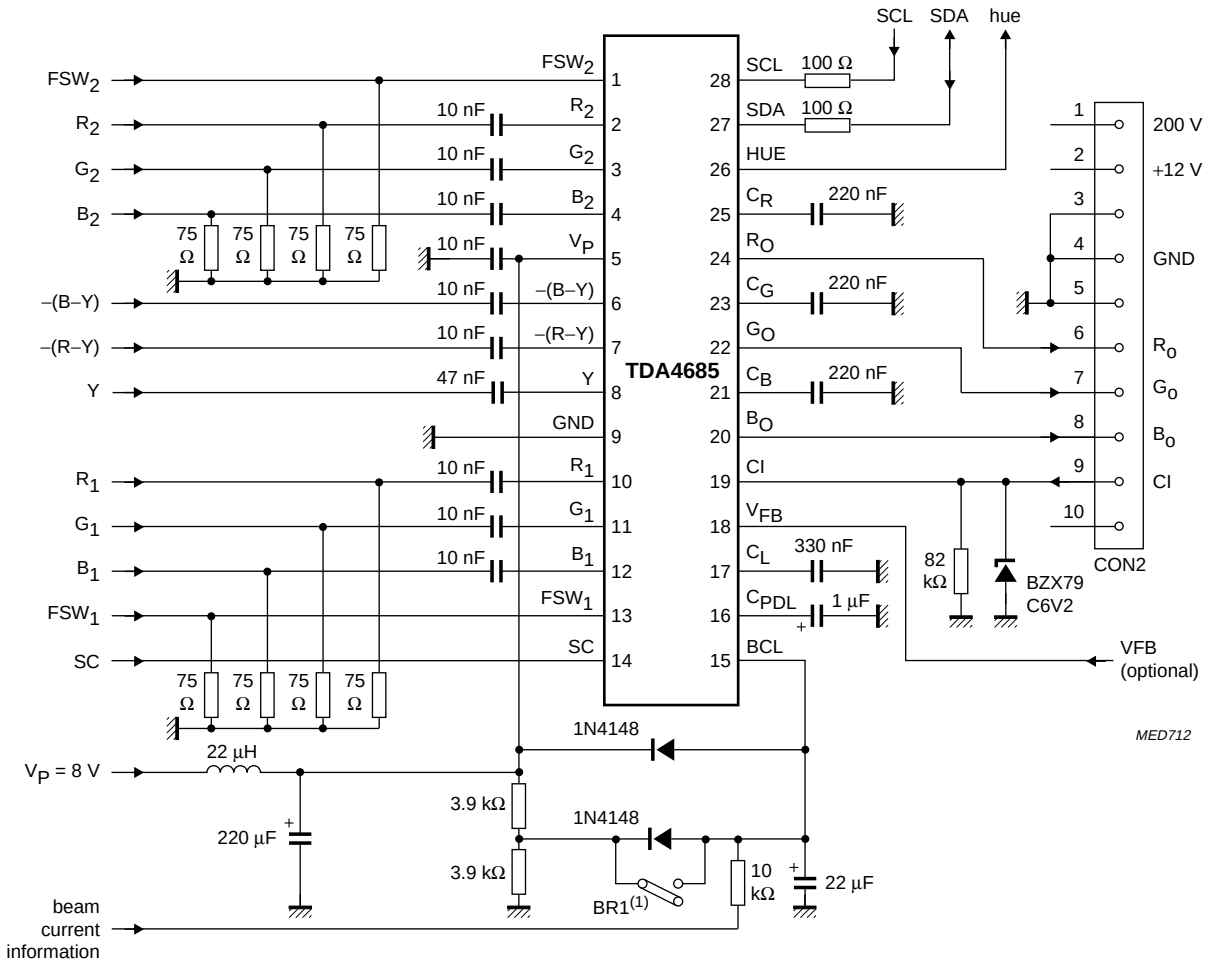
   6.5 V for the burst key pulse.

   The internal threshold voltages, control bit SC5 = 1, are:

   1.5 V for horizontal and vertical blanking pulses,

   3.5 V for the burst key pulse.

7. Vertical signal blanking is determined by the vertical component of the sandcastle pulse. The leakage and the RGB cut-off measurement lines are positioned in the first four complete lines after the end of the vertical component. In this case, the RGB output signals are blanked until the end of the last measurement line; see Fig 9(a). If an extra vertical flyback pulse VFB is applied to pin 18, the four measurement lines start in the first complete line after the end of the VFB pulse; see Fig 9(b). In this case, the output signals are blanked either until the end of the last measurement line or until the end of the vertical component of the sandcastle pulse, according to which occurs last.
8. If no VFB pulse is applied, pin 18 can be left open-circuit or connected to V_P. If pin 18 is always LOW neither automatic cut-off control nor output clamping can happen.
9. Average beam current limiting reduces the contrast, at minimum contrast it reduces the brightness.
10. Peak drive limiting reduces the RGB outputs by reducing the contrast, at minimum contrast it reduces the brightness. The maximum RGB outputs are determined via the I^2C-bus under sub-address $0A_{Hex}$. When an RGB output exceeds the maximum voltage, peak drive limiting is delayed by one horizontal line.
11. During leakage current measurement, the RGB channels are blanked to ultra-black level. During cut-off measurement one channel is set to the measurement pulse level, the other channels are blanked to ultra-black. Since the brightness adjust shifts the colour signal relative to the black level, the brightness adjust is disabled during the vertical blanking interval (see Fig.8 and Fig.9).
12. During picture cathode warm-up (first switch-on delay) the RGB outputs (pins 24, 22 and 20) are blanked to the ultra-black level during line scan. During the vertical blanking interval a white-level monitor pulse is fed out on the RGB outputs and the cathode currents are measured. When the voltage threshold on pin 19 is greater than 4.5 V, the monitor pulse is switched off and cut-off control is activated (second switch-on delay). As soon as cut-off control stabilizes, RGB output blanking is removed.
13. The cut-off measurement level range at the RGB outputs is 1 to 5 V. The recommended value is 3 V.
14. The hue control output at pin 26 is an emitter follower with current source.



(1) Insert link BR1 if average beam current limiting is not applied.

Fig.7 Test and application circuit.

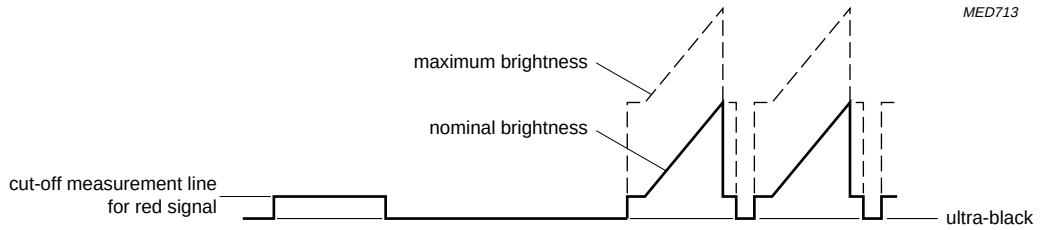
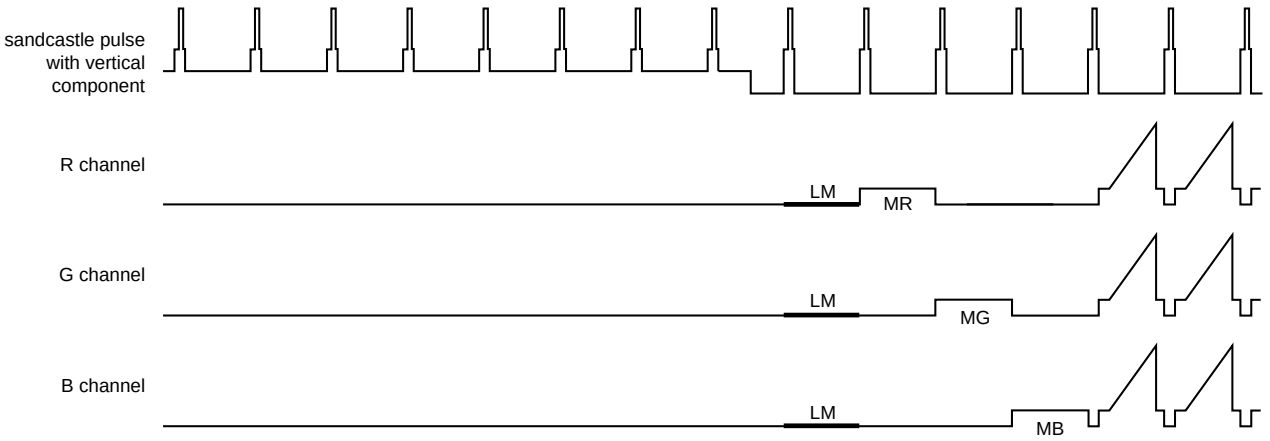
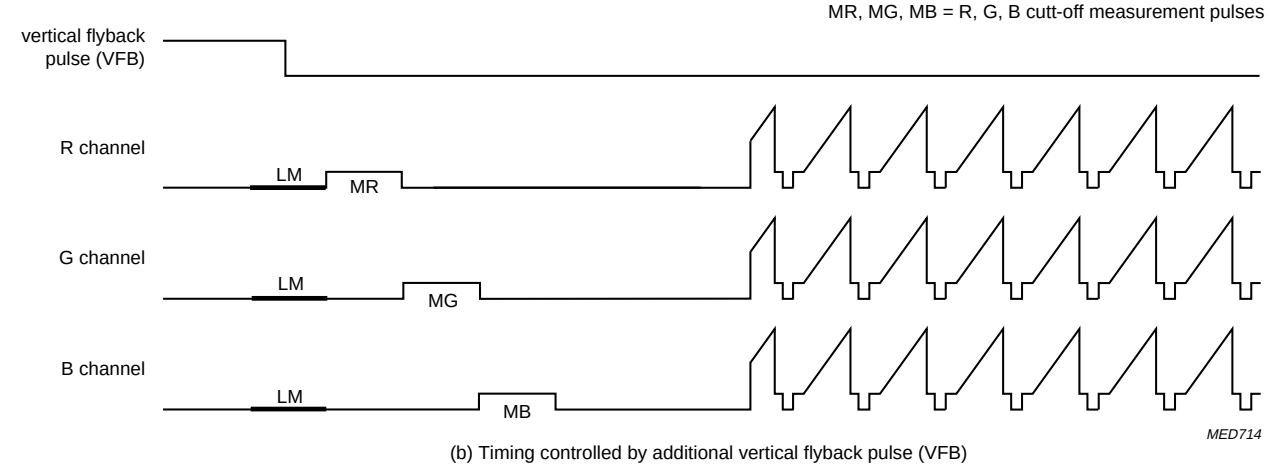


Fig.8 Cut-off measurement pulse.



(a) Timing controlled by sandcastle pulse

LM = leakage current measurement time
MR, MG, MB = R, G, B cutt-off measurement pulses

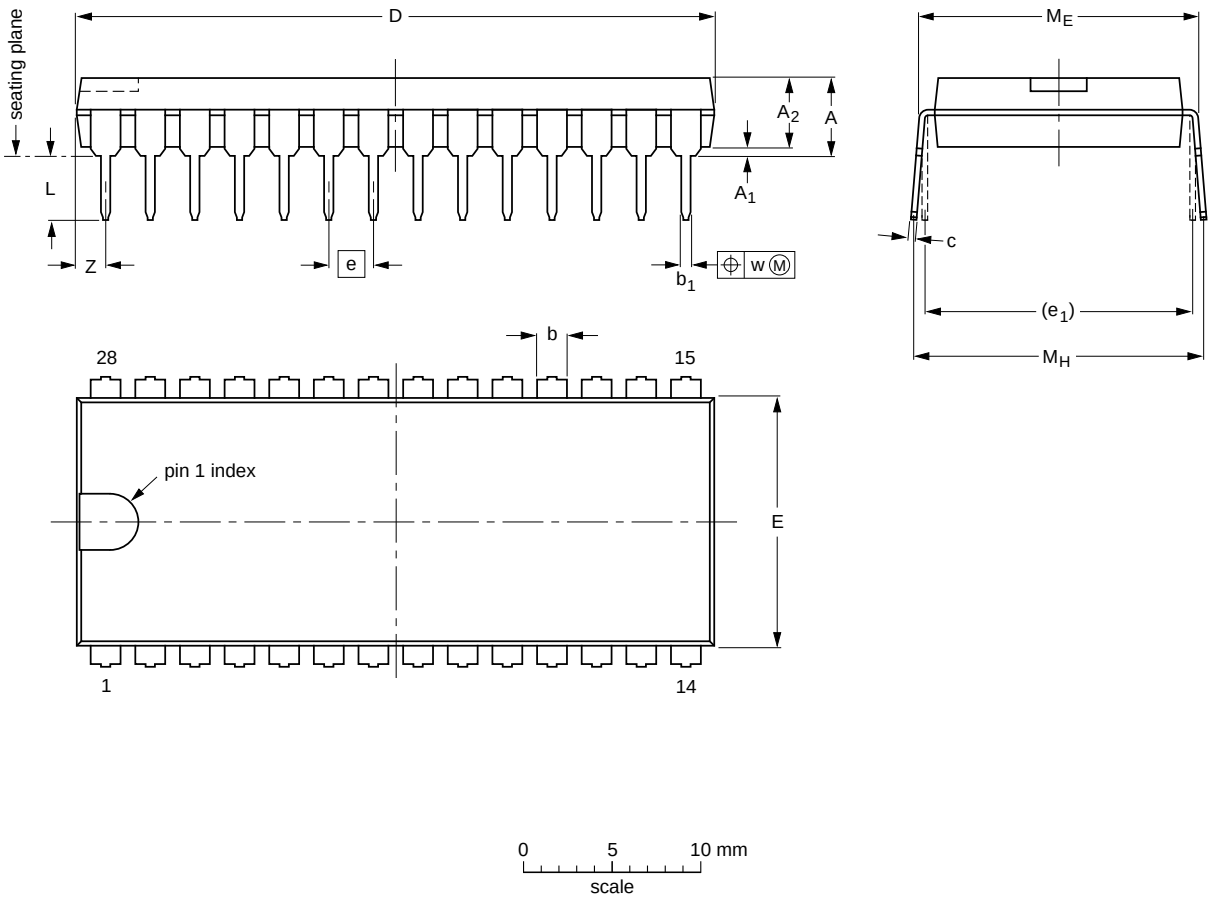


(b) Timing controlled by additional vertical flyback pulse (VFB)

Fig.9 Leakage and cut-off current measurement timing diagram.

PACKAGE OUTLINE

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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