# DATA SHEET

# TDA4800
## Vertical deflection circuit for monitor applications

Product specification
Supersedes data of February 1992
File under Integrated Circuits, IC02

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# Vertical deflection circuit for monitor applications

# TDA4800

## FEATURES

- Fully integrated, few external components
- RC oscillator with wide sync range of 1 : 3 (e.g. 50 to 150 Hz)
- Synchronization by positive or negative going sync pulse
- Blanking pulse duration is determined externally
- Dual frequency criterion for automatic amplitude switch-over (e.g. 50 to 60 Hz)
- Guard circuit for screen protection
- Sawtooth generator with buffer stage supplied by external voltage
- Preamplifier
- Power output stage with thermal and SOAR protection
- Flyback generator
- Internal voltage stabilizer.

## GENERAL DESCRIPTION

The TDA4800 is an integrated circuit for vertical deflection primarily in monitors (and TV receivers). The complete circuit consists of 11 main functional blocks as shown in Fig.1.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{P1}$ | supply voltage (pin 6) | | 10 | – | 30 | V |
| $V_{P2}$ | supply voltage (pin 10) | | 10 | – | 45 | V |
| $I_P$ | supply current (pins 6 and 10) | note 1 | – | 215 | – | mA |
| $I_{7(p-p)}$ | output current (peak-to-peak value) | | – | – | 2.6 | A |
| $f_{sync}$ | picture frequency | notes 1 and 2 | – | – | 135 | Hz |
| $V_3$ | positive sync input pulse | | 1.0 | – | 6.0 | V |
| $V_3$ | negative sync input pulse | | –0.5 | – | –0.7 | V |
| $T_{amb}$ | operating ambient temperature | note 3 | –20 | – | +70 | °C |

**Notes**

1. Measured in Fig.4.
2. $f_o$ = 45 Hz ($f_{sync(max)} = 3f_o$).
3. $P_{tot}$ = 3.6 W for $R_{th(j-a)}$ = 20 K/W.

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| TDA4800 | DBS13P | plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm) | SOT141-6 |

## BLOCK DIAGRAM

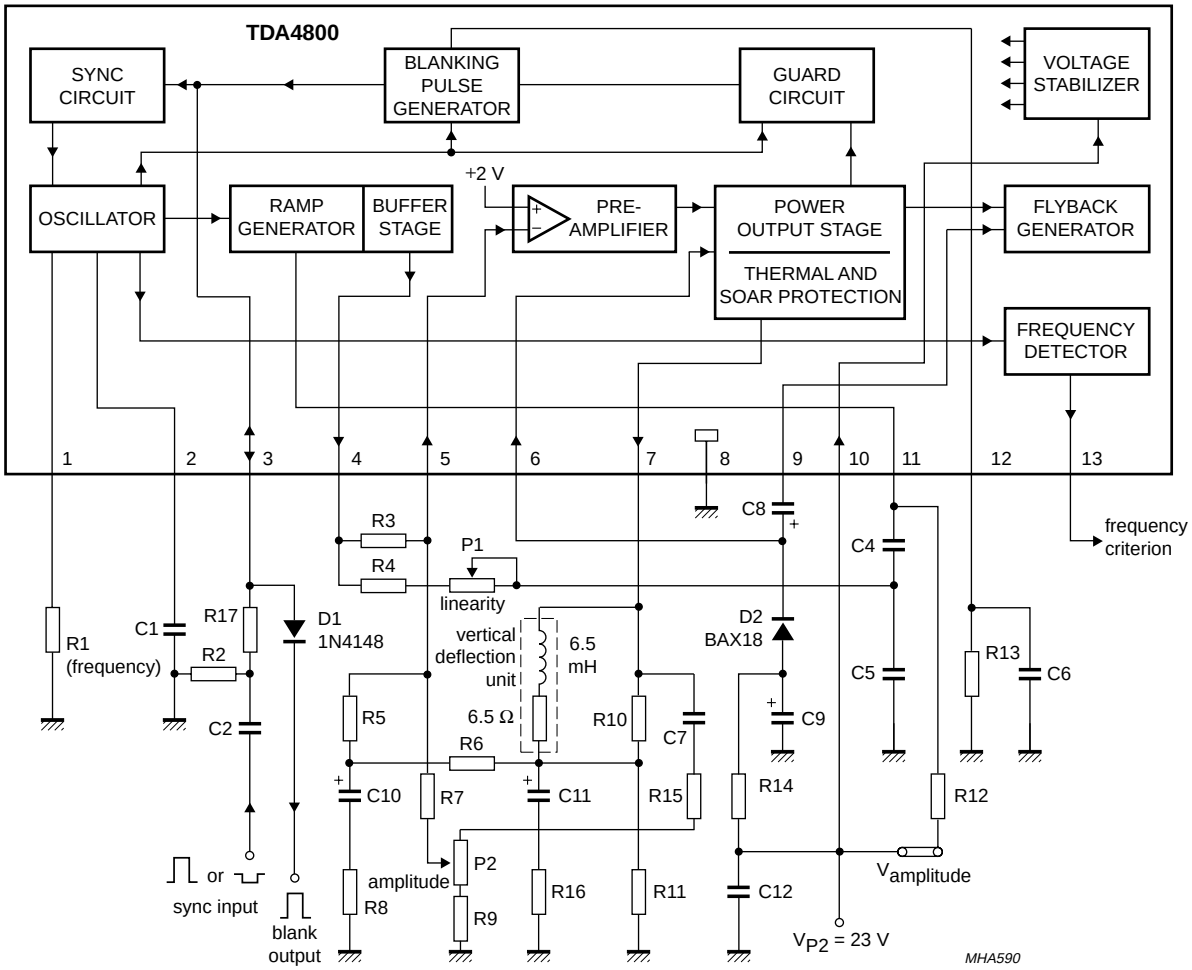



Fig.1 Block diagram.

## PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| $OSC_R$ | 1 | oscillator resistor |
| $OSC_C$ | 2 | oscillator capacitor |
| $SYB_O$ | 3 | sync input; blanking pulse output |
| $S_{OUT}$ | 4 | sawtooth output |
| $PRE_I$ | 5 | preamplifier input |
| $V_{P1}$ | 6 | supply voltage 1 |
| OUTP | 7 | deflection output |
| GND | 8 | ground |
| $C_{FLY}$ | 9 | pin for the flyback generator capacitor |
| $V_{P2}$ | 10 | supply voltage 2 |
| $S_{GEN}$ | 11 | sawtooth generator |
| $BP_{DU}$ | 12 | blanking pulse duration |
| $FRQ_C$ | 13 | frequency criterion |

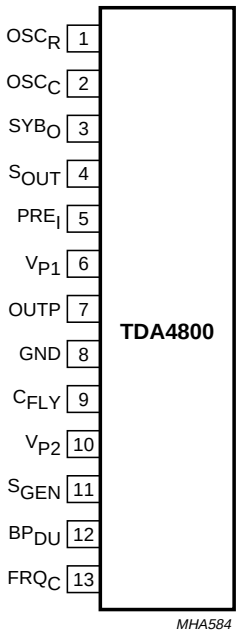



Fig.2 Pin configuration.

## FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Fig.1:

1. Oscillator
2. Synchronization circuit
3. Blanking pulse generator
4. Frequency detector and storage
5. Ramp generator
6. Buffer stage
7. Preamplifier
8. Power output stage
9. Flyback generator
10. Guard circuit
11. Voltage stabilizer.

### Oscillator (pins 1 and 2)

The oscillator is an RC-oscillator with a threshold value switch, which ensures very good frequency stability.

The upper and lower threshold voltages are defined by an internal voltage divider.

An external capacitor C1 at pin 2 is charged by a constant current source. When the scan voltage of C1 reaches the upper threshold voltage, oscillator flyback starts. Capacitor C1 discharges via an internal resistor and transistor until the lower threshold is reached.

The constant charge current and free-running frequency $f_o$ are adjusted by an external resistor R1 at pin 1:

$$f_o = \frac{1}{K \times R1 \times C1} \text{ with } K = 0.68.$$

### Synchronization circuit (pin 3)

A positive- or negative-going pulse fed to pin 3 synchronizes the oscillator by lowering the upper threshold voltage. The synchronizing range is $f_o$ to $3f_o$. For example: $f_o = 50\ Hz \rightarrow f_{sync(max)} = 150\ Hz$.

### Blanking pulse generator (pin 3)

Also at pin 3 a blanking pulse is available. Diode D1 separates the synchronization pulse from the blanking pulse. During scanning, the external capacitor C6 at pin 12 is charged to an internal stabilized voltage $V_{stab2}$.
The blanking pulse starts with the beginning of oscillator flyback; then capacitor C6 discharges via the external resistor R13 at pin 12. The blanking pulse stops when the capacitor voltage is $\frac{1}{2}V_{stab2}$.

The blanking pulse duration is determined by the values of external components R13 and C6 at pin 12:
$t_{bl} = R13 \times C6 \times Ln2$.

### Frequency detector with storage (pin 13)

At the end of the scanning period a frequency detector detects the oscillator frequency (see “Note” below).

When this frequency is above the threshold a flip-flop is set to store this information. The output is an open collector output.

NOTE

Frequency detector change-over at pin 13 from low (= low frequency) to high (= high frequency) is determined by $f_o$: $f_{threshold} = 1.23 \times f_o$.

### Ramp generator (pin 11)

The ramp generator consists of two external series capacitors C4 and C5, external charge resistor R12 (connected to pin 11), and an internal differential amplifier which is synchronously switched by the oscillator.

External capacitors C4 and C5 at pin 11 are charged by the charging current via the external charge resistor R12 until oscillator flyback starts. C4 and C5 are then discharged via pin 11 by an internal resistor and transistor. This generates a positive-going ramp voltage.

### Buffer stage (pin 4)

The buffer stage consists of two emitter followers.
The ramp voltage is fed via the buffer stage and is available at pin 4 with a low ohmic output impedance. With R4 and P1 it generates a ramp function, which, together with the feedback network of the deflection yoke, gives a high degree of linearity at the picture tube. The linearity can be adjusted by P1.

### Preamplifier (pin 5)

The preamplifier is a differential amplifier.
The non-inverting input is fixed at about 2 V by an internal voltage divider. The inverting input at pin 5 is connected to the ramp voltage via R3 and feedback network P2, R5 to R11, R15, R16, C7, C10 and C11.

### Power output stage (pin 7)

The power output stage is an amplifier with a quasi-complementary class-B output. The output is connected to pin 7.

The power stage includes SOAR and thermal protection.

### Flyback generator (pin 9)

The flyback generator has an external capacitor C8 at pin 9. During scanning, the internal circuit switches pin 9 almost to ground; thereby C8 is charged by the supply voltage via external components R14 and D2.

During the flyback time pin 9 is switched almost to the supply voltage, so that the supply voltage for the power output stage (pin 6) is nearly doubled. This high flyback voltage ensures a very short flyback time.

### Guard circuit (pin 3)

When the vertical deflection current is absent (e.g. short-circuited, or open-circuited of the yoke) the guard circuit changes the blanking pulse at pin 3 into a DC signal which blanks the beam current to protect the screen.

Also an oscillator defect (C1 short-circuited or R1 disconnected from pin 1) switches on the guard circuit.

### Voltage stabilizer

The voltage stabilizer circuit provides a stable operating voltage of about 7.5 V for several internal circuits of the TDA4800.

### INTERNAL CIRCUITRY

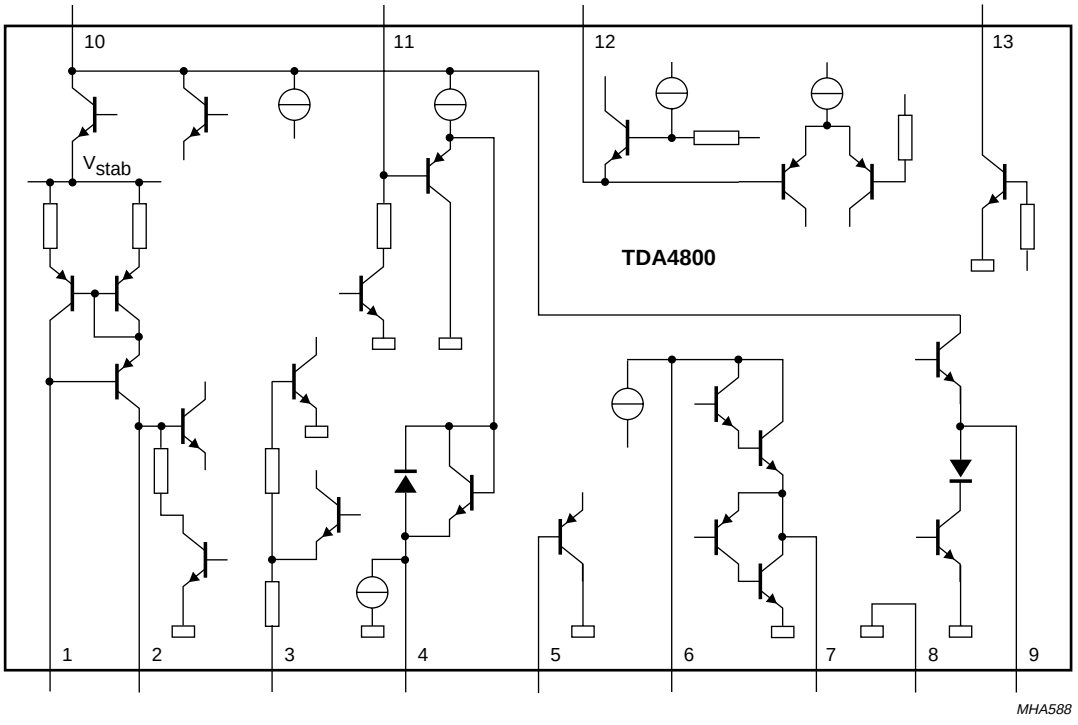



Fig.3 Internal circuitry.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_2$ | voltages | | 0 | 6 | V |
| $V_{11}$ | | | 0 | 24 | V |
| $V_{12}$ | | | 0 | 6 | V |
| $V_{13}$ | | | 0 | 50 | V |
| $V_{10}$ | supply voltages ($V_P$) | | 0 | 50 | V |
| $V_9$ | | | 0 | 50 | V |
| $V_7$ | | | 0 | 60 | V |
| $V_6$ | | | 0 | 60 | V |
| $V_5$ | | | 0 | 6 | V |
| $V_4$ | | | 0 | 24 | V |
| $V_3$ | | | −0.7 | +6 | V |
| $I_1$ | currents | | 0 | −1 | mA |
| $I_3$ | | | +3 | −10 | mA |
| $I_4$ | | | 0 | −5 | mA |
| $I_6$, $I_7$, $I_8$ | | | note 1 | | |
| $I_9$ | | | −1.5 | +1.5 | A |
| $I_{11}$ | | | −0.1 | +30 | mA |
| $T_{stg}$ | storage temperature | | −25 | +150 | °C |
| $T_{amb}$ | operating ambient temperature | note 2 | −20 | +70 | °C |
| $T_j$ | junction temperature | note 3 | − | 150 | °C |
| $P_{tot}$ | total power dissipation | note 2 | − | − | W |
| $V_{ESD}$ | ESD sensitivity | note 4 | −2000 | +2000 | V |

**Notes**

1. $I_6$, $I_7$ and $I_8$ are limited by SOAR protection circuit that ensures that short-circuiting between the output pin 7 and supply voltage or ground does not destroy the output stage. A short-circuit may be soldered into the printed-circuit board or may sometimes (non-periodically) occur in the applied circuit.
2. The maximum value for the operating ambient temperature range and the power dissipation depends on the heatsink.
3. Internally limited by thermal protection: switching temperature point at $T_j$ = 150 ±8 °C.
4. Human body model: 1.5 kΩ, 100 pF, 5 pulses.

## THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | VALUE | UNIT |
|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | 20 | K/W |
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | 5 | K/W |

## CHARACTERISTICS

All voltages are measured to GND (ground; pin 8); $T_{amb}$ = 25 °C; $V_P$ = 23 V; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{P1}$ | supply voltage (pin 6) | | 10 | – | 30 | V |
| $V_{P2}$ | supply voltage (pin 10) | | 10 | – | 45 | V |
| $I_{10}$ | supply current | $V_{10}$ = 25 V; $V_5$ = 3 V without load | – | 12 | – | mA |
| $I_6$ | supply current | $V_6$ = 25 V; $V_5$ = 1 V without load | – | 20 | – | mA |
| $I_6$ | supply current | $V_6$ = 25 V; $V_5$ = 3 V without load | – | 5 | – | mA |
| $V_{7(min)}$ | minimum output voltage | $I_7$ = 1 A | – | 1.4 | 1.65 | V |
| $V_{7(max)}$ | maximum output voltage | $I_7$ = −1 A | $V_6$ − 2.3 | $V_6$ − 2.0 | – | V |
| $V_9$ | output voltage during flyback | $I_9$ = −1 A | – | $V_{10}$ − 2.2 | – | V |
| $I_7$ | output current | | – | – | ±1.3 | A |
| $I_9$ | output current | | – | – | ±1.3 | A |
| $I_5$ | preamplifier input current | | – | −0.1 | – | µA |
| $V_1$ | stabilized voltage | | 6.1 | 6.8 | 7.3 | V |
| $V_3$ | blanking pulse output voltage | | – | 5.7 | – | V |
| $R_3$ | blanking pulse output resistance | | – | 300 | – | Ω |
| $I_3$ | blanking pulse output current | | 0 | – | −3 | mA |
| $t_{bl}$ | blanking pulse duration | R = 100 kΩ; C = 10 nF (pin 12) | 640 | 680 | 730 | µs |
| $V_{11}$ | output voltage ramp generator | | 0.3 | – | 20 | V |
| $I_{11}$ | output current ramp generator | | −2 | – | $15 \times 10^3$ | µA |
| $V_{13}$ | output voltage frequency detector | lower frequency $I_{13}$ = 1 mA | – | – | 1.0 | V |
| $I_{13}$ | leakage current frequency detector | higher frequency $V_{13}$ = 50 V | – | – | 1.0 | µA |
| $V_4$ | output voltage buffer stage | | 0 | – | 20 | V |
| $I_4$ | output current buffer stage | | – | – | −4.0 | mA |
| $V_3$ | synchronizing input voltage | positive sync | 1.0 | – | 6.0 | V |
| $V_3$ | synchronizing input voltage | negative sync | −0.5 | – | −0.7 | V |
| | tolerance of free running oscillator | without sync | −3.0 | – | +3.0 | % |
| $\frac{\Delta f}{f} \times \frac{1}{\Delta T_{mb}}$ | oscillator temperature dependency | $T_{mb}$ = 20 to 100 °C | – | $10^{-4}$ | – | $K^{-1}$ |
| $\frac{\Delta f}{f} \times \frac{1}{\Delta V_P}$ | oscillator voltage dependency | $V_P$ = 10 to 30 V | – | $4 \times 10^{-4}$ | – | $K^{-1}$ |
| $\frac{f_o}{f_{sync}}$ | synchronizing ratio | | 1 : 2.9 | 1 : 3 | – | |

## TEST AND APPLICATION INFORMATION

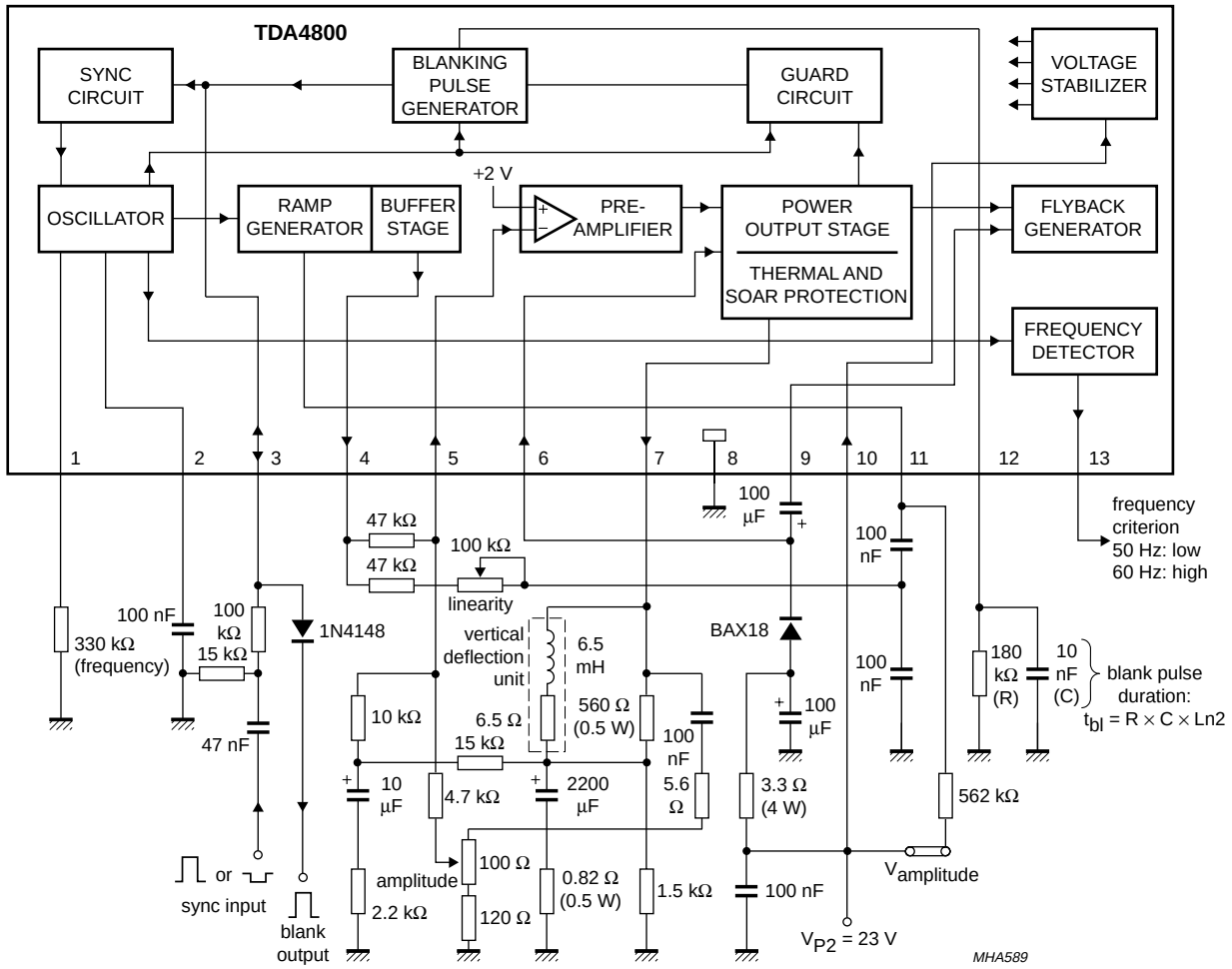


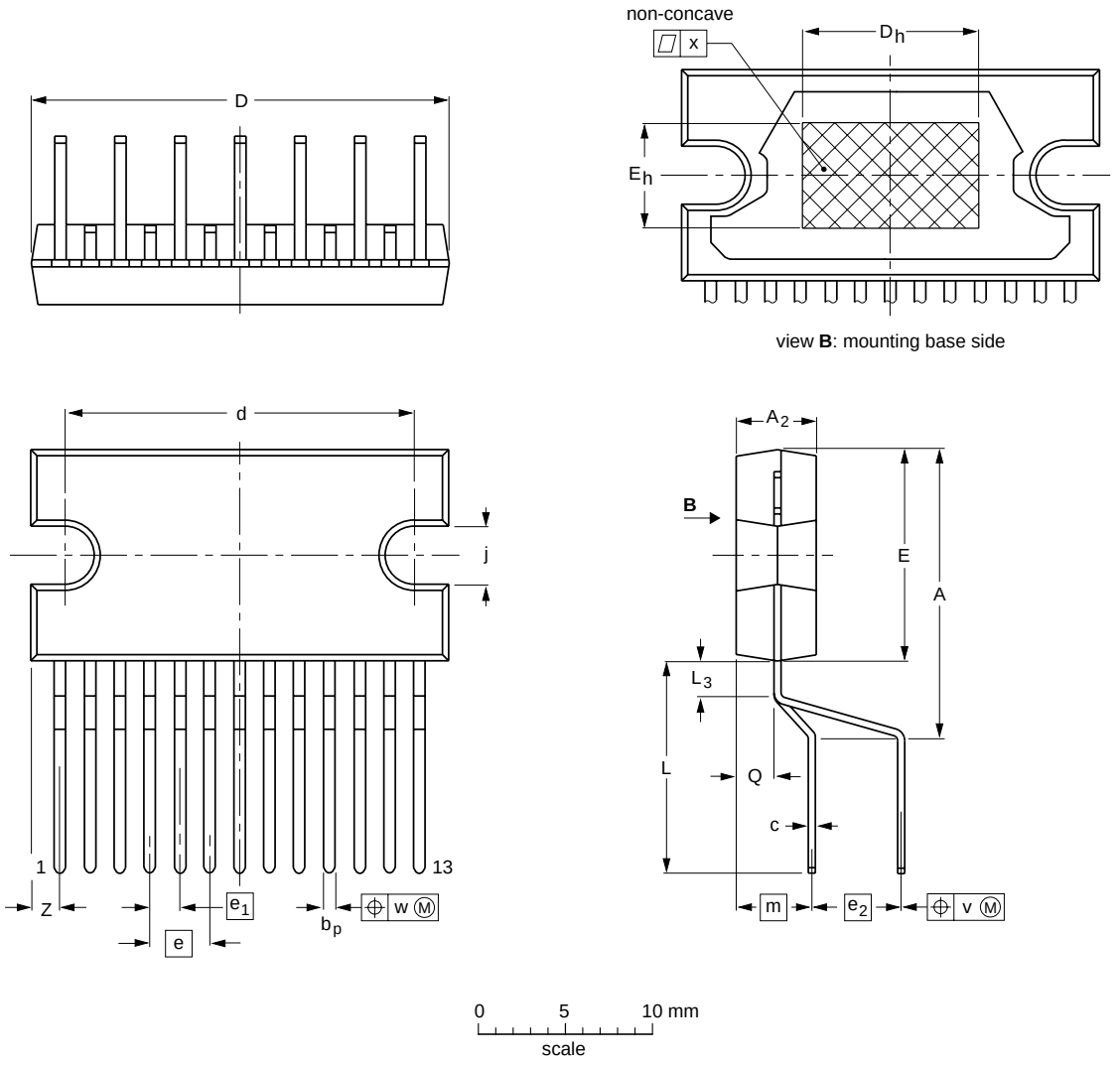

Fig.4 Test and application circuit.

**TDA4800 in the test and application circuit** (see Fig.4)

| SYMBOL | PARAMETER | CONDITIONS | TYP. | UNIT |
|---|---|---|---|---|
| $V_{P2}$ | supply voltage | | 23 | V |
| $I_P$ | supply current | | 215 | mA |
| $V_7$ | DC output voltage | | 11.8 | V |
| $V_{7M}$ | peak output voltage | | 45 | V |
| $I_7$ | output current | | 0.8 | A |
| $I_{Y(p-p)}$ | vertical deflection current (peak-to-peak value) | | 1.5 | A |
| $t_{fb}$ | flyback time | | 0.3 | ms |
| $t_{bl}$ | blanking pulse duration | | 1.25 | ms |
| $P_{tot}$ | total power dissipation | | 3.3 | W |
| $f_o$ | free running oscillator frequency | without sync | 45 | Hz |

## PACKAGE OUTLINE

**DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)** **SOT141-6**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_2$ | $b_p$ | c | $D^{(1)}$ | d | $D_h$ | $E^{(1)}$ | e | $e_1$ | $e_2$ | $E_h$ | j | L | $L_3$ | m | Q | v | w | x | $Z^{(1)}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 17.0<br>15.5 | 4.6<br>4.2 | 0.75<br>0.60 | 0.48<br>0.38 | 24.0<br>23.6 | 20.0<br>19.6 | 10 | 12.2<br>11.8 | 3.4 | 1.7 | 5.08 | 6 | 3.4<br>3.1 | 12.4<br>11.0 | 2.4<br>1.6 | 4.3 | 2.1<br>1.8 | 0.8 | 0.25 | 0.03 | 2.00<br>1.45 |

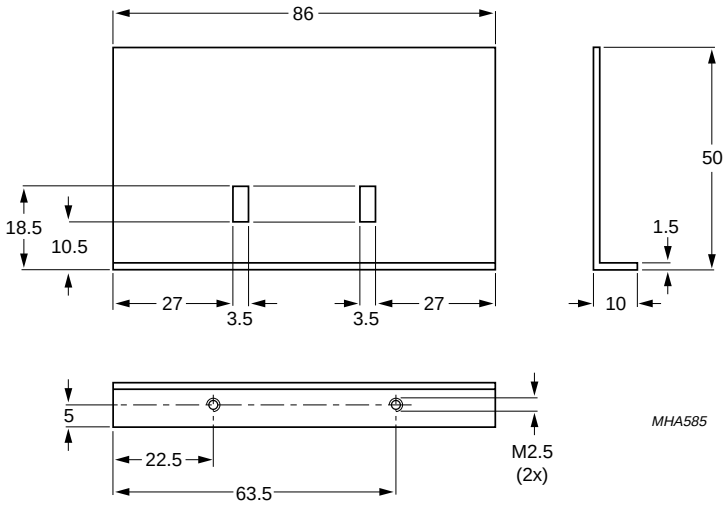
**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT141-6 | | | | | | ~~92-11-17~~<br>95-03-11 |

## MOUNTING INSTRUCTIONS FOR 13-LEAD DBS13P POWER PACKAGE

The rise in temperature caused by power dissipation in the circuit is reduced by adding a heatsink with a sufficiently low thermal resistance: $R_{th(mb-h)} + R_{th(h-a)} = R_{th(mb-a)}$ (e.g. the heatsink of Fig.5). It is possible to attach the package to the heatsink by screws (Fig.6) or by a compression spring (Fig.7). A layer of silicon grease between the heatsink and the mounting base optimizes thermal contact.




Dimensions in mm.

Fig.5 Heatsink made of black-leaded Aluminium.

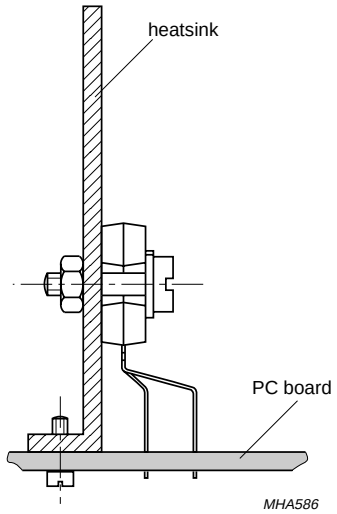
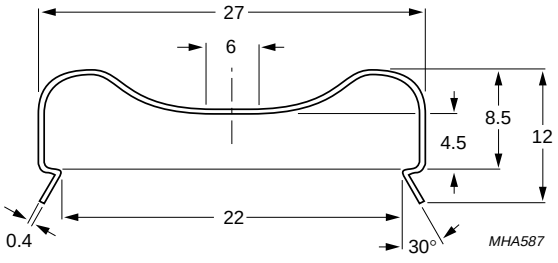



Fig.6 Package and heatsink attached by screws.




Dimensions in mm.

Fig.7 Compression spring for easily attaching the package to the heatsink of Fig.5.