Tentative Device Specification

Type: Commercial: TDA4822PS CMOS ONECHIP SHARPNESS AND MULTIMEDIA IC
Experimental: V10240

CONTENTS

1 FEATURES

- Combination of analog video processing with logic, timing detection and decoding according CustoMax protocol
- Video Enhancement (VE) single area or window activation
- Sharpness control on R,G,B -signal activated within the calculated video area or window; 4 time constants and 4 peaking amplitudes can be selected by I^2C-Bus
- Video amplitude boosting control on R,G,B- signals activated within the calculated video area or window; 4 boosting levels can be selected by I^2C-Bus
- Suitable for input video bandwidth up to 250 M pixels resolution
- Video outputs capable of driving most of the current video processors (reference is Philips TDA488x)
- Video inputs directly fed by the VGA connector
- Video input clamping compatible with the TDA485x CLBL output signal
- Internal line locked clock PLL
- R, G, B message decoding
- Sync polarity unification
- H and V timing parameters measurements
- OSD fast blanking processing
- I^2C-Bus transceiver (400KHz version) with buffered mode
- Window or area activation output
- Power dip detection with VE de-activation
- LLC unlock detection with VE de-activation
- Build in auto reset

2 GENERAL DESCRIPTION

The TDA4822PS is an integrated circuit capable of boosting the amplitude and increasing the sharpness of the R, G, B input signals of a graphic display (in the followings, when a distinction is not needed, both functions are grouped in the “Video Enhancement =VE” definition). Although the device application is conceived for CRT based displays, its use could be extended, with limitations, to Flat Panel Displays with analog interface.

The TDA4822PS incorporates all the circuitries necessary for a "windowed" or "local" activation of the VE: the activation area coordinates (expressed in pixels and referred to the running active video resolution) are encoded according the CustoMax protocol (CustoMax is proprietary Philips software that allows users to adjust monitor paramenters under Windows) and sent by the host PC through the R,G,B lines. The TDA4822PS strips these data from the RGB lines, measures some video timing parameters with its local Line Locked Clock (LLC) and send all the informations via its I^2C-Bus transceiver to the system micro-controller. The latter returns to the TDA4822PS the window coordinates expressed in LLC pulses and referenced to the H and V timings. The TDA4822PS then generates an internal VE activation signal that gates both a sharpness improvement block and a highlight (increased video contrast) block. These blocks can be activated separately (contrast amplitude, peaking amplitude and peaking time constant). The result is a windowed video output enhancement with sharper contours and TV-like light output.

3 QUICK REFERENCE DATA

Voltages referring to V_{SSA}=V_{SSC}

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDC}	core supply voltages (Pin 15)	3	3.3	3.6	V
V_{DDA}	analog supply voltage (Pin 22)	3	3.3	3.6	V
$V_{DD(PLL)}$	PLL supply voltage (Pin 18)	3	3.3	3.6	V
$V_{VIR,VIG,VIB}$	Peak to peak video input voltage (Pins 2, 4, 6) ; ac coupled C1,2,3=10nF	0	–	1	Vpp
$V_{VOR, VOG, VOB}$	Peak to peak video output voltage (Pins 23, 21, 19) ; ac coupled with C=10nF	0	–	1.4	Vpp
$Vu_{nominal}$	nominal gain (VE inactive) $V_{VOR,G,B}/V_{VIR,G,B}$; note 1	0.93	0.98	1.03	
$Vu_{contrast}$	gain boosting (VE =active) ($V_{VOR,G,B(VE=active)}/V_{VOR,G,B(VE=inactive)}$				
	HLA=00H	105	110	115	%
	HLA=00H03H	135	140	145	%
$Vu_{sharpness}$	sharpness/peaking boosting ($V_{VOR,G,B(VE=active)}/V_{VOR,G,B(VE=inactive)}$				
	SA=00H ($T_{sharpness}$>/=50nsec)	105	110	-	%
	SA=03H ($T_{sharpness}$ >/=50nsec)	140	145	-	%
$T_{sharpness}$	time constant of sharpness/peaking boosting; note 2 +3				
	STC=00H	-	150	-	nsec
	STC=03H	-	20	-	nsec
tr	rise time video output (VE=inactive); note 2	-	2.7	-	nsec
tf	fall time video output (VE=inactive); note 2	-	2.3	-	nsec
F_{LLC}	Internal line lock frequency	30.7	–	132	MHz
$F_{IIC-Bus}$	max. I^2C-Bus clock frequency		-	400	KHz

Notes

1. External output load =1.1kΩ to V_{SSA}
2. External output load =1.1kΩ parallel to 5pF; input rise/fall time =1nsec;
   measurement of tr and tf at 10 to 90% amplitude; nominal video output signal =700mV
3. Definition of the sharpness time constants: duration for sharpness amplitude >50% of the maximum peak amplitude.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4822PS CMOS ONECHIP SHARPNESS AND MULTIMEDIA IC	SDIP24	shrink dual in line package; 24 leads (400mil)	SOT234AH2

5 BLOCK DIAGRAM

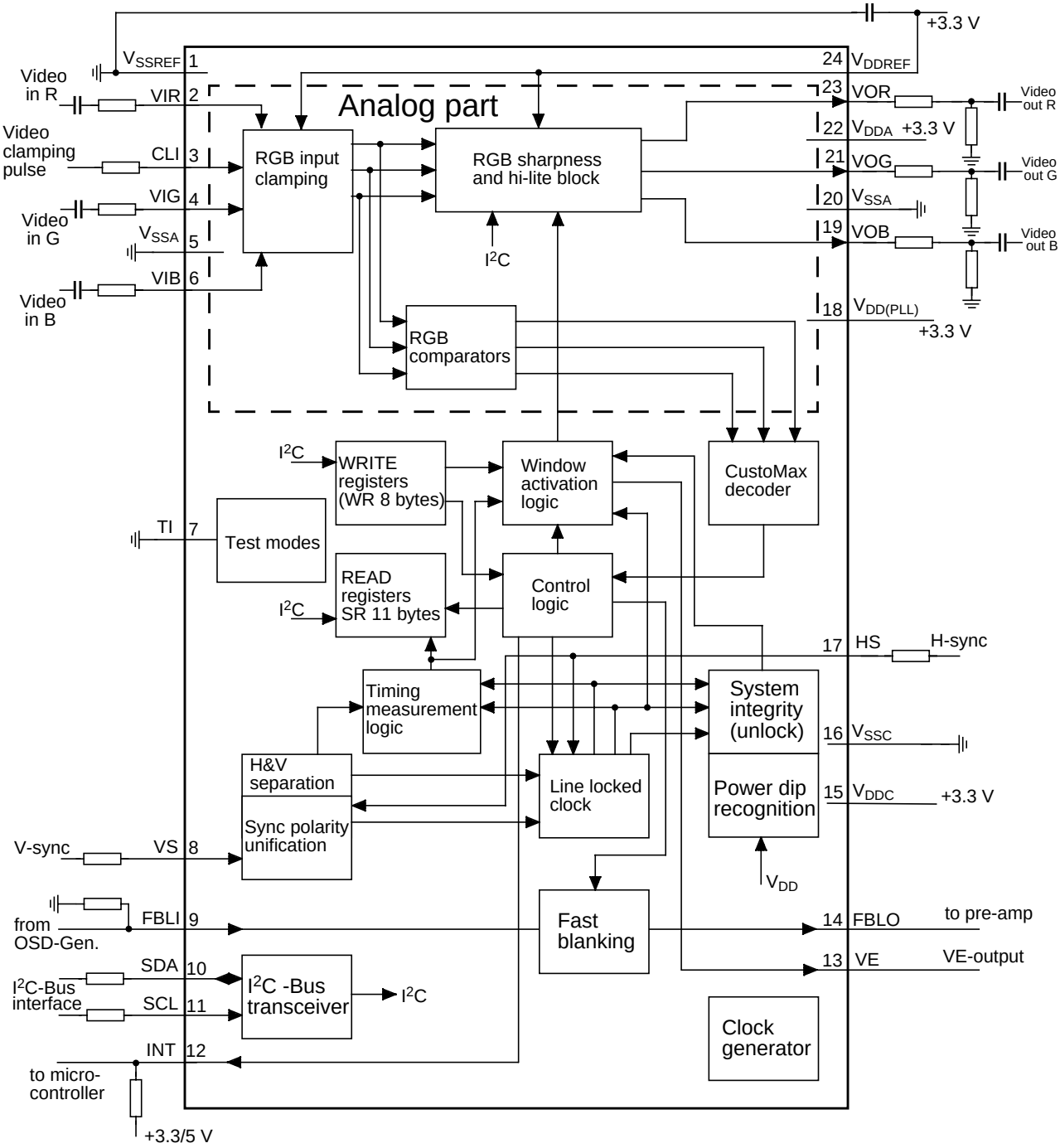


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSREF}	1	reference ground
VIR	2	video input R
CLI	3	clamping input
VIG	4	video signal input G
V_{SSA}	5	analog ground
VIB	6	video input B
TI	7	test mode input
VS	8	vertical sync input
FBLI	9	fast blanking input
SDA	10	I^2C-bus serial data input/output
SCL	11	I^2C-bus clock input
INT	12	interupt output
VE	13	video enhancement output
FBLO	14	fast blanking output
V_{DDC}	15	digital core supply voltage
V_{SSC}	16	digital core ground
HS	17	horizontal sync input
$V_{DD(PLL)}$	18	analog supply voltage
VOB	19	video output B
V_{SSA}	20	supply ground
VOG	21	video out put G
V_{DDA}	22	Supply voltage
VOR	23	video output R
V_{DDREF}	24	Supply reference voltage

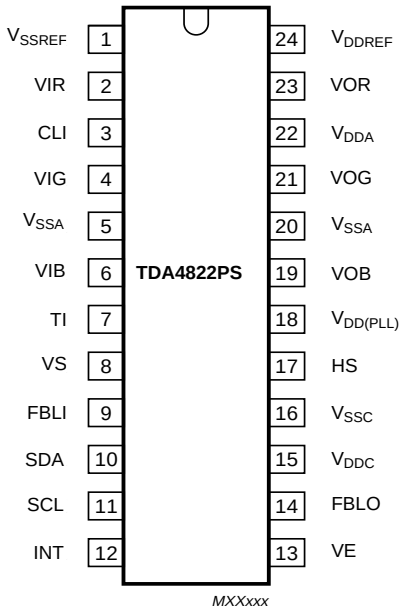


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

The TDA4822PS is an integrated circuit capable of enhancing the visual perception of displayed pictures, internet objects or user selectable screen areas by improving the sharpness and/or increasing the video output signal (done in the analog video section). This IC will be connected in front of the video processor and just after the VGA interface cable connection and is able to resume, decode and process the window/area coordinates as sent by the host PC through the R, G, B lines. These data are encoded in one active line of the video signals based on the (customer specific) CustoMax protocol. The high video bandwidth performance enables an application range from the low end up to the high end segment.

7.1 R, G, B- analog video section

The analogue video section of the TDA4822PS consists of 3 blocks as there are:

1. R, G, B -input clamping

2. R, G, B -sharpness and hi-lite block

3. R,G,B-comparators/slicers

The RGB input signals of the TDA4822PS are assumed to be be RS-370 like (video amplitude on 714 mV; sync amplitude (when present) 286 mV below the black level that is represented by the back porch voltage). As a result the video input performance is compatible with standard video processors (reference is the Philips TDA4887). The only possible difference is related to ultra black sync tips of a Composite Video Signal, that can be left unclipped or partially saturated at the outputs but this will neither degrade the original SoG signal on the VGA input nor influences the VE functionality.

This IC is able to handle high pixel rates without significant bandwidth reduction at the output. That means the rise and fall times tr and tf of the video output signal are very fast without having larger over/undershoots or smearing effects.

7.1.1 R, G, B -input clamping

The R, G, B video signals from the VGA interface are ac-coupled to the video inputs (VIR,VIG,VIB) and their black levels are internally clampled. The clamping signal (CLI) is coming from e.g. the CLBL output of the TDA485x.

7.1.2 R, G, B -comparators/slicers

This block is used to extract the MVL-like message from the last line of the video information. The PC application software provides RGB signals at full amplitude (nominal 714 mV) and the slicing level is then around 40% of the R,G,B signal amplitude (without hysteresis) in order to match some (common) graphic adapter that have a very low video output. The outputs of the R, G, B -slicers are fed to the MVL decoder unit.

7.1.3. R, G, B -sharpness and hi-lite blocks

The activation of the R, G, B -sharpness and hi-lite block is controlled by the VE signal of the window activation block. The VE function can be controlled by the bits WEN (window enable; WR0[1]); SE (sharpness enable; WR1[4]) and HLE (high lite enable; WR1[7]). Clearing these bits (WEN=0; SE=0; HLE=0) will disable these functions. Without VE the nominal gain of the R, G, B -video channels is 0.98.

The R, G, B -video sharpness function has a first order peaking characteristic and both the amplitude (4 levels) and the time constants (4 levels) (see Tables 1 an 2 and Figs 3 and 4) are adjustable via I^2C-Bus in order to optimize the hi-litened window on screen.

The R,G,B -video boosting function (cascaded to the sharpness function) controls 4 levels (see Table 3 and Fig. 5) adjustable via the I^2C-Bus. The activation method is similar to the sharpness function: it is turned on by the VE window /area activation signal , coming from the Window activation logic.

Table 1:Sharpness/peaking amplitude (VE=active)

Sharpness/peaking Amplitude	Bit SA1 WR1(3)	Bit SA0 WR1(2)	Level
1	0	0	110%
2	0	1	120%
3	1	0	130%
4	1	1	140%

The peaking levels are expressed as a percentage of the “unsharpened” (VE =inactive) video signal

Table 2: Time constants of the sharpness/peaking signal (VE =active)

Time constants	Bit STC1 WR1(1)	Bit STC0 WR1(0)	Duration
1	0	0	150 nsec
2	0	1	100nsec
3	1	0	50 nsec
4	1	1	20 nsec

Table 3: Boosting/Hi-lite amplitude (VE =active)

Boosting Amplitude	Bit HLA1 WR1(6)	Bit HLA0 WR1(5)	Level
1	0	0	110%
2	0	1	120%
3	1	0	130%
4	1	1	140%

The boosting levels are expressed as a percentage of the “unsharpened” (VE =inactive) video signal

On the video outputs (VOR,VOG,VOB) the “VE-improved” R, G, B-signals are available. Additional external resistor deviders in each channel (devider factor =0.9) followed by coupling capacitors are used to connect the video pre-amplifier circuit (reference is TDA4887). The resistor deviders are needed due to the limited video voltage range of the video pre-amplifier. The driver capability of VOR,VOG and VOB is limited to 800 Ohms to ground (e.g. 50/75 Ohms loads cannot be driven) and capacitive loads (e.g. PCB tracks) should be reduced to a minimum in order to achieve fast rise and fall times.

7.2 Sync polarity unification/H & V sync separation

The horizontal and vertical sync inputs (HS, VS) are able to handle both 5 or 3.3V level H/V sync input signals and have Schmitt trigger input characteristic. Both signals are internally processed by edge detectors followed by an auto polarity detection and correction circuitry. The autopolarity circuit react in 50% of the line duration of the H-sync- or V-sync signal. This circuitry is able to detect and handle standard H+V composite signals as well as separate sync signals. Other kind of composite TTL H+V signals e.g. signals with serration and/or equalisation pulses cannot be handled.

7.3 Line locked clock

A line locked clock (LLC) is included which locks on the H-sync signal (Pin HS). Together with the internal coast mode detector the LLC maintains its lock even in presence of composite “H &V TTL” signals (both AND and OR’ed composite -sync will be detected) with a V- duration of less or equal than 8 lines (see Fig.6). Other kind of composite TTL H & V signals (e.g. with serration and/or equalisation pulses) cannot be applied . The function of the coast mode detector can be disabled via I^2C-bus (register CMD; see Table 4) for special reasons.

The locking time of the LLC is less than 10 lines (H-periods). An unlock detector is included which detects a LLC deviation of more than 2 clocks lasting for at least 7 lines. In case an unlock is detected and if the bit “unlock disable” (register ULD; see Table 4) has been set before to 0 via I2C-Bus, the VE function, timing measurement logic and the data transmission on the I2C-Bus (no acknoledge) will be shut down then. The unlock/inlock status of the LLC can be read via I2C-Bus by the bit LLCI. The LLCI bit needs an initial setting and this will be done if the RST bit (register WR0[0]) is set to “High”. After that any unlock status of the LLC will immediately sets the LLCI bit ot “Low”

Table 4: LLC Clock multiplier

Bit CMD WR0 [2]	Coast mode disable	Bit ULD WR0 [6]	shut down during unlock	Bit LLCI WR0[7]	LLC
0	normal function	0	yes	0	unlock
1	Coast mode =off	1	no	1	inlock

7.4 CustoMax decoder

As already mentioned, in one active line of the video R, G, B -signal the messages will be sent to the monitor, encoded according the Customax protocol.

On the BLUE channel a clock signal is transmitted (depending on both fH and resolution: it can range from ~ 2 to ~20 Mhz), the Red channel carries the data and the Green channel gives an active High enable signal that lasts the whole active video and that is also used for timing detection (see fig. 7). Clocking is done with the raising edge (blue channel) in the middle of the RED data bit .

Two different types of messages are foreseen: SETUP and COORDINATES as explained in the following:

The 88 bits have the following meanings, depending on the type of message:

Table 5: Setup Message Description

Message	Shift Register	Bits	Description
As	SR& +SR6	12	Identifier =B”100011001001 this data cannot be read by I²C-Bus
Bs	SR6	4	command type; SETUP =B”0011”
Cs	SR5	12	horizontal resolution
Ds	SR5	12	vertical resolution
Es	SR4	12	Initially filled with ‘0’ (see 7.6)
Fs	SR3	12	Initially filed with ‘0’ (see 7.6)
Gs	SR2	12	Initially filled with ‘0’ (see 7.6)
Hs	SR1	4	initially filled with ‘0’
Is	SR1	8	CRC of all the previous bits this data cannot be read by I²C-Bus

Table 6: Coordinates Message Description

Message	Shift Register	Bits	Description
Ac	SR7 +SR6	12	Identifier =B”100011001001 this data cannot be read by I²C-Bus
Bc	SR6	4	command type; COORDINATES=B”101X” note 1
Cc	SR5	12	X coordinate of top left corner window
Dc	SR5	12	Y coordinate of top left corner window
Ec	SR4	12	X coordinate of bottom right corner of window
Fc	SR3	12	Y coordinate of bottom right corner of window
Gc	SR2	8	(VE control byte) Provisional -foreseen for user software control
Hc	SR1	8	bits dummy
Ic	SR1	8	CRC (cycle redundancy check) of all the previous bits; this data cannot be read by I²C-Bus

Note

1. X=don’t care

The 88-bits shift register is devided in 7 smaller shift registers (SR1 -SR7). Once the shift registers have received the (CustoMax) data they can be read by the microcontroller via the I²C-bus and this is indicated by setting the RST bit ;WR0[0]. After sending the CustoMax messages to the registers there is a period of 8 frames until next data are allowed to send.

7.4.1 Register description

The 88 bits stream is loaded into 7 cascaded shift registers (SR1 to SR7). All these behave as a whole shift register in the reception phase, but shift registers SR2, SR3 and SR4 allow also a parallel load (filled by the timing measurement logic) to store the timing parameters (see 7.5). When the SR is read by the micro controller (via I²C-Bus; see 7.7.1 and

7.7.2) , the message part A (SR7 +part of SR6) and I (part of SR1) are not read (both for the SETUP and COORDINATES messages).

The identifier code is stored in two separate shift registers in order to allow the reading of only the type of message by the microprocessor.

7.4.2 Code recognition

The loading and the hardware control of the CRC (cycle redundancy check) is performed through a 7 bits scrambler having polynomial $1+X^{(-1)}+X^{(-5)}+X^{(-7)}$; its initial state is B"1111111". The last 8 bits of the incoming message are calculated in such a way that at the end of the transmission the content of the scrambler is B"00000000" (see Fig. 8) . The complete message has to be recognised as valid if the identifier is acknowledged as correct, as well as the CRC content.

7.5 Timing measurement

Besides knowing the resolution of the displayed active video, for a proper VE operation, it is essential to measure some of the remaining timing parameters that are graphic adapters dependent and cannot be retrieved easily by the software running on PCs.

During the SETUP phase the three 12 bits groups E, F and G (SR4, SR3, SR2) are filled serially with zeroes. If at the end of the transmission the identifier code,the SETUP code and the CRC are correctly recognized, a timing measurement routine will be activated automatically. Clock reference is the internal LLC while reference signals are the H-sync, the V-sync and the G channel (that will fill the entire line independently of the length in pixel of the 88-bits message.) The following measures are executed using a LLC pulses counter and a H-sync (line) counter:

1. The horizontal back porch, measured in number of LLC clock pulses starting at the end (trailing edge) of H-sync and terminating at the leading edge of the Green signal (stored in SR4)

2. The position of the last active pixel in the Green channel of the active video line, measured in number of LLC clock pulses starting at the end (trailing edge)of H-sync (active line + Hor. back porch) (stored in SR3)

3. The position of the last active line, measured in number of H-sync pulses (lines) starting at the leading edge of V-sync (V-sync width + vert. back porch + active video) (stored in SR2).

These measurements constitute the three 12 bits groups E, F and G (SR4, SR3 and SR2) and they are stored (parallel loading) in the registers accordingly. These three parameters are measured only once in the frame that immediately follows the one in which the SETUP command is recognised.

7.6 Data exchange to external microcontroller

7.6.1 Hold-on period and auto reset

After the measurement of the timing parameters is done, an interrupt signal is generated on the pin INT to the external microcontroller, so that it can read the complete stream of the needed information (9 bytes out of the 11 that fill the SR register; identifier and CRC are not read) and generate a reset signal (bit RST of WR0[0] - see Table 8). If, for any reason, the reset signal from the external microcontroller is not generated, an autoreset signal is internally generated at the 8th V-sync pulse after the TDA4822PS acknoledge of SETUP stream. The auto reset allows the TDA4822PS to accept new SETUP or COORDINATES messages, even in the case of no reaction from the external microcontroller.

In the case of COORDINATES message, all the groups are filled directly by the decoded message and, at the end of the reception, an interrupt to the micro is generated provided that the identifier, the COORDINATES code and the CRC are valid. Also in this case the microcontroller has 7 frames time to read the info message and generate the reset, before the autoreset is generated. As soon as the auto reset signal occurs the control logic provides an signal which clears the INT output.

7.6.2 External microcontroller support

Once the system microcontroller has downloaded the contents of the SR group of registers, it performs some simple calculations for converting the window coordinates ,expressed in resolution pixels, in LLC pulse numbers. At the same

time, the micro retrieves from the System EEPROM the preset value of the VE control byte, it packs it with the TDA4822PS control byte and the new window coordinates expressed in LLC pulses and writes, through the I²C bus connection, the WR group of registers.

7.7 I²C-Bus transceiver and register description

The microprocessor is connected to the device through an I²C-Bus transceiver. 9 reading 8-bit registers and 8 writing 8-bit registers are foreseen; the reading registers share the same circuits that latch the incoming video stream and/or allow the parallel load of the timing parameters.

The TDA4822PS device address is: 0110 011X. which means 66H for write and 67H for read. All registers (read or write) are “readable” as well as “writable” via the I²C-Bus.

The I²C-bus interface handle standard I²C-bus features, including auto-increment , so databyte by databyte can be transferred after each other without sending a new subaddress each time. The interface can handle both 100 and 400 kHz I²C-bus standards. The SDA and SCL pins (5 V tolerable I/O’s) have digital filters, which remove all spikes smaller than 60 ns.

The meaning of the registers corresponding to the physical allocation descriptions(Tables 5 and 6) is as follows.Both SETUP(above; Xs) and COORDINATES(below; Xc) messages are shown:

Table 7: I²C-Bus READ Registers (RR) -Subaddresses and data byte format

Register notation	**Sub addr. HEX**	**DATA BYTE**								Notes and register description
		D7	D6	D5	D4	D3	D2	D1	D0	
Read Register 0	08H	As3	As2	As1	As0	Bs3	Bs2	Bs1	Bs0	it contains the last 4 bits (LSB) of the identifier and the 4 bits of the message typ
		Ac3	Ac2	Ac1	Ac0	Bc3	Bc2	Bc1	Bc0	
Read Register 1	09H	Cs11	Cs10	Cs9	Cs8	Cs7	Cs6	Cs5	Cs4	SR5, SR4 and SR3 are here represented. The first bit that comes out of RR 1 is 'shiftout' of SR5 (Cc11). In the SET UP phase these registers contain: -- the horizontal resolution -- the vertical resolution -- the horizontal back porch (SR4) and the position of the last active video (SR3) In the COORDINATES phase these registers contain the coordinates in pixel units of the windows (left, top, right, bottom 12 bit each)
		Cc11	Cc10	Cc9	Cc8	Cc7	Cc6	Cc5	Cc4	
Read Register 2	0AH	Cs3	Cs2	Cs1	Cs0	Ds11	Ds10	Ds9	Ds8	
		Cc3	Cc2	Cc1	Cc0	Dc11	Dc10	Dc9	Dc8	
Read Register 3	0BH	Ds7	Ds6	Ds5	Ds4	Ds3	Ds2	Ds1	Ds0	
		Dc7	Dc6	Dc5	Dc4	Dc3	Dc2	Dc1	Dc0	
Read Register 4	0CH	Es11	Es10	Es9	Es8	Es7	Es6	Es5	Es4	
		Ec11	Ec10	Ec9	Ec8	Ec7	Ec6	Ec5	Ec4	
Read register 5	0DH	Es3	Es2	Es1	Es0	Fs11	Fs10	Fs9	Fs8	
		Ec3	Ec2	Ec1	Ec0	Fc11	Fc10	Fc9	Fc8	
Read Register 6	0EH	Fs7	Fs6	Fs5	Fs4	Fs3	Fs2	Fs1	Fs0	
		Fc7	Fc6	Fc5	Fc4	Fc3	Fc2	Fc1	Fc0	
Read Register 7	0FH	Gs11	Gs10	Gs9	Gs8	Gs7	Gs6	Gs5	Gs4	SR2 and SR1 are here represented. The first bit that comes out of Read Register 7 is 'shiftout" of SR2 (Gc7 or Gs11). SR1 is read only partially. In the SETUP phase these registers contain the position of the last active line (SR2) (the first 12 bits are significant only). In the COORDINATES phase RR 7 is significant only and contains the control parameter byte for the window.
		Gc7	Gc6	Gc5	Gc4	Gc3	Gc2	Gc1	Gc0	
Read Register 8	10H	Gs3	Gs2	Gs1	Gs0	Hs3	Hs2	Hs1	Hs0	
		Hc7	Hc6	Hc5	Hc4	Hc3	Hc2	Hc1	Hc0	

Table 8: I²C-Bus WRITERegisters (WR) -Subaddresses and data byte format

Register notation	**Subaddress (HEX)**		**DATA BYTES**								Notes and register description
	Direct	Buffered	D7	D6	D5	D4	D3	D2	D1	D0	
Write Register 0	00H	80H	LLCI	ULD	0	BLP	VOE	CMD	WEN	RST	It contains the hardware control bits: -RST =reset bit (active high) -WEN = window enable bit (active high) -CMD disables the coast mode detector(High =coast mode is disabled; Low =normal function) -VOE enable the VE output signal on pin 13 (active high) -BLP last row fast blanking enable (active high) -Bit D5 must be set to 0 -ULD=unlock disable ULD=0=shut down during unlock -LLCI =LLC inlock (read bit) LLCI=1= inlock; LLCI=0=unlock
Write Register 1	01H	81H	HLE	HA1	HA0	SE	SA1	SA0	STC1	STC0	It contains the VE control byte -HLE =Hi-Lite enable (active high) -HA1/HA0 = HI-Lite amplitude control over 4 levels -SE = Sharpness enable (active high) SA1/SA2 = sharpness/peaking amplitude over 4 levels -STC1/STC0 =time constant of the peaking
Write Register 2	02H	none	XL11	XL10	XL9	XL8	XL7	XL6	XL5	XL4	These registers contain the window coordinates expressed in LLC clocks: -XL =top left X coordinates -YT = top left Y coordinate -XR = bottom right X coordinate -YB = bottom right Y coordinate All coordinates are 12 bit data.
Write Register 3	03H	none	XL3	XL2	XL1	XL0	YT11	YT10	YT9	YT8	
Write Register 4	04H	none	YT7	YT6	YT5	YT4	YT3	YT2	YT1	YT0	
Write Register 5	05H	none	XR11	XR10	XR9	XR8	XR7	XR6	XR5	XR4	
Write Register 6	06H	none	XR3	XR2	XR1	XR0	YB11	YB10	YB9	YB8	
Write Register 7	07H	none	YB7	YB6	YB5	YB4	YB3	YB2	YB1	YB0	

1.All sub-addresses within the range from RR0 to RR8 and from Write Registers WR2 to WR7 can be addressed by auto increment.

2. Buffered mode availabe for WRITE registers WR0 and WR1

3. After power-up, internal power-on reset of the I^2C-bus or after an unlock detection of the LLC,all the registers are set to their initial value (see following note 4) and an internal power-on reset bit will be set with the consequence that the device will give no acknowledge on the addressing byte after a first addressing. The power-on reset bit will be cleared if the TDA4822PS hardware control register (WR0) is addressed. At the same time, the micro-controller can read the WEN status (now cleared) and have a further confirmation of the occurred "protection".

4. After power-up or internal power-on reset of the I^2C-bus the registers are set to the following values:

4.1. Control bit RST to logic 0

4.2. Control bit WEN to logic 0

4.3. Control bit CMD to logic 0

4.4. Control bit VOE to logic 0 (but not significant

4.5. Control bit BLP to logic 0

4.6. All the other write registers to logic H00

Furthermore the output INT is set to High.

7.8 VE window activation

After the WEN control bit is set to High, this IC loads the VE window/area co-ordinates (XL,YT,XR and YB) in a digital double comparator that is fed also by the LLC counter and by the line counter of the timing detector (see 7.5). The result of this double comparison is the Video Enhancement signal that switches the sharpness block and to the Hi-lite block on/off and is available on the VE output pin too. All these functional blocks became active only when the related enable control bits (SE, HLE and VOE - seeTable 8) are set to HIGH.

The VE function will be switched off if FBLi =high e.g. this will occur if the OSD-generator sends data to the video path.

7.9 Fast blanking

The position of the “data” row, means the row on that the CustoMax data are send,must also be stored and used to generate a specific blanking signal, needed for hiding the messages that come later on this “data” row on the screen. In the fast blanking block an internal signal is generated , which becomes High, when the line counter value is equal with the saved “data” line value. This signal is ORED with the FBLI input signal coming from the OSD generator IC (see Fig. 9) . The output signal of the TDA4822PS is compatible with most of the video pre- processors fast blanking inputs.

The “data” line blanking can be disabled with the bit BLP (WR0[4]). BLP cannot be resetted directly but the following sequence is needed: set BLP =low; set RST high; set RST low again; send MVL data to the TDA4822

7.10 Test circuitry

With the internal test circuitry the testability of this IC will be performed. The test modes can be activated with the pin TI (TI=High). For operation in the functional mode TI has been set to V_{SS}. Via the pins SLC and SDA different test modes can be activated:

Table 9: Activation of the test modes

Pin TI	Pin SDA	Pin SCL	Description
0	X	X	functional mode
1	0	0	scantest normal mode
1	0	1	scantest shift mode
1	1	0	analogue test mode
1	1	1	PLL test mode

The description of the pins in test modes are:

functional mode: all pins are normally used

scantest normal: FBLI =clock

scantest shift: FBLI = clock
FBLO =meas_clk (ringosc. ;typ. 12.5 MHz)
H = scanin1
V = scanin2
INT = scanout1
VE = scanout2

Analogue test: INT = Href
VE = apor
FBLO = inlock

PLL test: INT = Href
VE = coast_mode
FBLO = LLC

Some logic can be turned off by FBLi during the analog test and PLL test:

Analog = coastmode; PLL = coastmode + polarity

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134))

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDC}	core supply voltage (Pin 15)		-0.5	4	V
V_{DDA}	analogue supply voltage (Pin 22)		-0.5	4	V
$V_{DD(PLL)}$	PLL supply voltage (Pin 18)		-0.5	4	V
$V_{I/O5V}$	voltages on VS, FBLI, SDA, SCL, INT and HS, (Pins 8, 9, 10, 11, 12, 17)		-0.5	5.5	V
$V_{I/O}$	voltage on all other I/O pins		-0.5	Vdd+0.5	V
I_{SDA}	DC output sink/source current (Pin 10)	external load	-	20	mA
I_{DDC}	core supply DC current (Pin 15)		-	20	mA
I_{DDA}	analogue supply DC current (Pin 22)	external load on I/O's	-	40	mA
$I_{DD(PLL)}$	PLL supply current (Pin 18)			2	mA
P_{tot}	total power dissipation		-	300	mW
Tstg	storage temperature		-40	+125	°C
Tamb	operating ambient temperature		-20	+70	°C
Tj	operating junction temperature		-20	+125	°C
V_{ES}	electrostatic handling for all pins	Note 1	2000	-	V
		Note 2	400	-	V

Notes

1. Human body model: C=100pF; R=1.5 KΩ
2. Machine model: C=200pF; L=0.75uH; R=0 Ω

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient (in free air)	70	K/W

10 CHARACTERISTICS

V_{DDC}=V_{DDA}=$V_{DD(PLL)}$=V_{DDFEF}= 3.3V T_{amb} = 25 °C; voltages referring to V_{SSC}=V_{SSA}=$V_{ss(PLL)}$ (Pins 16,5, 20) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDC}	core supply voltage (Pin 15)		3	3.3	3.6	V
V_{DDA}	analogue supply voltage (Pin 22)		3	3.3	3.6	V
$V_{DD(PLL)}$	PLL supply voltage (Pin 18)		3	3.3	3.6	V
V_{DDREF}	supply reference voltage (Pin 24)	100nF between V_{DDREF} and V_{SSREF}	3	3.3	3.6	V
I_{DDC}	core supply current (Pin 15)	int. LLC frequency =130MHz int. LLC frequency =65MHz	- -	11 6	14 9	mA mA
I_{DDA}	analogue supply current (Pin 22)		-	20	30	mA
$I_{DD(PLL)}$	PLL supply current (Pin 18)	line frequency =130KHz	-	0.8	1.1	mA
Ptot	total power consumption		-	100	-	mW
V_{POR}	Power dip recognition level		2.4	2.6	2.8	V
R, G, B-analogue video section						
V_{VIR} V_{VIG} V_{VIB}	Peak to peak video input voltage (Pins 2, 4, 6) ;	AC coupled; $C_{1,2,3}$ =10nF	0	-	1	Vpp
$V_{clampVIR}$ $V_{clampVIG}$ $V_{clampVIB}$	clamping level for video inputs	AC coupled; $C_{1,2,3}$ =10nF	0.9	1.0	1.1	V
V_{SLC}	CustoMax-decoder slicing level	for MVL decoding of the last line; VE =off	1.2	-	1.45	V
$V_{VORp-p,}$ V_{VOGp-p} V_{VOBp-p}	Peak to peak video output voltage (Pins 23, 21, 19) ; ac coupled C4,5,6=10nF	Ac coupled to video pre amplifier; $C_{4,5,6}$ =10nF	-	-	1.4	Vpp
V_{VOR0} V_{VOG0} V_{VOB0}	black level output voltage (Pins 23, 21, 19); video input signal =0	clamping signal applied to CLI input	0.85	1.0	1.15	V
I_{clampR} I_{clampG} I_{clampB}	max. clamping current (Pins 2, 4, 6)	input voltage on VIR,VIB, VIG (Pins 2, 4, 6) =0V	350	600	850	uA
R_{load}	resistive output load to V_{SS}		800	1100	-	Ω
C_{load}	capacitive output load		-	-	5	pF
t_r	rise time of video output voltages (VE=inactive)	ext. load =5pF parallel to 1k ; further conditions see: note 1	-	2.7	-	nsec
t_f	fall time of video output voltages (VE=inactive)	ext. load =5pF parallel to 1k ; further conditions see: note 1	-	2.3	-	nsec
d_t	delay time from video input to output (VE=inactive)	ext. load =5pF parallel to 1k ; further conditions see: note 1	-	2.5	-	nsec
dV	Over/undershoot (VE= inactive)	ext. load =5pF parallel to 1k ; further conditions see: note 1	-	10	-	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\alpha_{ctsignal}$	cross talk among the channels	f_{video}=50MHz sinewave see: note 2	35	-	-	dB
$\alpha_{ctnoise}$	signal to noise ratio (single channel operation)	α_{ct}=nom. video sig./RMS noise see: note 3	-	50	-	dB
$Vu_{nominal}$	nominal gain (VE inactive) $V_{VOR,G,B}/V_{VIR,G,B}$	note 1	0.93	0.98	1.03	
$Vu_{contrast}$	gain boosting (VE= active) ($V_{VOR,G,B(VE=active)}/V_{VOR,G,B(VE=inactive)}$					
	HLA=00H		105	110	115	%
	HLA=03H		135	140	145	%
dV_{VE}	deviation among the channels during VE=active	video input signal =700mV gain boosting=140%	-	-	3	%
$Vu_{sharpness}$	sharpness/peaking boosting (VVOR,G,B(VE=active)/VVOR,G,B(VE=inactive)	ext. load =5pF parallel to 1.1 k ; further conditions see: note 1+5 for $T_{sharpness}$ =50/100/150nsec				
	SA=00H		105	110	-	%
	SA=03H		140	145	-	%
$T_{sharpness}$	time constant of sharpness/peaking boosting	note 1 and 4				
	STC=00H		-	150	-	nsec
	STC=03H		-	20	-	nsec
t_{VE}	High lite activation speed	see: note 5	-	2.5	6	nsec
$dV_{VEon/off}$	max. VE active/inactive switching over/undershoot	see: note 5	-	10	-	%
Clamping circuit						
t_{clamp}	pulse width of clamping signal (Pin 3)		0.4	-	-	usec
V_{CLITH}	clamping activation threshold voltage on CLI (PIN 3)		1.8	2.1	2.4	V
I_{CLI}	current into CLI (Pin 3)	V_{CLI} =2.1V	-	350	-	uA
V_{CLIMAX}	max. allowed voltage on CLI (PIN 3)		-	5	5.25	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LLC						
F_{HS}	H-sync input frequency		30	-	130	KHz
F_{LLC}	Internal LLC frequency		30.8		132	MHz
t_{onPLL}	LLC start up time after power on		-	-	3	msec
t_{lockin}	lock in time (expressed in H-lines)	after e.g. mode changes or recovery from power save mode	-	-	10	
$t_{composite}$	V-duration of H&V composite sync signal (expressed in horizontal lines)	note 6	-	-	8	
Ring oscillator						
F_{ring}	internal ring oscillator frequency	measured in scantest shift mode	9	12.5	15	MHz
Digital inputs and outputs						
input pin FBLI (Pin 9)						
V_{IL}	Low level input voltage		-	-	0.8	V
V_{IH}	High level input voltage		2	-	-	V
I_{IK}	input leakage current		-	-	2	µA
V_{INmax}	max. input voltage range		0	-	5.25	V
input pins VS and HS (Pins 8, 17)						
V_{IL}	Low level input voltage (Schmitt trigger)	falling edge (hysteresis input)	0.9	-	1.35	V
V_{IH}	High level input voltage (Schmitt trigger)	rising edge (hysteresis input)	1.3	-	1.9	V
I_{IK}	input leakage current		-	-	2	uA
V_{INmax}	max. input voltage range				5.25	V
I^2C-Bus input/output pins SDA and SCL (Pin 10, 11)						
V_{IL}	Low level input voltage		-	-	$0.3V_{DD}$	V
V_{IH}	High level input voltage		$0.7V_{DD}$	-	-	V
I_{IK}	Input leakage current		-	-	2	µA
V_{OL}	Low level output voltage	I_{OL}=3mA	-	-	$0.3V_{DD}$	V
V_{OH}	High level output voltage	I_{OL}=-3mA	$0.7V_{DD}$	-	-	V
V_{INmax}	max. voltage range	external pull up resistor to 5V	0	-	5,25	V
I_{OL}	SDA output current	external load	-	-	3	mA
F_{BUS}	max IIC-bus clock frequency		-	-	400	KHz
output pins VE, FBLO (Pin13, 14)						
d_{tFBL}	delay time from FBLI to FBLO	external load=5pF	-	3	-	nsec
$t_{r,f\text{-}FBL}$	rise/fall time of FBLO	external load=5pF	-	1.5	-	nsec
$t_{r,f\text{-}VE}$	rise/fall time of VE-output	external load =5pF	-	1.5	-	nsec
V_{OL}	Low level output voltage		-	-	0.4	V
V_{OH}	High level output voltage		0.85 V_{DD}	-	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OUTmax}	max. voltage range		0		V_{DD}	V
I_{OL}	output current			-	2	mA
output pin INT (Pin 12)						
V_{OL}	Low level output voltage		-	-	0.4	V
V_{OH}	High level output voltage		0.85 V_{DD}	-	-	V
V_{OUTmax}	max. voltage range	pull up resistor to 5V supply	0		5.25	V
I_{OL}	output current		-	-	2	mA

Notes:

1: External load =1.1kΩ parallel to 5pF; input rise/fall time =1ns; measurement of tr/tf at10 to 90% amplitude; nominal video output signal =700mV

2: sine wave signal applied to one channel and measure the crosstalk on the other 2 video outputs.

3: S/N =(nominal video signal)/(RMS noise); noise on the 3 video outputs related to nominal video output signal (700mV)

4: Definition of the sharpness time constants: duration of sharpness amplitude >33% of the max. peak amplitude

5: switching characteristic from VE=inactive to active or VE= active to inactive

6. For some composite sync modes a V-duration of >8 horizontal lines will be detected correctly.

10.1 Windowed VE functions

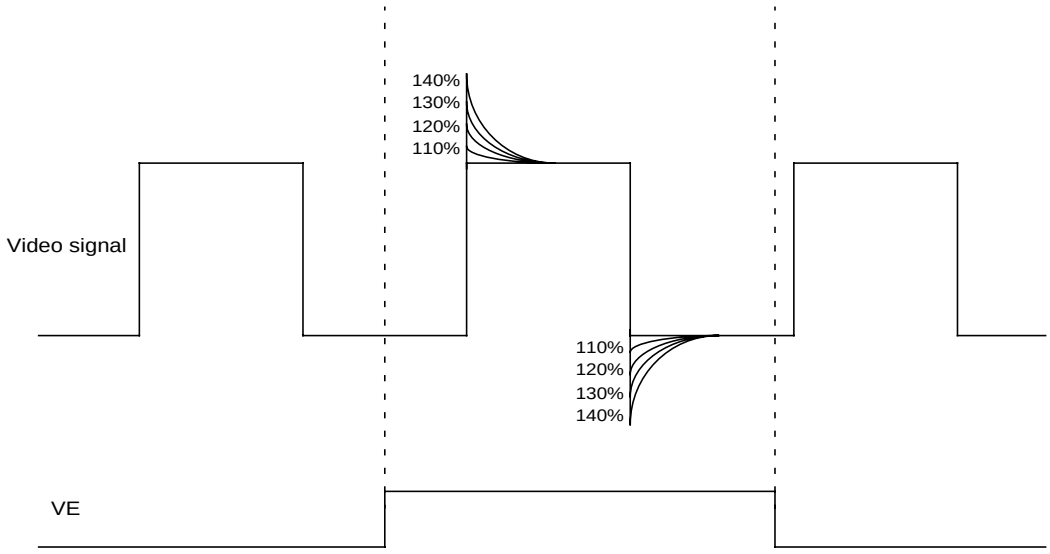


Fig.3 Sharpness amplitudes

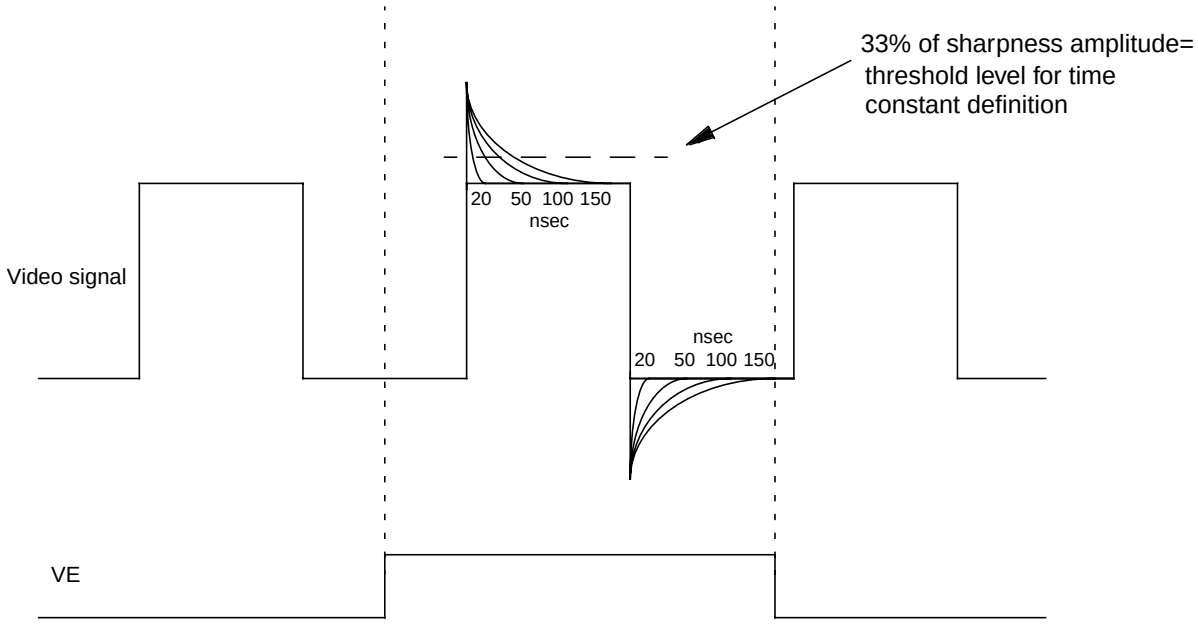


Fig.4 Sharpness time constants

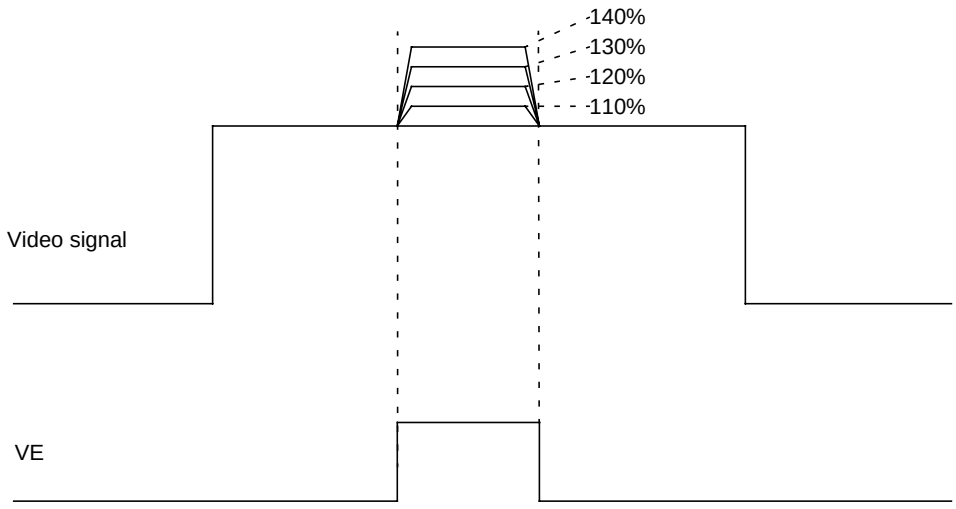


Fig.5 Hi-lite amplitudes

10.2 Timing diagrammes

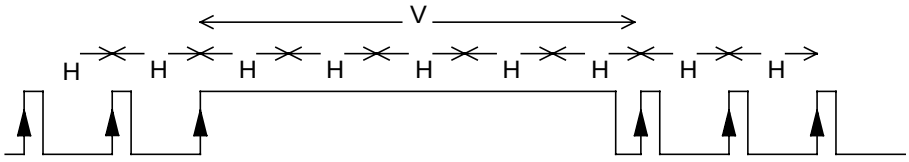


Fig.6 Example of a composite H+V TTL signal

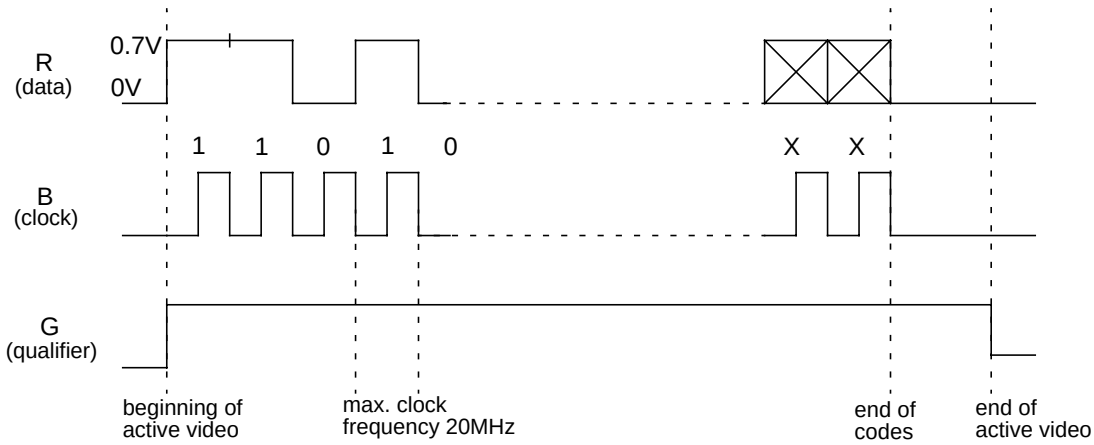


Fig.7 MVL-like code transmission

10.3 Block description

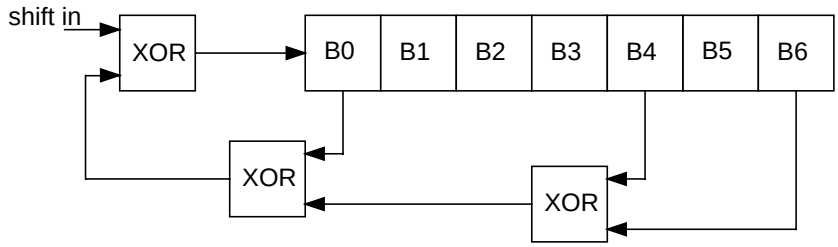


Fig.8 Code recognition scrambler block

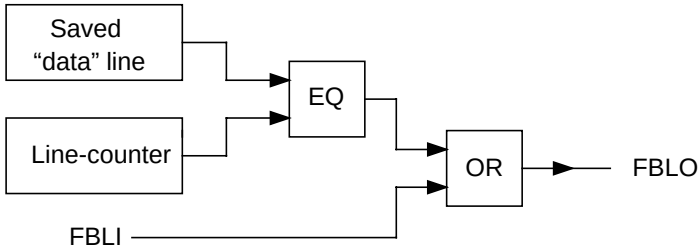


Fig.9 Fast blanking block

11 APPLICATION INFORMATION

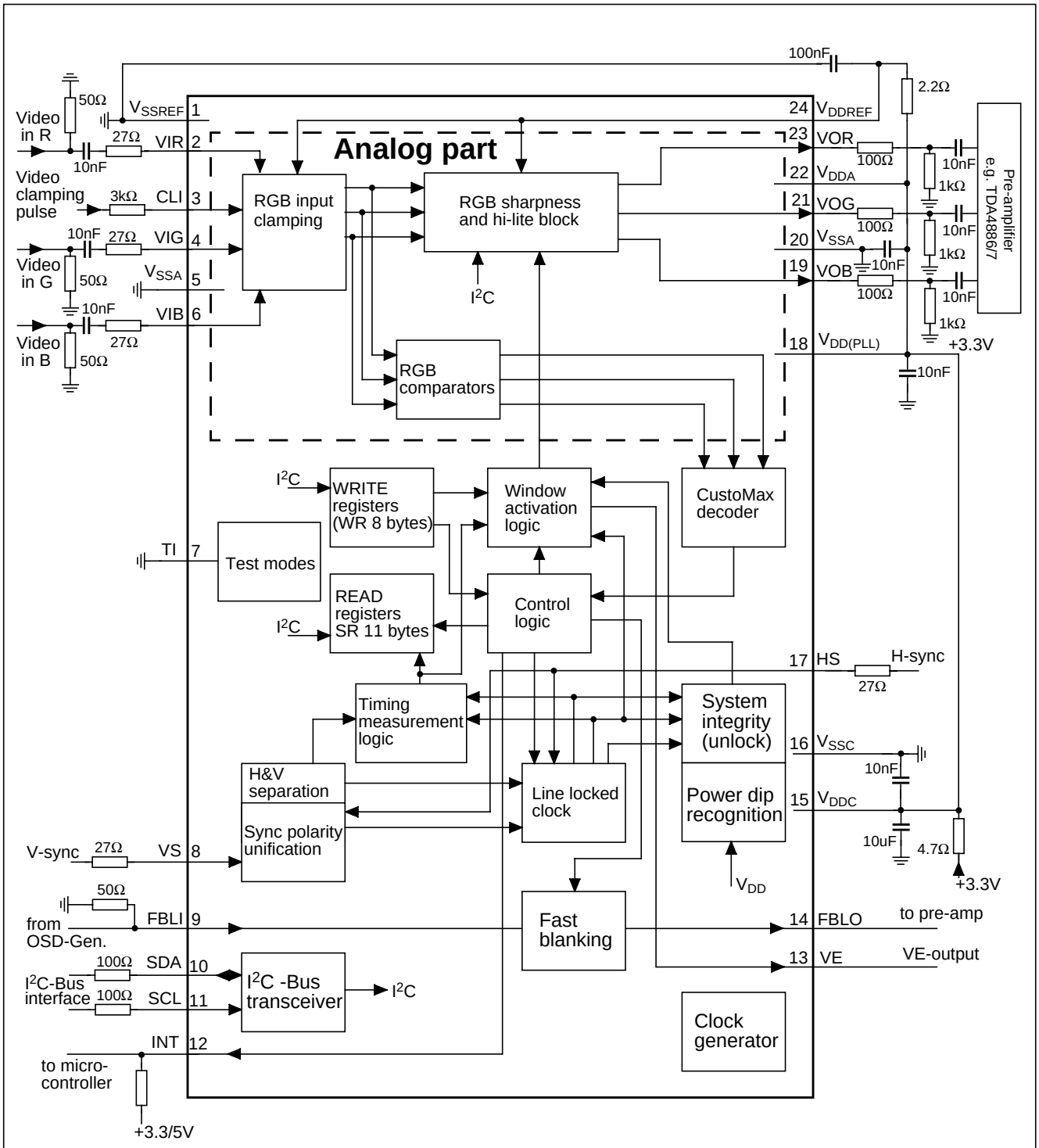
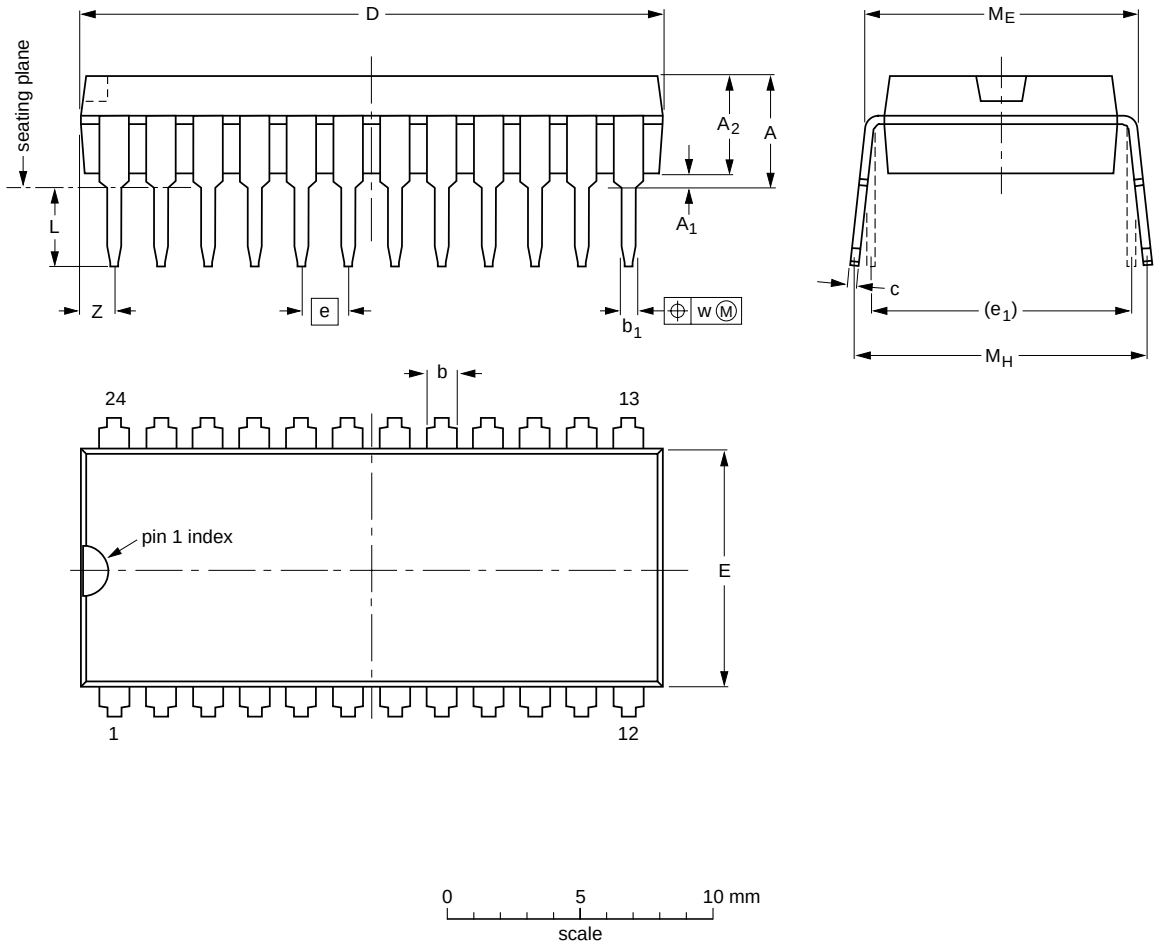


Fig.10 Application diagram.

SDIP24: plastic shrink dual in-line package; 24 leads (400 mil) **SOT234-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	22.3 21.4	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT234-1						~~92-11-17~~ 95-02-04