INTEGRATED CIRCUITS

# DATA SHEET

# TDA6111Q
## Video output amplifier

Preliminary specification
Supersedes data of February 1992
File under Integrated Circuits, IC02

1995 Feb 07

Philips Semiconductors

PHILIPS

## FEATURES

- High bandwidth and high slew rate
- Black-current measurement output for Automatic Black-current Stabilization (ABS)
- Two cathode outputs; one for DC currents, and one for transient currents
- A feedback output separated from the cathode outputs
- Internal protection against positive appearing Cathode-Ray Tube (CRT) flashover discharges
- ESD protection
- Simple application with a variety of colour decoders
- Differential input with a designed maximum common mode input capacitance of 3 pF, a maximum differential mode input capacitance of 0.5 pF and a differential input voltage temperature drift of 50 µV/K
- Defined switch-off behaviour.

## GENERAL DESCRIPTION

The TDA6111Q is a video output amplifier with 16 MHz bandwidth. The device is contained in a single in-line 9-pin medium power (DBS9MPF) package, using high-voltage DMOS technology, intended to drive the cathode of a colour CRT.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{DDH}$ | high level supply voltage | | 0 | – | 250 | V |
| $V_{DDL}$ | low level supply voltage | | 0 | – | 14 | V |
| $I_{DDH}$ | quiescent high voltage supply current | $V_{oc} = 0.5V_{DDH}$ | 7.0 | 9.0 | 11.0 | mA |
| $I_{DDL}$ | quiescent low voltage supply current | $V_{oc} = 0.5V_{DDH}$ | 5.0 | 6.8 | 8.0 | mA |
| $V_I$ | input voltage | | 0 | – | $V_{DDL}$ | V |
| $V_{oc}$, $V_{fb}$ | output voltage | | $V_{DDL}$ | – | $V_{DDH}$ | V |
| $T_{stg}$ | storage temperature | | –55 | – | +150 | °C |
| $T_{amb}$ | operating ambient temperature | | –20 | – | +65 | °C |

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| TDA6111Q | DBS9MPF | plastic DIL-bent-SIL medium power package with fin; 9 leads | SOT111-1 |

## BLOCK DIAGRAM

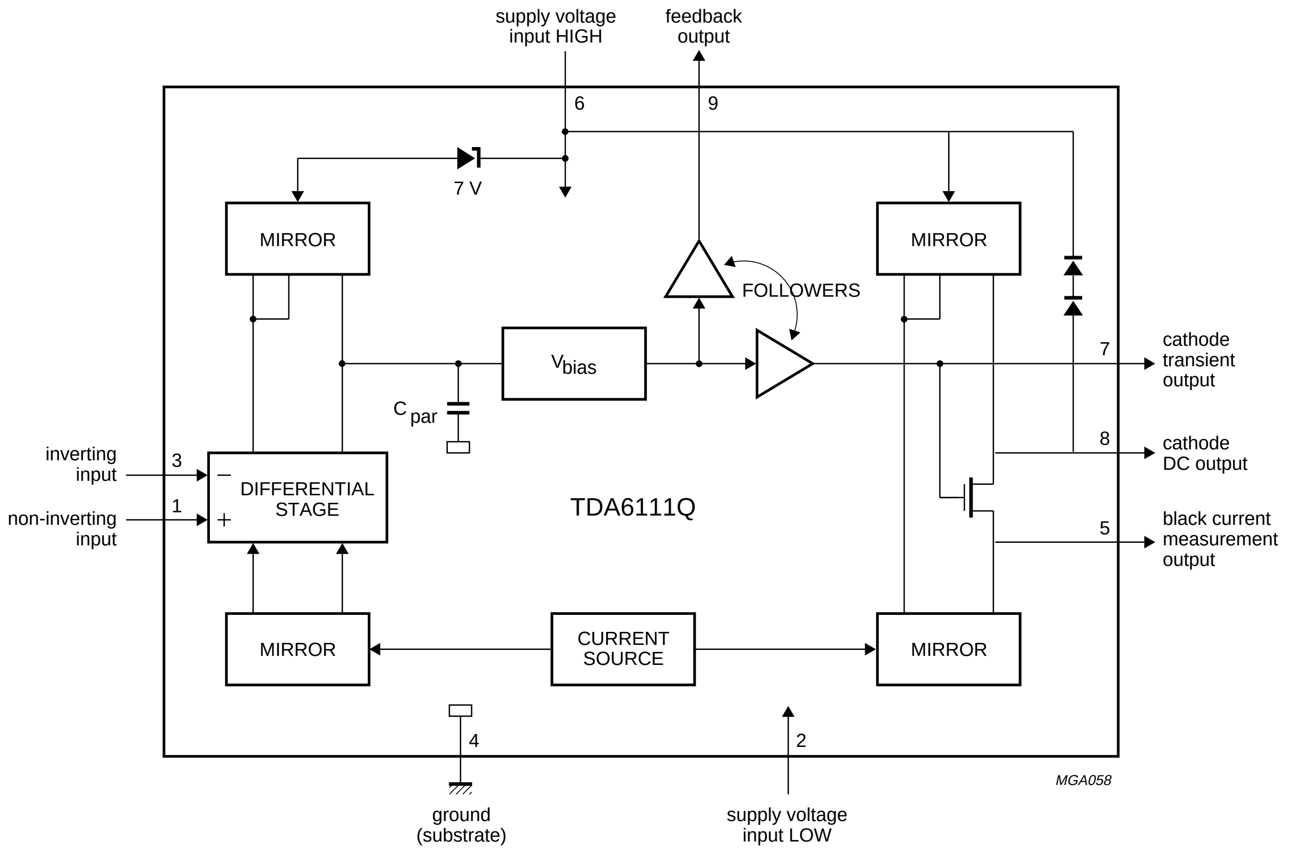



Fig.1 Block diagram.

## PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| $V_{ip}$ | 1 | non-inverting voltage input |
| $V_{DDL}$ | 2 | supply voltage LOW |
| $V_{in}$ | 3 | inverting voltage input |
| GND | 4 | ground, substrate |
| $I_{om}$ | 5 | black current measurement output |
| $V_{DDH}$ | 6 | supply voltage HIGH |
| $V_{cn}$ | 7 | cathode transient voltage output |
| $V_{oc}$ | 8 | cathode DC voltage output |
| $V_{fb}$ | 9 | feedback voltage output |

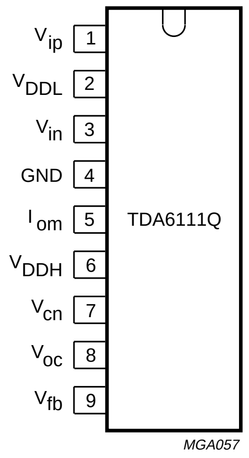



Fig.2 Pin configuration.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages measured with respect to GND (pin 4); currents as specified in Fig.1; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DDH}$ | high level supply voltage | | 0 | 250 | V |
| $V_{DDL}$ | low level supply voltage | | 0 | 14 | V |
| $V_I$ | input voltage | | 0 | $V_{DDL}$ | V |
| $V_{Idm}$ | differential mode input voltage | | –6 | +6 | V |
| $V_{om}$ | measurement output voltage | | 0 | $V_{DDL}$ | |
| $V_{oc}$ | cathode output voltage | | $V_{DDL}$ | $V_{DDH}$ | V |
| $V_{fb}$ | feedback output voltage | | $V_{DDL}$ | $V_{DDH}$ | V |
| $I_{in}$,$I_{ip}$ | input current | | 0 | 1 | mA |
| $I_{ocsmL}$ | low non-repetitive peak cathode output current | flashover discharge = 100 µC | 0 | 5 | A |
| $I_{ocsmH}$ | high non-repetitive peak cathode output current | flashover discharge = 100 nC | 0 | 10 | A |
| $P_{tot}$ | total power dissipation | | 0 | 4 | W |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| $T_j$ | junction temperature | | –20 | +150 | °C |
| $V_{es}$ | electrostatic handling | | | | |
| | human body model (HBM) | | – | > 1500 | V |
| | machine model (MM) | | – | > 400 | V |

## HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

## QUALITY SPECIFICATION

Quality specification *"SNW-FQ-611 part E"* is applicable, except for ESD Human body model see Chapter "Limiting values", and can be found in the *"Quality reference handbook"* (ordering number 9398 510 63011).

## THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | VALUE | UNIT |
|---|---|---|---|
| $R_{th\ j\text{-}c}$ | thermal resistance from junction to case (note 1) | 12 | K/W |

**Note**

1. External heatsink is required.

## CHARACTERISTICS

Operating range: $T_{amb}$ = –20 to 65 °C; $V_{DDH}$ = 180 to 210 V; $V_{DDL}$ = 10.8 to 13.2 V; $V_{ip}$ = 2.6 to 5 V; $V_{om}$ = 1.4 V to $V_{DDL}$.

Test conditions (unless otherwise specified): $T_{amb}$ = 25 °C; $V_{DDH}$ = 200 V; $V_{DDL}$ = 12 V; $V_{ip}$ = 5 V; $V_{om}$ = 6 V; $C_L$ = 10 pF ($C_L$ consists of parasitic and cathode capacitance); $R_{th\text{-}heatsink}$ = 10 K/W; measured in test circuit Fig.3.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{DDH}$ | quiescent HIGH voltage supply current | $V_{oc} = 0.5V_{DDH}$ | 7.0 | 9.0 | 11.0 | mA |
| $I_{DDL}$ | quiescent LOW voltage supply current | $V_{oc} = 0.5V_{DDH}$ | 5.0 | 6.8 | 8.0 | mA |
| $I_{bias}$ | input bias current | $V_{oc} = 0.5V_{DDH}$ | 0 | – | 40 | μA |
| $I_{offset}$ | input offset current | $V_{oc} = 0.5V_{DDH}$ | –6 | – | +6 | μA |
| $I_{om(offset)}$ | offset current of measurement output | $I_{oc}$ = 0 μA; –1.0 V < $V_{1-3}$ < 1.0 V; 1.4 V < $V_{om}$ < $V_{DDL}$ | –10 | 0 | +10 | μA |
| $\frac{\Delta I_{om}}{\Delta I_{oc}}$ | linearity of current transfer | –10 μA < $I_{oc}$ < 3 mA; –1.0 V < $V_{1-3}$ < 1.0 V; 1.4 V < $V_{om}$ < $V_{DDL}$ | 0.9 | 1.0 | 1.1 | |
| $V_{offset}$ | input offset voltage | $V_{oc} = 0.5V_{DDH}$ | –50 | – | +50 | mV |
| $V_{oc(min)}$ | minimum output voltage | $V_{1-3}$ = –1 V | – | – | 20 | V |
| $V_{oc(max)}$ | maximum output voltage | $V_{1-3}$ = –1 V | $V_{DDH}$ – 12 | – | – | V |
| GB | gain-bandwidth product of open-loop gain: $V_{fb}$ / $V_{i,\,dm}$ | f = 500 kHz; $V_{ocDC}$ = 100 V | – | 1.6 | – | GHz |
| $B_S$ | small signal bandwidth | $V_{ocAC}$ = 60 V (p-p); $V_{ocDC}$ = 100 V | 13 | 16 | – | MHz |
| $B_L$ | large signal bandwidth | $V_{ocAC}$ = 100 V (p-p); $V_{ocDC}$ = 100 V | 10 | 13 | – | MHz |
| $t_{pd}$ | cathode output propagation delay time 50% input to 50% output | $V_{ocAC}$ = 100 V (p-p); $V_{ocDC}$ = 100 V square wave; f < 1 MHz; $t_r = t_f$ = 22 ns; see Figs 4 and 5 | 17 | 23 | 29 | ns |
| $t_r$ | cathode output rise time 10% output to 90% output | $V_{oc}$ = 50 to 150 V square wave; f < 1 MHz; $t_f$ = 22 ns; see Fig.4 | 23 | 30 | 36 | ns |
| $t_f$ | cathode output fall time 90% output to 10% output | $V_{oc}$ = 150 to 50 V square wave; f < 1 MHz; $t_r$ = 22 ns; see Fig.5 | 23 | 30 | 36 | ns |
| $t_s$ | settling time 50% input to (99% < output < 101%) | $V_{ocAC}$ = 100 V (p-p); $V_{ocDC}$ = 100 V square wave; f < 1 MHz; $t_r = t_f$ = 22 ns; see Figs 4 and 5 | – | – | 350 | ns |
| SR | slew rate between 50 V to 150 V | $V_{1-3}$ = 2 V (p-p) square wave; f < 1 MHz; $t_r = t_f$ = 22 ns | – | 3000 | – | V/μs |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $O_v$ | cathode output voltage overshoot | $V_{ocAC}$ = 100 V (p-p); $V_{ocDC}$ = 100 V square wave; f < 1 MHz; $t_r = t_f$ = 22 ns; see Figs 4 and 5; note 1 | – | 9 | – | % |
| SVRRH | high supply voltage rejection ratio | f < 50 kHz; note 2 | – | 85 | – | dB |
| SVRRL | low supply voltage rejection ratio | f < 50 kHz; note 2 | – | 70 | – | dB |

**Notes**

1. If the difference between $V_{DDL}$ and $V_{ip}$ is less than 7 V, overshoot cannot be specified.
2. SVRR: The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.

### Cathode output

The cathode output is protected against peak currents (caused by positive voltage peaks during high-resistance flash) of 5 A maximum with a charge content of 100 µC.

The cathode is also protected against peak currents (caused by positive voltage peaks during low-resistance flash) of 10 A maximum with a charge content of 100 nC.

### Flashover protection

The TDA6111Q incorporates protection diodes against CRT flashover discharges that clamp the cathode output pin to the $V_{DDH}$ pin. The DC supply voltage at the $V_{DDH}$ pin has to be within the operating range of 180 to 210 V to ensure that the Absolute Maximum Rating for $V_{DDH}$ of 250 V will not be exceeded during flashover. To limit the diode current, an external 680 Ω carbon high-voltage resistor in series with the cathode output and a 2 kV spark gap are needed (for this resistor-value, the CRT has to be connected to the main PCB). This addition produces an increase in the rise and fall times of approximately 5 ns and a decrease in the overshoot of approximately 4%.

$V_{DDH}$ to GND must be decoupled:

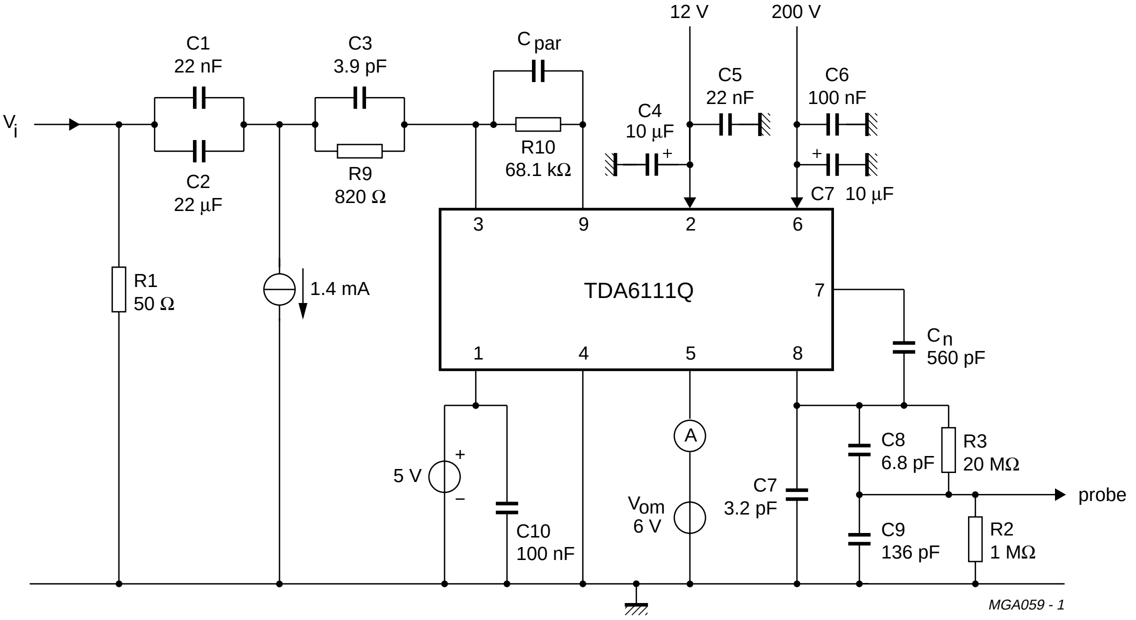
1. With a capacitor >20 nF with good HF behaviour (e.g. foil). This capacitance must be placed as close as possible to pins 6 and 4, but definitely within 5 mm.
2. With a capacitor >10 µF on the picture tube base print (common for three output stages).

$V_{DDL}$ to GND must be decoupled:

1. With a capacitor >20 nF with good HF behaviour (e.g. ceramic). This capacitance must be placed as close as possible to pins 2 and 4, but definitely within 10 mm.

### Switch-off behaviour

The switch-off behaviour of the TDA6111Q is defined: when the bias current becomes zero, at $V_{DDL}$ (pin 2) lower than approximately 5 V, all the output pins (pins 7, 8 and 9) will be high.




$C_{par}$ = 150 fF.

Fig.3 Test circuit with feedback factor $1/83$.

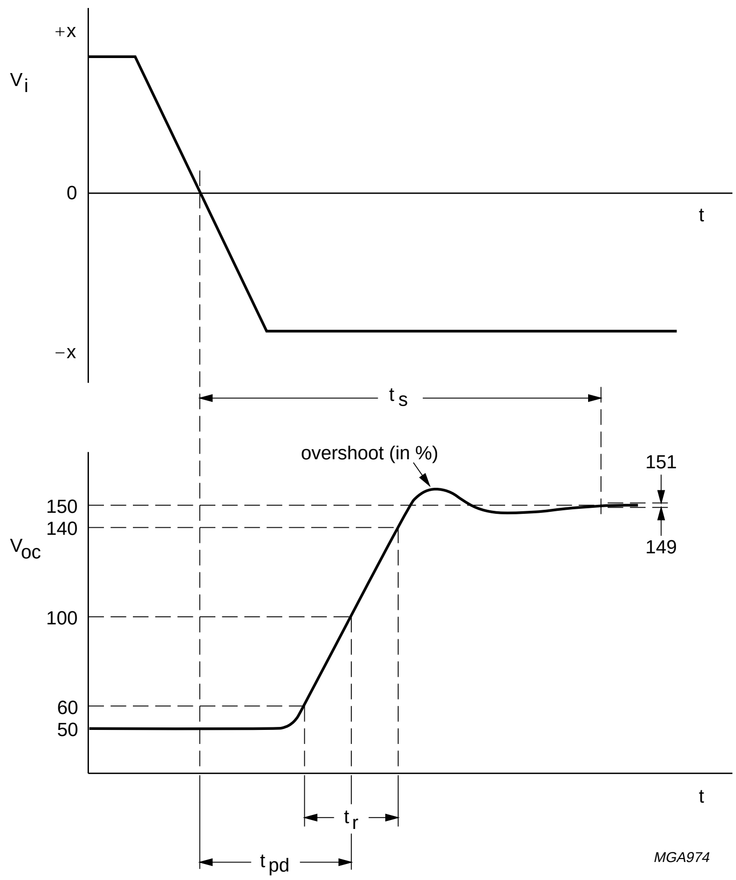



Fig.4 Output voltage (pin 8) rising edge as a function of the AC input signal.

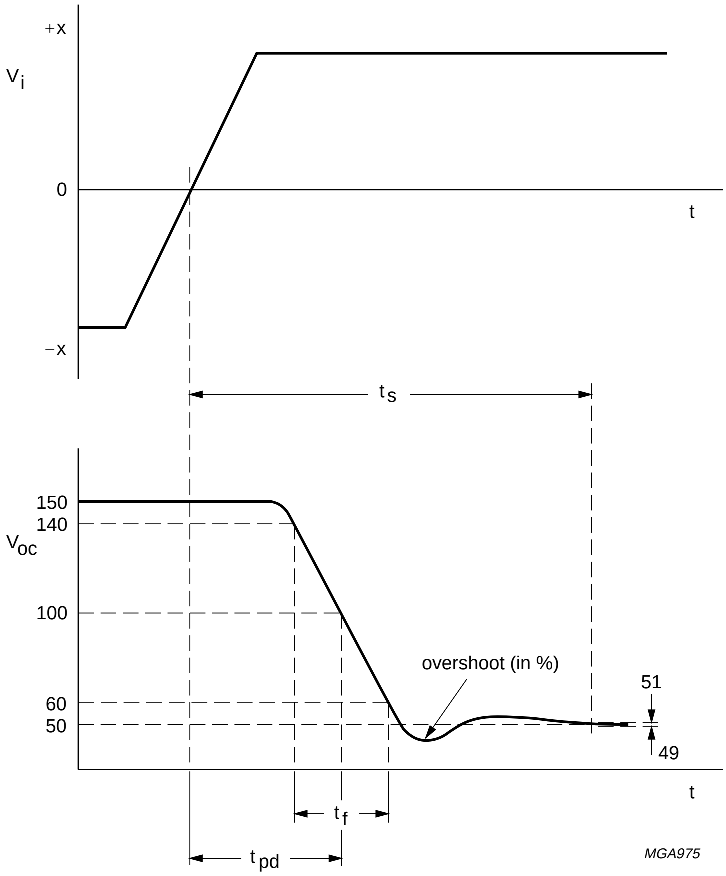



Fig.5 Output voltage (pins 8) falling edge as a function of the AC input signal.

## TEST AND APPLICATION INFORMATION

### Dissipation

Regarding dissipation, distinction must first be made between static dissipation (independent of frequency) and dynamic dissipation (proportional to frequency).

The static dissipation of the TDA6111Q is due to high and low voltage supply currents and load currents in the feedback network and CRT.

The static dissipation equals:

$$P_{stat} = V_{DDL} \times I_{DDL} + V_{DDH} \times I_{DDH} + V_{oc} \times I_{oc} - V_{fb} \times \left(\frac{V_{fb}}{R_{fb}}\right)$$

$R_{fb}$ = value of feedback resistor.

$I_{oc}$ = DC value of cathode current.

With $V_{fb} = V_{oc} = 100$ V, $R_{fb} = 68$ kΩ, $I_{oc} = 0.6$ mA and other typical conditions as mentioned in Chapter “Characteristics”, the static dissipation $P_{stat} = 2.0$ W.

The dynamic dissipation equals:

$$P_{dyn} = V_{DDH} \times (C_L + C_{fb} + C_{int}) \times f_i \times V_{o(p-p)} \times \delta$$

$C_L$ = load capacitance.

$C_{fb}$ = feedback capacitance (≈ 150 fF).

$C_{int}$ = internal load capacitance (≈ 4 pF).

$f_i$ = input frequency.

$V_{o(p-p)}$ = output voltage (peak-to-peak value).

$\delta$ = non-blanking duty-cycle (≈ 0.8).

With $C_L = 10$ pF, $C_{fb} = 0$, $C_{int} = 4$ pF, $f_i = 8$ MHz (simulation of worst-case noise), $V_{o(p-p)} = 100$ V and $\delta = 80\%$ then $P_{dyn} = 1.8$ W

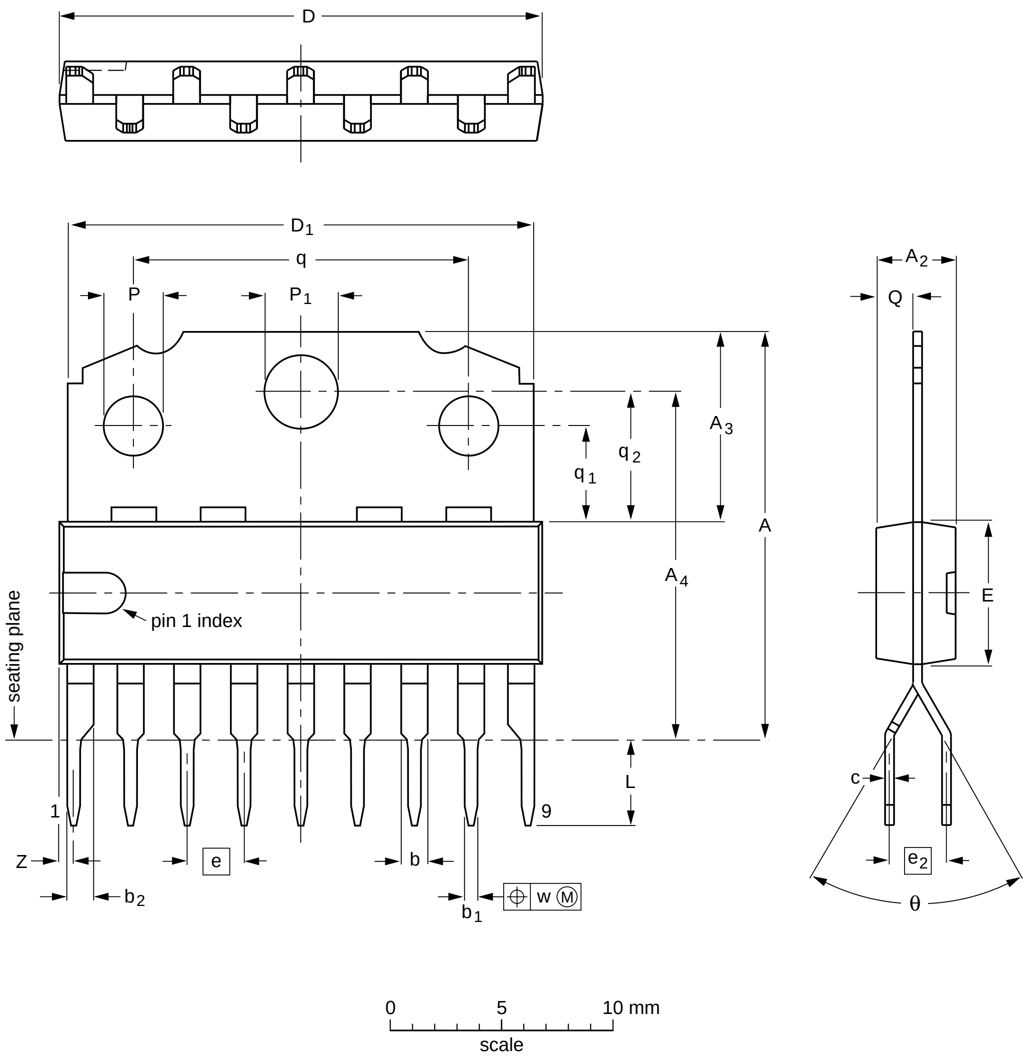
The IC must be mounted on the picture tube base print to minimize the load capacitance ($C_L$).

The total power dissipation, $P_{tot} = P_{stat} + P_{dyn}$ thus amounts to 3.6 W under given conditions.

From $T_j = T_{amb} + P_{tot} \times R_{th\ j\text{-}a} < T_{j(max)} = 150$ °C, $R_{th\ j\text{-}a}$ of the package and heatsink together must be < 24 K/W.

## PACKAGE OUTLINE

**DBS9MPF: plastic DIL-bent-SIL medium power package with fin; 9 leads** **SOT111-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_2$ max. | $A_3$ | $A_4$ | b | $b_1$ | $b_2$ | c | $D^{(1)}$ | $D_1$ | $E^{(1)}$ | e | $e_2$ | L | P | $P_1$ | Q | q | $q_1$ | $q_2$ | w | $Z^{(1)}$ max. | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 18.5<br>17.8 | 3.7 | 8.7<br>8.0 | 15.5<br>15.1 | 1.40<br>1.14 | 0.67<br>0.50 | 1.40<br>1.14 | 0.48<br>0.38 | 21.8<br>21.4 | 21.4<br>20.7 | 6.48<br>6.20 | 2.54 | 2.54 | 3.9<br>3.4 | 2.75<br>2.50 | 3.4<br>3.2 | 1.75<br>1.55 | 15.1<br>14.9 | 4.4<br>4.2 | 5.9<br>5.7 | 0.25 | 1.0 | $65^{o}$<br>$55^{o}$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT111-1 | | | | | | ~~92-11-17~~<br>95-03-11 |

## SOLDERING

### Plastic single in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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