INTEGRATED CIRCUITS



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TDA6120Q

FEATURES

- High large signal bandwidth of 32 MHz (typ.) at 125 V (p-p)
- High small signal bandwidth of 47 MHz (typ.) at 60 V (p-p)
- Rise/fall time of 12.5 ns for 125 V (p-p)
- High slew rate of 10 V/ns
- Low static power dissipation of 2.5 W at 200 V supply voltage
- High maximum output voltage
- Bandwidth independent of voltage gain
- Maximum overall voltage gain over 46 dB
- High Power Supply Rejection Ratio (PSRR)
- Fast cathode current measurement output for dark current control loop
- Differential voltage input.

ORDERING INFORMATION

GENERAL DESCRIPTION

The TDA6120Q is a single 30 MHz, 125 V (p-p) video output amplifier contained in a plastic DIL-bent-SIL power package. The device uses high-voltage DMOS technology and is intended to drive the cathodes of a CRT in High Definition TVs (HDTVs) or monitors.

TYPE		PACKAGE								
NUMBER	NAME	DESCRIPTION	VERSION							
TDA6120Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 7.7 mm)	SOT141-8							

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BLOCK DIAGRAM





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PINNING

SYMBOL	PIN	DESCRIPTION
RC-	1	inverting input pre-emphasis network
VIN–	2	inverting voltage input
RC+	3	non-inverting input pre-emphasis network
VIN+	4	non-inverting voltage input
lin	5	feedback current input
V _{CC}	6	low supply voltage (12 V)
OUTM	7	cathode current measurement output
GND	8	power ground and heatsink
n.c.	9	not connected
V _{DD}	10	high supply voltage (200 V)
n.c.	11	not connected
OUTC	12	cathode output
OUT	13	feedback output



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DD}	high supply voltage		0	280	V
V _{CC}	low supply voltage		0	20	V
Vi	input voltage (pins 2 and 4)		0	V _{CC}	V
V _{i(dif)}	differential mode input voltage (pins 2 and 4)		-V _{CC}	V _{CC}	V
V _{i(pe)}	pre-emphasis input voltage (pins 1 and 3)		0	V _{CC}	V
V _{i(dif)(pe)}	differential mode pre-emphasis input voltage (pins 1 and 3)		-V _{CC}	V _{CC}	V
V _{IIN}	input voltage (pin 5)		0	2V _{BE}	V
V _{OUTM}	measurement output voltage		0	20	V
Vo	output voltage (pins 12 and 13)		0	V _{DD}	V
T _{stg}	storage temperature		-55	+150	°C
Tj	junction temperature		-20	+150	°C
V _{ESD}	voltage peak human body model	note 1	-	2000	V
	voltage peak machine model		-	300	V

Note

1. 1250 V for IIN (pin 5).

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QUALITY SPECIFICATION

Quality specification in accordance with "SNW-FQ-611 part E".

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-c}	thermal resistance from junction to case	3.0	K/W

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CHARACTERISTICS

Operating range: $T_j = -20$ to +150 °C; $V_{DD} = 180$ to 210 V; $V_{CC} = 10.8$ to 13.2 V; $V_{OUTM} = 4$ to 20 V; $V_{VIN-} = 1.5$ to 5 V; $V_{VIN+} = 1.5$ to 5 V.

Test conditions: $T_{amb} = 25 \text{ °C}$; $V_{DD} = 200 \text{ V}$; $V_{CC} = 12 \text{ V}$; $V_{VIN+} = 3 \text{ V}$; $V_{OUTM} = 6 \text{ V}$; $C_L = 10 \text{ pF}$ (C_L consists of parasitic and cathode capacitance); $R_{th h} = 4 \text{ K/W}$; test circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT	
I _{DD(q)}	quiescent high voltage supply current	V _{OUTC} = 100 V	8	10	12	mA	
I _{CC(q)}	quiescent low voltage supply current	$V_{VIN-} = V_{VIN+}$	25	31	39	mA	
I _{bias}	input bias current (pins 2 and 4)	V _{OUTC} = 100 V	-	30	-	μA	
V _{OUTC}	DC output voltage (pins 12 and 13)	$V_{VIN-} = V_{VIN+}$	70	100	130	V	
ΔV _{OUTC(T)}	DC output voltage temperature drift (pins 12 and 13)	$V_{VIN-} = V_{VIN+}$	_	_	5	V	
I _(offset) OUTM	offset current of measurement output	note 1	-40	+20	+120	μA	
ΔΙ _{ΟυΤΜ} /ΔΙ _{ΟυΤC}	linearity of current transfer	–50 μA < I _{OUTC} < +50 μA; note 1	-	1.0	-		
C _i	input capacitance (pins 2 and 4)	V _{OUTC} = V _{OUTC(max)}	-	3	-	pF	
I _{OUTC(max)}	maximum dynamic peak output current (pin 12)	20 V < V _{OUTC} < V _{DD} – 20 V	-	100	-	mA	
V _{OUTC(min)}	minimum output voltage (pin 12)		-	4	10	V	
V _{OUTC(max)}	maximum output voltage (pin 12)		V _{DD} - 10	$V_{DD} - 6$	-	V	
G _{int}	internal gain		1.68	1.87	2.08		
B _s	small signal bandwidth (pin 12)	$V_{OUTC(AC)} = 60 V (p-p);$ $V_{OUTC(DC)} = 100 V$	40	47	-	MHz	
B _l	large signal bandwidth (pin 12)	V _{OUTC(AC)} = 125 V (p-p); V _{OUTC(DC)} = 100 V	28	32	-	MHz	
t _{pd}	cathode output propagation time 50% input to 50% output (pin 12)	$\begin{split} V_{OUTC(AC)} &= 125 \ V \ (p\text{-}p); \\ V_{OUTC(DC)} &= 100 \ V; \\ square wave; f < 1 \ MHz; \\ t_{f(VIN-)} &= 10 \ ns; \\ t_{r(VIN-)} &= 10 \ ns; \\ see \ Figs \ 6 \ and \ 7 \end{split}$	10	-	15	ns	
t _{o(r)}	cathode output rise time 10% output to 90% output (pin 12)		10	14	18	ns	

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t _{o(f)}	cathode output fall time 90% output to 10% output (pin 12)	$\begin{split} V_{OUTC(AC)} &= 125 \ V \ (p\text{-}p); \\ V_{OUTC(DC)} &= 100 \ V; \\ square \ wave; \ f < 1 \ MHz; \\ t_{f(VIN-)} &= 10 \ ns; \\ t_{r(VIN-)} &= 10 \ ns; \\ see \ Fig.7 \end{split}$	10	12.5	15	ns
t _{st}	settling time 50% input to (99% < output < 101%) (pin 12)	$\begin{split} V_{OUTC(AC)} &= 125 \ V \ (p\text{-}p); \\ V_{OUTC(DC)} &= 100 \ V; \\ square \ wave \ f < 1 \ MHz; \\ t_{f(VIN-)} &= 10 \ ns; \\ t_{r(VIN-)} &= 10 \ ns; \\ see \ Figs \ 6 \ and \ 7 \end{split}$	-	-	250	ns
SRr	slew rate rise between 30 V to (V _{DD} – 30 V) (pin 12)	$V_{VIN-} = 2 V (p-p) square$ wave; f < 1 MHz; $t_{f(VIN-)} = 10 ns;$ $t_{r(VIN-)} = 10 ns$	-	8	-	V/ns
SRf	slew rate fall between (V _{DD} – 30 V) to 30 V (pin 12)	$V_{VIN-} = 2 V (p-p)$ square wave; f < 1 MHz; $t_{f(VIN-)} = 10 \text{ ns};$ $t_{r(VIN-)} = 10 \text{ ns};$	_	10	_	V/ns
O _{Vr}	cathode output voltage overshoot rise (pin 12)	$\begin{split} V_{OUTC(AC)} &= 125 \ V \ (p\text{-}p); \\ V_{OUTC(DC)} &= 100 \ V; \\ square \ wave; \ f < 1 \ MHz; \\ t_{f(VIN-)} &= 10 \ ns; \\ t_{r(VIN-)} &= 10 \ ns; \\ see \ Figs \ 6 \ and \ 7 \end{split}$	-	5	-	%
O _{Vf}	cathode output voltage overshoot fall (pin 12)	$\begin{split} V_{OUTC(AC)} &= 125 \ V \ (p\text{-}p); \\ V_{OUTC(DC)} &= 100 \ V; \\ square wave; \ f < 1 \ MHz; \\ t_{f(VIN-)} &= 10 \ ns; \\ t_{r(VIN-)} &= 10 \ ns; \\ see \ Figs \ 6 \ and \ 7 \end{split}$	-	20	-	%
PSRRh	high voltage power supply rejection ratio	f < 50 kHz; note 2	-	44	-	dB
PSRRI	low voltage power supply rejection ratio	f < 50 kHz; note 2	-	48	-	dB

Notes

1. The operating range of the measurement output OUTM is 4 to 20 V. Below 4 V, OUTM acts as a voltage source with an output resistance such that the maximum current input from OUTM is 2 mA.

- a) The linearity of the current transfer is guaranteed until a junction temperature of 125 °C.
- 2. The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.

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FLASHOVER PROTECTION

The TDA6120Q does NOT include protection diodes that clamp the cathode output pin to the high voltage supply pin during a CRT flashover discharge. Therefore an external high voltage reverse biased diode has to be connected between the OUTC pin and the V_{DD} pin. An external 147 Ω carbon high-voltage resistor in combination with a 2 kV spark gap between the cathode and ground will limit the maximum clamp current (for this resistor value, the CRT has to be connected to the main printed-circuit board).

This external network causes an increase in the rise and fall times and a decrease in the overshoot.

Pin 10 must be decoupled to pin 8:

- By a capacitor >22 nF with good HF behaviour (e.g. foil). This capacitor must be placed as close as possible to pin 10 and pin 8; definitely within 5 mm.
- By a capacitor >3.3 μF on the picture tube base printed circuit board (common for three output stages).

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TEST AND APPLICATION INFORMATION

Dissipation

Regarding dissipation, distinction must be made between static dissipation (independent of frequency) and dynamic dissipation (proportional to frequency). The static dissipation of the TDA6120Q is due to supply currents, and currents in the feedback network and CRT.

The static dissipation is given by the following equation:

$$P_{stat} = V_{CC} \times I_{CC} + V_{DD} \times I_{DD} - V_{OUTC} \times \frac{V_{OUTC}}{R_f - I_{OUTC}}$$

Where:

 R_{f} = feedback resistance

 $I_{OUTC} = DC$ cathode current.

The dynamic dissipation is given by the following equation: $P_{dyn} = V_{DD} \times (C_L + C_{int}) \times f \times V_{OUTC(p-p)} \times b$

Where:

C_L = load capacitance

C_{int} = effective internal load capacitance (approximately 7 pF)

f = frequency

V_{OUTC(p-p)} = output voltage (peak-to-peak value)

b = non-blanking duty cycle (0.8).

The IC must be mounted on the picture tube base printed-circuit board to minimize the load capacitance C_L .

Switch-off

The voltage at output pins OUT and OUTC will be pulled to ground when the low voltage supply voltage (V_{CC}) is switched off.

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INTERNAL PIN CONFIGURATION



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PACKAGE OUTLINE

S13P	: plas	stic D	DIL-bo	ent-S	IL po	wer	pack	age;	13 le	ads	(lead	leng	th 7.7	7 mm)					sc	DT14 1
					- D							non-cc									
									0	5 L L L L SCA	; i	10 m 	m								
UNIT	IONS ((mm ai	b _p	origina c	D ⁽¹⁾	nsions d) D _h	E ⁽¹⁾	е	e ₁	e ₂	Eh	j	L	L ₃	m	Q	v	w	x	Z ⁽¹⁾
mm	17.0 15.5	4.6 4.2	0.75	0.48	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	8.4 7.0	2.4 1.6	4.3	2.1 1.8	0.6	0.25	0.03	2.00 1.45
lote . Plastic	c or me	etal pro	otrusion	s of 0.2	25 mm	maxim	um pe	side a	re not	include	ed.								<u> </u>		
OL								REFE	RENC	ES						EUR	OPEA	N	ISS	UE DA	TE
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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\,max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 $^{\circ}$ C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 $^{\circ}$ C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.