DATA SHEET

TDA8354Q
Full bridge current driven vertical deflection output circuit in LVDMOS

Preliminary specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

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Full bridge current driven vertical deflection output circuit in LVDMOS

TDA8354Q

FEATURES

- Few external components
- Highly efficient fully DC-coupled vertical output bridge circuit
- Short rise and fall times of the vertical flyback switch
- Guard circuit
- Temperature (thermal) protection
- High ElectroMagnetic Compatibility (EMC) because of common mode inputs
- Guard signal in zoom mode.

GENERAL DESCRIPTION

The TDA8354Q is a power circuit for use in 90° and 110° colour deflection systems for field frequencies of 25 to 200 Hz and 16 : 9 picture tubes. The circuit provides a DC-driven vertical deflection output circuit, operating as a highly efficient class G system. Due to the full bridge output circuit the deflection coils can be DC coupled.

The IC is constructed in a low-voltage DMOS process that combines bipolar, CMOS and DMOS devices, to provide ruggedness.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	supply voltage		7.5	12	18	V
$I_{q(av)}$	average quiescent supply current	during scan	–	10	15	mA
V_{flb}	flyback supply voltage		$2 \times V_P$	45	68	V
$I_{Vflb(av)}$	average flyback supply current	during scan	–	–	10	mA
Vertical circuit						
$I_{o(p-p)}$	output current (peak-to-peak value)		–	–	3.2	A
$I_{i(diff)(p-p)}$	input current (peak-to-peak value) at pin 11 or 12		–	500	600	μA
Flyback switch						
$I_{o(Vflb)}$	peak output current	$t \leq 1.5$ ms	–	–	±1.6	A
Thermal data (in accordance with IEC 747-1)						
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	operating ambient temperature		–25	–	+75	°C
T_j	junction temperature		–	–	150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8354Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

BLOCK DIAGRAM

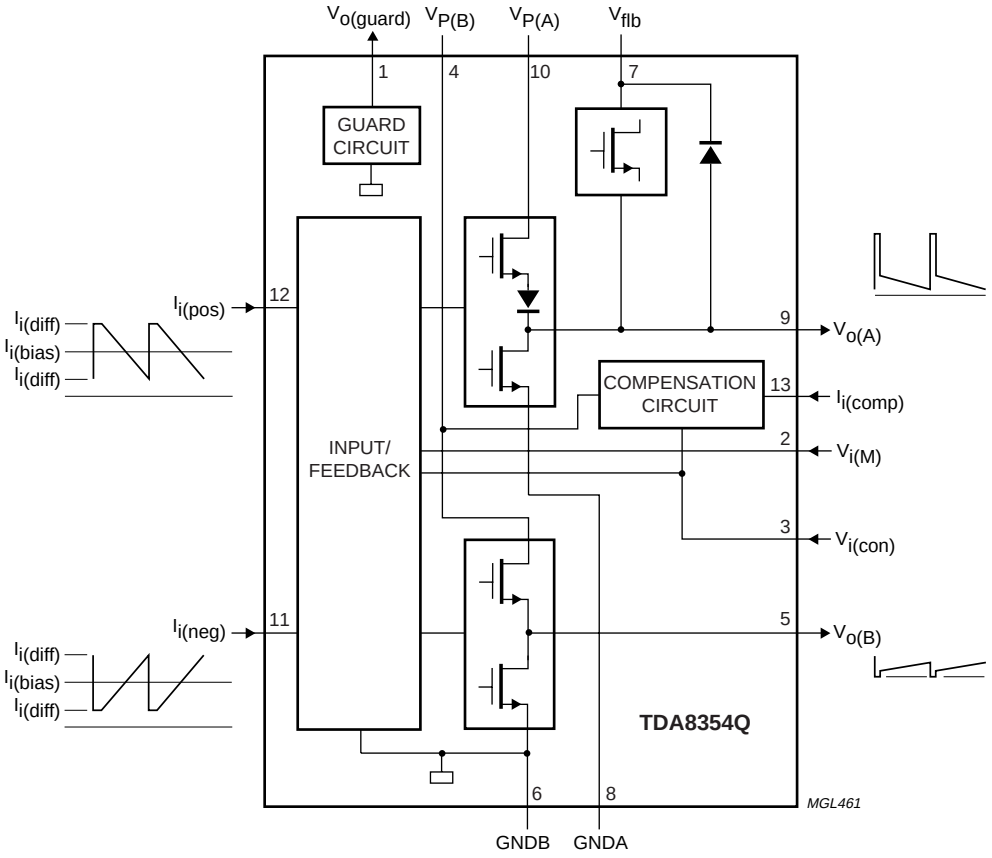
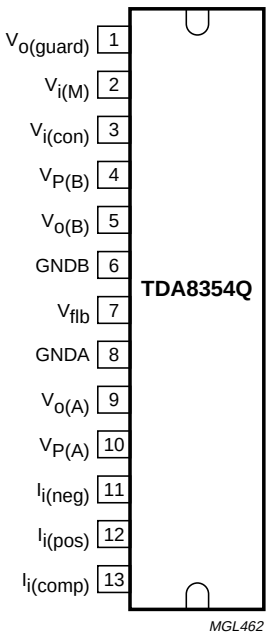


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{o(guard)}$	1	guard output voltage
$V_{i(M)}$	2	measuring resistor input
$V_{i(con)}$	3	conversion resistor input
$V_{P(B)}$	4	supply voltage B
$V_{o(B)}$	5	output voltage B
GNDB	6	ground B
V_{flb}	7	flyback supply voltage
GNDA	8	ground A
$V_{o(A)}$	9	output voltage A
$V_{P(A)}$	10	supply voltage A
$I_{i(neg)}$	11	input power-stage (negative); includes $I_{i(bias)}$ signal bias
$I_{i(pos)}$	12	input power-stage (positive); includes $I_{i(bias)}$ signal bias
$I_{i(comp)}$	13	damping resistor compensation current input



The die has been glued to the metal block of the package. If the metal block is not insulated from the heat sink, the heat sink may only be connected directly to pins 6 and 8.

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The vertical driver circuit is a bridge configuration. The deflection coil is connected between the output amplifiers, which are driven in phase opposition. The differential input circuit is current driven. The input circuit is special intended for direct connection to driver circuits which deliver symmetrical current signals, but is also suitable for asymmetrical currents. The current to voltage conversion is done by the external resistor (R_{con}) connected between the output of the input conversion stage and output stage B. This voltage is compared with the output current through the deflection coil measured as voltage across R_M, which provides internal feedback information. The relationship between the differential input current and the output current is defined by: $2 \times I_{i(diff)} \times R_{con} = I_{coil} \times R_M$ The output current is adjustable from 0.5 A (p-p) to 3.2 A (p-p) by varying R_{con}. The maximum input current is 800 μA peak for each pin. The minimum input current should be 50 μA.

Flyback supply

The flyback voltage is determined by an additional supply voltage V_{flb}. The principle of operating with two supply voltages (class G) makes it possible to fix the supply voltage V_P optimum for the scan voltage and the second supply voltage V_{flb} optimum for the flyback voltage. Using this method, very high efficiency is achieved. The supply voltage V_{flb} is almost totally available as flyback voltage across the coil, this being possible due to the absence of a coupling capacitor (not necessary, due to the bridge configuration). The very short rise and fall time of the flyback switch is >400 V/μs.

Protection

The output circuit has protection circuits for:

- Die temperature control
- Overvoltage of output stage A.

Guard circuit

A guard circuit with output signal $V_{o(guard)}$ is provided.

The guard circuit generates an active HIGH level during the flyback period. The guard circuit is also activated for one or more of the following conditions:

- When the thermal protection is activated ($T_j \approx 170$ °C)
- During short-circuit of the output pins (pins 5 and 9) to V_P or ground
- During open coil
- During open loop
- During short-circuit of the input pins (pins 11 and 12) to V_P or ground.

An active HIGH level of the guard signal is also generated for the next conditions:

- No drive signal
- Short-circuit of the coil.

However, for these events the signal is generated via an internal timer circuit. The guard signal set via this timer has a delay of ≈120 ms. The delay time is given by the lowest applicable field frequency.

The guard signal can be used for blanking the picture tube screen and signalling a fault condition.

Damping resistor compensation

For HF-loop stability a damping resistor is connected across the deflection coil. There is a big difference in current in the damping resistor R_p during scan and flyback. The resistor current is summed to the current in the deflection coil via the measuring resistor R_M, which results in a too low current in the deflection coil at the start of the scan.

To reach a short settling time the difference in the current during scan and flyback in the damping resistor can be compensated for by external means. To do so a resistor (R_{comp}) of about 1 MΩ can be connected between the output of stage A (pin 9) and the damping resistor compensation current input (pin 13).

For a more accurate calculation of R_{comp} refer to the following formula:

$$R_{comp} = \frac{(V_{flb} - V_{loss} - V_P) \times R_p \times R_{con}}{(V_{flb} - V_{loss} - I_L \times R_L) \times R_M}$$

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
DC supply					
V_P	supply voltage		–	18	V
V_{flb}	flyback supply voltage		–	68	V
Vertical circuit					
$I_{o(p-p)}$	output current (peak-to-peak value)		–	3.2	A
$V_{o(A)}$	output voltage (pin 9)	note 1	–	68	V
$V_{o(B)}$	output voltage (pin 5)		–	V_P	V
$I_{1,2,3,11,12,13}$	current into or out of pins 1 to 3 and 11 to 13		–20	+20	mA
$V_{1,2,3,11,12,13}$	peak voltage on pins 1 to 3 and 11 to 13		–0.5	V_P	V
Flyback switch					
$I_{o(Vflb)}$	peak output current		–	±1.6	A
Thermal data (in accordance with IEC 747-1)					
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–25	+75	°C
T_j	junction temperature	note 2	–	150	°C
Miscellaneous					
t_{sc}	short-circuiting time	note 3	–	1	h
$I_{i/o}$	current into any pin	$+1.5 \times \lvert V_{P(max)} \rvert$; note 4	–	+200	mA
	current out of any pin	$-1.5 \times \lvert V_{P(max)} \rvert$; note 4	–200	–	mA
V_{ESD}	electrostatic handling	note 5	–	±300	V
		note 6	–	±2000	V

Notes

1. When the pin voltage exceeds 70 V the device behaves like a power zener diode thus limiting the voltage.
2. Internally limited by thermal protection; switching point ≈170 °C.
3. Up to V_P = 18 V.
4. At $T_{j(max)}$.
5. Machine model: equivalent to discharge a 200 pF capacitor through a 0 Ω series resistor. Except pin 7: ±250 V.
6. Human body model: equivalent to discharge a 100 pF capacitor through a 1.5 kΩ series resistor. Except pin 7: ±1500 V.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case		4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W

CHARACTERISTICS

V_P = 12 V; V_{flb} = 45 V; f_i = 50 Hz; $I_{i(bias)}$ = 330 μA; T_{amb} = 25 °C; measured in test circuit of Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	operating supply voltage		7.5	12	18	V
V_{flb}	flyback supply voltage		$2 \times V_P$	45	68	V
$I_{q(av)}$	average quiescent supply current	during scan	–	10	15	mA
I_q	quiescent supply current	no signal; no load	–	60	80	mA
$I_{Vflb(av)}$	average flyback supply current	during scan	–	–	10	mA
Output stage A and B						
V_{loss}	voltage loss from pin 10 to 9 and from pin 5 to 6	I_o = 3.2 A (p-p); note 1	–	–	6.0	V
	voltage loss from pin 4 to 5 and from pin 9 to 8		–	–	4.8	V
	voltage loss from pin 10 to 9 and from pin 5 to 6	I_o = 2.2 A (p-p); note 1	–	–	4.2	V
	voltage loss from pin 4 to 5 and from pin 9 to 8		–	–	3.4	V
LE	linearity error					
	adjacent blocks	I_o = 3.2 A (p-p); note 2	–	0.5	2	%
	not adjacent blocks	I_o = 3.2 A (p-p); note 2	–	0.5	3	%
V_o	output voltage swing (flyback) $V_{o(A)} - V_{o(B)}$	$I_{i(diff)}$ = 0.3 mA; I_o = 1.6 A	–	46	–	V
$\lvert V_{offset} \rvert$	offset voltage across R_M	$I_{i(diff)}$ = 0				
		$I_{i(bias)}$ = 500 μA	–	–	15	mV
		$I_{i(bias)}$ = 100 μA	–	–	13	mV
$\Delta V_{offset(T)}$	offset voltage as function of temperature	$I_{i(diff)}$ = 0	–	–	40	μV/K
$V_{o(A)}$, $V_{o(B)}$	DC output voltage	$I_{i(diff)}$ = 0; note 3	–	$\frac{V_P}{2}$	–	V
$G_{v(ol)}$	open-loop voltage gain $V_{9\ to\ 5}/V_{3\ to\ 5}$	notes 4 and 5	–	60	–	dB
$V_{3\ to\ 5}/V_{2\ to\ 5}$	voltage ratio $V_{3\ to\ 5}/V_{2\ to\ 5}$	note 4	–	0	–	dB
f_{res}	frequency response (–3 dB)	open loop	–	1	–	kHz
G_i	current gain ($I_o/I_{i(diff)}$)		–	8000	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta G_{i(T)}$	current gain drift as function of temperature		–	–	10^{-4}	/K
PSRR	power supply rejection ratio	note 6	80	90	–	dB
Input stage						
$I_{i(bias)}$	signal bias current		–	330	500	μA
$I_{i(diff)(p-p)}$	differential mode input current (peak-to-peak value) pin 11 or 12	note 7	–	500	600	μA
$V_{i(diff)}$	differential mode input voltage	$I_{i(diff)}$ = 500 μA	–	0.75	–	V
$V_{i(cm)}$	common mode input voltage	$I_{i(bias)}$ = 330 μA	0.95	1.15	1.35	V
Flyback switch						
$I_{o(Vflb)}$	output peak current	t < 1.5 ms	–	–	±1.6	A
V_{loss}	voltage loss ($V_{flb} - V_{o(A)}$)	I_o = +1.6 A	–	8	9	V
Guard circuit						
$I_{o(guard)}$	output current	not active; $V_{o(guard)}$ = 0 V	–	–	10	μA
		active; $V_{o(guard)}$ = 4.5 V	1	–	2.5	mA
$V_{o(guard)}$	output voltage on pin 1	$I_{o(guard)}$ = 100 μA	5	6	7	V
	allowable voltage on pin 1	maximum leakage current = 10 μA	–	–	18	V

Notes

1. At T_j = 125 °C. The temperature coefficient of V_{loss} has a positive sign.
2. The linearity error is measured without S correction and based on the same measurement principle as performed on the screen. The measuring method is as follows:
   Divide the output signal into 22 equal time parts ranging from 1 to 22 inclusive. Measure the value of the voltage across R_M of two succeeding parts called one block (a) starting with part 2 and 3 (block 1) and ending with part 20 and 21 (block 10). Thus parts 1 and 22 are unused. The equations for linearity error for adjacent blocks (LEAB) and not adjacent blocks (LENAB) are given below:

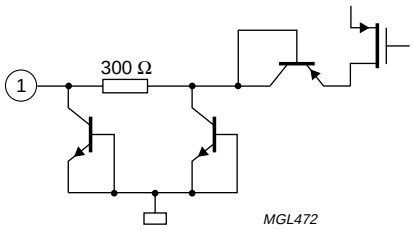
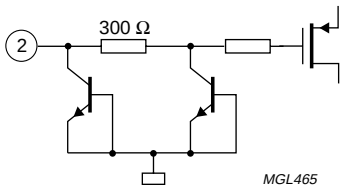
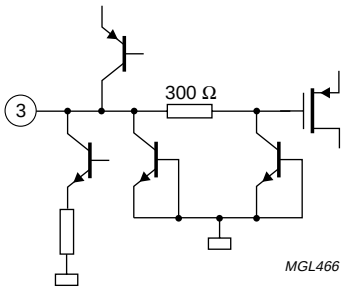
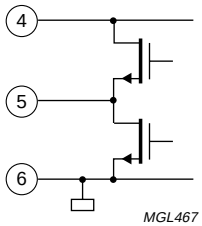
   $$LEAB = \frac{a_k - a_{(k+1)}}{a_{av}}$$

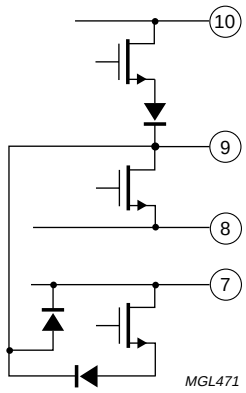
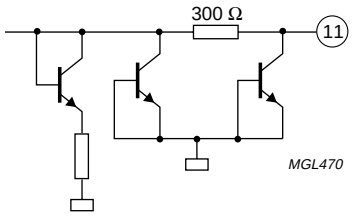
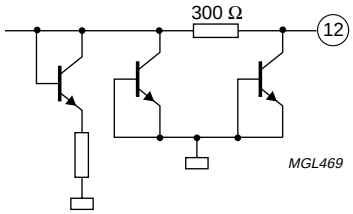
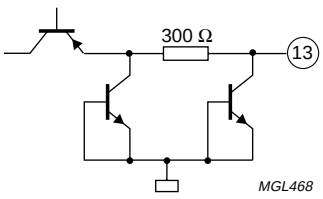
   $$LENAB = \frac{a_{max} - a_{min}}{a_{av}}$$

3. $V_{o(A)} + V_{o(B)} = V_P$. At the start of the scan this equation is one diode voltage less.
4. The V value within formulae relates to voltages at or between relative pin numbers, i.e. $V_{9\ to\ 5}/V_{3\ to\ 5}$ = voltage value across pins 9 and 5 divided by voltage value across pins 3 and 5.
5. $V_{2\ to\ 5}$ AC short-circuited.
6. At $V_{(ripple)}$ = 500 mV (eff) at V_P; measured across R_M; $f_{(ripple)}$ = 50 Hz – 1 kHz.
7. $I_{i(bias)} + I_{i(diff)} \leq 800$ μA and $I_{i(bias)} - I_{i(diff)} \geq 50$ μA per pin.

INTERNAL CIRCUITRY

Table 1 Equivalent pin circuits

PIN	SYMBOL	EQUIVALENT CIRCUIT
1	$V_{o(guard)}$	
2	$V_{i(M)}$	
3	$V_{i(con)}$	
4	$V_{P(B)}$	
5	$V_{o(B)}$	
6	GNDB	

PIN	SYMBOL	EQUIVALENT CIRCUIT
7	V_{flb}	
8	GNDA	
9	$V_{o(A)}$	
10	$V_{P(A)}$	
11	$I_{i(neg)}$	
12	$I_{i(pos)}$	
13	$I_{i(comp)}$	

TEST AND APPLICATION INFORMATION

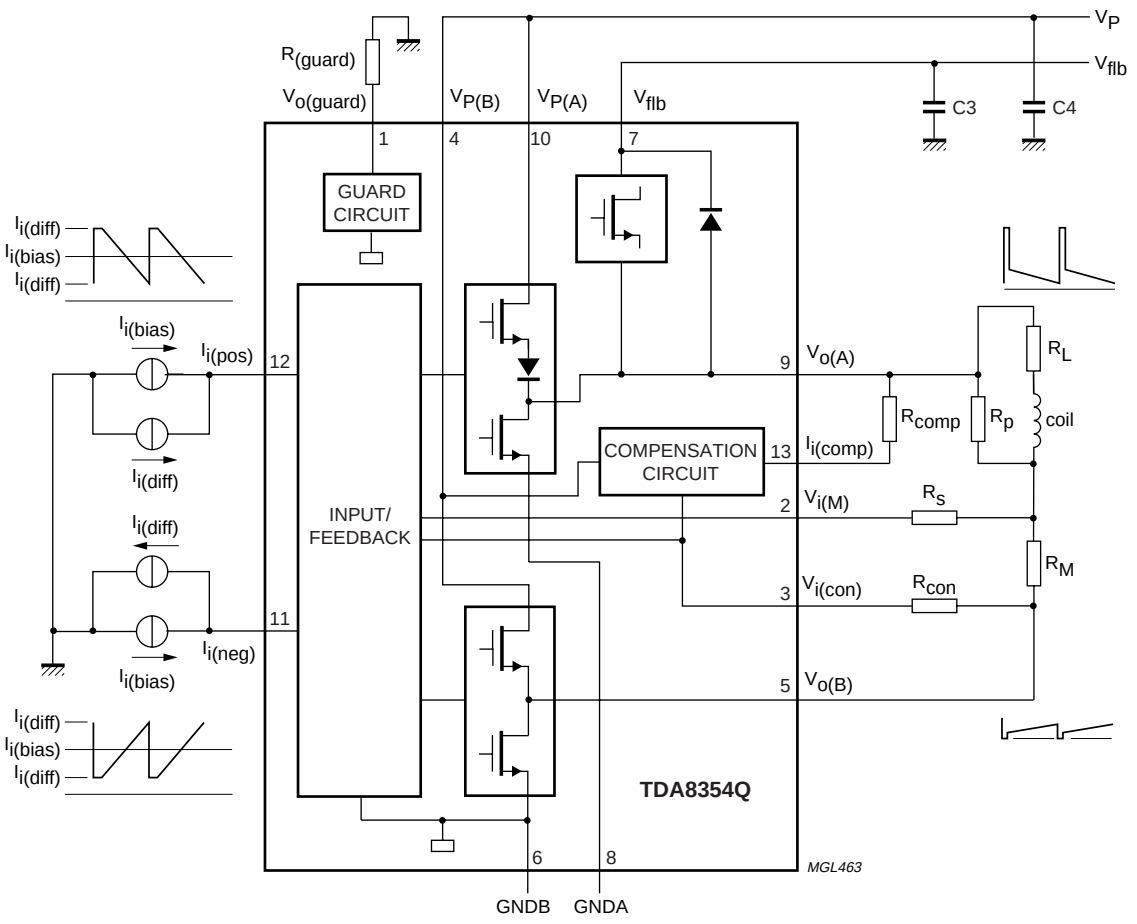
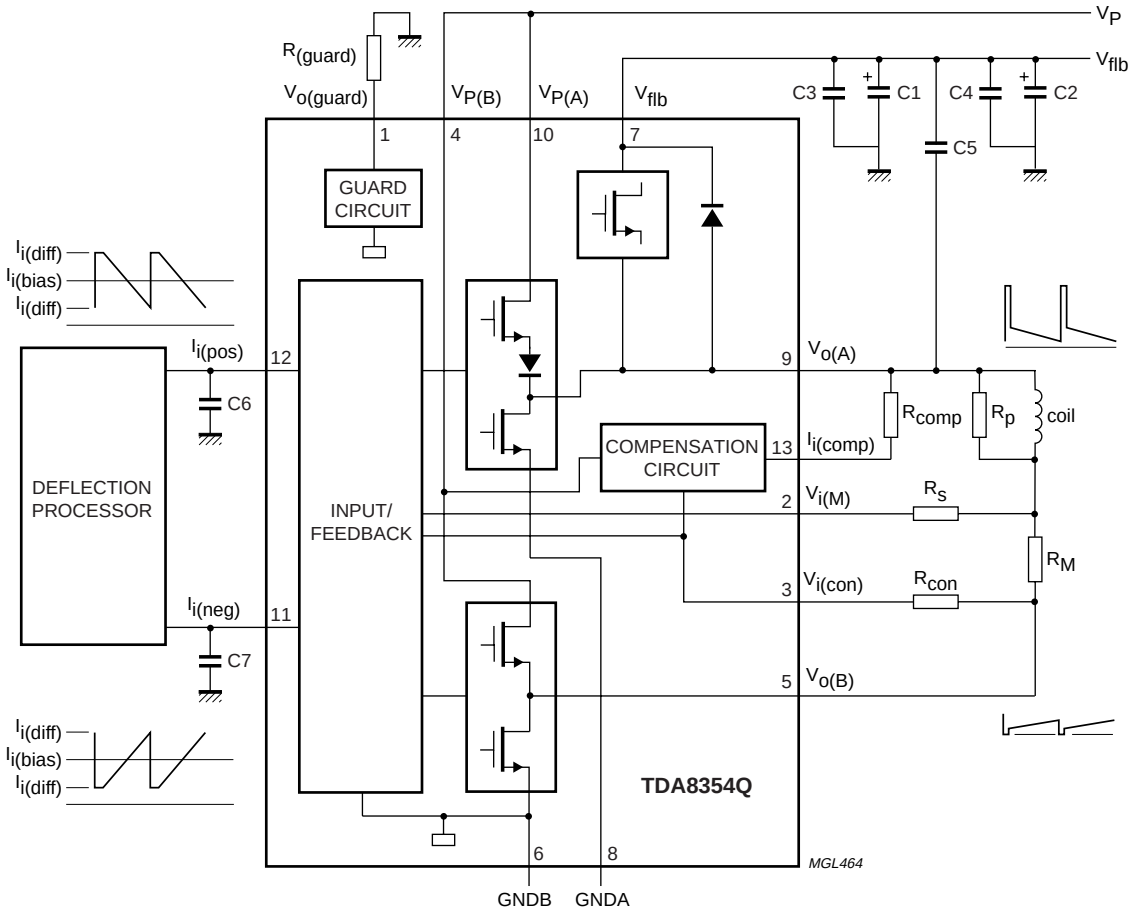


Fig.3 Test diagram.



Coil: AT6216/42;
V_P = 12.1 V at f_v = 50 Hz (vertical frame frequency); inclusive spread (absolute) and temperature rise in the coil;
V_P = 12.8 V at f_v = 100 Hz (vertical frame frequency); inclusive spread (absolute) and temperature rise in the coil;
$I_{o(p-p)}$ = 2.33 A (peak-to-peak);
$I_{i(bias)}$ = 330 μA;
$I_{i(diff)(12-11)}$ = 485 μA (peak value);
V_{flb} = 45 V;
t_{flb} = 0.6 ms.

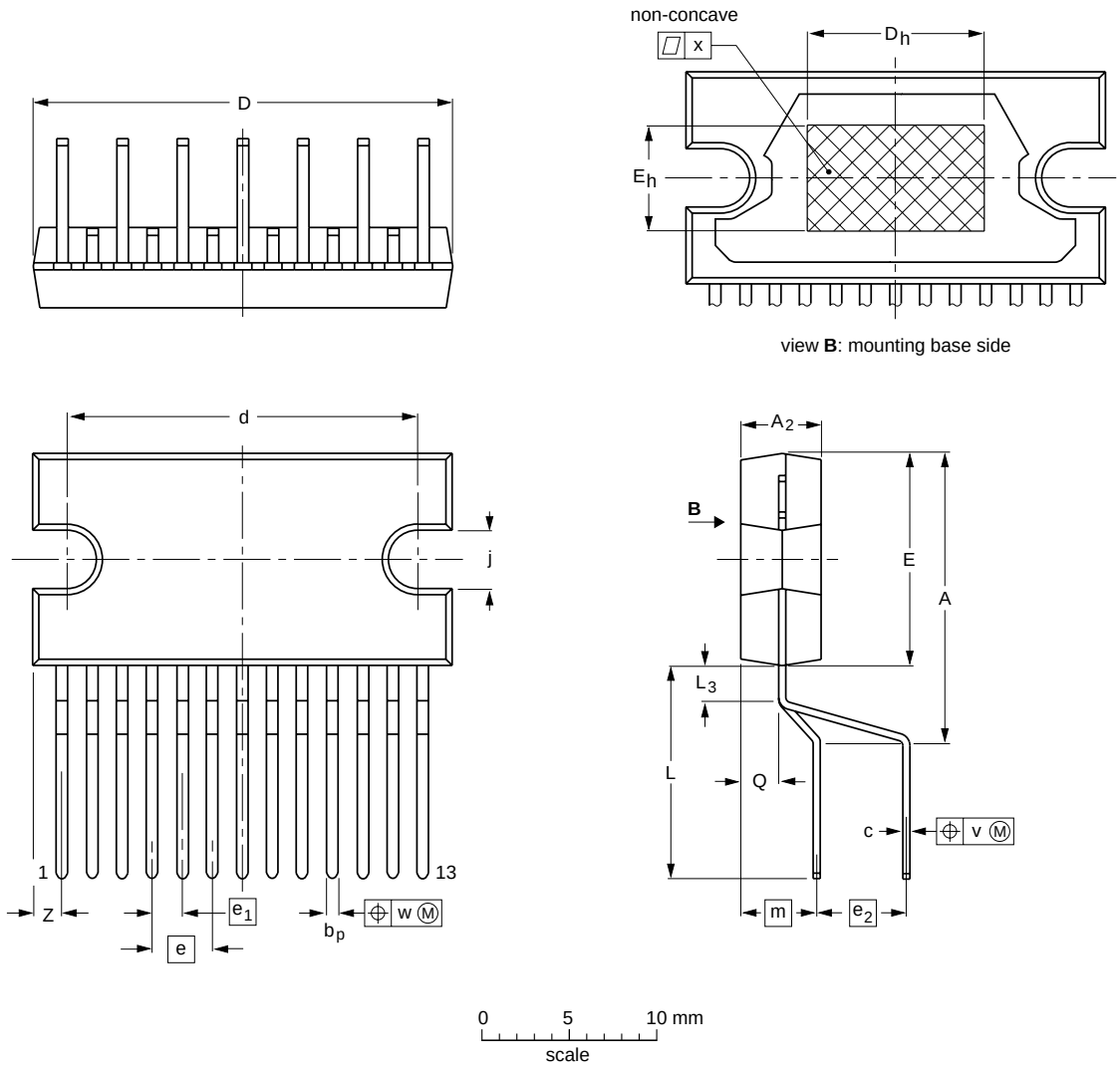
R_M = 0.5 Ω;
R_{con} = R_s = 1.2 kΩ;
R_p = 300 Ω;
R_{comp} = 650 kΩ;
$R_{(guard)}$ = 5 kΩ.

C1 = 47 μF; 100 V;
C2 = 220 μF; 25 V;
C3 = C4 = 100 nF;
C5 = 10 nF;
C6 = C7 = 10 nF.

Fig.4 Application diagram.

PACKAGE OUTLINE

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm) **SOT141-6**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT141-6						~~95-03-11~~ 97-12-16