DATA SHEET

TDA10021
Single Chip DVB-C Channel Receiver

Preliminary specification
File under Integrated Circuits, IC02

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Philips
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FEATURES

- 4/16/32/64/128/256 QAM demodulator (DVB-C compatible : ETS 300-429).
- High performance for 256 QAM especially for direct IF applications.
- On chip 10-bit ADC.
- On chip PLL for crystal frequency multiplication (Typically 4MHz crystal)
- Digital down conversion.
- Half Nyquist filter (roll off = 15 %).
- Two PWM AGC outputs with programmable take over point (For Tuner and Downconverter Control)
- Clock timing recovery, with programmable second order loop filter.
- Variable symbol rate capability from SACLK/64 to SACLK/4 (SACLK max = 36 MHz)
- Programmable anti-aliasing filters.
- Full digital carrier recovery loop.
- Carrier acquisition range up to 18 % of symbol rate.
- Integrated adaptative equalizer (Linear Transversal Equalizer or Decision Feedback Equalizer).
- On chip FEC decoder (Deinterleaver & RS decoder), full DVB-C compliant.
- DVB compatible differential decoding and mapping.
- Parallel and serial transport stream interface simultanously .
- I2C bus interface, for easy control.
- CMOS 0.2µm technology.

APPLICATIONS

- DVB-C fully compatible.
- Digital data transmission using QAM modulations.
- Cable demodulation.
- Cable modems
- MMDS (ETS 300-429).

DESCRIPTION

The TDA10021 is a single chip DVB-C Channel receiver for 4, 16, 32, 64, 128 and 256-QAM modulated signals. The device interfaces directly to the IF signal, which is sampled by a 10-bit A/D converter.

The TDA10021 performs the clock and the carrier recovery functions. The digital loop filters for both clock and carrier recovery are programmable in order to optimize their characteristics according to the current application.

After base band conversion, equalization filters are used for echo cancellation in cable applications. These filters are configured as T-spaced transversal equalizer or DFE equalizer, so that the system performance can be optimized according to the network characteristics. A proprietary equalization algorithm, independent of carrier offset, is achieved in order to assist carrier recovery. Then a decision directed algorithm takes place, to achieve final equalization convergence.

The TDA10021 implements a FORNEY convolutional deinterleaver of depth 12 blocks and a Reed-Solomon decoder which corrects up to 8 erroneous bytes. The deinterleaver and the RS decoder are automatically synchronized thanks to the frame synchronization algorithm which uses the MPEG2 sync byte. Finally descrambling according to DVB-C standard, is achieved at the Reed Solomon output. This device is controlled via an I^2C bus.

Designed in 0.2 µm CMOS technology and housed in a 64 pin TQFP package, the TDA10021 operates over the commercial temperature range.

FIGURE 1 : FUNCTIONAL BLOCK DIAGRAM

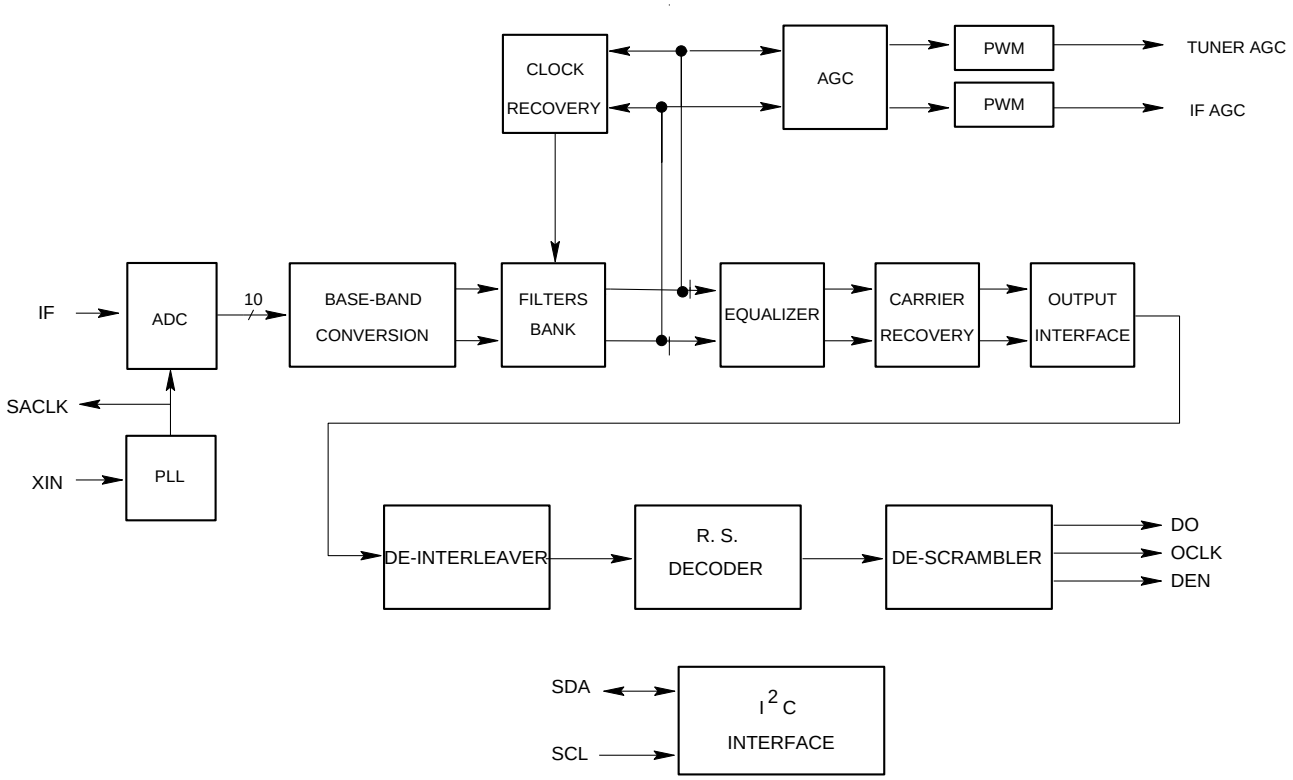


TABLE 1 : ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Ambient operating temperature : Ta	0	70	°C
DC supply voltage	- 0.5	Tbd	V
DC Input voltage	- 0.5	VDD + 0.5	V
DC Input Current		± 20	mA
Lead Temperature		+300	°C
Junction Temperature		+150	°C

Stresses above the absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

TABLE 2 : RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VDD	Digital supply voltage	1.62	1.8	1.98	V	1.8V ±10%
VCC	5V supply	4.75	5	5.25	V	pin 13 Only for 5V requirements
Ta	Operating temperature	0		70	°C	Ambient temperature
VIH[1]	High-level input voltage	2		VCC + 0.3	V	TTL input
VIL	Low-level input voltage	-0.5		0.8	V	TTL input
VOH[2]	High-level output voltage	VDD -0.1 2.4			V	@ IOH = -0.8 mA @ IOH = + 2mA
VOL[2]	Low-level output voltage			0.1 0.4	V	@ IOL = 0.8 mA @ IOL = + 2mA
IDD	Supply current		t.b.d		mA	Fsampl. = 57.84Mhz Symbol Rate =6Mbd
CIN	Input capacitance		t.b.d		pF	
COUT	Output capacitance		t.b.d		pF	
VD1	Analog supply voltage	1.6	1.8	2.0	V	1.8V ± 10%
VD2, VD3	Analog supply voltage	3.0	3.3	3.6	V	3.3V ± 10%
VIP	Positive analog input		0.5		V	
VIM	Negative analog input		-0.5		V	

[1] All inputs are 5V tolerant
[2] IOH, IOL = ± 4mA only for pins SACLK, OCLK, SDA, CTRL1, CTRL2, IT

FUNCTIONAL DESCRIPTION

- **ADC**
  The TDA10021 implements a 10-bit analog to digital converter. No external voltage references are required to use the ADC.

- **PLL**
  The TDA10021 implements a PLL used as clock multiplier by [M/(N.P)] (programmable parameters in index 28_{16}, 29_{16}, $2A_{16}$), so that the crystal can be low frequency (fundamental tone – typically 4Mhz)

- **DOWN CONVERTER AND NYQUIST FILTERS**
  The digital down converter performs the down conversion of the bandpass input signal into the 2 classical quadrature I & Q channels. Then these two signals are passed through anti-alias filters and through a half Nyquist filter having a fixed roll-off of 0.15. The digital filter gives a stop band attenuation of more than 40 dB.

- **EQUALIZER**
  After Nyquist filtering, the signal is fed to an equalization filter, for echo cancellation. This equalizer can be configured as either a transversal Equalizer or a decision feedback equalizer. The following table shows some echos configuration that the TDA10021 corrects with an equivalent degradation of less than 1dB @ BER = 10^{-4}.

DELAY (nS)	AMPLITUDE (dB)	PHASE
50	-10	worst
150 and 800	-12 and -20	worst
1600	-20	worst

- **CARRIER RECOVERY**
  The carrier synchronizer implements a fully digital algorithm allowing to recover carrier frequency offsets up to ± 18 % symbol rate. A phase error detector followed by a programmable second order loop filter provides an estimation of the carrier phase, to compensate the input carrier frequency offset.

- **CLOCK RECOVERY**
  A timing error detector implements an application of Gardner algorithm for digital clock recovery.
  The resulting error is fed to a programmable second order loop filter, which provides a 8-bit command to the NCO block. This one allows to determine the right sampling time instant of the input signal.

- **AUTOMATIC GAIN CONTROL (2 PWM outputs)**
  An estimation of input signal magnitude is performed and compared to two programmable threshold. The resulting errors are filtered to produce two 10-bit commands which are then PWM encoded and provided on pins VAGC1 and VAGC2. The PWM signals can be passed through two low pass filters to control the gain amplifier.

- **OUTPUT INTERFACE**
  After carrier recovery, the demodulated output symbol must be decoded according to the constellation diagram given by DVB standard for 4, 16, 32, 64, 128 and 256 QAM. The resulting symbols are then differentially decoded (DVB compliant) and serially provided to the FEC part.

- **BLOCK SYNCHRONIZATION**
  At demodulator output, the length of some error bursts may exceed that which can be reliably corrected by the Reed-Solomon decoder. The implemented de-interleaving is a convolutional one (Forney) of depth 12. The first operation consists in synchronizing the de-interleaver. This is accomplished by detecting α consecutive MPEG2 sync words (or $\overline{\text{sync}}$) which are present as the first byte of each packet.
  Next, the RAM memory associated with the deinterleaver fills up and the first deinterleaved bytes are provided to the input of the Reed-Solomon decoder. The state machine of the de-interleaver goes to the control phase which

counts β consecutive missed MPEG2 sync words (or $\overline{\text{sync}}$) before declaring the system desynchronized and going back to the synchronization phase. α and β are programmable through the I2C interface.
When the inverted sync word is detected at the input of the de-interleaver, the bytes provided to the Reed-Solomon decoder are inverted at the output of the deinterleaver.

- **REED-SOLOMON DECODER**

The Reed-Solomon decoder decodes the symbol stream from the de-interleaver according to the (204, 188) shortened Reed-Solomon code. Synchronization to Reed-Solomon code is defined over the finite Galois field GF (2^8). The field generator polynomial is given by :

$$G(x) = \prod_{i=0}^{15} (x + \alpha^i)$$

This Reed-Solomon decoder corrects up to eight erroneous symbols in each block. When the correction capability of the decoder is exceeded, the block is not changed and is provided as it has been entered. In this case the flag UNCOR is set and the MSB of the second byte in the MPEG2 frame is forced to one (error indicator). The correction capability of the RS decoder can be inhibited.

- **DESCRAMBLER**

In order to comply with energy dispersal requirements of radio transmission regulations and to ensure adequate binary transitions, the MPEG2 frames are scrambled at the encoder side. Dual operation is achieved at the output of the Reed-Solomon decoder using the same scrambler/descrambler. The polynomial for the pseudo random binary sequence (PRBS generator is $1 + x^{14} + x^{15}$. The PRBS registers are initialized at the start of every eight transport packets. To provide an initialization signal for the descrambler, the MPEG2 sync byte of the first transport packet is inverted from 47_{16} to $B8_{16}$. When detected, the descrambler is loaded with the initial sequence "100101010000000". The descrambler can be inhibited.

- **INTERFACE**

The TDA10021 integrates an I^2C interface in slave mode. This I2C interface fulfills the Philips component I2C bus specification.

INPUT - OUTPUT SIGNAL DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
CLR#	16	I (5v tol)	The CLR# input is asynchronous and active low, and clears the TDA10021. When CLR# goes low, the circuit immediately enters its RESET mode and normal operation will resume 4 XIN falling edges later after CLR# returned high. The I2C register contents are all initialized to their default values. The minimum width of CLR# at low level is 4 XIN clock periods.
XIN	2	I	XTAL oscillator input pin. Typically a fundamental XTAL oscillator is connected between the XIN and XOUT pins. The XTAL frequency MUST be chosen so that the system frequency SYSCLK (= XIN * multiplying factor of the PLL) equals to 1.6 times the tuner output Intermediate Frequency : SYSCLK = 1.6 x IF.
XOUT	3	O	XTAL oscillator output pin. Typically a fundamental XTAL oscillator is connected between the XIN and XOUT pins.
SACLK	5	O	Sampling CLocK. This output clock can be fed to an external 10-bit ADC as the sampling clock. SACLK = SYSCLK/2.
VAGC1	9	O	First PWM encoded output signal for AGC Tuner. This signal is typically fed to the AGC amplifier through a single RC network.The maximum signal frequency on VAGC output is XIN/16. AGC information is refreshed every 1024 symbols.
VAGC2	11	O	Second PWM encoded output signal for AGC IF. This signal is typically fed to the AGC amplifier through a single RC network. The maximum signal frequency on VAGC output is XIN/16. AGC information is refreshed every 1024 symbols. But VAGC2 can also be configured to output a PWM signal, which value can be programmed through the I2C interface (see register PWMREF, index 34_{16})
DO[7:0]	37,38,39,40 45,46,47,48	O	Data Output bus . These 8-bit parallel data are the outputs of the TDA10021 after demodulation, de-interleaving, RS decoding and de-scrambling. When one of the two possible parallel interfaces is selected (Parameter SERINT=0, index 20_{16}) then DO[7:0] is the transport stream output. When the serial interface is selected (Parameter SERINT=1, index 20_{16}) then the serial output is on pin DO[0] (pin 48).
OCLK	35	O	Output CLock. OCLK is the output clock for the parallel DO[7:0] outputs. OCLK is internally generated depending on which interface is selected.
DEN	36	O	Data ENable : this output signal is high when there is a valid data on output bus DO[7:0].
UNCOR	33	O	UNCORrectable packet. This output signal is high when the provided packet is uncorrectable (during the 188 bytes of the packet). The uncorrectable packet is not affected by the Reed Solomon decoder, but the MSB of the byte following the sync. byte is forced « 1 » for the MPEG2 process : Error Flag Indicator (if RSI and IEI are set low in the I2C table).
PSYNC	34	O	Pulse SYNChro. This output signal goes high when the sync byte (47_{16}) is provided, then it goes low until the next sync byte. If the serial interface is selected, then PSYNC is high only during the first bit of the sync byte (47_{16}
IICDIV	10	I (5v tol)	IICDIV allow to select the frequency of the I2C internal system clock, depending on the crystal frequency. Internal I2C clock is a division of XIN by 4^{IICDIV} and must be between 6 and 20 MHz.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
SADDR	12	I (5v tol)	SADDR is the LSB of the I2C address of the TDA10021. The MSBs are internally set to 000110. Therefore the complete I2C address of the TDA10021 is (MSB to LSB) : 0, 0, 0, 1, 1, 0, SADDR.
SDA	18	I/O (5v tol)	SDA is a bidirectional signal. It is the serial input/output of the I2C internal block. A pull-up resistor (typically 4.7 kΩ) must be connected between SDA and VDD for proper operation (Open Drain output).
SCL	17	I (5v tol)	I2C clock input. SCL should nominally be a square wave with a maximum frequency of 400KHz. SCL is generated by the system I2C master.
TEST	6	I (5v tol)	Test input pin. For normal operation of the TDA10021, TEST must be grounded.
ENSERI	21	I (5v tol)	When high this pin enables the serial output transport stream through the boundary scan pins (TRST,TDO,TCK,TDI,TMS). Must be set low in bist and boundary scan mode.
TRST	26	I/O (5v tol)	Test ReSeT. This active low input signal is used to reset the TAP controller when in boundary scan mode. In normal mode of operation TRST must be set low. *In serial mode, TRST is the the uncorrectable output.*
TDO	28	O	Test Data Out. This is the serial Test output pin used in boundary scan mode. Serial Data are provided on the falling edge of TCK. *In Serial mode, TDO is the data output.*
TCK	22	I/O (5v tol)	Test ClocK : an independant clock used to drive the TAP controller when in boundary scan mode. In normal mode of operation, TCK must be set low. *In serial mode, TCK is the clock output.*
TDI	23	I/O (5v tol)	Test Data In. The serial input for Test data and instruction when in boundary scan mode. In normal mode of operation, TDI must be set to low. *In serial mode, the TDI is the psync output.*
TMS	27	I/O (5v tol)	Test Mode Select. This input signal provides the logic levels needed to change the TAP controller from state to state. In normal mode of operation, TMS must be set to high. *In serial mode TMS is then den output.*
CTRL	32	O	CTRL is a control output pin programmable by I2C (parameter CTRL of register CONTROL (index $2C_{16}$)). CTRL is open drain output, and therefore requires an external pull up resistor.
SCLT	20	O	SCLT can be configured to be a control line output or to output SCL input. This is controlled by parameter BYPIIC and CTRL_SCLT of register TEST (index $0F_{16}$). SCLT is an open drain output and therefore requires an external pull up resistor.
SDAT	19	I/O (5v tol)	SDAT is equivalent to SDA I/0 of TDA10021 but can be tri-stated by I2C programmation. It is actually the output of a switch controlled by parameter BYPIIC of register TEST (index $0F_{16}$). SDAT is an open drain output and therefore requires an external pull up resistor.
GPIO	29	O	GPIO can be configured by I2C (parameter selgpio[1:0], index OF_{16}) either as: - a front end lock indicator (FEL) (default mode), or - an active low output interrupt line (IT) which can be configured by the I2C interface. See registers ITsel (index 32_{16}) and Itstat (index 33_{16}), or - a control output pin programmable by I2C (parameter CTRL_GPIO, index $2C_{16}$). GPIO is an open drain output and therefore requires an external pull up resistor.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
VIP	58	I	Positive input to the A/D converter. This pin is DC biased to half-supply through an internal resistor divider (2 x 20kΩ resistors). In order to stay in the range of the ADC, |VIP-VIM| should remain between the input range corresponding to the sw0 and sw1 bits (index $1B_{16}$ - default value = 0.5 v).
VIM	57	I	Negative input to the A/D converter. This pin is DC biased to half-supply through an internal resistor divider (2 x 20kΩ resistors). In order to stay in the range of the ADC, |VIP-VIM| should remain between the input range corresponding to the sw0 and sw1 bits (index $1B_{16}$ - default value = 0.5 v).
VREFP	53	O	This is a positive voltage reference for the A/D converter. It is derived from the internal bandgap voltage, VBG, with an on-chip fully differential amplifier.
VREFM	54	O	This is the negative voltage reference for the A/D converter. It is derived from the internal bandgap voltage, VBG, with an on-chip fully differential amplifier.
VD1	50	I	Power supply input for the digital switching circuitry (1.8 typ).
VS1	49	I	Ground return for the digital switching circuitry.
VD2	52	I	Power supply input for the analog clock drivers (3.3V typ).
VS2	51	I	Ground return for the analog clock drivers.
VD3	60,55	I	Power supply input for the analog circuits (3.3V typ).
VS3	59,56	I	Ground return for analog circuits.
DVCC	61	I	1.8V supply for the digital section of the PLL.
DGND	62	I	Ground connection for the digital section of the PLL.
PLLGND	63	I	Ground connection for the analog section of the PLL.
PLLVCC	64	I	3.3V supply for the analog section of the PLL.

FIGURE 2 : BLOCK DIAGRAM

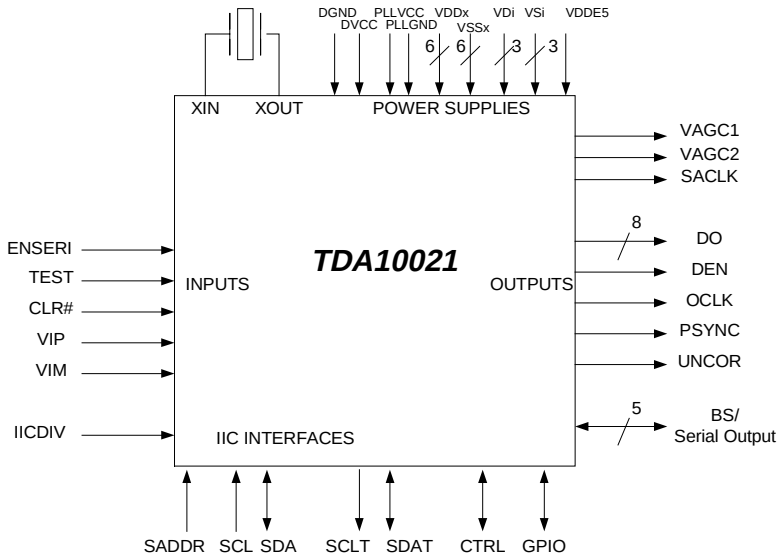


FIGURE 3 : PIN CONFIGURATION

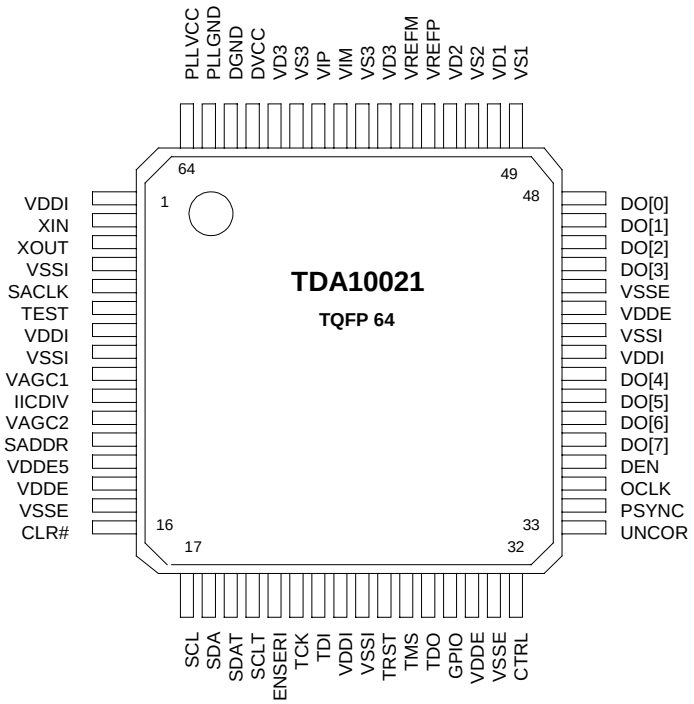


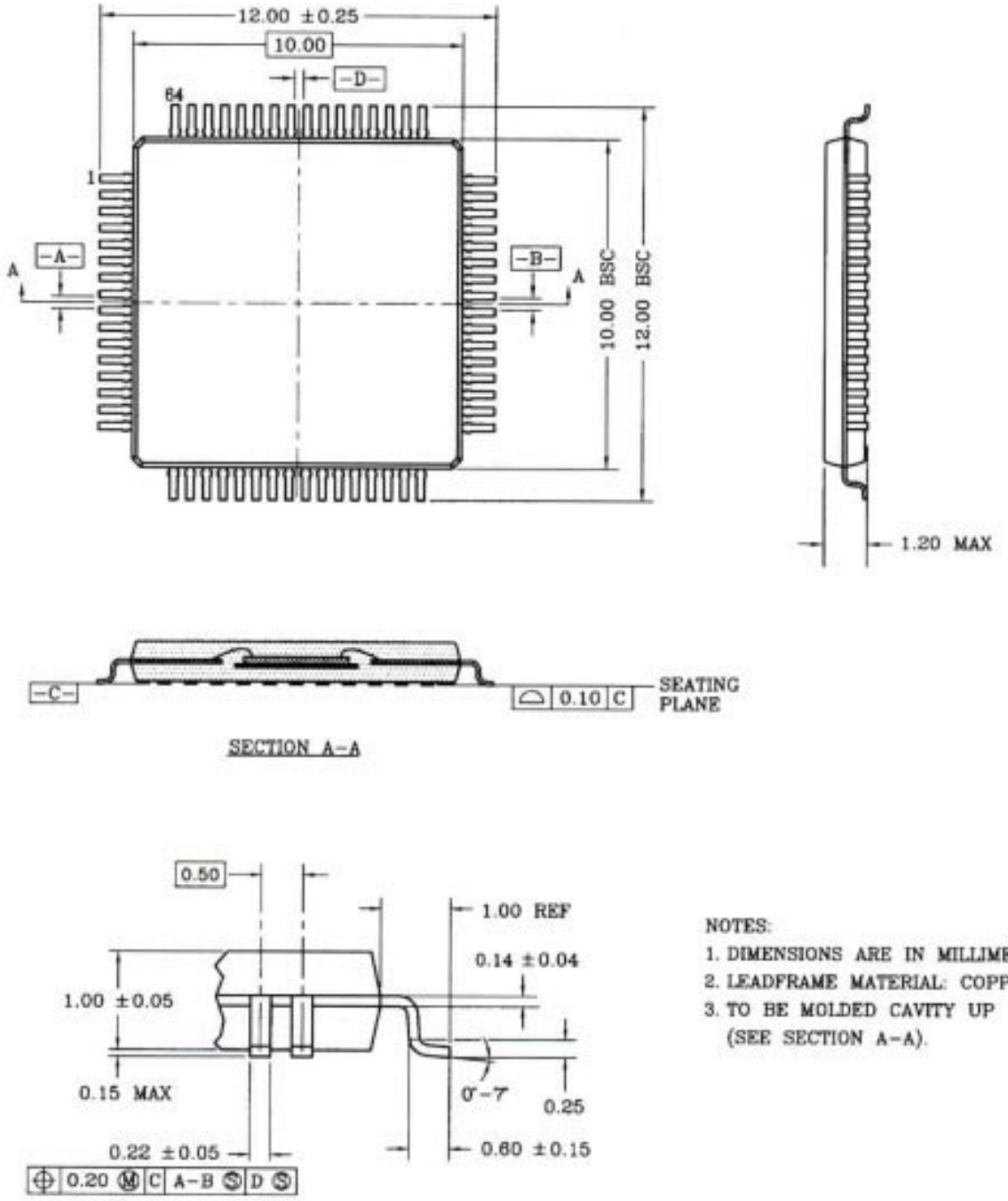
TABLE 3 : PIN DESCRIPTION

Pin	Pin Name	Direction
1	VDDI	-
2	XIN	I
3	XOUT	O
4	VSSI	-
5	SACLK	O
6	TEST	I
7	VDDI	-
8	VSSI	-
9	VAGC1	OD
10	IICDIV	I
11	VAGC2	OD
12	SADDR	I
13	VDDE5	-
14	VDDE	I
15	VSSE	I
16	CLR#	I
17	SCL	I
18	SDA	I/OD
19	SDAT	I/OD
20	SCLT	I/OD
21	ENSERI	I
22	TCK	I/O
23	TDI	I/O
24	VDDI	-
25	VSSI	-
26	TRST	I/O
27	TMS	I/O
28	TDO	O
29	GPIO	OD
30	VDDE	-
31	VSSE	-
32	CTRL	OD
33	UNCOR	O

Pin	Pin Name	Direction
34	PSYNC	O
35	OCLK	O
36	DEN	O
37	DO[7]	O
38	DO[6]	O
39	DO[5]	O
40	DO[4]	O
41	VDDI	-
42	VSSI	-
43	VDDE	-
44	VSSE	-
45	DO[3]	O
46	DO[2]	O
47	DO[1]	O
48	DO[0]	O
49	VS1	-
50	VD1	-
51	VS2	-
52	VD2	-
53	VREFP	-
54	VREFM	-
55	VD3	-
56	VS3	-
57	VIM	-
58	VIP	-
59	VS3	-
60	VD3	-
61	DVCC	-
62	DGND	-
63	PLLGND[5]	-
64	PLLVCC	-

Notes :
1.All inputs (I) are TTL, 5V tolerant inputs
2.OD are Open Drain 5V outputs, so they must be connected to a pull-up resistor to either VDD or VCC

PACKAGE DESCRIPTION



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. LEADFRAME MATERIAL: COPPER.
3. TO BE MOLDED CAVITY UP (SEE SECTION A-A).

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
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Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

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