DATA SHEET

TDA10045
Single Chip DVB-T Channel Receiver

Preliminary specification
File under Integrated Circuits, IC02

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FEATURES

- 2K and 8K COFDM demodulator (Fully DVB-T compliant : ETS 300-744).
- All modes supported including hierarchical modes.
- Fully automatic transmission parameters detection.
- DSP based synchronization (upgradability).
- No extra-host software required.
- On chip 10-bit ADC.
- 2^{nd} or 1^{st} IF variable analog input.
- Only fundamental Crystal oscillator needed.
- Frequency offset estimator to speed up the scan.
- RF Tuner input power measurement
- Parallel or serial transport stream interface.
- On chip FEC decoder.
- BER measurement (before and after Viterbi decoder)
- SNR estimation
- TPS bits I2C readable (including spare ones)
- Channel frequency response output.
- Controllable dedicated I2C tuner bus (5V tolerant).
- 2 low frequency spare DAC. ($\Delta\Sigma$)
- Spare I/O.
- CMOS 0.2µm technology.

APPLICATIONS

- DVB-T fully compatible.
- Digital data transmission using COFDM modulations.

DESCRIPTION

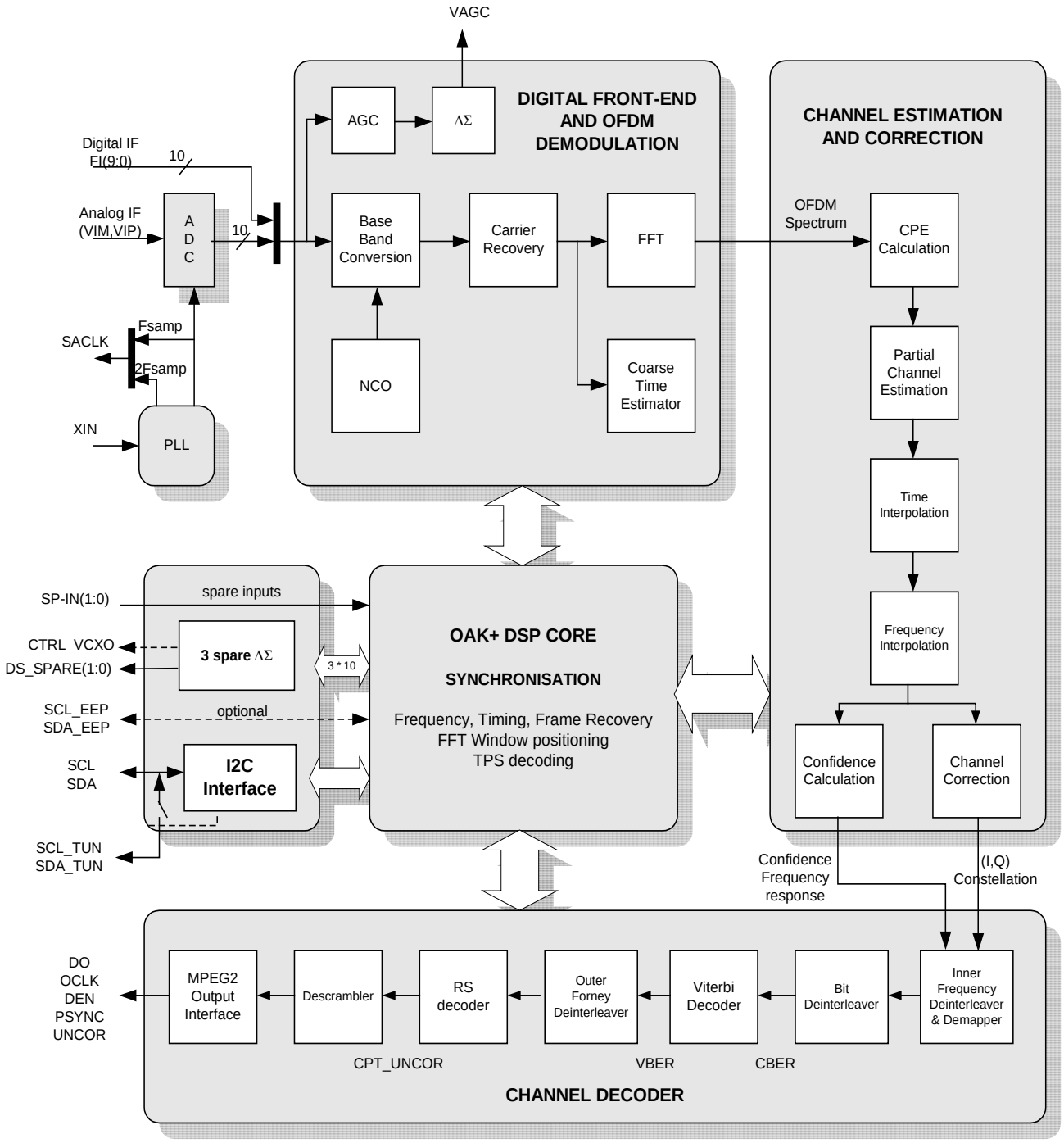
The TDA10045 is a single chip channel receiver for 2K and 8K COFDM modulated signals based on the ETSI specification (ETSI 300 744). The device interfaces directly to an IF signal, which could be either first or second IF and integrates a 10-bit AD converter, a NCO and a PLL, simplifying external logic requirements and limiting system costs.

The TDA10045 performs all the COFDM demodulation tasks from IF signal to the MPEG2 transport stream. An internal DSP core manages the synchronization and the control of the demodulation process, and implements specialy developed software for robustness against co and adjacent channel interferers, to deal with SFN echoes situations, and to help for a very fast scan of the bandwidth.
After base band conversion and FFT demodulation, the channel frequency response is estimated based on the scattered pilots, filtered in both time and frequency domains. This estimation is used as a correction on the signal, carrier by carrier. A common phase error and estimator is used to deal with the tuner phase noise.
The FEC decoder is automatically synchronized thanks to the frame synchronization algorithm that uses the TPS information included in the modulation.

This device is controlled via an I2C bus (called master). The chip provides 2 switchable I2C bus derived from the master. A tuner I2C bus to be disconnected from the I2C master when not necessary and an Eeprom I2C bus. The DSP software code can be fed to the chip via the master I2C bus or via the dedicated Eeprom I2C bus.

Designed in 0.2 µm CMOS technology and housed in a 100-pin MQFP package, the TDA10045 operates over the commercial temperature range.

FIGURE 1 : INTERNAL BLOCK DIAGRAM



INPUT - OUTPUT SIGNAL DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
CLOCK AND RESET SIGNALS			
CLR#	14	I	Asynchronous reset signal, active low
XIN	80	I	Crystal oscillator input pin. Typically a fundamental XTAL oscillator is connected between XIN and XOUT.
XOUT	79	O	Crystal oscillator output pin.
SACLK	33	O (3.3V)	Sampling frequency output. This output clock can be fed to an external (10-bit) ADC as sampling clock. Depending on “Sel_Saclk” (Reg CONFADC), SACLK could also provide twice the sampling clock.
CTRL_VCXO	3	O (3.3V)	If not in NCO mode, control of an external sampling VCXO (after low-pass filtering)
DEMODULATOR SIGNALS			
FI[9:0]	34-35-36-37-38-41-42-43-44-45	IO TRI	Input data from an external ADC, FI must be tied to ground when not used, positive notation (from 0 to 1023) or two's complement notation (from -512 to 511). In internal ADC mode, these outputs can be used to monitor extra demodulator output signal (constellation, frequency response).
FFT_WIN	30	IO TRI	Output or input signal indicating the start of the active data; equals 1 during complex sample 0 of the active FFT block. Can be used to synchronize 2 chips.
VAGC	4	O (3.3V)	output value from the Delta-Sigma Modulator, used to control a log-scaled amplifier (after analog filtering)
FEL	49	0D (5V)	front end lock. FEL is an output drain output and therefore requires an external pull up resistor.
IT	48	OD (5V)	Interrupt line. This output interrupt line can be configured by the I2C interface. See registers Itsel and Itstat. IT is an open drain output and therefore requires an external pull up resistor.
FEC OUTPUTS			
DO[7:0]	67-68-69-72-73-74-75-76	O (3.3V)	output data carrying the current sample of the current MPEG2 packet (188 bytes), delivered on the rising edge of OCLK by default. When the serial mode is selected, the output data is delivered by DO[0].
OCLK	66	O (3.3V)	Output CLock. OCLK is the output clock for the parallel DO[7:0] outputs. (may be inverted, see POCLK and DISABLE_TS I2C registers)
DEN	65	O (3.3V)	output data validation signal active high during the valid and regular data bytes (may be inverted, see PDEN and DISABLE_TS I2C registers).
PSYNC	64	O (3.3V)	Pulse Synchro. This output signal goes high on a rising edge of OCLK when a synchro byte is provided, then goes low until the next synchro byte (may be inverted, see PPSYNC and DISABLE_TS I2C registers).
UNCOR	63	O (3.3V)	RS error flag, active high on one RS packet if the RS decoder fails in correcting the errors (may be inverted, see PUNCOR and DISABLE_TS I2C registers).

ON-CHIP ADC SIGNALS			
VIM	92	I	Negative input to the A/D converter. This pin is DC biased to half supply through an internal resistor divider (2x20K resistors). In order to remain in the range of the ADC, the voltage difference between pins VIP and VIM should be between -0.5 and 0.5 volts (See SW I2C register).
VIP	91	I	Positive input to the A/D converter. This pin is DC biased to half supply through an internal resistor divider (2x20K resistors). In order to remain in the range of the ADC, the voltage difference between pins VIP and VIM should be between –0.5 and 0.5 volts.
VREFP	94	O	Positive voltage reference for the A/D converter. See SW I2C register for the output level.
VREFM	93	O	Negative voltage reference for the A/D converter. See SW I2C register for the output level.
VD1	100	I	Power supply input for the digital switching circuitry sensitive to the supply noise. The DC voltage should be 1,8V.
VS1	99	I	Ground return for the digital switching circuitry.
VD2	98	I	Power supply input for the analog clock drivers. The DC voltage should be 3.3V.
VS2	97	I	Ground return for the analog clock drivers.
VD3	95-90	I	Power supply input for the analog circuits. The DC voltage should be 3.3V.
VS3	96-89	I	Ground return for analog circuits.

I2C INTERFACES			
SCL	11	I	I2C master serial clock. Up to 700 kbit/s.
SDA	12	I/O	I2C master serial data inout, open drain I/O pad.
SADDR[1:0]	16-17	I	SADDR[1:0] are the 2 LSBs of the I2C address of the TDA10045. The MSBs are internally set to 00010. Therefore the complete I2C address of the TDA10045 is (MSB to LSB): 0,0,0,1,0,SADDR[1], SADDR[0]
SCL_TUN	9	OD	Tuner I2C serial clock signal.This signal derived from the master SCL can be set to high impedance when no tuner acces needed. (See BP_I2C_TUN register) (open drain)
SDA_TUN	10	I/O	Tuner I2C serial data signal.This signal derived from the master SDA can be set to high impedance when no tuner acces needed. (See BP_I2C_TUN register) (open drain)
SCL_EEP	5	O	Extra I2C clock to download DSP code from an external EEPROM. (Optional mode). Can be connected to the master I2C Bus. (open drain)
SDA_EEP	8	I/O	Extra I2C data bus to download DSP code from an external EEPROM. (Optional mode). Can be connected to the master I2C Bus. (open drain)
EEPADDR	15	I	EEPRAD is the LSB of the I2C address of the EEPROM. The MSBs are internally set to 101000. Therefore the complete I2C address of the EEPROM is (MSB to LSB): 1,0,1,0,0,0, EEPADDR

DSP SIGNALS			
DOWNLOAD	27	I	Processor control, Boot Mode If 0 the DSP downloads the software from an external eeprom on the dedicated I2C BUS (SDA_EEP, SCL_EEP). If 1 the software is downloaded in the I2C register CODE_IN from the host. In this case no need of external eeprom.
SP_IN[1:0]	28-29	I	Spare inputs
DS_SPARE_1	60	O (3.3V)	Spare delta-sigma output. Managed by the DSP to handle a low frequency DAC. (automatic first stage tuner AGC measurement for example).
DS_SPARE_2	59	O (3.3V)	Spare delta-sigma output. Managed by the DSP or by an I2C register to generate an analog level. (after a RC low-pass filter)

PLL SIGNALS			
PLLVCC	88	I	Power supply input for the analog circuits of the PLL module. (typ 3.3V)
PLLGND	87	I	Ground return for the analog circuits of the PLL module.
DGND	85	I	Ground return for the digital circuits of the PLL module.
DVCC	84	I	Power supply input for the digital circuits of the PLL module. (typ 1.8V)

BOUNDARY SCAN			
TCK	55	I	clock signal for boundary-scan. Wired to GND (if not used)
TDI	54	I	Input port for boundary-scan. Wired to GND (if not used)
TMS	53	I	Mode programming signal for boundary-scan. Wired to GND (if not used)
TRST	52	I	Asynchronous reset signal for boundary-scan. Wired to GND (if not used)
TDO	56	O (3.3V)	Output port for boundary-scan. NC (if not used)

POWER SUPPLIES			
VSS	2-7-19-26-32-40-47-58-62-71-78-82	GND 0V	Ground level 0 V
VDD50	25-46	VCC 5V	Positive Power Supply 5 V typical. If no need of 5V tolerant IO can be set to 3.3V (with caution).
VDD33	1-6-31-61-77	VDD 3.3V	Positive Power Supply 3.3V typical
VDD18	18-39-57-70-81	VDD 1.8V	Positive Power Supply 1.8V typical

FIGURE 2 : EXTERNAL BLOCK DIAGRAM

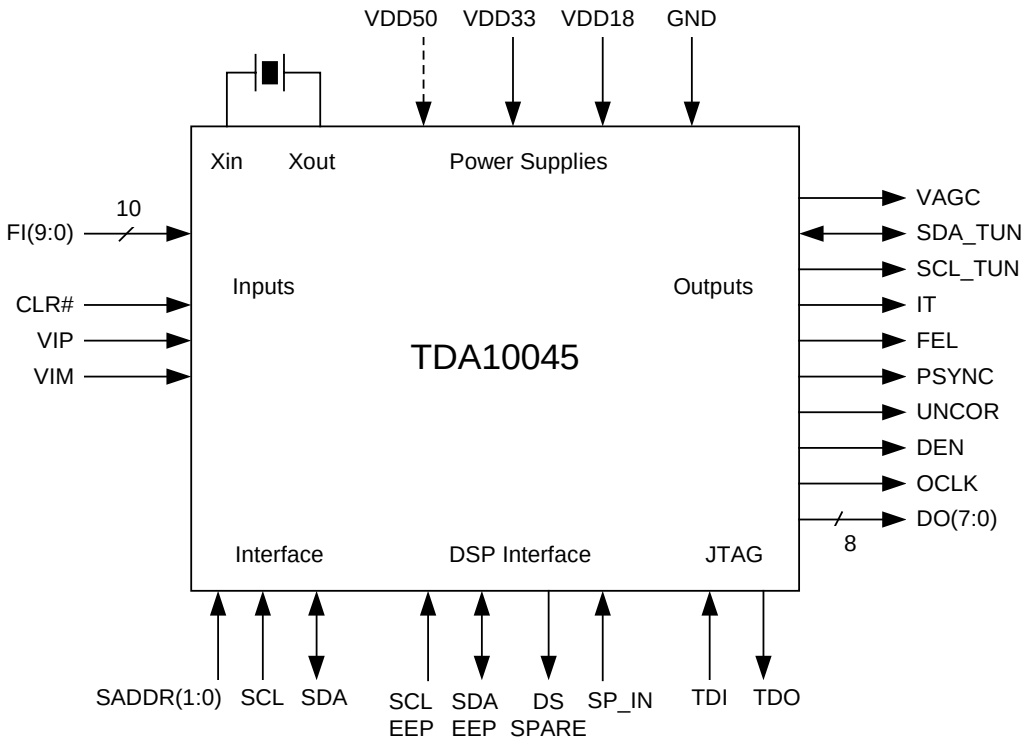
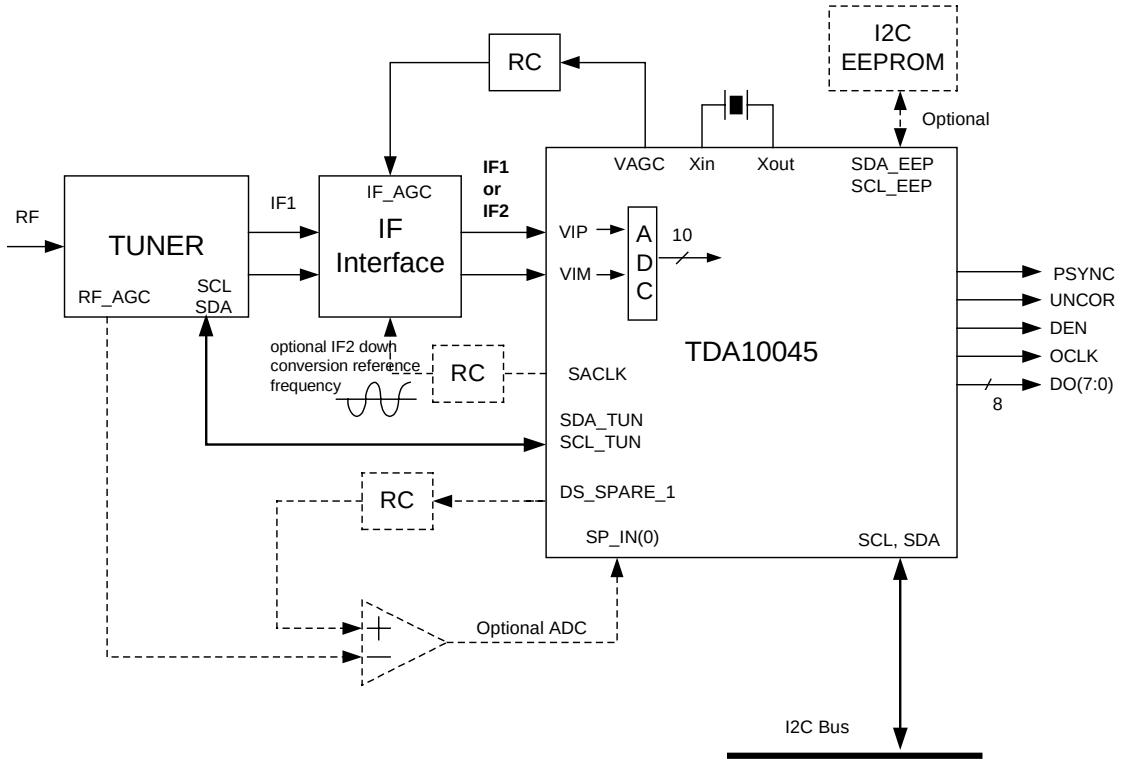


FIGURE 3 : TYPICAL APPLICATION : DVB-T FRONT END RECEIVER



TUNER

- A RF tracking filter tracks the RF wanted frequency and suppresses the image.
- A first local AGC could be done at RF level, the AGC level information could be provided externaly and the chip offers facilities to measure this level thanks to the optional ADC (Rem: this measure is automaticaly made by the DSP, the host has just to read the result).
- A mixer oscillator and a PLL down-convert the RF signal to Intermediate Frequency IF1 typicaly 36.125 MHz
- SAW filters reject the adjacent analog channels power at IF1

IF INTERFACE

- It is either an analog IF amplifier when IF1 is sampled (digital down-conversion concept)
- Or an analog IF amplifier followed by a down-conversion from IF1 to IF2 at few MHz (ex :4.57 MHz)
- When this second solution is used, the ADC sampling clock could be used (after low-pass filtering) as reference clock for down-conversion (rem : twice the ADC sampling clock could also be provided – see reg CONFADC).
- The IF amplifier is controlled by the digital AGC of the chip. A simple RC circuitry will filter the single-bit ($\Delta\Sigma$ modulated) AGC control (VAGC)
- The sampling clock could also be used to control an external ADC, then the input of the chip are digital (FI[9 :0])

TDA10045

- The chip is controlled by an I2C Bus and driven by an external low-cost crystal oscillator
- The software of the embedded DSP could be downloaded from the main I2C bus or from a dedicated I2C Bus connected to an external slave I2C Eeprom.
- An internal bidirectional switch allows to program the tuner through the chip and then switch off this link in order to avoid phase noise distortions due to I2C Bus traffic

FIGURE 4 : PIN DIAGRAM

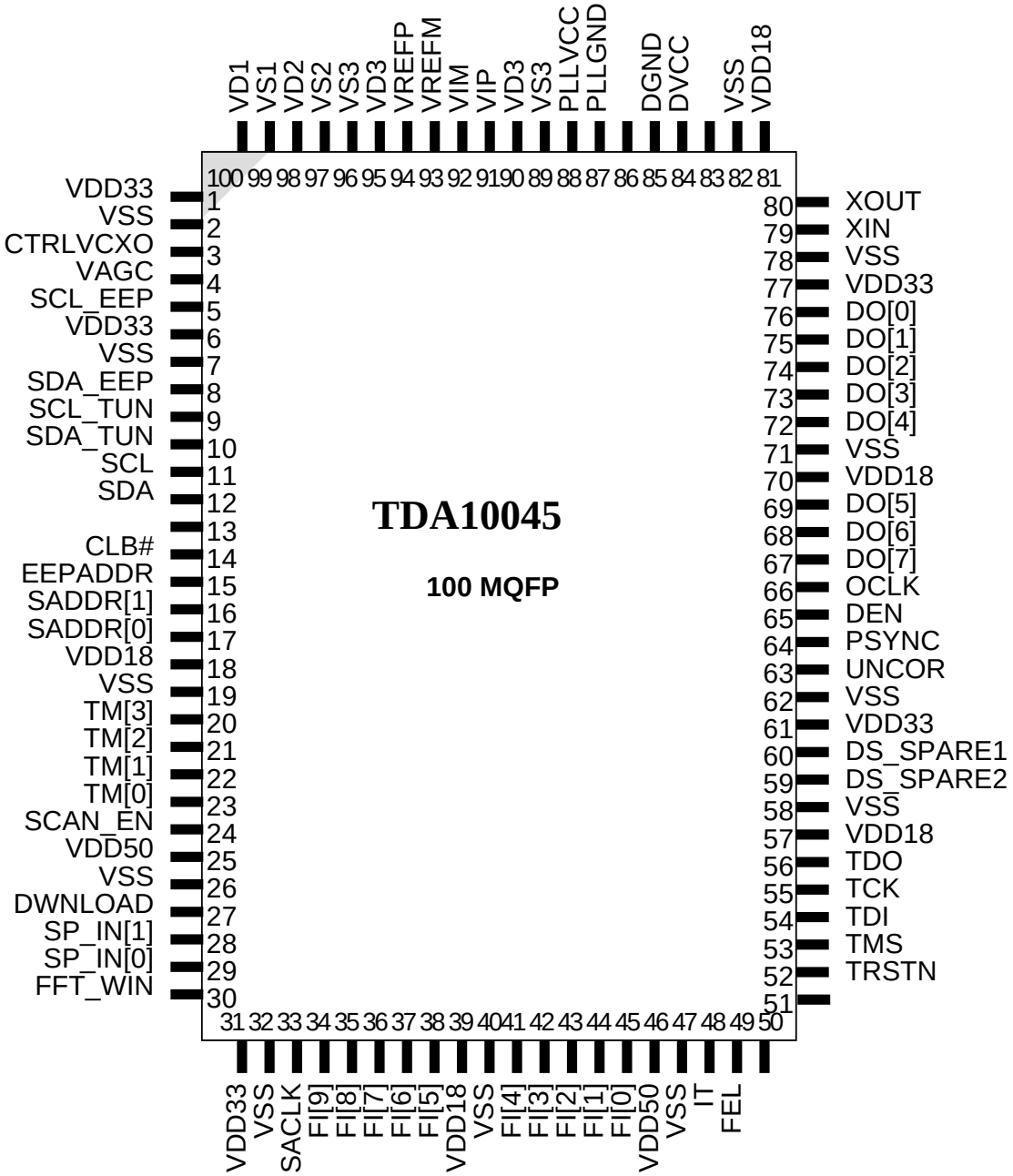


TABLE 1 : PIN DESCRIPTION

Pin	Pin Name	Direction
1	VDD33	-
2	VSS	-
3	CTRLVCXO	I
4	VAGC	O
5	SCL_EEP	O
6	VDD33	-
7	VSS	-
8	SDA_EEP	IOD
9	SCL_TUN	OD
10	SDA_TUN	IOD
11	SCL	I
12	SDA	IOD
13	-	-
14	CLB#	I
15	EEPADDR	I
16	SADDR[1]	I
17	SADDR[0]	I
18	VDD18	-
19	VSS	-
20	VSS	I^3
21	VSS	I^3
22	VSS	I^3
23	VSS	I^3
24	VSS	I^3
25	VDD50	-
26	VSS	-
27	DWNLOAD	I
28	SP_IN[1]	I
29	SP_IN[0]	I
30	FFT_WIN	IO
31	VDD33	-
32	VSS	-
33	SACLK	O
34	FI[9]	IO
35	FI[8]	IO
36	FI[7]	IO
37	FI[6]	IO
38	FI[5]	IO
39	VDD18	-
40	VSS	-
41	FI[4]	IO
42	FI[3]	IO
43	FI[2]	IO
44	FI[1]	IO
45	FI[0]	IO
46	VDD50	-
47	VSS	-
48	IT	OD
49	FEL	OD
50	-	-
51	-	-
52	TRSTN	I
53	TMS	I
54	TDI	I
55	TCK	I
56	TDO	O
57	VDD18	-
58	VSS	-
59	DS_SPARE2	O
60	DS_SPARE1	O
61	VDD33	-
62	VSS	-
63	UNCOR	O
64	PSYNC	O
65	DEN	O
66	OCLK	O
67	DO[7]	O
68	DO[6]	O
69	DO[5]	O
70	VDD18	-
71	VSS	-
72	DO[4]	O
73	DO[3]	O
74	DO[2]	O
75	DO[1]	O
76	DO[0]	O
77	VDD33	-
78	VSS	-
79	XIN	I
80	XOUT	O
81	VDD18	-
82	VSS	-
83	-	-
84	DVCC	-
85	DGND	-
86	-	-
87	PPLGND	-
88	PLLVCC	-
89	VS3	-
90	VD3	-
91	VIP	-
92	VIM	-
93	VREFM	-
94	VREFP	-
95	VD3	-
96	VS3	-
97	VS2	-
98	VD2	-
99	VS1	-
100	VD1	-

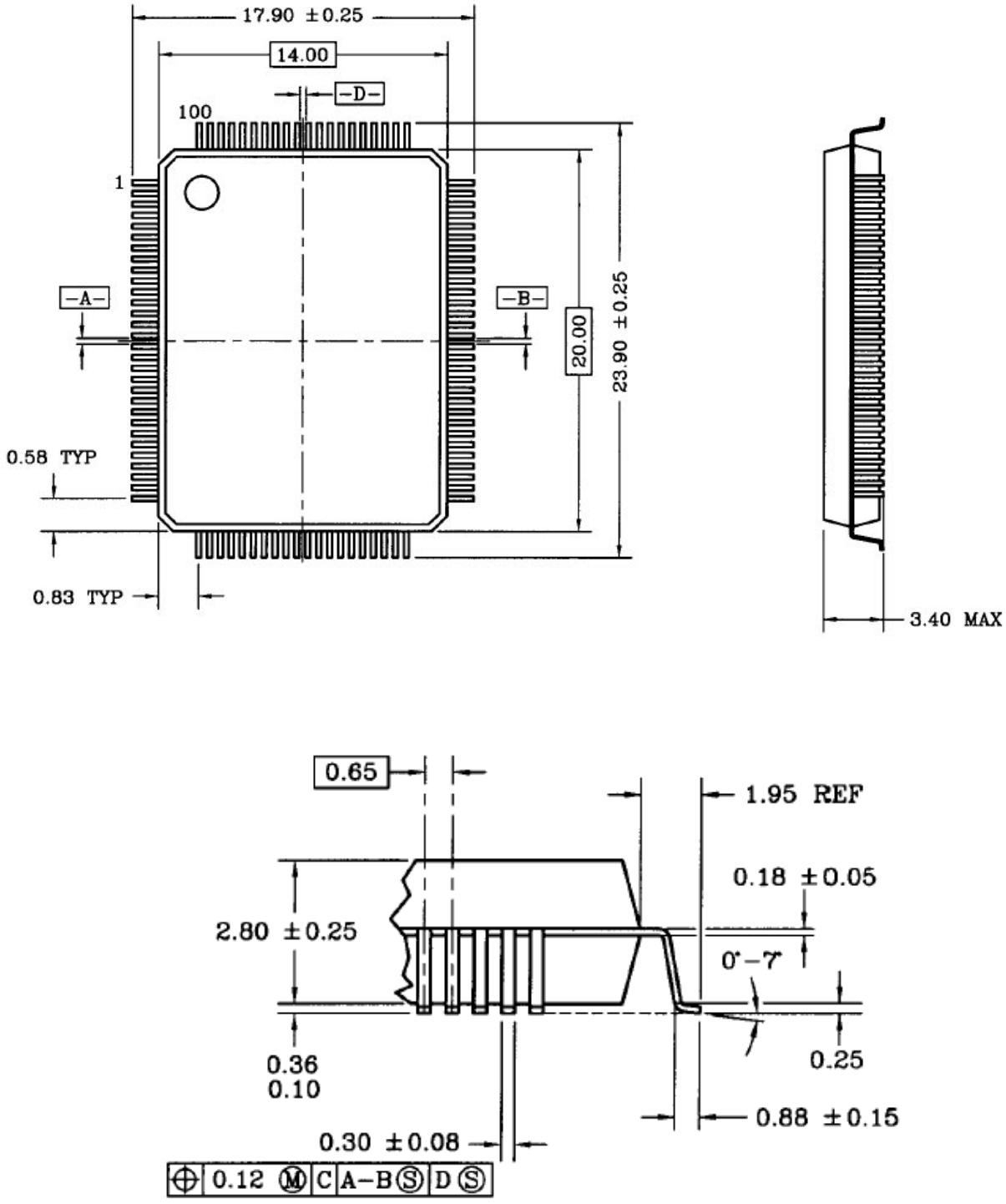
Notes :

1.All inputs (I) are TTL, 5V tolerant inputs. (If VDD50 set to 5V).

2.OD are Open Drain 5V outputs, so they must be connected to a pull-up resistor to either VDD33 or VDD50

3. Foundry test IO, inputs **must be connected to GND**.

PACKAGE INFORMATION



NOTE : Dimensions are in millimeters

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DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
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Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

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Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

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Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

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Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 5F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2451, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
60/14 MOO 11, Bangna Trad Road KM. 3, Bagna, BANGKOK 10260,
Tel. +66 2 361 7910, Fax. +66 2 398 3447

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
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United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
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Tel. +381 11 3341 299, Fax.+381 11 3342 553

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Marketing Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN,
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