DATA SHEET

TEA1610P; TEA1610T
Zero-voltage-switching resonant converter controller

Product specification
2001 Apr 25
File under Integrated Circuits, IC11

Philips Semiconductors

PHILIPS

FEATURES

- Integrated high voltage level-shift function
- Integrated high voltage bootstrap diode
- Transconductance error amplifier for ultra high-ohmic regulation feedback
- Latched shut-down circuit for overcurrent and overvoltage protection
- Low start-up current (green function)
- Adjustable minimum and maximum frequencies
- Adjustable dead time
- Undervoltage lockout.

GENERAL DESCRIPTION

The TEA1610 is a monolithic integrated circuit implemented in a high-voltage DMOS process. The circuit is a high voltage controller for a zero-voltage switching resonant converter. The IC provides the drive function for two discrete power MOSFETs in a half-bridge configuration. It also includes a level-shift circuit, an oscillator with accurately-programmable frequency range, a latched shut-down function and a transconductance error amplifier.

To guarantee an accurate 50% switching duty factor, the oscillator signal passes through a divide-by-two flip-flop before being fed to the output drivers.

The circuit is very flexible and enables a broad range of applications for different mains voltages.

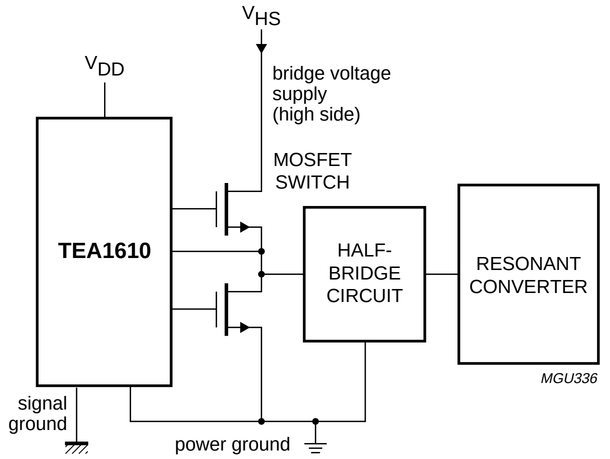


Fig.1 Basic configuration.

APPLICATIONS

- TV and monitor power supplies
- High voltage power supplies.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{HS}	bridge voltage supply (high side)		600	V
$I_{GH(source)}$; $I_{GL(source)}$	gate driver source current		–225	mA
$I_{GH(sink)}$; $I_{GL(sink)}$	gate driver sink current		300	mA
$f_{bridge(max)}$	maximum bridge frequency	C_f = 100 pF (see Fig.10)	550	kHz
$V_{I(CM)}$	error amplifier common mode input voltage		2.5	V

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1610P	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
TEA1610T	SO16	plastic small outline package; 16 leads; body width 3.9 mm; low stand-off height	SOT109-2

BLOCK DIAGRAM

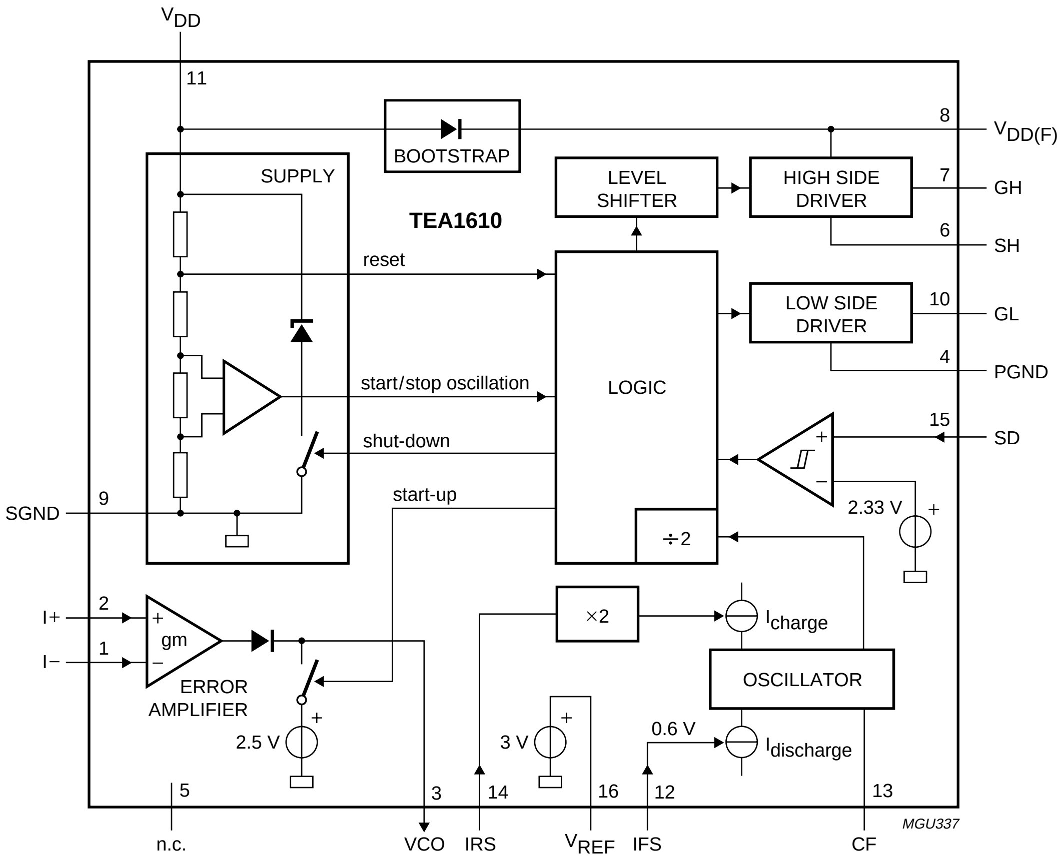


Fig.2 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
I–	1	error amplifier inverting input
I+	2	error amplifier non-inverting input
VCO	3	error amplifier output
PGND	4	power ground
n.c.	5	not connected (high voltage spacer)
SH	6	high side switch source
GH	7	gate of the high side switch
$V_{DD(F)}$	8	floating supply voltage for the high side driver
SGND	9	signal ground
GL	10	gate of the low side switch
V_{DD}	11	supply voltage
IFS	12	oscillator discharge current input
CF	13	oscillator capacitor
IRS	14	oscillator charge current input
SD	15	shut-down input
V_{REF}	16	reference voltage

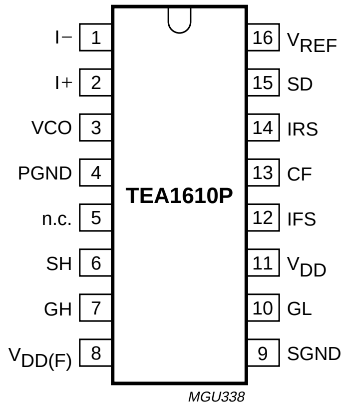


Fig.3 Pin configuration: TEA1610P.

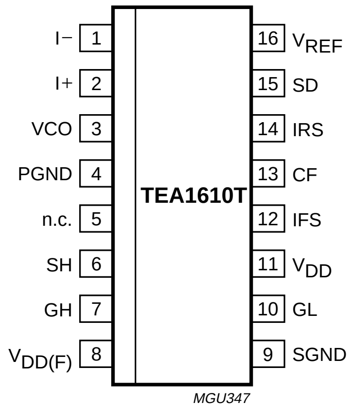


Fig.4 Pin configuration: TEA1610T.

FUNCTIONAL DESCRIPTION

Start-up

When the applied voltage at V_{DD} reaches $V_{DD(initial)}$ (see Fig.5), the low side power switch is turned-on while the high side power switch remains in the non-conducting state. This start-up output state guarantees the initial charging of the bootstrap capacitor (C_{boot}) used for the floating supply of the high side driver.

During start-up, the voltage on the frequency capacitor (C_f) is zero and defines the start-up state. The output voltage of the error amplifier is kept constant (typ. 2.5 V) and switching starts at about 80% of the maximum frequency at the moment pin V_{DD} reaches the start level.

The start-up state is maintained until V_{DD} reaches the start level (13.5 V), the oscillator is activated and the converter starts operating.

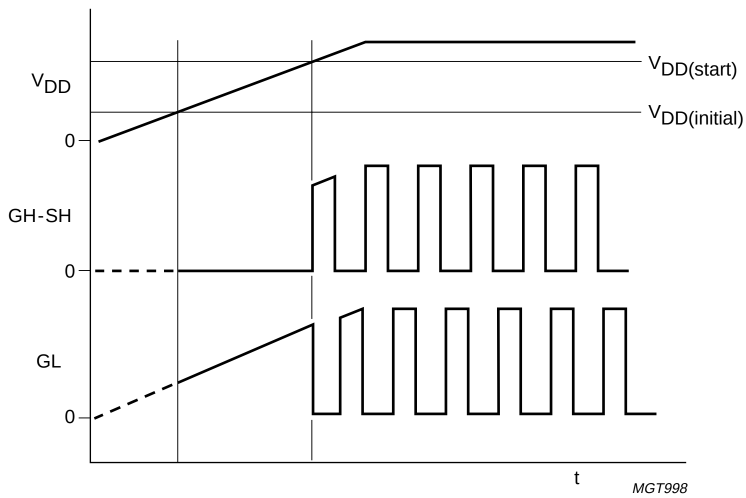


Fig.5 Start-up.

Oscillator

The internal oscillator is a current-controlled oscillator that generates a sawtooth output. The frequency of the sawtooth is determined by the external capacitor C_f and the currents flowing into the IFS and IRS pins.

The minimum frequency and the dead time are set by the capacitor C_f and resistors $R_{f(min)}$ and R_{dt}. The maximum frequency is set by resistor $R_{\Delta f}$ (see Fig.10). The oscillator frequency is exactly twice the bridge frequency to achieve an accurate 50% duty factor. An overview of the oscillator and driver signals is given in Fig.6.

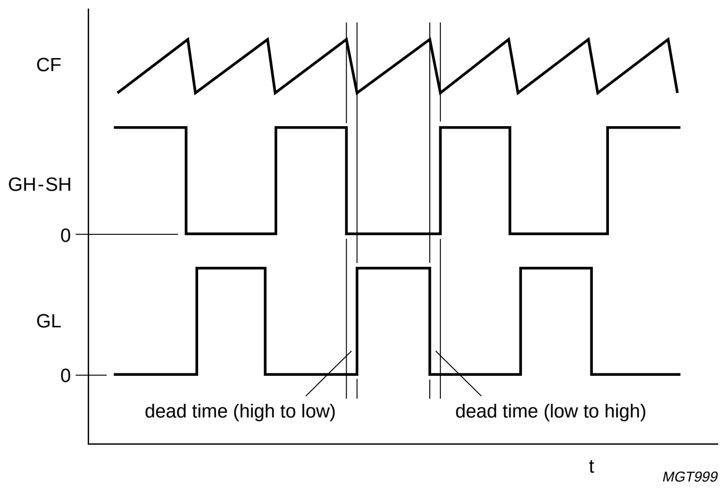


Fig.6 Oscillator and driver signals.

Dead time resistor R_{dt} (see Fig.10)

The dead time resistor R_{dt} is connected between the 3 V reference pin (V_{REF}) and the IFS current input pin. The voltage on the IFS pin is kept constant at a temperature independant value of 0.6 V. The current that flows into the IFS pin is determined by the value of resistor R_{dt} and the 2.4 V voltage drop across this resistor. The IFS input current equals the discharge current of capacitor C_f and determines the falling slope of the oscillator.

The falling slope time is used to create a dead time (t_{dt}) between two successive switching actions of the half-bridge switches:

$$I_{IFS} = \frac{2.4\ V}{R_{dt}}$$

$$t_{dt} = \frac{C_f \times \Delta V_{Cf}}{I_{IFS}}$$

$$t_{IFS} = t_{dt}$$

Minimum frequency resistor (see Fig.10)

The $R_{f(min)}$ resistor is connected between the V_{REF} pin (3 V reference voltage) and the IRS current input (held at a temperature independant voltage level of 0.6 V). The charge current of the capacitor C_f is twice the current flowing into the IRS pin.

The $R_{f(min)}$ resistor has a voltage drop of 2.4 V and its resistance defines the minimum charge current (rising slope) of the C_f capacitor if the control current is zero. The minimum frequency is defined by this minimum charge current (I_{IRS1}) and the discharge current:

$$I_{IRS1} = \frac{2.4\ V}{R_{f(min)}}$$

$$t_{IRS1} = \frac{C_f \times \Delta V_{Cf}}{2 \times I_{IRS1}}$$

$$f_{min} = \frac{1}{t_{dt} + t_{IRS1}}$$

Maximum frequency resistor

The output voltage is regulated by changing the frequency of the half-bridge converter. The maximum frequency is determined by the $R_{\Delta f}$ resistor which is connected between the error amplifier output VCO and the oscillator current input pin IRS. The current that flows through the $R_{\Delta f}$ resistor (I_{IRS2}) is added to the current flowing through the $R_{f(min)}$ resistor. As a result, the charge current I_{CF} increases and the oscillation frequency increases. As the falling slope of the oscillator is constant, the relationship between the output frequency and the charge current is not a linear function (see Figs 7 and 9):

$$I_{IRS2} = \frac{V_{VCO} - 0.6}{R\Delta f}$$

$$t_{IRS2} = \frac{C_f \times \Delta V_{Cf}}{I_{IRS1} + I_{IRS2}} \times 2$$

The maximum output voltage of the error amplifier and the value of $R_{\Delta f}$ determine the maximum frequency:

$$I_{IRS2(max)} = \frac{V_{VCO(max)} - 0.6}{R_{\Delta f}}$$

$$t_{IRS(min)} = \frac{C_f \times \Delta V_{Cf}}{I_{IRS1} + I_{IRS2(max)}} \times 2$$

$$f_{max} = \frac{1}{T_{osc}}$$

$$T_{osc} = t_{IRS(min)} + t_{IFS}$$

Bridge frequency accuracy is optimum in the low frequency region. At higher frequencies both the dead time and the oscillator frequency show a decay.

The frequency of the oscillator depends on the value of capacitor C_f, the peak-to-peak voltage swing V_{Cf} and the charge and discharge currents. However, at higher frequencies the accuracy decreases due to delays in the circuit.

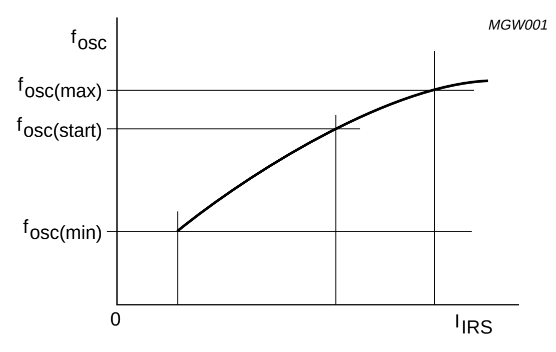


Fig.7 Frequency range.

Error amplifier

The error amplifier is a transconductance amplifier. Thus the output current at pin VCO is determined by the amplifier transconductance and the differential voltage on input pins I+ and I–. The output current I_{VCO} is fed to the IRS input of the current-controlled oscillator.

The source capability of the error amplifier increases current in the IRS pin when the differential input voltage is positive. Therefore the minimum current is determined by resistor $R_{f(min)}$ and the minimum frequency setting is independent of the characteristics of the error amplifier.

The error amplifier has a maximum output current of 0.5 mA for an output voltage up to 2.5 V. If the source current decreases, the oscillator frequency also decreases resulting in a higher regulated output voltage.

During start-up, the output voltage of the amplifier is held at a constant value of 2.5 V. This voltage level defines, together with resistor $R_{\Delta f}$, the initial switching frequency of the TEA1610 after start-up.

Shut-down

The shut-down input (SD) has an accurate threshold level of 2.33 V. When the voltage on input SD reaches 2.33 V, both power switches immediately switch off and the TEA1610 enters shut-down mode.

During shut-down mode, pin V_{DD} is clamped by an internal Zener diode at 12.0 V with 1 mA input current. This clamp prevents V_{DD} rising above the rating of 14 V due to low supply current to the TEA1610 in shut-down mode.

When the TEA1610 is in the shut-down mode, it can be activated again only by lowering V_{DD} below the V_{DD} reset level (5.3 V typical). The shut-down latch is then reset and a new start-up cycle can commence (see Fig.8).

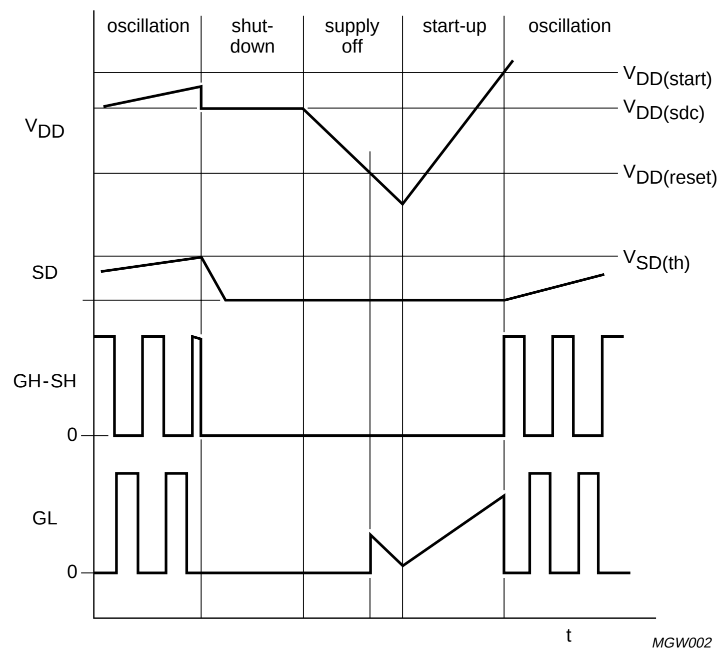


Fig.8 Shut-down.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referred to the ground pins which must be interconnected externally; positive currents flow into the IC.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Voltages					
V_{SH}	high side driver voltage		0	600	V
V_{DD}	supply voltage		0	14	V
V_{I+}	amplifier non-inverting input voltage		0	5	V
V_{I-}	amplifier inverting input voltage		0	5	V
V_{SD}	shut-down input voltage		0	5	V
Currents					
I_{IFS}	oscillator falling slope input current		–	1	mA
I_{IRS}	oscillator rising slope input current		–	1	mA
I_{REF}	V_{REF} source current		–	–2	mA
Power and temperature					
P_{tot}	total power dissipation	T_{amb} < 70 °C	–	0.8	W
T_{amb}	ambient temperature	operating	–25	+70	°C
T_{stg}	storage temperature		–25	+150	°C
Handling					
V_{ES}	electrostatic handling voltage	note 1	–	2000	V
		note 2	–	200	V

Notes

1. Human body model class 2: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
2. Machine model class 2: equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and 10 Ω resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	100	K/W
$R_{th(j-pin)}$	thermal resistance from junction to pin		50	K/W

QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611-E”*.

CHARACTERISTICS

All voltages are referred to the ground pins which must be connected externally; positive currents flow into the IC; V_{DD} = 13 V and T_{amb} = 25 °C; tested in the circuit of Fig.10; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
High voltage pins $V_{DD(F)}$, GH and SH						
I_L	leakage current	$V_{DD(F)}$, V_{GH} and V_{SH} = 600 V	–	–	30	µA
Supply pin V_{DD}						
$V_{DD(initial)}$	supply voltage for defined driver output	low side on; high side off	–	4	5	V
$V_{DD(start)}$	start oscillator voltage		12.9	13.4	13.9	V
$V_{DD(stop)}$	stop oscillator voltage		9.0	9.4	9.8	V
$V_{DD(hys)}$	start-stop hysteresis voltage		3.8	4.0	4.2	V
$V_{DD(sdc)}$	shut-down clamp voltage	low side off; high side off; I_{DD} = 1 mA	11.0	12.0	13.0	V
$V_{DD(reset)}$	reset voltage		4.5	5.3	6.0	V
I_{DD}	supply current:					
	start-up	low side on; high side off	130	180	220	µA
	operating	C_f = 100 pF; I_{IFS} = 0.5 mA; I_{IRS} = 50 µA; C_o = 200 pF; note 1	–	2.4	–	mA
	shut-down	low side off; high side off; V_{DD} = 9 V	–	130	180	µA
Reference voltage pin V_{REF}						
V_{REF}	reference voltage	I_{REF} = 0 mA	2.9	3.0	3.1	V
I_{REF}	current capability	source only	–1.0	–	–	mA
$Z_{o(VREF)}$	output impedance	I_{REF} = –1 mA	–	5.0	–	Ω
$\frac{\Delta V_{REF}}{\Delta T}$	temperature coefficient	I_{REF} = 0; T_j = 25 to 150 °C	–	–0.3	–	mV/K
Current controlled oscillator pins IRS, IFS, CF						
$I_{CF(ch)(min)}$	minimum CF charge current	I_{IRS} = 15 µA; V_{CF} = 2 V	28	30	32	µA
$I_{CF(ch)(max)}$	maximum CF charge current	I_{IRS} = 200 µA; V_{CF} = 2 V	340	380	420	µA
V_{IRS}	pin IRS voltage	I_{IRS} = 200 µA	570	600	630	mV
$I_{CF(dis)(min)}$	minimum CF discharge current	I_{IRS} = 50 µA; V_{CF} = 2 V	47	50	53	µA
$I_{CF(dis)(max)}$	maximum CF discharge current	I_{IFS} = 1 mA; V_{CF} = 2 V	0.93	0.98	1.03	mA
V_{IFS}	pin IFS voltage	I_{IFS} = 1 mA	570	600	630	mV
$f_{bridge(min)}$	minimum bridge frequency (for stable operation)	C_F = 100 pF; I_{IFS} = 0.5 mA; I_{IRS} = 50 µA; $f_{bridge} = \frac{f_{osc}}{2}$	188	200	212	kHz
$f_{bridge(max)}$	maximum bridge frequency	C_f = 100 pF; I_{IFS} = 1 mA; I_{IRS} = 200 µA; $f_{bridge} = \frac{f_{osc}}{2}$; note 2	450	500	550	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CF(L)}$	CF trip level LOW	DC level	–	1.27	–	V
$V_{CF(H)}$	CF trip level HIGH	DC level	–	3.0	–	V
$V_{Cf(p-p)}$	C_f voltage (peak-to-peak value)		1.63	1.73	1.83	V
t_{dt}	dead time	C_f = 100 pF; I_{IFS} = 0.5 mA; I_{IRS} = 50 μA	0.37	0.40	0.43	μs
Output drivers						
$I_{GH(source)}$	high side output source current	$V_{DD(F)}$ = 13 V; V_{SH} = 0; V_{GH} = 0	–135	–180	–225	mA
$I_{GH(sink)}$	high side output sink current	$V_{DD(F)}$ = 13 V; V_{SH} = 0; V_{GH} = 13 V	–	300	–	mA
$I_{GL(source)}$	low side output source current	V_{GL} = 0	–135	–180	–225	mA
$I_{GL(sink)}$	low side output sink current	V_{GL} = 14 V	–	300	–	mA
$V_{GH(H)}$	high side output voltage HIGH	$V_{DD(F)}$ = 13 V; V_{SH} = 0; I_{GH} = 10 mA	10.8	12	–	V
$V_{GH(L)}$	high side output voltage LOW	$V_{DD(F)}$ = 13 V; V_{SH} = 0; I_{GH} = 10 mA	–	0.2	0.5	V
$V_{GL(H)}$	low side output voltage HIGH	I_{GL} = 10 mA	10.8	12	–	V
$V_{GL(L)}$	low side output voltage LOW	I_{GL} = 10 mA	–	0.2	0.5	V
$V_{d(boot)}$	bootstrap diode voltage drop	I = 5 mA	1.5	1.8	2.1	V
Shut-down input pin SD						
I_{SD}	input current	V_{SD} = 2.33 V	0	0.2	0.5	μA
$V_{SD(th)}$	threshold level		2.26	2.33	2.40	V
Error amplifier pins I+, I–, VCO						
$I_{I(CM)}$	common mode input current	$V_{I(CM)}$ = 1 V	–	–0.1	–0.5	μA
$V_{I(CM)}$	common mode input voltage		–	–	2.5	V
$V_{I(offset)}$	input offset voltage	$V_{I(CM)}$ = 1 V; I_{VCO} = –10 mA	–2	0	+2	mV
g_m	transconductance	$V_{I(CM)}$ = 1 V; source only	–	330	–	μA/mV
A_o	open loop gain	R_L = 10 kΩ to GND; $V_{I(CM)}$ = 1 V	–	70	–	dB
GB	gain bandwidth product	R_L = 10 kΩ to GND; $V_{I(CM)}$ = 1 V	–	5	–	MHz
$V_{VCO(max)}$	maximum output voltage	operating; R_L = 10 kΩ to GND	3.2	3.6	4.0	V
$I_{VCO(max)}$	maximum output current	operating; V_{VCO} = 1 V	–0.4	–0.5	–0.6	mA
$V_{VCO(start)}$	output voltage during start-up	I_{VCO} = 0.3 mA	2.30	2.50	2.70	V

Notes

1. Supply current I_{DD} will increase with increasing bridge frequency to drive the capacitive load of two MOSFETs. Typical MOSFETs for the TEA1610 application are 8N50 (Philips type PHX80N50E, $Q_{g(tot)}$ = 55 nC typ.) and these will increase the supply current at 150 kHz according to the following formula:
   $\Delta I_{DD} = 2 \times Q_{g(tot)} \times f_{bridge} = 2 \times 55\ nC \times 150\ kHz = 16.5\ mA$.
2. The frequency of the oscillator depends on the value of capacitor C_f, the peak-to-peak voltage swing V_{CF} and the charge/discharge currents $I_{CF(ch)}$ and $I_{CF(dis)}$.

APPLICATION INFORMATION

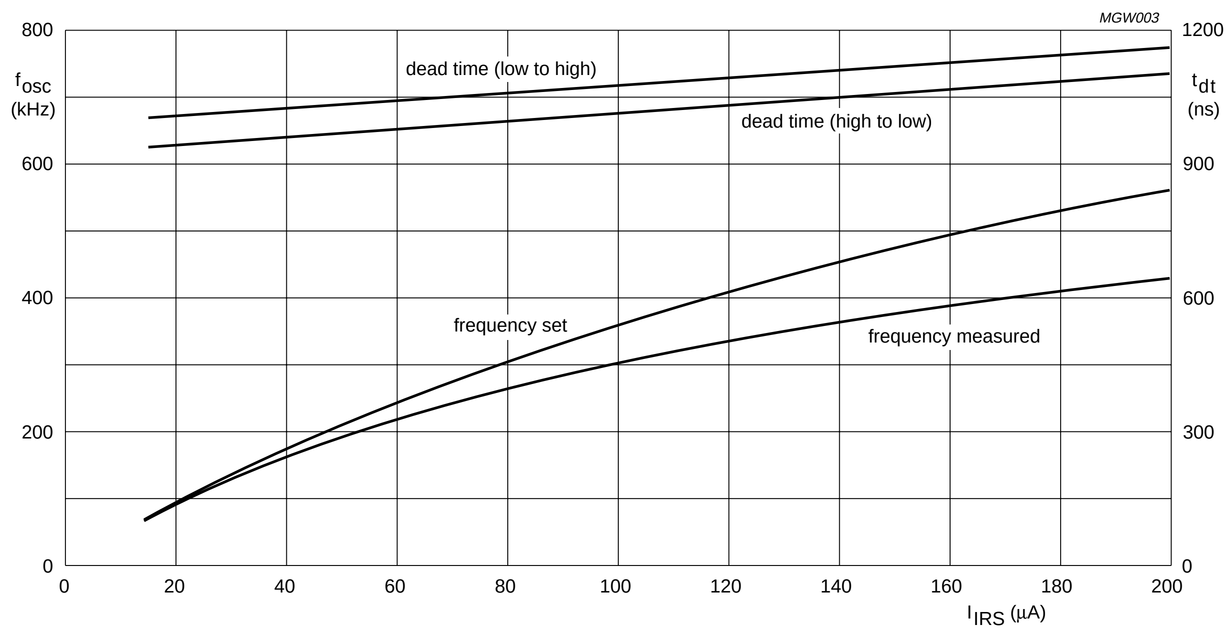
An application example of a zero-voltage-switching resonant converter application using TEA1610 is shown in Fig.10. In the off-mode the V_{DD} voltage is pulled below the stop level of 9.4 V by the 7.5 V Zener diode and the half-bridge is not driven. In the on-mode the TEA1610 starts-up with a high-ohmic bleeder resistor. After passing the level for start of oscillation, the TEA1610 is in normal operating mode and consumes the normal supply current delivered by the 12 V supply. The dead time is set by R_{dt} and C_f. The minimum frequency is adjusted by $R_{f(min)}$ and the frequency range is set by $R_{\Delta f}$. The output voltage is adjusted with a potentiometer connected to the inverting input of the error amplifier and is regulated via a feedback circuit. The shut-down input is used for overvoltage protection. To prevent interference, filter capacitors can be added on pins IFS, IRS and V_{REF}. The maximum value of each filter capacitor is 100 pF.

Practical values of the application example are given in Fig.9 in which the measured oscillator frequency with capacitor C_f = 220 pF is shown as a function of the charge current I_{IRS}. Note that the slope of the measured frequency differs from the theoretical frequency (frequency set) calculated as described in Section “Maximum frequency resistor”.

The measured dead time is directly related to charge current (total current flowing into pin IRS) and therefore to oscillator frequency.

The measured frequency graph can be used to determine the required $R_{\Delta f}$ resistor for a certain maximum frequency in an application with the same value of capacitor C_f.

More application information can be found in application note *“AN99011”*.



f_{osc} at I_{IFS} = 500 μA.
$f_{osc} = 2 \times f_{bridge}$.

Fig.9 Oscillator frequency and measured dead time as functions of charge current I_{IRS}.

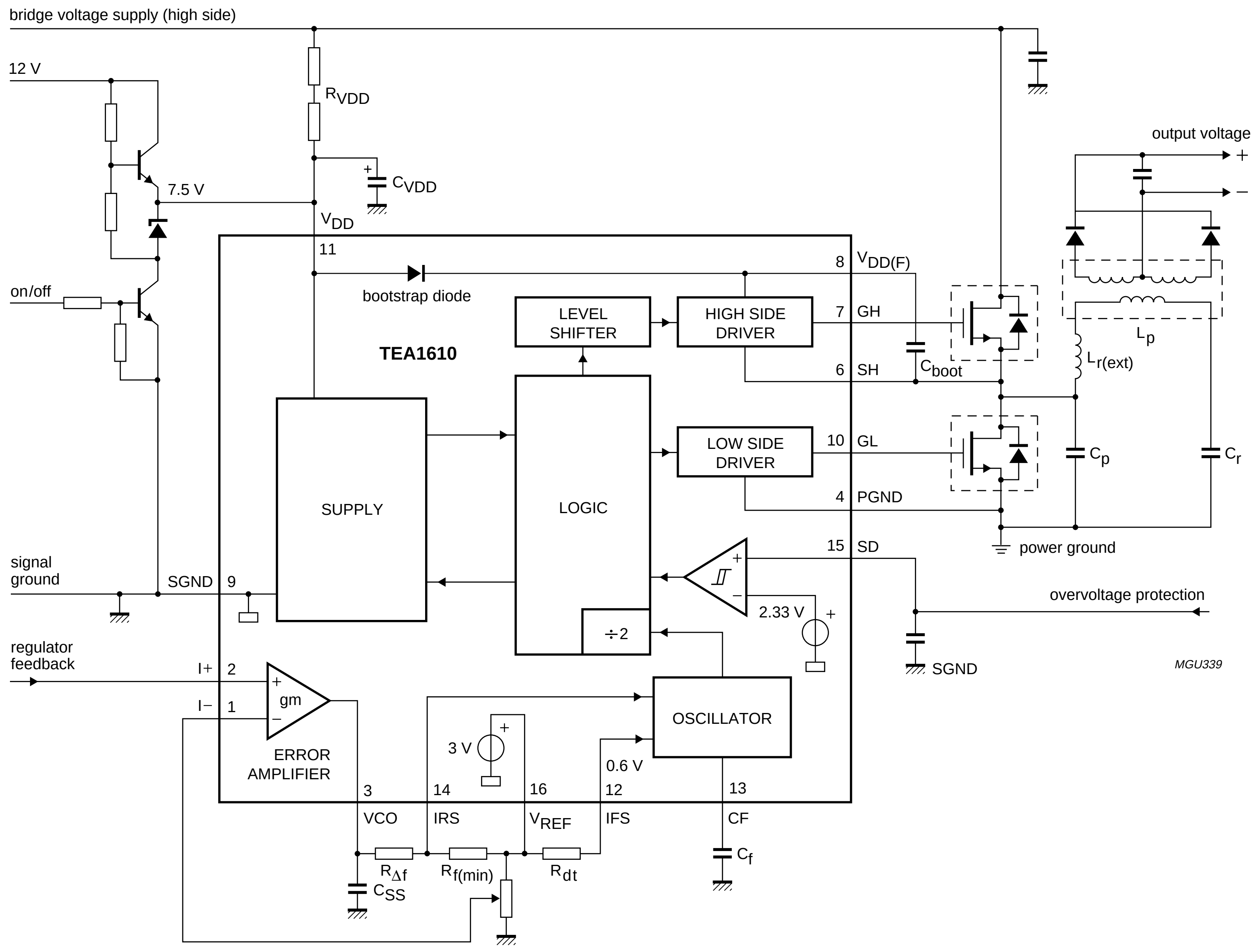
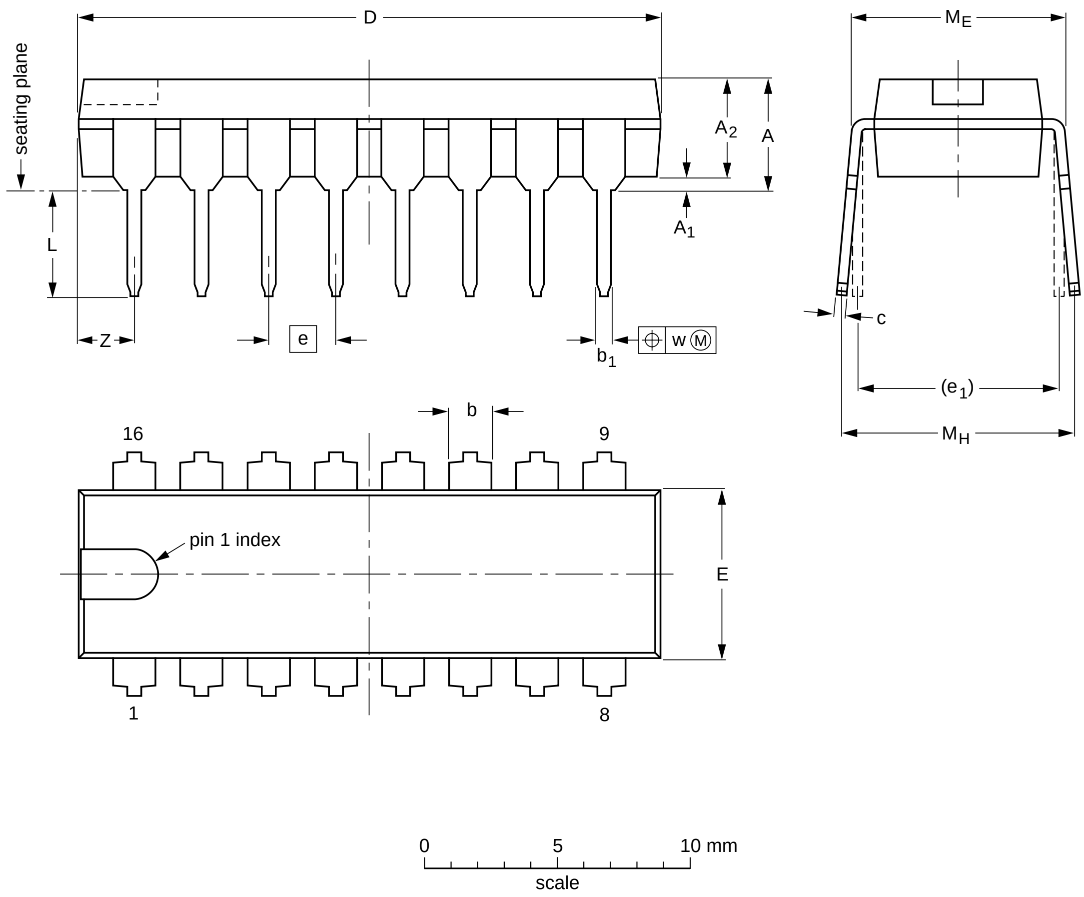


Fig.10 Application diagram.

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil); long body SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

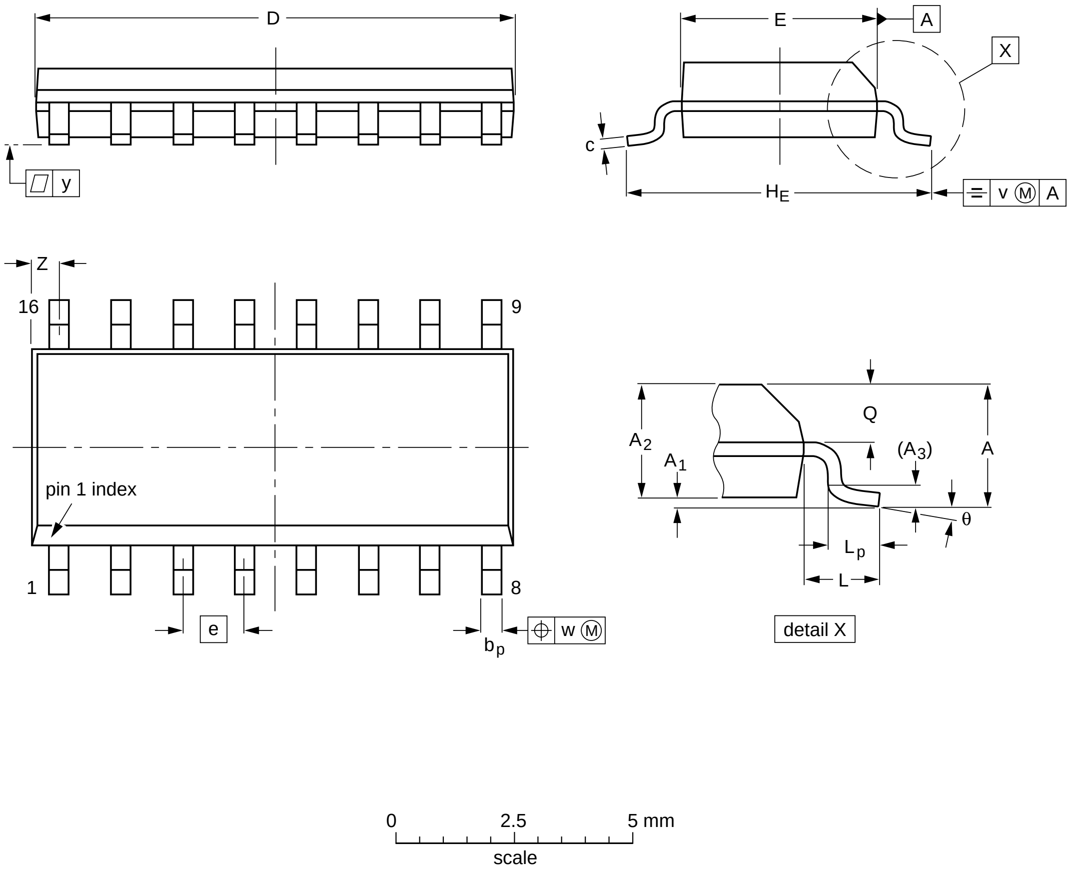
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D [(1)]	E [(1)]	e	e_1	L	M_E	M_H	w	Z [(1)] max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001	SC-503-16			~~95-01-19~~ 99-12-27

SO16: plastic small outline package; 16 leads; body width 3.9 mm; low stand-off height **SOT109-2**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.65	0.20 0.05	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.065	0.008 0.002	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-2	076E07	MS-012				~~97-05-22~~ 99-12-27

SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW[1]	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable[2]	–	suitable
Surface mount	BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable	–
	HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable[3]	suitable	–
	PLCC[4], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended[4][5]	suitable	–
	SSOP, TSSOP, VSO	not recommended[6]	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS[(1)]	PRODUCT STATUS[(2)]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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