Inv № 216

К1229КП1Р,КП1Н4/ К1229КП2Р,КП2Н4 (UC3714/UC3715)

Complementary Switch FET Drivers

February 2001- revised September 2002

DESCRIPTION

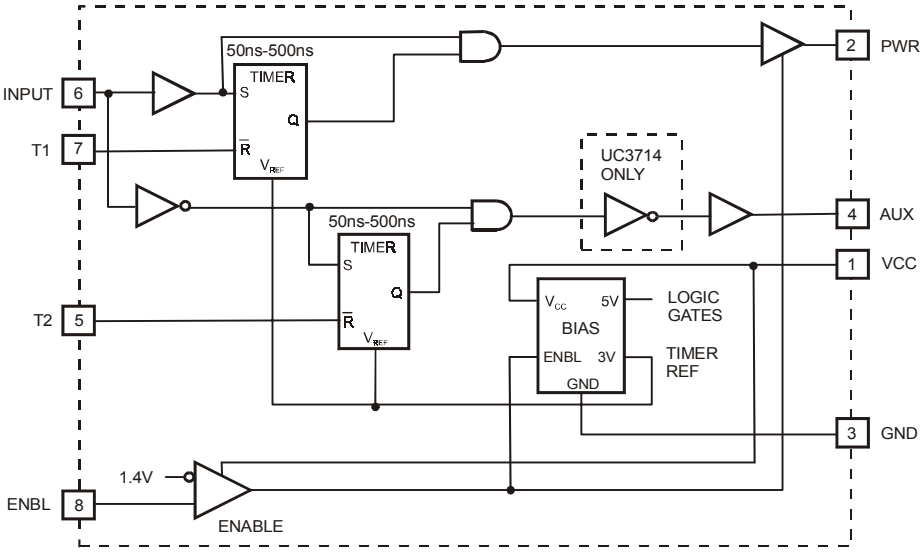
These two families of high speed drivers are designed to provide drive waveforms for complementary switches. Complementary switch configurations are commonly used in synchronous rectification circuits and active clamp/reset circuits, which can provide zero voltage switching. In order to facilitate the soft switching transitions, independently programmable delays between the two output waveforms are provided on these drivers. The delay pins also have true zero voltage sensing capability which allows immediate activation of the corresponding switch when zero voltage is applied. These devices require a PWM-type input to operate and can be interfaced with commonly available PWM controllers.
In the UC3714 series, the AUX output is inverted to allow driving a p-channel MOSFET. In the UC3715* series the two outputs are configured in a true complementary fashion.

* The UC3715 series are not produced yet.

FEATURES

- Single Input (PWM and TTL Compatible)
- High Current Power FET Driver, 1.0A Source/2A Sink
- Auxiliary Output FET Driver, 0.5A Source/1A Sink
- Time Delays Between Power and Auxiliary Outputs Independently Programmable from 50ns to 500 ns
- Time Delay or True Zero-Voltage Operation Independently Configurable for Each Output
- Switching Frequency to 1MHz
- Typical 50 ns Propagation Delays
- ENBL Pin Activates 220 μA Sleep Mode
- Power Output is Active Low in Sleep Mode
- Synchronous Rectifier Driver

BLOCK DIAGRAM



Note: Pin numbers refer to J, N and D packages

Absolute Maximum Ratings

Supply Voltage (low impedance source)	V_{CC}	20	V
Power Driver	I_{OH}		
continuous		-200	mA
peak		-1	A
Power Driver	I_{OL}		
continuous		400	mA
peak		2	A
Auxiliary Driver	I_{OH}		
continuous		-100	mA
peak		-500	mA
Auxiliary Driver	I_{OL}		
continuous		200	mA
peak		1	A
Input Voltage Range	INPUT, ENBL	-0.3 to 20	V
Storage Temperature Range		-65 to150	°C
Operating Junction Temperature (Note 1)		150	°C
Lead Temperature (Soldering 10 seconds)		300	°C

К1229КП1Р,КП1Н4/ К1229КП2Р,КП2Н4 (UC3714/UC3715)

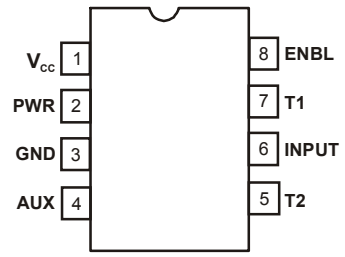
Complementary Switch FET Drivers

February 2001- revised September 2002

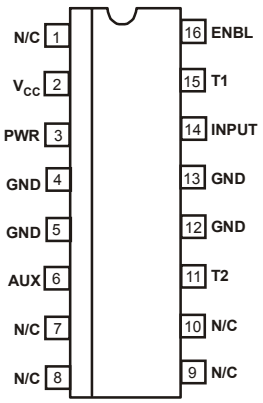
Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive info, negative out of, the specified terminals.
Note 2: Consult Peckaging Section of databook for thermal limitations and specifications of packages.

CONNECTION DIAGRAMS

DIL-8, SOIC-8 (Top View)
J or N, D Packages



SOIC-16 (Top View)
DP Packages



ELECTRICAL CHARACTERISTICS (V_{CC}=15V,ENBL ≥ 2V, R_T1=100kΩ from T1 to GND, R_T2=100kΩ from T2 to GND, and T_A=0°C to +70°C, for the UC3714/5, $T_A = T_J$ unless otherwise stated)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Units
Overall						
V_{CC}	V_{CC}		7		20	V
I_{CC}, nominal	I_{CC}	ENBL = 2.0V		18	24	mA
I_{CC}, sleep model	$I_{CC\ sleep}$	ENBL = 0.8V		200	300	µA
Power Driver (PWR)						
Pre Turn-on PWR Output, Low	V_{OL} Pre Turn-on	V_{CC} = 0V, I_{OUT} = 10mA, ENBL ® 0.8V		0.3	1.6	V
PWR Output Low, Sat. (V_{PWR})	V_{OL}	INPUT = 0.8V, I_{OUT} = 40 mA		0.3	0.8	V
		INPUT = 0.8V, I_{OUT} = 400 mA		2.1	2.8	
PWR Output High, Sat. (V_{CC} -V_{PWR})	V_{OH}	INPUT = 2.0V, I_{OUT} = -20 mA		2.1	3	
		INPUT = 2.0V, I_{OUT} = -200 mA		2.3	3	
Rise Time	Tr	C_L = 2200pF		30	60	ns
Fall Time	Tf	C_L = 2200pF		25	60	
T1 Delay, AUX to PWR	T1 delay	INPUT = rising edge, R_T1 = 10kΩ (Note 4)	20	35	80	
T1 Delay, AUX to PWR	T1 delay	INPUT = rising edge, R_T1 = 100kΩ (Note 4)	350	500	700	
PWR Prop Delay	Tpd	INPUT falling edge, 50% (Note 3)		35	100	
Auxiliary Driver (AUX)						
AUX Output Low, Sat (V_{AUX})	V_{OL}	V_{IN} = 2.0V, I_{OUT} = 20mA		0.3	0.8	V
		V_{IN} = 2.0V, I_{OUT} = 200mA		1.8	2.6	
AUX Output High, Sat (V_{CC} -V_{AUX})	V_{OH}	V_{IN} = 0.8V, I_{OUT} = -10mA		2.1	3.0	
		V_{IN} = 0.8V, I_{OUT} = -100mA		2.3	3.0	
Rise Time	Tr	C_L = 1000pF		45	60	ns
Fall Time	Tf	C_L = 1000pF		30	60	
T2 Delay, AUX to PWR	T2 delay	INPUT = rising edge, R_T2 = 10kΩ (Note 4)	20	50	80	
T2 Delay, AUX to PWR	T2 delay	INPUT = rising edge, R_T2 = 100kΩ (Note 4)	250	350	550	
AUX Prop Delay	Tpd	INPUT falling edge, 50% (Note 3)		35	80	
Enable (ENBL)						
Input Threshold	Vth		0.8	1.2	2.0	V
Input Current, I_{IH}	I_{IH}	ENBL = 15V		1	10	µA
Input Current, I_{IL}	I_{IL}	ENBL = 0V		-1	-10	µA

К1229КП1Р,КП1Н4/
К1229КП2Р,КП2Н4
(UC3714/UC3715)

Complementary Switch FET Drivers

February 2001- revised September 2002

Characteristics	Symbol	Test Condition	Min	Typ	Max	Units
T1						
Current Limit	I_{LIM}	T1 = 0V		-1.6	-2	mA
Nominal Voltage at T1	V_{T1}		2.7	3	3.3	V
Minimum T1 Delay	TdZVS	T1 = 2.5V (Note 4)		40	70	ns
T2						
Current Limit	I_{LIM}	T2 = 0V		-1.2	-2	mA
Nominal Voltage at T2	V_{T2}		2.7	3	3.3	V
Minimum T2 Delay	TdZVS	T2 = 2.5V (Note 4)		50	100	ns
Input (INPUT)						
Input Threshold	Vth		0.8	1.4	2.0	V
Input Current, I_{IH}	I_{IH}	INPUT = 15V		1	10	μA
Input Current, I_{IL}	I_{IL}	INPUT = 0V		-5	-20	μA

Note 3: Propagation delay times are measured from the 50% point of the input signal to the 10% point of the output signal's transition with no load on outputs.
Note 4: T1 delay is defined from the 50% point of the transition edge of AUX to the 10% of the rising edge of PWR. T2 delay is defined from the 90% of the falling edge of PWR to the 50% point of the transition edge of AUX.

PIN FUNCTION

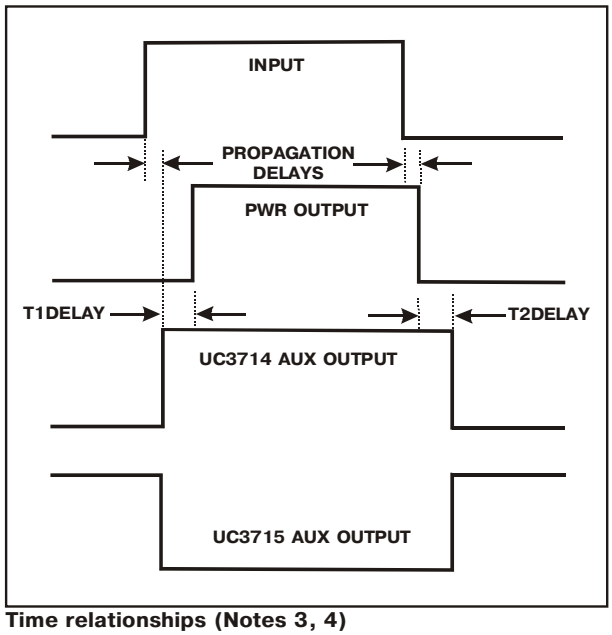
NAME	DESCRIPTION
AUX:	The AUX switches immediately at INPUT`s rising edge but waits through the T2 delay after input's falling edge before switching. AUX is capable of sourcing 0.5A and sinking 1.0A of drive current. See the Time Relationships diagram below for the difference between the UC3714 and UC3715 for INPUT, MAIN, and AUX. During sleep mode, AUX is inactive with a high impedance.
ENBL:	The ENBL input switches at TTL logic levels (approximately 1.2V), and its input range is from 0V to 20V. The ENBL input will place the device into sleep mode when it is a logical low. The current into Vcc during the sleep mode is typically 220μA.
GND:	This is the reference pin for all input voltages and the return point for all device currents. It carries the full peak sinking current from the outputs. Any tendency for the outputs to ring below GND voltage must be damped or clamped such that GND remains the most negative potential.
INPUT:	The input switches at TTL logic levels (approximately 1.4V) but the allowable range is from 0V to 20V, allowin gdirect connection to most common IC PWM controller outputs. The rising edge immediately switches the AU Xoutput, and initiates a timing delay, T1, before switching on the PWR output. Similarly, the INPUT falling edg e immediately turns off the PWR output and initiates a timing delay, T2, before switching the AUX output. It should be noted that if the input signal comes from a controller with FET drive capability, this signal provide sanother option. INPUT and PWR provide a delay only at the leading edge while INPUT and AUX provide the delay at the trailing edge.
PWR:	The PWR output waits for the T1 delay after the INPUT`s rising edge before switching on, but switches off immediately at INPUT`s falling edge (neglecting propagation delays). This output is capable of sourcing 1A and sinking 2A of peak gate drive current. PWR output includes a passive, self-biased circuit which holds this pin active low, when ENBL ≥ 0.8V regardless of VCC's voltage.
T1:	A resistor to ground programs the time delay between AUX switch turn-off and PWR turn-on.
T2:	This pin functions in the same way as T1 but controls the time delay between PWR turn-off and activation of the AUX switch.
T1, T2:	The resistor on each of these pins sets the charging current on internal timing capacitors to provide independent time control. The nominal voltage level at each pin is 3V and the current is internally limited to 1mA. The total delay from INPUT to each output includes a propagation delay in addition to the programmabl etimer but since the propagation delays are approximately equal, the relative time delay between the two outputs can be assumed to be solely a function of the programmed delays. The relationship of the time delay vs. RT is shown in the Typical Characteristics curves. Either or both pins can alternatively be used for voltage sensing in lieu of delay programming. This is done by pulling the timer pins below their nominal voltage level which immediately activates the timer output.
V_{CC}:	The Vcc input range is from 7V to 20V. This pin should be bypassed with a capacitor to GND consistent with peak load current demands.

К1229КП1Р,КП1Н4/
К1229КП2Р,КП2Н4
(UC3714/UC3715)

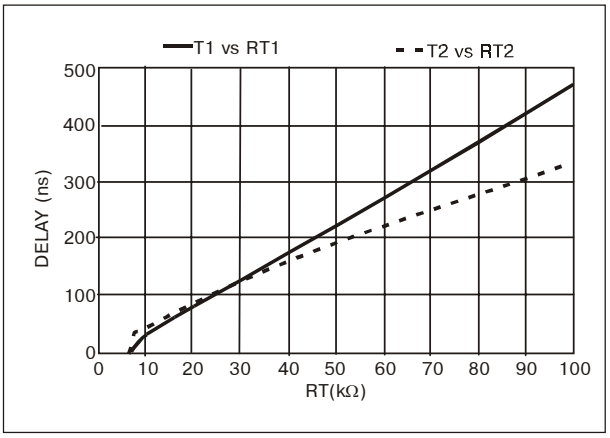
Complementary Switch FET Drivers

February 2001- revised September 2002

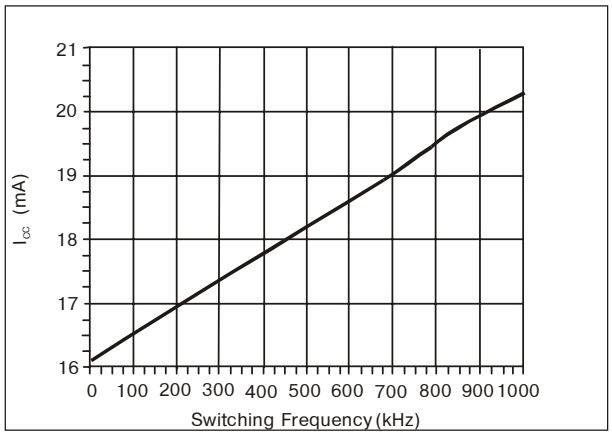
TYPICAL CHARACTERISTICS



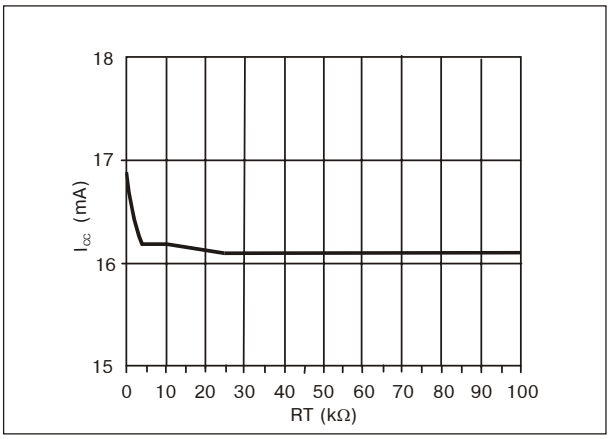
Time relationships (Notes 3, 4)



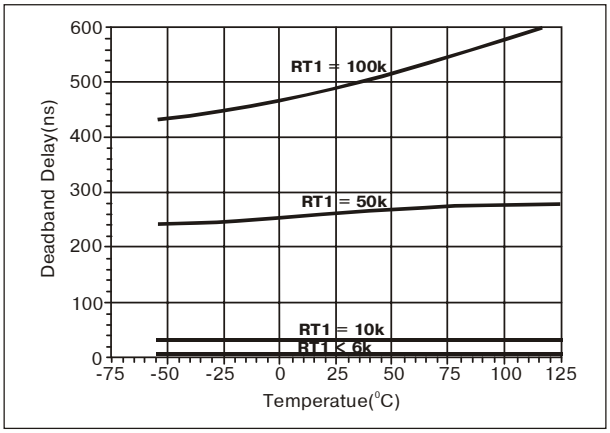
T1 Delay, T2 Delay vs. RT



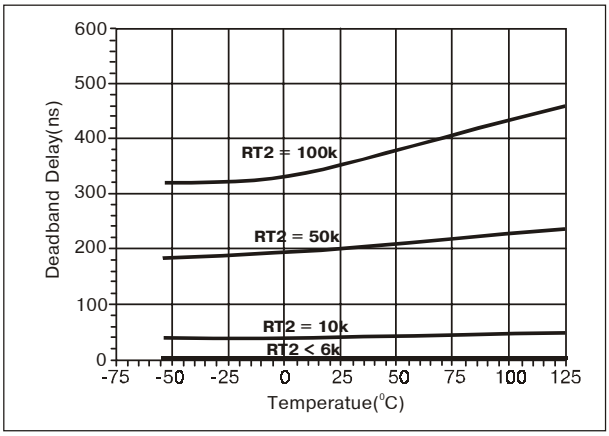
I_{cc} vs Switching Frequency with No Load and 50% Duty Cycle $R_T1 = R_T2 = 50k$



I_{cc} vs R_T with Opposite R_T = 50k



T1 Deadband vs. Temperature AUX to PWR



T2 Deadband vs. Temperature AUX to PWR

К1229КП1Р,КП1Н4/
К1229КП2Р,КП2Н4
(UC3714/UC3715)

Complementary Switch FET Drivers

February 2001- revised September 2002

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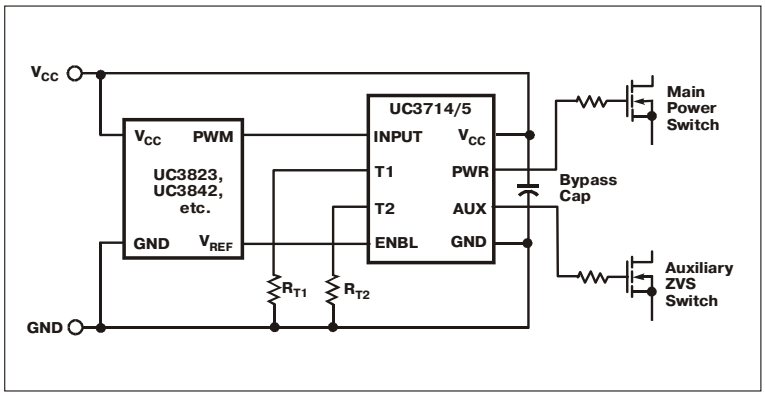


Figure 1. Typical application with timed delays

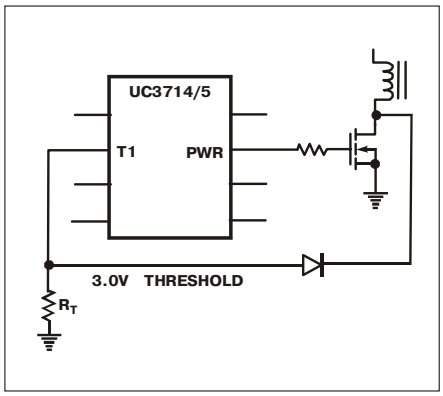


Figure 2. Using the timer input for zero-voltage sensing

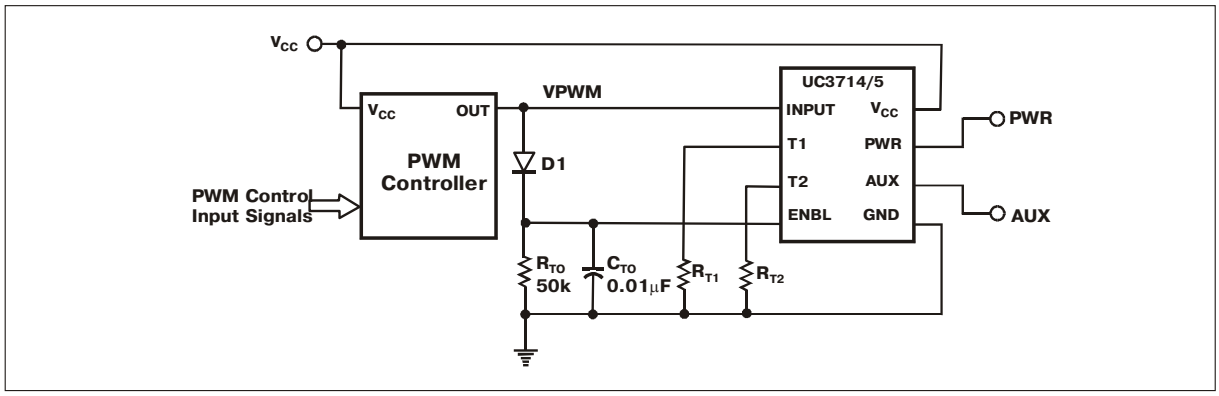


Figure 3. Self-actuated sleep mode with the absence of an input PWM signal. Wake up occurs with the first pulse while turn-off is determined by the (RTO CTO) time constant.

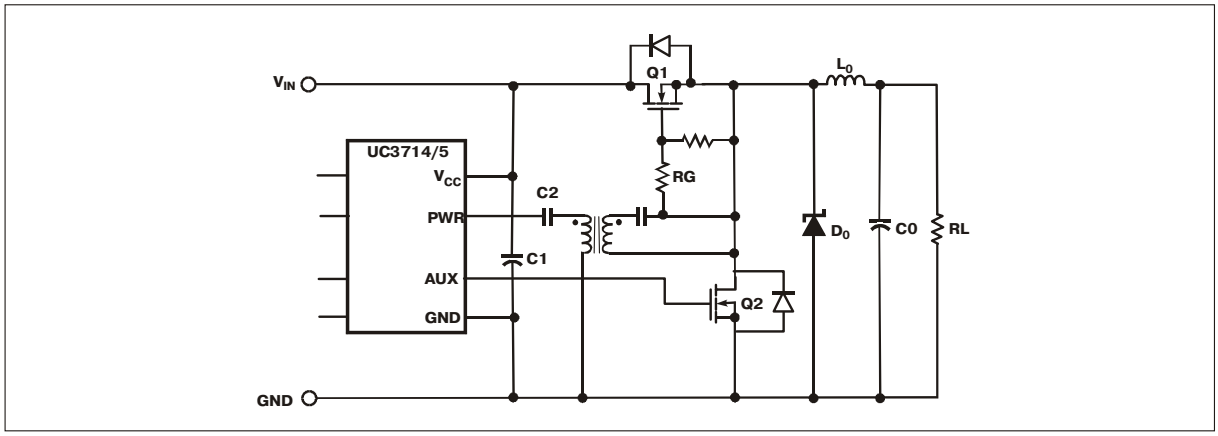


Figure 4. Using the UC3715 as a complementary synchronous rectifier switch driver with n-channel FETs

TYPICAL CHARACTERISTICS

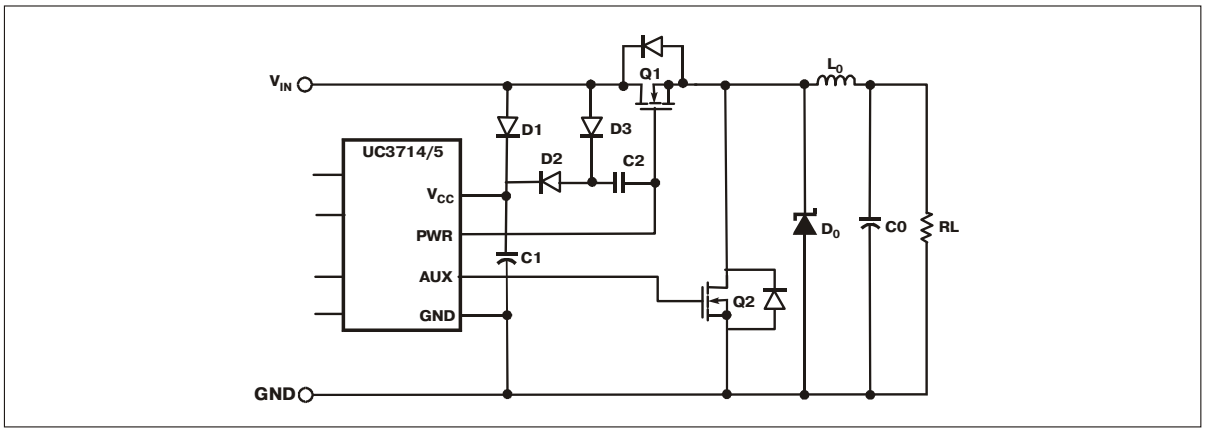


Figure 5. Synchronous rectifier application with a charge pump to drive the high-side n-channel buck switch. V_{IN} is limited to 10V as V_{CC} will rise to approximately $2V_{IN}$.

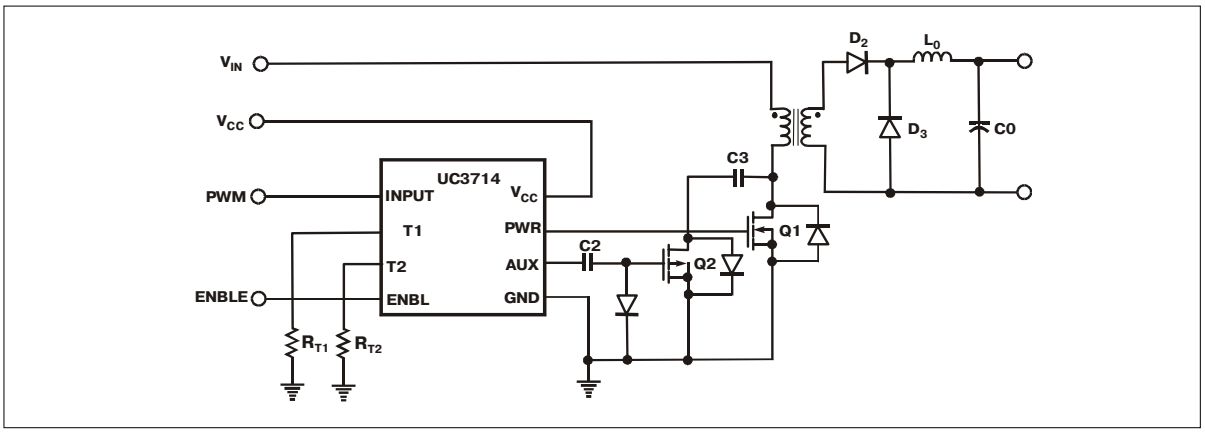


Figure 6. Typical forward converter topology with active reset provided by the UC3714 driving an N-channel switch (Q1) and a P-channel auxiliary switch (Q2).

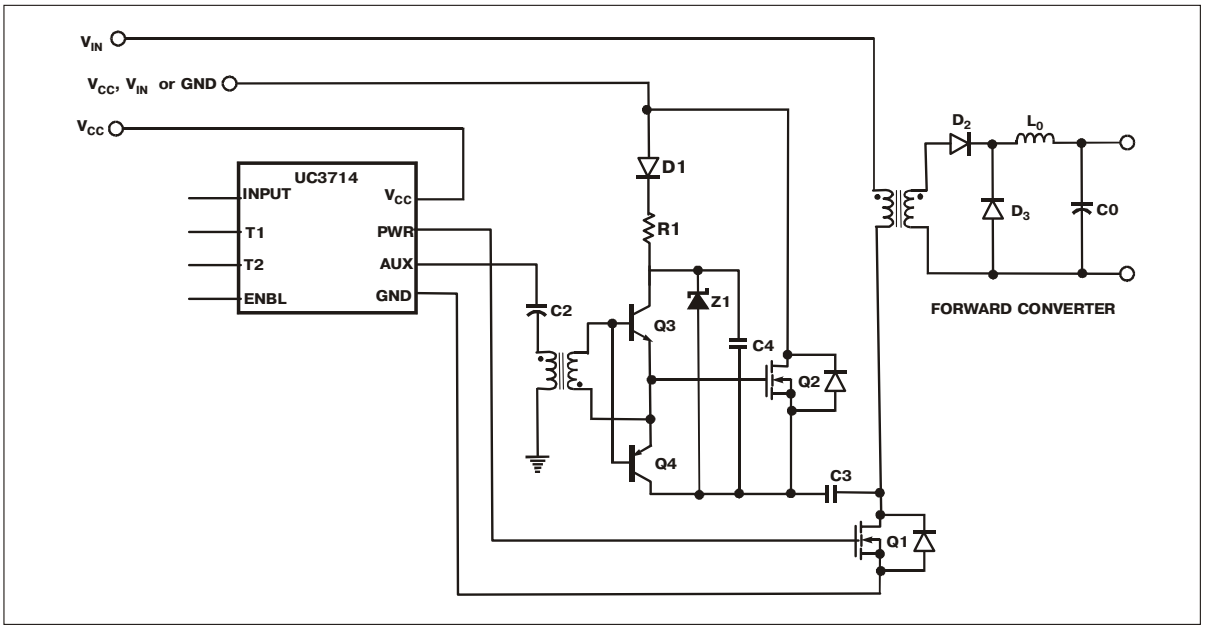


Figure 7. Using an N-channel active reset switch with a floating drive command.

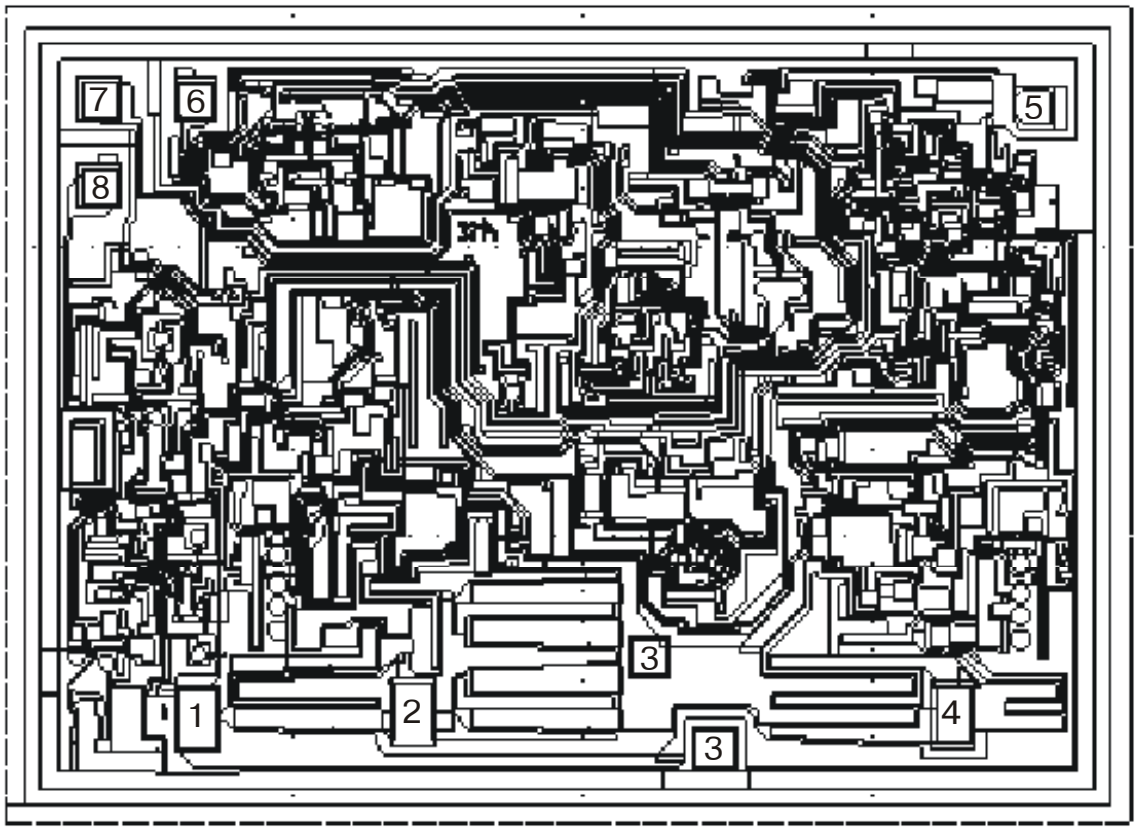
Inv № 216

К1229КП1Р,КП1Н4/
К1229КП2Р,КП2Н4
(UC3714/UC3715)

Complementary Switch FET Drivers

February 2001- revised September 2002

PAD LOCATION UC3714



Chip size: 2.92mm x 2.12 mm

PAD LOCATION COORDINATES
(The Center of Pads)

Pad N	Coordinates μm	
	X	Y
1	499	270
2	1059	292,5
3	1669,5	432
3	1842	195
4	2460	284
5	2670,5	1861,5
6	495	1881,5
7	245	1881,5
8	245	1656,5