Switch-Mode LED Driver IC with High Current Accuracy

Features

- Switch mode controller for single switch drivers
  - Buck
  - Boost
  - Buck-boost
  - SEPIC
- Works with high side current sensing
- Closed loop control of output current
- High PWM dimming ratio
- Internal 250V linear regulator (can be extended using external Zener diodes)
- Internal 2% voltage reference ($0°C < T_A < 85°C$)
- Constant frequency or constant off-time operation
- Programmable slope compensation
- Enable & PWM dimming
- +0.2A/-0.4A GATE drive
- Output short circuit protection
- Output over voltage protection
- Synchronization capability
- Programmable MOSFET current limit

Applications

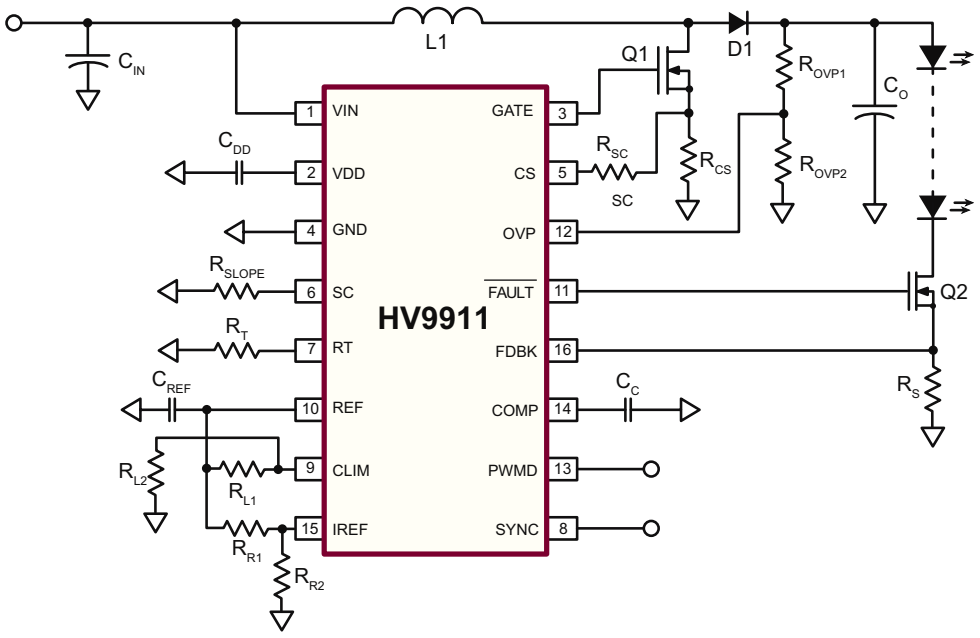
- RGB backlight applications
- Battery powered LED lamps
- Other DC/DC LED drivers

General Description

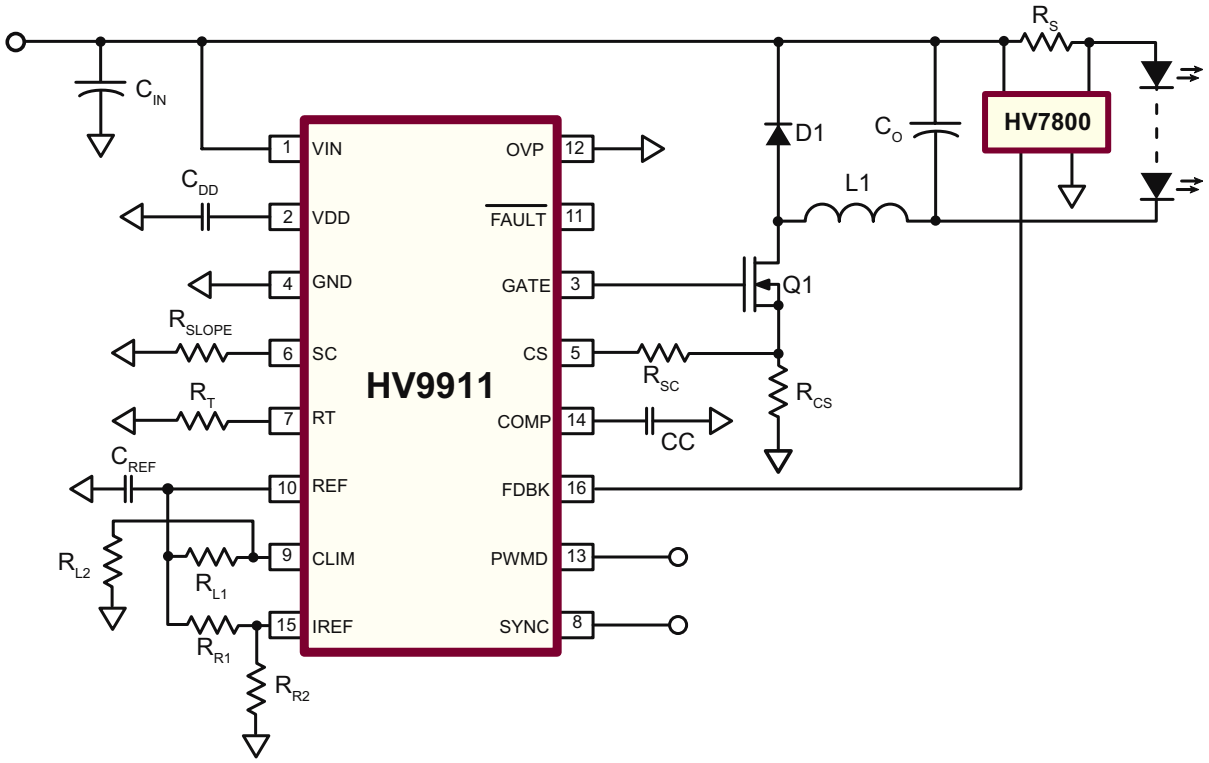
The HV9911 is a current mode control LED driver IC designed to control single switch PWM converters (buck, boost, buck-boost, or SEPIC), in a constant frequency or constant off-time mode. The controller uses a peak current control scheme, (with programmable slope compensation), and includes an internal transconductance amplifier to control the output current in closed loop, enabling high output current accuracy. In the constant frequency mode, multiple HV9911s can be synchronized to each other, or to an external clock, using the SYNC pin. Programmable MOSFET current limit enables current limiting during input under voltage and output overload conditions. The IC also includes a 0.2A source and 0.4A sink GATE driver for high power applications. An internal 9.0 - 250V linear regulator powers the IC, eliminating the need for a separate power supply for the IC. HV9911 provides a TTL compatible, PWM dimming input that can accept an external control signal with a duty ratio of 0-100% and a frequency of up to a few kilohertz. The IC also provides a $\overline{\text{FAULT}}$ output which, can be used to disconnect the LEDs in case of a fault condition, using an external disconnect FET.

The HV9911 based LED driver is ideal for RGB backlight applications with DC inputs. The HV9911 based LED lamp drivers can achieve efficiency in excess of 90% for buck and boost applications.

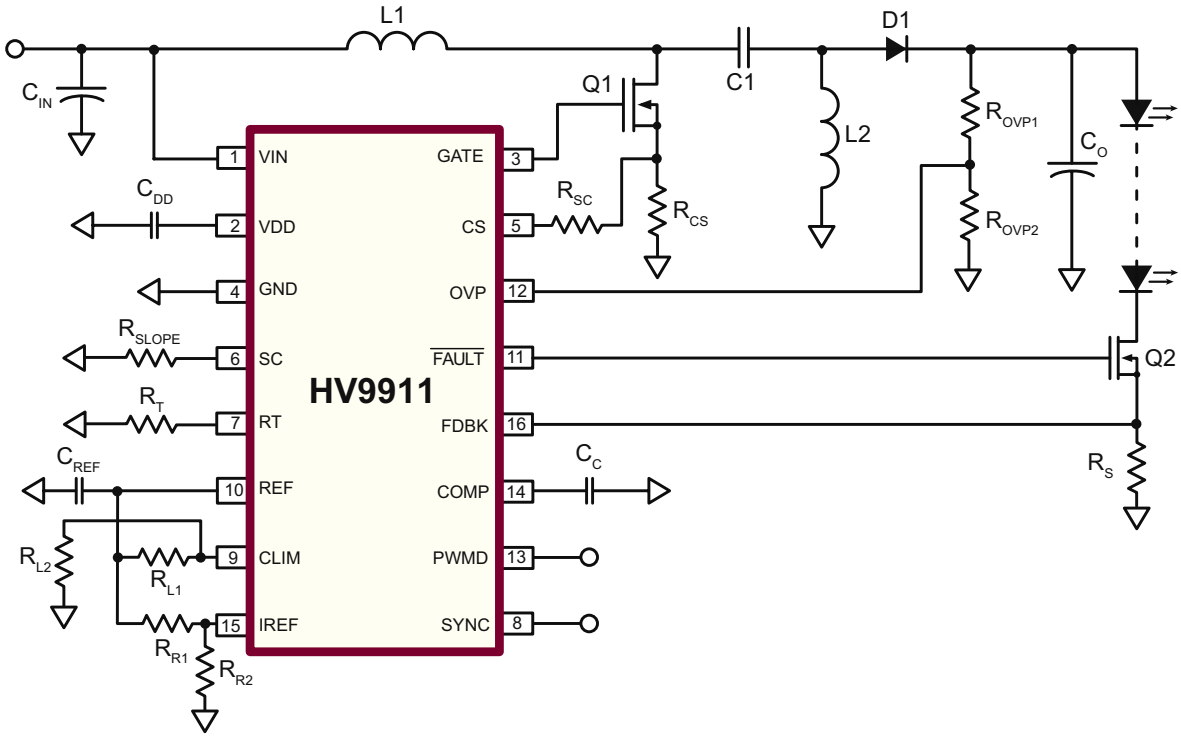
Typical Application Circuit - Boost



Typical Application Circuit - Buck



Typical Application Circuit - SEPIC



Ordering Information

Device	Package Options
	16-Lead SOIC
HV9911	HV9911NG-G

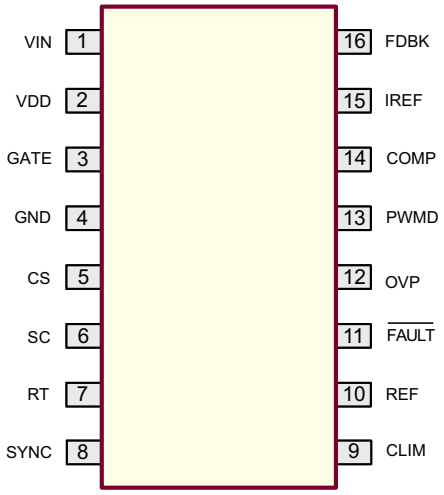
-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
V_{IN} to GND	-0.5V to +250V
V_{DD} to GND	-0.3V to +13.5V
CS1, CS2 to GND	-0.3V to (V_{DD} + 0.3V)
PWMD to GND	-0.3V to (V_{DD} + 0.3V)
GATE to GND	-0.3V to (V_{DD} + 0.3V)
All other pins to GND	-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +25°C)	
(derate 10.0mW/°C above +25°C)	1000mW
Junction to ambient thermal impedance	82°C/W
Operating ambient temperature range	-40°C to +85°C
Junction temperature	+125°C
Storage temperature range	-65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

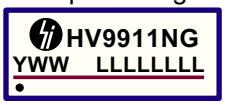
Pin Configuration



16-Lead SOIC (NG)
(top view)

Product Marking

Top Marking



Bottom Marking

Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin
A = Assembler ID*
____ = "Green" Packaging
**May be part of top marking*

Package may or may not include the following marks: Si or

16-Lead SOIC (NG)

Electrical Characteristics

(The specifications are at T_A = 25°C and V_{IN} = 24V, unless otherwise noted.)

Sym	Parameter			Min	Typ	Max	Units	Conditions
Input								
V_{INDC}	Input DC supply voltage range	*	-	(1)	-	250	V	DC input voltage
I_{INSD}	Shut-down mode supply current	*	-	-	1.0	1.5	mA	PWMD connected to GND, V_{IN} = 24V
Internal Regulator								
V_{DD}	Internally regulated voltage	*	-	7.25	7.75	8.25	V	V_{IN} = 9.0 - 250V, $I_{DD(ext)}$ = 0, PWMD connected to GND
UVLO	V_{DD} undervoltage lockout threshold	-	-	6.65	6.90	7.20	V	V_{DD} rising
ΔUVLO	V_{DD} undervoltage lockout hysteresis	-	-	-	500	-	mV	---
$V_{DD(ext)}$	Steady state external voltage that can be applied at the V_{DD} pin(2)	-	-	-	-	12	V	---

Notes:

* *Denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +85°C.*

1. *See application section for minimum input voltage.*
2. *Parameters are not guaranteed to be within specifications if the external V_{DD} voltage is greater than $V_{DD(ext)}$ or if V_{DD} < 7.25V.*

Electrical Characteristics *(cont.)*

(The specifications are at T_A = 25°C and V_{IN} = 24V, unless otherwise noted.)

Sym	Parameter			Min	Typ	Max	Units	Conditions
Reference								
V_{REF}	REF pin voltage (0°C < T_A < 25°C)	-	-	1.225	1.25	1.275	V	REF bypassed with a 0.1µF capacitor to GND; I_{REF} = 0; V_{DD} = 7.75V; PWMD = GND
	REF pin voltage (-40°C < T_A < 85°C)	-	-	1.225	1.25	1.275		
$V_{REFLINE}$	Line regulation of reference voltage	-	-	0	-	20	mV	REF bypassed with a 0.1µF capacitor to GND; I_{REF} = 0; V_{DD} = 7.25 - 12V; PWMD = GND
$V_{REFLOAD}$	Load regulation of reference voltage	-	-	0	-	10	mV	REF bypassed with a 0.1µF capacitor to GND; I_{REF} = 0-500µ; PWMD = GND
PWM Dimming								
$V_{PWMD(lo)}$	PWMD input low voltage	*	-	-	-	0.80	V	V_{DD} = 7.25V - 12V
$V_{PWMD(hi)}$	PWMD input high voltage	*	-	2.0	-	-	V	V_{DD} = 7.25V - 12V
R_{PWMD}	PWMD pull-down resistance	-	-	50	100	150	kΩ	V_{PWMD} = 5.0V
GATE								
I_{SOURCE}	GATE short circuit current	-	-	0.2	-	-	A	V_{GATE} = 0V; V_{DD} = 7.75V
I_{SINK}	GATE sinking current	-	-	0.4	-	-	A	V_{GATE} = 7.75V ; V_{DD} = 7.75V
T_{RISE}	GATE output rise time	-	-	-	50	85	ns	C_{GATE} = 1nF; V_{DD} = 7.75V
T_{FALL}	GATE output fall time	-	-	-	25	45	ns	C_{GATE} = 1nF; V_{DD} = 7.75V
Over Voltage Protection								
V_{OVP}	IC shut down voltage	*	-	1.215	1.25	1.285	V	V_{DD} = 7.25 - 12V ; OVP rising
Current Sense								
T_{BLANK}	Leading edge blanking	-	-	100	-	375	ns	---
T_{DELAY1}	Delay to output of COMP comparator	-	-	-	-	180	ns	COMP = V_{DD}; C_{LIM} = REF; V_{CS} = 0 to 600mV step
T_{DELAY2}	Delay to output of C_{LIMIT} comparator	-	-	-	-	180	ns	COMP = V_{DD} ; C_{LIM} = 300mV; V_{CS} = 0 to 400mV step
V_{OFFSET}	Comparator offset voltage	-	-	-10	-	10	mV	---
Internal Transconductance Opamp								
GB	Gain bandwidth product	-	#	-	1.0	-	MHz	75pF capacitance at COMP pin
A_V	Open loop DC gain	-	-	66	-	-	dB	Output Open
V_{CM}	Input common-mode range	-	#	-0.3	-	3.0	V	---
V_O	Output voltage range	-	#	0.7	-	6.75	-	V_{DD} = 7.75V
g_m	Transconductance	-	-	340	435	530	µA/V	---
V_{OFFSET}	Input offset voltage	-	-	-2.0	-	4.0	mV	---
I_{BIAS}	Input bias current	-	#	-	0.5	1.0	nA	---

Notes:

* *Denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +85°C.*

\# *Denotes guaranteed by design.*

Electrical Characteristics *(cont.)*

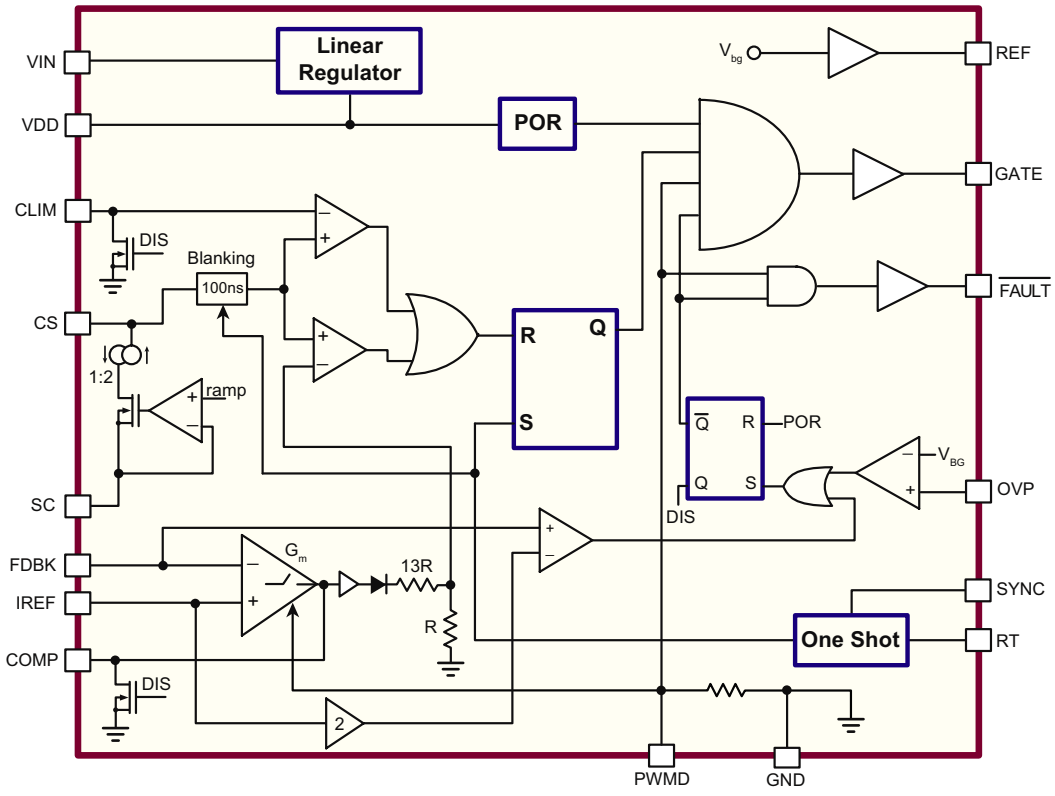
(The specifications are at T_A = 25°C and V_{IN} = 24V, unless otherwise noted.)

Sym	Parameter			Min	Typ	Max	Units	Conditions
Oscillator								
f_{OSC1}	Oscillator frequency	*	-	88	100	112	kHz	R_T = 909kΩ
f_{OSC2}	Oscillator frequency	*	-	308	350	392	kHz	R_T = 261kΩ
D_{MAX}	Maximum duty cycle	-	-	-	90	-	%	---
$I_{OUTSYNC}$	Sync output current	-	-	-	10	20	µA	---
I_{INSYNC}	Sync input current	-	-	0	-	200	µA	V_{SYNC} < 0.1V
Output Short Circuit								
T_{OFF}	Propagation time for short circuit detection	-	-	-	-	250	ns	I_{REF} = 200mV; FDBK = 450mV; $\overline{FAULT}$ goes from high to low
$T_{RISE,FAULT}$	Fault output rise time	-	-	-	-	300	ns	1.0nF capacitor at $\overline{FAULT}$ pin
$T_{FALL,FAULT}$	Fault output fall time	-	-	-	-	200	ns	1.0nF capacitor at $\overline{FAULT}$ pin
G_{FAULT}	Amplifier gain at IREF pin	-	-	1.8	2	2.2		I_{REF} = 200mV
Slope Compensation								
I_{SLOPE}	Current sourced out of SC pin	-	-	0	-	100	µA	---
G_{SLOPE}	Internal current mirror ratio	-	-	1.8	2	2.2	-	I_{SLOPE} = 50µA; RC_{SENSE} = 1.0kΩ

Notes:

* *Denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +85°C.*

Functional Block Diagram



Functional Description

Power Topology

The built in linear regulator of the HV9911 can operate up to 250V at the VIN pin. The linear regulator provides an internally regulated voltage of 7.75V (typ) at VDD if the input voltage is in the range of 9.0 – 250V. This voltage is used to power the IC and also provide the power to external circuits connected at the VDD and VREF pins. This linear regulator can be turned off by overdriving the VDD pin using an external boostrap circuit at voltages higher than 8.25V (up to 12V).

In practice, the input voltage range of the IC is limited by the current drawn by the IC. Thus, it becomes important to determine the current drawn by the IC to find out the maximum and minimum operating voltages at the VIN pin. The main component of the current drawn by the IC is the current drawn by the switching FET driver at the GATE pin. To estimate this current, we need to know a few parameters of the FET being used in the design and the switching frequency.

The typical waveform of the current being sourced out of GATE is shown in Fig. 1. Fig. 2 shows the equivalent circuit of the GATE driver and the external FET. The values of V_{DD} and R_{GATE} for the HV9911 are 7.75V and 40Ω respectively.
Note: The equations given below are approximations and are to be used only for estimation purposes. The actual values will differ somewhat from the computed values.

Consider the case when the external FET is FDS3692 and the switching frequency is f_S = 200kHz with an LED string voltage V_O = 80V. From the datasheet of the FET, the following parameters can be determined:

C_{ISS} = 746pF
$C_{GD} = C_{RSS}$ = 27pF
$C_{GS} = C_{ISS} - C_{GD}$ = 719pF
V_{TH} = 3.0V

Fig. 1. Current Sourced Out of GATE at FET Turn-on Driver

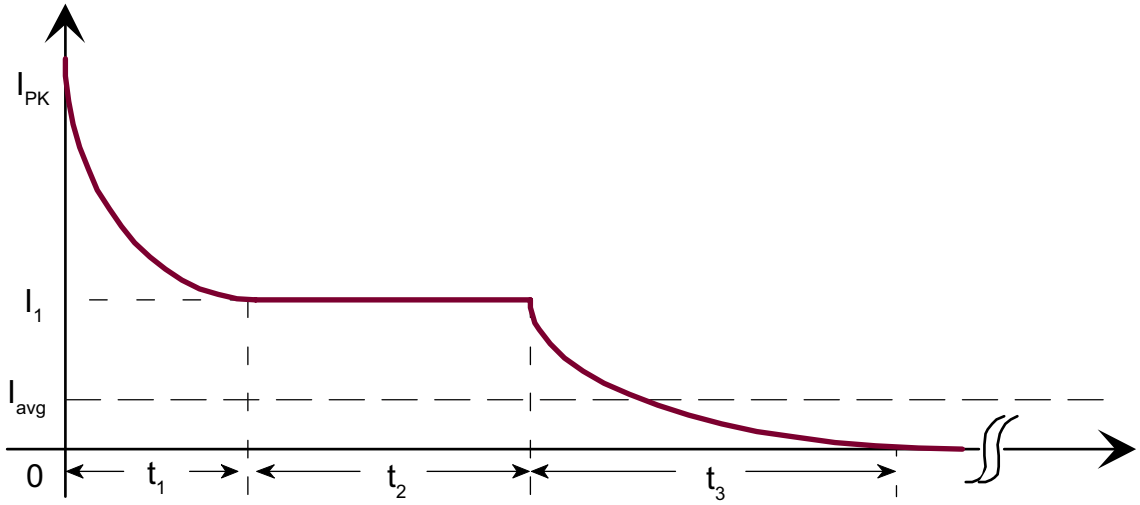
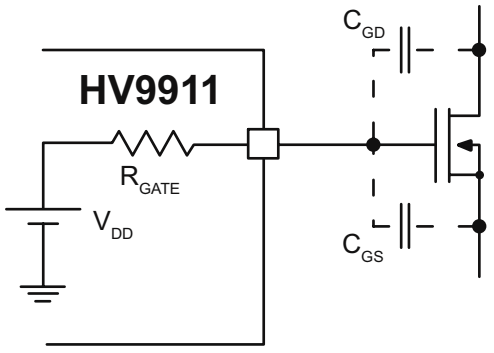


Fig. 2. Equivalent Circuit of the GATE Driver



When the external FET is being turned on, current is being sourced out of the GATE and that current is being drawn from the input. Thus, the average current drawn from V_{DD} (and thus from V_{IN}) needs to be computed. Without going into the details of the FET operation, the various values in the graph of Fig. 1 can be computed as follows:

Parameter	Formula		Value (for given example)
I_{PK}	V_{DD} / R_{GATE}		193.75mA
I_1	$(V_{DD} - V_{TH}) / R_{GATE}$		118.75mA
t_1	$-R_{GATE} \cdot C_{ISS} \cdot \ln (I_1 / I_{PK})$		14.61ns
t_2	$[(V_O - V_{TH}) \cdot C_{GD}] / I_1$ $[(V_{IN} - V_{TH}) \cdot C_{GD}] / I_1$	(for a boost converter) (for a buck converter)	17.5ns
t_3	$2.3 \cdot R_{GATE} \cdot C_{GS}$		66ns
I_{avg}	$[I_1 \cdot (t_1 + t_2) + 0.5 \cdot (I_{PK} - I_1) \cdot t_1 + 0.5 \cdot I_1 \cdot t_3] \cdot f_S$		1.66mA

The total current being drawn from the linear regulator for a typical HV9911 circuit can be computed as follows (the values provided are based on the continuous conduction mode boost design in the application note - AN-H55).

Current	Formula	Typical Value
Quiescent Current	1000µA	1000µA
Current sourced out of REF pin	$(V_{REF} / R_{L1} + R_{L2}) + (V_{REF} / R_{R1} + R_{R2})$	100µA
Current sourced out of RT pin	$6_V / R_T$	13.25µA
Current sourced out of SC pin	$(1 / 2) \cdot (2.5V / R_{SLOPE})$	30.8µA
Current sourced out of CS pin	$2.5V / R_{SLOPE}$	61.6µA
Current drawn by FET GATE driver	I_{AVG}	1660µA
Total Current drawn from the linear regulator		***2.865mA***

Note:

For a discontinuous mode converter, the currents sourced out of the SC and CS pin will be zero.

Maximum Input Voltage at VIN pin computed using the Power Dissipation Limit

The maximum input voltage that the HV9911 can withstand without damage if the regulator is drawing about 2.8mA will depend on the ambient temperature. If we consider an ambient temperature of 40°C, the power dissipation in the package cannot exceed:

$$P_{MAX} = 1000mW - 10mW \bullet (40^{O}C - 25^{O}C)$$
$$= 850mW$$

The above equation is based on package power dissipation limits as given in the Absolute Maximum Limits section of this datasheet.

To dissipate a maximum power of 850mW in the package, the maximum input voltage cannot exceed:

$$V_{INMAX} = P_{MAX} / I_{TOTAL}$$
$$= 296V$$

Since the maximum voltage is far greater than the actual input voltage (24V), power dissipation will not be a problem for this design.

For this design, at 24V input, the increase in the junction temperature of the IC (over the ambient) will be

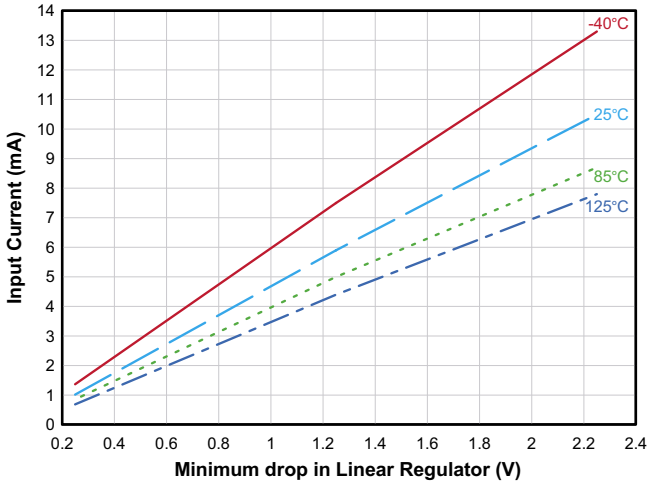
$$\Delta\theta = V_{IN} \bullet I_{TOTAL} \bullet \theta_{ja}$$
$$= 5.64^{O}C$$

where θ_{ja} is the junction to ambient thermal impedance of the 16-Lead SOIC package of the HV9911.

Minimum Input Voltage at VIN pin

The minimum input voltage at which the converter will start and stop depends on the minimum voltage drop required for the linear regulator. The internal linear regulator will regulate the voltage at the VDD pin when V_{IN} is between 9.0 and 250V. However, when V_{IN} is less than 9.0V, the converter will still function as long as V_{DD} is greater than the under voltage lockout. Thus, the converter might be able to start at input voltages lower than 9.0V. The start/stop voltages at the VIN pin can be determined using the minimum voltage drop across the linear regulator as a function of the current drawn. This data is shown in Fig. 3 for different junction temperatures.

Fig. 3. Graph of the Input Current vs Minimum Voltage Drop Across Linear Regulator for Different Junction Temperatures



Assume a maximum junction temperature of 85°C (this give a reasonable temperature rise of 45°C at an ambient temperature of 40°C). At 2.86mA input current, the minimum voltage drop from Fig. 3 can be approximately estimated to be V_{DROP} = 0.75V. However, before the IC starts switching the current drawn will be the total current minus the GATE drive current. In this case, that current is I_{Q_TOTAL} = 1.2mA. At this current level, the voltage drop is approximately V_{DROP1} = 0.4V. Thus, the start/stop V_{IN} voltages can be computed to be:

$$VIN_{START} = UVLO_{MAX} + V_{DROP1}$$
$$= 7.2V + 0.4V$$
$$= 7.60V$$

$$VIN_{STOP} = UVLO_{MAX} - 0.5V + V_{DROP}$$
$$= 7.2V - 0.5V + 0.75V$$
$$= 7.45V$$

Note:

In some cases, if the GATE drive draws too much current, VIN_{START} might be less than VIN_{STOP}. In such cases, the control IC will oscillate between ON and OFF if the input voltage is between the start and stop voltages. In these circumstances, it is recommended that the input voltage be kept higher than VIN_{STOP}.

Reference

HV9911 includes a 2% accurate, 1.25V reference, which can be used as the reference for the output current as well as to set the switch current limit. This reference is also used internally to set the over voltage protection threshold. The reference is buffered so that it can deliver a maximum of 500µA external current to drive the external circuitry. The reference should be bypassed with at least a 10nF low ESR capacitor.

Note:

In order to avoid abnormal startup conditions, the bypass capacitor at the REF pin should not exceed 0.22µF.

Oscillator

The oscillator can be set in two ways. Connecting the oscillator resistor between the RT and GATE pins will program the off-time. Connecting the resistor between RT and GND will program the time period.

In both cases, resistor R_T sets the current, which charges an internal oscillator capacitor. The capacitor voltage ramps up linearly and when the voltage increases beyond the internal set voltage, a comparator triggers the SET input of the internal SR flip-flop. This starts the next switching cycle. The time period of the oscillator can be computed as:

$$T_S \approx R_T \bullet 11pF$$

Slope Compensation

For converters operating in the constant frequency mode, slope compensation becomes necessary to ensure stability of the peak current mode controller, if the operating duty cycle is greater than 0.5. Choosing a slope compensation which is one half of the down slope of the inductor current ensures that the converter will be stable for all duty cycles.

Slope compensation can be programmed by two resistors R_{SLOPE} and R_{SC}. Assuming a down slope of DS (A/µs) for the inductor current, the slope compensation resistors can be computed as:

$$R_{SLOPE} = (10 \bullet R_{SC}) / (DS \bullet 10^6 \bullet T_S \bullet R_{CS})$$

A typical value for R_{SC} is 499Ω.

Note:

The maximum current that can be sourced out of the SC pin is 100µA. This limits the minimum value of the R_{SLOPE} resistor to 25kΩ. If the equation for slope compensation produces a value of R_{SLOPE} less than this value, then R_{SC} would have to be increased accordingly. It is recommended that R_{SLOPE} be chosen in the range of 25 - 50kΩ.

Current Sense

The current sense input of the HV9911 includes a built in 100ns (minimum) blanking time to prevent spurious turn off due to the initial current spike when the FET turns on.

The HV9911 includes two high-speed comparators - one is used during normal operation and the other is used to limit the maximum input current during input under voltage or overload conditions.

The IC includes an internal resistor divider network, which steps down the voltage at the COMP pin by a factor of 15. This stepped-down voltage is given to one of the comparators as the current reference. The reference to the other comparator, which acts to limit the maximum inductor current, is given externally.

It is recommended that the sense resistor R_{CS} be chosen so as to provide about 250mV current sense signal.

Current Limit

Current limit has to be set by a resistor divider from the 1.25V reference available on the IC. Assuming a maximum operating inductor current I_{pk} (including the ripple current), the voltage at the CLIM pin can be set as:

$$V_{CLIM} \geq 1.2 \bullet I_{PK} \bullet R_{CS} + (5 \bullet R_{SC} / R_{SLOPE}) \bullet 0.9$$

Note that this equation assumes a current limit at 120% of the maximum input current. Also, if V_{CLIM} is greater than 450mV, the saturation of the internal opamp will determine the limit on the input current rather than the CLIM pin. In such a case, the sense resistor R_{CS} should be reduced till V_{CLIM} reduces below 450mV.

It is recommended that no capacitor be connected between CLIM and GND.

Fault Protection

The HV9911 has built-in output over-voltage protection and output short circuit protection. Both protection features are latched, which means that the power to the IC must be recycled to reset the IC. The IC also includes a $\overline{\text{FAULT}}$ pin which goes low during any fault condition. At startup, a monoshot circuit, (triggered by the POR circuit), resets an internal flip-flop which causes $\overline{\text{FAULT}}$ to go high, and remains high during normal operation. This also allows the GATE drive to function normally. This pin can be used to drive an external disconnect switch (Q2 in the Typical Boost Application Circuit on pg.1), which will disconnect the load during a fault condition. This disconnect switch is very important in a boost converter, as turning off the switching

FET (Q_1) during an output short circuit condition will not remove the fault (Q_1 is not in the path of the fault current). The disconnect switch will help to disconnect the shorted load from the input.

Over Voltage Protection

Over voltage protection is achieved by connecting the output voltage to the OVP pin through a resistive divider. The voltage at the OVP pin is constantly compared to the internal 1.25V. When the voltage at this pin exceeds 1.25V, the IC is turned off and $\overline{\text{FAULT}}$ goes low.

Output Short Circuit Protection

The output short circuit condition is indicated by $\overline{\text{FAULT}}$. At startup, a monoshot circuit, (triggered by the POR circuit), resets an internal flip-flop, which causes $\overline{\text{FAULT}}$ to go high, and remains high during normal operation. This also allows the GATE drive to function normally.

The steady state current is reflected in the reference voltage connected to the transconductance amplifier. The instantaneous output current is sensed from the FDBK terminal of the amplifier. The short circuit threshold current is internally set to 200% of the steady state current.

During short circuit condition, when the current exceeds the internally set threshold, the SR flip-flop is set and $\overline{\text{FAULT}}$ goes low. At the same time, the GATE driver of the power FET is inhibited, providing a latching protection. The system can be reset by cycling the input voltage to the IC.

Note:

The short circuit FET should be connected before the current sense resistor as reversing R_S and Q_2 will affect the accuracy of the output current (due to the additional voltage drop across Q_2 which will be sensed).

Synchronization

The SYNC pin is an input/output (I/O) port to a fault tolerant peer-to-peer and/or master clock synchronization circuit. For synchronization, the SYNC pins of multiple HV9911 based converters can be connected together, and may also be connected to the open drain output of a master clock. When connected in this manner, the oscillators will lock to the device with the highest operating frequency. When synchronizing multiple ICs, it is recommended that the same timing resistor, corresponding to the switching frequency, be used in all the HV9911 circuits.

On rare occasions, given the length of the connecting lines for the SYNC pins, a resistor between SYNC and GND may be required to damp any ringing due to parasitic capacitances. It is recommended that the resistor chosen be greater than 300kΩ.

When synchronized in this manner, a permanent HIGH or LOW condition on the SYNC pin will result in a loss of synchronization, but the HV9911 based converters will continue to operate at their individually set operating frequency. Since loss of synchronization will not result in total system failure, the SYNC pin is considered fault tolerant.

Note:

The HV9911 is designed to SYNC up to four ICs at a time without the use of an external buffer. To SYNC more than four ICs, it is recommended that a buffered external clock be used.

Internal 1MHz Transconductance Amplifier

HV9911 includes a built in 1MHz transconductance amplifier, with tri-state output, which can be used to close the feedback loop. The output current sense signal is connected to the FDBK pin and the current reference is connected to the IREF pin.

The output of the opamp is controlled by the signal applied to the PWMD pin. When PWMD is high, the output of the opamp is connected to the COMP pin. When PWMD is low, the output is left open. This enables the integrating capacitor to hold the charge when the PWMD signal has turned off the GATE drive. When the IC is enabled, the voltage on the integrating capacitor will force the converter into steady state almost instantaneously.

The output of the opamp is buffered and connected to the current sense comparator using a 15:1 divider. The buffer helps to prevent the integrator capacitor from discharging during the PWM dimming state.

Linear Dimming

Linear dimming can be accomplished by varying the voltage at the IREF pin, as the output current is proportional to the voltage at the IREF pin. This can be done either by using a potentiometer from the REF pin or by applying an external voltage source at the IREF pin.

Note:

Due to the offset voltage of the transconductance opamp, pulling the IREF pin very close to GND will cause the internal short circuit comparator to trigger and shut down the IC. This limits the linear dimming range of the IC. However, a 1:10 linear dimming range can be easily obtained. It is recommended that the PWMD pin be used to get zero output current rather than pull the I_{REF} pin to GND.

PWM Dimming

PWM dimming can be achieved by driving the PWMD pin with a TTL compatible source. The PWM signal is connected internally to the three different nodes – the transconductance amplifier, the $\overline{\text{FAULT}}$ output, and the GATE output.

When the PWMD signal is high, the GATE and $\overline{\text{FAULT}}$ pins are enabled, and the output of the transconductance opamp is connected to the external compensation network. Thus, the internal amplifier controls the output current. When the PWMD signal goes low, the output of the transconductance amplifier is disconnected from the compensation network. Thus, the integrating capacitor maintains the voltage across it. The GATE is disabled, so the converter stops switching and the $\overline{\text{FAULT}}$ pin goes low, turning off the disconnect switch.

The output capacitor of the converter determines the PWM dimming response of the converter, since it has to get charged and discharged whenever the PWMD signal goes high or low. In the case of a buck converter, since the inductor current is continuous, a very small capacitor is used across the LEDs. This minimizes the effect of the capacitor on the PWM dimming response of the converter. However, in the case of a boost converter, the output current is discontinuous, and a very large output capacitor is required to reduce the ripple in the LED current. Thus, this capacitor will have a significant impact on the PWM dimming response. By turning off the disconnect switch when PWMD goes low, the output capacitor is prevented from being discharged, and thus the PWM dimming response of the boost converter improves dramatically.

Note:

Disconnecting the capacitor might cause a sudden spike in the capacitor voltage as the energy in the inductor is dumped into the capacitor. This might trigger the OVP comparator if the OVP point is set too close to the maximum operating voltage. Thus, either the capacitor has to sized slightly larger or the OVP set point has to be increased.

Note:

The HV9911 IC might latch-up if the PWMD pin is pulled 0.3V below GND, causing failure of the part. This abnormal condition can happen if there is a long cable between the PWM signal and the PWMD pin of the IC. It is recommended that a 1.0kΩ resistor be connected between the PWMD pin and the PWM signal input to the HV9911. This resistor, when placed close to the IC, will damp out any ringing that might cause the voltage at the PWMD pin to go below GND.

Avoiding False Shutdowns of the HV9911

The HV9911 has two fault modes which trigger a latched protection mode, an over current (or short circuit) protection, and an over voltage protection.

To prevent false triggering due to the tripping of the over voltage comparator, (due to noise in the GND traces on the PCB), it is recommended that a 1.0 - 10nF capacitor be connected between the OVP pin and GND. Although this capacitor will slow down the response of the over voltage protection circuitry somewhat, it will not affect the overall performance of the converter, as the large output capacitance in the boost design will limit the rate of rise of the output voltage.

In some cases, the over current protection may be triggered during PWM dimming, when the $\overline{\text{FAULT}}$ goes high and the disconnect switch is turned on. This triggering of the over current protection is related to the parasitic capacitance of the LED string (shown as a lumped capacitance C_{LED} in Fig. 4).

During normal PWM dimming operation, the HV9911 maintains the voltage across the output capacitor (C_O), by turning off the disconnect switch and preserving the charge in the output capacitance when the PWM dimming signal is low. At the same time, the voltage at the drain of the disconnect FET is some non-zero value V_D. When the PWM dimming signal goes high, FET Q_2 is turned ON. This causes the voltage at the drain of the FET (V_D) to instantly go to zero. Assuming a constant output voltage V_O,

$$i_{SENSE} = C_{LED} \bullet d(V_O - V_D) / dt$$

$$= -C_{LED} \bullet dV_D / dt$$

In this case, the rate of fall of the drain voltage of the disconnect FET is a large value (since the FET turns on very quickly) and this causes a spike of current through the sense resistor, which could trigger the over current protection (depending on the parasitic capacitance of the LED string).

To prevent this condition, a simple RC low pass filter network can be added as shown in Fig. 5. Typical values are R_F = 1.0kΩ and C_F = 470pF. This filter will block the FDBK pin from seeing the turn-on spike and normalize the PWM dimming operation of the HV9911 boost converter. This will have minimal effect on the stability of the loop but will increase the response time to an output short. If the increase in the response time is large, it might damage the output current sense resistor due to exceeding its peak-current rating.

The increase in the short circuit response time can be computed using the various component values of the boost converter. Consider a boost converter with a nominal output current I_O = 350mA, an output sense resistor R_S = 1.24Ω, LED string voltage V_O = 100V and an output capacitor C_O = 2.0mF. The disconnect FET is a TN2510N8 from Supertex which has a saturation current I_{SAT} = 3A (at V_{GS} = 6.0V). The increase in the short circuit response time due to the RC filter can then be computed as:

$$\Delta t \approx R_F \bullet C_F \bullet \left| ln\left(1 - \frac{I_O}{I_{SAT} - I_O}\right)\right|$$

$$= 1k\Omega \bullet 470pF \bullet \left| ln\left(1 - \frac{0.35A}{3A - 0.35A}\right)\right|$$

$$\approx 66ns$$

This increase is found to be negligible (note that the equation is valid for $\Delta T << R_S \bullet C_O$. In this case, $R_S \bullet C_O$ = 2.48µs, and the condition holds.

Sizing the Output Sense Resistor

To avoid exceeding the peak-current rating of the output sense resistor during short circuit conditions, the power rating of the resistor has to be chosen properly.

In this case, the maximum power dissipated in the sense resistor is:

$$P_{SC} = I^2_{SAT} \bullet R_S = 11W$$

From the datasheet for a 1.24Ω, 1/4W resistor, the maximum power it can dissipate for a single 1ms pulse of current is 11W. Since the total short circuit time is about 350ns (including the 300ns time for turn off), the resistor should be able to handle the current.

Fig. 4. Output of the Boost Converter Showing LED Parsed Capacitance

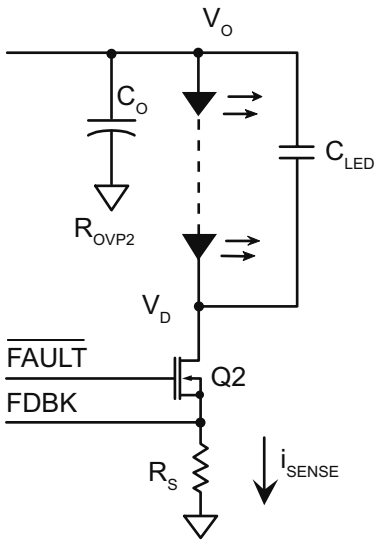
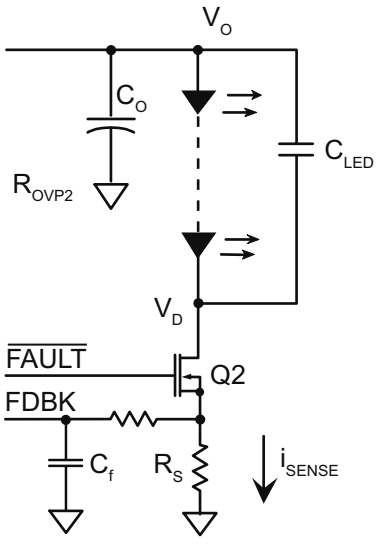


Fig. 5. Adding a Low-pass Filter to Prevent Pulse Triggering

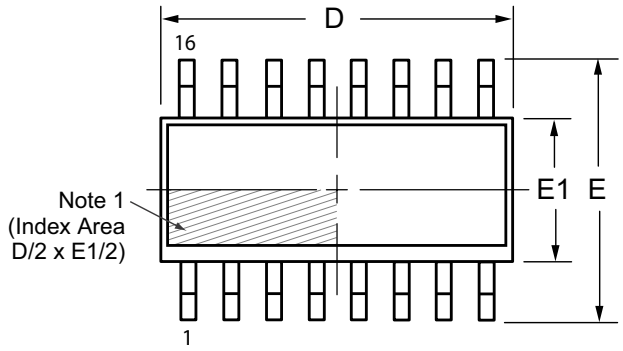


Pin Description

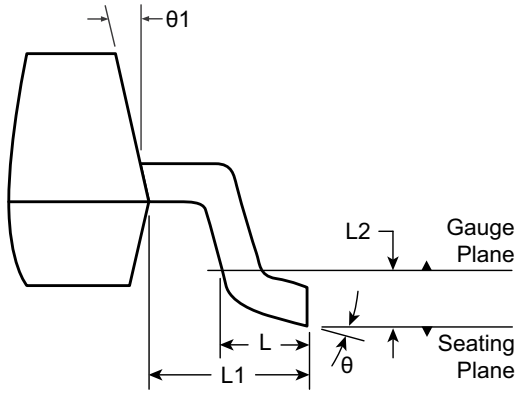
Pin #	Pin	Description
1	VIN	This pin is the input of a 250V high voltage regulator.
2	VDD	This is a power supply pin for all internal circuits. It must be bypassed with a low ESR capacitor to GND (at least 0.1uF).
3	GATE	This pin is the output GATE driver for an external N-channel power MOSFET.
4	GND	Ground return for all circuits. This pin must be connected to the return path from the input.
5	CS	This pin is used to sense the drain current of the external power FET. It includes a built-in 100ns (min) blanking time.
6	SC	Slope compensation for current sense. A resistor between SC and GND will program the slope compensation. In case of constant off-time mode of operation, slope compensation is unnecessary and the pin can be left open.
7	RT	This pin sets the frequency or the off-time of the power circuit. A resistor between RT and GND will program the circuit in constant frequency mode. A resistor between RT and GATE will program the circuit in a constant off-time mode.
8	SYNC	This I/O pin may be connected to the SYNC pin of other HV9911 circuits and will cause the oscillators to lock to the highest frequency oscillator.
9	CLIM	This pin provides a programmable input current limit for the converter. The current limit can be set by using a resistor divider from the REF pin.
10	REF	This pin provides 2% accurate reference voltage. It must be bypassed with at least a 10nF - 0.22µF capacitor to GND.
11	$\overline{\text{FAULT}}$	This pin is pulled to ground when there is an output short circuit condition or output over voltage condition. This pin can be used to drive an external MOSFET in the case of boost converters to disconnect the load from the source.
12	OVP	This pin provides the over voltage protection for the converter. When the voltage at this pin exceeds 1.25V, the GATE output of the HV9911 is turned off and $\overline{\text{FAULT}}$ goes low. The IC will turn on when the power is recycled.
13	PWMD	When this pin is pulled to GND (or left open), switching of the HV9911 is disabled. When an external TTL high level is applied to it, switching will resume.
14	COMP	Stable Closed loop control can be accomplished by connecting a compensation network between COMP and GND.
15	IREF	The voltage at this pin sets the output current level. The current reference can be set using a resistor divider from the REF pin.
16	FDBK	This pin provides output current feedback to the HV9911 by using a current sense resistor.

16-Lead SOIC (Narrow Body) Package Outline (NG)

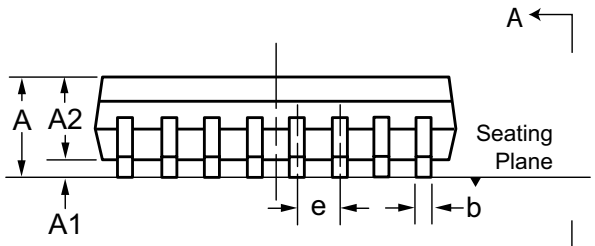
9.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



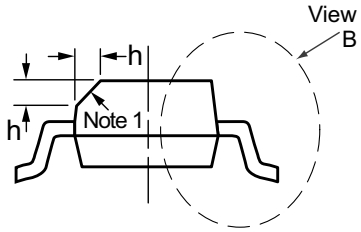
Top View



View B



Side View



View A-A

Note:

1. *This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	9.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	9.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	10.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AC, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
***Supertex Doc. #:** DSPD-16SONG, Version G041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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