

HEXFET® Power MOSFET

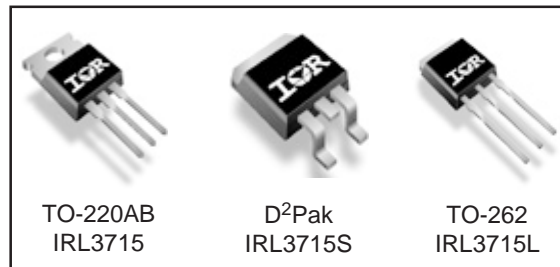
Applications

- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
- High Frequency Buck Converters for Computer Processor Power

Benefits

- Ultra-Low Gate Impedance
- Very Low $R_{DS(on)}$ at 4.5V V_{GS}
- Fully Characterized Avalanche Voltage and Current

V_{DS}	$R_{DS(on)}$ max	I_D
20V	14m Ω	54A [Ⓒ]



Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	± 20	V
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	54 [Ⓒ]	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	38 [Ⓒ]	
I_{DM}	Pulsed Drain Current [Ⓓ]	210	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	71	W
$P_D @ T_A = 25^\circ\text{C}$	Maximum Power Dissipation [Ⓔ]	3.8	W
	Linear Derating Factor	0.48	W/ $^\circ\text{C}$
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 175	$^\circ\text{C}$

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.1	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface [Ⓓ]	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient [Ⓓ]	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) [Ⓔ]	—	40	

Notes [Ⓓ] through [Ⓔ] are on page 11

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	20	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.022	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	11	14	mΩ	V _{GS} = 10V, I _D = 26A ③
		—	15	20		V _{GS} = 4.5V, I _D = 21A ③
V _{GS(th)}	Gate Threshold Voltage	1.0	—	3.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 16V, V _{GS} = 0V
		—	—	100		V _{DS} = 16V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V _{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-200		V _{GS} = -16V

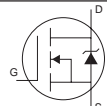
Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	26	—	—	S	V _{DS} = 10V, I _D = 21A
Q _g	Total Gate Charge	—	11	17	nC	I _D = 21A
Q _{gs}	Gate-to-Source Charge	—	3.8	—		V _{DS} = 10V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	4.4	—		V _{GS} = 4.5V
Q _{oss}	Output Gate Charge	—	11	17		V _{GS} = 0V, V _{DS} = 10V
t _{d(on)}	Turn-On Delay Time	—	6.4	—	ns	V _{DD} = 10V
t _r	Rise Time	—	73	—		I _D = 21A
t _{d(off)}	Turn-Off Delay Time	—	12	—		R _G = 1.8Ω
t _f	Fall Time	—	5.1	—		V _{GS} = 4.5V ③
C _{iss}	Input Capacitance	—	1060	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	700	—		V _{DS} = 10V
C _{rss}	Reverse Transfer Capacitance	—	120	—		f = 1.0MHz

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy②	—	110	mJ
I _{AR}	Avalanche Current①	—	21	A

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	54⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	210		
V _{SD}	Diode Forward Voltage	—	0.9	1.3	V	T _J = 25°C, I _S = 21A, V _{GS} = 0V ③
		—	0.8	—		T _J = 125°C, I _S = 21A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	37	56	ns	T _J = 25°C, I _F = 21A, V _R = 20V
Q _{rr}	Reverse Recovery Charge	—	28	42	nC	di/dt = 100A/μs ③
t _{rr}	Reverse Recovery Time	—	38	57	ns	T _J = 125°C, I _F = 21A, V _R = 20V
Q _{rr}	Reverse Recovery Charge	—	30	45	nC	di/dt = 100A/μs ③

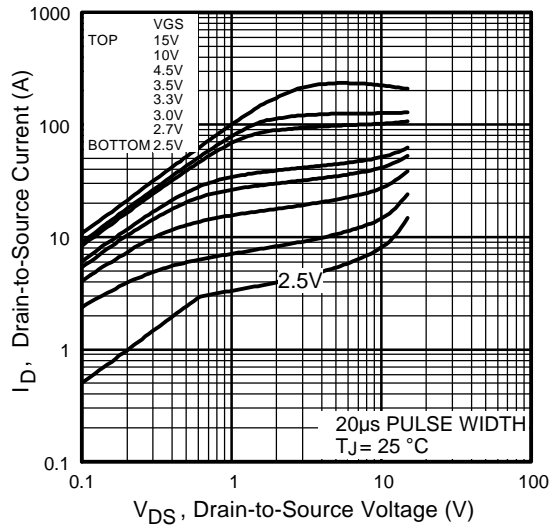


Fig 1. Typical Output Characteristics

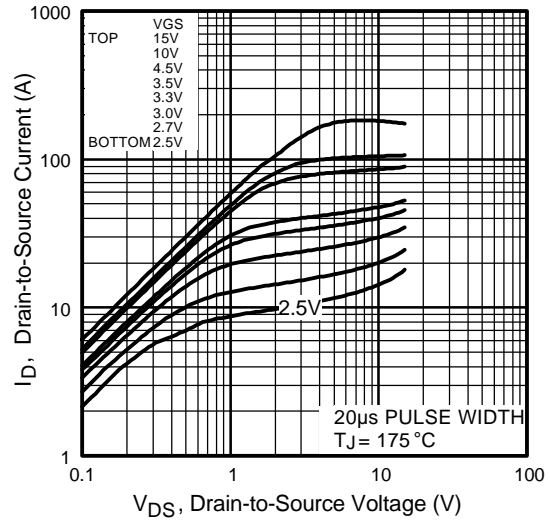


Fig 2. Typical Output Characteristics

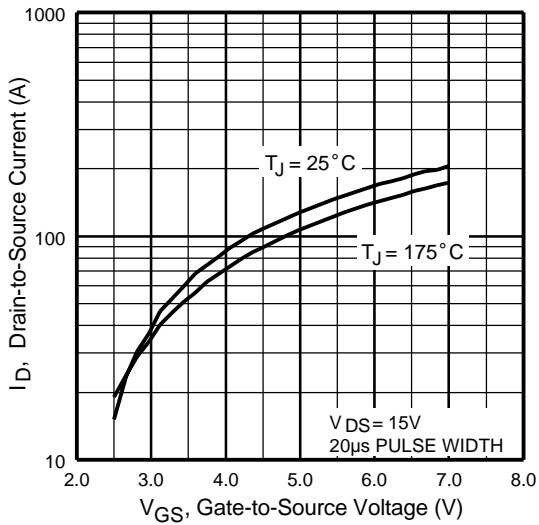


Fig 3. Typical Transfer Characteristics

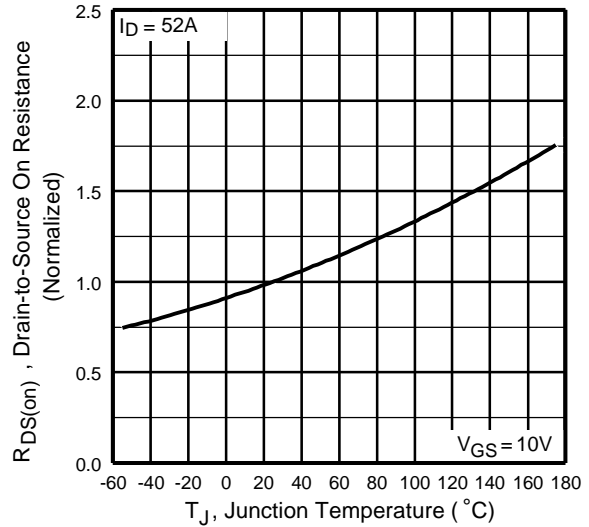


Fig 4. Normalized On-Resistance Vs. Temperature

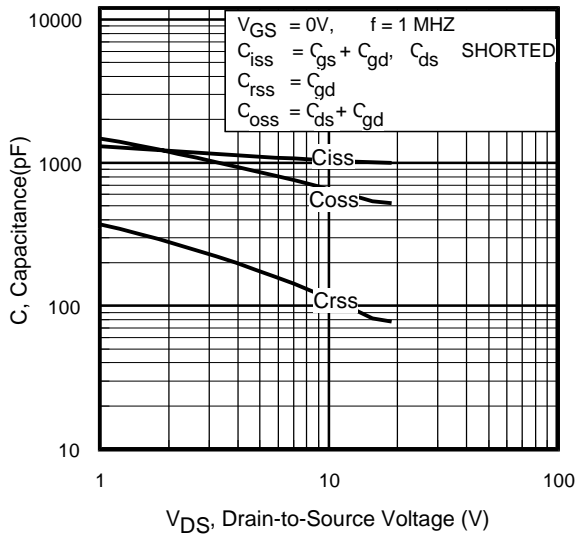


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

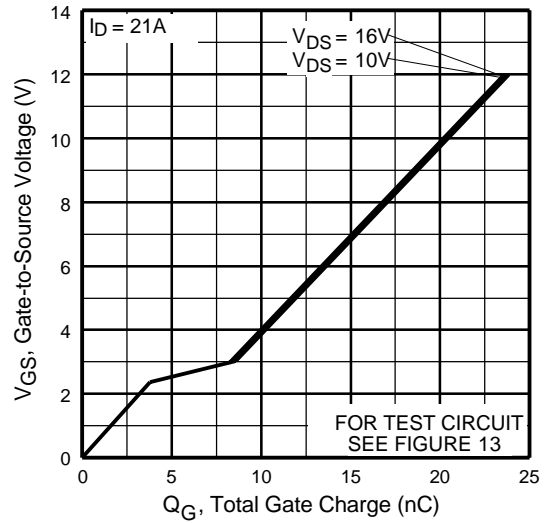


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

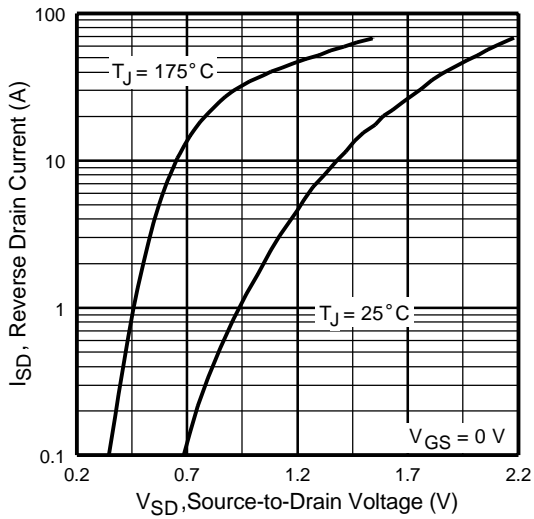


Fig 7. Typical Source-Drain Diode Forward Voltage

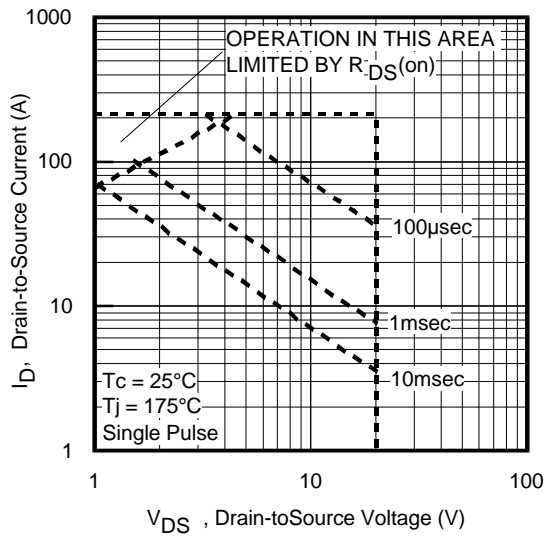


Fig 8. Maximum Safe Operating Area

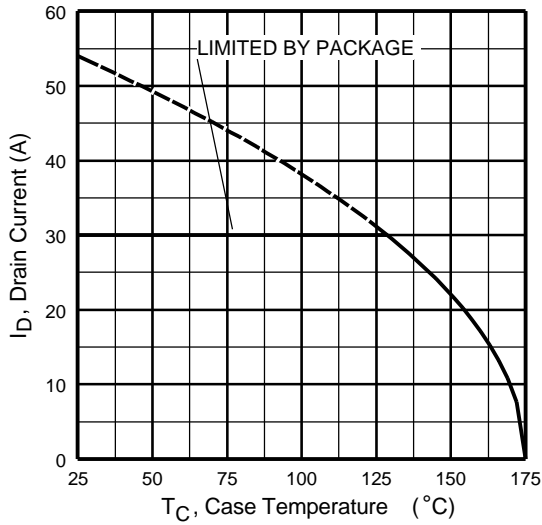


Fig 9. Maximum Drain Current Vs. Case Temperature

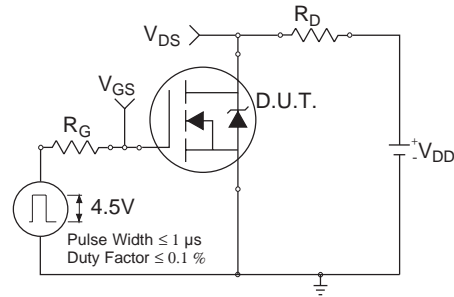


Fig 10a. Switching Time Test Circuit

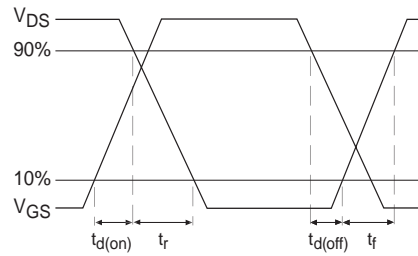


Fig 10b. Switching Time Waveforms

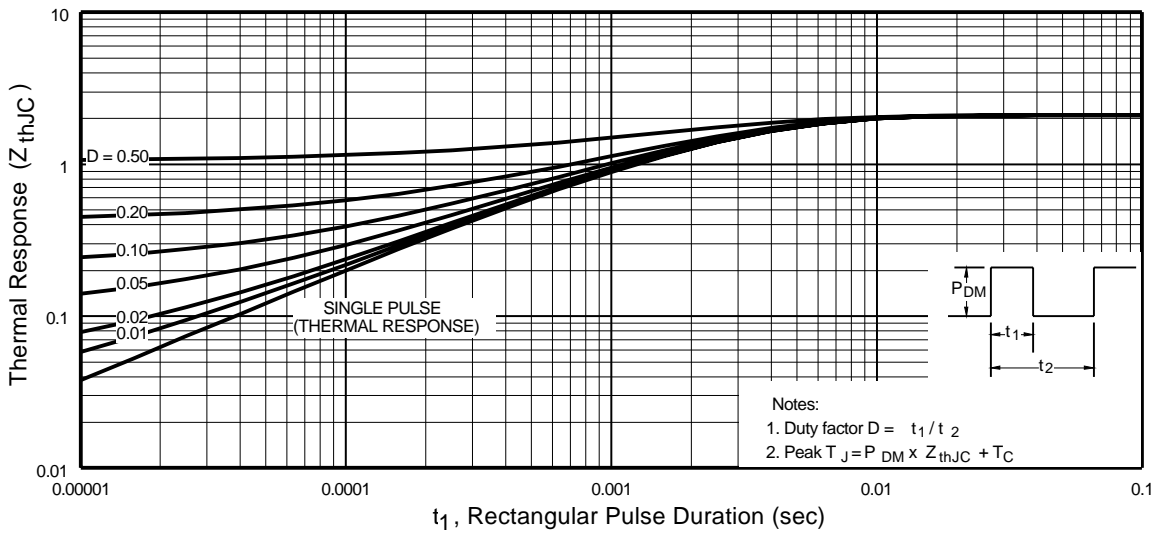


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

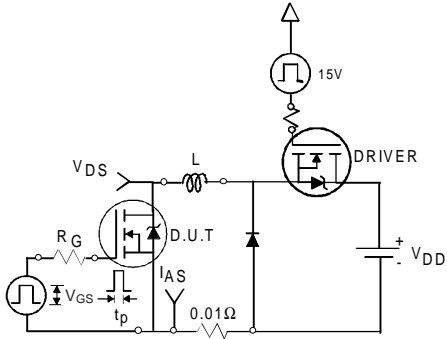


Fig 12a. Unclamped Inductive Test Circuit

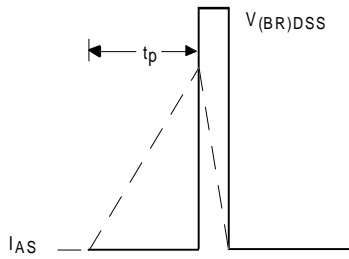


Fig 12b. Unclamped Inductive Waveforms

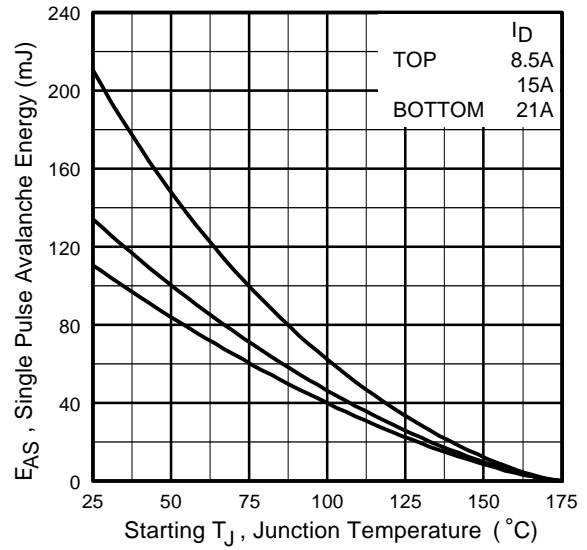


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

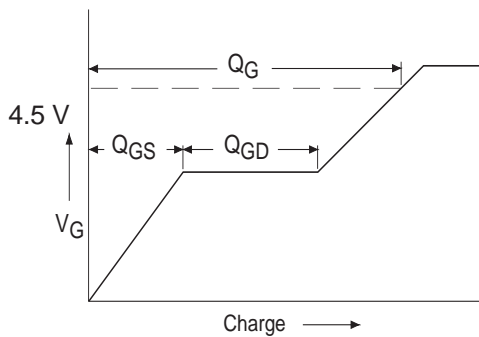


Fig 13a. Basic Gate Charge Waveform

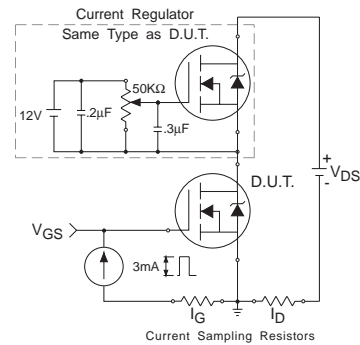
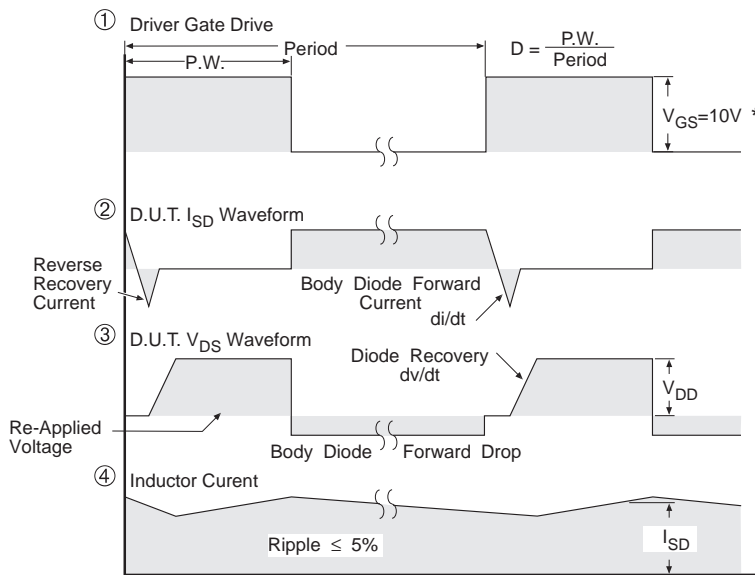
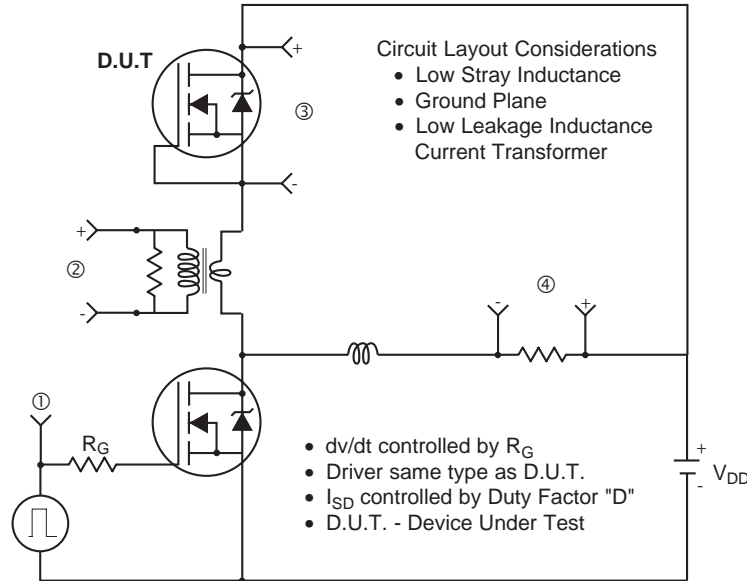


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

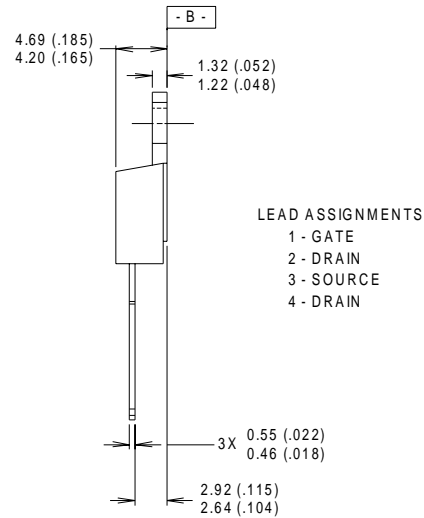
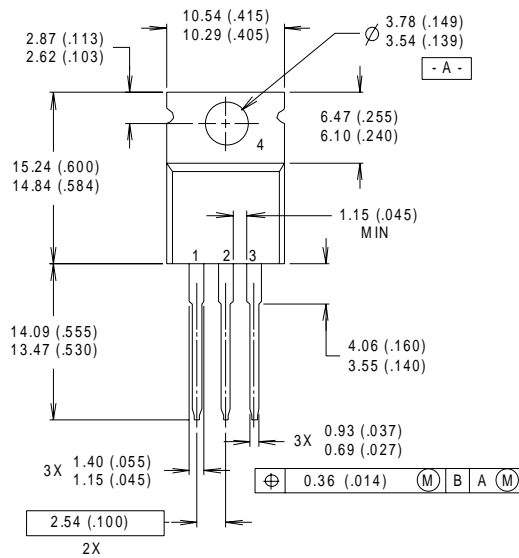
Fig 14. For N-Channel HEXFET® Power MOSFETs

IRL3715/S/L



TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



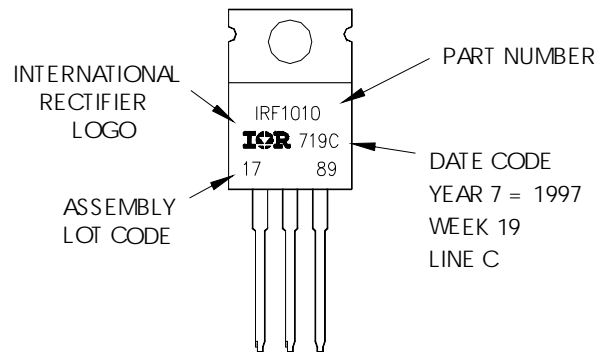
NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANS Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

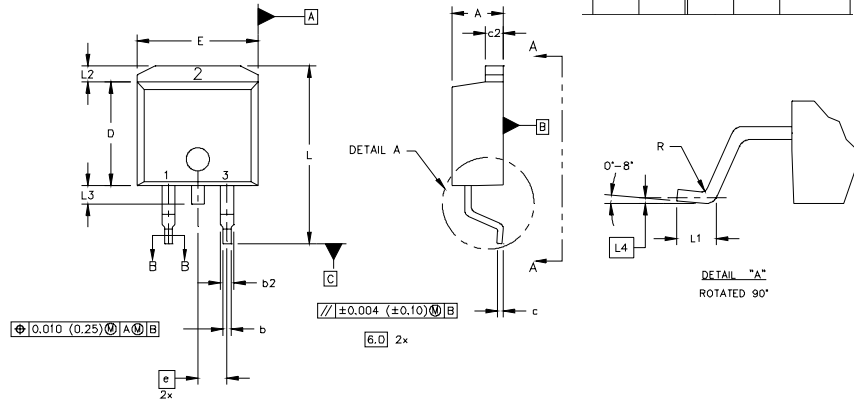
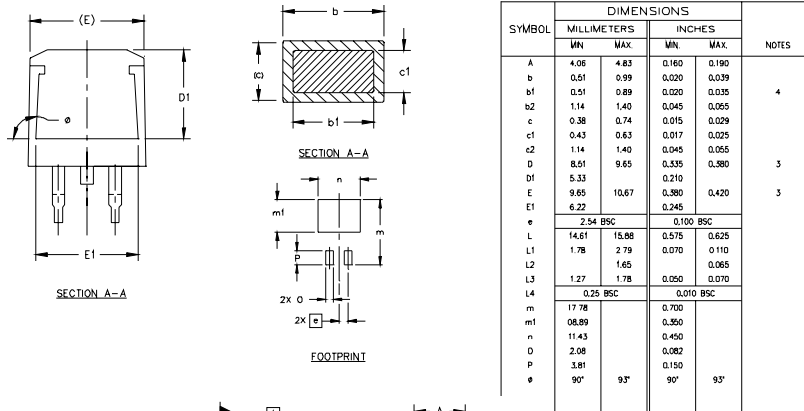
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"



D²Pak Package Outline



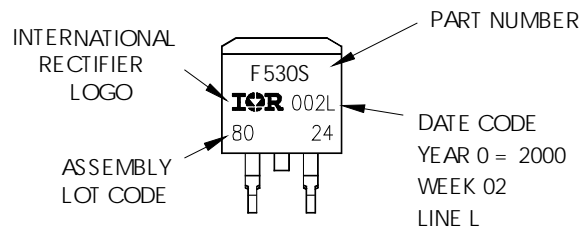
NOTES:
 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 3.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 4.0 DIMENSION b1 APPLY TO BASE METAL ONLY.
 5.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.
 6.0 CONTROLLING DIMENSION : INCHES.

LEAD ASSIGNMENTS

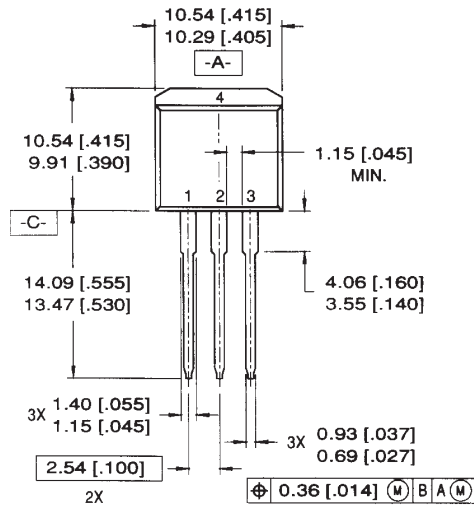
HEXFET	IGBTs, CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
 LOT CODE 8024
 ASSEMBLED ON WW 02, 2000
 IN THE ASSEMBLY LINE "L"

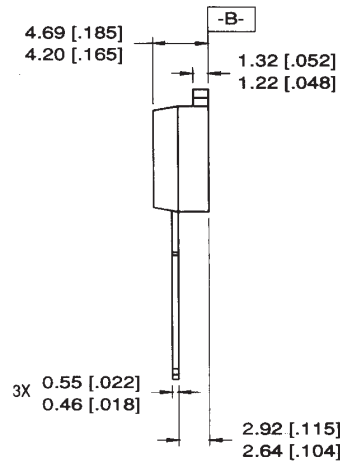


TO-262 Package Outline



LEAD ASSIGNMENTS

- | | |
|-----------|------------|
| 1 = GATE | 3 = SOURCE |
| 2 = DRAIN | 4 = DRAIN |

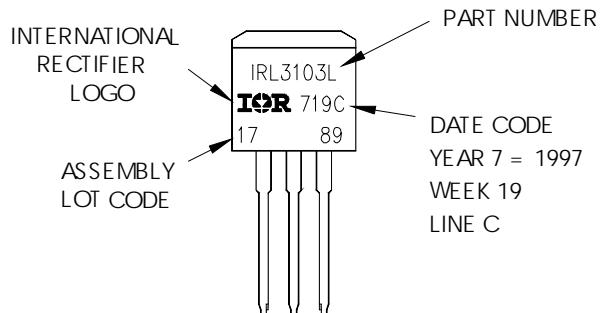


NOTES:

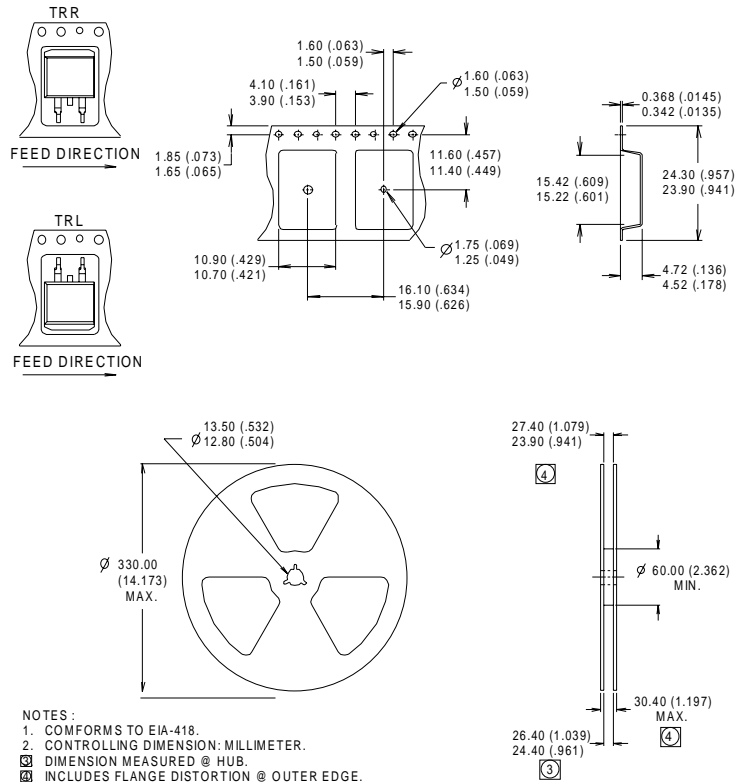
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"



D²Pak Tape & Reel Information



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.51\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 21\text{A}$, $V_{GS} = 10\text{V}$
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ This is only applied to TO-220A package
- ⑤ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
Package limitation current is 30A.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.