2.5V Drive Pch+Pch MOS FET

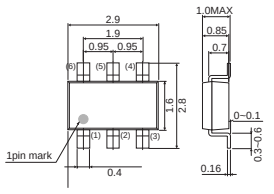
QS6J3

●Structure
Silicon P-channel MOS FET

●Features
1) Two Pch MOS FET transistors in a single TSMT6 package.
2) Low on-state resistance with a fast switching.
3) Low voltage drive (2.5V).

●External dimensions (Unit : mm)

TSMT6

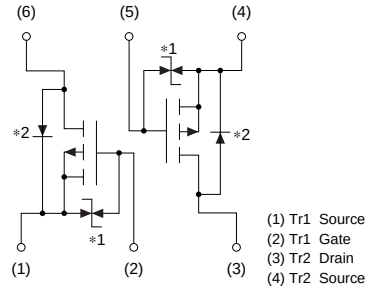


Each lead has same dimensions

Abbreviated symbol : J03

●Applications
Switching

●Inner circuit



∗1 ESD PROTECTION DIODE
∗2 BODY DIODE

●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS6J3		○

●Absolute maximum ratings (Ta=25°C)
<It is the same ratings for Tr1 and Tr2 >

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	−20	V
Gate-source voltage		V_{GSS}	±12	V
Drain current	Continuous	I_D	±1.5	A
	Pulsed	I_{DP} ∗1	±6.0	A
Source current (Body diode)	Continuous	I_S ∗1	−0.75	A
	Pulsed	I_{SP}	−6.0	A
Total power dissipation		P_D ∗2	1.25	W / TOTAL
			0.9	W / ELEMENT
Channel temperature		Tch	150	°C
Range of Storage temperature		Tstg	−55 to +150	°C

∗1 Pw≤10µs, Duty cycle≤1% ∗2 Mounted on a ceramic board

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth (ch-a) ∗	100	°C / W / TOTAL
		139	°C / W / ELEMENT

∗ Mounted on a ceramic board

●**Electrical characteristics** (Ta=25°C)

<It is the same characteristics for Tr1 and Tr2. MOS FET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	±10	μA	V_{GS}=±12V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	–20	–	–	V	I_D= –1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	–1	μA	V_{DS}= –20V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	–0.7	–	–2.0	V	V_{DS}= –10V, I_D= –1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$ *	–	155	215	mΩ	I_D= –1.5A, V_{GS}= –4.5V
		–	170	235	mΩ	I_D= –1.5A, V_{GS}= –4V
		–	310	430	mΩ	I_D= –0.75A, V_{GS}= –2.5V
Forward transfer admittance	$\|Y_{fs}\|$ *	1.0	–	–	S	V_{DS}= –10V, I_D= –0.75A
Input capacitance	C_{iss}	–	270	–	pF	V_{DS}= –10V
Output capacitance	C_{oss}	–	40	–	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	–	35	–	pF	f=1MHz
Turn-on delay time	$t_{d\ (on)}$ *	–	10	–	ns	I_D= –0.75A V_{DD}≒ –15V V_{GS}= –4.5V R_L=20Ω R_G=10Ω
Rise time	t_r *	–	12	–	ns	
Turn-off delay time	$t_{d\ (off)}$ *	–	45	–	ns	
Fall time	t_f *	–	20	–	ns	
Total gate charge	Q_g *	–	3.0	–	nC	V_{DD}≒ –15V R_L=10Ω
Gate-source charge	Q_{gs} *	–	0.8	–	nC	V_{GS}= –4.5V R_G=10Ω
Gate-drain charge	Q_{gd} *	–	0.85	–	nC	I_D= –1.5A

*Pulsed

<Body diode (Source-drain)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}	–	–	–1.2	V	I_S= –0.75A, V_{GS}=0V

●**Electrical characteristic curves**

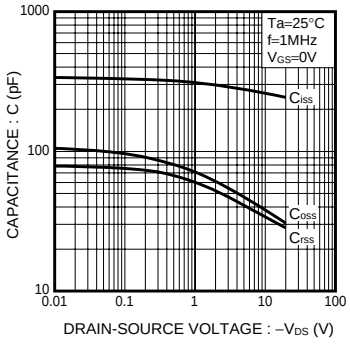


Fig.1 Typical Capacitance vs. Drain-Source Voltage

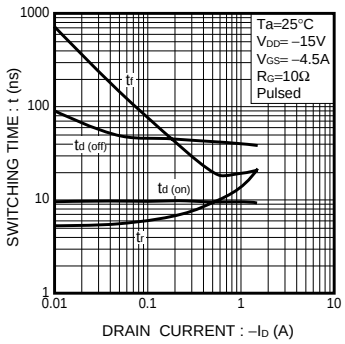


Fig.2 Switching Characteristics

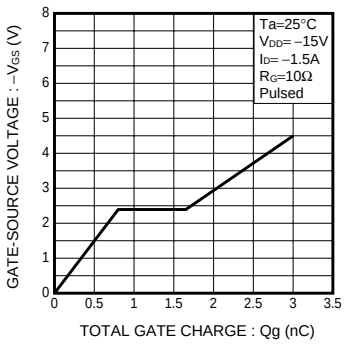


Fig.3 Dynamic Input Characteristics

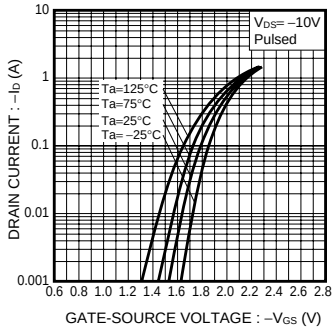


Fig.4 Typical Transfer Characteristics

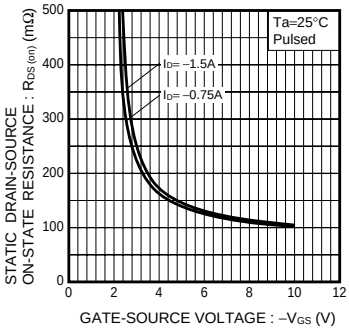


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

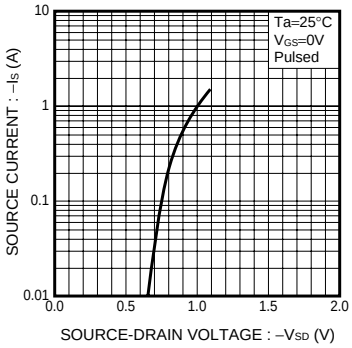


Fig.6 Source Current vs. Source-Drain Voltage

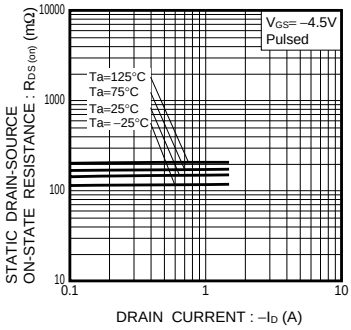


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

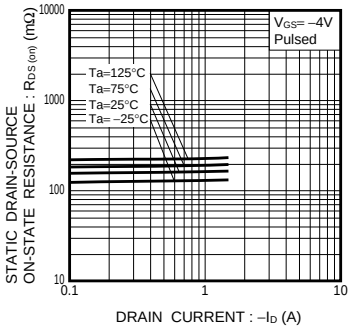


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

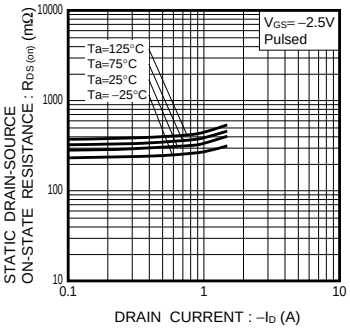


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

●**Measurement circuits**

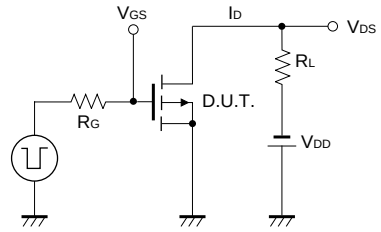


Fig.10 Switching Time Measurement Circuit

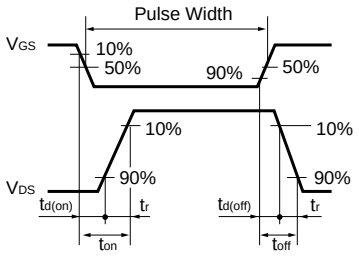


Fig.11 Switching Waveforms

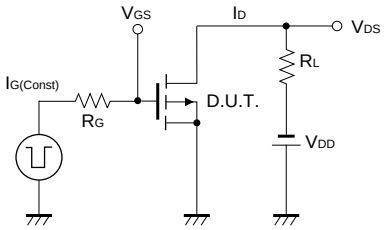


Fig.12 Gate Charge Measurement Circuit

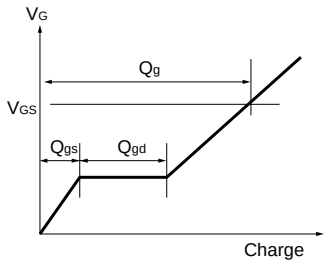


Fig.13 Gate Charge Waveform

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