

## Monolithic N-Channel JFET Duals

**SST404NL  
SST406NL**

**U401NL  
U404NL**

**U406NL**

### PRODUCT SUMMARY

Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	$g_{fs}$ Min (mS)	$I_G$ Typ (pA)	$ V_{GS1} - V_{GS2} $ Max (mV)
U401NL	-0.5 to -2.5	-40	1	-2	5
SST/U404NL	-0.5 to -2.5	-40	1	-2	15
SST/U406NL	-0.5 to -2.5	-40	1	-2	40

### FEATURES

- Anti Latchup Capability
- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 2 pA
- Low Noise
- High CMRR: 102 dB

### BENEFITS

- External Substrate Bias—Avoids Latchup
- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

### APPLICATIONS

- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters

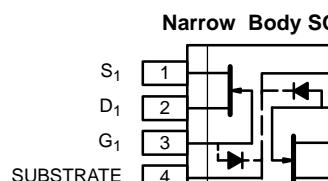
### DESCRIPTION

The SST/U401NL series of high-performance monolithic dual JFETs features extremely low noise, tight offset voltage and low drift over temperature specifications, and is targeted for use in a wide range of precision instrumentation applications. This series has a wide selection of offset and drift specifications with the U401NL featuring a 5-mV offset and 10- $\mu$ V/ $^{\circ}$ C drift.

Pins 4 and 8 of the SST series, and pin 4 of the U series part

numbers enable the substrate to be connected to a positive polarity, external bias ( $V_{DD}$ ) to avoid latchup.

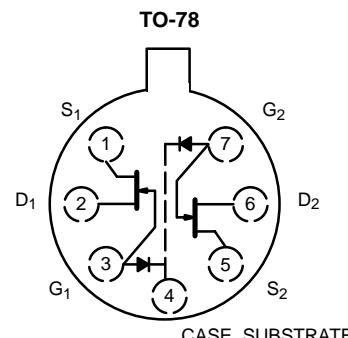
The U series, hermetically sealed TO-78 package is available with full military processing. The SST series SO-8 package provides ease of manufacturing, and the symmetrical pinout prevents improper orientation. The SO-8 package is available with tape-and-reel options for compatibility with automatic assembly methods.



Top View

Marking Codes:

SST404NL - 404NL  
SST406NL - 406NL



Case, Substrate

Top View

U401NL  
U404NL  
U406NL

### ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage .....	-40 V
Gate Current .....	10 mA
Lead Temperature (1/16" from case for 10 sec.) .....	300°C
Storage Temperature :      U Prefix .....	-65 to 200°C
SST Prefix .....	-55 to 150°C

For applications information see AN106.

Operating Junction Temperature ....., -55 to 150°C

Power Dissipation :      Per Side<sup>a</sup> ....., 300 mW  
                                  Total<sup>b</sup> ....., 500 mW

Notes

- a. Derate 2.4 mW/ $^{\circ}$ C above 25°C  
b. Derate 4 mW/ $^{\circ}$ C above 25°C

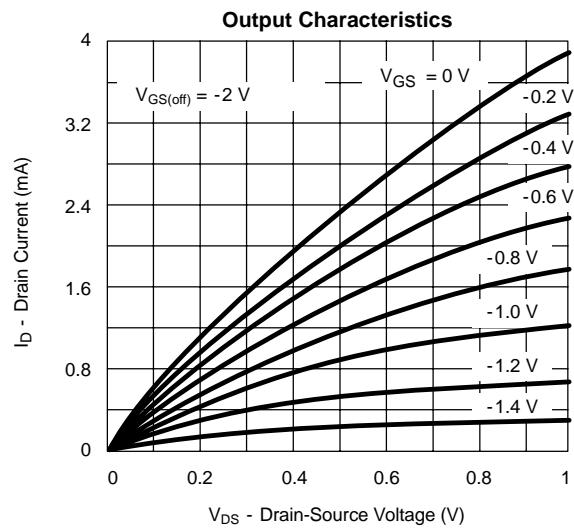
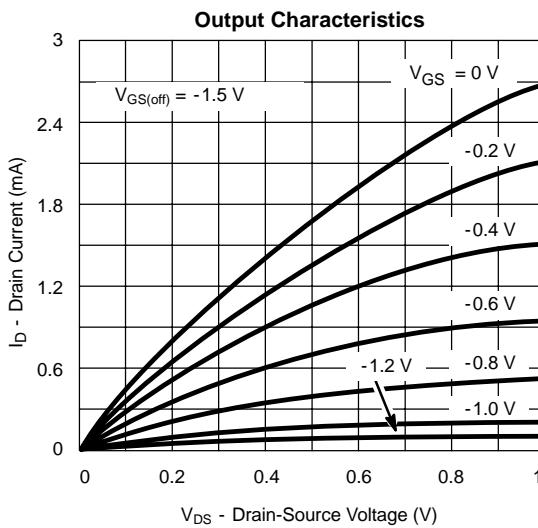
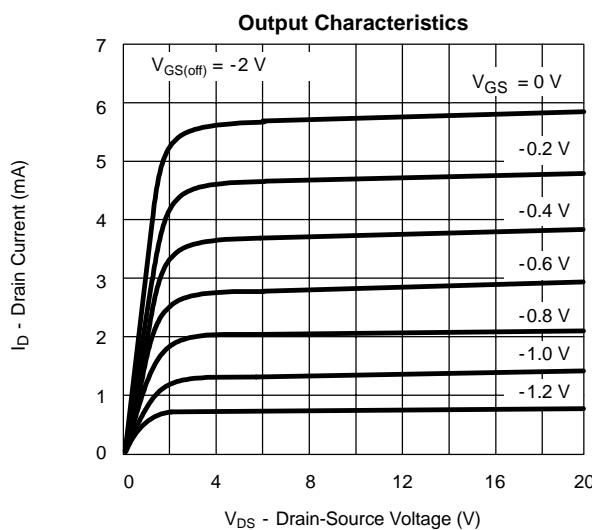
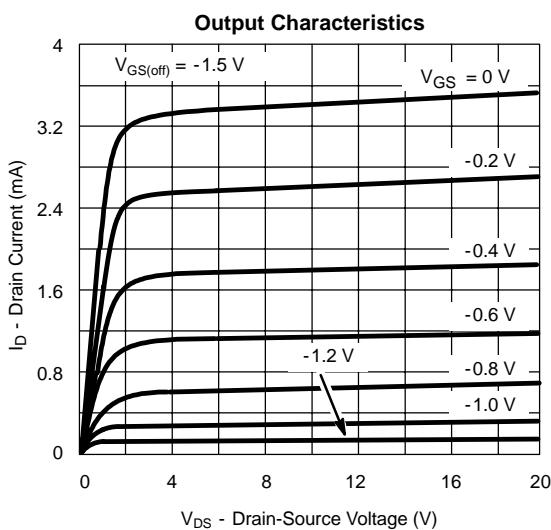
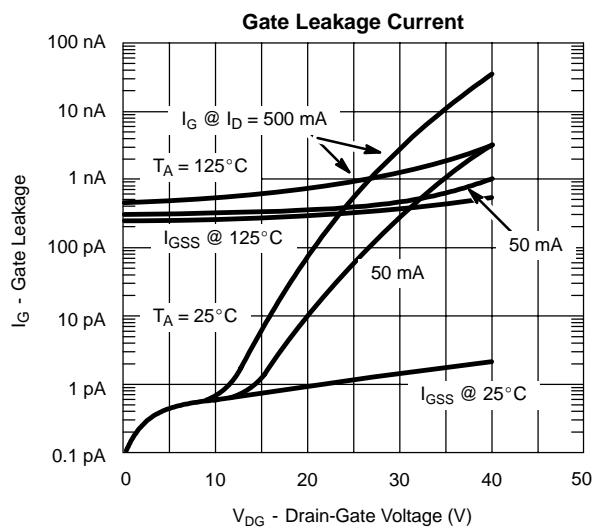
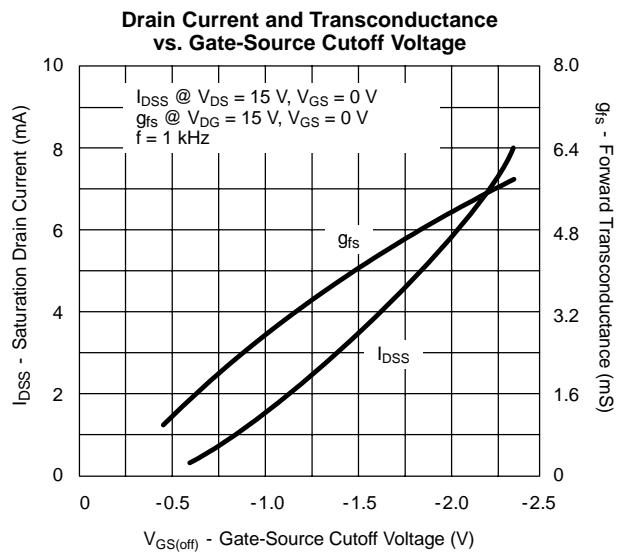
**SPECIFICATIONS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Conditions	Typ <sup>a</sup>	Limits						Unit	
				U401NL		SST/U404NL		SST/U406NL			
				Min	Max	Min	Max	Min	Max		
<b>Static</b>											
Gate-Source Breakdown Voltage	$V_{(\text{BR})\text{GSS}}$	$I_G = -1 \mu\text{A}, V_{DS} = 0 \text{ V}$	-58	-40		-40		-40		V	
	$V_{(\text{BR})\text{G1 - G2}}$	$I_G = \pm 1 \mu\text{A}, V_{DS} = 0 \text{ V}, V_{GS} = 0 \text{ V}$	$\pm 45$	$\pm 30$		$\pm 30$		$\pm 30$			
Gate-Source Cutoff Voltage	$V_{GS(\text{off})}$	$V_{DS} = 15 \text{ V}, I_D = 1 \text{ nA}$	-1.5	-0.5	-2.5	-0.5	-2.5	-0.5	-2.5		
Saturation Drain Current <sup>b</sup>	$I_{DSS}$	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}$	3.5	0.5	10	0.5	10	0.5	10	mA	
Gate Reverse Current	$I_{GSS}$	$V_{GS} = -30 \text{ V}, V_{DS} = 0 \text{ V}$	-2		-25		-25		-25	pA	
		$T_A = 125^\circ\text{C}$	-1							nA	
Gate Operating Current	$I_G$	$V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}$	-2		-15		-15		-15	pA	
		$T_A = 125^\circ\text{C}$	-0.8		-10		-10		-10	nA	
Drain-Source On-Resistance	$r_{DS(\text{on})}$	$V_{GS} = 0 \text{ V}, I_D = 0.1 \text{ mA}$	250							$\Omega$	
Gate-Source Voltage	$V_{GS}$	$V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}$	-1		-2.3		-2.3		-2.3	V	
Gate-Source Forward Voltage	$V_{GS(F)}$	$I_G = 1 \text{ mA}, V_{DS} = 0 \text{ V}$	0.7								
<b>Dynamic</b>											
Common-Source Forward Transconductance	$g_{fs}$	$V_{DS} = 15 \text{ V}, I_D = 200 \mu\text{A}$ $f = 1 \text{ kHz}$	1.5	1	2	1	2	1	2	mS	
Common-Source Output Conductance	$g_{os}$		1.3		2		2		2	$\mu\text{S}$	
Common-Source Forward Transconductance	$g_{fs}$	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}$ $f = 1 \text{ kHz}$	4	2	7	2	7	2	7	mS	
Common-Source Output Conductance	$g_{os}$		5		30		30		30	$\mu\text{S}$	
Common-Source Input Capacitance	$C_{iss}$	$V_{DS} = 15 \text{ V}, I_D = 200 \mu\text{A}$ $f = 1 \text{ MHz}$	4		8		8		8	pF	
Common-Source Reverse Transfer Capacitance	$C_{rss}$		1.5		3		3		3		
Equivalent Input Noise Voltage	$\bar{e}_n$	$V_{DS} = 15 \text{ V}, I_D = 200 \mu\text{A}$ $f = 10 \text{ Hz} (\text{U Only})$	10		20		20		20	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	
<b>Matching</b>											
Differential Gate-Source Voltage	$ V_{GS1} - V_{GS2} $	$V_{DG} = 10 \text{ V}, I_D = 200 \mu\text{A}$			5		15		40	mV	
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	$V_{DG} = 10 \text{ V}$ $I_D = 200 \mu\text{A}$ $T_A = -55 \text{ to } 125^\circ\text{C}$	SST404NL	20						$\frac{\mu\text{V}}{^\circ\text{C}}$	
			SST406NL	40							
			All U		10		25		80		
Common Mode Rejection Ratio	CMRR	$V_{DG} = 10 \text{ to } 20 \text{ V}, I_D = 200 \mu\text{A}$	102	95		95				dB	

## Notes

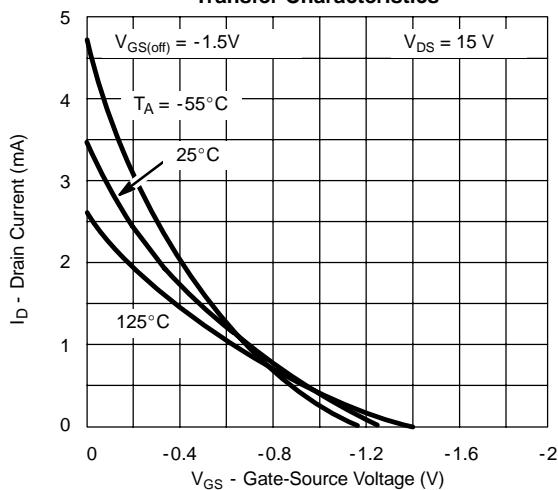
- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.  
 b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.

NRR

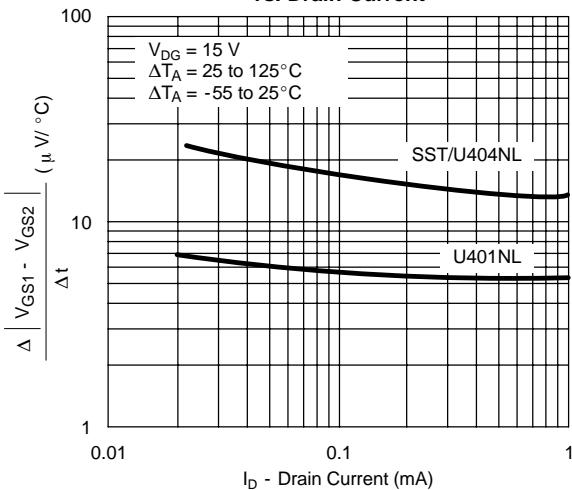
**TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)**


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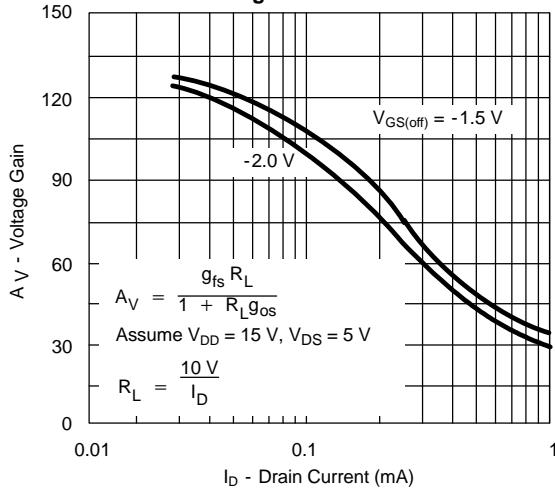
Transfer Characteristics



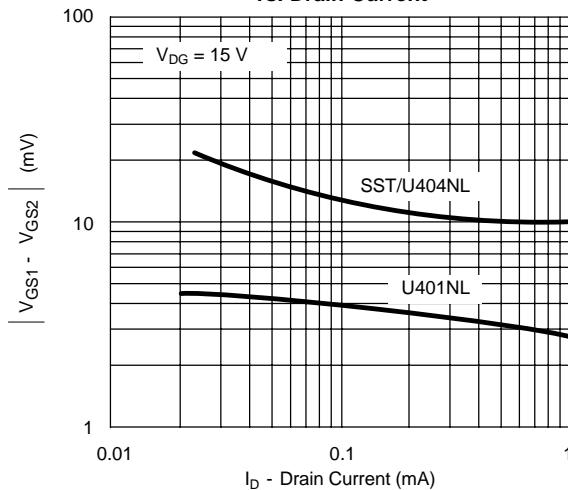
Voltage Differential with Temperature vs. Drain Current



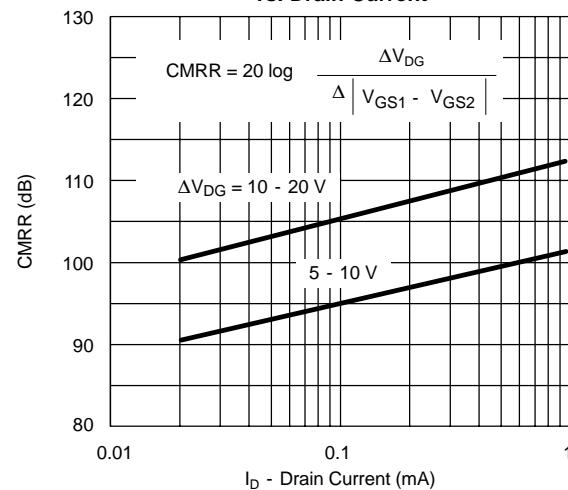
Circuit Voltage Gain vs. Drain Current



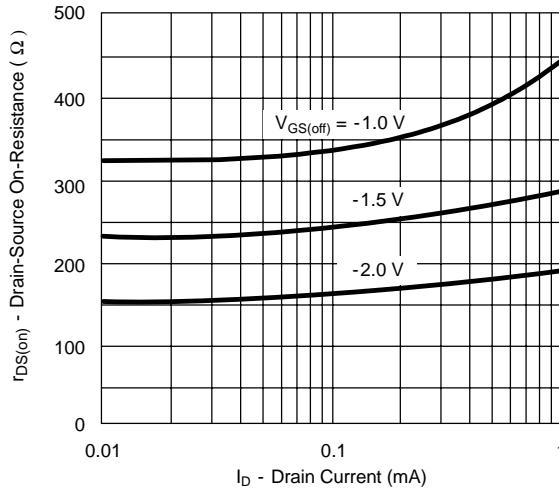
Gate-Source Differential Voltage vs. Drain Current



Common Mode Rejection Ratio vs. Drain Current



On-Resistance vs. Drain Current



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