



## Monolithic N-Channel JFET Duals

PRODUCT SUMMARY				
$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	$g_{fs}$ Min (mS)	$I_G$ Typ (pA)	$ V_{GS1} - V_{GS2} _{Max}$ (mV)
-1 to -6	-25	4.5	-1	20

### FEATURES

- Anti Latchup Capability
- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 1 pA
- Low Noise
- High CMRR: 90 dB

### BENEFITS

- External Substrate Bias—Avoids Latchup
- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- High-Speed Performance
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

### APPLICATIONS

- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High Speed Comparators
- Impedance Converters

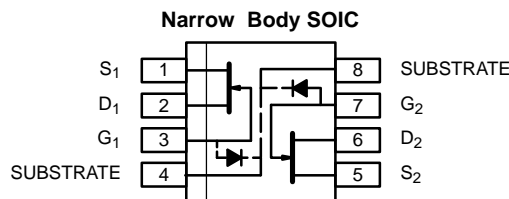
### DESCRIPTION

The SST441NL is a monolithic high-speed dual JFET mounted in a single SO-8 package. This JFET is an excellent choice for use as wideband differential amplifiers in demanding test and measurement applications.

Pins 4 and 8 on the SST441NL and pin 4 on the U441NL part numbers enable the substrate to be connected to a positive, external bias ( $V_{DD}$ ) to avoid latchup.

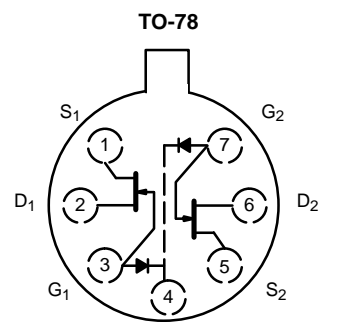
The U441NL in the hermetically sealed TO-78 package is available with full military processing.

The SO-8 package provides ease of manufacturing. The symmetrical pinout prevents improper orientation. The SO-8 package is available with tape-and-reel options for compatibility with automatic assembly methods.



Top View

Marking Codes:  
SST441NL - 441NL



Top View  
U441NL

### ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage	-25 V
Gate Current	50 mA
Lead Temperature ( $1/16$ " from case for 10 sec.)	300°C
Storage Temperature	-55 to 150°C
Operating Junction Temperature	-55 to 150°C

Power Dissipation :	Per Side <sup>a</sup>	300 mW
	Total <sup>b</sup>	500 mW

- Notes
- Derate 2.4 mW/°C above 25°C
  - Derate 4 mW/°C above 25°C

For applications information see AN102.

SPECIFICATIONS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ <sup>a</sup>	Max	
<b>Static</b>						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1\ \mu\text{A}, V_{DS} = 0\ \text{V}$	-25	-35		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 10\ \text{V}, I_D = 1\ \text{nA}$	-1	-3.5	-6	
Saturation Drain Current <sup>b</sup>	$I_{DSS}$	$V_{DS} = 10\ \text{V}, V_{GS} = 0\ \text{V}$	6	15	30	mA
Gate Reverse Current	$I_{GSS}$	$V_{GS} = -15\ \text{V}, V_{DS} = 0\ \text{V}$		-1	-500	pA
			$T_A = 125^\circ\text{C}$		-0.2	
Gate Operating Current	$I_G$	$V_{DG} = 10\ \text{V}, I_D = 5\ \text{mA}$		-1	-500	pA
			$T_A = 125^\circ\text{C}$		-0.2	
Gate-Source Forward Voltage	$V_{GS(F)}$	$I_G = 1\ \text{mA}, V_{DS} = 0\ \text{V}$		0.7		V
<b>Dynamic</b>						
Common-Source Forward Transconductance	$g_{fs}$	$V_{DS} = 10\ \text{V}, I_D = 5\ \text{mA}$ $f = 1\ \text{kHz}$	4.5	6	9	mS
Common-Source Output Conductance	$g_{os}$				20	200
Common-Source Forward Transconductance	$g_{fs}$	$V_{DS} = 10\ \text{V}, I_D = 5\ \text{mA}$ $f = 100\ \text{MHz}$		5.5		mS
Common-Source Output Conductance	$g_{os}$				30	
Common-Source Input Capacitance	$C_{iss}$	$V_{DS} = 10\ \text{V}, I_D = 5\ \text{mA}$ $f = 1\ \text{MHz}$		3.5		pF
Common-Source Reverse Transfer Capacitance	$C_{rss}$				1	
Equivalent Input Noise Voltage	$\bar{e}_n$	$V_{DS} = 10\ \text{V}, I_D = 5\ \text{mA}$ $f = 10\ \text{kHz}$		4		$\text{nV}/\sqrt{\text{Hz}}$
<b>Matching</b>						
Differential Gate-Source Voltage	$ V_{GS1} - V_{GS2} $	$V_{DG} = 10\ \text{V}, I_D = 5\ \text{mA}$		7	20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	$V_{DG} = 10\ \text{V}, I_D = 5\ \text{mA}$ $T_A = -55\ \text{to}\ 125^\circ\text{C}$		10		$\mu\text{V}/^\circ\text{C}$
Saturation Drain Current Ratio <sup>c</sup>	$\frac{I_{DSS1}}{I_{DSS2}}$	$V_{DS} = 10\ \text{V}, V_{GS} = 0\ \text{V}$		0.98		
Transconductance Ratio <sup>c</sup>	$\frac{g_{fs1}}{g_{fs2}}$	$V_{DS} = 10\ \text{V}, I_D = 5\ \text{mA}$ $f = 1\ \text{kHz}$		0.98		
Common Mode Rejection Ratio	CMRR	$V_{DG} = 10\ \text{to}\ 15\ \text{V}, I_D = 5\ \text{mA}$		90		dB

## Notes

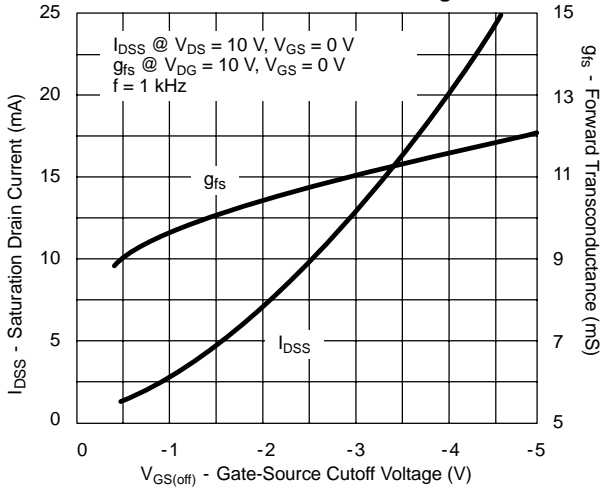
- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.  
 b. Pulse test:  $PW \leq 300\ \mu\text{s}$  duty cycle  $\leq 3\%$ .  
 c. Assumes smaller value in the numerator.

NNZ

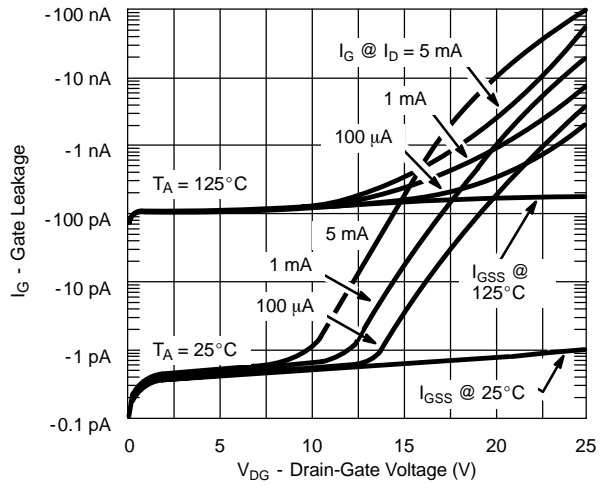


**TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)**

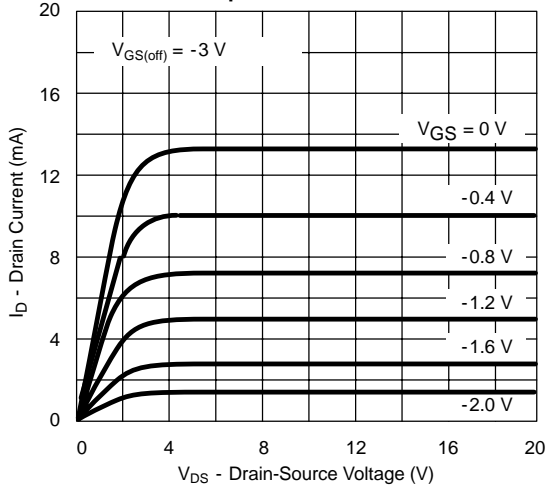
**Drain Current and Transconductance vs. Gate-Source Cutoff Voltage**



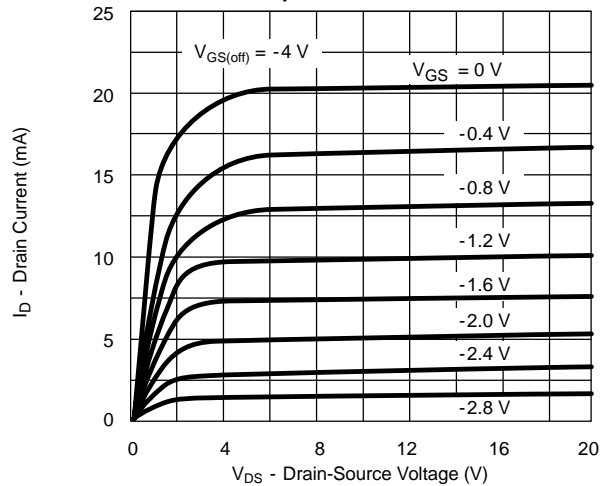
**Gate Leakage Current**



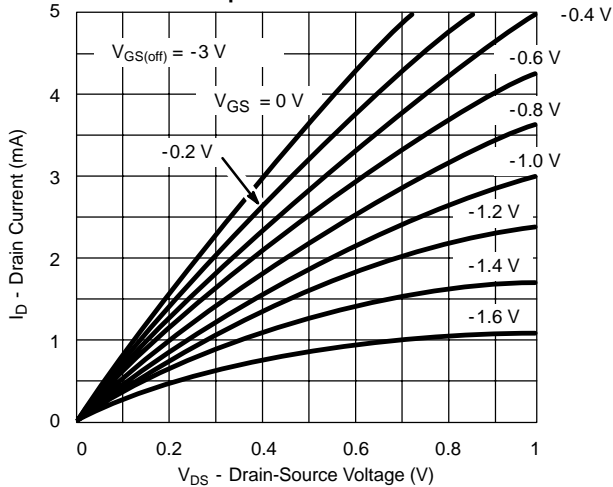
**Output Characteristics**



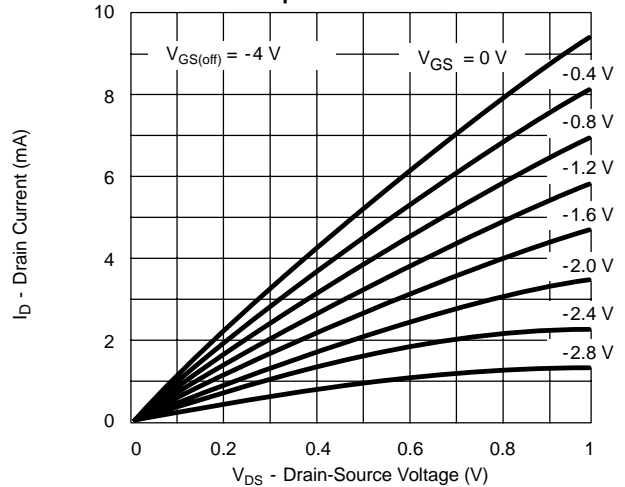
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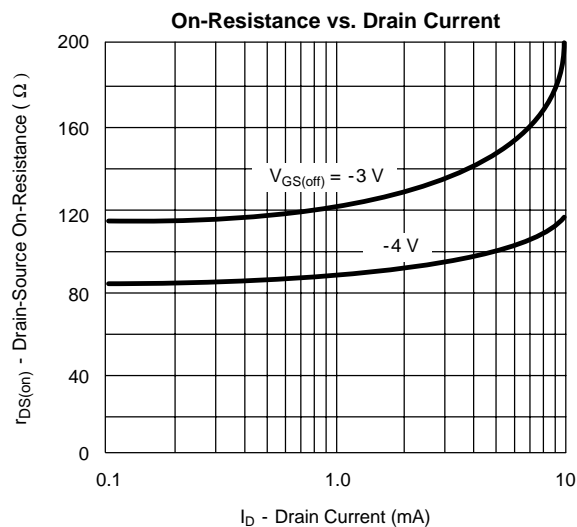
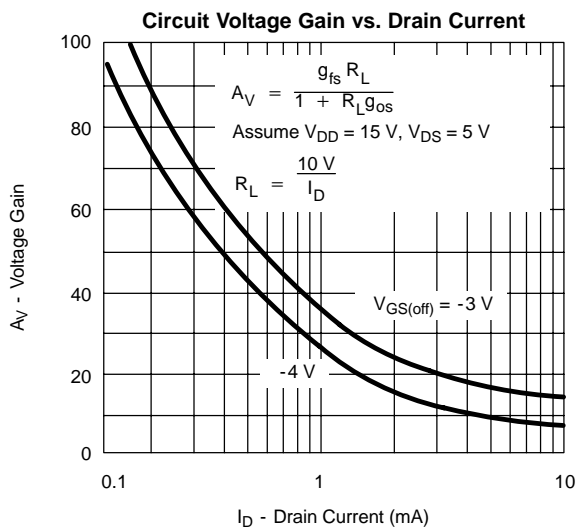
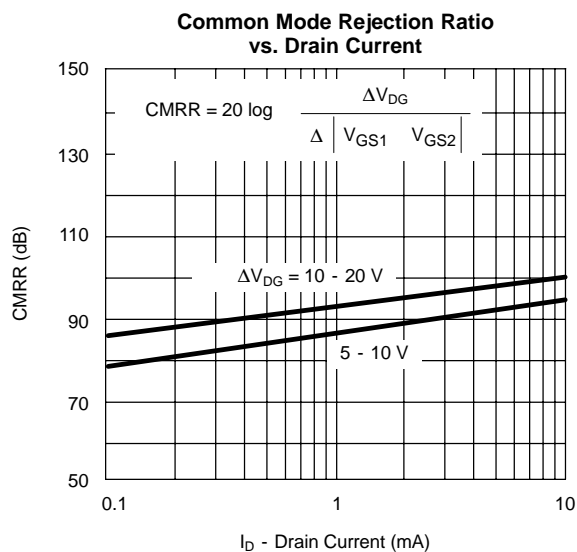
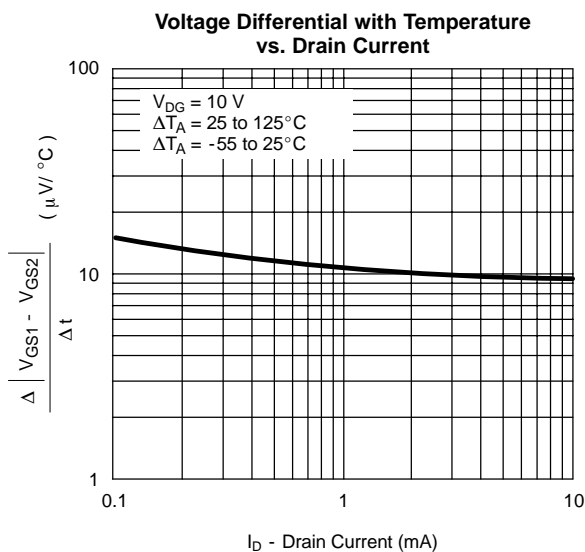
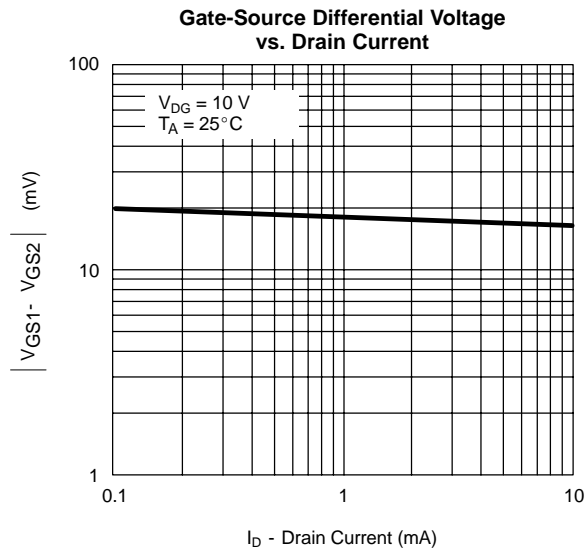
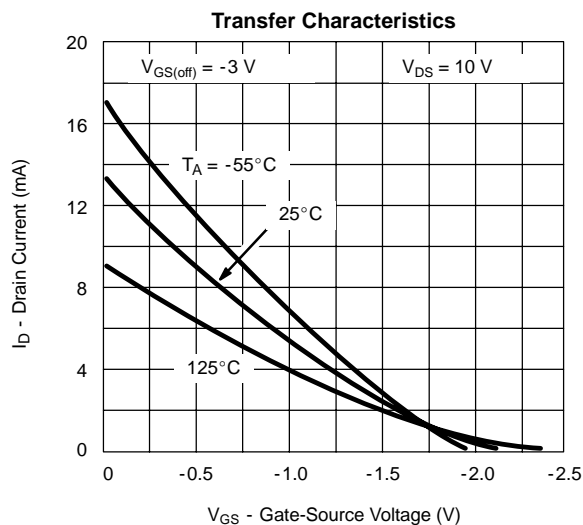
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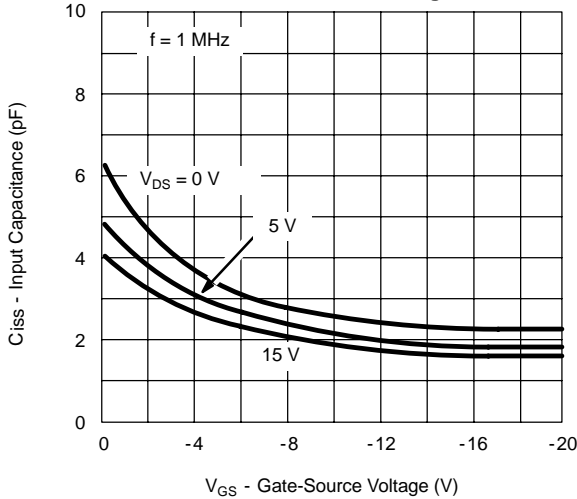
### TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



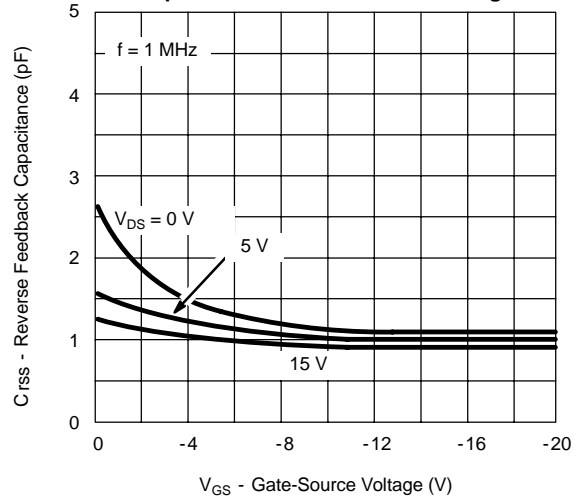


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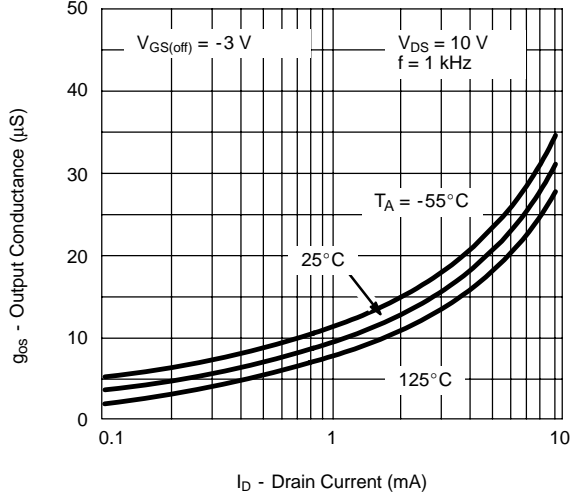
**Common-Source Input Capacitance vs. Gate-Source Voltage**



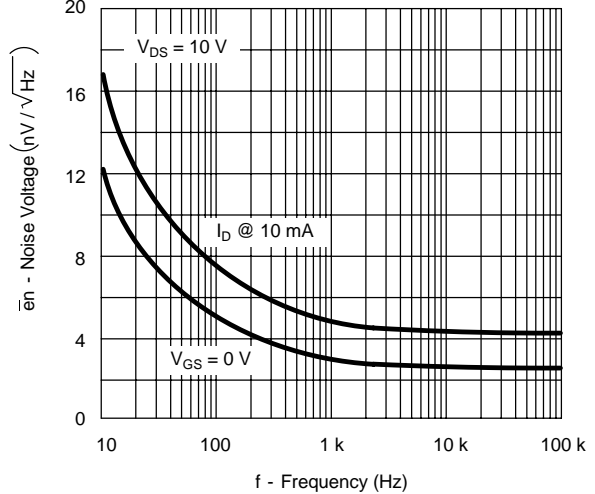
**Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage**



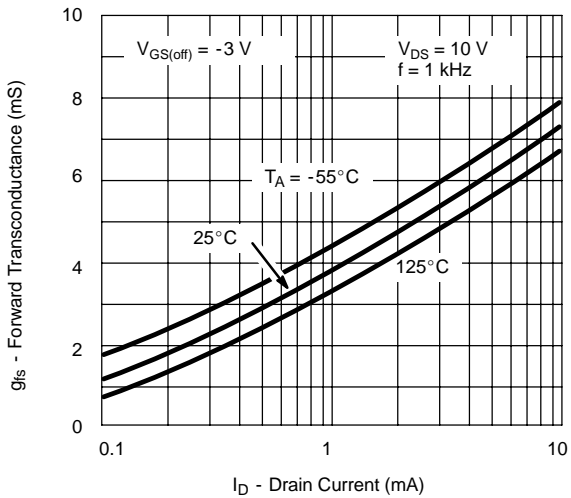
**Output Conductance vs. Drain Current**



**Equivalent Input Noise Voltage vs. Frequency**



**Common-Source Forward Transconductance vs. Drain Current**



**On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage**

