N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY			
$V_{DS(min)}$ (V)	$R_{DS(on)}$ (Ω)	$V_{GS(th)}$ (V)	I_D (mA)
60	1.40 at V_{GS} = 10 V	1 to 2.5	500

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- Low On-Resistance: 1.40 Ω
- Low Threshold: 2 V (typ.)
- Low Input Capacitance: 30 pF
- Fast Switching Speed: 15 ns (typ.)
- Low Input and Output Leakage
- ESD Protected: 2000 V
- Miniature Package
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE

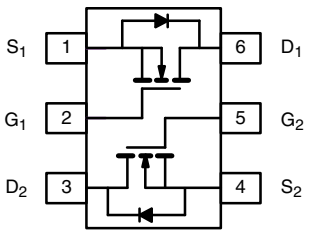
BENEFITS

- Low Offset Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Error Voltage
- Small Board Area

APPLICATIONS

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc.
- Battery Operated Systems
- Solid-State Relays

SC-89



Top View

Marking Code: E

Ordering Information: Si1026X-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)					
Parameter		**Symbol**	**5 s**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	60		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	320	305	mA
	T_A = 85 °C		230	220	
Pulsed Drain Current[b]		I_{DM}	- 650		
Continuous Source Current (Diode Conduction)[a]		I_S	450	380	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	280	250	mW
	T_A = 85 °C		145	130	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C
Gate-Source ESD Rating (HBM, Method 3015)		ESD	2000		V

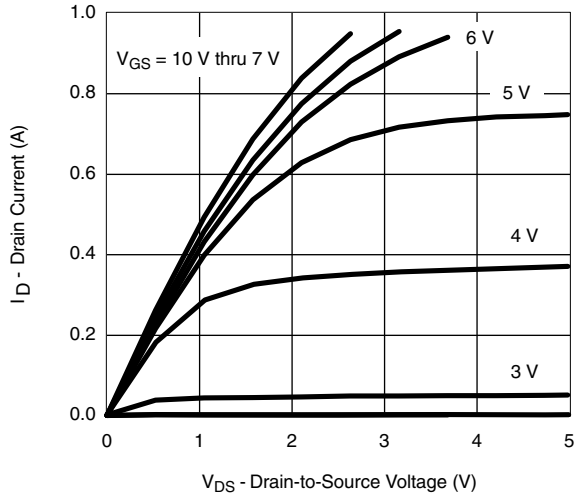
Notes:
a. Surface mounted on FR4 board.
b. Pulse width limited by maximum junction temperature.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 10 µA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 0.25 mA	1		2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 10 V			± 150	nA
		V_{DS} = 0 V, V_{GS} = ± 5 V			± 50	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			1	µA
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 85 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	500			mA
		V_{DS} = 7.5 V, V_{GS} = 10 V	800			
Drain-Source On-Resistance[a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 200 mA			3.0	Ω
		V_{GS} = 10 V, I_D = 500 mA			1.40	
		V_{GS} = 10 V, I_D = 500 mA, T_J = 125 °C			2.50	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 200 mA		200		mS
Diode Forward Voltage[a]	V_{SD}	V_{GS} = 0 V, I_S = 200 mA			1.40	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 10 V, I_D = 250 mA, V_{GS} = 4.5 V		600		pC
Gate-Source Charge	Q_{gs}			120		
Gate-Drain Charge	Q_{gd}			225		
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz		30		pF
Output Capacitance	C_{oss}			6		
Reverse Transfer Capacitance	C_{rss}			3		
Switching[b, c]						
Turn-On Time	$t_{(on)}$	V_{DD} = 30 V, R_L = 150 Ω, I_D = 200 mA, V_{GEN} = 10 V, R_g = 10 Ω		15		ns
Turn-Off Time	$t_{(off)}$			20		

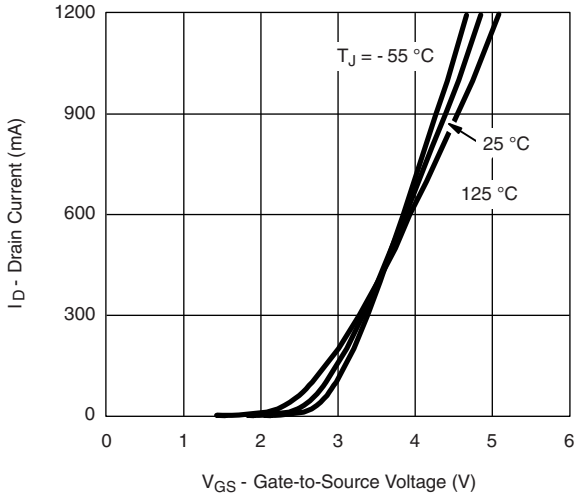
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. For DESIGN AID ONLY, not subject to production testing.
c. Switching time is essentially independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

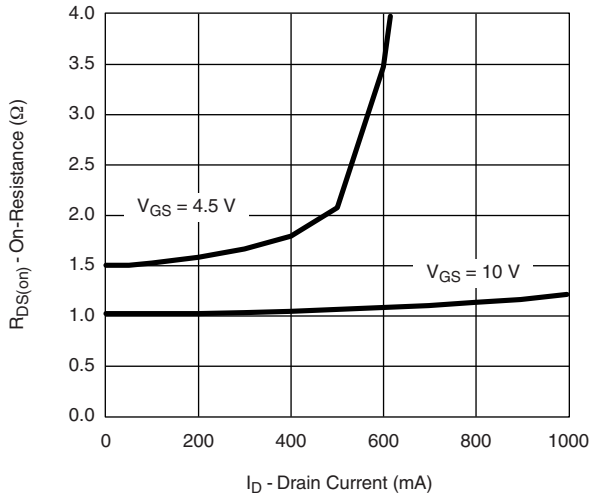
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



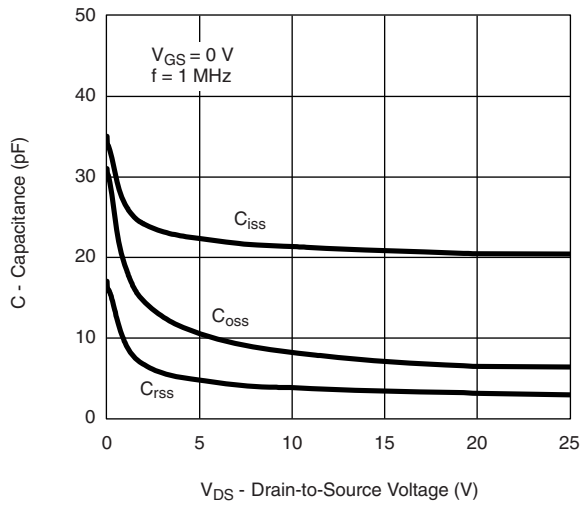
Output Characteristics



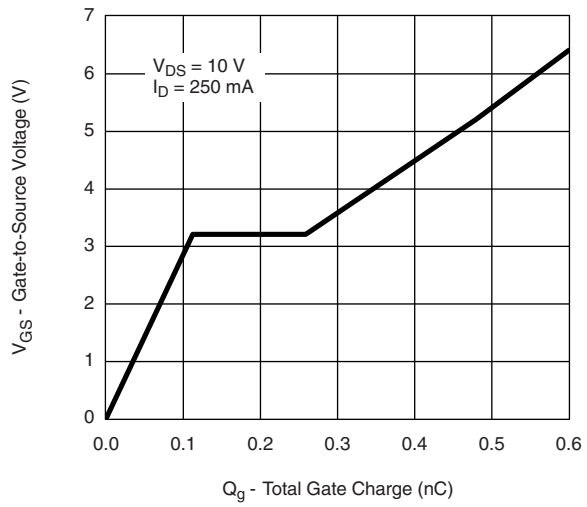
Transfer Characteristics



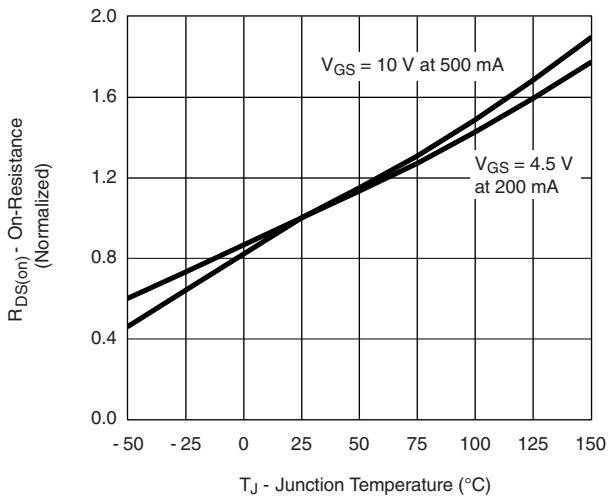
On-Resistance vs. Drain Current



Capacitance

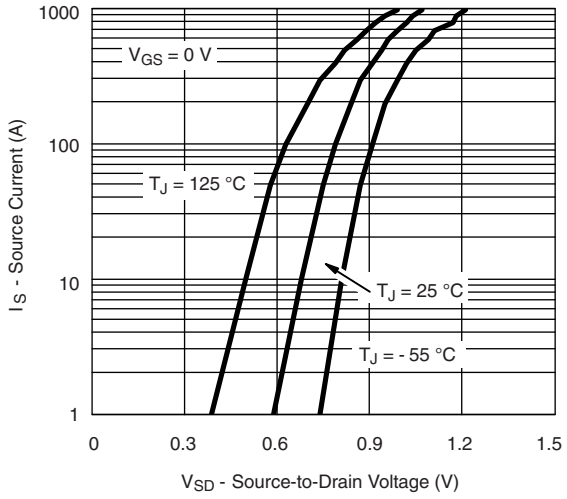


Gate Charge

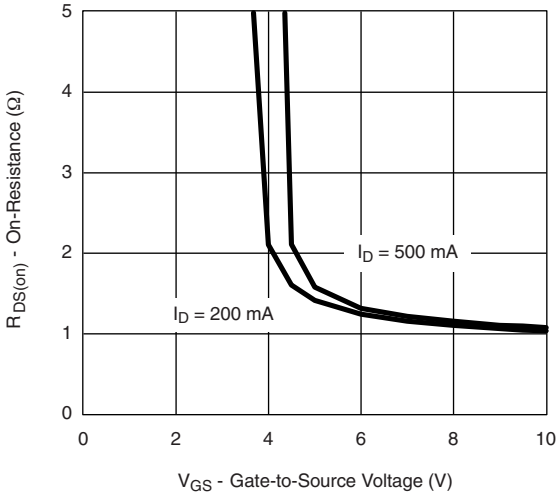


On-Resistance vs. Junction Temperature

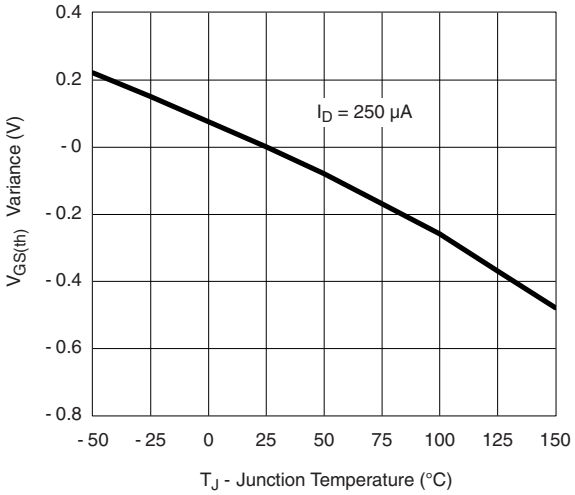
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



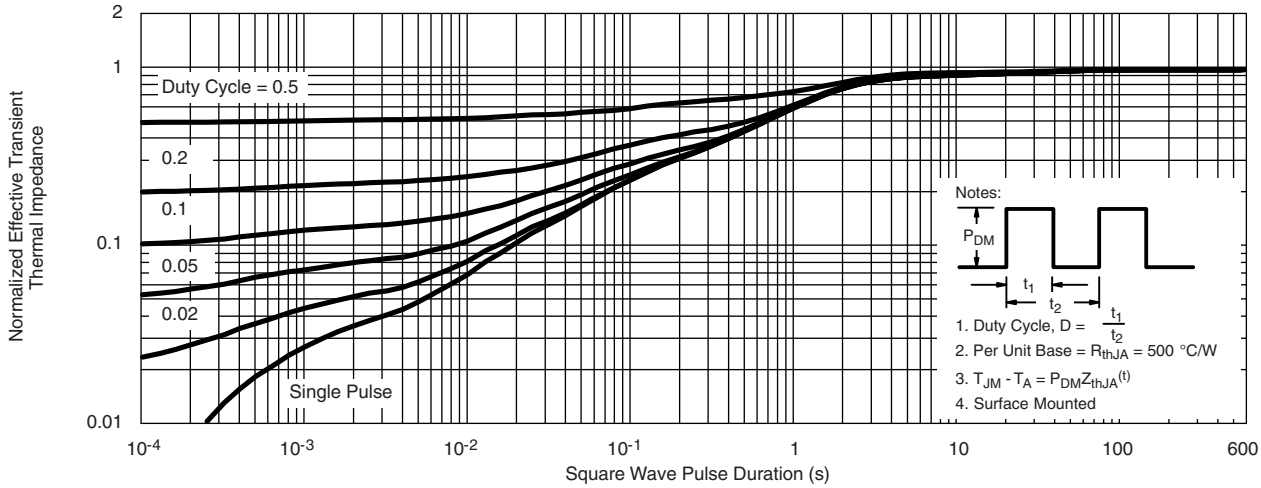
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



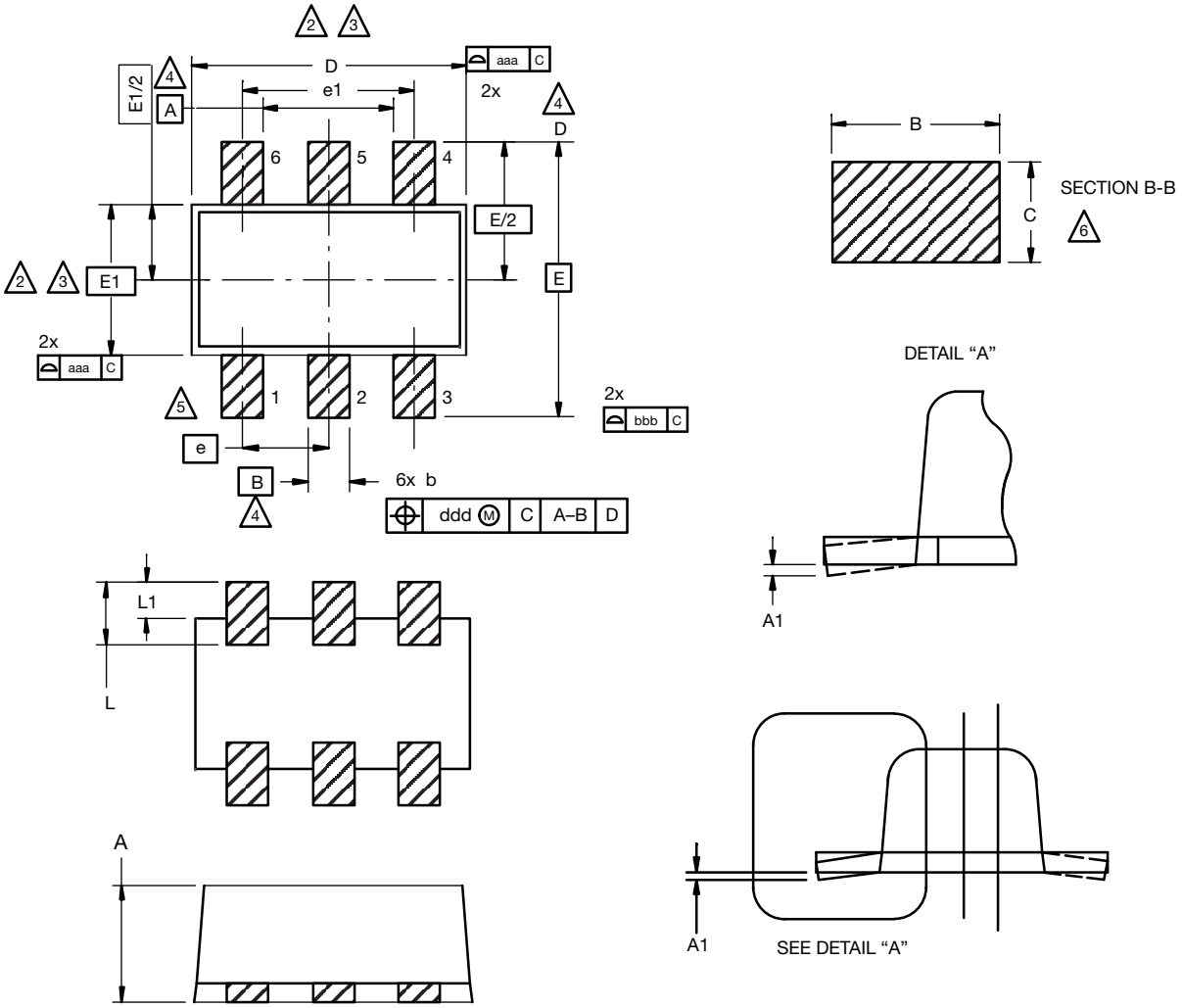
Threshold Voltage Variance Over Temperature



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71434.

SC-89 6-Leads (SOT-563F)



Notes

1. Dimensions in millimeters.

2. Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.

3. Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

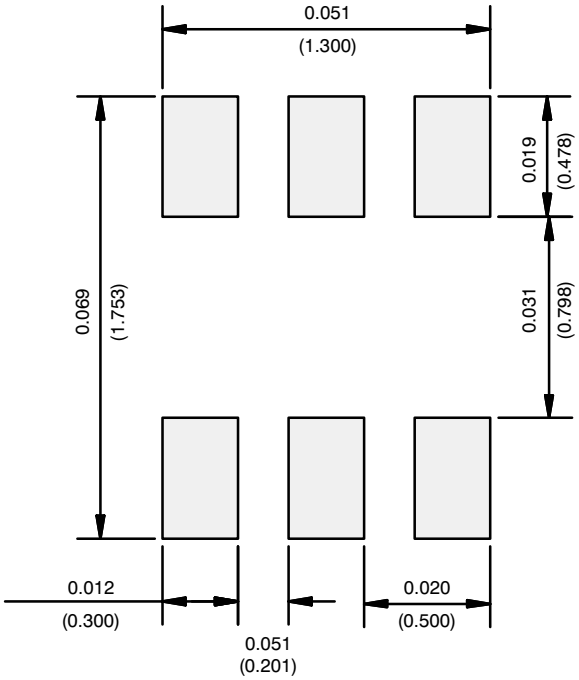
4. Datums A, B and D to be determined 0.10 mm from the lead tip.

5. Terminal numbers are shown for reference only.

6. These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.56	0.58	0.60
A1	0	0.02	0.10
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.50	1.60	1.70
E	1.50	1.60	1.70
E1	1.15	1.20	1.25
e	0.45	0.50	0.55
e1	0.95	1.00	1.05
L	0.25	0.35	0.50
L1	0.10	0.20	0.30
C14-0439-Rev. C, 11-Aug-14 DWG: 5880			

RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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