P-Channel 12-V (D-S) MOSFET

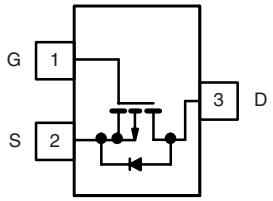
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
- 12	0.051 at V_{GS} = - 4.5 V	- 4.0
	0.070 at V_{GS} = - 2.5 V	- 3.5
	0.106 at V_{GS} = - 1.8 V	- 3.0

FEATURES

- **Halogen-free According to IEC 61249-2-21 Available**
- TrenchFET® Power MOSFETs: 1.8 V Rated

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

TO-236
(SOT-23)



Top View

Si2335DS (E5)*

*Marking Code

Ordering Information: Si2335DS-T1-E3 (Lead (Pb)-free)
Si2335DS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		**Symbol**	**5 s**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	- 12		V
Gate-Source Voltage		V_{GS}	± 8		
Continuous Drain Current (T_J = 150 °C)[a, b]	T_A = 25 °C	I_D	- 4.0	- 3.2	A
	T_A = 70 °C		- 3.3	- 2.6	
Pulsed Drain Current		I_{DM}	- 15		
Continuous Source Current (Diode Conduction)[a, b]		I_S	- 1.6		
Maximum Power Dissipation[a, b]	T_A = 25 °C	P_D	1.25	0.75	W
	T_A = 70 °C		0.8	0.48	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 5 s	R_{thJA}	75	100	°C/W
	Steady State		120	166	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	40	50	

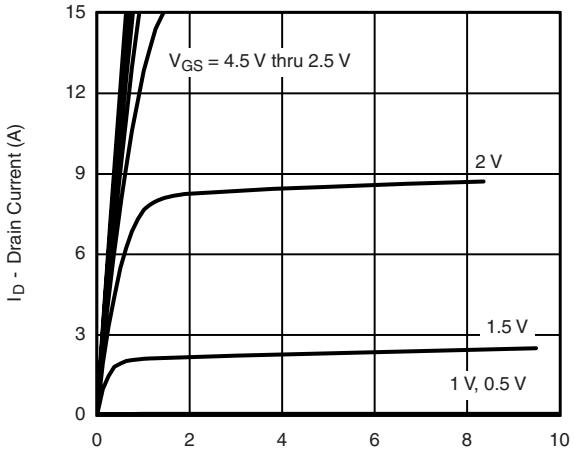
Notes:
a. Surface mounted on 1" x 1" FR4 board.
b. Pulse width limited by maximum junction temperature.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
			Limits			
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 10 µA	- 12			V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 0.45			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 9.6 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 9.6 V, V_{GS} = 0 V, T_J = 55 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ - 5 V, V_{GS} = - 4.5 V	- 15			A
		$V_{DS} \leq$ - 5 V, V_{GS} = - 2.5 V	- 6			
Drain-Source On-Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 4.0 A		0.042	0.051	Ω
		V_{GS} = - 2.5 V, I_D = - 3.5 A		0.058	0.070	
		V_{GS} = - 1.8 V, I_D = - 2.0 A		0.082	0.106	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 5 V, I_D = - 4.0 A		7		S
Diode Forward Voltage	V_{SD}	I_S = - 1.6 A, V_{GS} = 0 V			- 1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = - 6 V, V_{GS} = - 4.5 V, $I_D \cong$ - 4.0 A		9	15	nC
Gate-Source Charge	Q_{gs}			1.9		
Gate-Drain Charge	Q_{gd}			1.5		
Input Capacitance	C_{iss}	V_{DS} = - 6 V, V_{GS} = 0 V, f = 1 MHz		1225		pF
Output Capacitance	C_{oss}			260		
Reverse Transfer Capacitance	C_{rss}			130		
Switching[c]						
Turn-On Time	$t_{d(on)}$	V_{DD} = - 6 V, R_L = 6 Ω $I_D \cong$ - 1.0 A, V_{GEN} = - 4.5 V, R_G = 6 Ω		13.0	20	ns
	t_r			15	25	
Turn-Off Time	$t_{d(off)}$			50	70	
	t_f			19	35	

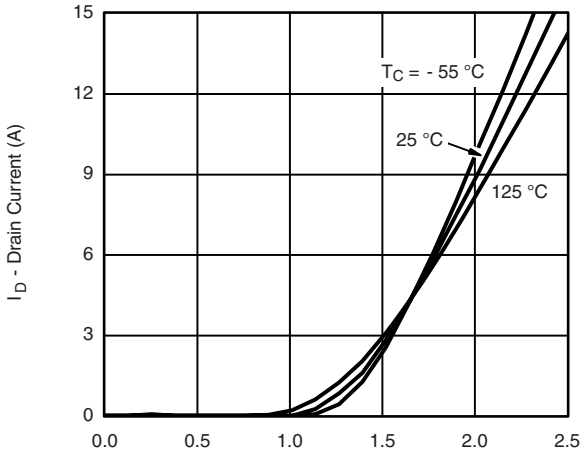
Notes:
a. Pulse test: PW ≤ 300 µs, duty cycle ≤ 2 %.
b. For design aid only, not subject to production testing.
c. Switching time is essentially independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

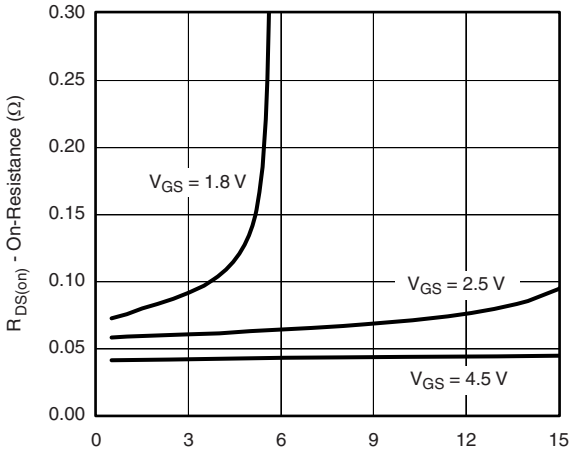
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



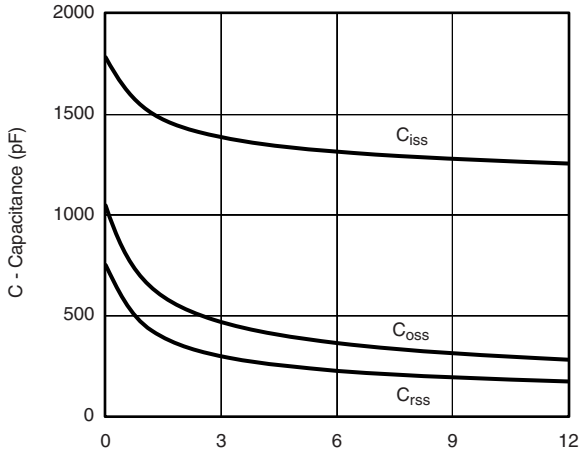
Output Characteristics



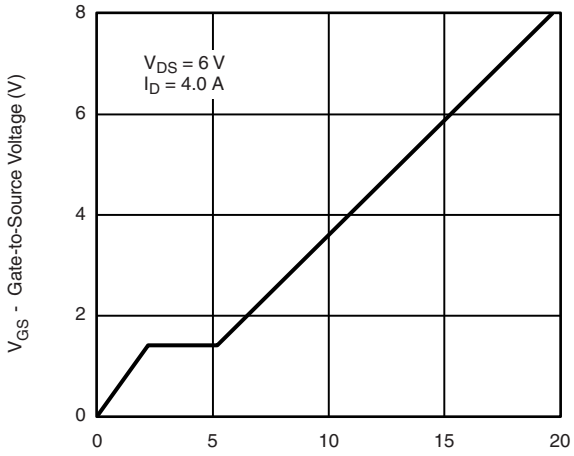
Transfer Characteristics



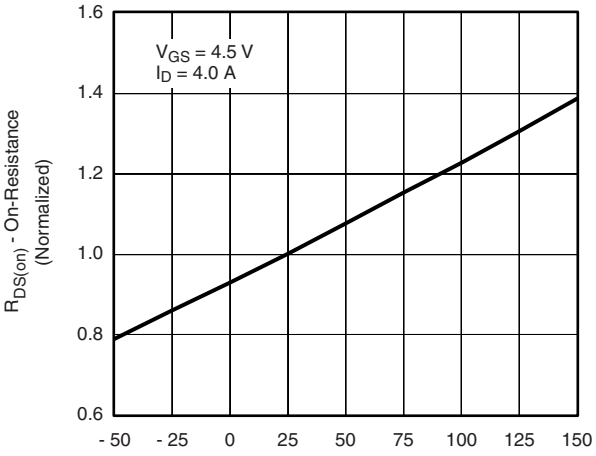
On-Resistance vs. Drain Current



Capacitance

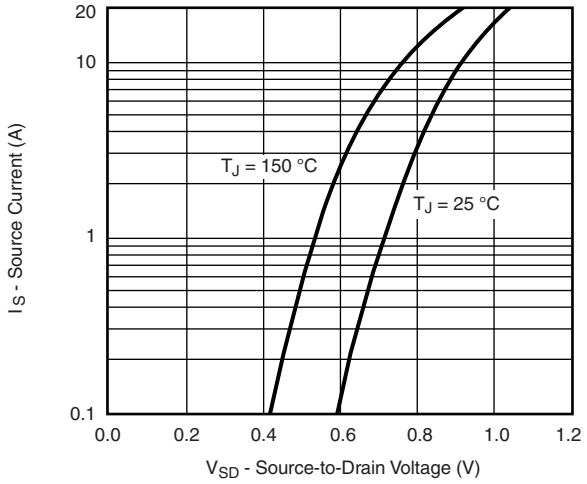


Gate Charge

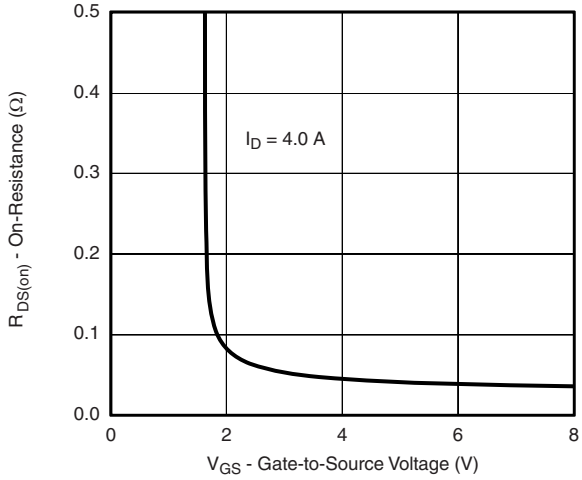


On-Resistance vs. Junction Temperature

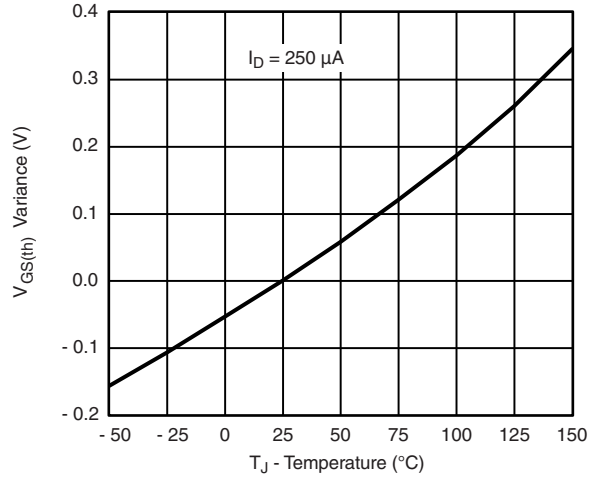
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



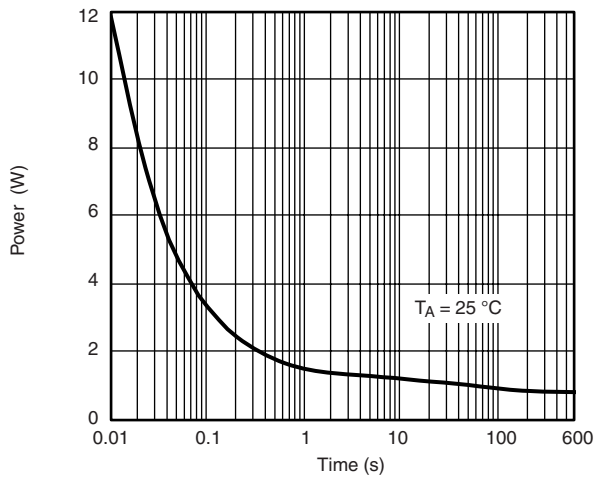
Source-Drain Diode Forward Voltage



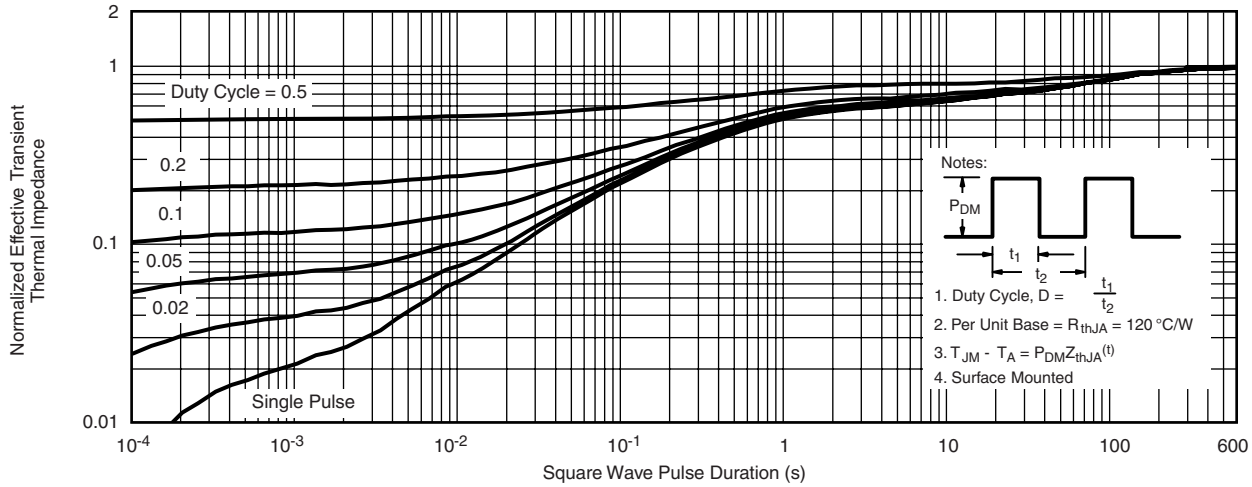
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



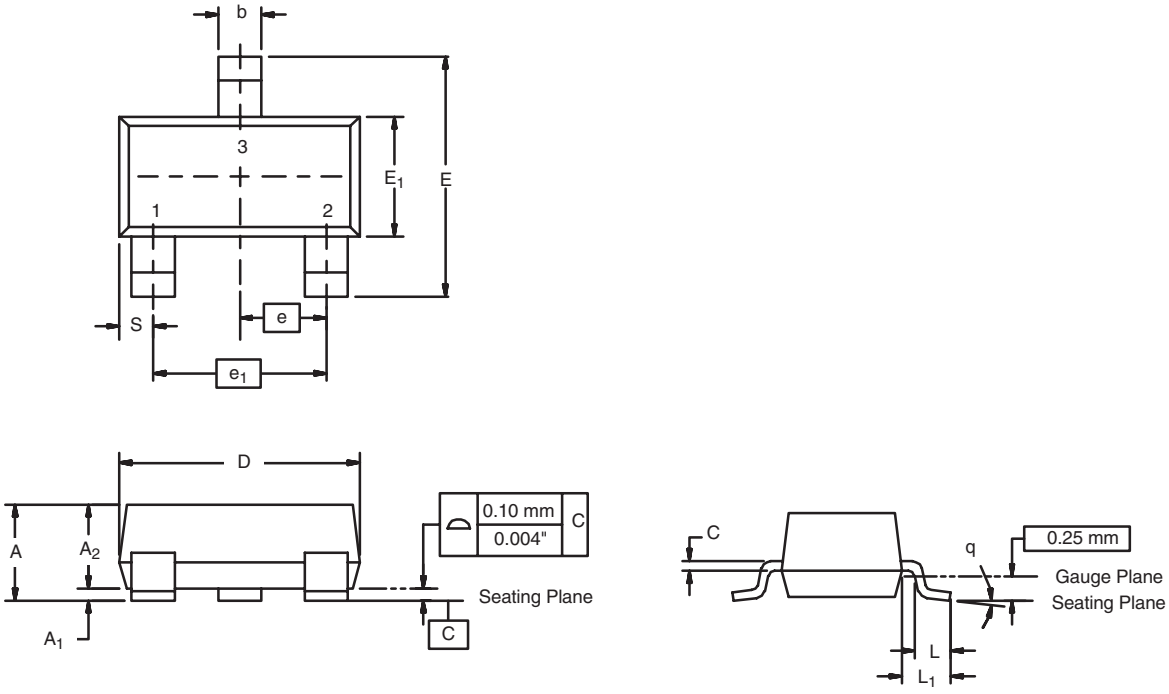
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71314.

SOT-23 (TO-236): 3-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	0.89	1.12	0.035	0.044
A_1	0.01	0.10	0.0004	0.004
A_2	0.88	1.02	0.0346	0.040
b	0.35	0.50	0.014	0.020
c	0.085	0.18	0.003	0.007
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E_1	1.20	1.40	0.047	0.055
e	0.95 BSC		0.0374 Ref	
e_1	1.90 BSC		0.0748 Ref	
L	0.40	0.60	0.016	0.024
L_1	0.64 Ref		0.025 Ref	
S	0.50 Ref		0.020 Ref	
q	3°	8°	3°	8°
ECN: S-03946-Rev. K, 09-Jul-01 DWG: 5479				

Mounting LITTLE FOOT® SOT-23 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/doc?72286), for the basis of the pad design for a LITTLE FOOT SOT-23 power MOSFET footprint . In converting this footprint to the pad set for a power device, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

The electrical connections for the SOT-23 are very simple. Pin 1 is the gate, pin 2 is the source, and pin 3 is the drain. As in the other LITTLE FOOT packages, the drain pin serves the additional function of providing the thermal connection from the package to the PC board. The total cross section of a copper trace connected to the drain may be adequate to carry the current required for the application, but it may be inadequate thermally. Also, heat spreads in a circular fashion from the heat source. In this case the drain pin is the heat source when looking at heat spread on the PC board.

Figure 1 shows the footprint with copper spreading for the SOT-23 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlies the drain pin and provides planar copper to draw heat from the drain lead and start the process of spreading the heat so it can be dissipated into the ambient air. This pattern uses all the available area underneath the body for this purpose.

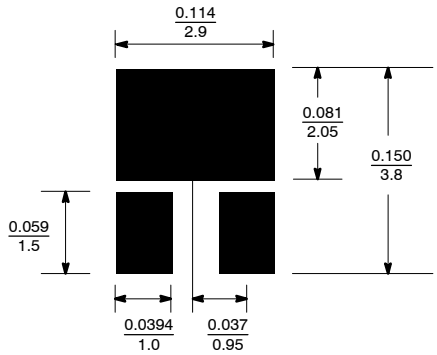
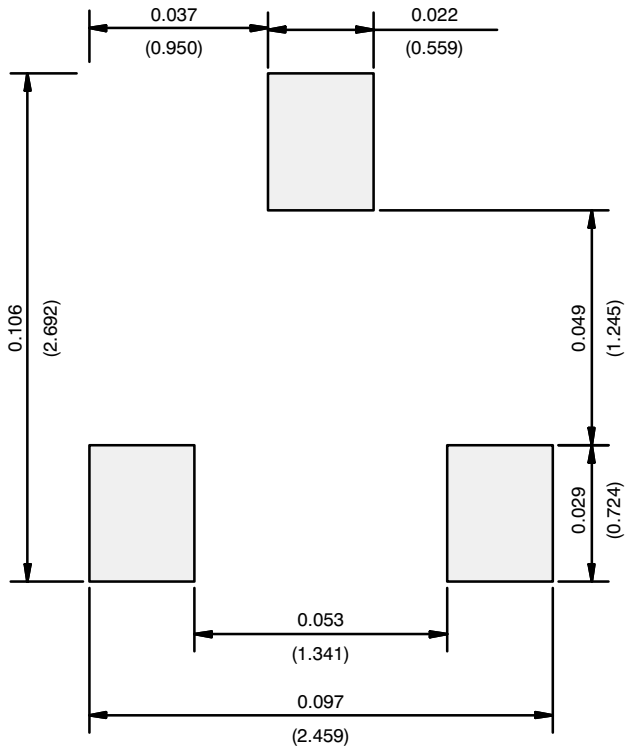


FIGURE 1. Footprint With Copper Spreading

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, “thermal” connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low-impedance path for heat to move away from the device.

RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads
Dimensions in Inches/(mm)

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