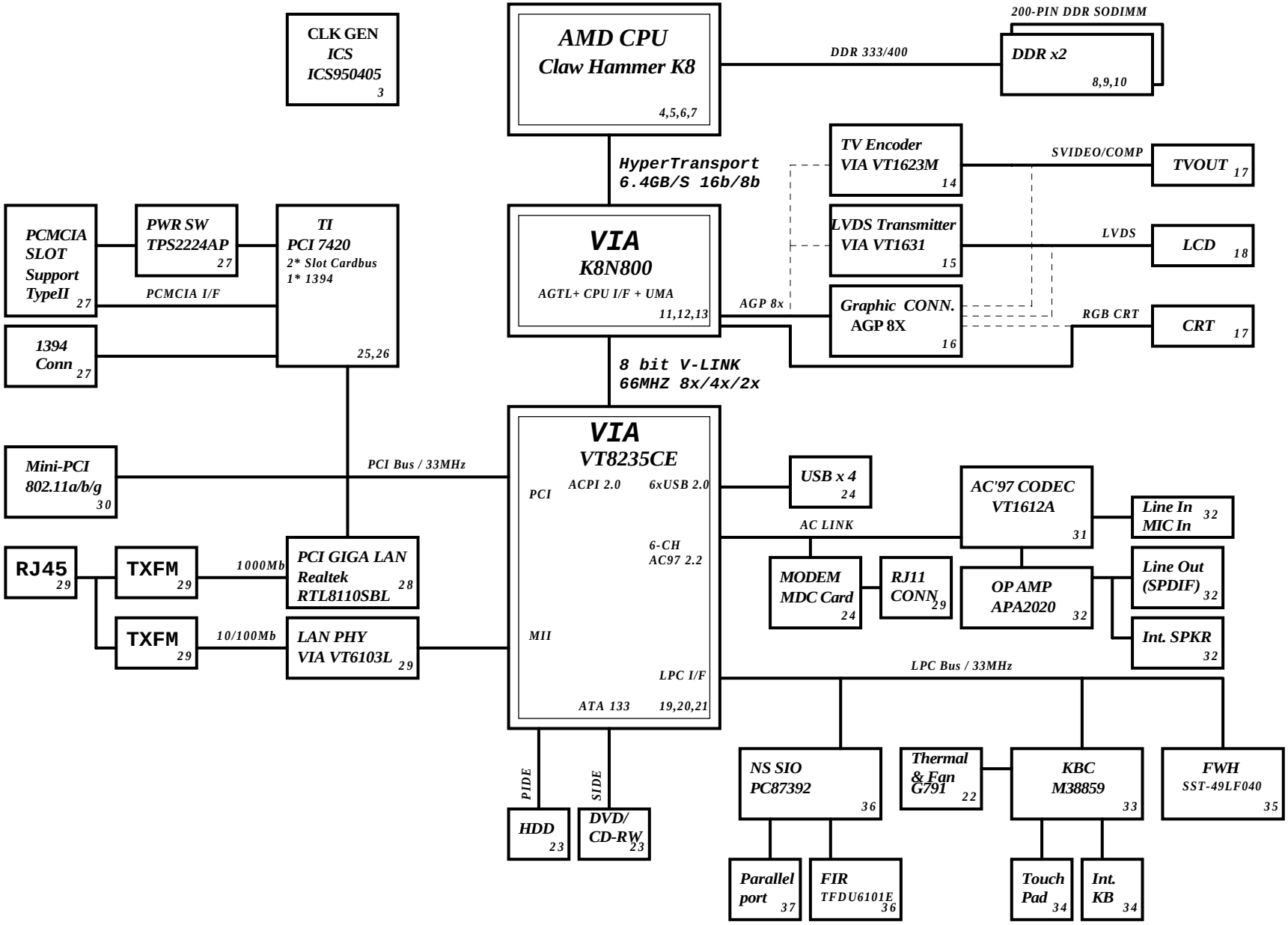
EGRET Block Diagram



PCB Layer Stackup
L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

Battery Charger 46
MAX1645BEEI

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

SYSTEM DC/DC 43
MAX1999

INPUT	OUTPUT
DCBATOUT	5V_S5, 3D3V_S5

SYSTEM DC/DC 44
TPS5110

INPUT	OUTPUT
DCBATOUT 2D5V_S3	2D5V_S3 1D5V_S0

CPU V_CORE 41,42
ISL6559CR

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM POWER 44,45
FDD6035AL/FDS9412-U
FDS9412-U/SI4892DY/LP2951ACM
APL5508-18VC/APL5308-25AC

INPUT	OUTPUT
5V_S3 3D3V_S5 3D3V_S3 3D3V_S0 DCBATOUT	2D5V_S5 5V_S0 3D3V_S3 3D3V_S0 3D3V_LAN_S3 1D8V_S0 +5V_AUX_S5 +5V_UP_S5 2D5V_S0

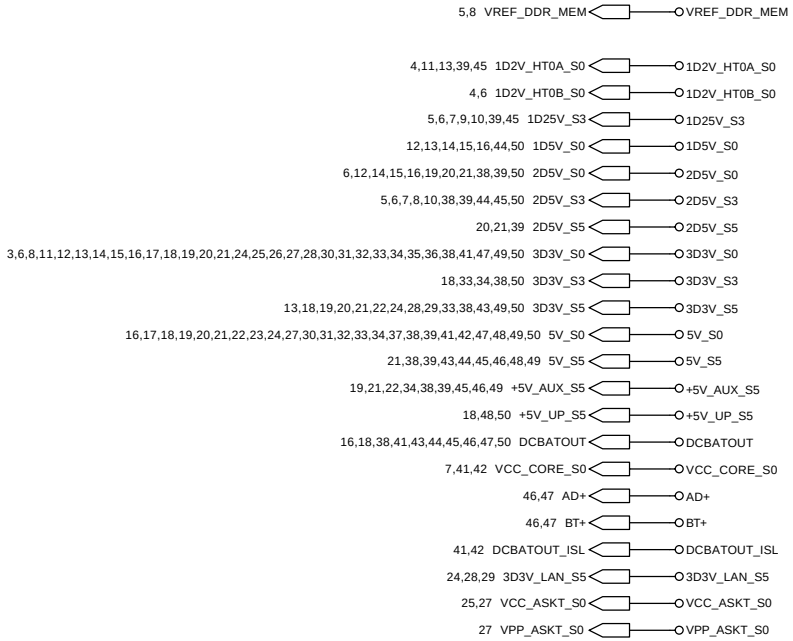
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram		
Size: A3	Document Number: EGRET	Rev: SC
Date: Friday, July 23, 2004	Sheet 1 of 50	

EGRET REVISION HISTORY

PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
VGA & AGP		P_INTA#	
PCI7420-CardBus A	AD22	P_INTB#	P_REQ#1/P_GNT#1
PCI7420-CardBus B	AD22	P_INTC#	P_REQ#1/P_GNT#1
PCI7420-IEEE1394A	AD22	P_INTD#	P_REQ#1/P_GNT#1
Mini-PCI	AD21	P_INTF#	P_REQ#0/P_GNT#0
Giga LAN RTL8110SBL	AD23	P_INTG#	P_REQ#2/P_GNT#2



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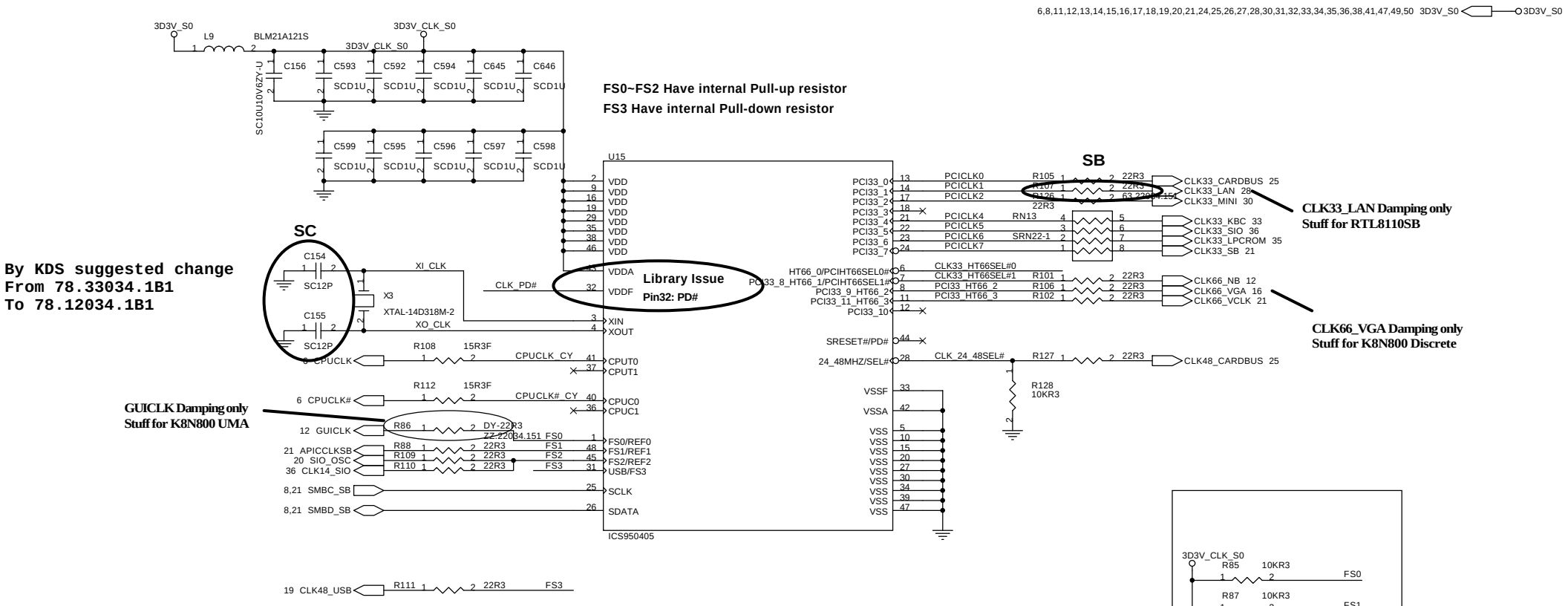
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***REVISION HISTORY***

Size	Document Number	Rev
A3	**EGRET**	SC

Date: Friday, July 23, 2004 Sheet 2 of 50



Input Configuration				Clock Generator Output			
FS3	FS2	FS1	FS0	CPU (MHz)	PCI33_HT66 (MHz)	PCI33 (MHz)	
0	0	0	0	100.90	67.27	33.63	All output Tri-state
0	0	0	1	133.90	66.95	33.48	
0	0	1	0	168.00	67.20	33.60	
0	0	1	1	202.00	67.33	33.67	
0	1	0	0	100.20	66.80	33.40	
0	1	0	1	133.50	66.75	33.38	
0	1	1	0	166.70	66.68	33.34	
* 0	1	1	1	200.40	66.80	33.40	Normal Hammer operation
1	0	0	0	150.00	60.00	30.00	
1	0	0	1	180.00	60.00	30.00	
1	0	1	0	210.00	70.00	35.00	
1	0	1	1	240.00	60.00	30.00	
1	1	0	0	270.00	67.50	33.75	
1	1	0	1	233.33	66.67	33.33	
1	1	1	0	266.67	66.67	33.33	
1	1	1	1	300.00	75.00	37.50	

*	24_48 SEL#	24_48MHz
	0	48MHz
	1	24MHz

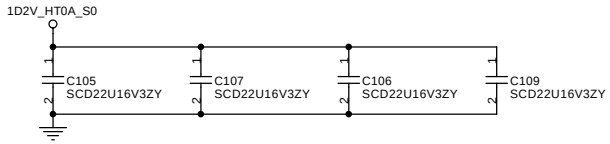
*	PCIHT66 SEL[1:0]#		PCI33_HT66[3:0]		
	SEL0	SEL1	PIN7	PIN8	PIN11
	0	0	HT66	HT66	PCI33
*	0	1	HT66	HT66	HT66
	1	0	PCI33	PCI33	PCI33
	1	1	HT66	PCI33	PCI33

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CLKGEN_ICS950405***

Size: A3 | Document Number: **EGRET** | Rev: SC

Date: Friday, July 23, 2004 | Sheet 3 of 50

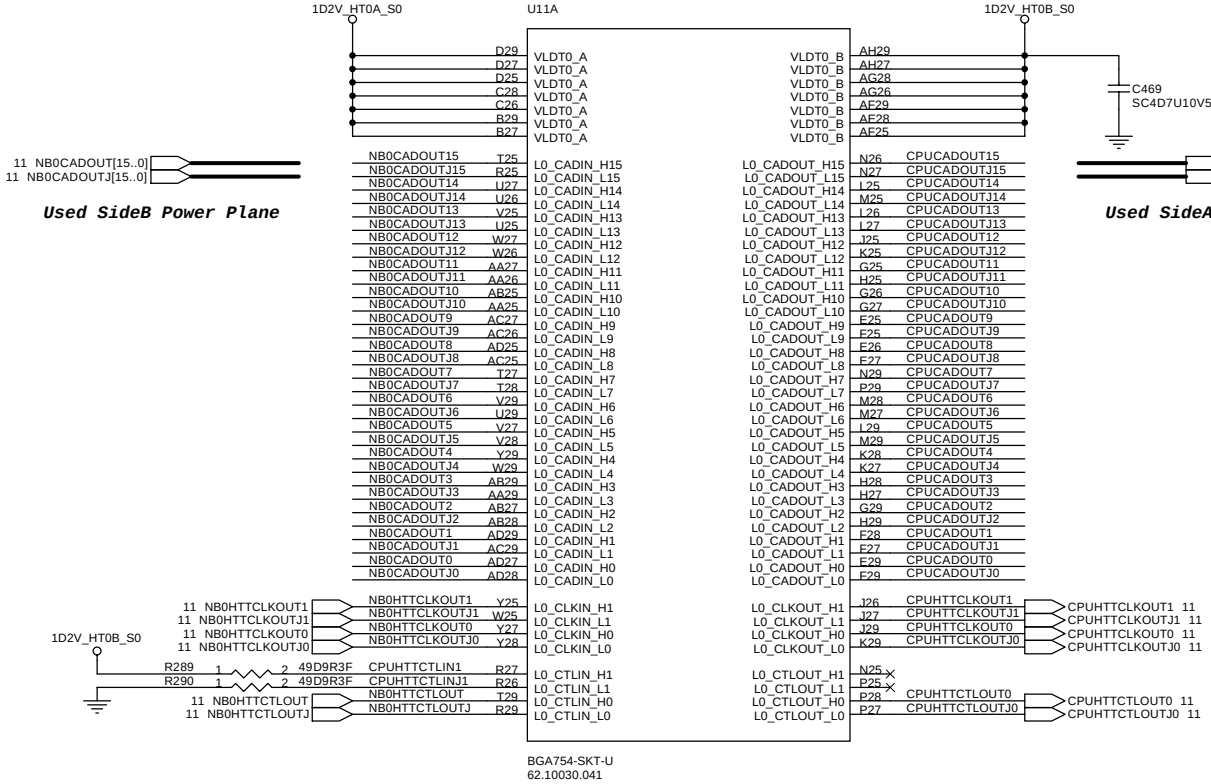


11,13,39,45 1D2V_HT0A_S0 — 1D2V_HT0A_S0

6 1D2V_HT0B_S0 — 1D2V_HT0B_S0

HTT for CPU sideA Transmit power and NB sideA Receive power

HTT for CPU sideB Receive power and NB sideA Transmit power



LAYOUT: Place bypass cap on topside of board near HTT power pins that are not connected directly to downstream HTT device, but connected internally to other HTT power pins.

By ME requset U11 P/N:
Main 62.10030.041
Second 62.10053.191
Third 62.10053.201

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

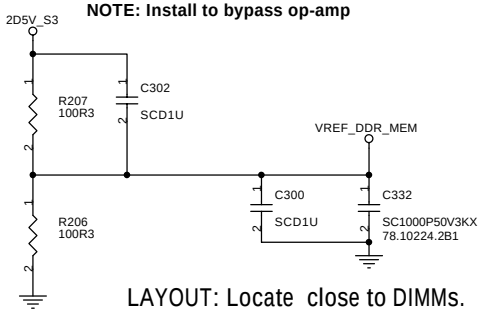
Title: ***CPU(1/4)_HyperTransport I/F***

Size: A3 | Document Number: **EGRET** | Rev: SC

Date: Friday, July 23, 2004 | Sheet 4 of 50

VREF_DDR_MEM

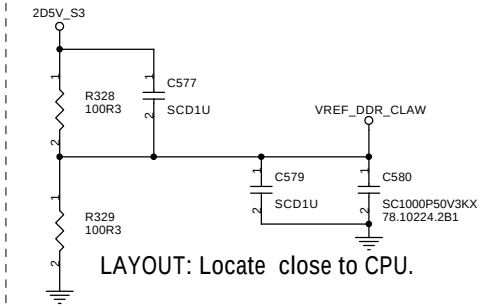
NOTE: Test with passive probes only.
NOTE: Install to bypass op-amp



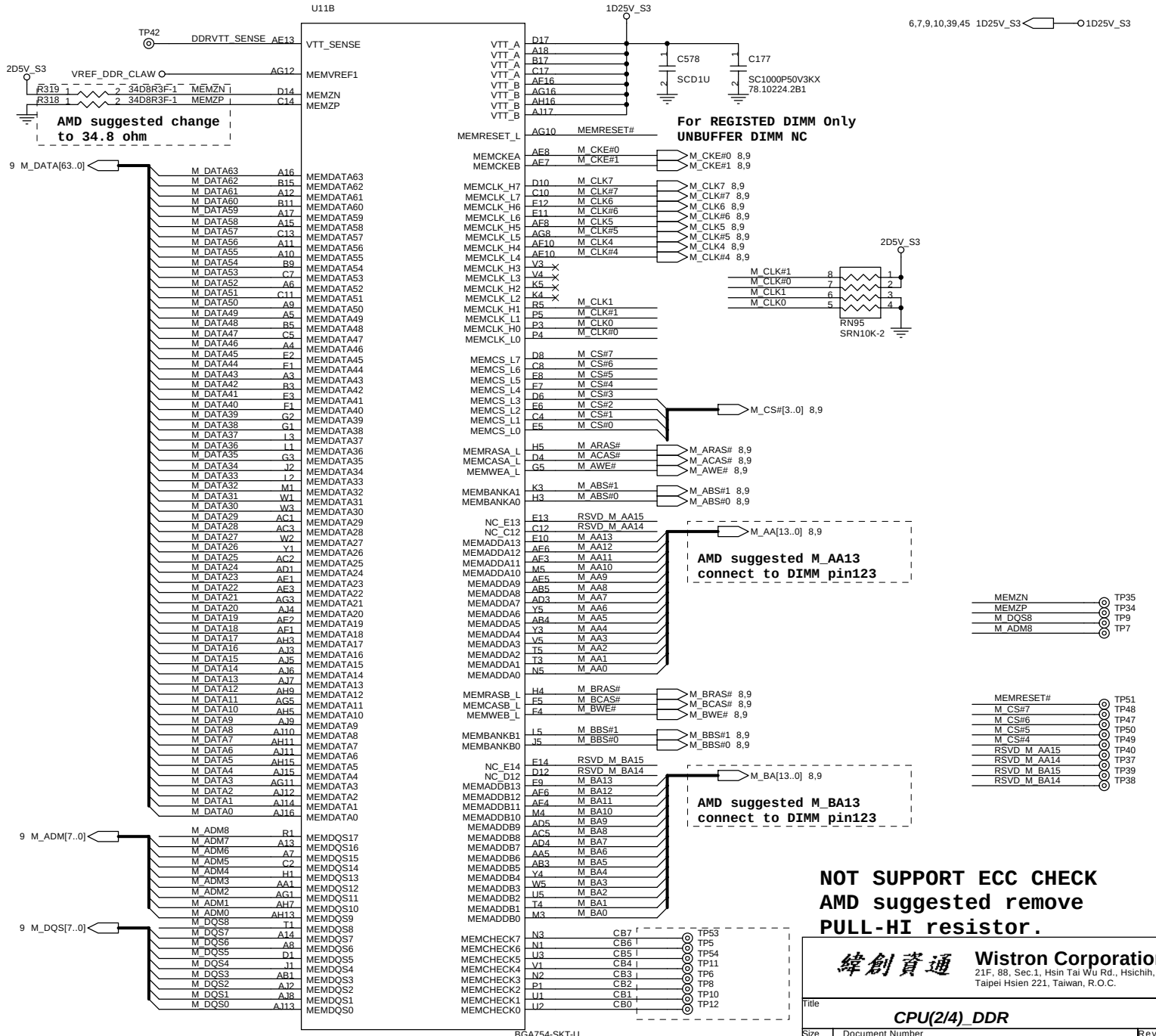
LAYOUT: Locate close to DIMMs.

NOTE: Remove to bypass op-amp

VREF_DDR_CLAW

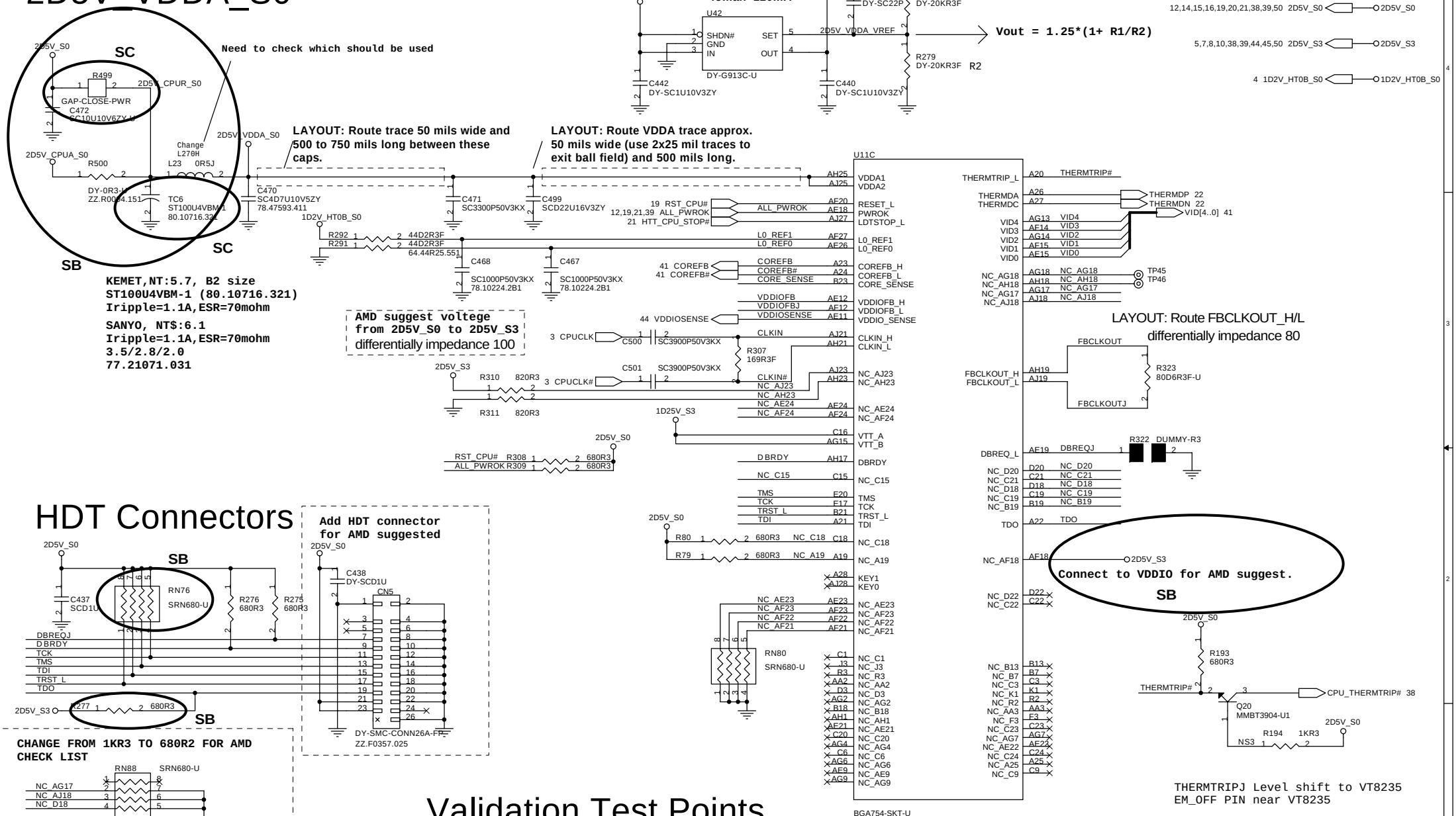


LAYOUT: Locate close to CPU.



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU(2/4)_DDR	
Size: A3	Document Number: EGRET	Rev: SC
Date: Friday, July 23, 2004	Sheet 5 of 50

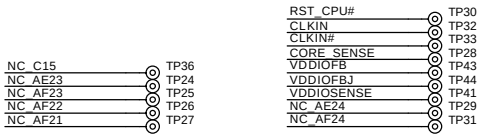
2D5V_VDDA_S0



HDT Connectors

Validation Test Points

LAYOUT: Place close to the CPU.

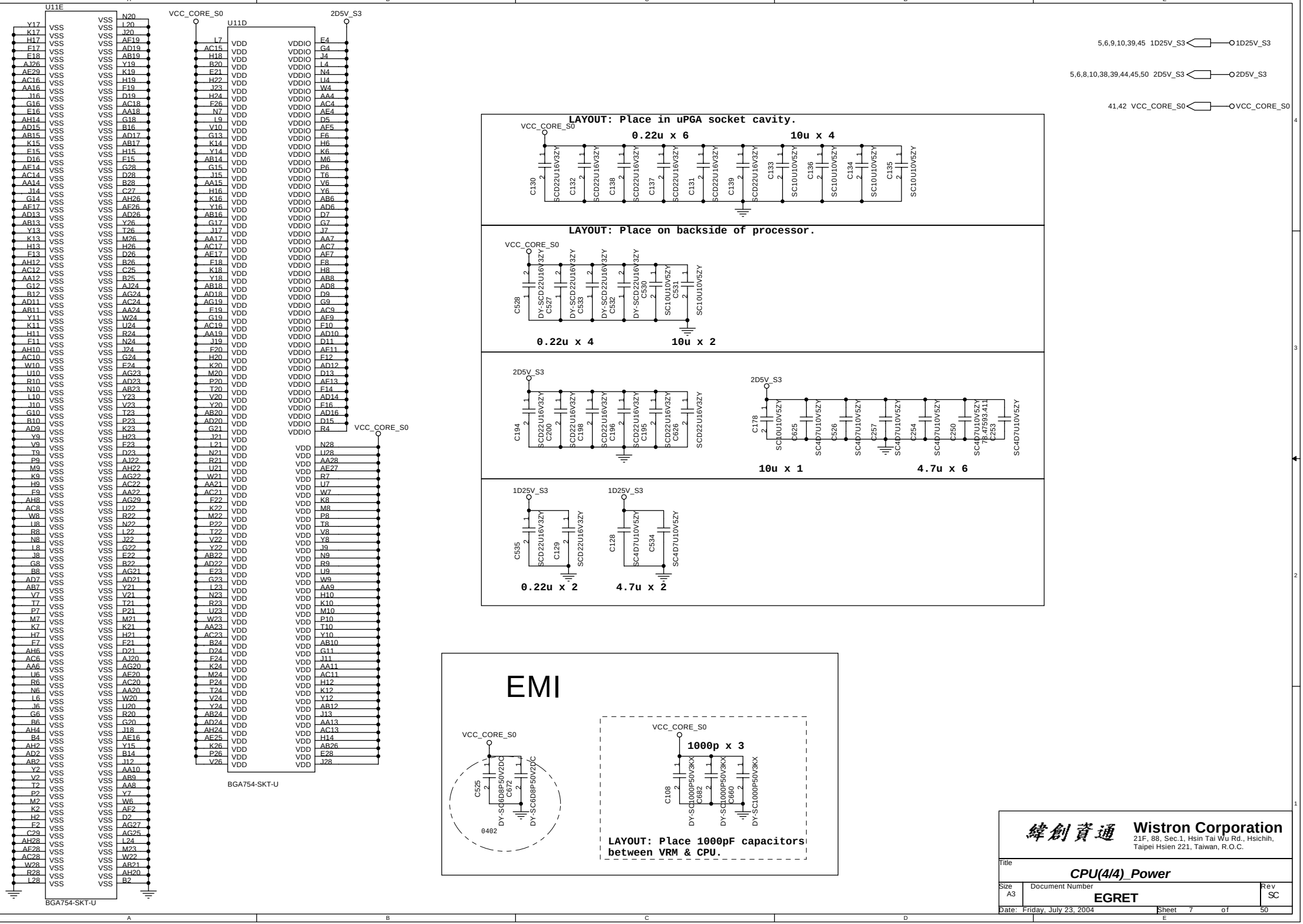


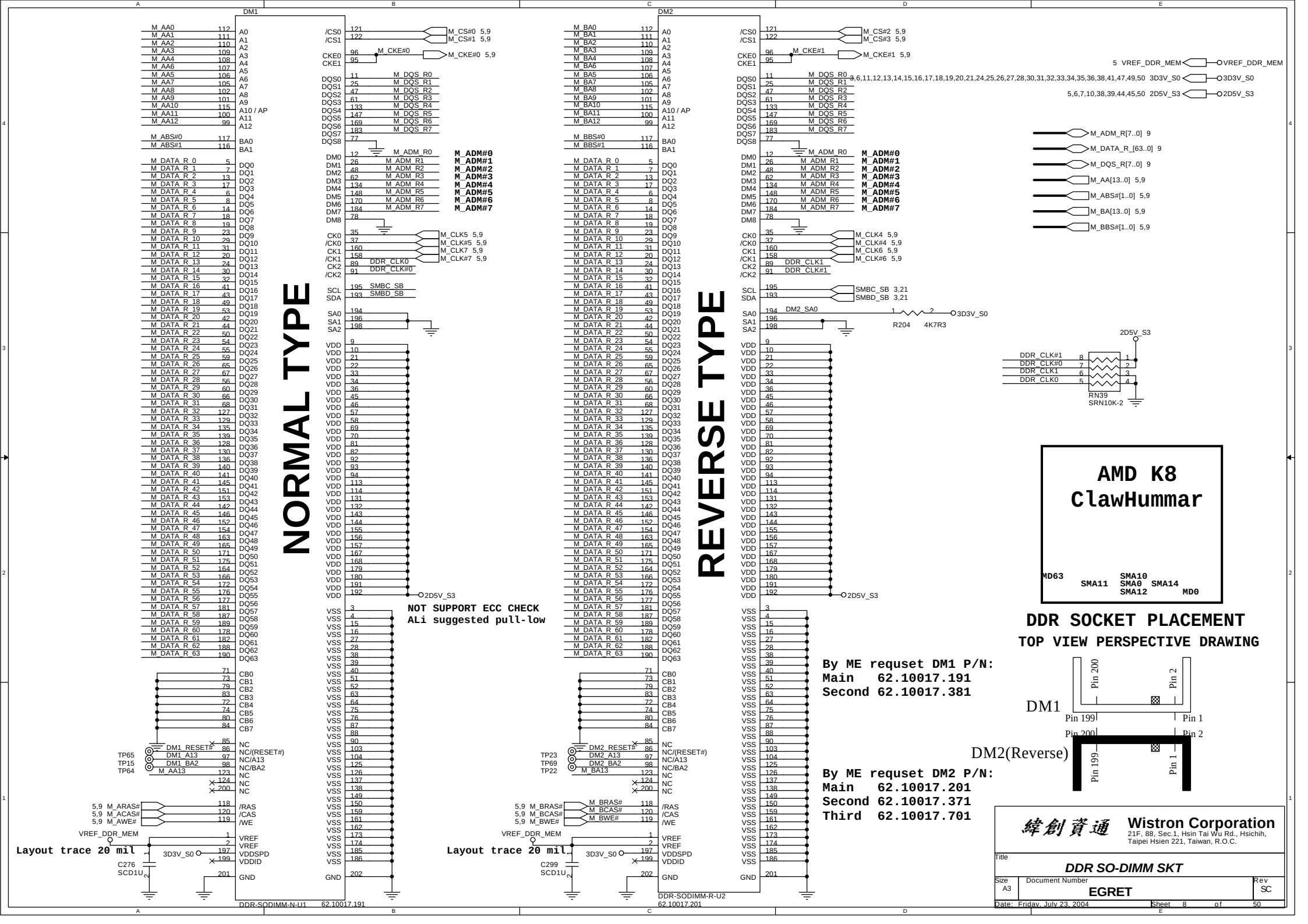
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU(3/4)_Control & Debug*

Size: A3 | Document Number: EGRET | Rev: SC

Date: Friday, July 23, 2004 | Sheet 6 of 50


U11E
VSS
BGA754-SKT-U
VCC_CORE_S0
U11D
VDD
2D5V_S3
VDDIO
BGA754-SKT-U
VCC_CORE_S0
5,6,9,10,39,45 1D25V_S3
1D25V_S3
5,6,8,10,38,39,44,45,50 2D5V_S3
2D5V_S3
41,42 VCC_CORE_S0
VCC_CORE_S0
LAYOUT: Place in uPGA socket cavity.
0.22u x 6
10u x 4
C130
C132
C138
C137
C131
C139
C133
C136
C134
C135
SCD22U16V3ZY
SC10U10V5ZY
LAYOUT: Place on backside of processor.
VCC_CORE_S0
C528
C527
C533
C532
C530
C531
DY-SCD22U16V3ZY
SC10U10V5ZY
0.22u x 4
10u x 2
2D5V_S3
C194
C200
C198
C196
C195
C626
SCD22U16V3ZY
2D5V_S3
C178
C625
C526
C257
C254
C250
C253
SC10U10V5ZY
SC4D7U10V5ZY
10u x 1
4.7u x 6
1D25V_S3
C535
C129
SCD22U16V3ZY
1D25V_S3
C128
C534
SC4D7U10V5ZY
0.22u x 2
4.7u x 2
EMI
VCC_CORE_S0
C525
C672
DY-SC6D8P50V2DC
0402
VCC_CORE_S0
1000p x 3
C108
C682
C660
DY-SC1000P50V3KX
LAYOUT: Place 1000pF capacitors between VRM & CPU.
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU(4/4)_Power
Size
A3
Document Number
EGRET
Rev
SC
Date: Friday, July 23, 2004
Sheet 7 of 50


DM1
NORMAL TYPE
DDR-SODIMM-N-U1 62.10017.191
NOT SUPPORT ECC CHECK
ALi suggested pull-low
Layout trace 20 mil
C276
SCD1U
3D3V_S0
VREF_DDR_MEM
DM2
REVERSE TYPE
DDR-SODIMM-R-U2
62.10017.201
Layout trace 20 mil
C299
SCD1U
3D3V_S0
VREF_DDR_MEM
By ME requset DM1 P/N:
Main 62.10017.191
Second 62.10017.381
By ME requset DM2 P/N:
Main 62.10017.201
Second 62.10017.371
Third 62.10017.701
AMD K8
ClawHummar
MD63
SMA11
SMA10
SMA0
SMA14
SMA12
MD0
DDR SOCKET PLACEMENT
TOP VIEW PERSPECTIVE DRAWING
DM1
Pin 200
Pin 2
Pin 199
Pin 1
DM2(Reverse)
Pin 200
Pin 2
Pin 199
Pin 1
R204 4K7R3
RN39
SRN10K-2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR SO-DIMM SKT
Size A3
Document Number
EGRET
Rev SC
Date: Friday, July 23, 2004
Sheet 8 of 50

SERIES DAMPING

PLACE RNs CLOSE TO FIRST DM (DM1), < 0.75"
STRICT EQUAL LENGTH LIMITATION WITH DQS,
CB PINS

RN23

M_DATA4	1	16	M_DATA_R_4
M_DATA5	2	15	M_DATA_R_5
M_ADM0	3	14	M_ADM_R0
M_DATA6	4	13	M_DATA_R_6
M_DATA7	5	12	M_DATA_R_7
M_DATA13	6	11	M_DATA_R_13
M_DATA12	7	10	M_DATA_R_12
M_ADM1	8	9	M_ADM_R1

SRN10J-3

RN20

M_DATA34	1	16	M_DATA_R_34
M_DATA32	2	15	M_DATA_R_32
M_DQS4	3	14	M_DQS_R4
M_DATA33	4	13	M_DATA_R_33
M_DATA36	5	12	M_DATA_R_36
M_DATA37	6	11	M_DATA_R_37
M_ADM4	7	10	M_ADM_R4
M_DATA39	8	9	M_DATA_R_39

SRN10J-3

RN44

M_DATA1	1	16	M_DATA_R_1
M_DATA0	2	15	M_DATA_R_0
M_DQS0	3	14	M_DQS_R0
M_DATA2	4	13	M_DATA_R_2
M_DATA3	5	12	M_DATA_R_3
M_DATA8	6	11	M_DATA_R_8
M_DATA9	7	10	M_DATA_R_9
M_DQS1	8	9	M_DQS_R1

SRN10J-3

RN32

M_DATA35	1	16	M_DATA_R_35
M_DATA41	2	15	M_DATA_R_41
M_DATA40	3	14	M_DATA_R_40
M_DQS5	4	13	M_DQS_R5
M_DATA42	5	12	M_DATA_R_42
M_DATA43	6	11	M_DATA_R_43
M_DATA49	7	10	M_DATA_R_49
M_DATA48	8	9	M_DATA_R_48

SRN10J-3

RN22

M_DATA14	1	16	M_DATA_R_14
M_DATA15	2	15	M_DATA_R_15
M_DATA21	3	14	M_DATA_R_21
M_DATA20	4	13	M_DATA_R_20
M_ADM2	5	12	M_ADM_R2
M_DATA23	6	11	M_DATA_R_23
M_DATA22	7	10	M_DATA_R_22
M_DATA25	8	9	M_DATA_R_25

SRN10J-3

RN19

M_DATA38	1	16	M_DATA_R_38
M_DATA45	2	15	M_DATA_R_45
M_DATA44	3	14	M_DATA_R_44
M_ADM5	4	13	M_ADM_R5
M_DATA47	5	12	M_DATA_R_47
M_DATA46	6	11	M_DATA_R_46
M_DATA53	7	10	M_DATA_R_53
M_DATA52	8	9	M_DATA_R_52

SRN10J-3

RN42

M_DATA11	1	16	M_DATA_R_11
M_DATA10	2	15	M_DATA_R_10
M_DATA17	3	14	M_DATA_R_17
M_DATA16	4	13	M_DATA_R_16
M_DQS2	5	12	M_DQS_R2
M_DATA19	6	11	M_DATA_R_19
M_DATA18	7	10	M_DATA_R_18
M_DATA24	8	9	M_DATA_R_24

SRN10J-3

RN29

M_DQS6	1	16	M_DQS_R6
M_DATA50	2	15	M_DATA_R_50
M_DATA51	3	14	M_DATA_R_51
M_DATA56	4	13	M_DATA_R_56
M_DATA57	5	12	M_DATA_R_57
M_DQS7	6	11	M_DQS_R7
M_DATA58	7	10	M_DATA_R_58
M_DATA59	8	9	M_DATA_R_59

SRN10J-3

RN21

M_DATA29	1	16	M_DATA_R_29
M_DATA28	2	15	M_DATA_R_28
M_DQS3	3	14	M_DQS_R3
M_ADM3	4	13	M_ADM_R3
M_DATA26	5	12	M_DATA_R_26
M_DATA27	6	11	M_DATA_R_27
M_DATA30	7	10	M_DATA_R_30
M_DATA31	8	9	M_DATA_R_31

SRN10J-3

RN18

M_ADM6	1	16	M_ADM_R6
M_DATA54	2	15	M_DATA_R_54
M_DATA55	3	14	M_DATA_R_55
M_DATA61	4	13	M_DATA_R_61
M_DATA60	5	12	M_DATA_R_60
M_ADM7	6	11	M_ADM_R7
M_DATA62	7	10	M_DATA_R_62
M_DATA63	8	9	M_DATA_R_63

SRN10J-3

5,8 M_CKE#0 — M_CKE#0

5,8 M_CKE#1 — M_CKE#1

05/10
Remove the damping resistor for AMD suggest.

PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO SECOND DM (DM2)
NO EQUAL LENGTH LIMITATION

1D25V_S3

RN45

M_ADM_R1	1	16	M_DATA_R_13
M_DATA_R_13	2	15	M_DATA_R_12
M_DATA_R_12	3	14	M_DATA_R_6
M_DATA_R_6	4	13	M_DATA_R_7
M_DATA_R_7	5	12	M_ADM_R0
M_ADM_R0	6	11	M_DATA_R_5
M_DATA_R_5	7	10	M_DATA_R_4
M_DATA_R_4	8	9	M_DATA_R_39

SRN68J-1

RN33

1	16	M_DATA_R_36
2	15	M_DATA_R_32
3	14	M_DATA_R_37
4	13	M_DATA_R_33
5	12	M_ADM_R4
6	11	M_DQS_R4
7	10	M_DATA_R_38
8	9	M_DATA_R_39

SRN68J-1

RN65

M_DATA_R_1	1	16	M_DATA_R_0
M_DATA_R_0	2	15	M_DQS_R0
M_DQS_R0	3	14	M_DATA_R_2
M_DATA_R_2	4	13	M_DATA_R_3
M_DATA_R_3	5	12	M_DATA_R_8
M_DATA_R_8	6	11	M_DATA_R_9
M_DATA_R_9	7	10	M_DQS_R1
M_DQS_R1	8	9	

SRN68J-1

RN61

1	16	M_DATA_R_48
2	15	M_DATA_R_49
3	14	M_DATA_R_43
4	13	M_DATA_R_42
5	12	M_DQS_R5
6	11	M_DATA_R_41
7	10	M_DATA_R_40
8	9	M_DATA_R_34

SRN68J-1

RN43

M_DATA_R_25	1	16	M_DATA_R_22
M_DATA_R_22	2	15	M_DATA_R_23
M_DATA_R_23	3	14	M_ADM_R2
M_ADM_R2	4	13	M_DATA_R_20
M_DATA_R_20	5	12	M_DATA_R_21
M_DATA_R_21	6	11	M_DATA_R_14
M_DATA_R_14	7	10	M_DATA_R_15
M_DATA_R_15	8	9	

SRN68J-1

RN31

1	16	M_DATA_R_35
2	15	M_DATA_R_46
3	14	M_DATA_R_47
4	13	M_ADM_R5
5	12	M_DATA_R_44
6	11	M_DATA_R_45
7	10	M_DATA_R_53
8	9	M_DATA_R_52

SRN68J-1

RN64

M_DATA_R_11	1	16	M_DATA_R_10
M_DATA_R_10	2	15	M_DATA_R_16
M_DATA_R_16	3	14	M_DATA_R_17
M_DATA_R_17	4	13	M_DQS_R2
M_DQS_R2	5	12	M_DATA_R_19
M_DATA_R_19	6	11	M_DATA_R_18
M_DATA_R_18	7	10	M_DATA_R_24
M_DATA_R_24	8	9	

SRN68J-1

RN60

1	16	M_DATA_R_59
2	15	M_DATA_R_58
3	14	M_DQS_R7
4	13	M_DATA_R_57
5	12	M_DATA_R_56
6	11	M_DATA_R_51
7	10	M_DATA_R_50
8	9	M_DQS_R6

SRN68J-1

RN41

M_DATA_R_30	1	16	M_DATA_R_31
M_DATA_R_31	2	15	M_DATA_R_26
M_DATA_R_26	3	14	M_DATA_R_27
M_DATA_R_27	4	13	M_ADM_R3
M_ADM_R3	5	12	M_DQS_R3
M_DQS_R3	6	11	M_DATA_R_29
M_DATA_R_29	7	10	M_DATA_R_28
M_DATA_R_28	8	9	

SRN68J-1

RN30

1	16	M_DATA_R_55
2	15	M_DATA_R_54
3	14	M_ADM_R6
4	13	M_DATA_R_60
5	12	M_DATA_R_61
6	11	M_ADM_R7
7	10	M_DATA_R_63
8	9	M_DATA_R_62

SRN68J-1

1D25V_S3

RN63

M_CKE#1	2	3	
M_BA12	1	4	

SRN47J

RN40

M_CKE#0	2	3	
M_AA12	1	4	

SRN47J

RN37

M_AA11	1	16	
M_AA9	2	15	
M_AA7	3	14	
M_AA5	4	13	
M_AA4	5	12	
M_AA8	6	11	
M_AA6	7	10	
M_AA3	8	9	

SRN47J-1-U

RN36

M_CS#3	1	16	
M_BA13	2	15	
M_CS#2	3	14	
M_BRAS#	4	13	
M_BBS#1	5	12	
M_BCAS#	6	11	
M_BA0	7	10	
M_BA2	8	9	

SRN47J-1-U

RN35

M_AA1	1	16	
M_AA10	2	15	
M_AA2	3	14	
M_AA0	4	13	
M_ABS#1	5	12	
M_ARAS#	6	11	
M_AWE#	7	10	
M_ABS#0	8	9	

SRN47J-1-U

RN62

M_BA7	1	16	
M_BA3	2	15	
M_BA6	3	14	
M_BA9	4	13	
M_BA10	5	12	
M_BA1	6	11	
M_BBS#0	7	10	
M_BWE#	8	9	

SRN47J-1-U

RN38

M_BA5	1	8	
M_BA8	2	7	
M_BA11	3	6	
M_BA4	4	5	

SRN47-1

RN34

M_AA13	1	8	
M_CS#0	2	7	
M_CS#1	3	6	
M_ACAS#	4	5	

SRN47-1

5,6,7,10,39,45 1D25V_S3 — 1D25V_S3

M_ADM_R[7..0] 8
M_ADM[7..0] 5
M_DATA[63..0] 5
M_DATA_R_[63..0] 8
M_DQS[7..0] 5
M_DQS_R[7..0] 8
M_AA[13..0] 5,8
M_ABS#[1..0] 5,8
M_BA[13..0] 5,8
M_BBS#[1..0] 5,8

M_AWE# 5,8
M_ACAS# 5,8
M_ARAS# 5,8

M_BWE# 5,8
M_BCAS# 5,8
M_BRAS# 5,8

M_CS#0 5,8
M_CS#1 5,8
M_CS#2 5,8
M_CS#3 5,8

PLACE BETWEEN DM1, DM2
CLOSE TO FIRST DM (DM 2) < 0.2", TO SECOND DM (DM1) < 1.1"
EQUAL LENGTH LIMITATION WITH SCK/SCK#

R171 121R3F — M_CLK7 — M_CLK7 5,8 / M_CLK#7 5,8

R239 121R3F — M_CLK6 — M_CLK6 5,8 / M_CLK#6 5,8

R205 121R3F — M_CLK5 — M_CLK5 5,8 / M_CLK#5 5,8

R240 121R3F — M_CLK4 — M_CLK4 5,8 / M_CLK#4 5,8

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR DAMPING & TERMINATION***

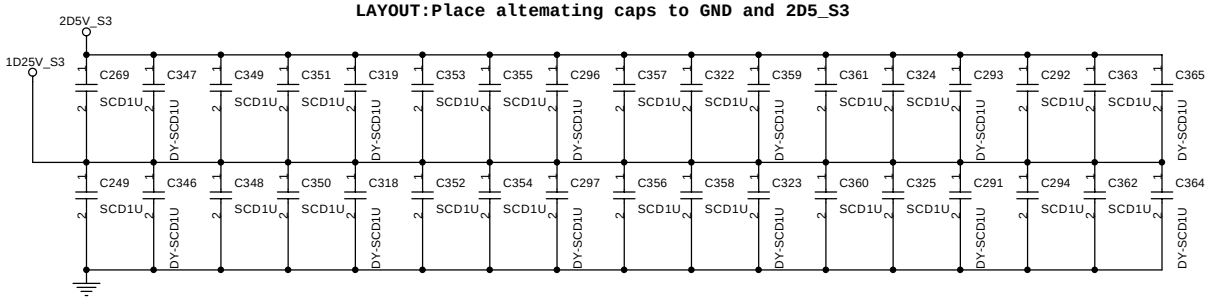
Size	Document Number	Rev
A3	EGRET	SC

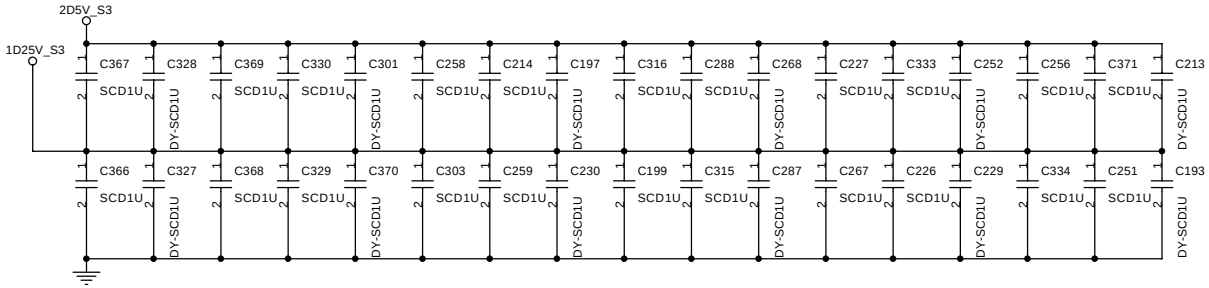
Date: Friday, July 23, 2004 Sheet 9 of 50

5,6,7,8,38,39,44,45,50 2D5V_S3 → 2D5V_S3

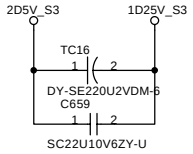
5,6,7,9,39,45 1D25V_S3 → 1D25V_S3

LAYOUT:Place altemating caps to GND and 2D5_S3

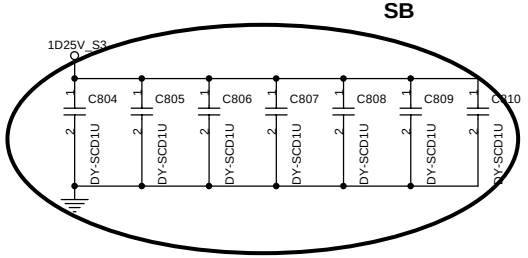




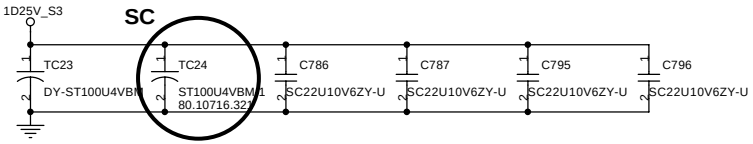
LAYOUT:Locate close to CPU socket.



SB



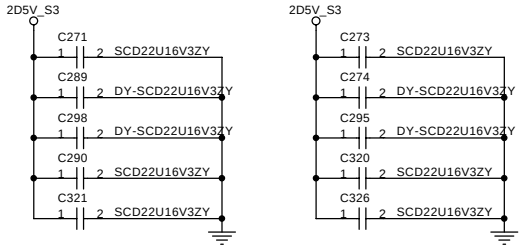
LAYOUT:Place at end of the DIMMs



KEMET,NT:5.7, B2 size
ST100U4VBM-1 (80.10716.321)
Iripple=1.1A,ESR=70mohm

SANYO, NT$:6.1
Iripple=1.1A,ESR=70mohm
3.5/2.8/2.0
77.21071.031

LAYOUT:Place close to Power Pin of DDR socket.

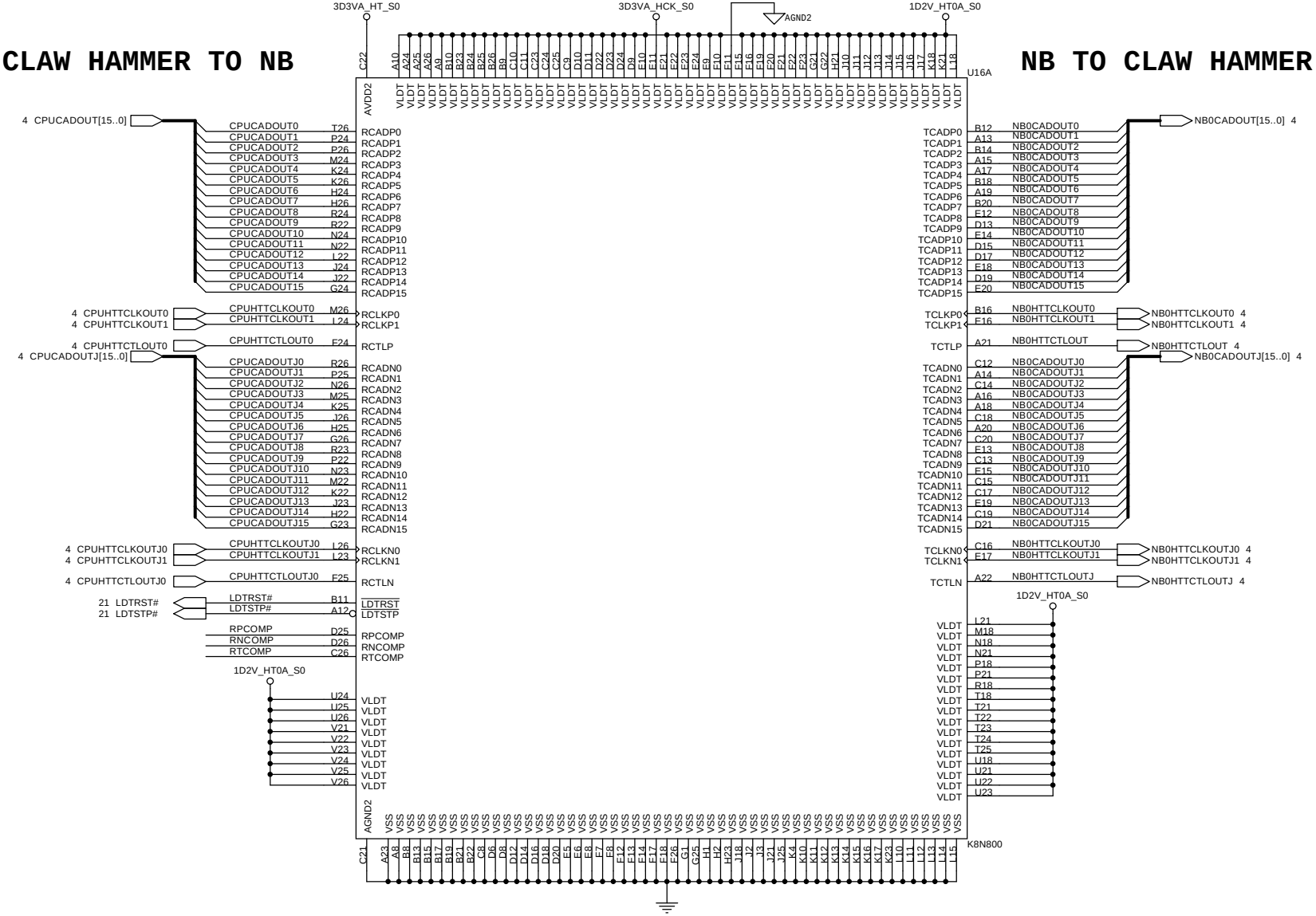


0.22u x 10

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***DDR DECOUPLING***		
Size: A3	Document Number: **EGRET**	Rev: SC
Date: Friday, July 23, 2004	Sheet 10 of 50	

CLAW HAMMER TO NB

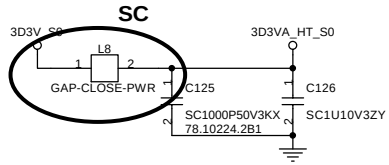
NB TO CLAW HAMMER

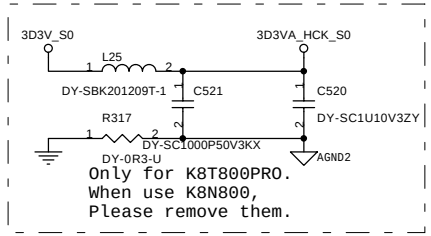


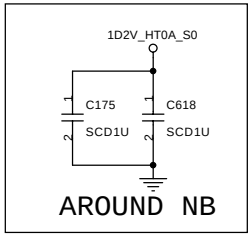
3,6,8,12,13,14,15,16,17,18,19,20,21,24,25,26,27,28,30,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0 — 3D3V_S0

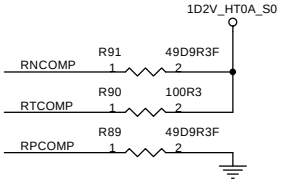
4,13,39,45 1D2V_HT0A_S0 — 1D2V_HT0A_S0

6,12,14,15,16,19,20,21,38,39,50 2D5V_S0 — 2D5V_S0

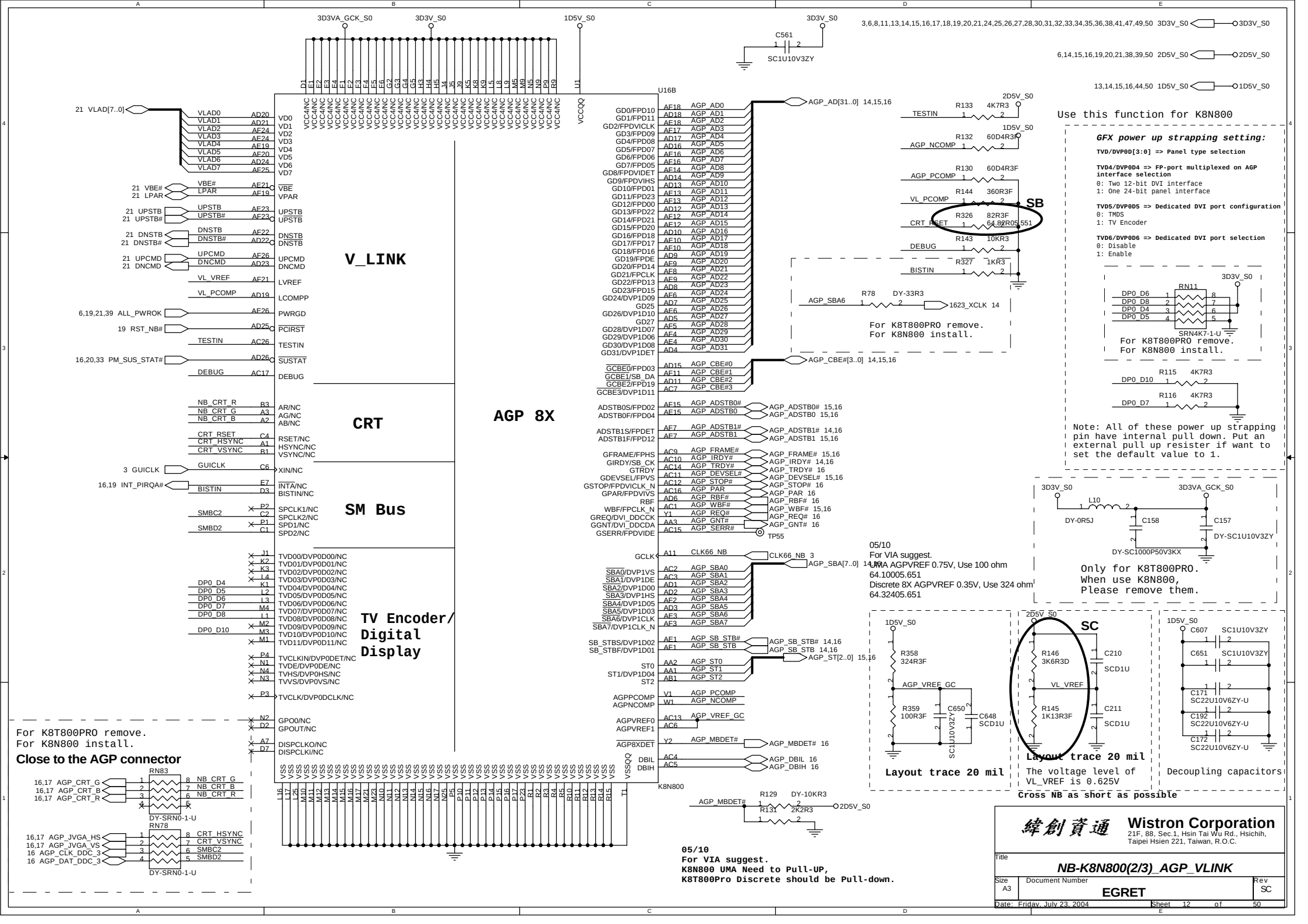




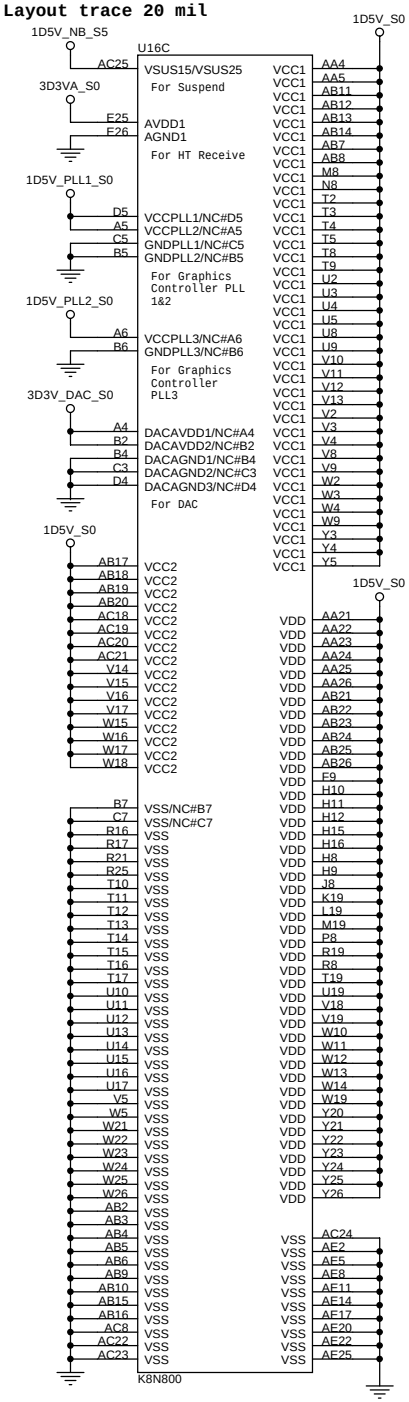




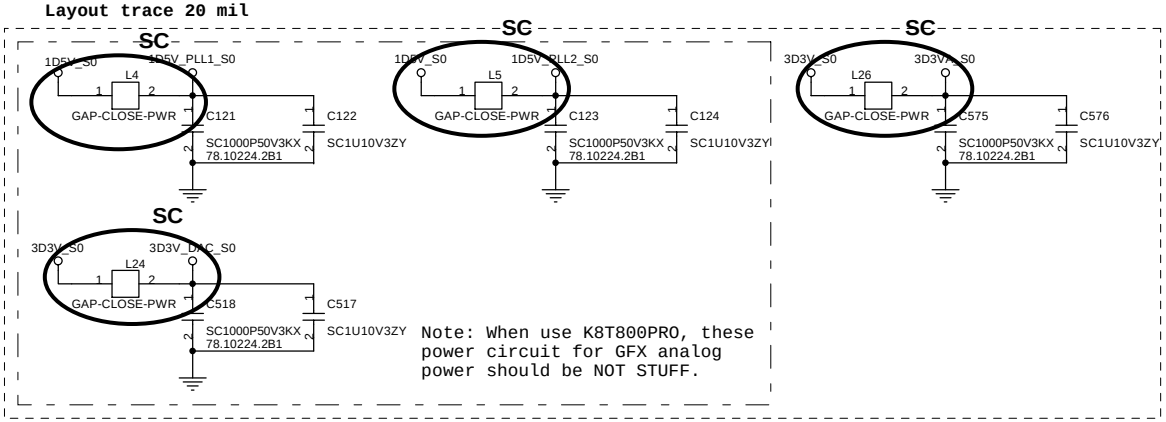
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: NB-K8N800(1/3)_HT		
Size: A3	Document Number: EGRET	Rev: SC
Date: Friday, July 23, 2004	Sheet 11 of 50	


V_LINK
CRT
SM Bus
TV Encoder/
Digital
Display
AGP 8X
U16B
K8N800
SB
SC
Use this function for K8N800
GFX power up strapping setting:
TVD/DVP0D[3:0] => Panel type selection
TVD4/DVP0D4 => FP-port multiplexed on AGP interface selection
0: Two 12-bit DVI interface
1: One 24-bit panel interface
TVD5/DVP0D5 => Dedicated DVI port configuration
0: TMDS
1: TV Encoder
TVD6/DVP0D6 => Dedicated DVI port selection
0: Disable
1: Enable
For K8T800PRO remove.
For K8N800 install.
Note: All of these power up strapping pin have internal pull down. Put an external pull up resister if want to set the default value to 1.
Only for K8T800PRO.
When use K8N800,
Please remove them.
05/10
For VIA suggest.
UMA AGPVREF 0.75V, Use 100 ohm
64.10005.651
Discrete 8X AGPVREF 0.35V, Use 324 ohm
64.32405.651
Layout trace 20 mil
Layout trace 20 mil
The voltage level of VL_VREF is 0.625V
Cross NB as short as possible
Decoupling capacitors
Close to the AGP connector
05/10
For VIA suggest.
K8N800 UMA Need to Pull-UP,
K8T800Pro Discrete should be Pull-down.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
NB-K8N800(2/3)_AGP_VLINK
EGRET
SC
Friday, July 23, 2004
Sheet 12 of 50

Layout trace 20 mil



Layout trace 20 mil

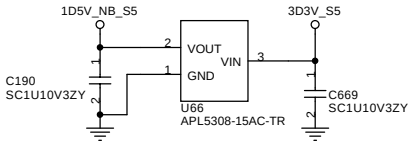


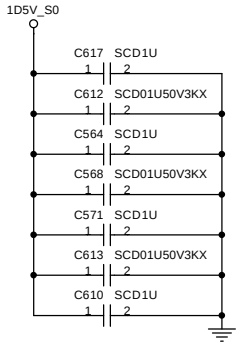
3,6,8,11,12,14,15,16,17,18,19,20,21,24,25,26,27,28,30,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0 → 3D3V_S0

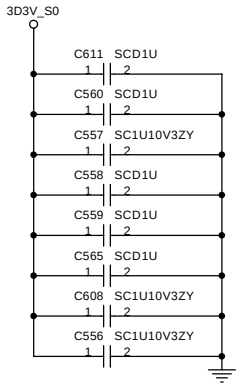
12,14,15,16,44,50 1D5V_S0 → 1D5V_S0

4,11,39,45 1D2V_HT0A_S0 → 1D2V_HT0A_S0

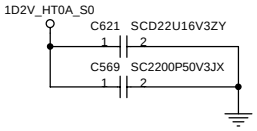
18,19,20,21,22,24,28,29,33,38,43,49,50 3D3V_S5 → 3D3V_S5

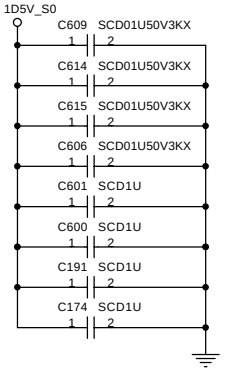


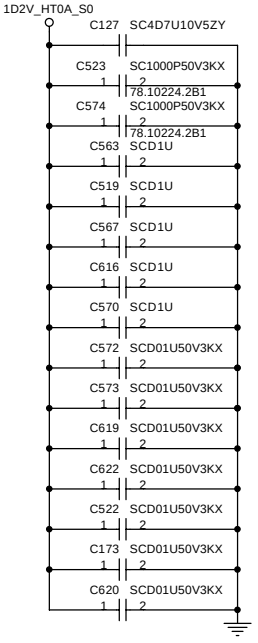


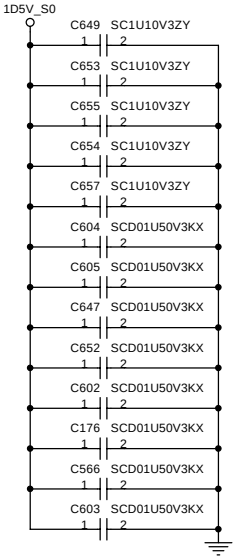


NEAR N/B ON BOT SIDE







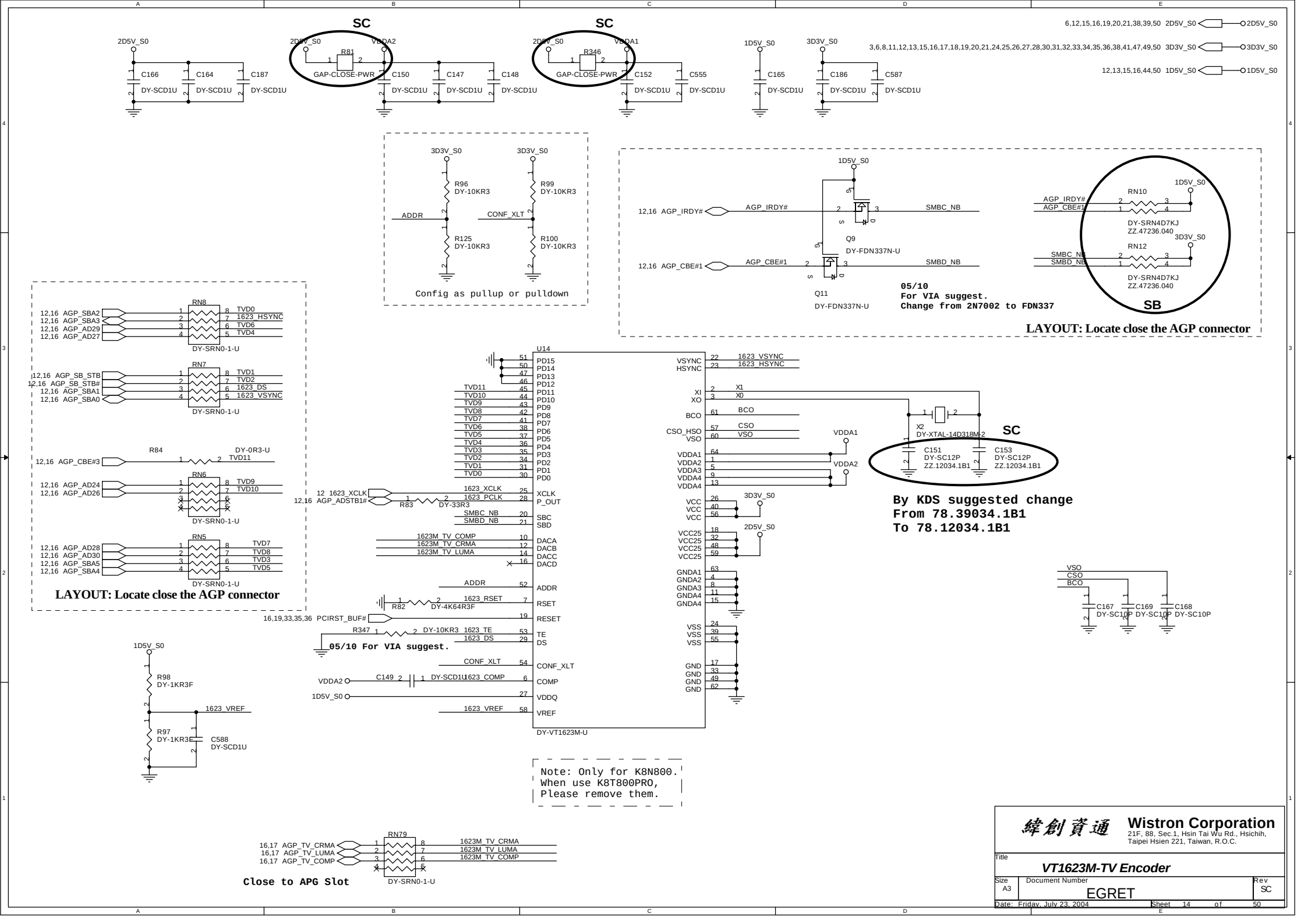


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

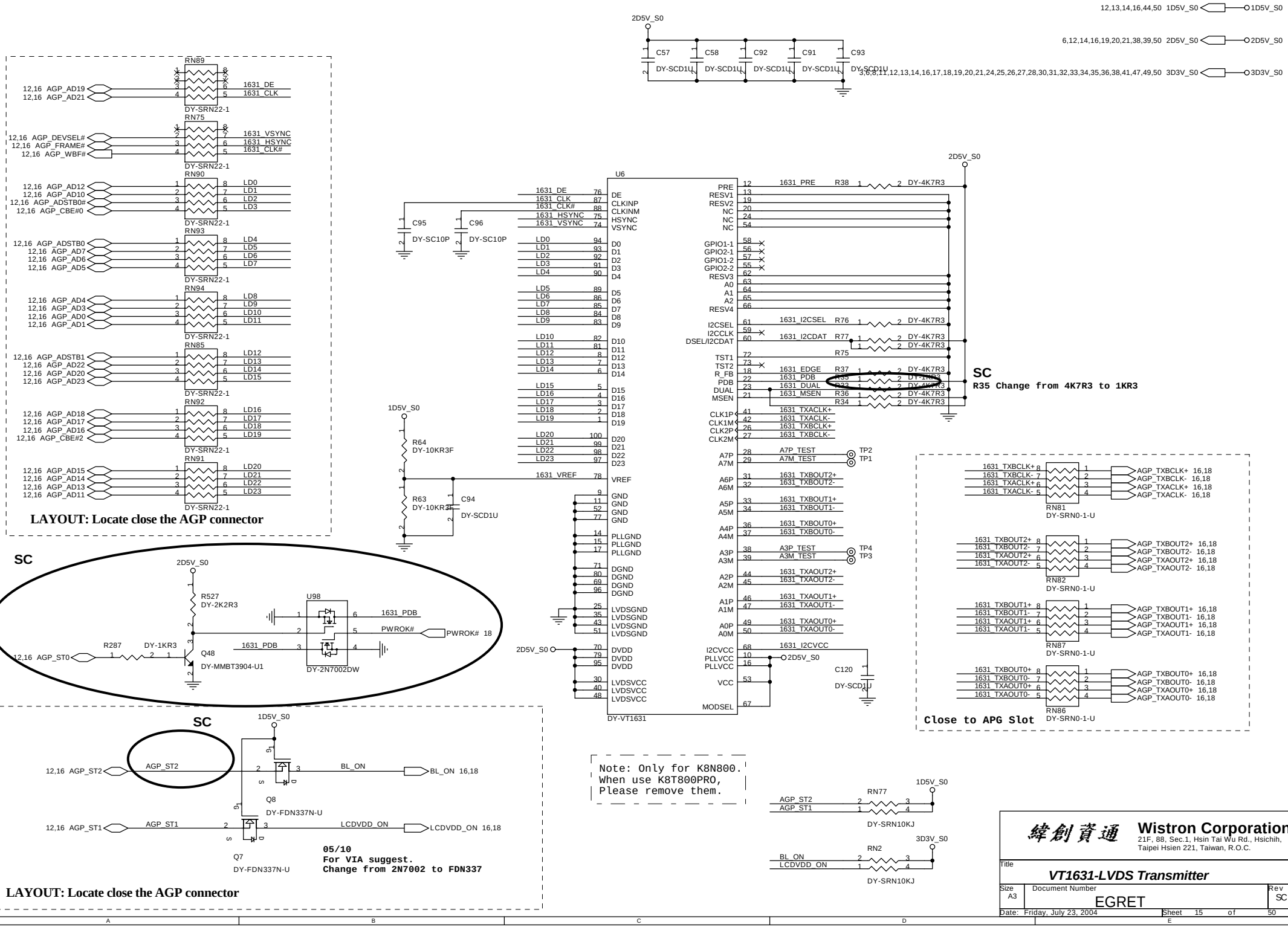
Title: ***NB-K8N800(3/3)_POWER***

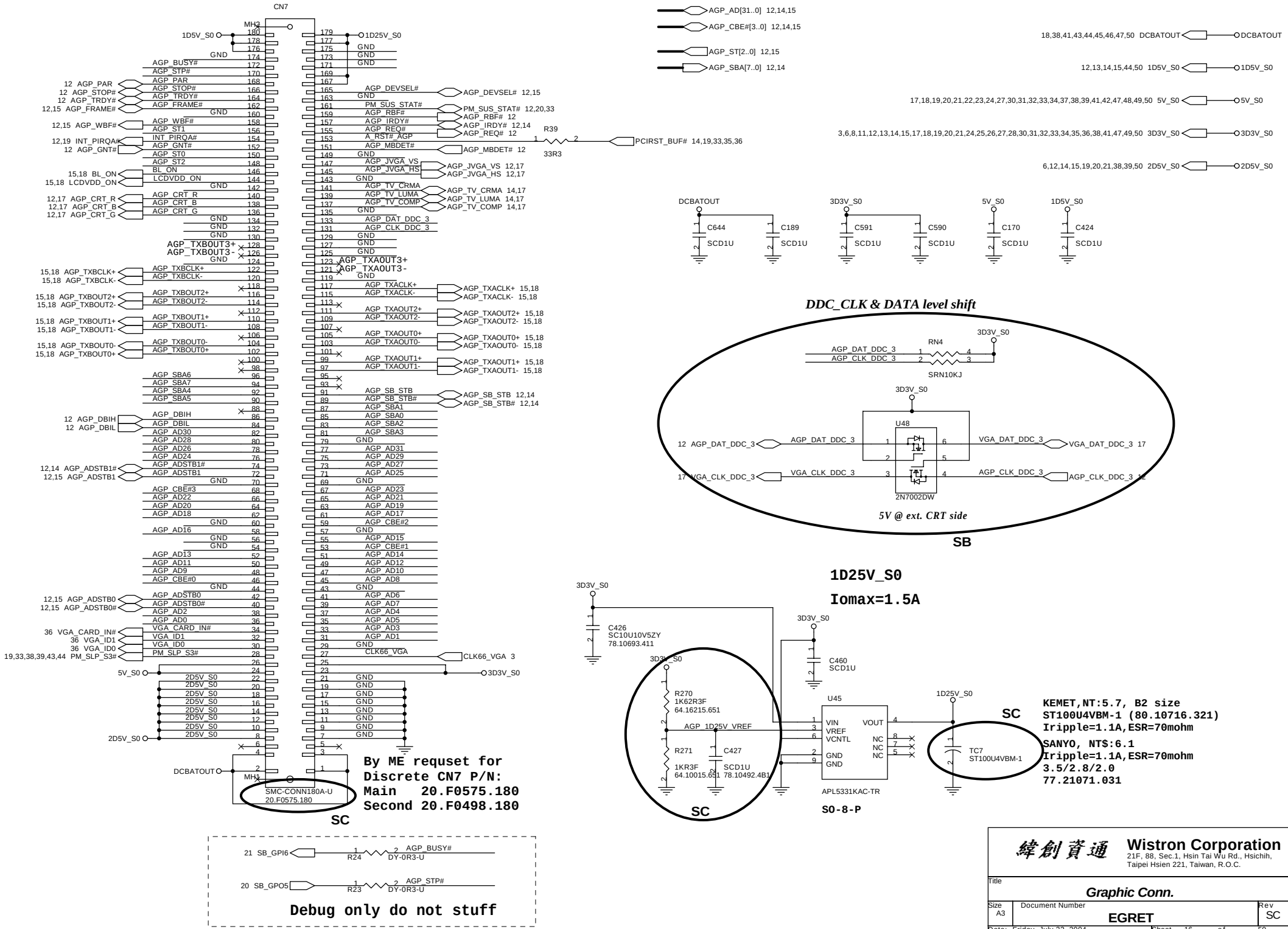
Size	Document Number	Rev
A3	**EGRET**	SC

Date: Friday, July 23, 2004 Sheet 13 of 50



緯創資通	**Wistron Corporation**
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***VT1623M-TV Encoder***
Size: A3	Document Number: EGRET
Rev: SC	
Date: Friday, July 23, 2004	Sheet 14 of 50

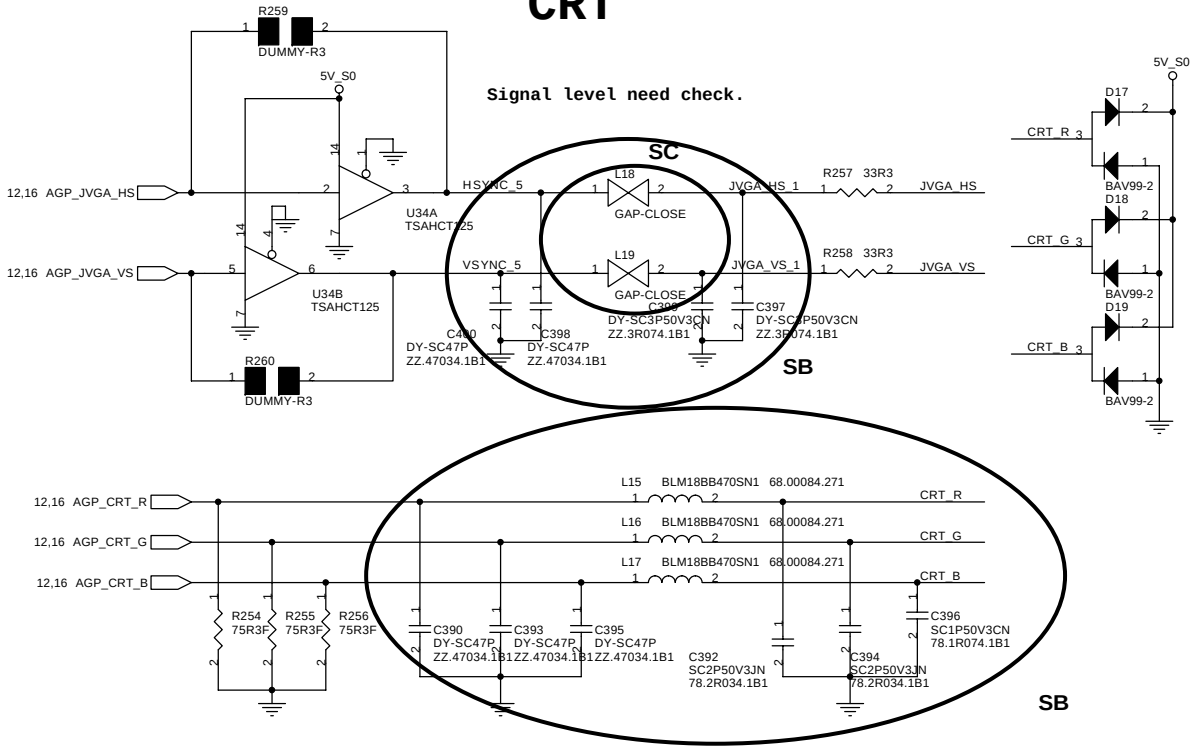

12,13,14,16,44,50 1D5V_S0
1D5V_S0
6,12,14,16,19,20,21,38,39,50 2D5V_S0
2D5V_S0
3,6,8,11,12,13,14,16,17,18,19,20,21,24,25,26,27,28,30,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0
3D3V_S0
2D5V_S0
C57 C58 C92 C91 C93
DY-SCD1U
RN89
12,16 AGP_AD19
12,16 AGP_AD21
1631_DE
1631_CLK
DY-SRN22-1
RN75
12,16 AGP_DEVSEL#
12,16 AGP_FRAME#
12,16 AGP_WBF#
1631_VSYNC
1631_HSYNC
1631_CLK#
RN90
12,16 AGP_AD12
12,16 AGP_AD10
12,16 AGP_ADSTB0#
12,16 AGP_CBE#0
LD0 LD1 LD2 LD3
RN93
12,16 AGP_ADSTB0
12,16 AGP_AD7
12,16 AGP_AD6
12,16 AGP_AD5
LD4 LD5 LD6 LD7
RN94
12,16 AGP_AD4
12,16 AGP_AD3
12,16 AGP_AD0
12,16 AGP_AD1
LD8 LD9 LD10 LD11
RN85
12,16 AGP_ADSTB1
12,16 AGP_AD22
12,16 AGP_AD20
12,16 AGP_AD23
LD12 LD13 LD14 LD15
RN92
12,16 AGP_AD18
12,16 AGP_AD17
12,16 AGP_AD16
12,16 AGP_CBE#2
LD16 LD17 LD18 LD19
RN91
12,16 AGP_AD15
12,16 AGP_AD14
12,16 AGP_AD13
12,16 AGP_AD11
LD20 LD21 LD22 LD23
LAYOUT: Locate close the AGP connector
U6
1631_DE
1631_CLK
1631_CLK#
1631_HSYNC
1631_VSYNC
DE
CLKINP
CLKINM
HSYNC
VSYNC
C95 C96
DY-SC10P
LD0 LD1 LD2 LD3 LD4 LD5 LD6 LD7 LD8 LD9 LD10 LD11 LD12 LD13 LD14 LD15 LD16 LD17 LD18 LD19 LD20 LD21 LD22 LD23
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23
1631_VREF
VREF
1D5V_S0
R64 DY-10KR3F
R63 DY-10KR3F
C94 DY-SCD1U
GND PLLGND DGND LVDSGND DVDD LVDSVCC
2D5V_S0
PRE RESV1 RESV2 NC GPIO1-1 GPIO2-1 GPIO1-2 GPIO2-2 RESV3 A0 A1 A2 RESV4 I2CSEL I2CCLK DSEL/I2CDAT TST1 TST2 R_FB PDB DUAL MSEN CLK1P CLK1M CLK2P CLK2M A7P A7M A6P A6M A5P A5M A4P A4M A3P A3M A2P A2M A1P A1M A0P A0M I2CVCC PLLVCC VCC MODSEL
1631_PRE R38 DY-4K7R3
1631_I2CSEL R76 DY-4K7R3
1631_I2CDAT R77 DY-4K7R3
R75 DY-4K7R3
1631_EDGE R37 DY-4K7R3
1631_PDB R35 DY-4K7R3
1631_DUAL R33 DY-4K7R3
1631_MSEN R36 DY-4K7R3
R34 DY-4K7R3
SC
R35 Change from 4K7R3 to 1KR3
1631_TXACLK+
1631_TXACLK-
1631_TXBCLK+
1631_TXBCLK-
A7P_TEST
A7M_TEST
TP2
TP1
1631_TXBOUT2+
1631_TXBOUT2-
1631_TXBOUT1+
1631_TXBOUT1-
1631_TXBOUT0+
1631_TXBOUT0-
A3P_TEST
A3M_TEST
TP4
TP3
1631_TXAOUT2+
1631_TXAOUT2-
1631_TXAOUT1+
1631_TXAOUT1-
1631_TXAOUT0+
1631_TXAOUT0-
1631_I2CVCC
C120 DY-SCD1U
DY-VT1631
1631_TXBCLK+ 1631_TXBCLK- 1631_TXACLK+ 1631_TXACLK-
AGP_TXBCLK+ 16,18
AGP_TXBCLK- 16,18
AGP_TXACLK+ 16,18
AGP_TXACLK- 16,18
RN81 DY-SRN0-1-U
1631_TXBOUT2+ 1631_TXBOUT2- 1631_TXAOUT2+ 1631_TXAOUT2-
AGP_TXBOUT2+ 16,18
AGP_TXBOUT2- 16,18
AGP_TXAOUT2+ 16,18
AGP_TXAOUT2- 16,18
RN82 DY-SRN0-1-U
1631_TXBOUT1+ 1631_TXBOUT1- 1631_TXAOUT1+ 1631_TXAOUT1-
AGP_TXBOUT1+ 16,18
AGP_TXBOUT1- 16,18
AGP_TXAOUT1+ 16,18
AGP_TXAOUT1- 16,18
RN87 DY-SRN0-1-U
1631_TXBOUT0+ 1631_TXBOUT0- 1631_TXAOUT0+ 1631_TXAOUT0-
AGP_TXBOUT0+ 16,18
AGP_TXBOUT0- 16,18
AGP_TXAOUT0+ 16,18
AGP_TXAOUT0- 16,18
RN86 DY-SRN0-1-U
Close to APG Slot
SC
2D5V_S0
R527 DY-2K2R3
U98
1631_PDB
PWROK#
PWROK# 18
R287 DY-1KR3
12,16 AGP_ST0
Q48 DY-MMBT3904-U1
DY-2N7002DW
SC
1D5V_S0
12,16 AGP_ST2
AGP_ST2
BL_ON
BL_ON 16,18
Q8 DY-FDN337N-U
12,16 AGP_ST1
AGP_ST1
LCDVDD_ON
LCDVDD_ON 16,18
Q7 DY-FDN337N-U
05/10
For VIA suggest.
Change from 2N7002 to FDN337
LAYOUT: Locate close the AGP connector
Note: Only for K8N800.
When use K8T800PRO,
Please remove them.
1D5V_S0
RN77
AGP_ST2
AGP_ST1
DY-SRN10KJ
3D3V_S0
RN2
BL_ON
LCDVDD_ON
DY-SRN10KJ
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VT1631-LVDS Transmitter
Size A3
Document Number
EGRET
Rev SC
Date: Friday, July 23, 2004
Sheet 15 of 50


CN7
1D5V_S0
GND
AGP_BUSY#
AGP_STP#
12 AGP_PAR
12 AGP_STOP#
12 AGP_TRDY#
12,15 AGP_FRAME#
12,15 AGP_WBF#
12,19 INT_PIRQA#
12 AGP_GNT#
15,18 BL_ON
15,18 LCDVDD_ON
12,17 AGP_CRT_R
12,17 AGP_CRT_B
12,17 AGP_CRT_G
AGP_TXBOUT3+
AGP_TXBOUT3-
15,18 AGP_TXBCLK+
15,18 AGP_TXBCLK-
15,18 AGP_TXBOUT2+
15,18 AGP_TXBOUT2-
15,18 AGP_TXBOUT1+
15,18 AGP_TXBOUT1-
15,18 AGP_TXBOUT0-
15,18 AGP_TXBOUT0+
12 AGP_DBIH
12 AGP_DBIL
12,14 AGP_ADSTB1#
12,15 AGP_ADSTB1
12,15 AGP_ADSTB0
12,15 AGP_ADSTB0#
36 VGA_CARD_IN#
36 VGA_ID1
36 VGA_ID0
19,33,38,39,43,44 PM_SLP_S3#
5V_S0
2D5V_S0
DCBATOUT
MH1
SMC-CONN180A-U
20.F0575.180
SC
1D25V_S0
AGP_DEVSEL#
AGP_DEVSEL# 12,15
PM_SUS_STAT#
PM_SUS_STAT# 12,20,33
AGP_RBF#
AGP_RBF# 12
AGP_IRDY#
AGP_IRDY# 12,14
AGP_REQ#
AGP_REQ# 12
A_RST# AGP
AGP_MBDET#
AGP_MBDET# 12
R39
33R3
PCIRST_BUF# 14,19,33,35,36
AGP_JVGA_VS
AGP_JVGA_VS 12,17
AGP_JVGA_HS
AGP_JVGA_HS 12,17
AGP_TV_CRMA
AGP_TV_CRMA 14,17
AGP_TV_LUMA
AGP_TV_LUMA 14,17
AGP_TV_COMP
AGP_TV_COMP 14,17
AGP_DAT_DDC_3
AGP_CLK_DDC_3
AGP_TXAOUT3+
AGP_TXAOUT3-
AGP_TXACLK+
AGP_TXACLK+ 15,18
AGP_TXACLK-
AGP_TXACLK- 15,18
AGP_TXAOUT2+
AGP_TXAOUT2+ 15,18
AGP_TXAOUT2-
AGP_TXAOUT2- 15,18
AGP_TXAOUT0+
AGP_TXAOUT0+ 15,18
AGP_TXAOUT0-
AGP_TXAOUT0- 15,18
AGP_TXAOUT1+
AGP_TXAOUT1+ 15,18
AGP_TXAOUT1-
AGP_TXAOUT1- 15,18
AGP_SB_STB
AGP_SB_STB 12,14
AGP_SB_STB#
AGP_SB_STB# 12,14
CLK66_VGA
CLK66_VGA 3
3D3V_S0
AGP_AD[31..0] 12,14,15
AGP_CBE#[3..0] 12,14,15
AGP_ST[2..0] 12,15
AGP_SBA[7..0] 12,14
18,38,41,43,44,45,46,47,50 DCBATOUT
12,13,14,15,44,50 1D5V_S0
17,18,19,20,21,22,23,24,27,30,31,32,33,34,37,38,39,41,42,47,48,49,50 5V_S0
3,6,8,11,12,13,14,15,17,18,19,20,21,24,25,26,27,28,30,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0
6,12,14,15,19,20,21,38,39,50 2D5V_S0
C644
SCD1U
C189
C591
C590
C170
C424
DDC_CLK & DATA level shift
RN4
SRN10KJ
U48
2N7002DW
12 AGP_DAT_DDC_3
17 VGA_CLK_DDC_3
VGA_DAT_DDC_3
VGA_DAT_DDC_3 17
VGA_CLK_DDC_3
AGP_CLK_DDC_3
AGP_CLK_DDC_3 17
5V @ ext. CRT side
SB
1D25V_S0
Iomax=1.5A
C426
SC10U10V5ZY
78.10693.411
C460
SCD1U
R270
1K62R3F
64.16215.651
R271
1KR3F
64.10015.651
C427
SCD1U
78.10492.4B1
U45
APL5331KAC-TR
S0-8-P
TC7
ST100U4VBM-1
KEMET,NT:5.7, B2 size
ST100U4VBM-1 (80.10716.321)
Iripple=1.1A,ESR=70mohm
SANYO, NT$:6.1
Iripple=1.1A,ESR=70mohm
3.5/2.8/2.0
77.21071.031
By ME requset for
Discrete CN7 P/N:
Main 20.F0575.180
Second 20.F0498.180
21 SB_GPI6
R24
DY-0R3-U
20 SB_GPO5
R23
Debug only do not stuff
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Graphic Conn.
EGRET
Size A3
Rev SC
Date: Friday, July 23, 2004
Sheet 16 of 50

16,18,19,20,21,22,23,24,27,30,31,32,33,34,37,38,39,41,42,47,48,49,50 5V_S0 — 5V_S0

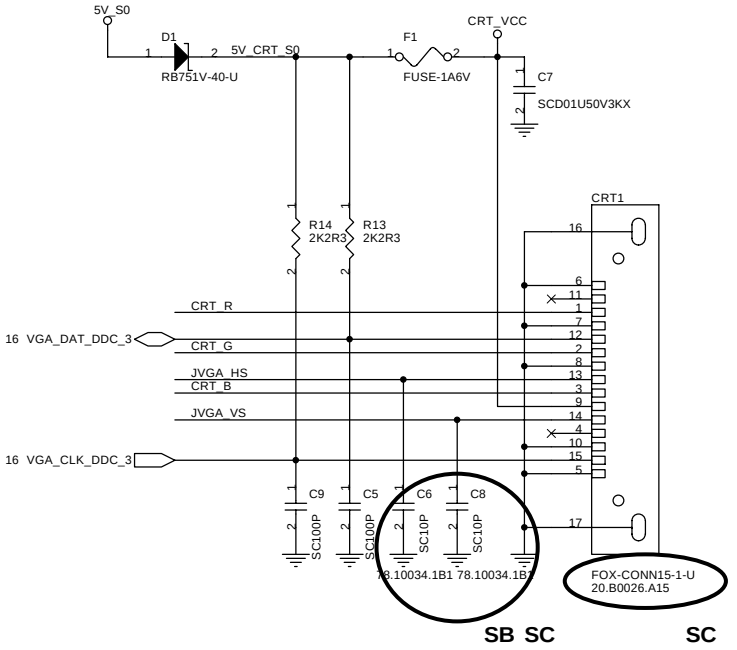
3,6,8,11,12,13,14,15,16,18,19,20,21,24,25,26,27,28,30,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0 — 3D3V_S0

CRT

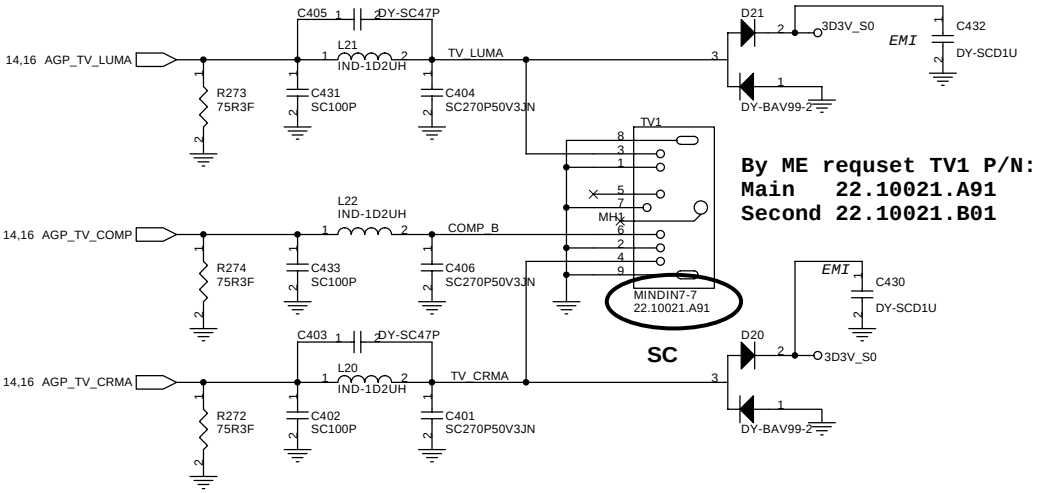


CRT CONN

200mA Rating/Spec 500mA

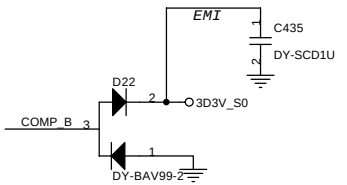


By ME requset CRT1 P/N:
Main 20.B0026.A15
Second 20.B0034.015



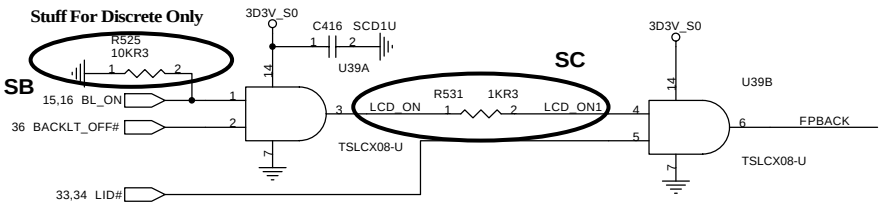
By ME requset TV1 P/N:
Main 22.10021.A91
Second 22.10021.B01

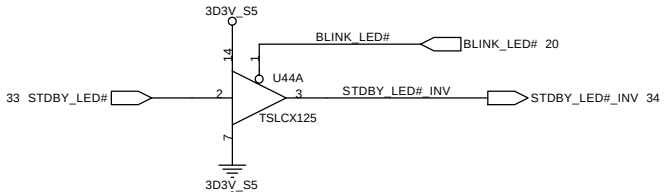
TV CONN

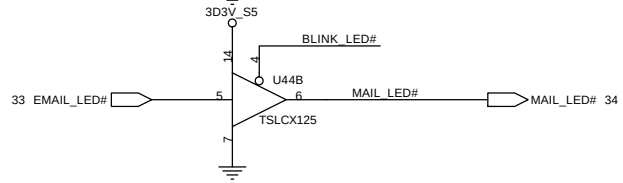


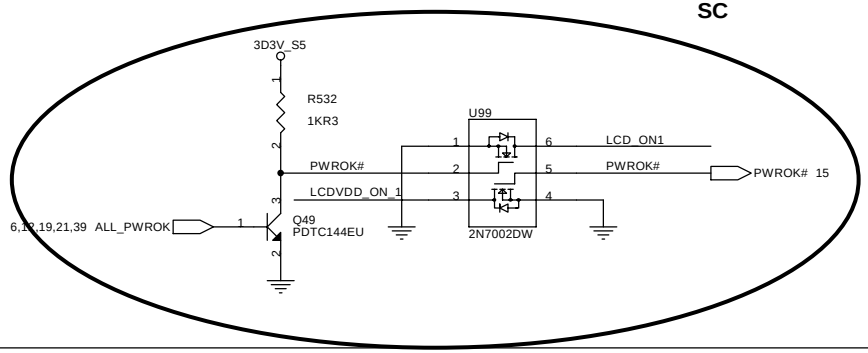
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT / TV***	
Size A3	Document Number **EGRET**	Rev SC
Date: Friday, July 23, 2004	Sheet 17 of 50	

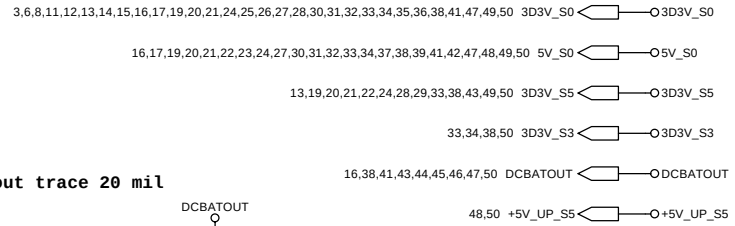
INVERTER/LED



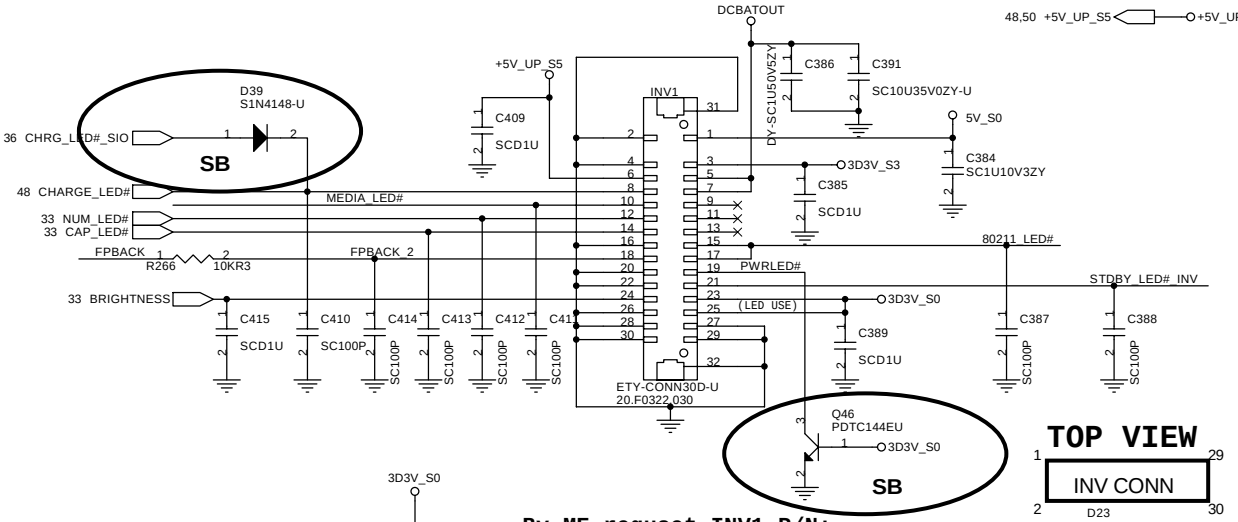


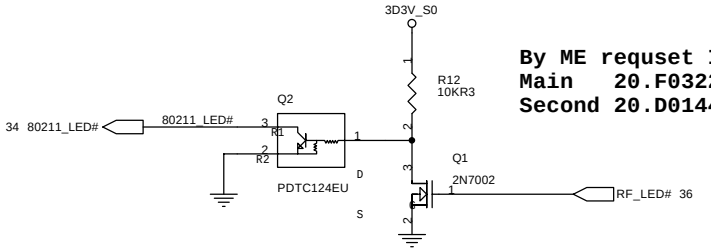




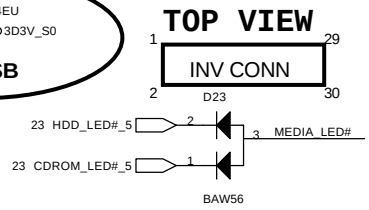


Layout trace 20 mil

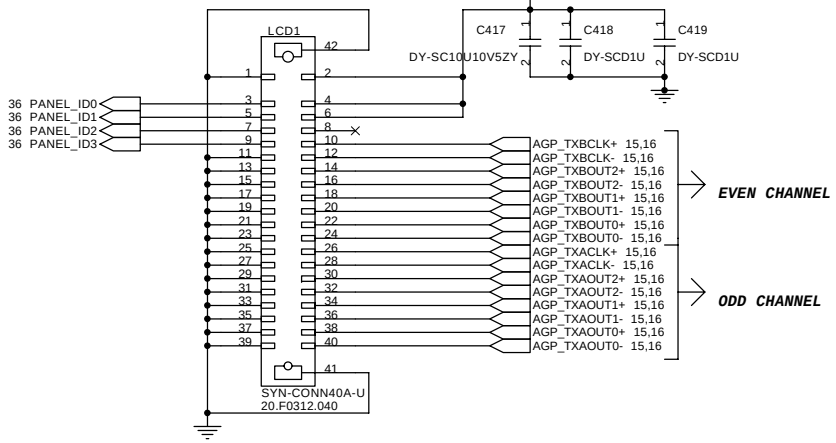




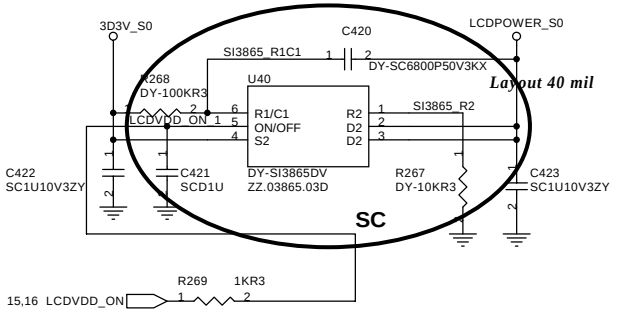
By ME requset INV1 P/N:
Main 20.F0322.030
Second 20.D0144.215

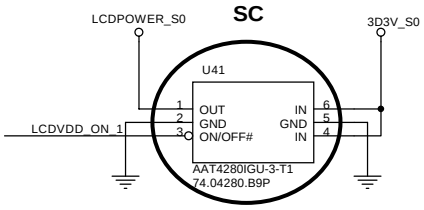


LCD CONN



LCD POWER



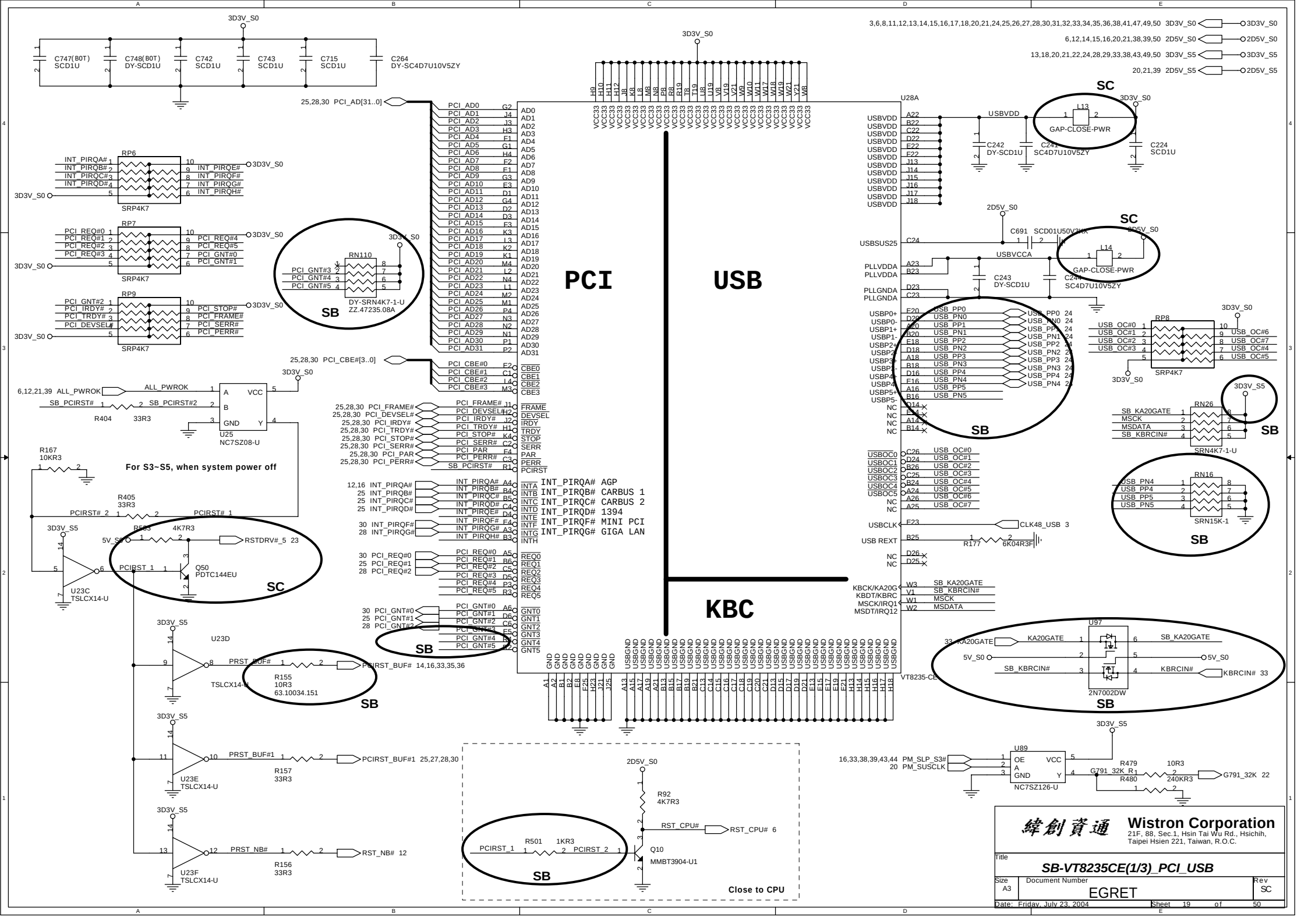


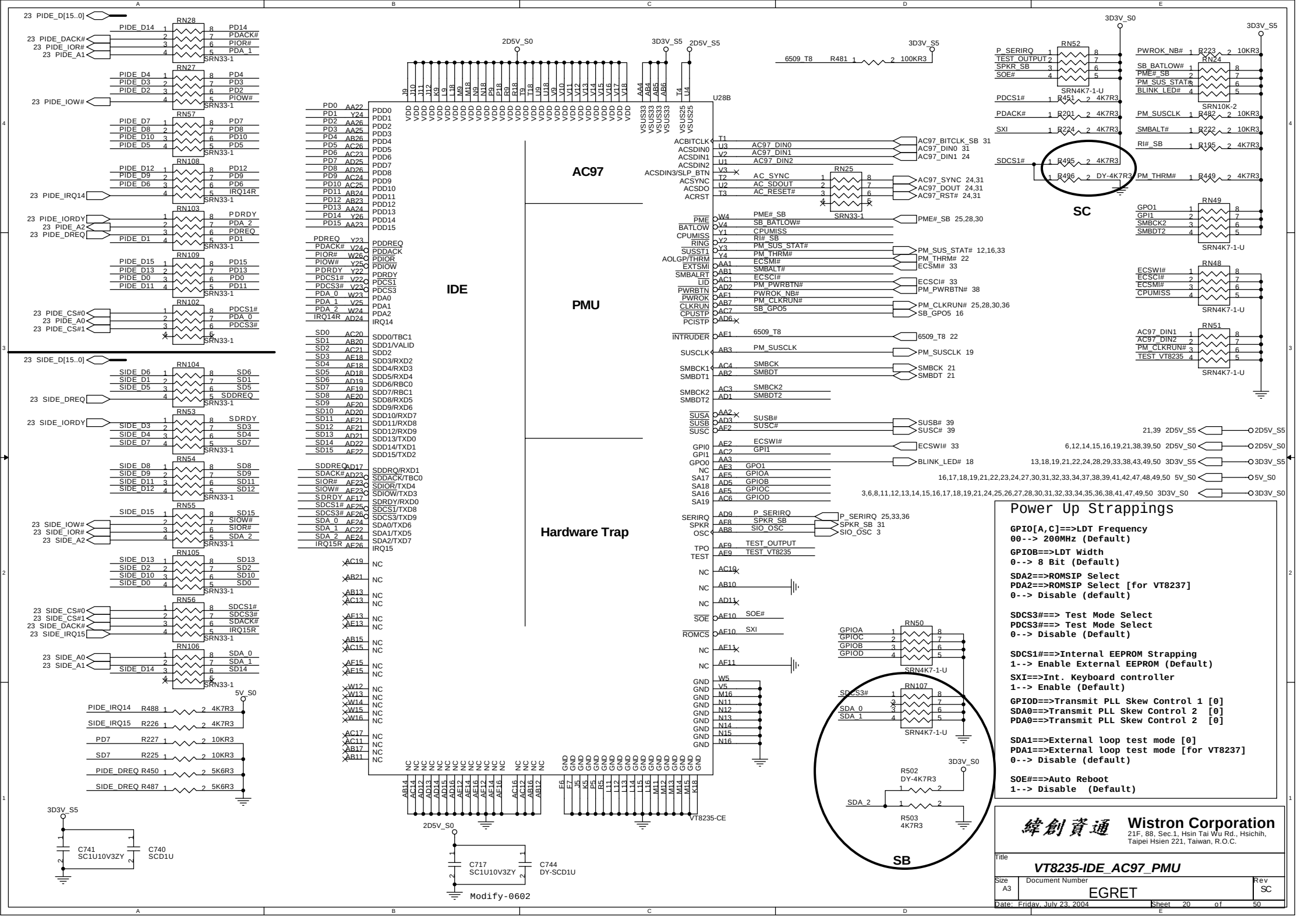
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

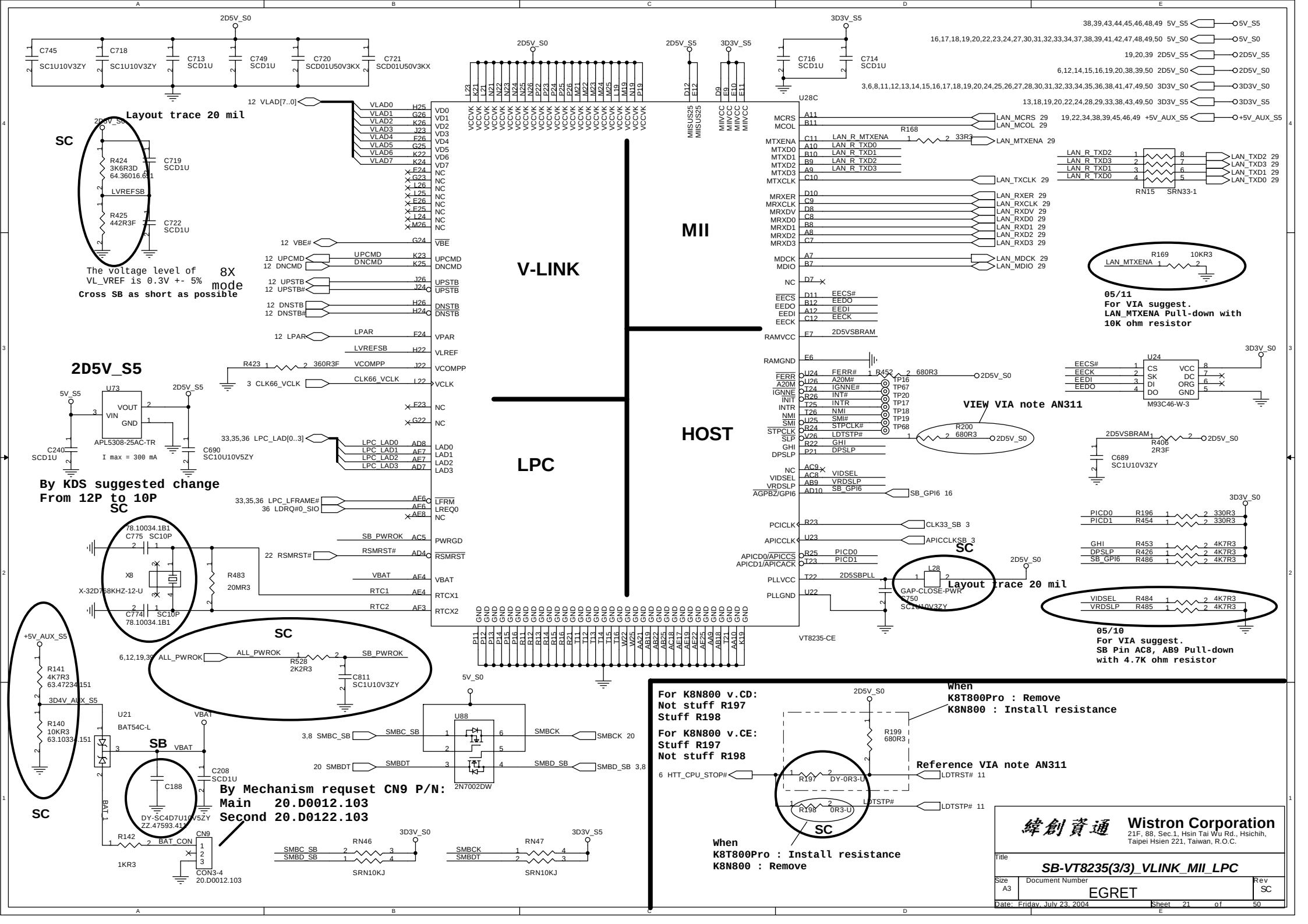
Title: ***INV / LCD***

Size: A3 | Document Number: **EGRET** | Rev: SC

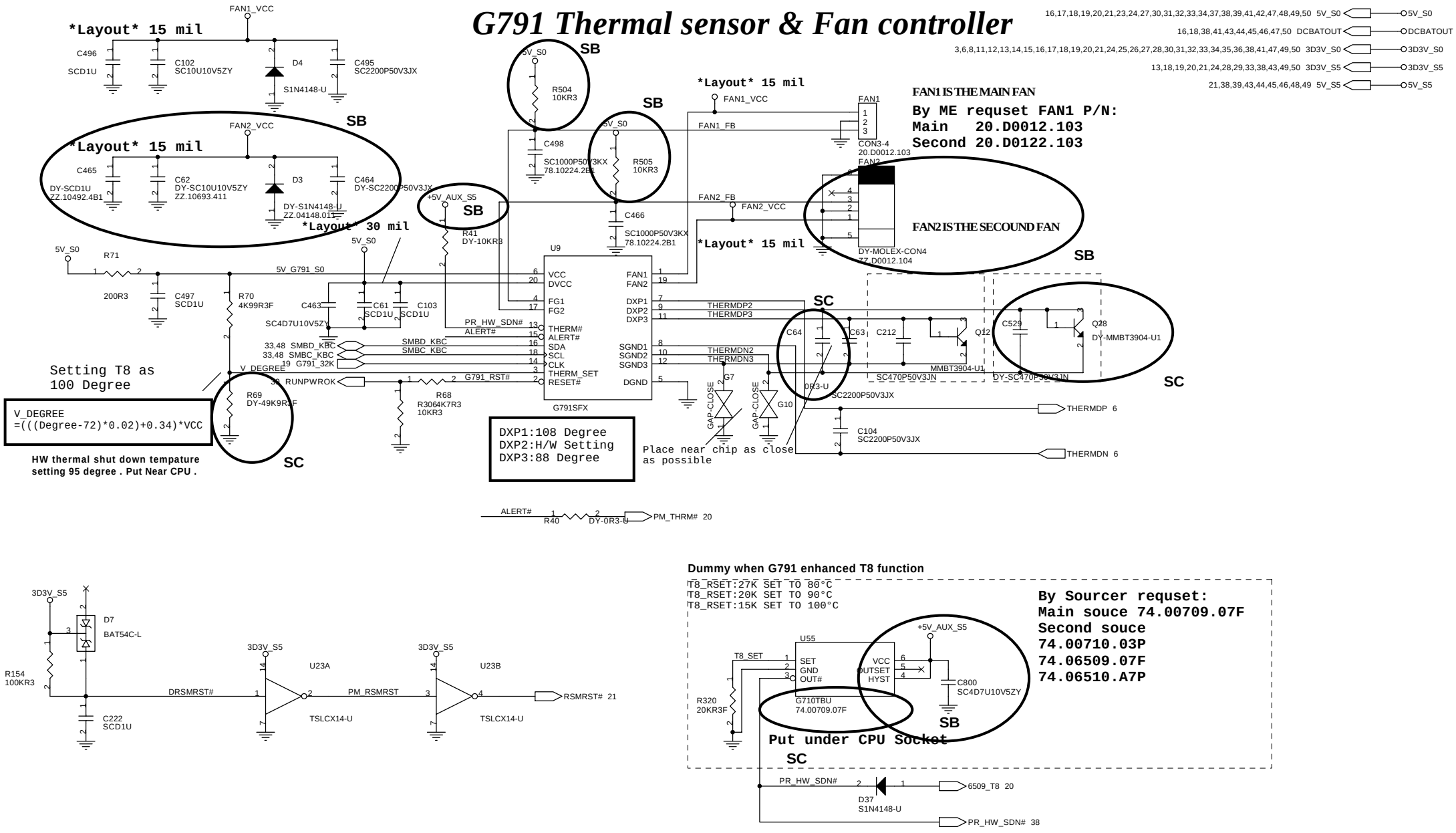
Date: Friday, July 23, 2004 | Sheet 18 of 50


PCI
USB
KBC
SB
SC
For S3~S5, when system power off
Close to CPU
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SB-VT8235CE(1/3)_PCI_USB
EGRET
Date: Friday, July 23, 2004
Sheet 19 of 50


IDE
AC97
PMU
Hardware Trap
SC
SB
Power Up Strappings
GPIO[A,C]==>LDT Frequency
00--> 200MHz (Default)
GPIOB==>LDT Width
0--> 8 Bit (Default)
SDA2==>ROMSIP Select
PDA2==>ROMSIP Select [for VT8237]
0--> Disable (default)
SDCS3#==> Test Mode Select
PDCS3#==> Test Mode Select
0--> Disable (Default)
SDCS1#==>Internal EEPROM Strapping
1--> Enable External EEPROM (Default)
SXI==>Int. Keyboard controller
1--> Enable (Default)
GPIOD==>Transmit PLL Skew Control 1 [0]
SDA0==>Transmit PLL Skew Control 2 [0]
PDA0==>Transmit PLL Skew Control 2 [0]
SDA1==>External loop test mode [0]
PDA1==>External loop test mode [for VT8237]
0--> Disable (default)
SOE#==>Auto Reboot
1--> Disable (Default)
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VT8235-IDE_AC97_PMU
Size A3
Document Number EGRET
Rev SC
Date: Friday, July 23, 2004
Sheet 20 of 50
Modify-0602


V-LINK
MII
HOST
LPC
VT8235-CE
U28C
Layout trace 20 mil
SC
The voltage level of VL_VREF is 0.3V +- 5%
8X mode
Cross SB as short as possible
2D5V_S5
By KDS suggested change
From 12P to 10P
By Mechanism requset CN9 P/N:
Main 20.D0012.103
Second 20.D0122.103
05/11
For VIA suggest.
LAN_MTXENA Pull-down with
10K ohm resistor
VIEW VIA note AN311
05/10
For VIA suggest.
SB Pin AC8, AB9 Pull-down
with 4.7K ohm resistor
Reference VIA note AN311
For K8N800 v.CD:
Not stuff R197
Stuff R198
For K8N800 v.CE:
Stuff R197
Not stuff R198
When
K8T800Pro : Remove
K8N800 : Install resistance
When
K8T800Pro : Install resistance
K8N800 : Remove
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SB-VT8235(3/3)_VLINK_MII_LPC
EGRET
Date: Friday, July 23, 2004
Sheet 21 of 50

G791 Thermal sensor & Fan controller

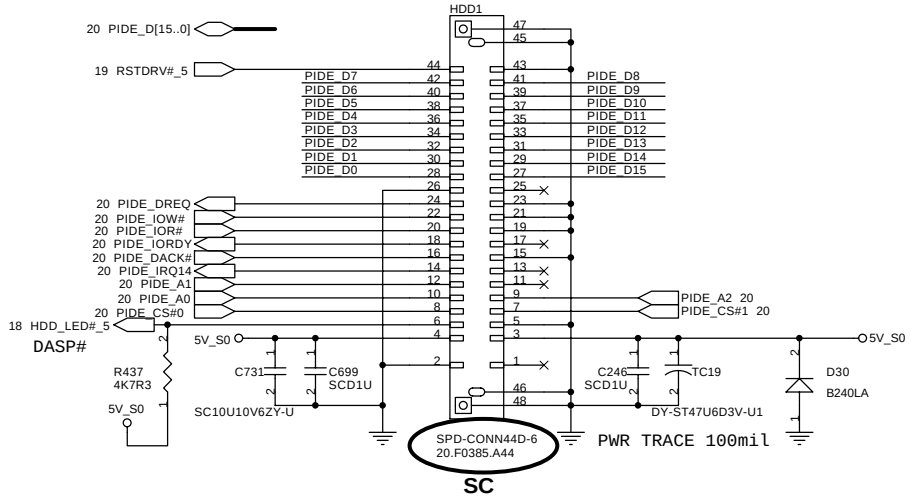


16,17,18,19,20,21,23,24,27,30,31,32,33,34,37,38,39,41,42,47,48,49,50 5V_S0 → 5V_S0
16,18,38,41,43,44,45,46,47,50 DCBATOUT → DCBATOUT
3,6,8,11,12,13,14,15,16,17,18,19,20,21,24,25,26,27,28,30,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0 → 3D3V_S0
13,18,19,20,21,24,28,29,33,38,43,49,50 3D3V_S5 → 3D3V_S5
21,38,39,43,44,45,46,48,49 5V_S5 → 5V_S5

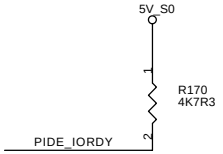
Dummy when G791 enhanced T8 function

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*G791*	
Size: Custom	Document Number: EGRET	Rev: SC
Date: Friday, July 23, 2004	Sheet 22 of 50	

HDD

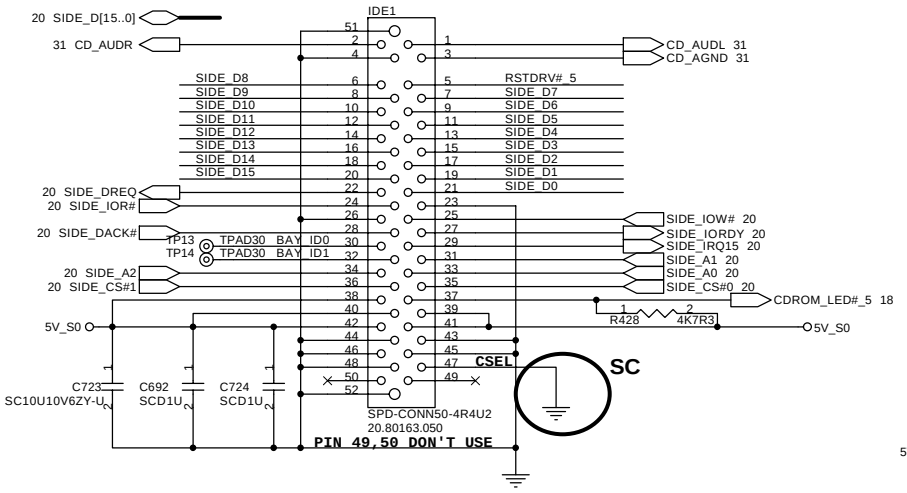


By ME requset change P/N:
from 20.F0385.044
to 20.F0385.A44



16,17,18,19,20,21,22,24,27,30,31,32,33,34,37,38,39,41,42,47,48,49,50 5V_S0 5V_S0

CDROM

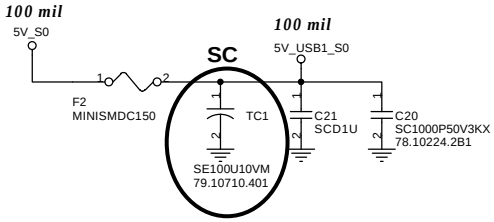


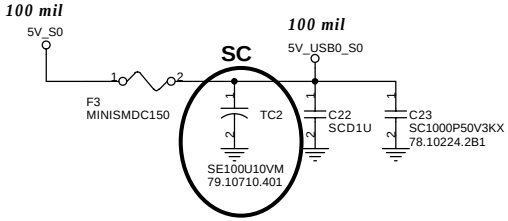
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

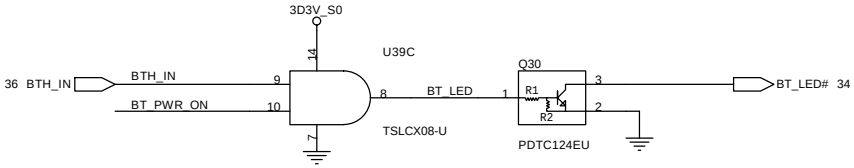
Title: ***HDD / CDROM***

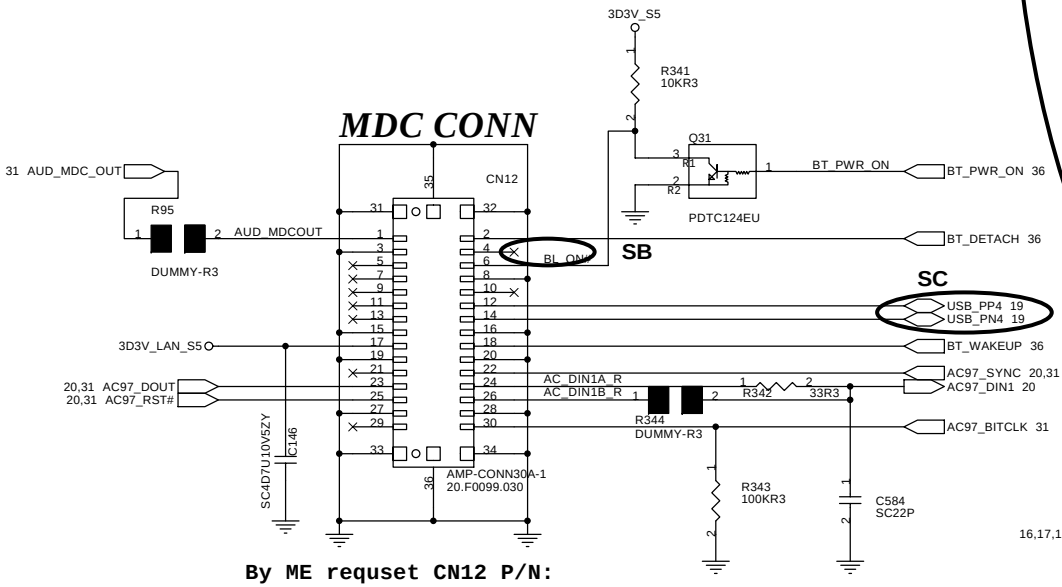
Size	Document Number	Rev
A3	EGRET	SC

Date: Friday, July 23, 2004 Sheet 23 of 50

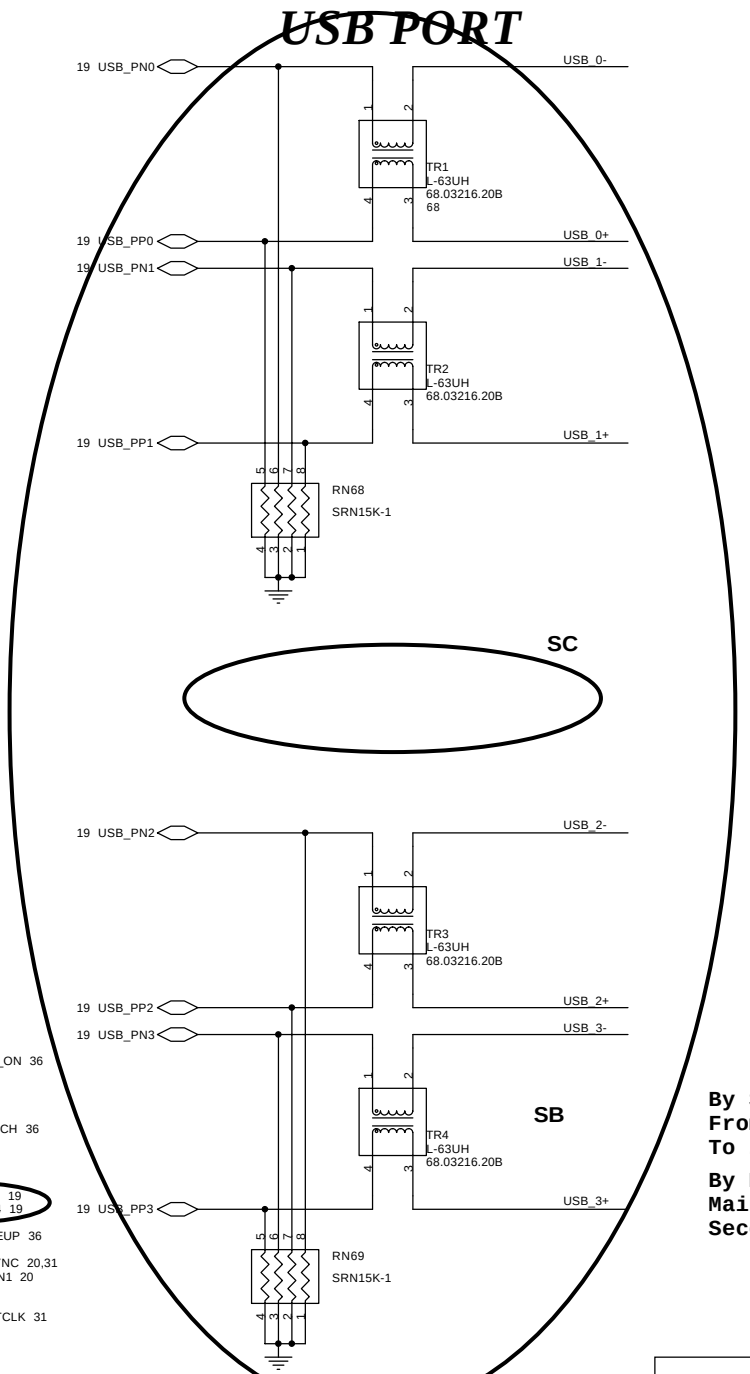


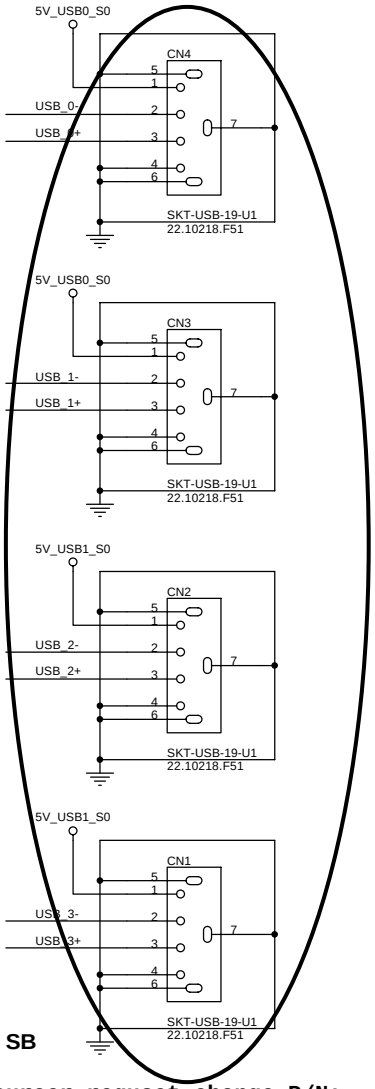






By ME requset CN12 P/N:
Main 20.F0099.030
Second 20.F0589.030





By Sourcer requset change P/N:
From 22.10218.701
To 22.10218.F51

By ME requset P/N:
Main 22.10218.F51
Second 22.10218.F41

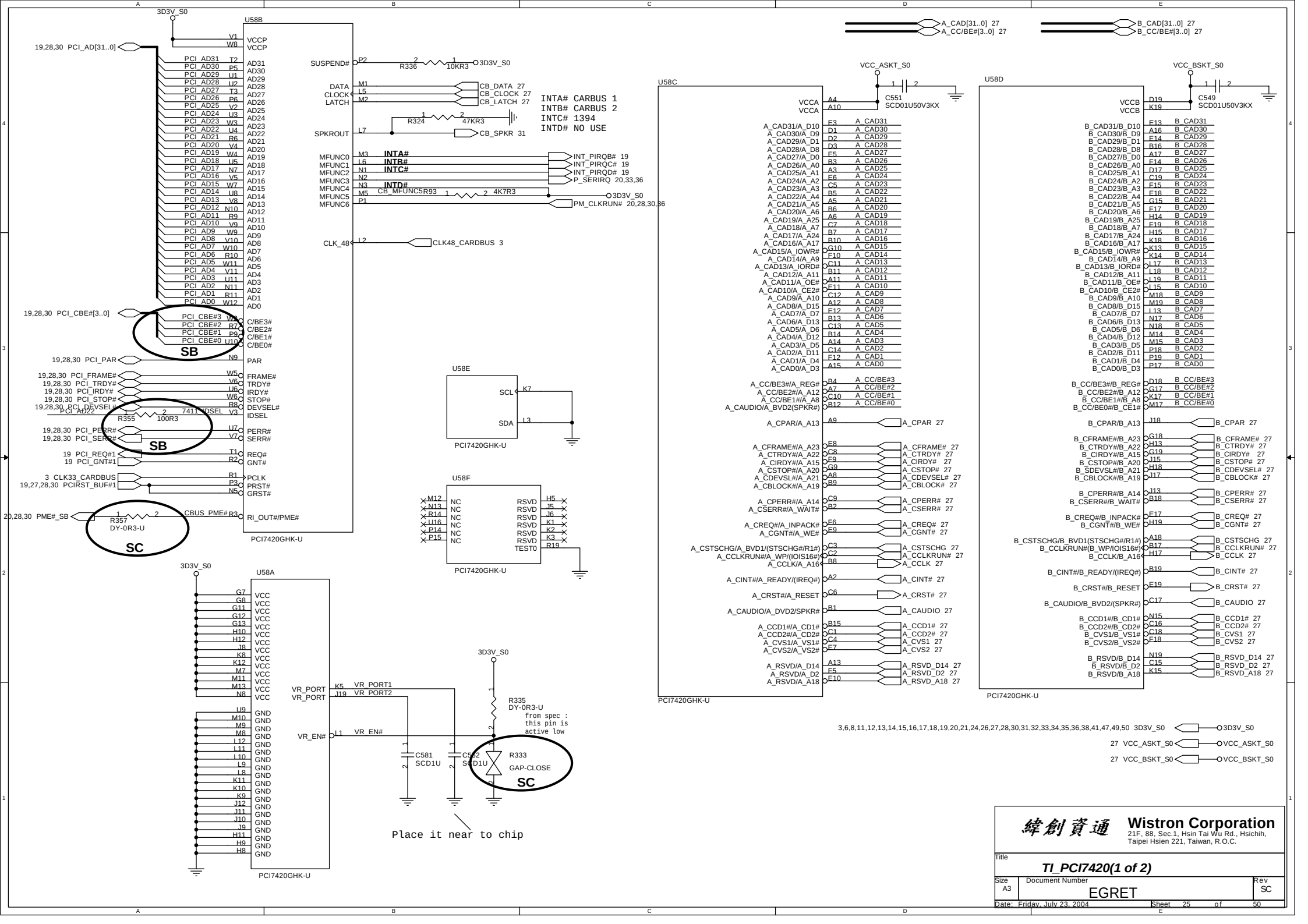
16,17,18,19,20,21,22,23,27,30,31,32,33,34,37,38,39,41,42,47,48,49,50 5V_S0 — 5V_S0
13,18,19,20,21,22,28,29,33,38,43,49,50 3D3V_S5 — 3D3V_S5
28,29 3D3V_LAN_S5 — 3D3V_LAN_S5
3,6,8,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,30,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0 — 3D3V_S0

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB and MDC**

Size	Document Number	Rev
A3	EGRET	SC

Date: Friday, July 23, 2004 Sheet 24 of 50



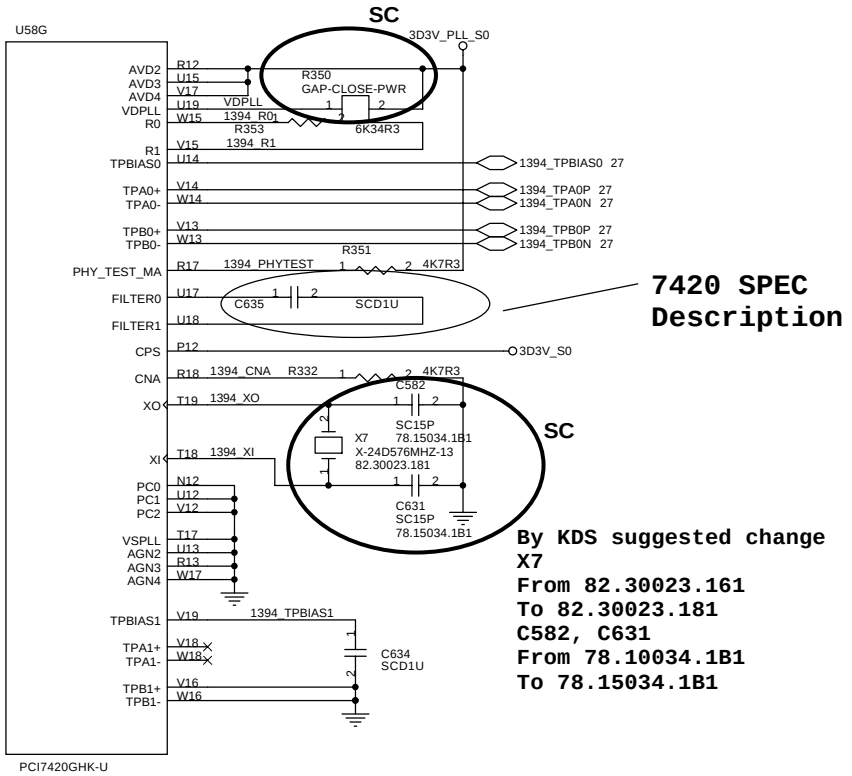
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TI_PCI7420(1 of 2)***

Size: A3 | Document Number: EGRET | Rev: SC

Date: Friday, July 23, 2004 | Sheet 25 of 50

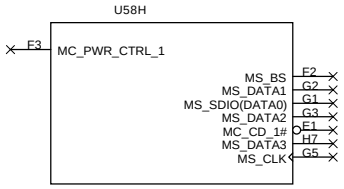
3,6,8,11,12,13,14,15,16,17,18,19,20,21,24,25,27,28,30,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0 3D3V_S0

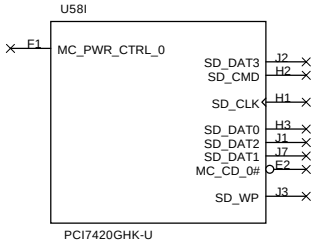


7420 SPEC Description

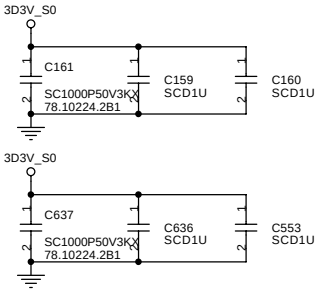
SC

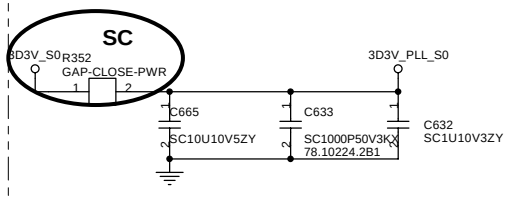
By KDS suggested change
X7
From 82.30023.161
To 82.30023.181
C582, C631
From 78.10034.1B1
To 78.15034.1B1





Bypass/Decupoling Capacitors
Should be places as close to
PCI7420 as possible



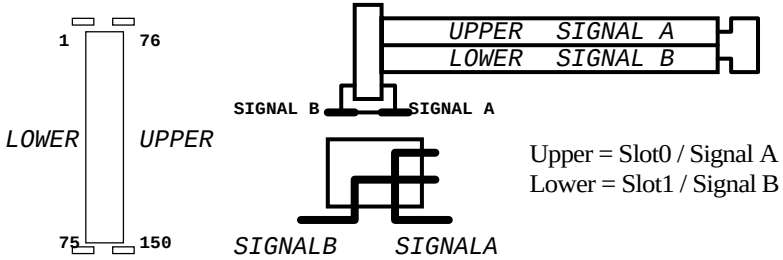


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

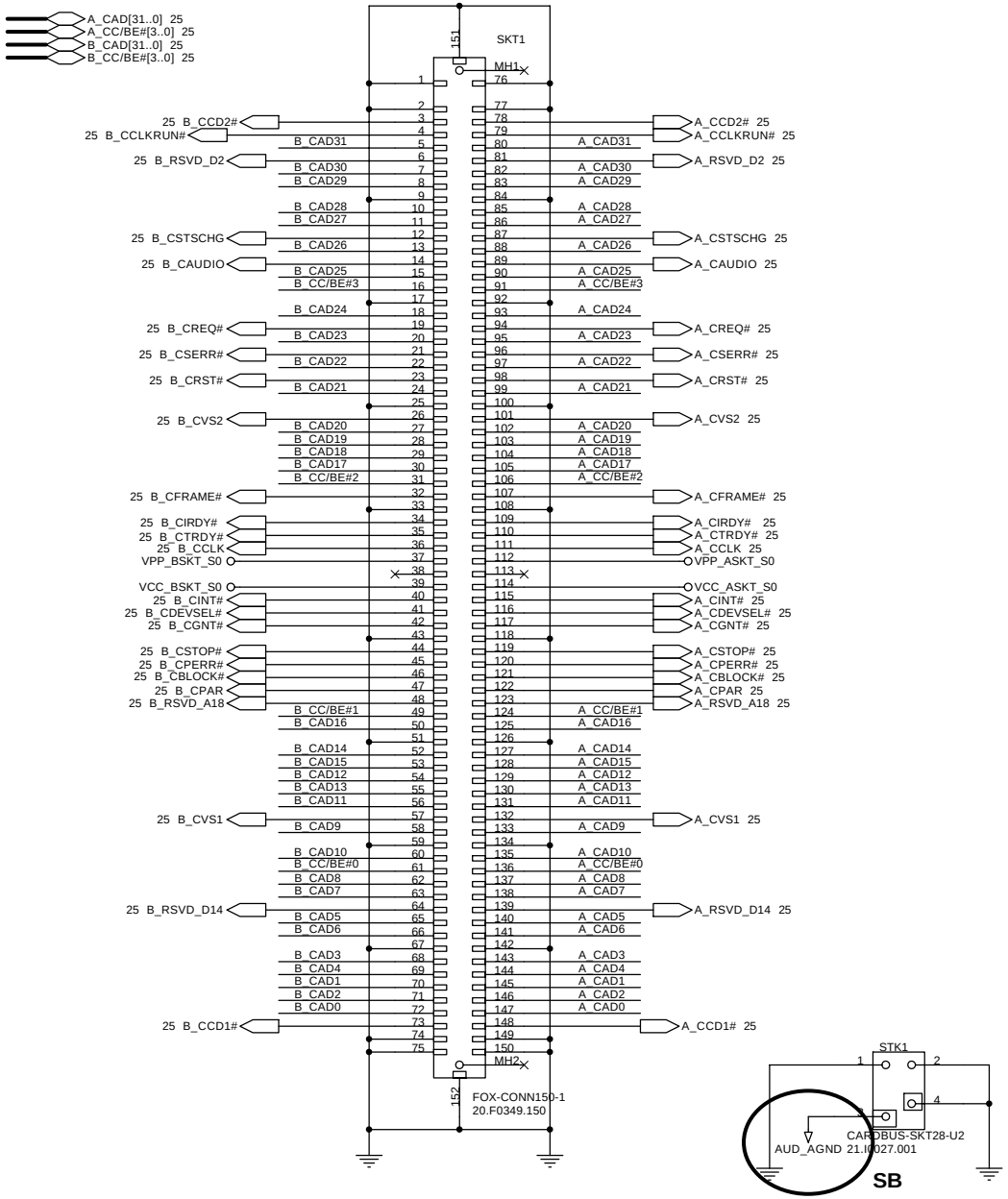
Title
TI_PCI7420(2 of 2)

Size	Document Number	Rev
A3	EGRET	SC

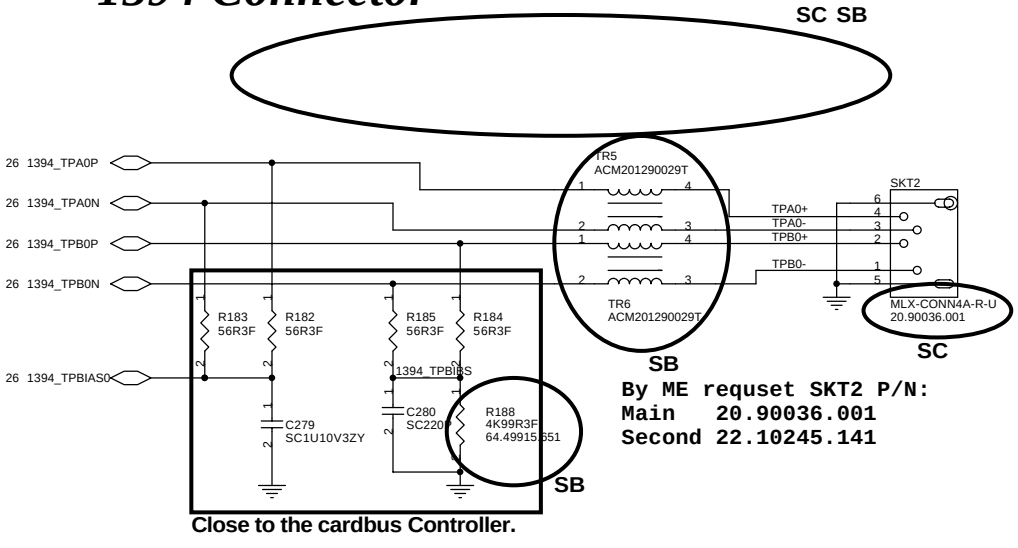
Date: Friday, July 23, 2004 Sheet 26 of 50



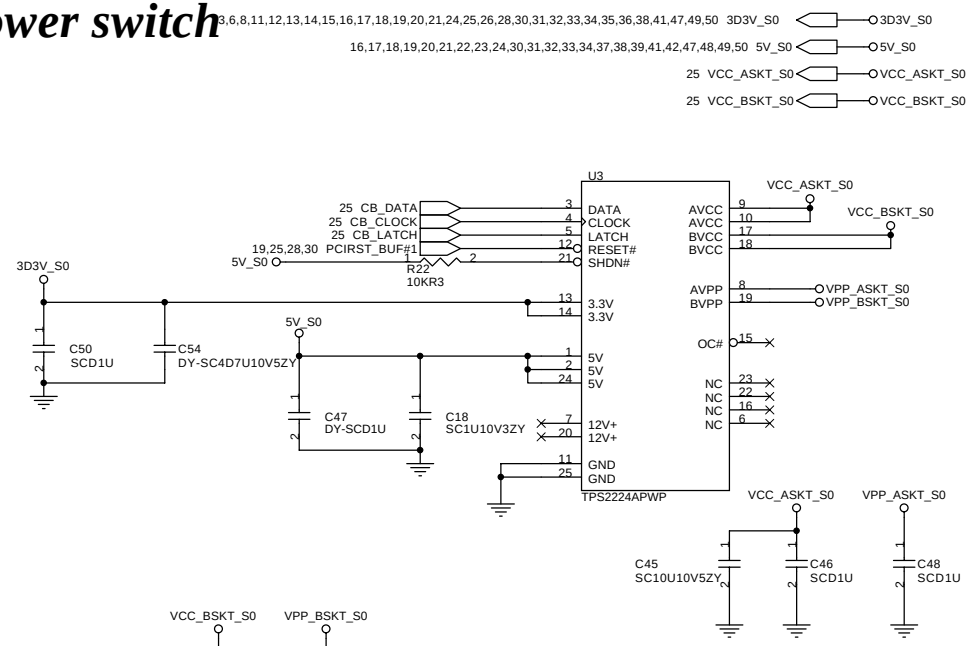
Upper = Slot0 / Signal A = Conn B
Lower = Slot1 / Signal B = Conn A



1394 Connector **



Power switch



緯創資通 Wistron Corporation
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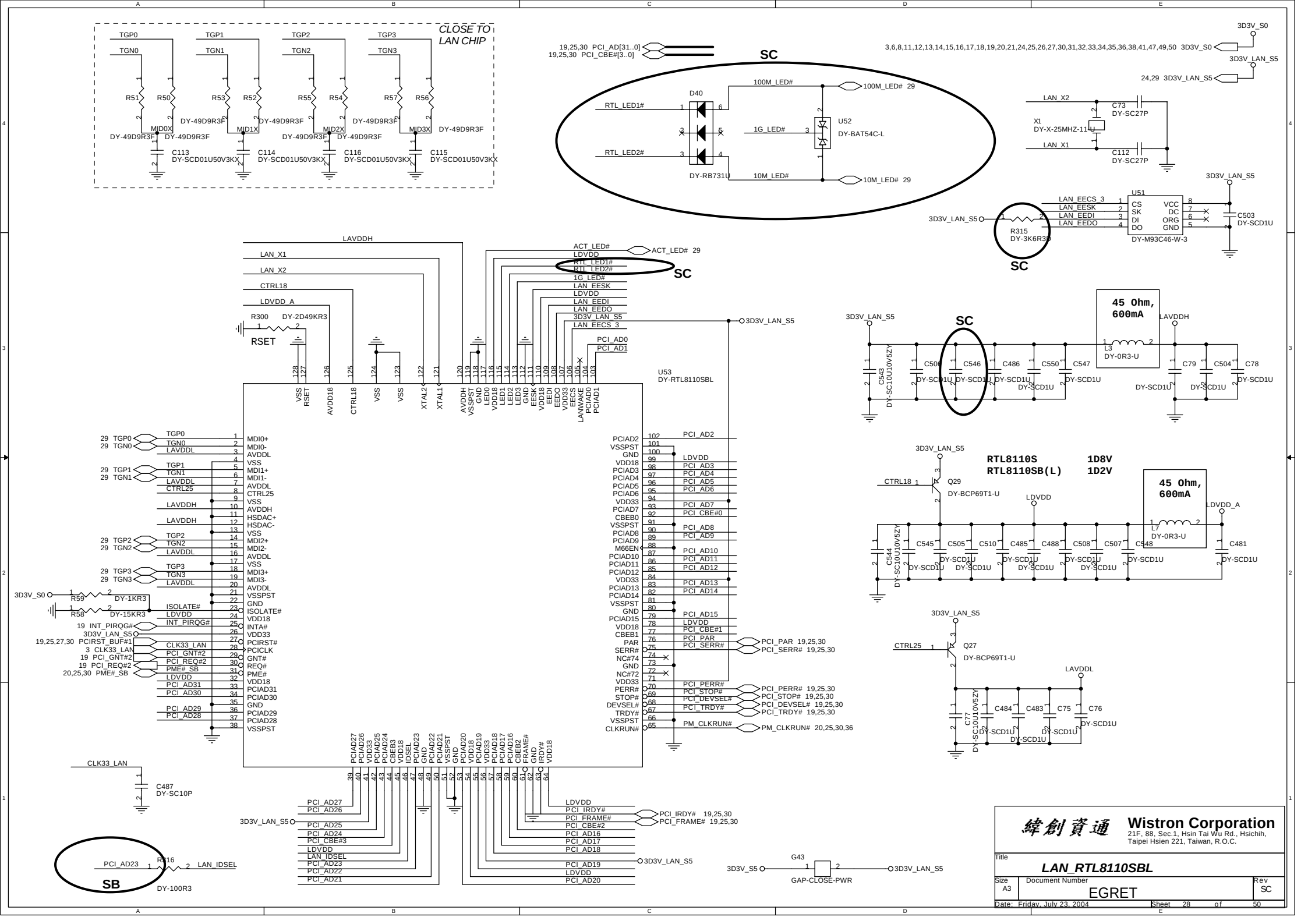
Taipei Hsien 221, Taiwan, R.O.C.

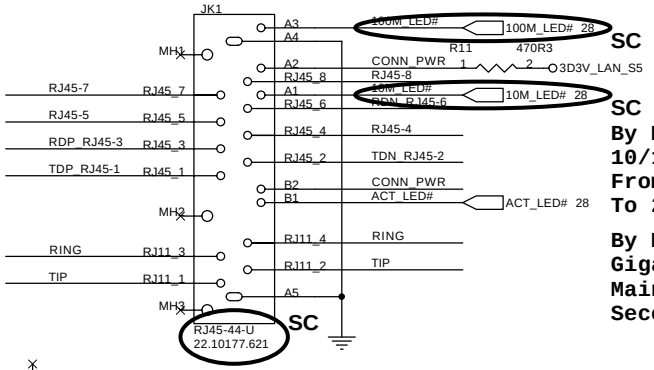
Title: PCMCA SLOT_1394 CONN
Size: A3
Document Number: EGRET
Rev: SC
Date: Friday, July 23, 2004
Sheet 27 of 50



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LAN_RTL8110SBL***	
Size A3	Document Number EGRET	Rev SC
Date: Friday, July 23, 2004	Sheet 28 of 50	

Link: Green - 10Mbps/802.11b
Orange - 100Mbps/802.11a
Yellow - 1Gbps

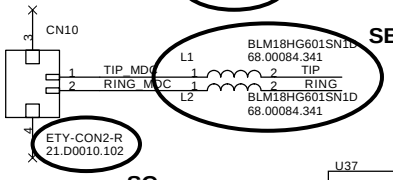
Activity: Yellow



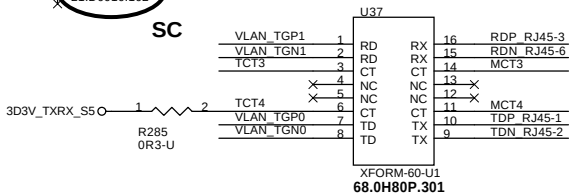
SC

By ME requset for
10/100 LAN change P/N:
From 22.10177.601
To 22.10177.621

By ME requset for
GigaLAN JK1 P/N:
Main 22.10177.601
Second 22.10245.771

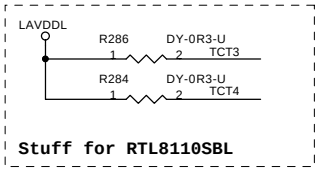


By ME requset change P/N:
From 20.D0121.102
To 21.D0010.102



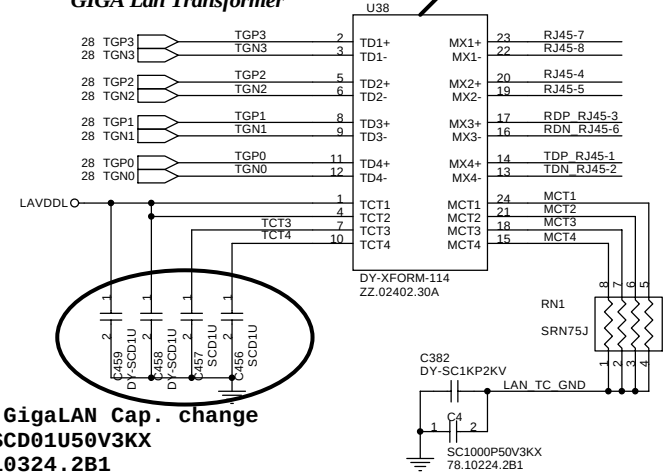
Stuff for VT6103L
10/100M Lan Transformer

By Sourcer requset change P/N:
From 68.H0013.301
To 68.0H80P.301

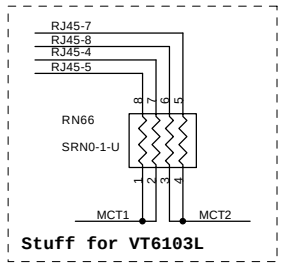


By Sourcer requset change P/N:
From 68.H5015.301
To 68.02402.30A

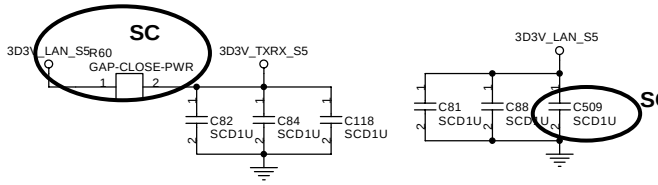
GIGA Lan Transformer

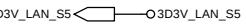


1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

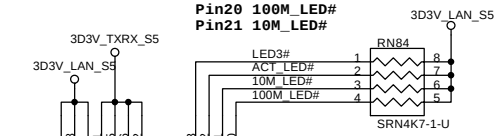


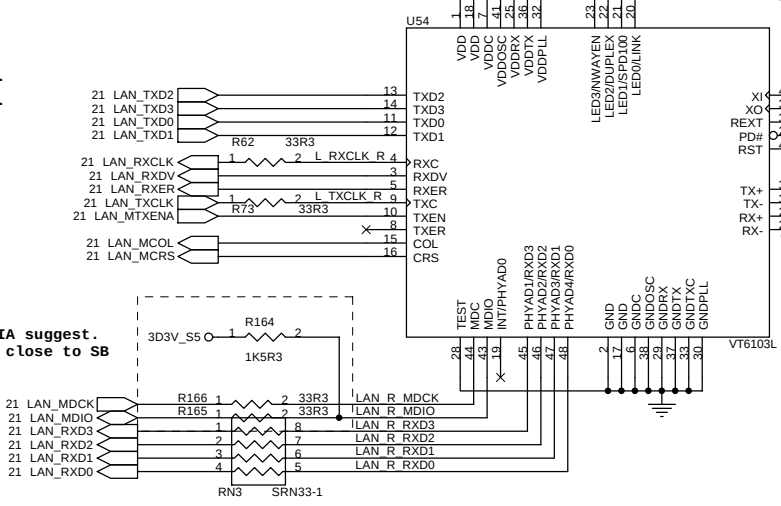
For GigaLAN Cap. change
to SCD01U50V3KX
78.10324.2B1





05/11
For VIA suggest.
Pin20 100M_LED#
Pin21 10M_LED#

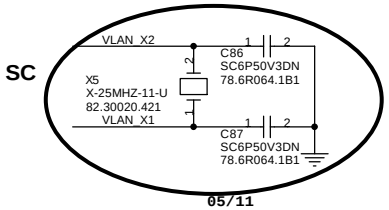




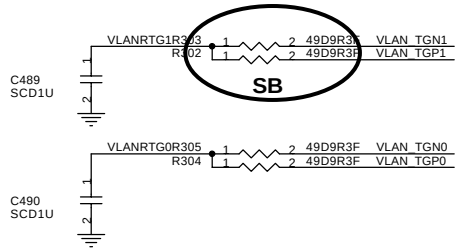
05/11
For VIA suggest.
Change from 2K26
ohm to 6K49 ohm

05/11
For VIA suggest.
VT6103L need 2U
capacitor for PHYRST#

05/11
For VIA suggest.
Place close to SB



05/11
For VIA suggest.
Change from 18P to 22P



By KDS suggested change
X5
From 82.30020.161
To 82.30023.421
C86, C87
From 22P To 6P

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LAN_CONN&10/100LAN*

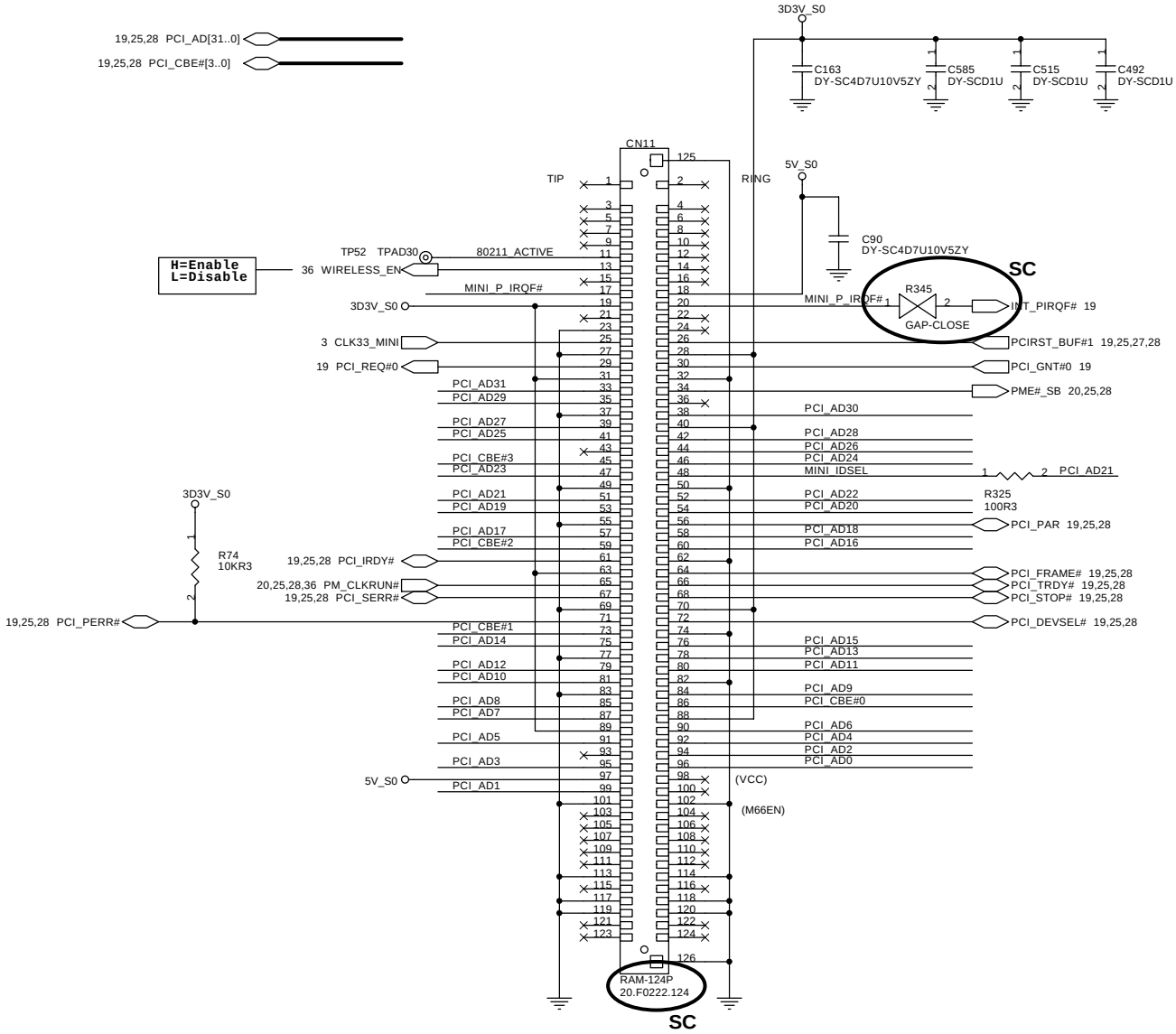
Size: A3 | Document Number: EGRET | Rev: SC

Date: Friday, July 23, 2004 | Sheet 29 of 50

MINI-PCI

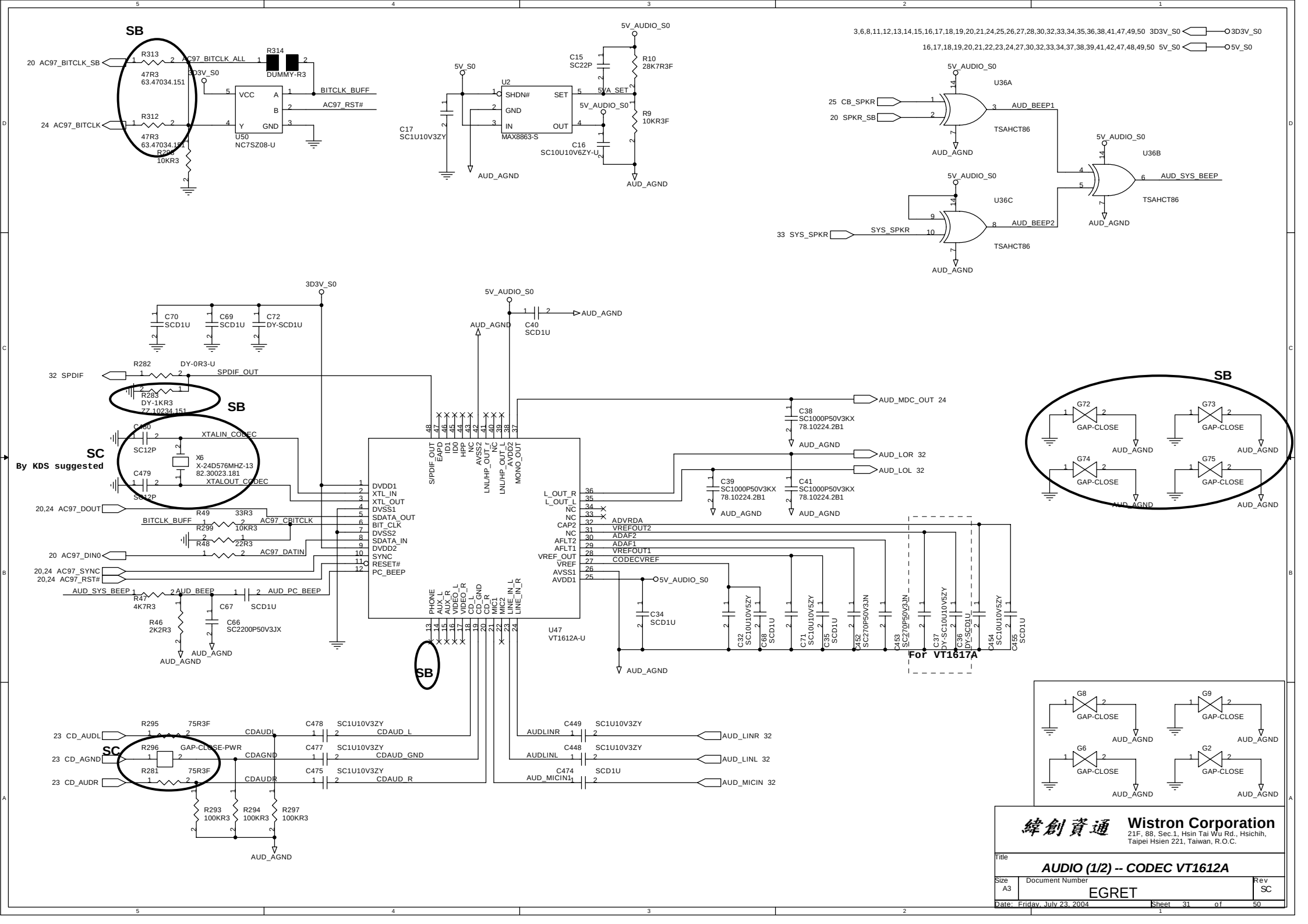
3,6,8,11,12,13,14,15,16,17,18,19,20,21,24,25,26,27,28,31,32,33,34,35,36,38,41,47,49,50 3D3V_S0 — 3D3V_S0

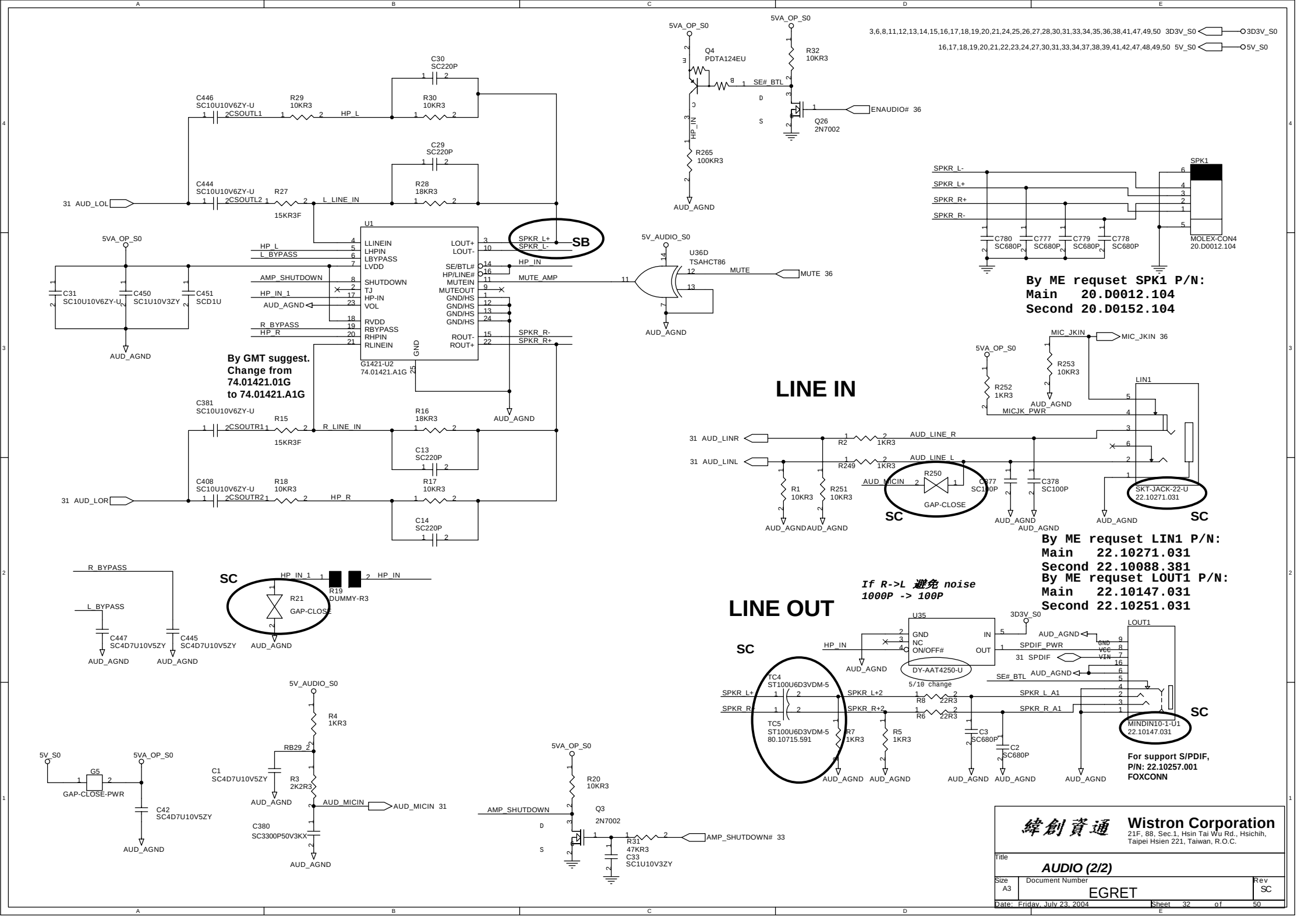
16,17,18,19,20,21,22,23,24,27,31,32,33,34,37,38,39,41,42,47,48,49,50 5V_S0 — 5V_S0

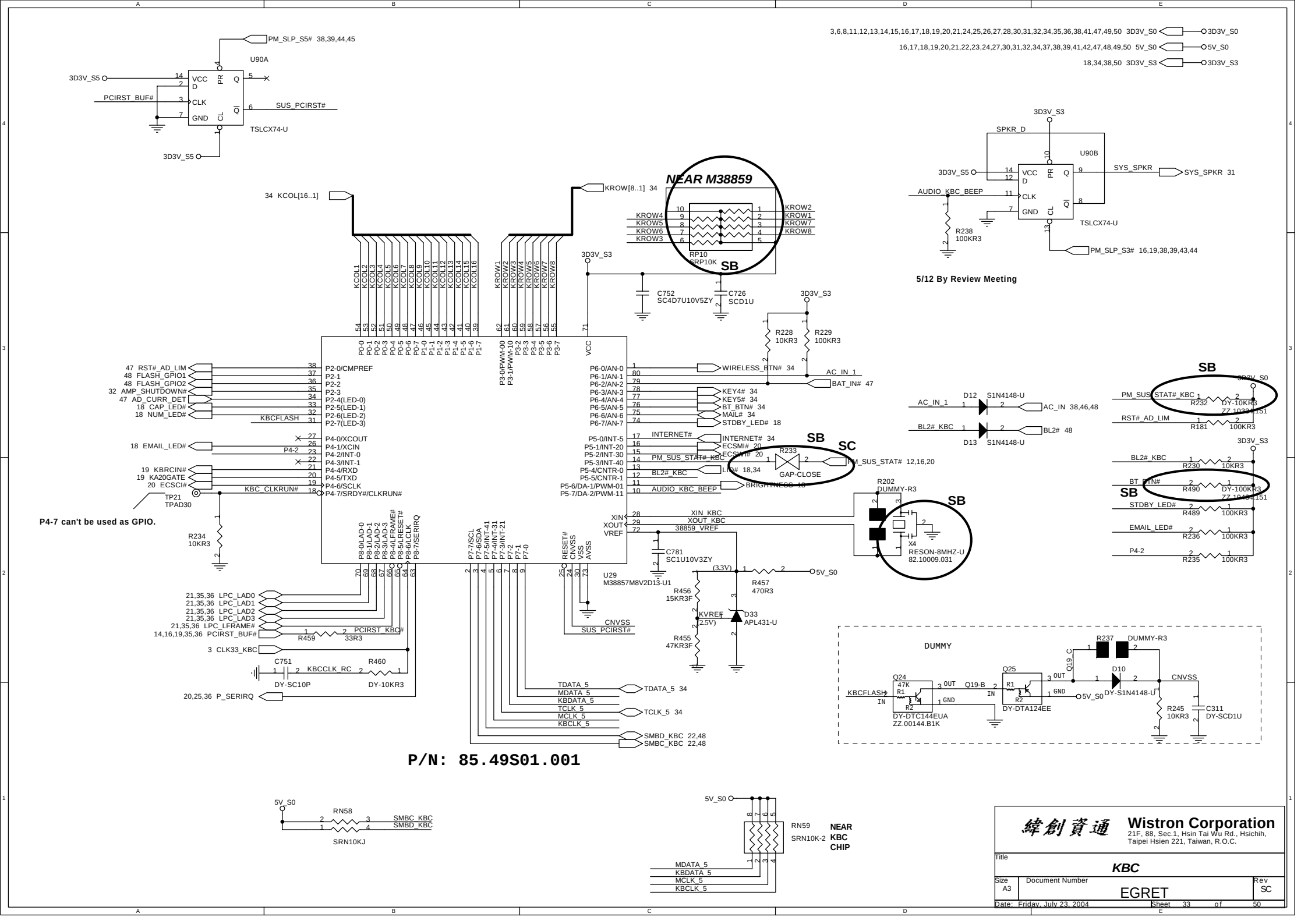


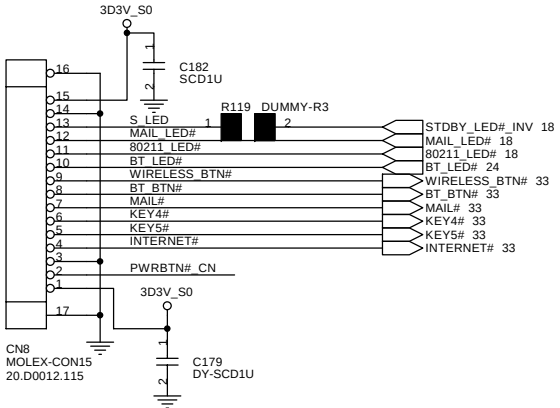
By ME requset CN11 P/N:
Main 20.F0222.124
Second 62.10034.031

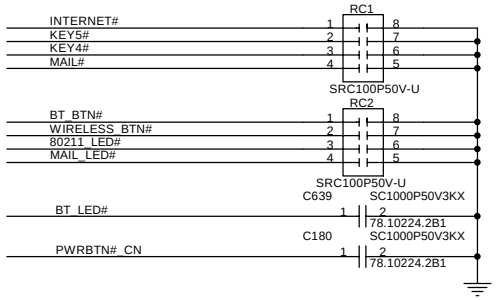
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI-PCI***	
Size A3	Document Number EGRET	Rev SC
Date: Friday, July 23, 2004	Sheet 30 of 50	


SB
20 AC97_BITCLK_SB
R313
47R3
63.47034.151
AC97_BITCLK_ALL
R314
DUMMY-R3
3D3V_S0
VCC
A
B
Y
GND
U50
NC7SZ08-U
BITCLK_BUFF
AC97_RST#
24 AC97_BITCLK
R312
47R3
63.47034.151
R299
10KR3
5V_AUDIO_S0
5V_S0
U2
SHDN#
SET
GND
IN
OUT
MAX8863-S
C15
SC22P
R10
28K7R3F
5VA_SET
R9
10KR3F
C17
SC1U10V3ZY
C16
SC10U10V6ZY-U
AUD_AGND
3,6,8,11,12,13,14,15,16,17,18,19,20,21,24,25,26,27,28,30,32,33,34,35,36,38,41,47,49,50 3D3V_S0
16,17,18,19,20,21,22,23,24,27,30,32,33,34,37,38,39,41,42,47,48,49,50 5V_S0
U36A
25 CB_SPKR
20 SPKR_SB
AUD_BEEP1
TSAHCT86
U36B
AUD_SYS_BEEP
U36C
33 SYS_SPKR
SYS_SPKR
AUD_BEEP2
3D3V_S0
C70
SCD1U
C69
SCD1U
C72
DY-SCD1U
C40
SCD1U
32 SPDIF
R282
DY-0R3-U
SPDIF_OUT
R283
DY-1KR3
ZZ.10234.151
SB
SC
By KDS suggested
C480
SC12P
XTALIN_CODEC
X6
X-24D576MHZ-13
82.30023.181
C479
SC12P
XTALOUT_CODEC
20,24 AC97_DOUT
R49
33R3
BITCLK_BUFF
AC97_CBITCLK
R299
10KR3
R48
22R3
20 AC97_DIN0
AC97_DATIN
20,24 AC97_SYNC
20,24 AC97_RST#
AUD_SYS_BEEP
R47
4K7R3
AUD_BEEP
AUD_PC_BEEP
C67
SCD1U
R46
2K2R3
C66
SC2200P50V3JX
DVDD1
XTL_IN
XTL_OUT
DVSS1
SDATA_OUT
BIT_CLK
DVSS2
SDATA_IN
DVDD2
SYNC
RESET#
PC_BEEP
S/PDIF_OUT
EAPD
ID1
ID0
HPP
NC
AVSS2
LNL/HP_OUT_r
NC
LNL/HP_OUT_L
AVDD2
MONO_OUT
PHONE
AUX_L
AUX_R
VIDEO_L
VIDEO_R
CD_L
CD_GND
CD_R
MIC1
MIC2
LINE_IN_L
LINE_IN_R
L_OUT_R
L_OUT_L
NC
NC
CAP2
NC
AFLT2
AFLT1
VREF_OUT
VREF
AVSS1
AVDD1
ADVRDA
VREFOUT2
ADAF2
ADAF1
VREFOUT1
CODECVREF
U47
VT1612A-U
AUD_MDC_OUT 24
C38
SC1000P50V3KXX
78.10224.2B1
AUD_LOR 32
AUD_LOL 32
C39
SC1000P50V3KXX
78.10224.2B1
C41
SC1000P50V3KXX
78.10224.2B1
C34
SCD1U
C32
SC10U10V5ZY
C68
SCD1U
C71
SC10U10V5ZY
C35
SCD1U
C462
SC270P50V3JN
C453
SC270P50V3JN
C37
DY-SC10U10V5ZY
C36
DY-SCD1U
C454
SC10U10V5ZY
C455
SCD1U
For VT1617A
SB
G72
GAP-CLOSE
G73
GAP-CLOSE
G74
GAP-CLOSE
G75
GAP-CLOSE
G8
GAP-CLOSE
G9
GAP-CLOSE
G6
GAP-CLOSE
G2
GAP-CLOSE
23 CD_AUDL
23 CD_AGND
23 CD_AUDR
SC
R295
75R3F
R296
GAP-CLOSE-PWR
R281
75R3F
CDAUDL
CDAGND
CDAUDR
C478
SC1U10V3ZY
C477
SC1U10V3ZY
C475
SC1U10V3ZY
CDAUD_L
CDAUD_GND
CDAUD_R
R293
100KR3
R294
100KR3
R297
100KR3
AUDLINR
AUDLINL
AUD_MICIN1
C449
SC1U10V3ZY
C448
SC1U10V3ZY
C474
SCD1U
AUD_LINR 32
AUD_LINL 32
AUD_MICIN 32
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO (1/2) -- CODEC VT1612A
Size
A3
Document Number
EGRET
Rev
SC
Date: Friday, July 23, 2004
Sheet 31 of 50

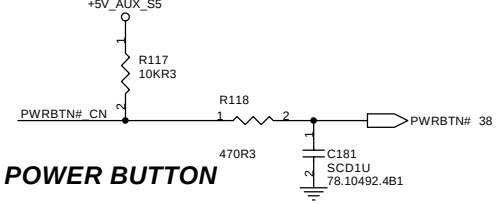

LINE IN
LINE OUT
By GMT suggest.
Change from
74.01421.01G
to 74.01421.A1G
By ME requset SPK1 P/N:
Main 20.D0012.104
Second 20.D0152.104
By ME requset LIN1 P/N:
Main 22.10271.031
Second 22.10088.381
By ME requset LOUT1 P/N:
Main 22.10147.031
Second 22.10251.031
If R->L 避免 noise
1000P -> 100P
For support S/PDIF,
P/N: 22.10257.001
FOXCONN
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO (2/2)
EGRET
Friday, July 23, 2004
Sheet 32 of 50


3,6,8,11,12,13,14,15,16,17,18,19,20,21,24,25,26,27,28,30,31,32,34,35,36,38,41,47,49,50 3D3V_S0
16,17,18,19,20,21,22,23,24,27,30,31,32,34,37,38,39,41,42,47,48,49,50 5V_S0
18,34,38,50 3D3V_S3
PM_SLP_S5# 38,39,44,45
U90A
3D3V_S5
PCIRST_BUF#
SUS_PCIRST#
TSLCX74-U
3D3V_S5
3D3V_S3
SPKR_D
U90B
SYS_SPKR
SYS_SPKR 31
AUDIO_KBC_BEEP
R238
100KR3
TSLCX74-U
PM_SLP_S3# 16,19,38,39,43,44
5/12 By Review Meeting
NEAR M38859
34 KCOL[16..1]
KROW[8..1] 34
KROW4
KROW5
KROW6
KROW3
KROW2
KROW1
KROW7
KROW8
RP10
8P10K
SB
3D3V_S3
C752
SC4D7U10V5ZY
C726
SCD1U
3D3V_S3
R228
10KR3
R229
100KR3
KCOL1
KCOL2
KCOL3
KCOL4
KCOL5
KCOL6
KCOL7
KCOL8
KCOL9
KCOL10
KCOL11
KCOL12
KCOL13
KCOL14
KCOL15
KCOL16
KROW1
KROW2
KROW3
KROW4
KROW5
KROW6
KROW7
KROW8
P0-0
P0-1
P0-2
P0-3
P0-4
P0-5
P0-6
P0-7
P1-0
P1-1
P1-2
P1-3
P1-4
P1-5
P1-6
P1-7
P3-0/PWM-00
P3-1/PWM-10
P3-2
P3-3
P3-4
P3-5
P3-6
P3-7
VCC
47 RST#_AD_LIM
48 FLASH_GPIO1
48 FLASH_GPIO2
32 AMP_SHUTDOWN#
47 AD_CURR_DET
18 CAP_LED#
18 NUM_LED#
KBCFLASH
P2-0/CMPREF
P2-1
P2-2
P2-3
P2-4(LED-0)
P2-5(LED-1)
P2-6(LED-2)
P2-7(LED-3)
18 EMAIL_LED#
P4-2
P4-0/XCOUT
P4-1/XCIN
P4-2/INT-0
P4-3/INT-1
P4-4/RXD
P4-5/TXD
P4-6/SCLK
P4-7/SRDY#/CLKRUN#
19 KBRCIN#
19 KA20GATE
20 ECSCI#
KBC_CLKRUN#
TP21
TPAD30
P4-7 can't be used as GPIO.
R234
10KR3
P6-0/AN-0
P6-1/AN-1
P6-2/AN-2
P6-3/AN-3
P6-4/AN-4
P6-5/AN-5
P6-6/AN-6
P6-7/AN-7
WIRELESS_BTN# 34
AC_IN_1
BAT_IN# 47
KEY4# 34
KEY5# 34
BT_BTN# 34
MAIL# 34
STDBY_LED# 18
P5-0/INT-5
P5-1/INT-20
P5-2/INT-30
P5-3/INT-40
P5-4/CNTR-0
P5-5/CNTR-1
P5-6/DA-1/PWM-01
P5-7/DA-2/PWM-11
INTERNET#
PM_SUS_STAT#_KBC
BL2#_KBC
AUDIO_KBC_BEEP
INTERNET# 34
ECSMI# 20
ECSWI# 20
LID# 18,34
BRIGHTNESS 18
SB
SC
R233
GAP-CLOSE
PM_SUS_STAT# 12,16,20
R202
DUMMY-R3
SB
X4
RESON-8MHZ-U
82.10009.031
XIN
XOUT
VREF
XIN_KBC
XOUT_KBC
38859_VREF
C781
SC1U10V3ZY
U29
M38857M8V2D13-U1
(3.3V)
R457
470R3
5V_S0
R456
15KR3F
KVREF
(2.5V)
D33
APL431-U
R455
47KR3F
P8-0/LAD-0
P8-1/LAD-1
P8-2/LAD-2
P8-3/LAD-3
P8-4/LFRAME#
P8-5/LRESET#
P8-6/LCLK
P8-7/SERIRQ
P7-7/SCL
P7-6/SDA
P7-5/INT-41
P7-4/INT-31
P7-3/INT-21
P7-2
P7-1
P7-0
RESET#
CNVSS
VSS
AVSS
21,35,36 LPC_LAD0
21,35,36 LPC_LAD1
21,35,36 LPC_LAD2
21,35,36 LPC_LAD3
21,35,36 LPC_LFRAME#
14,16,19,35,36 PCIRST_BUF#
PCIRST_KBC#
R459
33R3
3 CLK33_KBC
C751
DY-SC10P
KBCCLK_RC
R460
DY-10KR3
20,25,36 P_SERIRQ
CNVSS
SUS_PCIRST#
TDATA_5
MDATA_5
KBDATA_5
TCLK_5
MCLK_5
KBCLK_5
KBCLK_5
SMBD_KBC 22,48
SMBC_KBC 22,48
AC_IN_1
D12
S1N4148-U
AC_IN 38,46,48
BL2# KBC
D13
S1N4148-U
BL2# 48
SB
PM_SUS_STAT#_KBC
R232
DY-10KR3
ZZ.10234.151
RST#_AD_LIM
R181
100KR3
3D3V_S3
BL2#_KBC
R230
10KR3
BT_BTN#
R490
DY-100KR3
ZZ.10184.151
STDBY_LED#
R489
100KR3
EMAIL_LED#
R236
100KR3
P4-2
R235
100KR3
DUMMY
R237
DUMMY-R3
Q24
47K
R1
R2
DY-DTC144EUA
ZZ.00144.B1K
KBCFLASH
Q19-B
Q25
R1
R2
DY-DTA124EE
Q19
D10
DY-S1N4148-U
CNVSS
5V_S0
R245
10KR3
C311
DY-SCD1U
P/N: 85.49S01.001
5V_S0
RN58
SMBC_KBC
SMBD_KBC
SRN10KJ
5V_S0
RN59
SRN10K-2
NEAR
KBC
CHIP
MDATA_5
KBDATA_5
MCLK_5
KBCLK_5
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC
Size
A3
Document Number
EGRET
Rev
SC
Date: Friday, July 23, 2004
Sheet 33 of 50

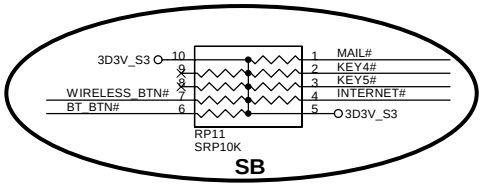




By ME requset CN8 P/N:
Main 20.D0012.115
Second 20.D0092.115

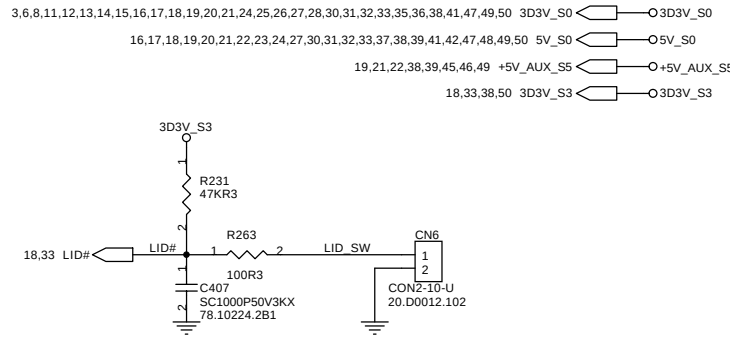


POWER BUTTON

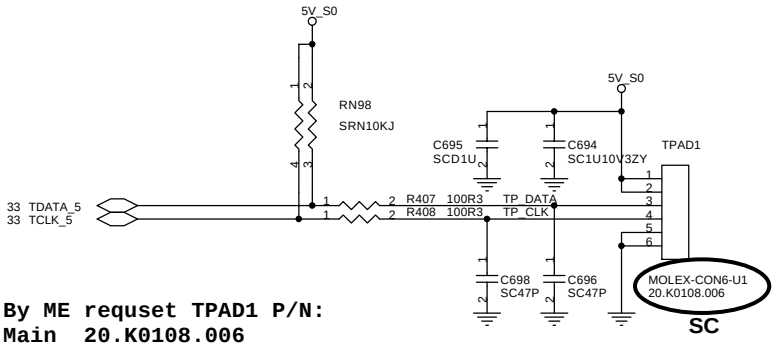


SB

Launch Board CONN



Cover Up Switch

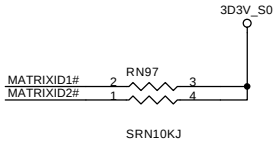


SC

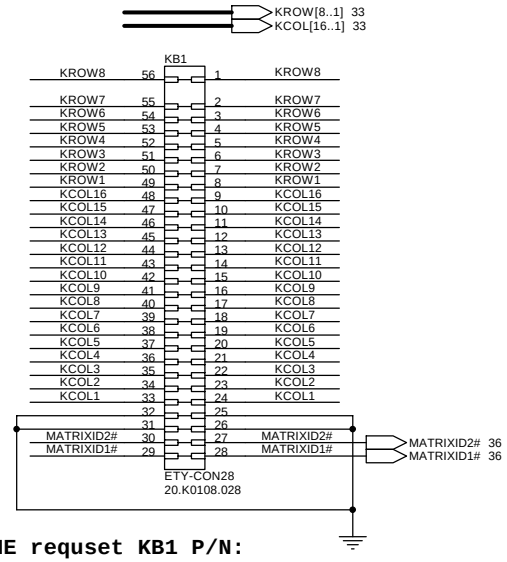
By ME requset TPAD1 P/N:
Main 20.K0108.006
Second 20.K0021.006

TOUCH PAD

Internal KeyBoard CONN

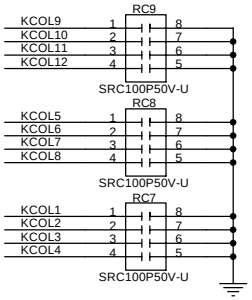


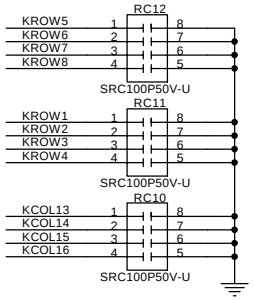
Keyboard matrix	(from vendor)			
	US	Jap	Eur	Other
Low Bit MATRIXID1#	1	1	0	0
High Bit MATRIXID2#	1	0	1	0



By ME requset KB1 P/N:
Main 20.K0108.028
Second 20.K0021.028

EMI Bypass cap.





緯創資通 **Wistron Corporation**
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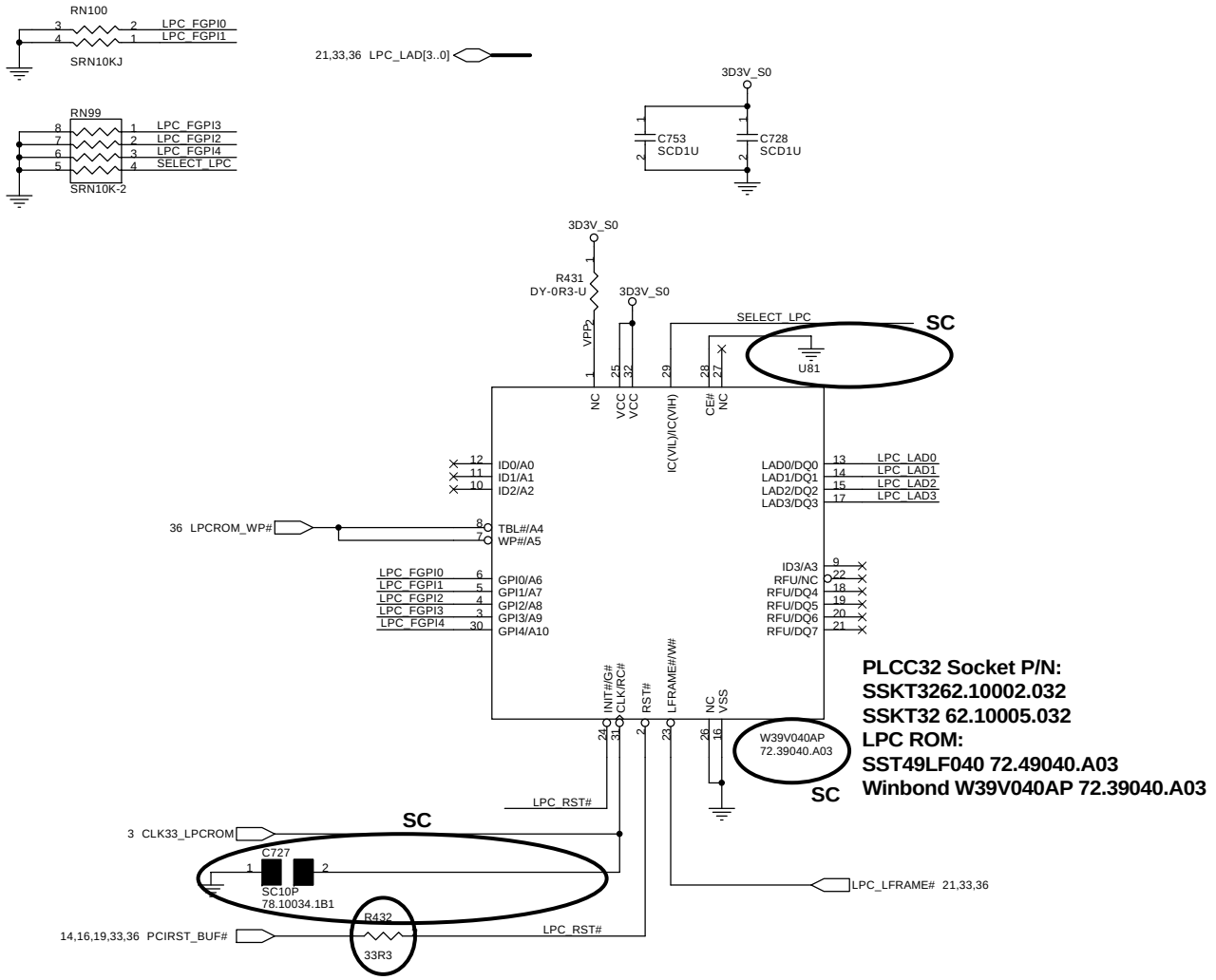
Title: ***LAUNCH / TOUCHPAD / KB CONN***

Size: A3 | Document Number: EGRET | Rev: SC

Date: Friday, July 23, 2004 | Sheet 34 of 50

3,6,8,11,12,13,14,15,16,17,18,19,20,21,24,25,26,27,28,30,31,32,33,34,36,38,41,47,49,50 3D3V_S0 3D3V_S0



PLCC32 Socket P/N:
SSKT3262.10002.032
SSKT32 62.10005.032
LPC ROM:
SST49LF040 72.49040.A03
Winbond W39V040AP 72.39040.A03

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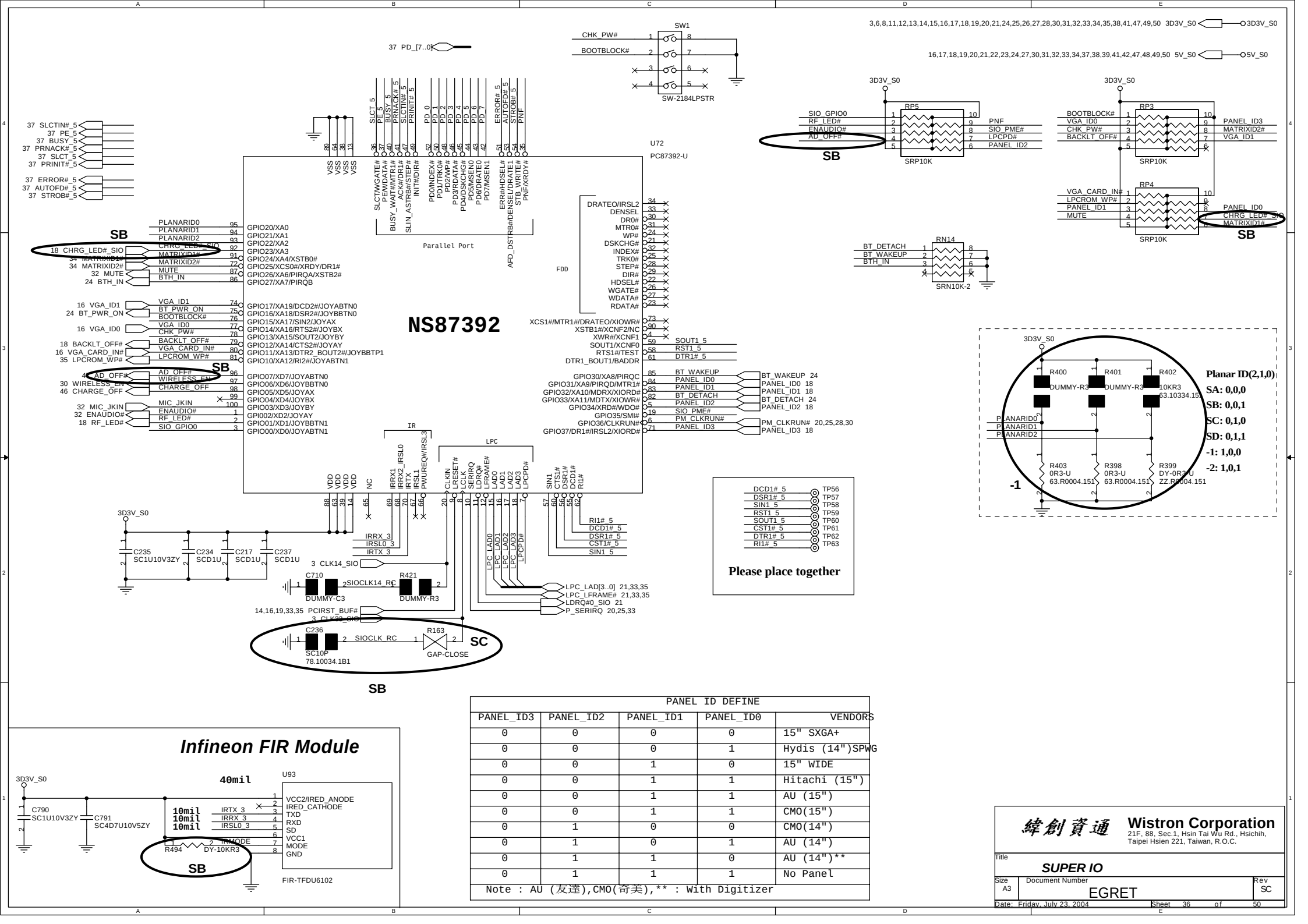
Title: *LPCROM / DEBUG PORT*		
Size: A3	Document Number: EGRET	Rev: SC
Date: Friday, July 23, 2004	Sheet 35 of 50	



PANEL ID DEFINE				
PANEL_ID3	PANEL_ID2	PANEL_ID1	PANEL_ID0	VENDORS
0	0	0	0	15" SXGA+
0	0	0	1	Hydis (14")SPWG
0	0	1	0	15" WIDE
0	0	1	1	Hitachi (15")
0	0	1	1	AU (15")
0	0	1	1	CMO(15")
0	1	0	0	CMO(14")
0	1	0	1	AU (14")
0	1	1	0	AU (14")**
0	1	1	1	No Panel

Note : AU (友達),CMO(奇美),** : With Digitizer

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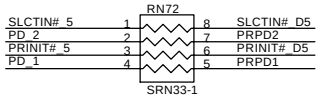
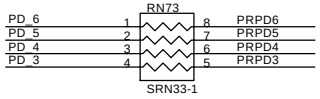
Title: ***SUPER IO***

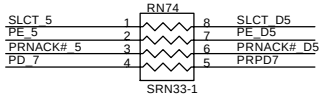
Size: A3 | Document Number: EGRET | Rev: SC

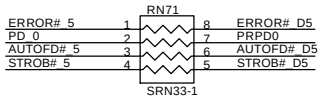
Date: Friday, July 23, 2004 | Sheet 36 of 50

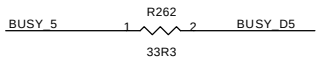
PRINTER PORT

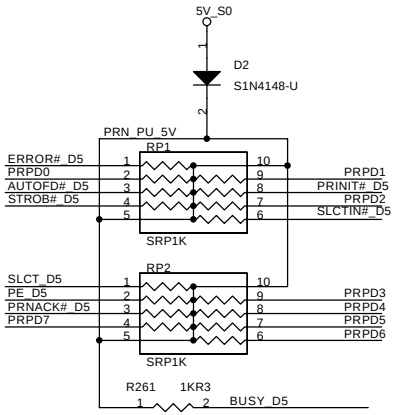




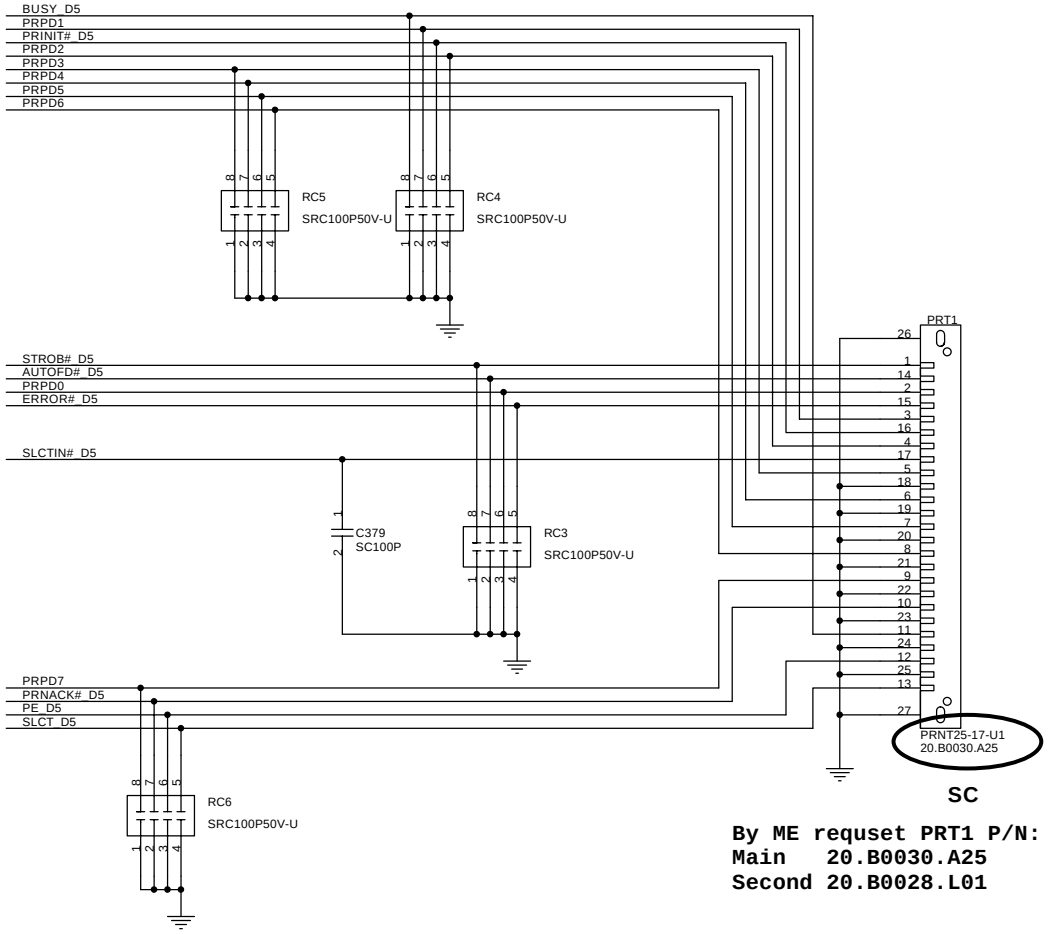








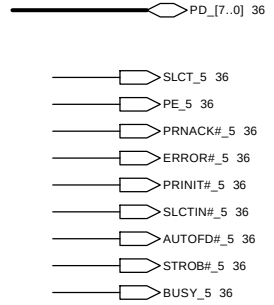
CHECK PULL HIGH



SC

By ME requset PRT1 P/N:
Main 20.B0030.A25
Second 20.B0028.L01

FROM SIO



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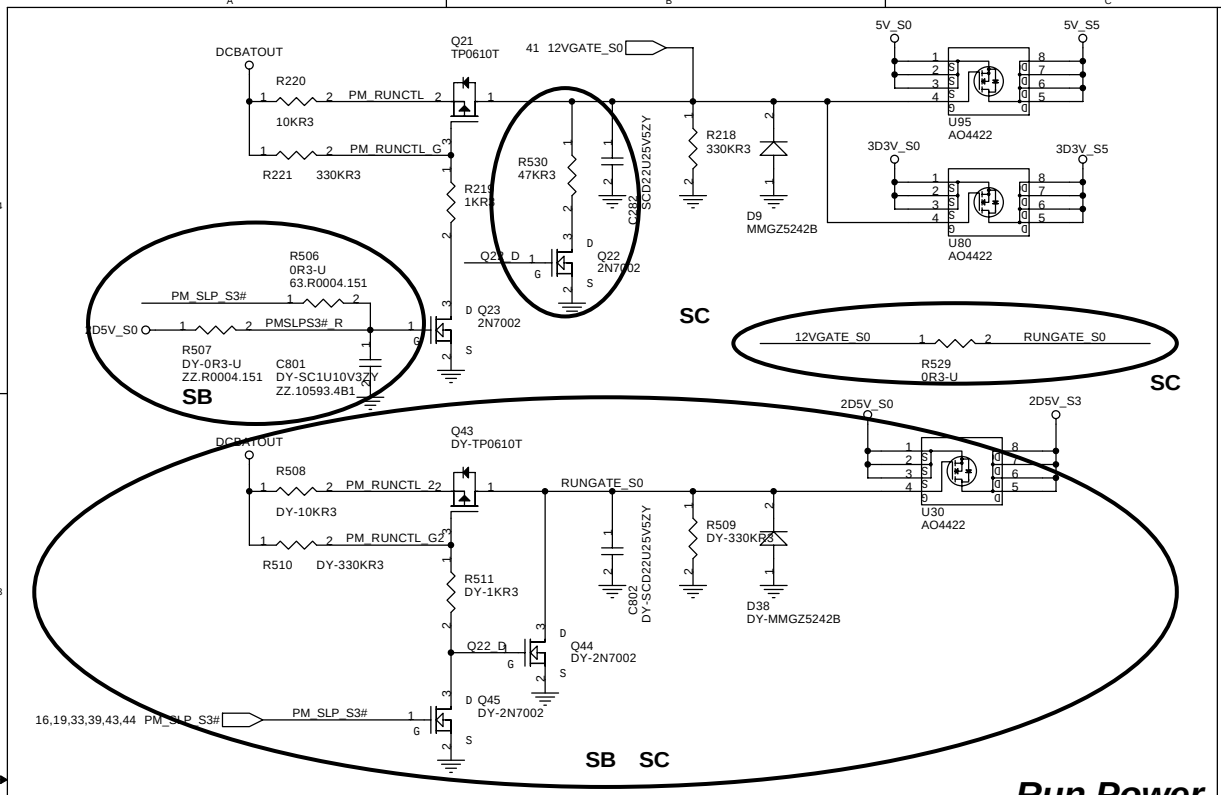
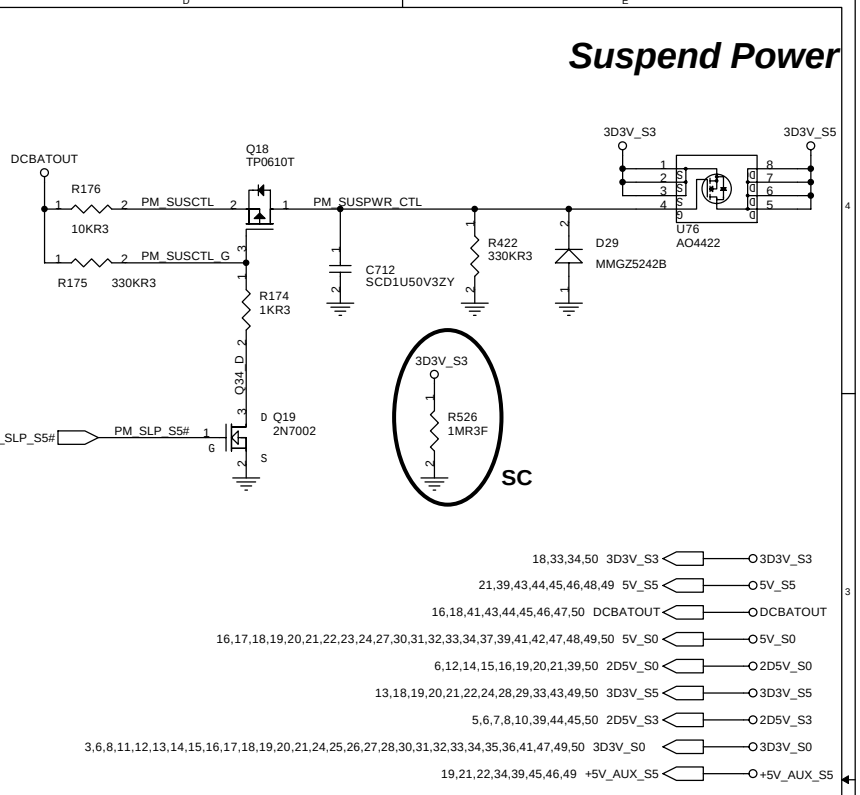
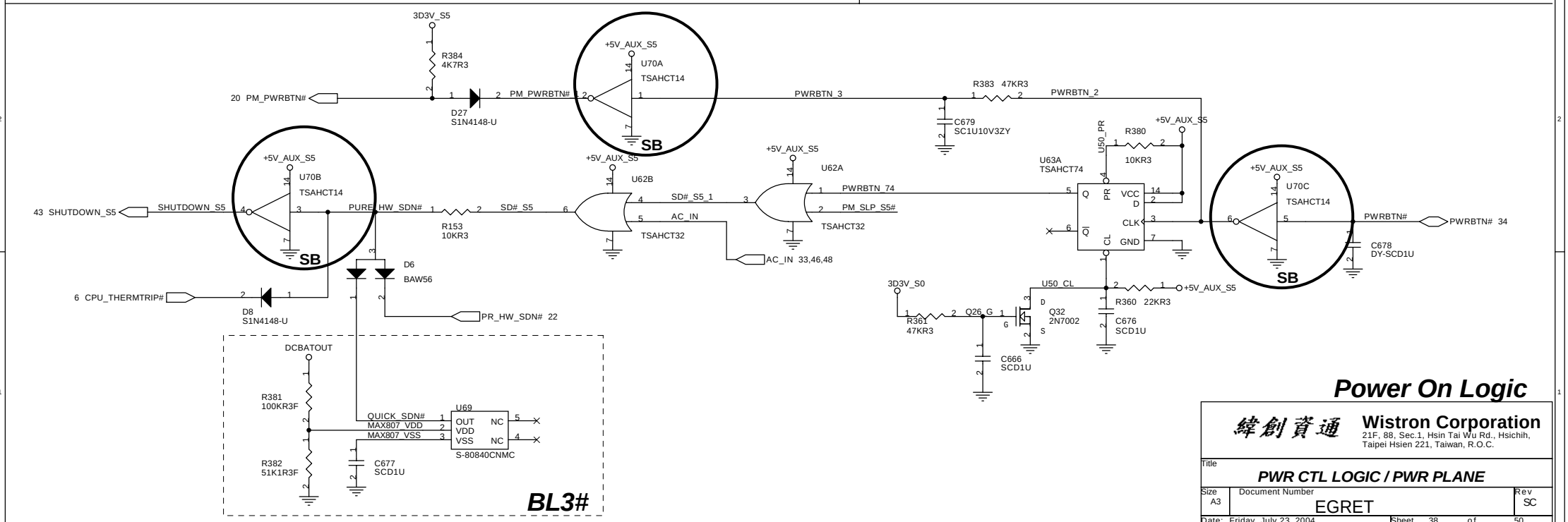
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Printer PORT***		
Size: A3	Document Number: EGRET	Rev: SC
Date: Friday, July 23, 2004	Sheet 37 of 50	







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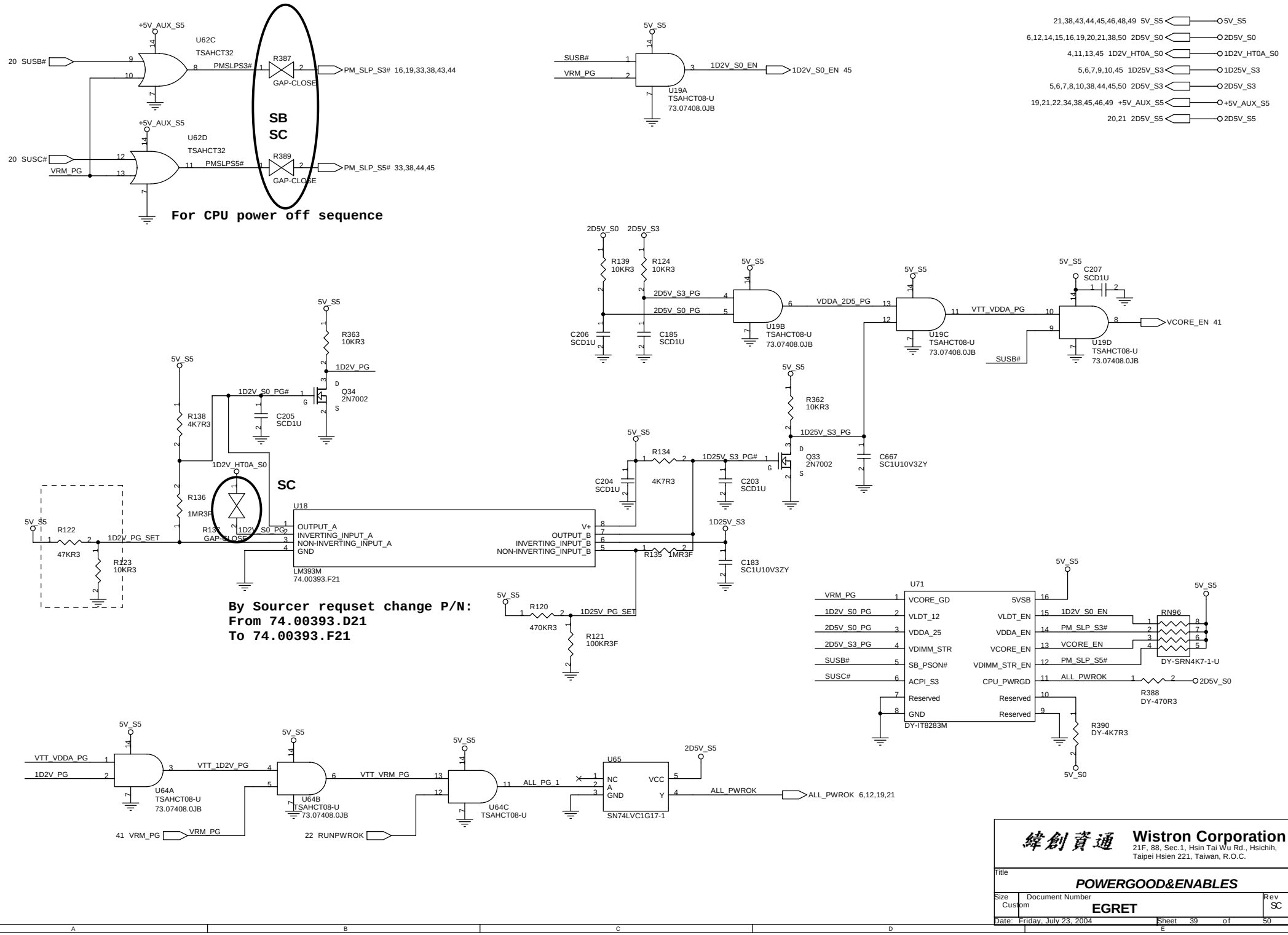
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PWR CTL LOGIC / PWR PLANE***

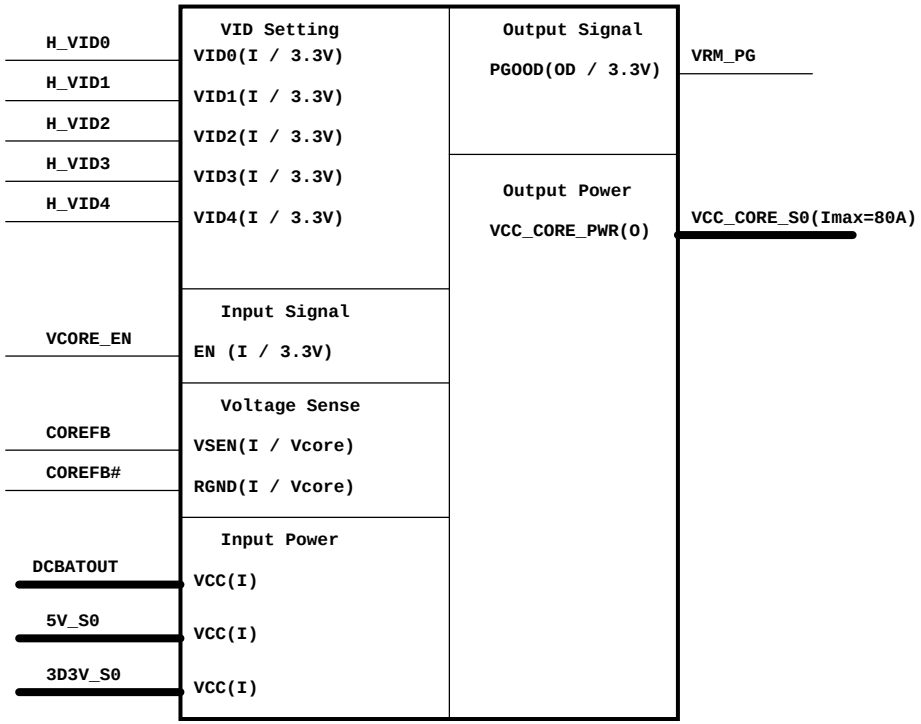
Size	Document Number	Rev
A3	EGRET	SC

Date: Friday, July 23, 2004 Sheet 38 of 50

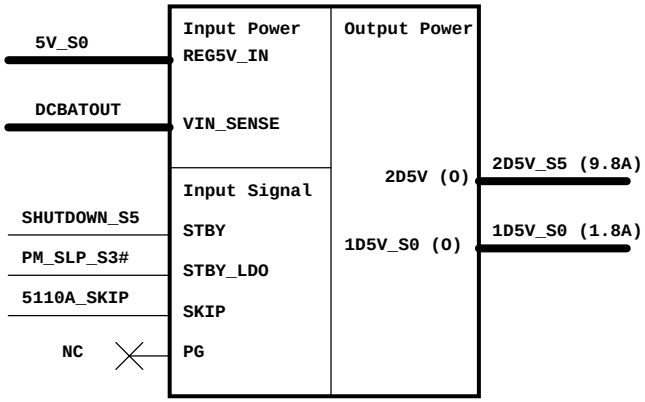


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***POWERGOOD&ENABLES***
Size: Custom	Document Number: **EGRET**
Rev	SC
Date: Friday, July 23, 2004	Sheet 39 of 50

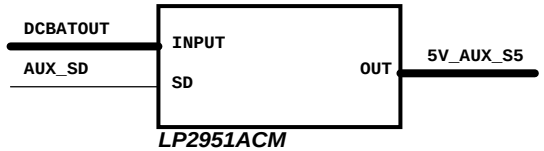
CPU_CORE
Intersil 6559CR + ISL6209CB*2



TI TPS5110
2D5V/1D5V

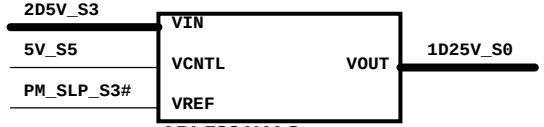


5V_AUX_S5



LP2951ACM

1D25V_S3

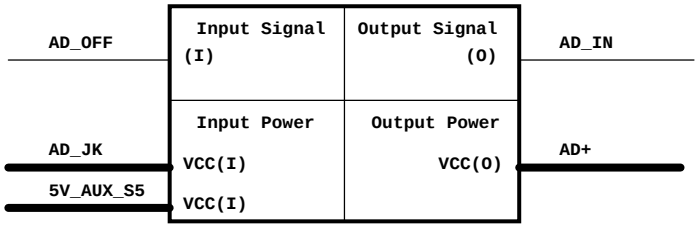


APL5331KAC

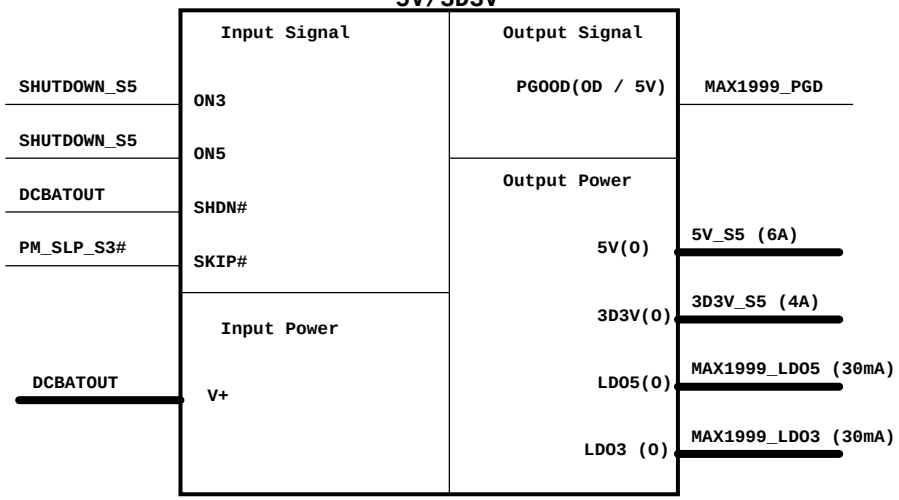
1D2V_S0

APL5331KAC

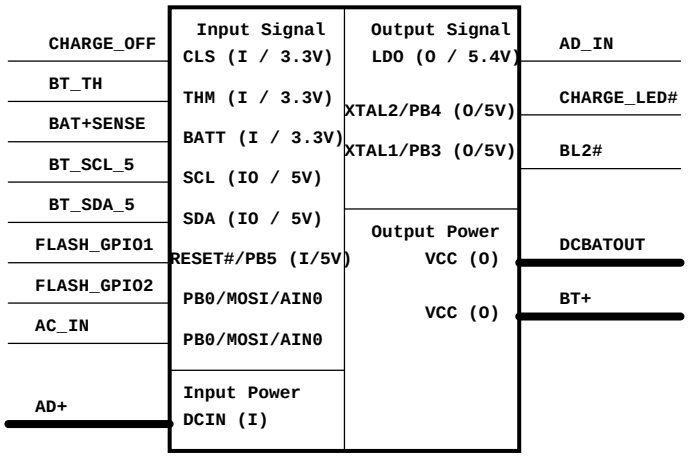
Adapter



Max1999
5V/3D3V



Charger_Max1645 + Tiny12



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

Size	Document Number	Rev
A3	EGRET	SC

Date: Friday, July 23, 2004 Sheet 40 of 50

Vcore_CPU=1.500V
Iomax=52.9A
Vcore_CPU=1.400V
Iomax=42.7A

53A*1.5=79.5A (OCP),=>79.5A/2Phase=39.75A/Phase
90uA*Rsense=39.75A*(6.5m/2)*1.4
=>Rsense=2.0K

Vdrop is over spec under max loading

R value large, then offset small.
=> 3K or 4.99K?
Now=>Offset value is over 0.05V
If without offset =>R158=0ohm

Rt=10^[11.09-1.13log(fs)]
Rt=107K,=>fs=230KHz
But real freq.=270KHz

Follow MOSFET rise time spec.

Gain value large, then bandwidth large!
=> 2.74K or 3.65K

PLACE IN THE BACK OF CPU

SHOWA 2V/ 7.3*4.3*1.0mm / SMD
79.22719.20B
ESR=9mohm , Iripplet=3.0A
2'nd Source:
NEC 220uF / 2.5V / ESR=9 / Iripple=3.7A 77.C2271.081
7.3*4.3*1.9 / NT$:8.0

SB Version:
Change U59 from ISL6209CB (74.06209.071)
to ISL6207CB-U (74.06207.071)

C216/C201/C140
Can not stuff!

DCR=1.3mohm+-10% / Imax=40A /
Panasonic /
ETQP2H0R7BF / 0.48uH /
13.4*13.3*4.9

Power-PAK
Id=46A
Rdson=6.9~8.6mohm

Power-PAK
Id=50A
Rdson=5.2~6.5mohm

SB Version:
53A=>2K

By PWRteam requset High side MosFETchange
From SI7888DP-U (84.07888.037)
To BSC059N03S-U (84.59N03.037)
Low side MosFETchange
From SI7338DP (84.07336.037)
To BSC042N03S-U (84.42N03.037)
2'nd Source:
H/S:SI7888DP (84.07888.037)
L/S:SI7886DP (84.07886.037)

Panasonic 25V / E1 Cap.
8.5*6.5mm / SMD
ESR=0.26ohm, Iripple=0.3A
FX Serial

Follow MOSFET rise time spec.
=> Mount 0ohm first.

SB Version:
Change U4 from ISL6209CB (74.06209.071)
to ISL6207CB-U (74.06207.071)

SB SC

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*CPU Vcore Power_1*
Size: Custom	Document Number: EGRET
Rev	SC
Date: Friday, July 23, 2004	Sheet 41 of 50

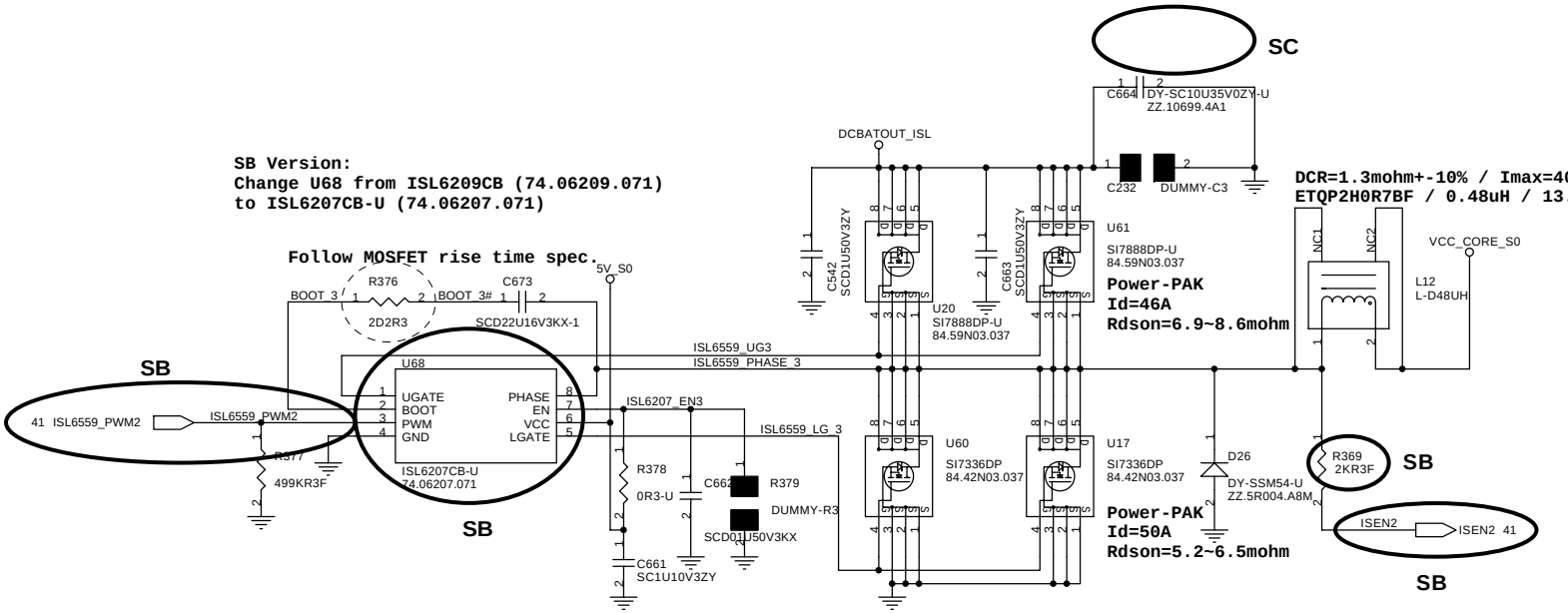


TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

41 DCBATOUT_ISL — DCBATOUT_ISL

7,41 VCC_CORE_S0 — VCC_CORE_S0

16,17,18,19,20,21,22,23,24,27,30,31,32,33,34,37,38,39,41,47,48,49,50 5V_S0 — 5V_S0

緯創資通 **Wistron Corporation**
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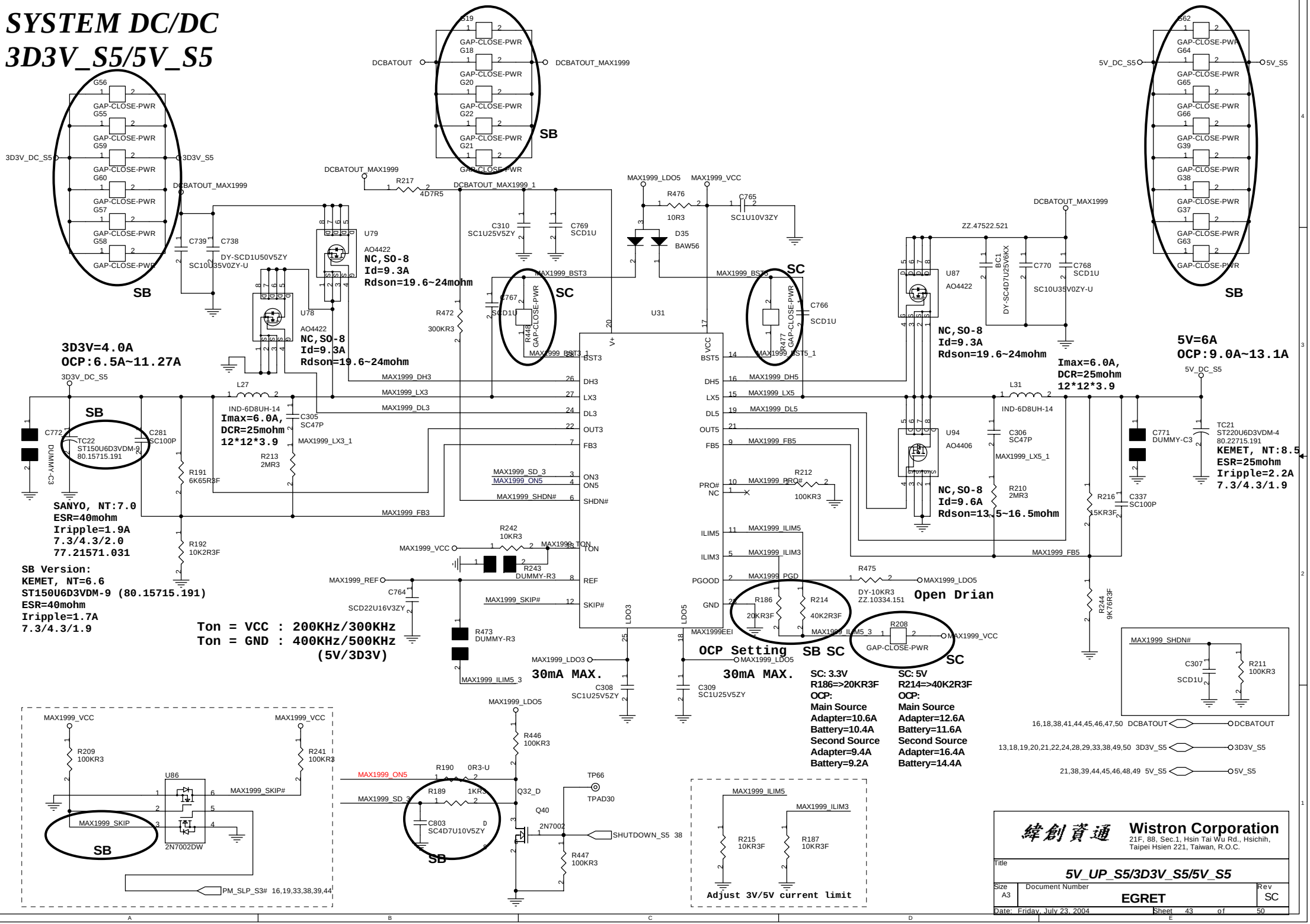
Taipei Hsien 221, Taiwan, R.O.C.

Title	***CPU Vcore Power_2***	
Size A3	Document Number **EGRET**	Rev SC
Date: Friday, July 23, 2004	Sheet 42 of 50	

SYSTEM DC/DC
3D3V_S5/5V_S5

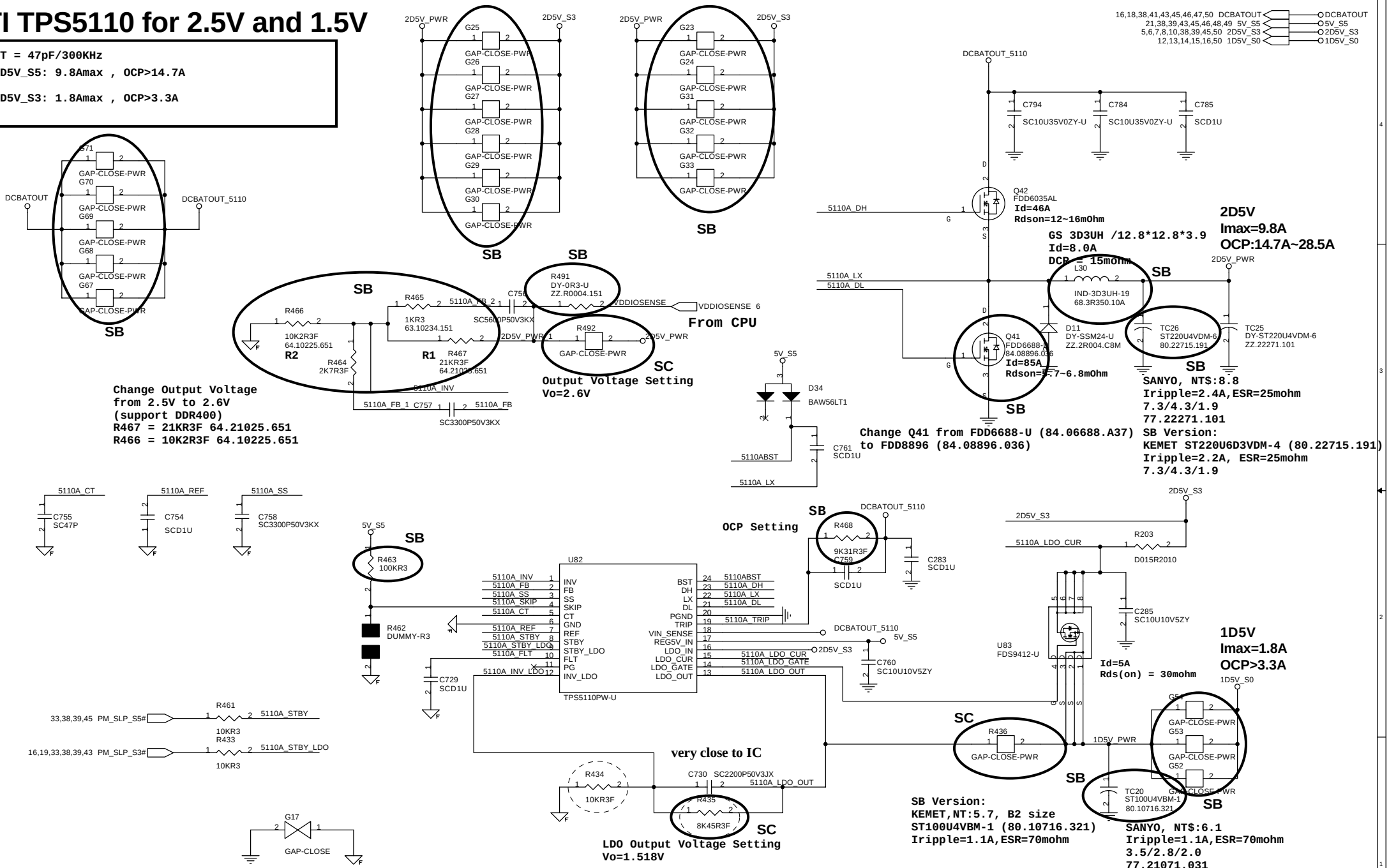


Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: 5V_UP_S5/3D3V_S5/5V_S5	
Size: A3	Document Number: EGRET
Rev: SC	
Date: Friday, July 23, 2004	Sheet 43 of 50

TI TPS5110 for 2.5V and 1.5V

CT = 47pF/300KHz
2D5V_S5: 9.8Amax , OCP>14.7A

1D5V_S3: 1.8Amax , OCP>3.3A



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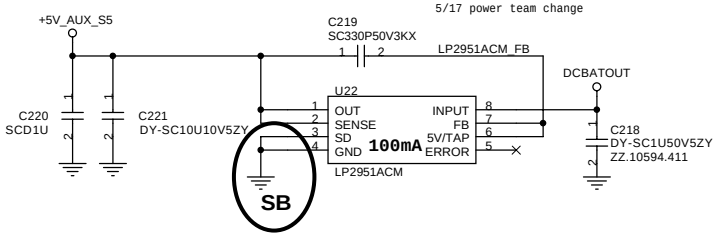
Title	***2D5V_S5/1D5V_S0_TPS5110***	
Size A3	Document Number **EGRET**	Rev **SC**
Date: Friday, July 23, 2004	Sheet 44 of 50	

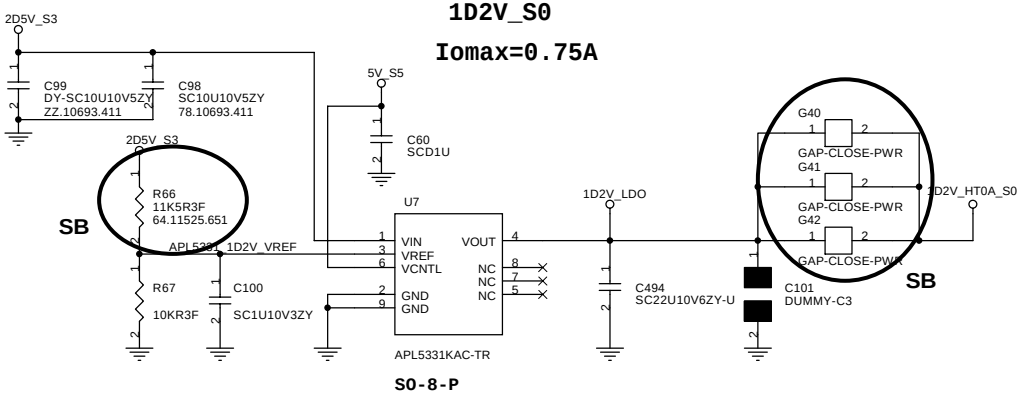
5V_AUX_S5

5/17 power team change

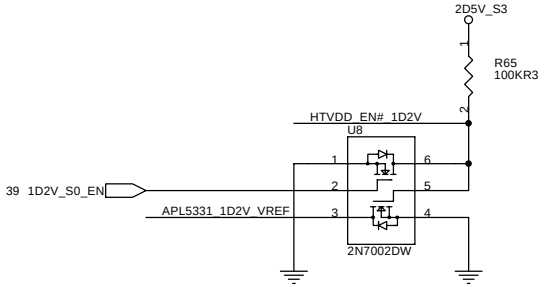


1D2V_S0

Iomax=0.75A

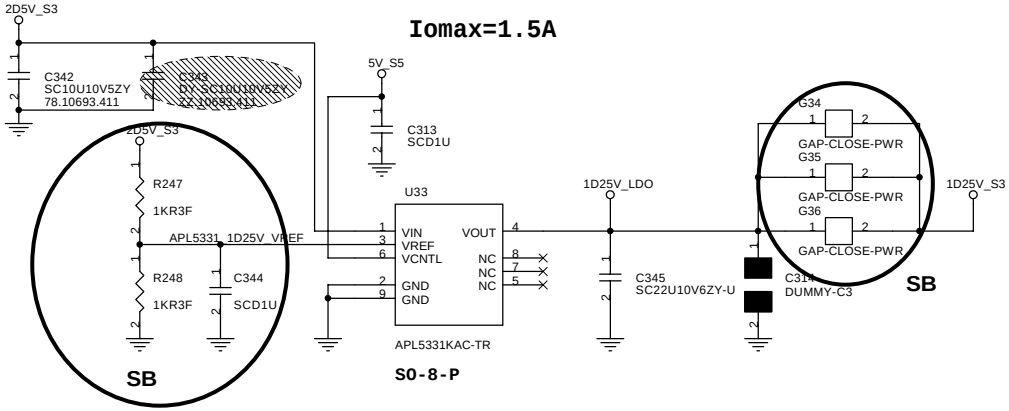


SO-8-P

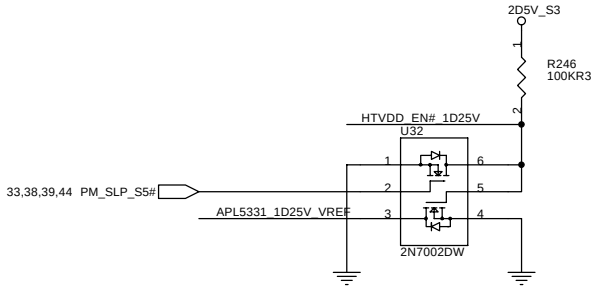


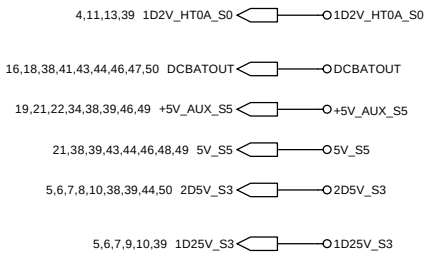
1D25V_S3

Iomax=1.5A



SO-8-P





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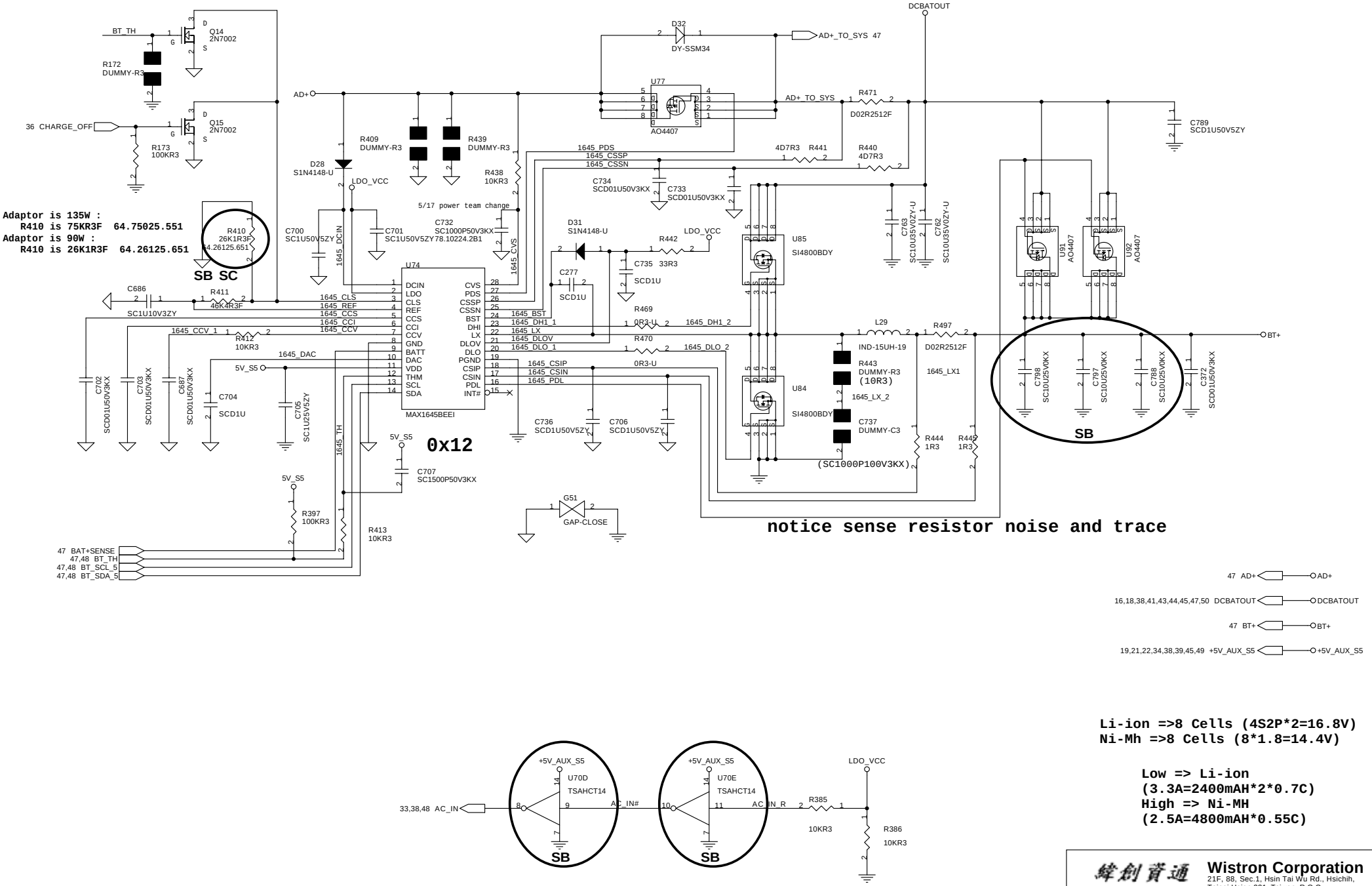
Title: ***1D25V_LDO/3V_AUX/5V_AUX***

Size: A3 | Document Number: **EGRET** | Rev: SC

Date: Friday, July 23, 2004 | Sheet 45 of 50



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Title	CHARGER MAX1645
Size: Custom	Document Number: EGRET
Rev	SC
Date: Friday, July 23, 2004	Sheet 46 of 50

Adaptor in to generate DCBATOUT

By ME requset change P/N:
From 22.10037.511
To 22.10037.971

Adaptor is 135W :
DCIN1 is 22.10037.821
Adaptor is 90W :
DCIN1 is 22.10037.971

SB SC

DCIN1
DC-JACK74-U1
22.10037.971
AD_JK
C11 SCD1U50V3ZY
C12 SCD1U50V3ZY
D24
DY-PZM24NB1
U43
AO4407
AD+_2
AD+
SC
C28 SCD1U50V5ZY
C27 SCD1U50V5ZY
ID = -10A/70deg
Rds(ON) = 24mohm
SO-8
R264 100KR3
C443 SCD1U
Q6 PDTA124EU
AD_OFF#_JK
R280 56KR3F
5V_S0
R512 1KR3
U96
AD_OFF
36 AD_OFF#
AD_OFF#_JK
R26 1KR3
2N7002DW
SB

19,21,22,34,38,39,45,46,49 +5V_AUX_S5 → +5V_AUX_S5
16,17,18,19,20,21,22,23,24,27,30,31,32,33,34,37,38,39,41,42,48,49,50 5V_S0 → 5V_S0
46 AD+ → AD+
46 BT+ → BT+

BATTERY CONNECTOR

5V_AUX_S5
D14 DY-BAV99-2 22.00089.L01
D16 DY-BAV99-2 22.00089.L01
D15 DY-BAV99-2 22.00089.L01
D39 S1N4148-U
BAT_IN#
R498 27R3F
R493 27R3F
BTSMCLK
BTSMDATA
BT_TH
BT+
33 BAT_IN#
46,48 BT_SCL_5
46,48 BT_SDA_5
46,48 BT_TH
46 BAT+SENSE
BAT1
SPD-CONN16D-7 20.D0091.208
C376 DY-SCD1U
C375 SCD1U50V3ZY
C374
C373 SC1000P50V3KX 78.10224.2B1
C799 SC1000P50V3KX 78.10224.2B1
DY-SC1000P50V3KX

3D3V_S0
R180 DY-10KR3F
DCBATOUT
U27
VCC
OUT
CIN1
GND
RS+
RS-
COUT1
RESET#
MAX4373_OUT
MAX4373_CIN1
R179 DY-4K42R3F
R178 DY-1KR3F
C278 DY-SCD1U50V3ZY
DY-MAX4373FEUA
AD+_TO_SYS 46
DCBATOUT 16,18,38,41,43,44,45,46,50
AD_CURR_DET 33
RST#_AD_LIM 33

Check Setting Value(6.5A)

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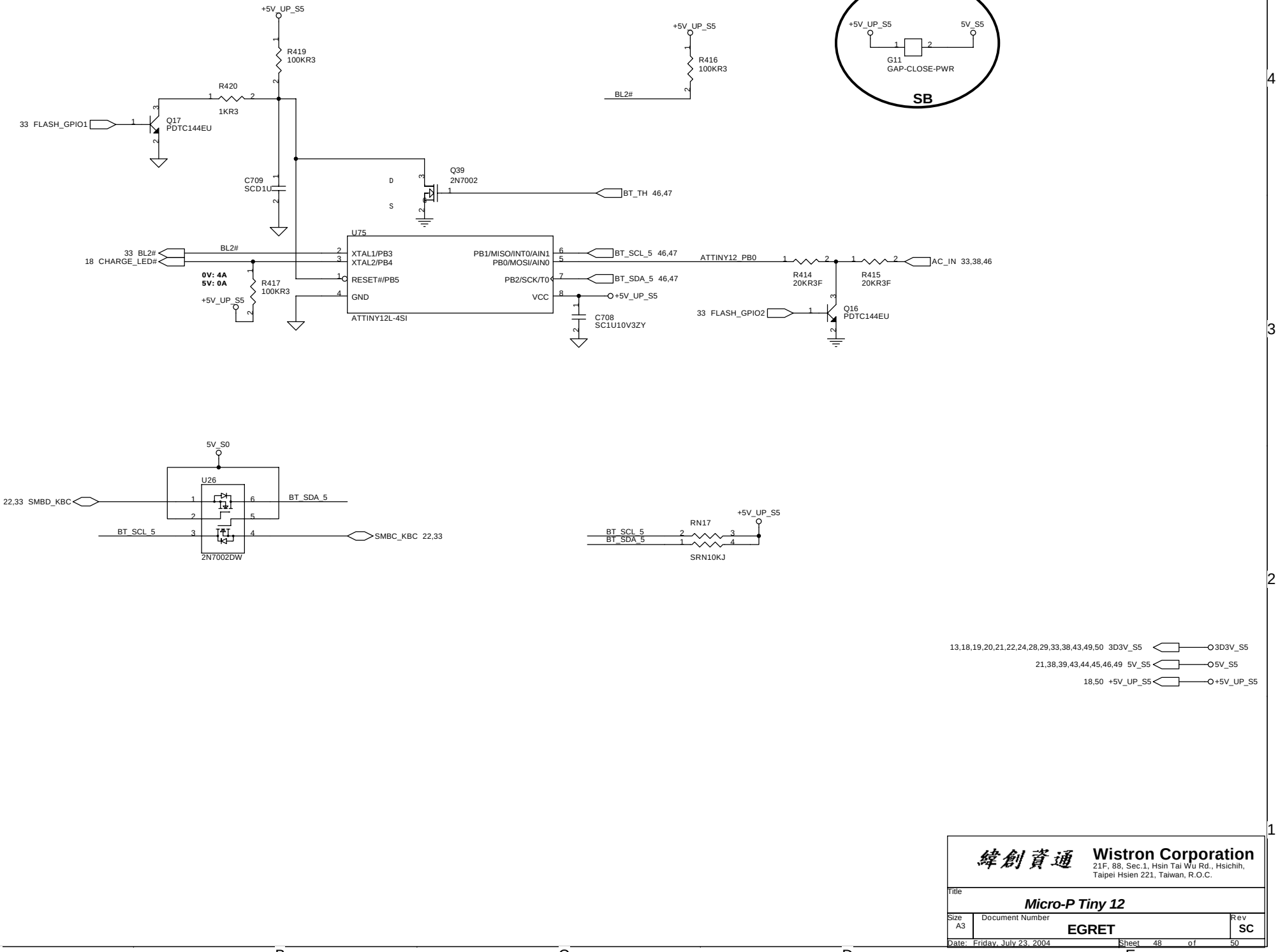
Title: ***DC/DC (1/2) -- 5V / 3.3V / 2.5V***
Size: A3 | Document Number: EGRET | Rev: SC
Date: Friday, July 23, 2004 | Sheet 47 of 50



Wistron Corporation	緯創資通
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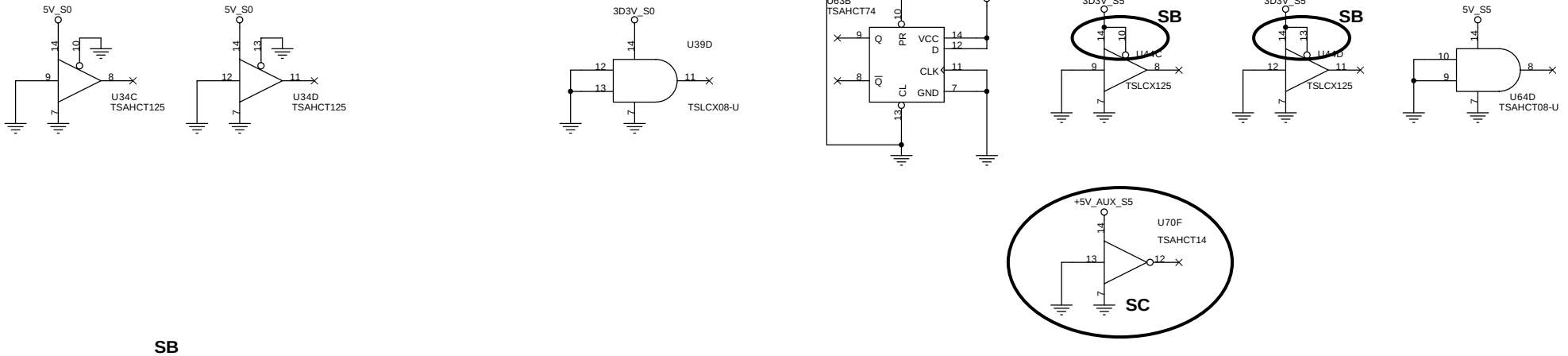
Title: *Micro-P Tiny 12*	
Size: A3	Document Number: EGRET
Rev: SC	
Date: Friday, July 23, 2004	Sheet 48 of 50

NO USE LOGIC



SB
SC

HOLE28 HOLEMDC
HOLE29 HOLEMDC
HOLE19 HOLE2
HOLE3 HOLELCD
HOLE13 HOLEVGA
HOLE7 HOLEVGA
HOLE17 HOLEVGA2
HOLE26 HOLEFAN
HOLE20 HOLEFAN

HOLE2 HOLE
HOLE9 HOLE
HOLE5 HOLE
HOLE6 HOLE
HOLE14 HOLE
HOLE15 HOLE
HOLE12 HOLE
HOLE16 HOLE
HOLE18 HOLE
HOLE21 HOLE

HOLE22 HOLE
HOLE23 HOLE
HOLE24 HOLE
HOLE25 HOLE
HOLE1 HOLE
HOLE4 HOLE
HOLE30 HOLE
HOLE31 HOLE
HOLE11 HOLE
HOLE8 HOLE3
HOLE27 HOLE

SB
GND29 GNDPADS177X118 ZZ.39S07.001
GND30 SPRING-1 ZZ.40V16.001
Stuff For UMA Only

SC
GND31 GNDPADS177X118 34.39S07.001
AUD_AGND

SC
GND32 GNDPAD ZZ.NDPAD.XXX

SB
GND28 GNDPADS157X118 ZZ.41P23.001
GND27 GNDPADS157X118 ZZ.41P23.001
Stuff For UMA Only

SC
GND2 GNDPAD-S4
GND11 GNDPADS126X87 34.45T31.001
GND13 SPRING-1 34.40V16.001
GND14 GNDPADS126X87 34.45T31.001
GND19 GNDPAD-S2
GND23 GNDPADS177X118 34.39S07.001
GND26 SPRING-3 34.49V19.001

SB
GND1 SPRING-1 ZZ.40V16.001
GND4 SPRING-1 ZZ.40V16.001
GND6 GNDPAD
GND10 GNDPAD
GND17 GNDPAD
GND18 GNDPADS236X354
GND20 GNDPAD
GND21 GNDPAD
Stuff For UMA Only

GND15 GNDPAD
GND22 GNDPAD
GND7 GNDPAD
SC
GND16 GNDPADS177X118 ZZ.39S07.001
Stuff For UMA Only

GND3 GNDPAD
GND8 GNDPAD
GND5 GNDPAD
GND9 GNDPAD
GND12 GNDPAD
GND25 GNDPAD
SC
GND24 GNDPADS157X118 ZZ.41P23.001
Stuff For UMA Only

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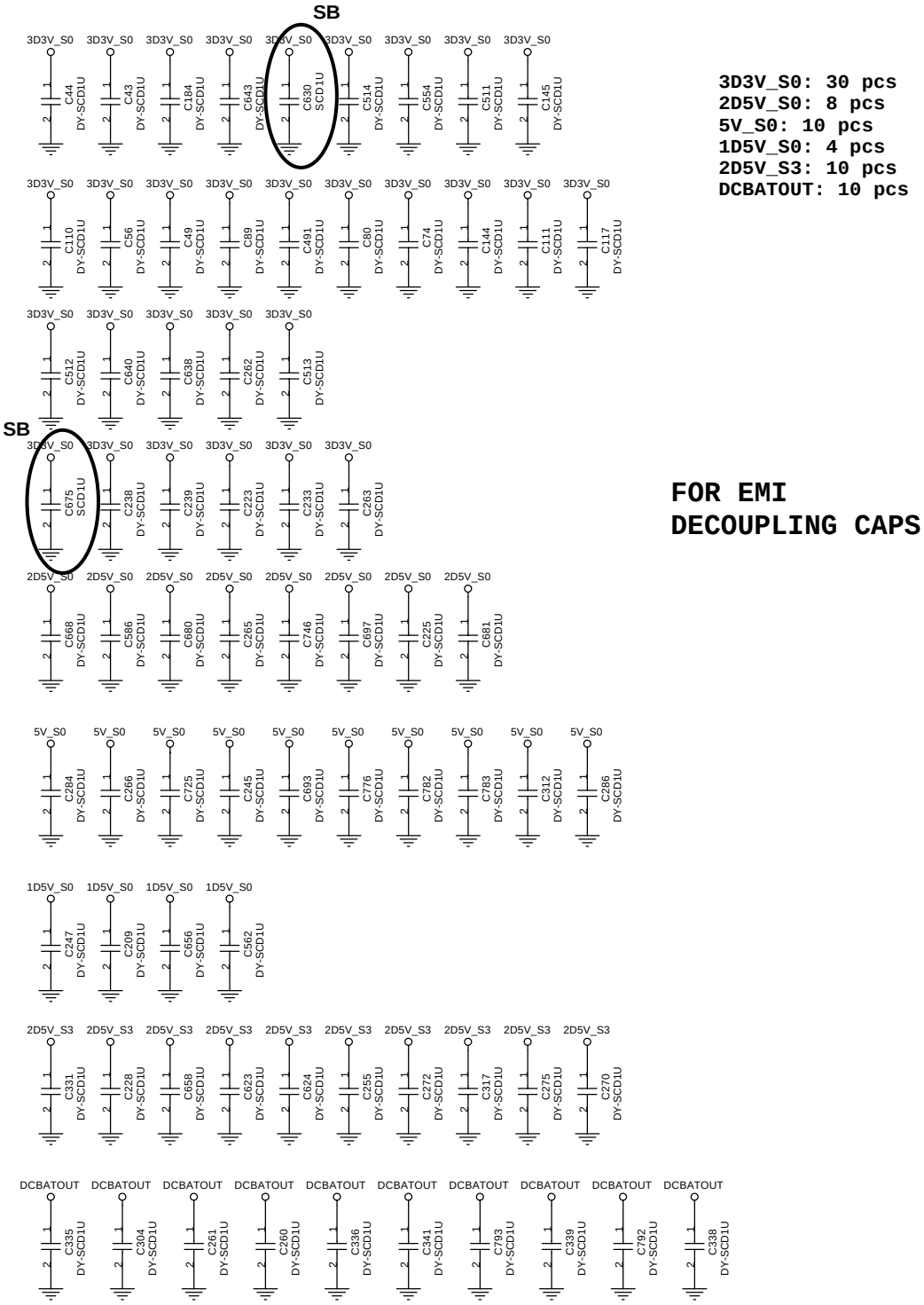
Taipei Hsien 221, Taiwan, R.O.C.

Title: MISC

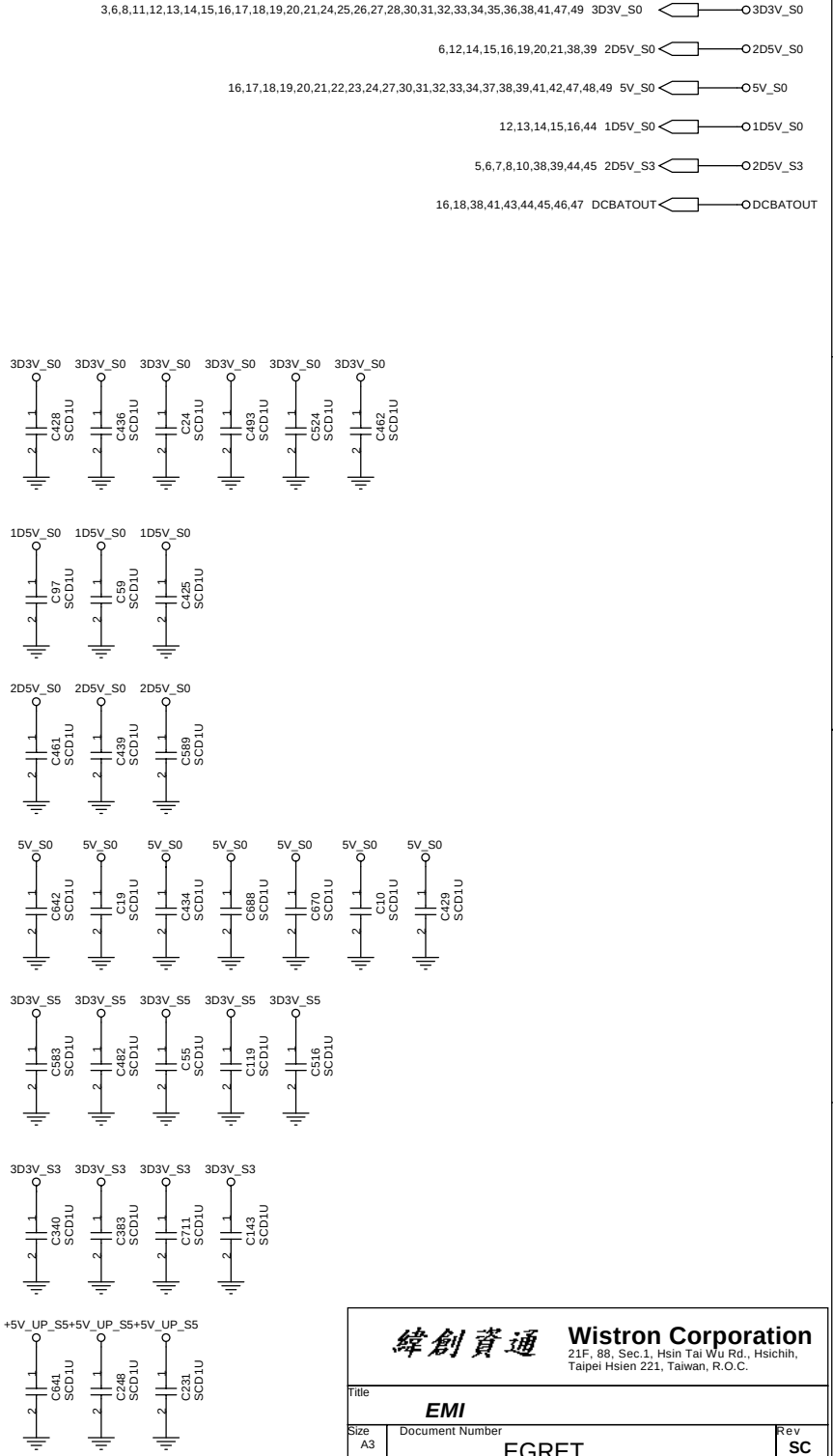
Size: A3 | Document Number: EGRET | Rev: SC

Date: Friday, July 23, 2004 | Sheet 49 of 50



3D3V_S0: 30 pcs
2D5V_S0: 8 pcs
5V_S0: 10 pcs
1D5V_S0: 4 pcs
2D5V_S3: 10 pcs
DCBATOUT: 10 pcs

FOR EMI
DECOUPLING CAPS



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Title: ***EMI***

Size	Document Number	Rev
A3	EGRET	SC

Date: Friday, July 23, 2004 Sheet 50 of 50