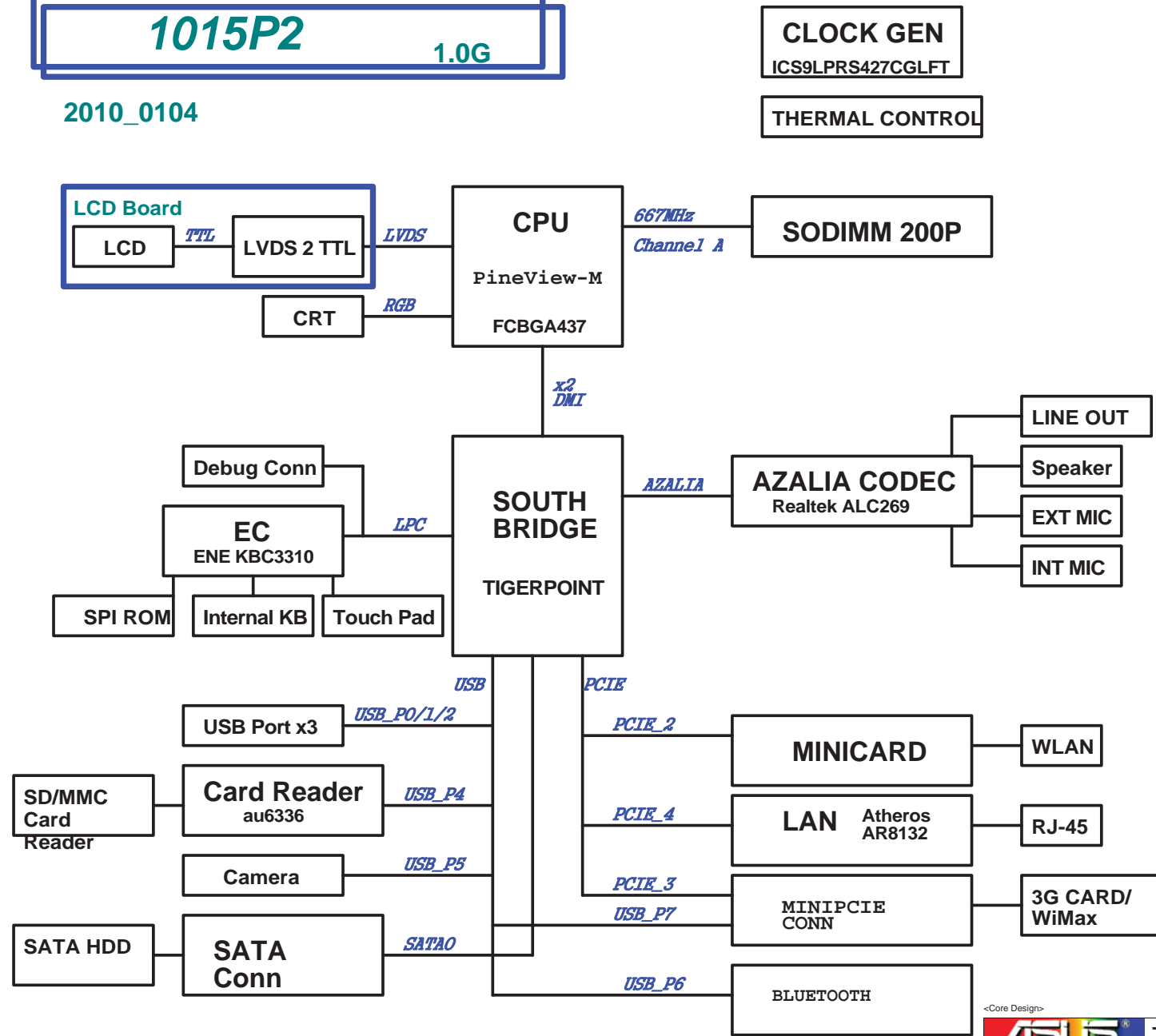


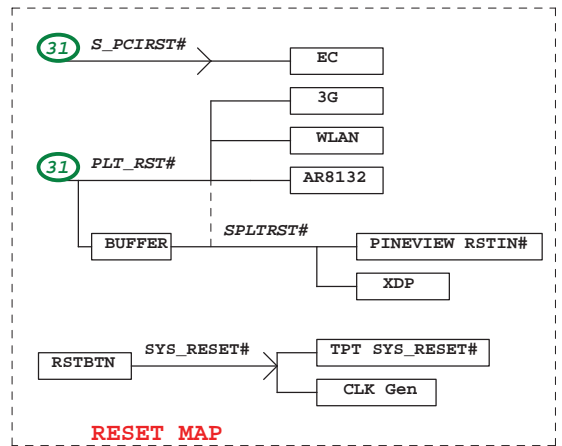
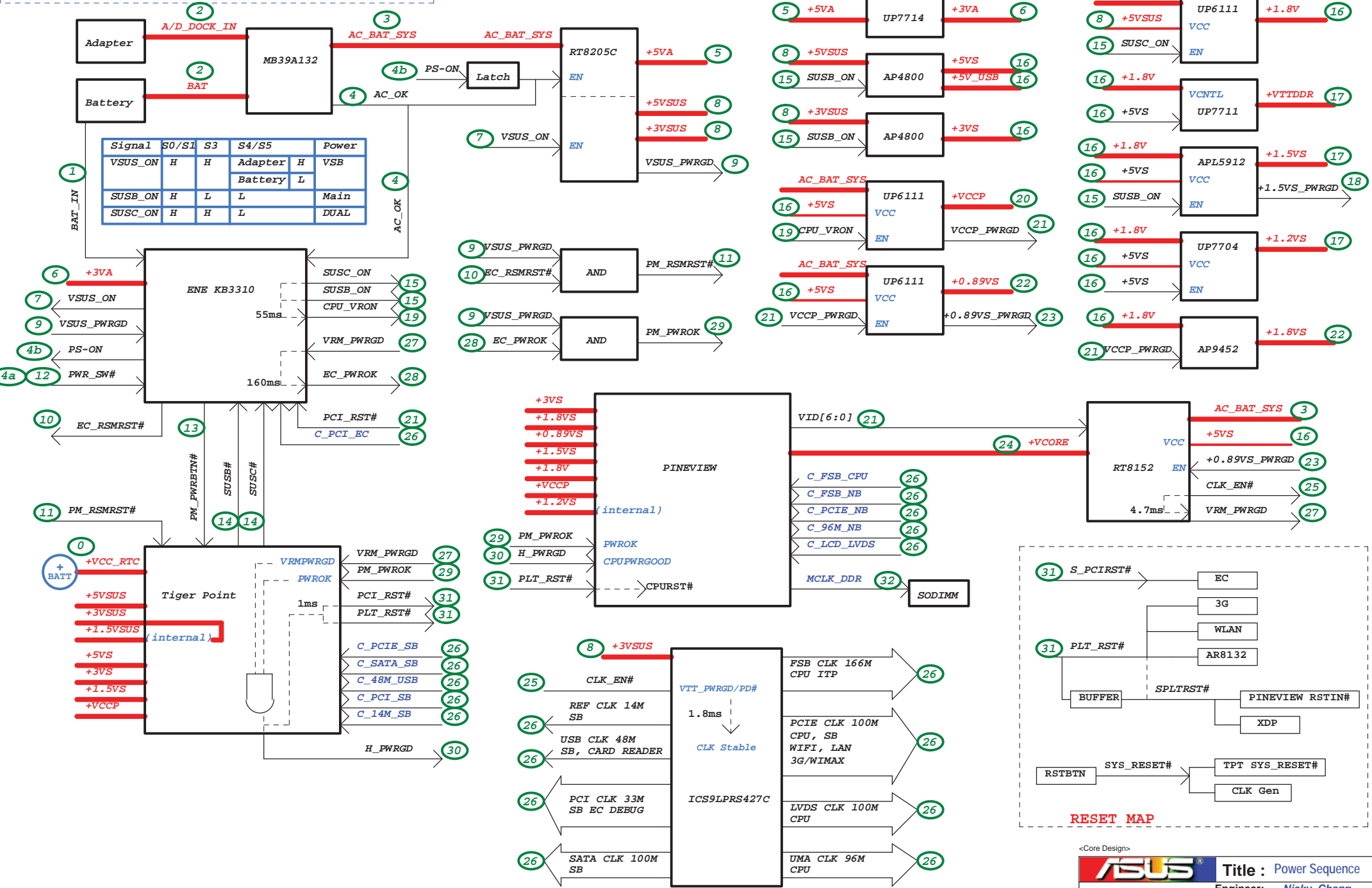
- 01\_Block Diagram
- 02\_Power Sequence
- 03\_Clock Gen\_ICS9LPRS427C
- 04.PineView-M\_1 (LVDS\_DMI\_CPU)
- 05.PineView-M\_2 (DDR2\_XDP\_CRT)
- 06.PineView-M\_3 (PWR&GND)
- 07.XDP
- 08.Tigerpoint\_DMI\_USB
- 09.Tigerpoint\_SYS
- 10.Tigerpoint\_PWR
- 11.DDR2 SODIMM
- 12.DDR2-Termination
- 13.Onboard VGA
- 14.LCD Conn\_LID
- 15.WIFI&SMART33SW
- 16.LAN\_AR8132
- 17.WLAN
- 18.USIN&3G\_CON
- 19.Bluetooth
- 20.HDD\_CON
- 21.
- 22.
- 23.USB Port1
- 24.EC\_ENE KB3310
- 25.KB\_TP
- 26.Fan\_debug
- 27.SPI\_ROM
- 28.DUA\_CON
- 29.PWR Jack
- 30\_Discharge
- 31.
- 32.Srew Hole&EMI
- 33.Power Flow
- 34.Power\_Charger
- 35.Vcore
- 36.Power\_+1.8V&VTTDDR&+1.8VS
- 37.Power\_VCCP
- 38.Power\_+0.89VS
- 39.Power\_+1.5VS
- 40.Power Latch
- 41.Power System
- 42.power switch

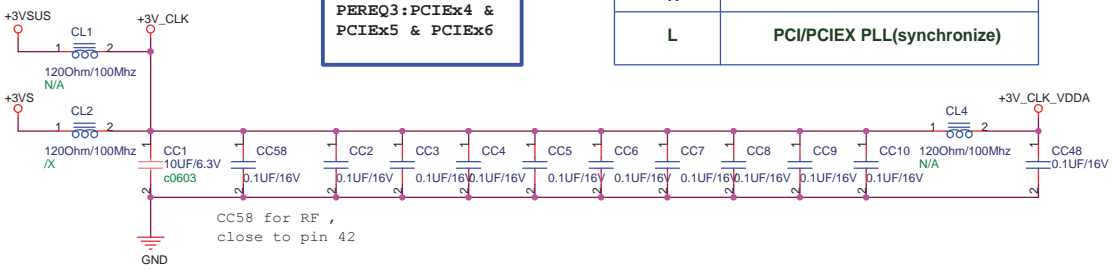
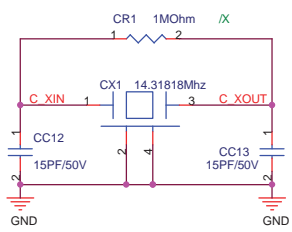
# 1015P2 1.0G

2010\_0104



For Adapter Mode: (1) -> (2) -> (3) -> (4) -> (5) -> ...  
 For Battery Mode: (1) -> (2) -> (3) -> (4) -> (4a) -> (4b) -> (5) -> ...



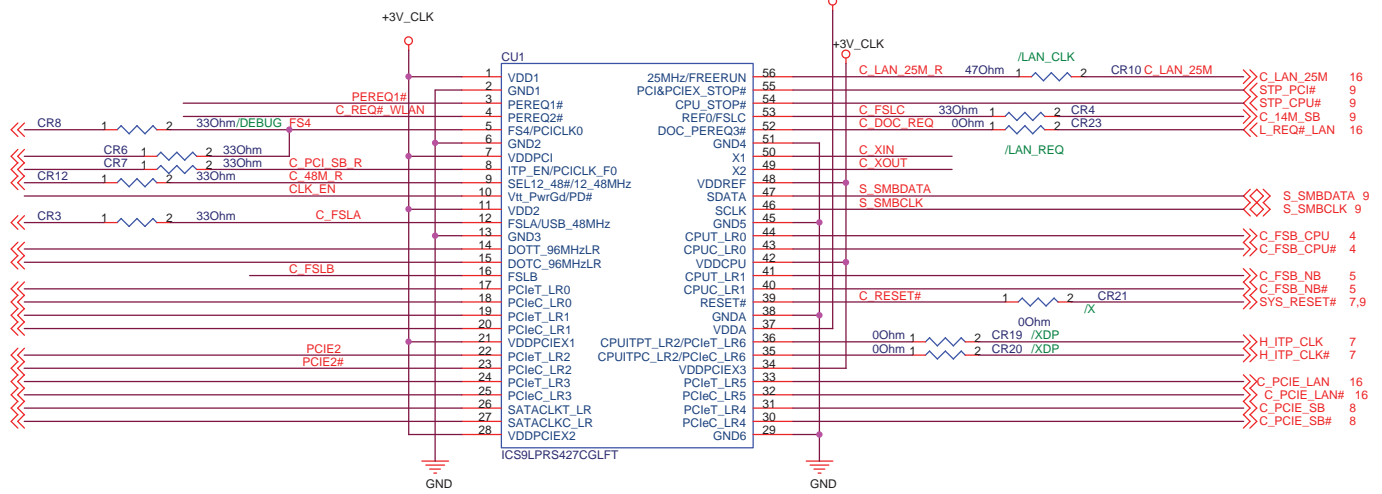


1:Disable  
0:Enable

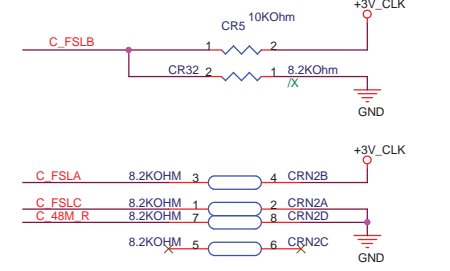
PEREQ1:PCIEx0 &  
PCIEx1  
PEREQ2:PCIEx2 &  
PCIEx3 & SATA  
PEREQ3:PCIEx4 &  
PCIEx5 & PCIEx6

FS4	Function
H	FIXED PLL (Asynchronous)
L	PCI/PCIEX PLL(synchronize)

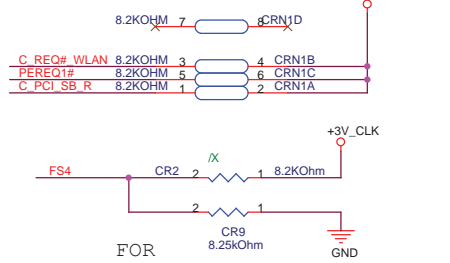
- 26 C\_PCI\_DEBUG
- 24 C\_LPC\_EC
- 8 C\_PCI\_SB
- 28 C\_48M\_CARD\_READER
- 8 C\_48M\_USB
- 5 C\_96M\_NB
- 5 C\_96M\_NB#
- 5 C\_LCD\_LVDS
- 5 C\_LCD\_LVDS#
- 4 C\_PCIE\_NB
- 4 C\_PCIE\_NB#
- 18 C\_PCIE\_WIMAX
- 18 C\_PCIE\_WIMAX#
- 17 C\_PCIE\_WLAN
- 17 C\_PCIE\_WLAN#
- 9 C\_SATA\_SB
- 9 C\_SATA\_SB#



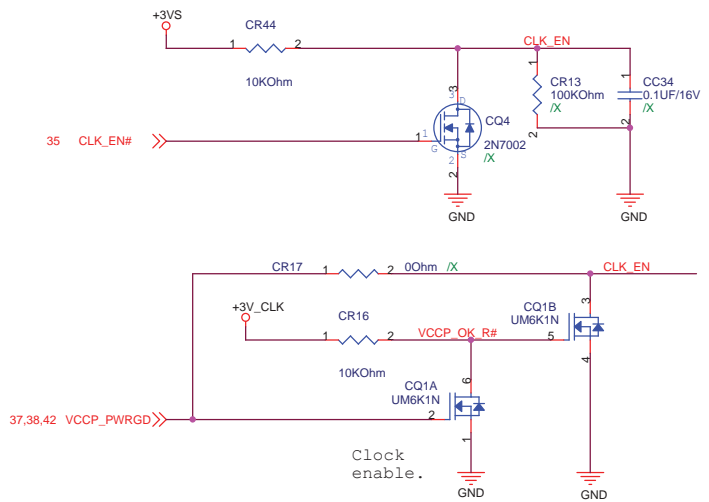
C_SATA_SB	CC50	2	1	10PF/50V
C_SATA_SB#	CC51	2	1	10PF/50V
PCIE2	CC52	2	1	10PF/50V
PCIE2#	CC53	2	1	10PF/50V
C_LCD_LVDS	CC54	2	1	10PF/50V
C_LCD_LVDS#	CC55	2	1	10PF/50V
STP_PCI#	EC7	2	1	10PF/50V
STP_CPU#	EC10	2	1	10PF/50V
C_PCI_SB_R	CC36	2	1	10PF/50V
FS4	CC37	2	1	10PF/50V
S_SMBDATA	EC14	2	1	10PF/50V
S_SMBCLK	EC15	2	1	10PF/50V
C_DOC_REQ	EC16	2	1	10PF/50V
C_FSLC	CC39	2	1	10PF/50V
C_FSLA	CC40	2	1	10PF/50V
C_48M_R	CC35	2	1	47PF/50V
C_LAN_25M_R	CC11	2	1	10PF/50V
C_PCIE_LAN	EC17	2	1	10PF/50V
C_PCIE_LAN#	EC18	2	1	10PF/50V
C_PCI_DEBUG	EC19	2	1	10PF/50V
C_LPC_EC	EC20	2	1	10PF/50V
C_14M_SB	EC21	2	1	10PF/50V



FSLC	FSLB	FSLA	CPU(MHZ)
0	1	1	166
0	0	1	133



O_DOC1	O_DOC2	Voltage	Status
L	L	2.4-3.3V	Super
L	H	0.5-2.36V	Normal
H	*	0-0.35V	Power saving



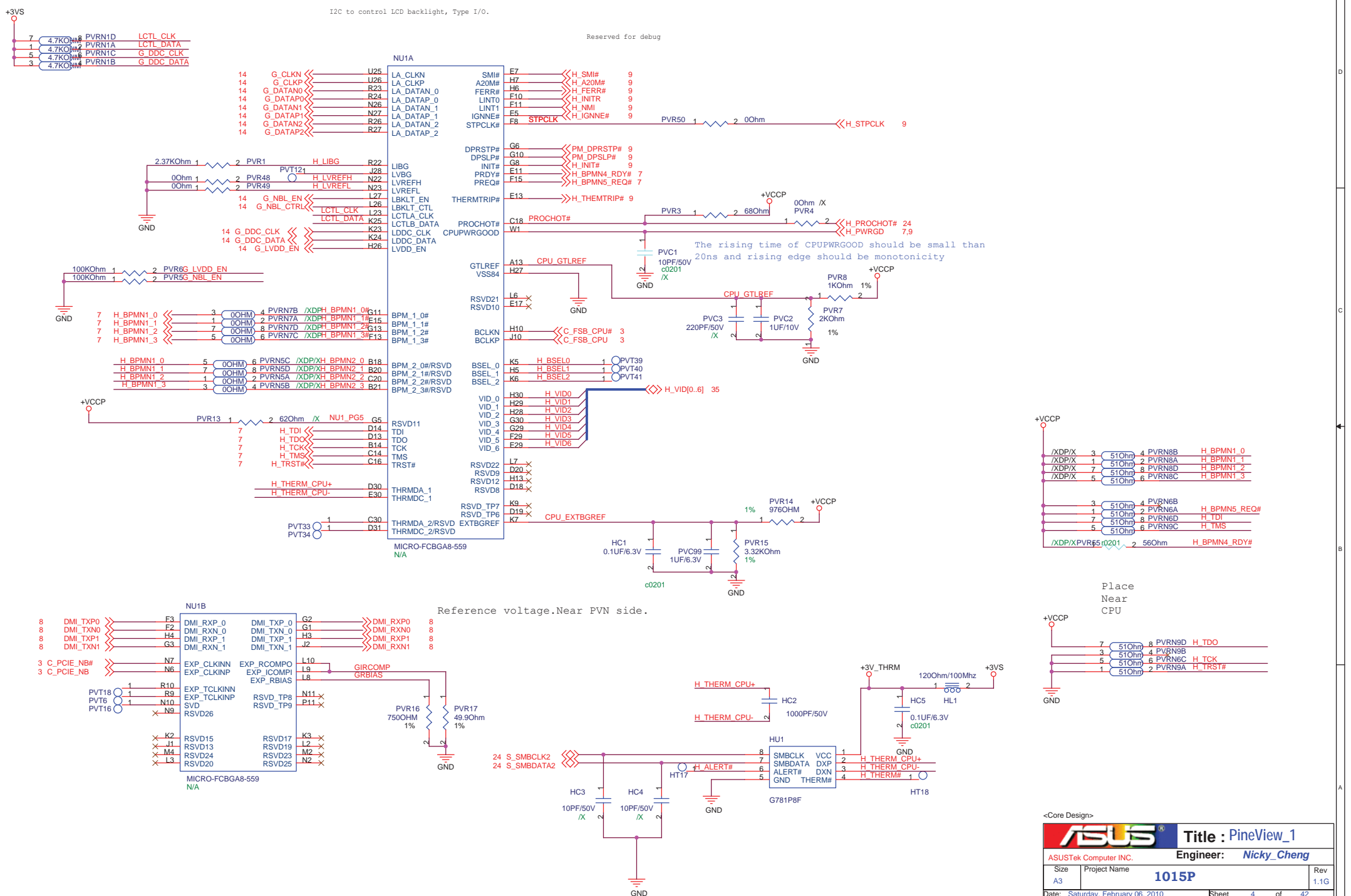
<Core Design>

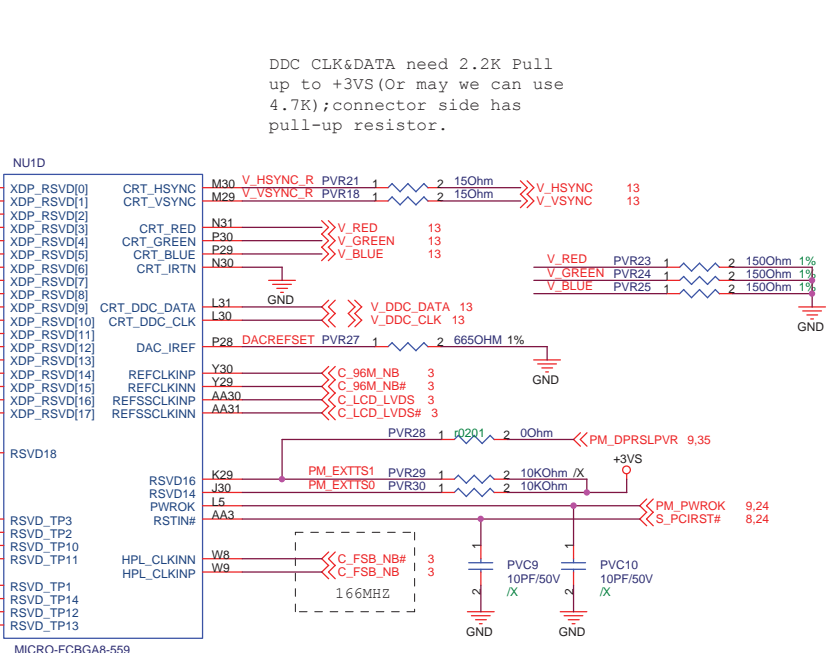
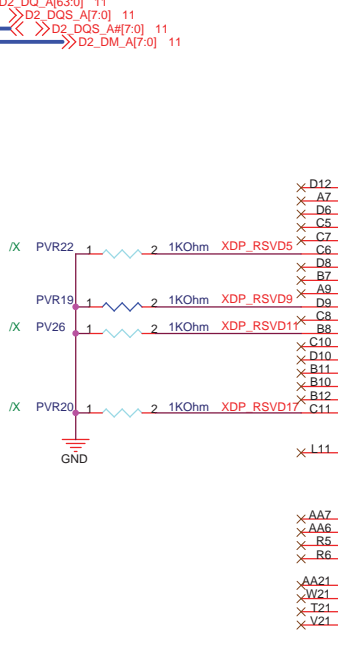
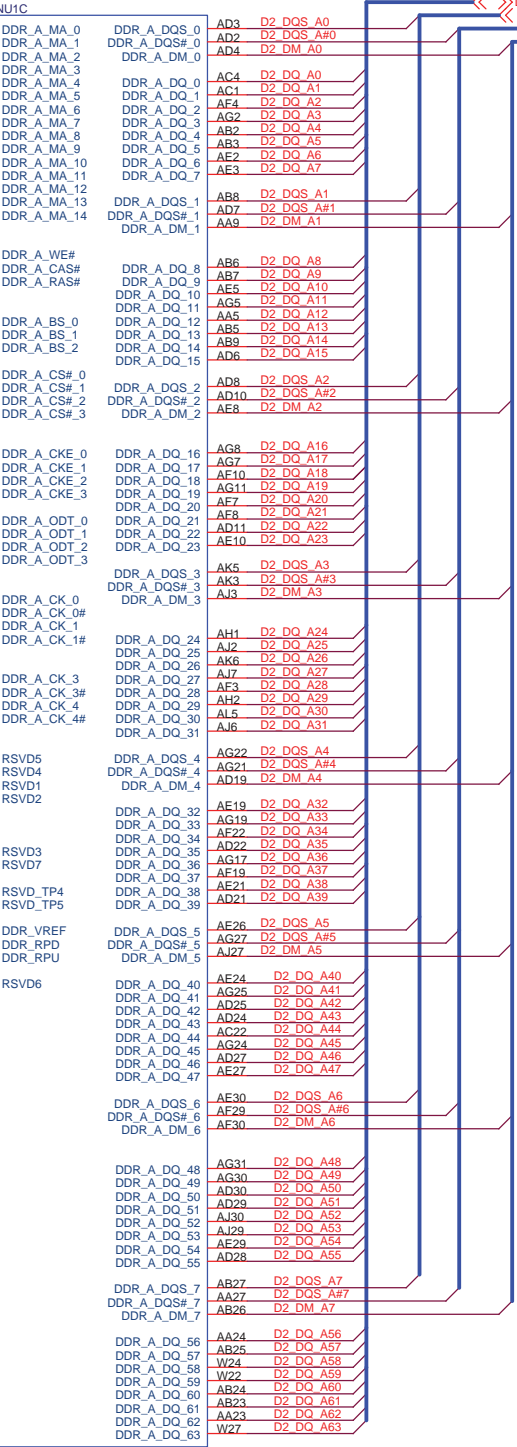
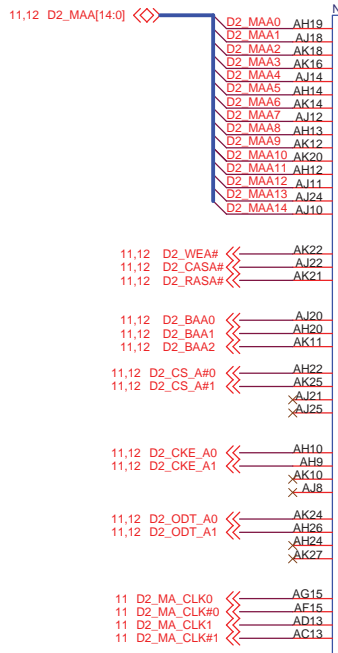
**ASUS** Title: ICS9LPRS427C

ASUSTek Computer INC. Engineer: Nicky\_Cheng

Size	Project Name	Rev
A3	1015P	1.1G

Date: Saturday, February 06, 2010 Sheet 3 of 42

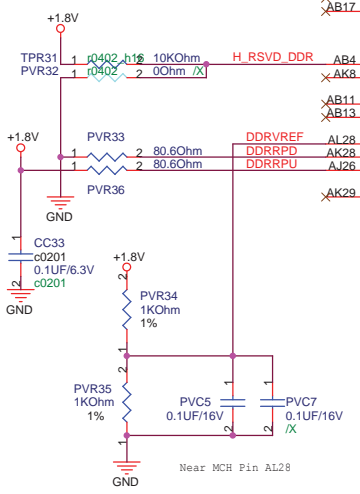




DDC CLK&DATA need 2.2K Pull up to +3VS(Or may we can use 4.7K);connector side has pull-up resistor.

CPU Sample SKU	ASUS P/N
ES1	01G013070000
ES2	01G0132000000
QS	01G0132000001
PRQ	01G0132000002

Intel confirm only RSVD9 need stuff 1K resistor.



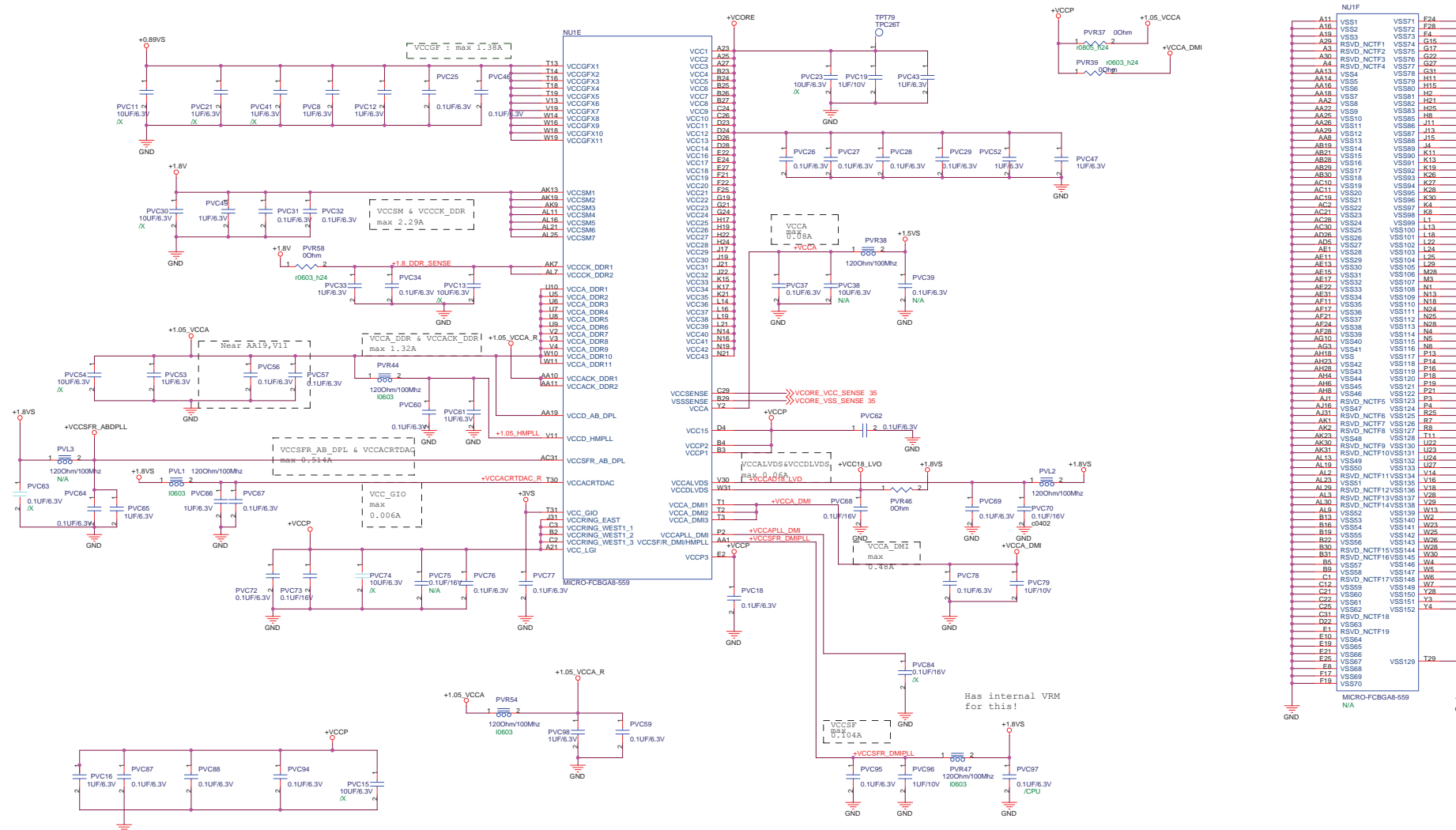
<Core Design>

**ASUS** Title : PineView\_2

ASUSTek Computer INC. Engineer: Nicky Cheng

Size	Project Name	Rev
A3	1015P	1.0G

Date: Saturday, February 06, 2010 Sheet 5 of 42

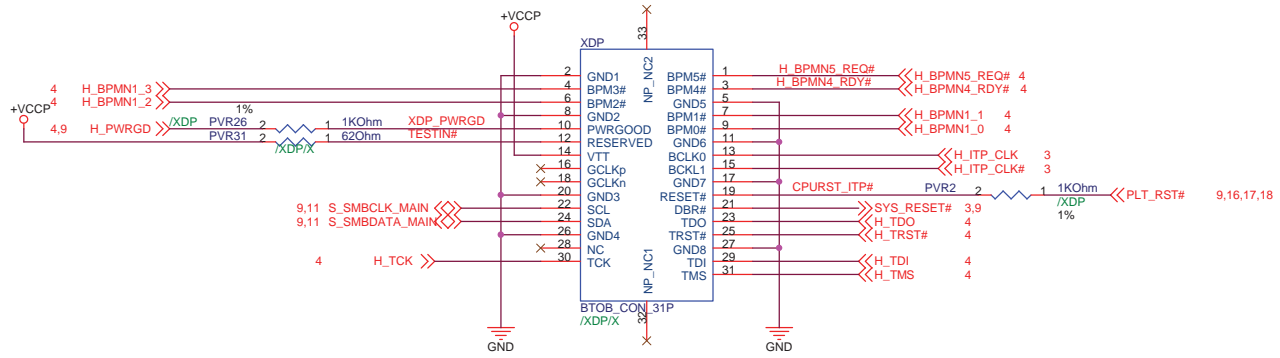


VCC = 3.5A  
 VCCA = 0.08A  
 VCCGFX = 1.38A  
 VCCALVDS , VCCDLVDS = 0.06A  
 VCCA\_DMI = 0.48A  
 VCCSFR\_DMIHPLL = 0.104A  
 VCCA\_DDR and VCCACK\_DDR = 1.32A  
 VCCSM and VCCCK\_DDR = 2.27A  
 VCCRING\_EAST , VCCRING\_EAST\_WEST , VCC\_LGI , VCCD\_AB\_DPL , VCCD\_HMPLL = 0.33A  
 VCC\_GIO = 0.006A  
 VCCSFR\_AB\_DPL , VCCACRTDAC = 0.154A

Current for PineView

Has internal VRM for this!

NU1F		
A11	VSS1	VSS71
A16	VSS2	VSS72
A19	VSS3	VSS73
A28	RSVD_NCTF1	VSS74
A31	RSVD_NCTF2	VSS75
A30	RSVD_NCTF3	VSS76
A4	RSVD_NCTF4	VSS77
AA13	RSVD_NCTF5	VSS78
AA16	VSS5	VSS79
AA25	VSS6	VSS80
AA8	VSS7	VSS81
AA2	VSS8	VSS82
AA25	VSS9	VSS83
AA25	VSS10	VSS84
AA25	VSS11	VSS85
AA29	VSS12	VSS87
AA8	VSS13	VSS88
AB19	VSS14	VSS89
AB21	VSS15	VSS90
AB28	VSS16	VSS91
AB29	VSS17	VSS92
AB30	VSS18	VSS93
AC10	VSS19	VSS94
AC19	VSS20	VSS95
AC2	VSS21	VSS96
AC2	VSS22	VSS97
AC41	VSS23	VSS98
AC28	VSS24	VSS99
AD26	VSS25	VSS100
AD5	VSS26	VSS101
AE1	VSS27	VSS102
AE1	VSS28	VSS103
AE11	VSS29	VSS104
AE15	VSS30	VSS105
AE15	VSS31	VSS106
AE17	VSS32	VSS107
AE22	VSS33	VSS108
AE31	VSS34	VSS109
AE17	VSS35	VSS110
AF21	VSS36	VSS111
AF21	VSS37	VSS112
AF24	VSS38	VSS113
AF28	VSS39	VSS114
AG10	VSS40	VSS115
AG3	VSS41	VSS116
AH23	VSS	VSS117
AH23	VSS42	VSS118
AH28	VSS43	VSS119
AH4	VSS44	VSS120
AH6	VSS45	VSS121
AH6	VSS46	VSS122
A11	RSVD_NCTF5	VSS123
A16	RSVD_NCTF6	VSS124
A31	RSVD_NCTF7	VSS125
AK1	RSVD_NCTF8	VSS126
AK2	RSVD_NCTF9	VSS127
AK23	VSS48	VSS128
AK30	RSVD_NCTF9	VSS130
AK31	RSVD_NCTF10	VSS131
AL13	VSS49	VSS132
AL19	VSS50	VSS133
AL2	RSVD_NCTF11	VSS134
AL24	VSS51	VSS135
AL28	RSVD_NCTF12	VSS136
AL3	RSVD_NCTF13	VSS137
AL9	RSVD_NCTF14	VSS138
B13	VSS52	VSS139
B16	VSS53	VSS140
B16	VSS54	VSS141
B19	VSS55	VSS142
B22	VSS56	VSS143
B30	RSVD_NCTF15	VSS144
B5	RSVD_NCTF16	VSS145
B5	VSS57	VSS146
B9	VSS58	VSS147
C11	RSVD_NCTF17	VSS148
C12	VSS59	VSS149
C21	VSS60	VSS150
C22	VSS61	VSS151
C25	VSS62	VSS152
C31	RSVD_NCTF18	VSS153
D22	VSS63	VSS154
E1	RSVD_NCTF19	VSS155
E10	VSS64	VSS156
E19	VSS65	VSS157
E41	VSS66	VSS158
E25	VSS67	VSS159
F8	VSS68	VSS160
F17	VSS69	VSS161
F19	VSS70	VSS162
F24	VSS71	VSS163
F28	VSS72	VSS164
F4	VSS73	VSS165
F15	VSS74	VSS166
G27	VSS75	VSS167
G31	VSS76	VSS168
H11	VSS77	VSS169
H2	VSS78	VSS170
H21	VSS79	VSS171
H25	VSS80	VSS172
H5	VSS81	VSS173
H13	VSS82	VSS174
J4	VSS83	VSS175
K11	VSS84	VSS176
K13	VSS85	VSS177
K28	VSS86	VSS178
K22	VSS87	VSS179
K4	VSS88	VSS180
K6	VSS89	VSS181
L13	VSS90	VSS182
L13	VSS91	VSS183
L18	VSS92	VSS184
L22	VSS93	VSS185
L25	VSS94	VSS186
L25	VSS95	VSS187
L29	VSS96	VSS188
M3	VSS97	VSS189
M1	VSS98	VSS190
N13	VSS99	VSS191
N24	VSS100	VSS192
N26	VSS101	VSS193
N26	VSS102	VSS194
N5	VSS103	VSS195
N4	VSS104	VSS196
N18	VSS105	VSS197
N18	VSS106	VSS198
N18	VSS107	VSS199
N18	VSS108	VSS200
N18	VSS109	VSS201
N18	VSS110	VSS202
N18	VSS111	VSS203
N18	VSS112	VSS204
N18	VSS113	VSS205
N18	VSS114	VSS206
N18	VSS115	VSS207
N18	VSS116	VSS208
N18	VSS117	VSS209
N18	VSS118	VSS210
N18	VSS119	VSS211
N18	VSS120	VSS212
N18	VSS121	VSS213
N18	VSS122	VSS214
N18	VSS123	VSS215
N18	VSS124	VSS216
N18	VSS125	VSS217
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N18	VSS127	VSS219
N18	VSS128	VSS220
N18	VSS129	VSS221
N18	VSS130	VSS222
N18	VSS131	VSS223
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N18	VSS141	VSS233
N18	VSS142	VSS234
N18	VSS143	VSS235
N18	VSS144	VSS236
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N18	VSS156	VSS248
N18	VSS157	VSS249
N18	VSS158	VSS250
N18	VSS159	VSS251
N18	VSS160	VSS252
N18	VSS161	VSS253
N18	VSS162	VSS254
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N18	VSS170	VSS262
N18	VSS171	VSS263
N18	VSS172	VSS264
N18	VSS173	VSS265
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N18	VSS184	VSS276
N18	VSS185	VSS277
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N18	VSS187	VSS279
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N18	VSS189	VSS281
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N18	VSS192	VSS284
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N18	VSS195	VSS287
N18	VSS196	VSS288
N18	VSS197	VSS289
N18	VSS198	VSS290
N18	VSS199	VSS291
N18	VSS200	VSS292
N18	VSS201	VSS293
N18	VSS202	VSS294
N18	VSS203	VSS295
N18	VSS204	VSS296
N18	VSS205	VSS297
N18	VSS206	VSS298
N18	VSS207	VSS299
N18	VSS208	VSS300



Change Device and PCB footprint of XDP1 to nomask footprint - nomask solution

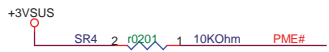
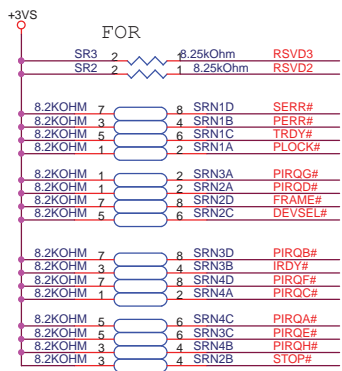
權 Layout 缺賀叫 XDP Connector 叫確 12G161300311 (w/ 2 through holes)



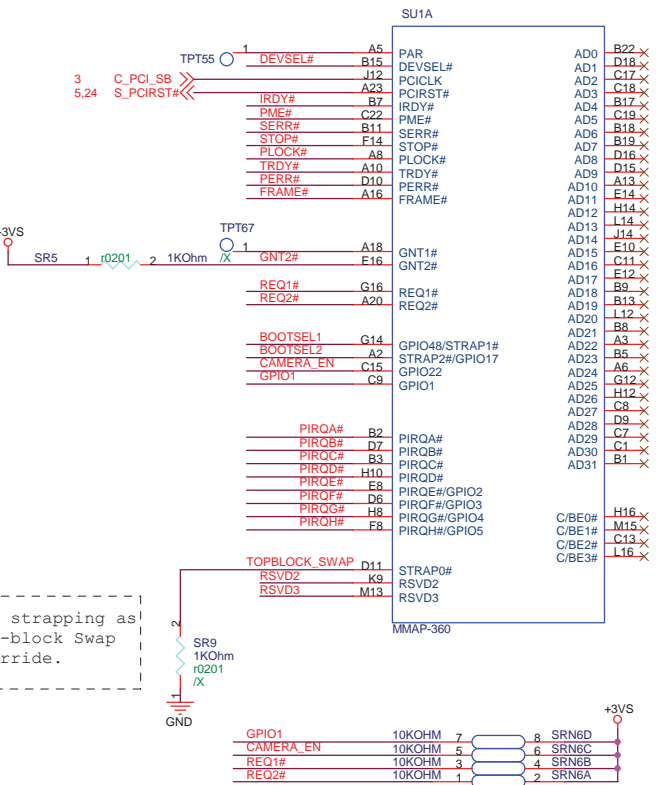
<Core Design>

<b>ASUS</b>		<b>Title : XDP</b>	
ASUSTek Computer INC.		Engineer: <i>Nicky_Cheng</i>	
Size A3	Project Name <b>1015P</b>	Rev 1.1G	
Date: Saturday, February 06, 2010		Sheet 7 of 42	

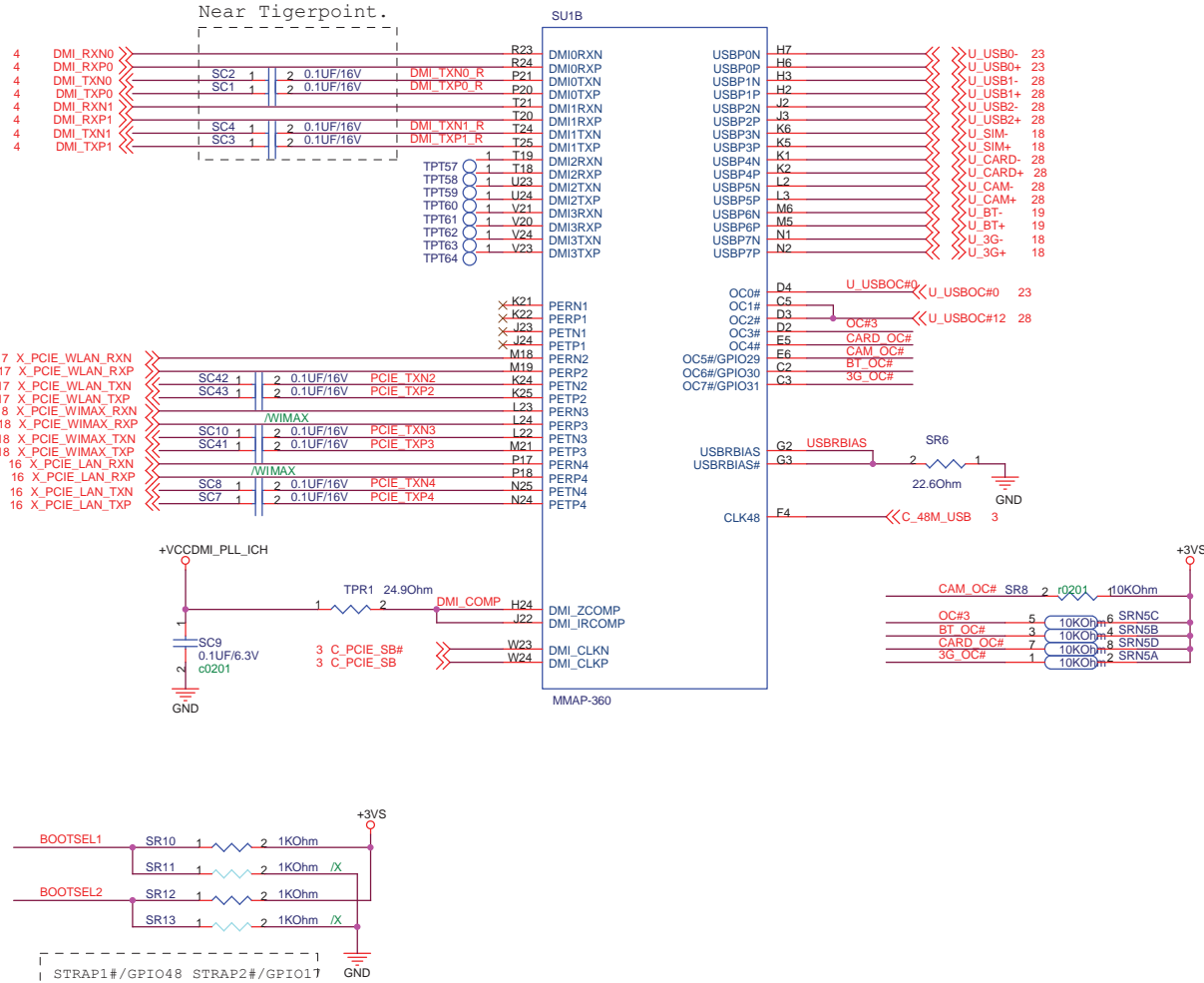




Remain  
PCICLK



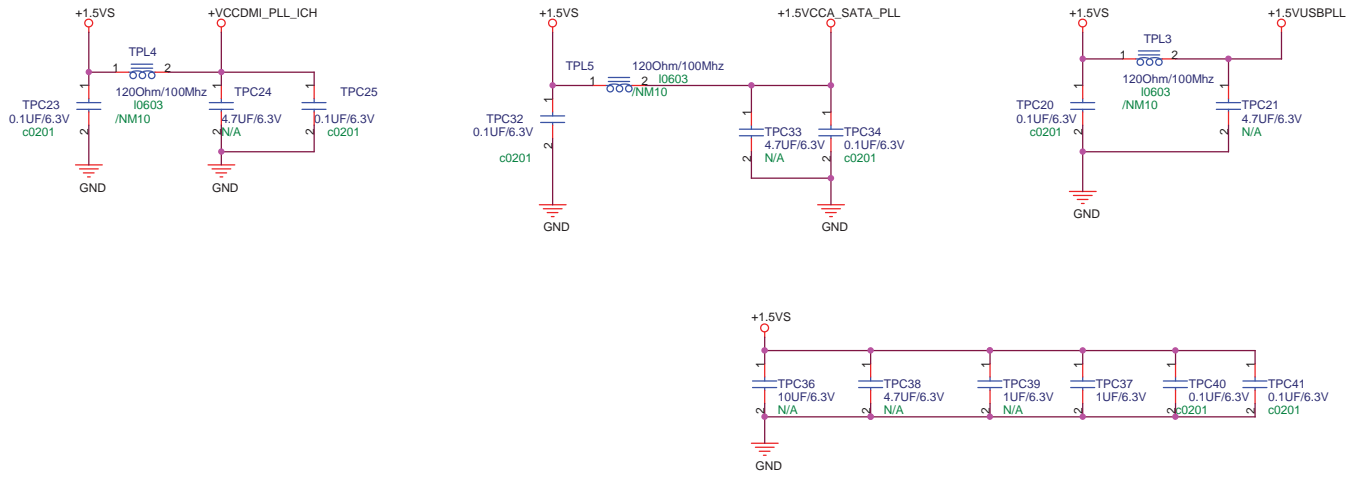
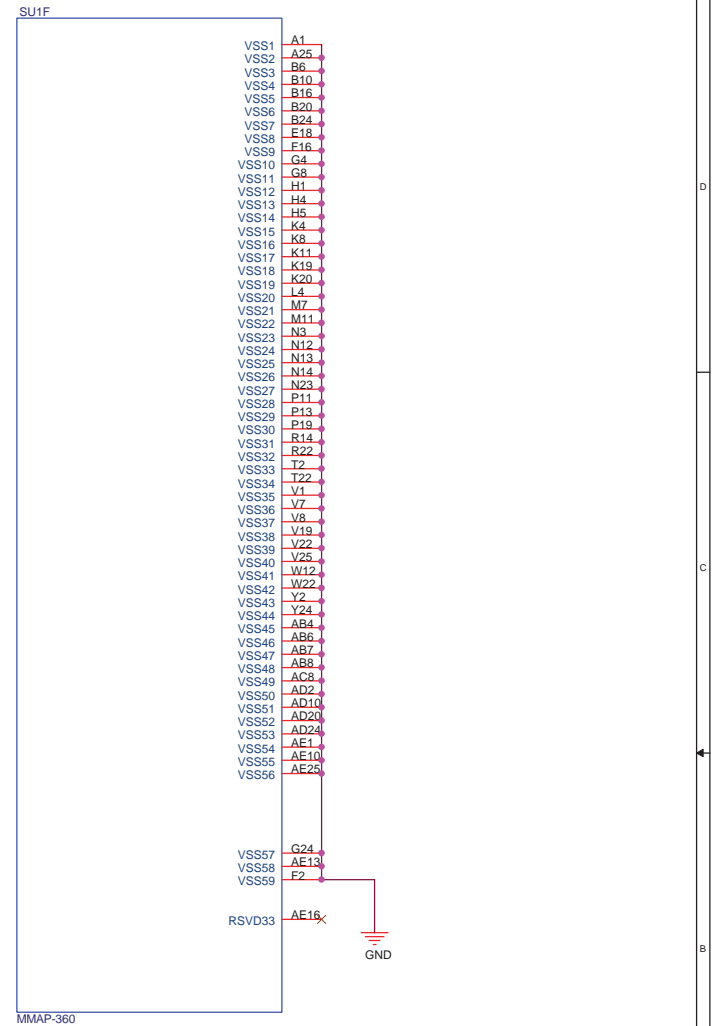
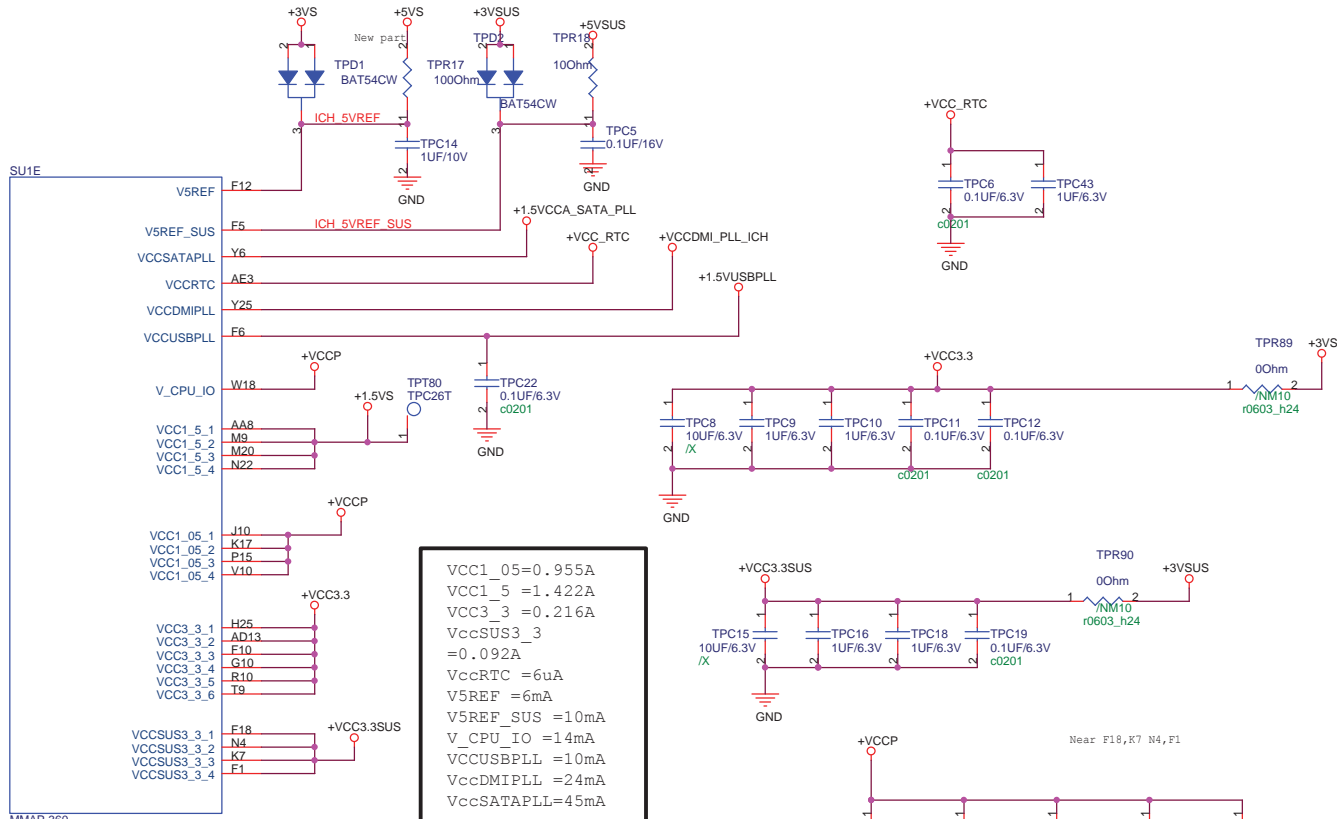
For strapping as  
Top-block Swap  
override.



USB0	USB CONN
USB1	USB CONN
USB2	USB CONN
USB3	USIM
USB4	Card Reader
USB5	Camera
USB6	Blue tooth
USB7	3G





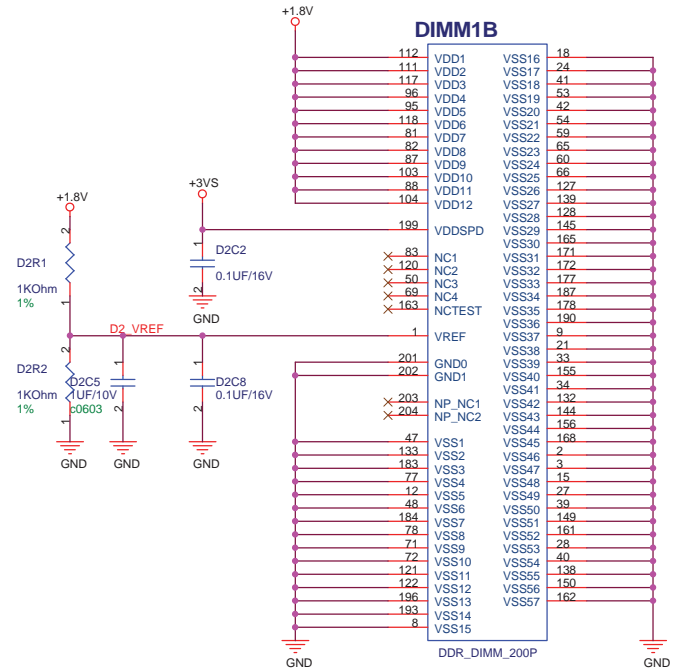
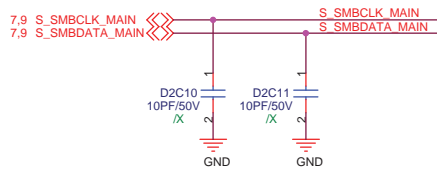
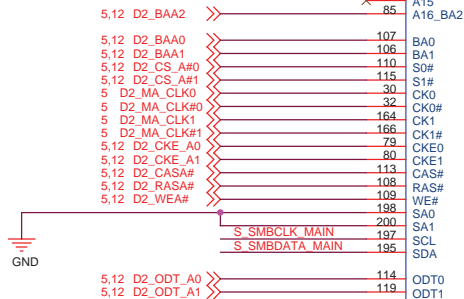


<< >>D2\_DQ\_A[63:0] 5  
 << >>D2\_DQS\_A[7:0] 5  
 << >>D2\_DQS\_A#[7:0] 5  
 << >>D2\_DM\_A[7:0] 5  
 << >>D2\_MAA[14:0] 5,12

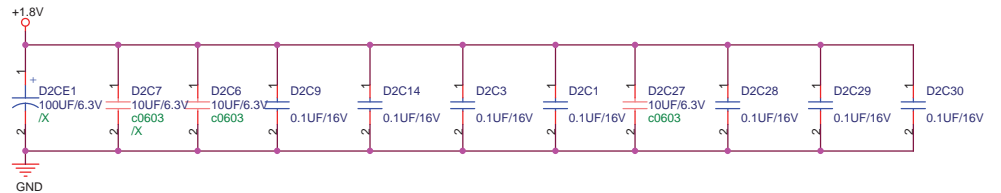
**DIMM1A**

D2_MAA0	102	A0	DQ0	5	D2_DQ_A0
D2_MAA1	101	A1	DQ1	7	D2_DQ_A1
D2_MAA2	100	A2	DQ2	17	D2_DQ_A2
D2_MAA3	99	A3	DQ3	19	D2_DQ_A3
D2_MAA4	98	A4	DQ4	4	D2_DQ_A4
D2_MAA5	97	A5	DQ5	6	D2_DQ_A5
D2_MAA6	94	A6	DQ6	14	D2_DQ_A6
D2_MAA7	92	A7	DQ7	16	D2_DQ_A7
D2_MAA8	93	A8	DQ8	23	D2_DQ_A8
D2_MAA9	91	A9	DQ9	25	D2_DQ_A9
D2_MAA10	105	A10/AP	DQ10	35	D2_DQ_A10
D2_MAA11	80	A11	DQ11	37	D2_DQ_A11
D2_MAA12	89	A12	DQ12	20	D2_DQ_A12
D2_MAA13	116	A13	DQ13	22	D2_DQ_A13
D2_MAA14	86	A14	DQ14	36	D2_DQ_A14
A15	85	A15	DQ15	38	D2_DQ_A15
A16_BA2		A16	DQ16	43	D2_DQ_A16
			DQ17	45	D2_DQ_A17
			DQ18	57	D2_DQ_A18
			DQ19	44	D2_DQ_A19
			DQ20	20	D2_DQ_A20
			DQ21	46	D2_DQ_A21
			DQ22	56	D2_DQ_A22
			DQ23	58	D2_DQ_A23
			DQ24	61	D2_DQ_A24
			DQ25	63	D2_DQ_A25
			DQ26	73	D2_DQ_A26
			DQ27	75	D2_DQ_A27
			DQ28	62	D2_DQ_A28
			DQ29	64	D2_DQ_A29
			DQ30	74	D2_DQ_A30
			DQ31	76	D2_DQ_A31
			DQ32	123	D2_DQ_A32
			DQ33	125	D2_DQ_A33
			DQ34	135	D2_DQ_A34
			DQ35	137	D2_DQ_A35
			DQ36	124	D2_DQ_A36
			DQ37	126	D2_DQ_A37
			DQ38	134	D2_DQ_A38
			DQ39	136	D2_DQ_A39
			DQ40	141	D2_DQ_A40
			DQ41	143	D2_DQ_A41
			DQ42	151	D2_DQ_A42
			DQ43	153	D2_DQ_A43
			DQ44	140	D2_DQ_A44
			DQ45	142	D2_DQ_A45
			DQ46	152	D2_DQ_A46
			DQ47	154	D2_DQ_A47
			DQ48	157	D2_DQ_A48
			DQ49	159	D2_DQ_A49
			DQ50	173	D2_DQ_A50
			DQ51	175	D2_DQ_A51
			DQ52	158	D2_DQ_A52
			DQ53	160	D2_DQ_A53
			DQ54	174	D2_DQ_A54
			DQ55	176	D2_DQ_A55
			DQ56	179	D2_DQ_A56
			DQ57	181	D2_DQ_A57
			DQ58	189	D2_DQ_A58
			DQ59	191	D2_DQ_A59
			DQ60	180	D2_DQ_A60
			DQ61	182	D2_DQ_A61
			DQ62	192	D2_DQ_A62
			DQ63	194	D2_DQ_A63

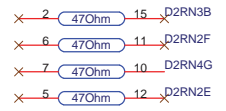
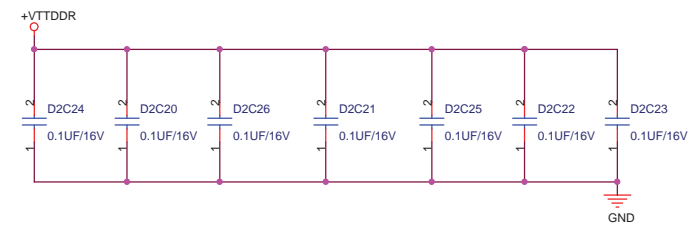
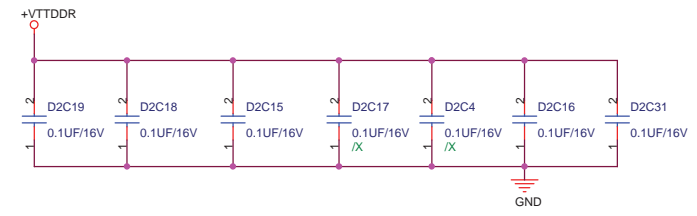
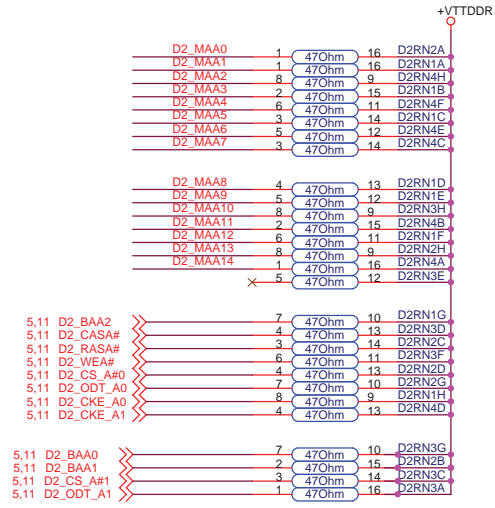
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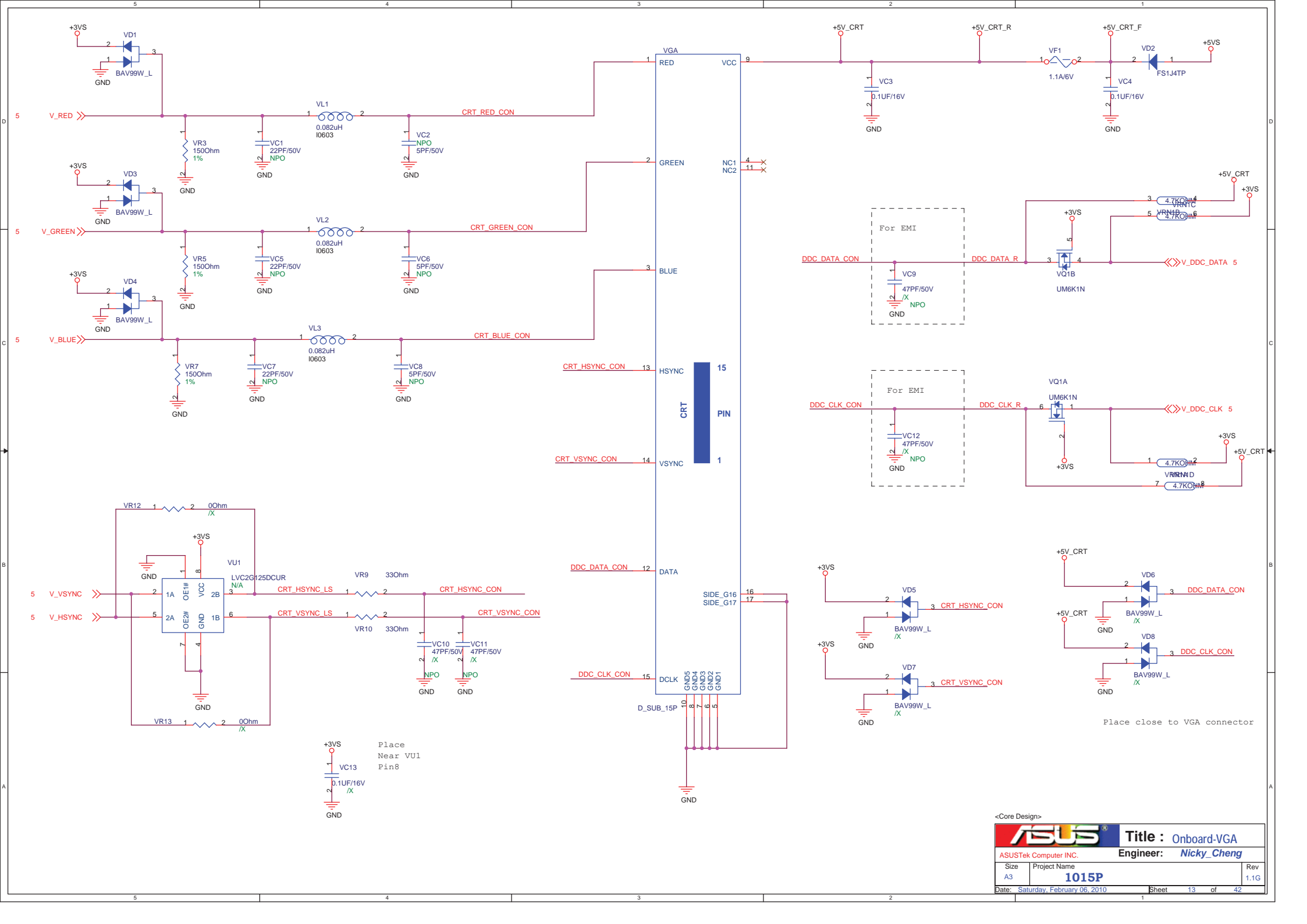


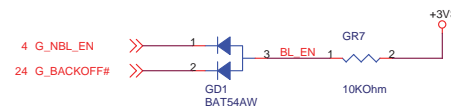
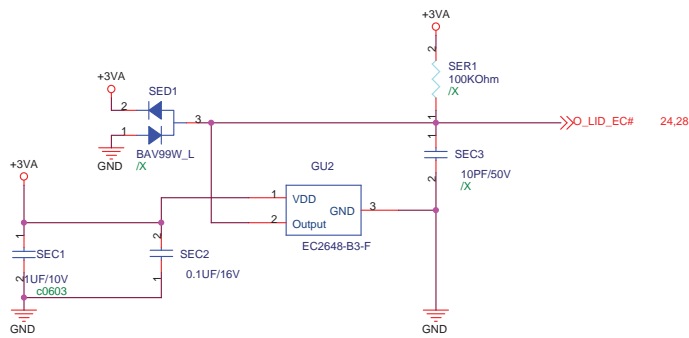
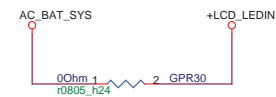
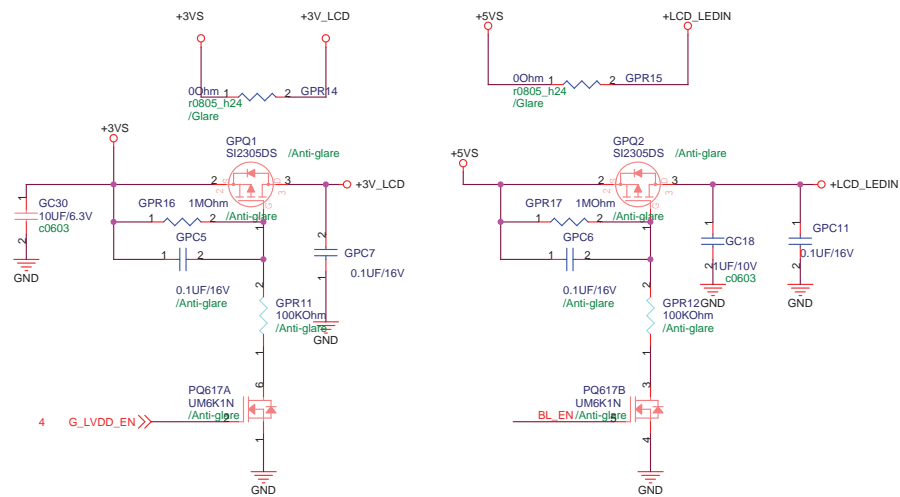
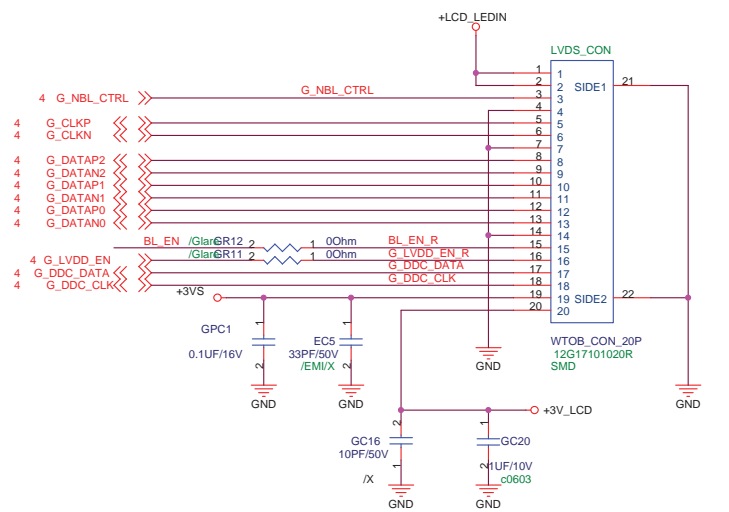
"糧 Layout 訣賀叫σ祇2nd source / 12G025C2200X PCB footprint  
 , 磷 2nd DIMM 斂耗婉築ノ玻ネ 豊- 2nd source PCB footprint  
 數main source size DIMM羅 Tトイ"



<> D2\_MAA[14:0] 5,11



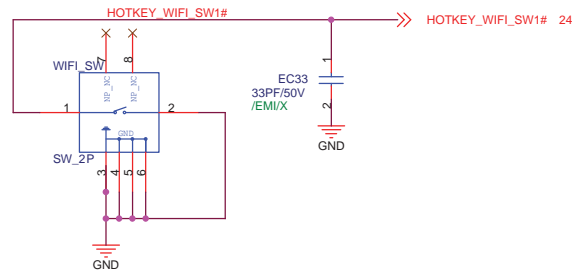
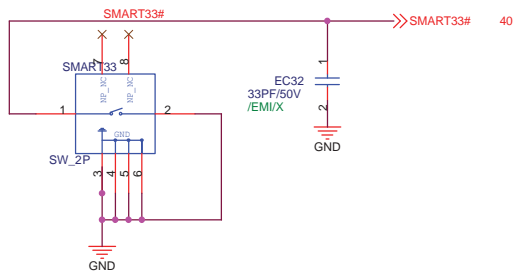




G_DDC_CLK	GC1	2	1	10PF/50V	/X
G_DDC_DATA	GC2	2	1	10PF/50V	/X
G_CLKP	GC3	2	1	10PF/50V	N/A
G_CLKN	GC4	2	1	10PF/50V	N/A
G_DATAP2	GC5	2	1	10PF/50V	N/A
G_DATAN2	GC6	2	1	10PF/50V	N/A
G_DATAP1	GC7	2	1	10PF/50V	N/A
G_DATAN1	GC8	2	1	10PF/50V	N/A
G_DATAP0	GC9	2	1	10PF/50V	N/A
G_DATAN0	GC10	2	1	10PF/50V	N/A
G_NBL_CTRL	GC12	2	1	10PF/50V	/X
BL_EN	EC11	2	1	10PF/50V	EMI/X
G_LVDD_EN	EC12	2	1	10PF/50V	EMI/X

<Core Design>

		<b>Title : LVDS Conn_LID</b>	
ASUSTek Computer INC.		Engineer: <i>Nicky_Cheng</i>	
Size	Project Name	Rev	
Custom	<b>1015P</b>	1.1G	
Date: Saturday, February 06, 2010	Sheet	14	of 42



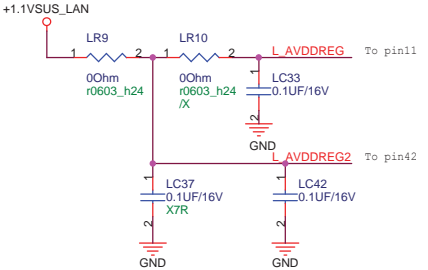
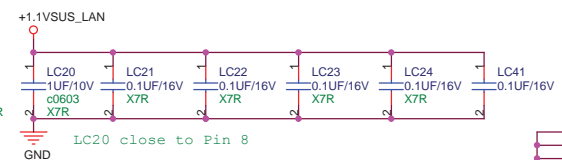
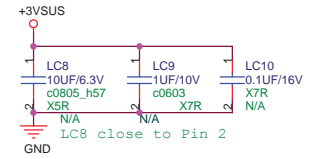
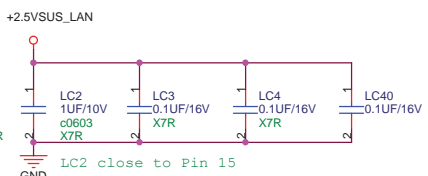
<Core Design>

		<b>Title :</b> WIFI_SAMRT33	
ASUSTek Computer INC.		Engineer: <i>Nicky_Cheng</i>	
Size A3	Project Name <b>1015P</b>		Rev 1.1G
Date: Saturday, February 06, 2010		Sheet 15 of 42	

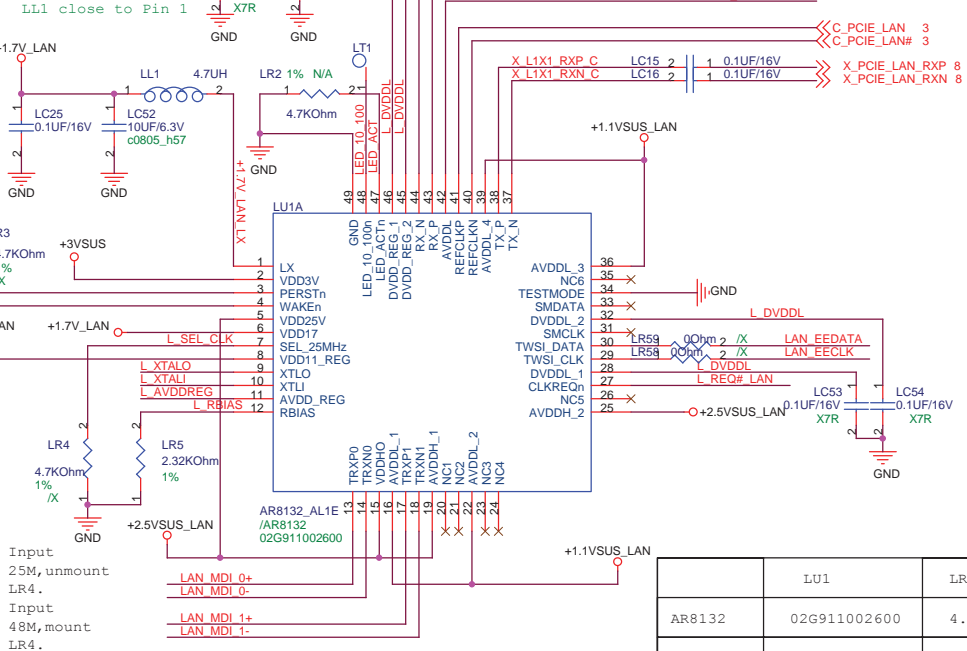
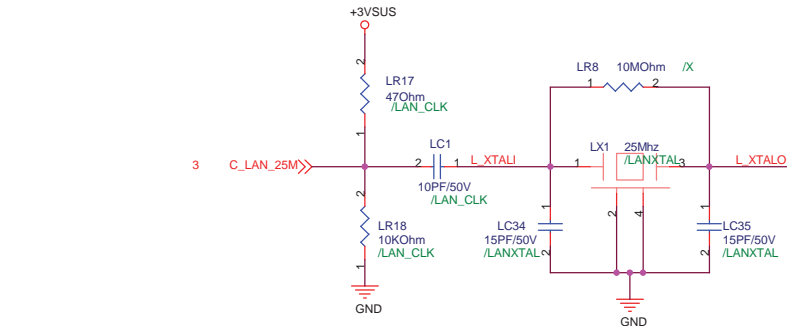


**LAN AR8132M**  
**Symbol 02G911002600**  
**BOM 02G911002601**

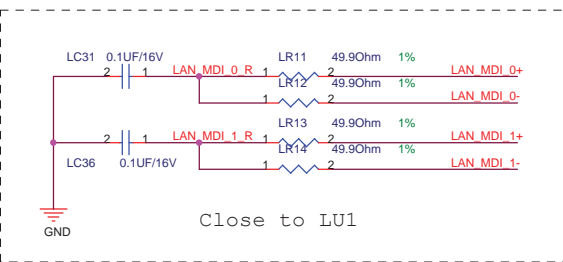
	LR2
Normal	N/A
Overclocking	/X



	LR9	LR10
Normal	N/A	/X
Overclocking	/X	N/A



	LU1	LR59	LR58	LC51	LU2	LC49	LC50
AR8132	02G911002600	4.7K	N/A	N/A	N/A	/X	/X
AR8132M	02G911002601	0 ohm	/X	/X	/X	/X	N/A



<Core Design>

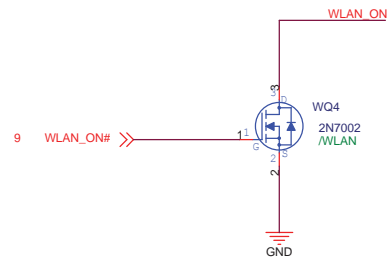
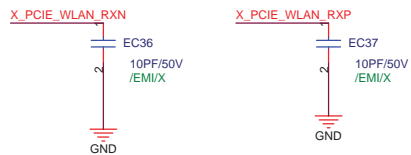
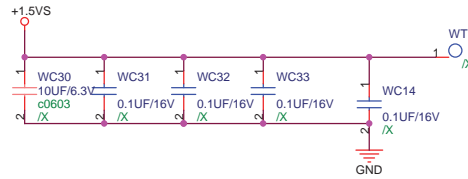
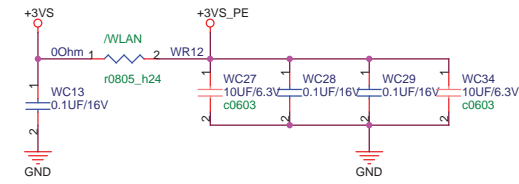
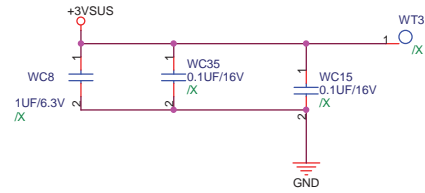
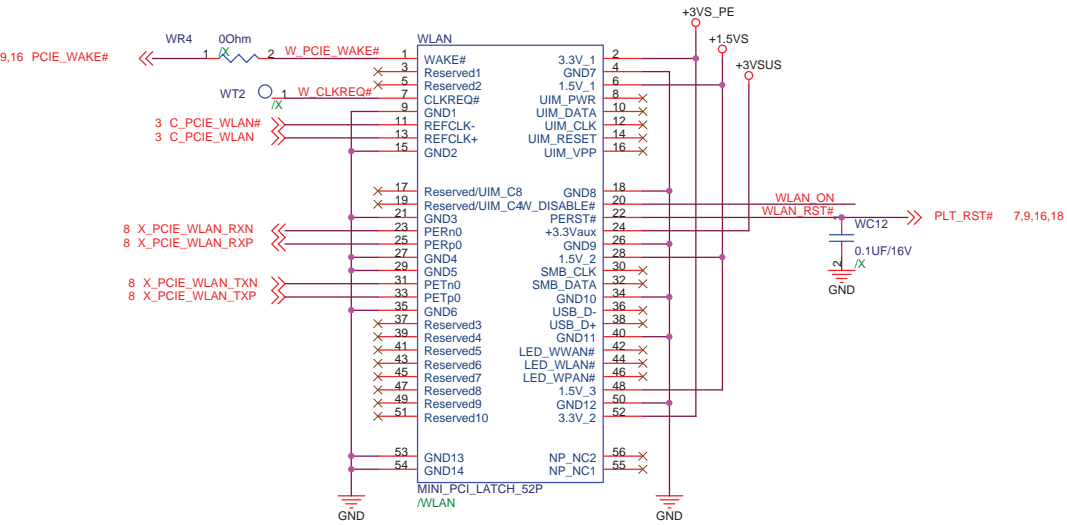
**ASUS** Title: LAN\_AR8132

ASUSTek Computer INC. Engineer: Nicky\_Cheng

Size	Project Name	Rev
A3	1015P	1.1G

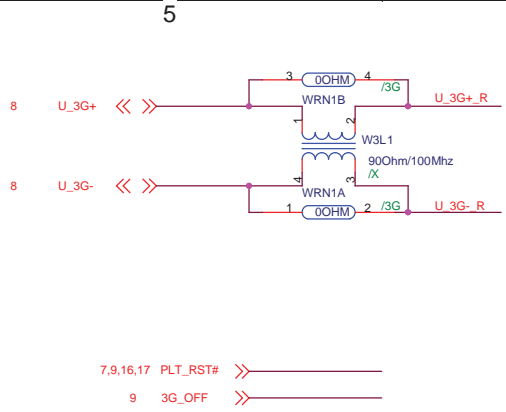
Date: Saturday, February 06, 2010 Sheet 16 of 41

**WIFI use PCIE 1.1 Spec**  
**+3VS = 1.0A peak / 0.75A Normal**  
**+1.5VS = 0.5A peak / 0.375A Normal**  
**+3VSUS = 0.375A peak / 0.25A Normal**

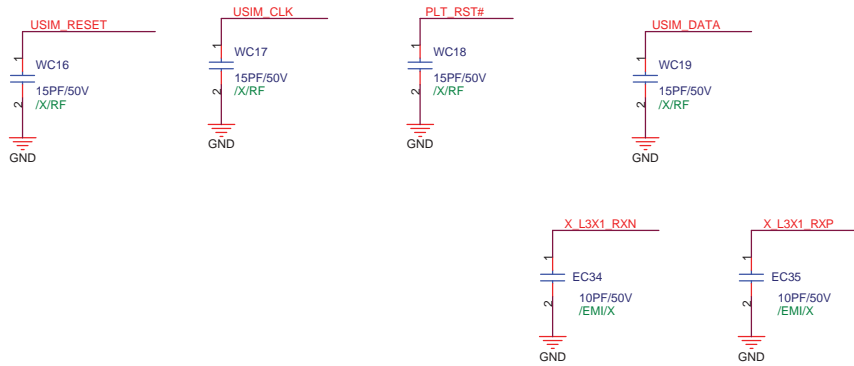
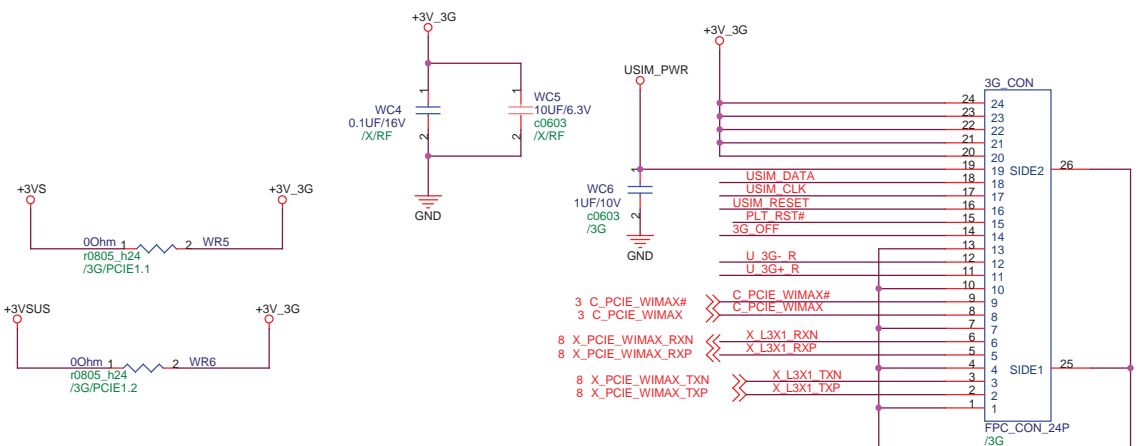
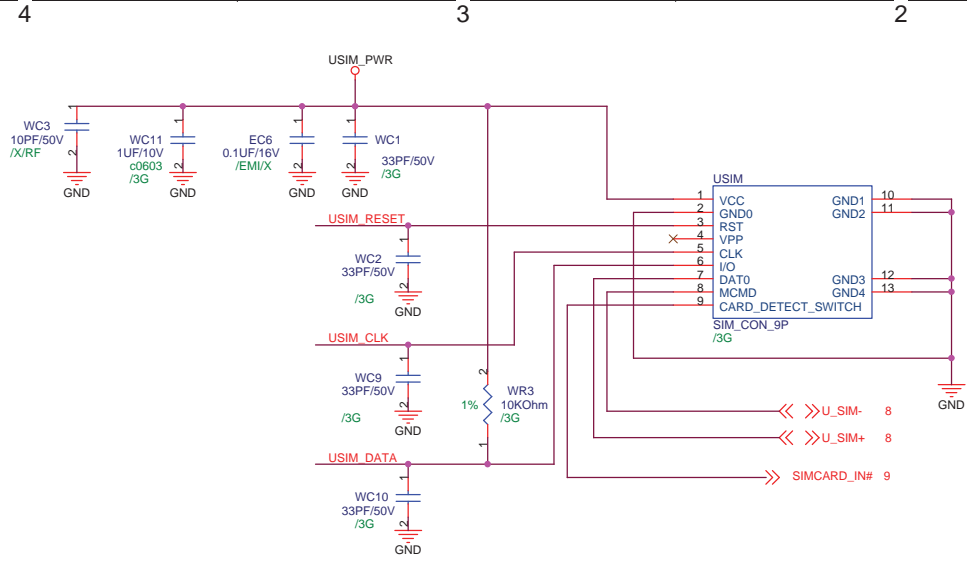


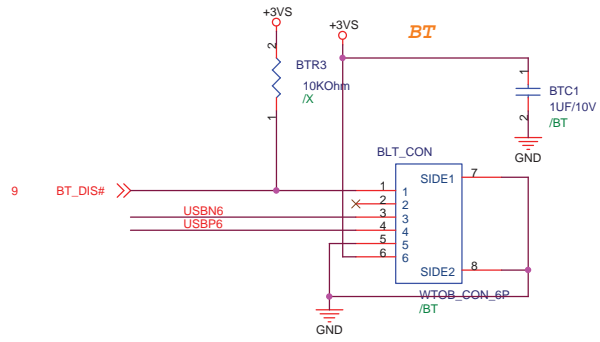
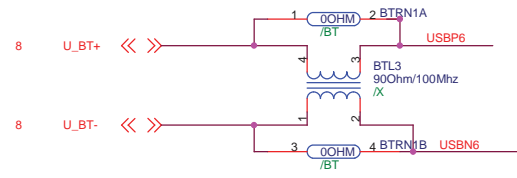
<Core Design>

<b>ASUS</b>		<b>Title : WLAN</b>	
ASUSTek Computer INC.		Engineer: <b>Nicky_Cheng</b>	
Size A3	Project Name <b>1015P</b>	Rev 1.1G	
Date: Saturday, February 06, 2010		Sheet 17 of 42	



7,9,16,17 PLT\_RST# >>>  
 9 3G\_OFF >>>

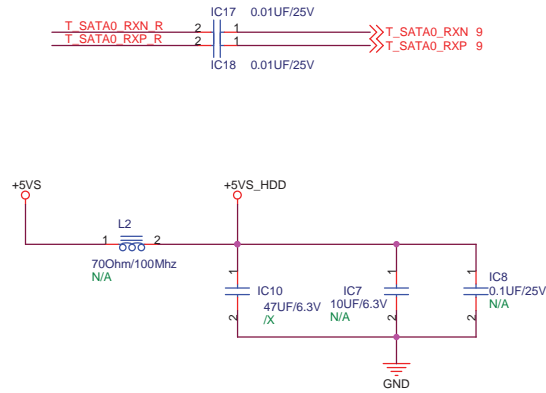
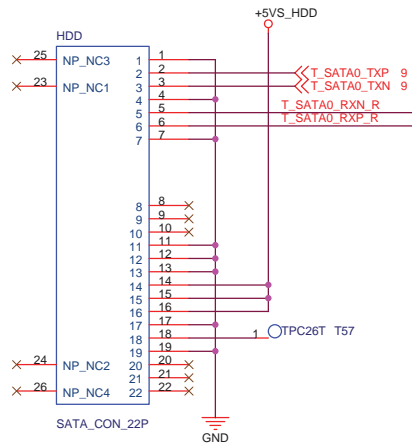




<Core Design>

<b>ASUS</b>		<b>Title : Bluetooth</b>	
ASUSTek Computer INC.		Engineer: <i>Nicky_Cheng</i>	
Size A3	Project Name <b>1015P</b>	Rev 1.1G	
Date: Saturday, February 06, 2010		Sheet	19 of 42

# SATA HDD Connector



<Core Design>

<b>ASUS</b>		<b>Title : HD_CON</b>	
ASUSTek Computer INC.		Engineer: <i>Nicky_Cheng</i>	
Size A3	Project Name <b>1015P</b>	Rev 1.1G	
Date: Saturday, February 06, 2010		Sheet	20 of 42

5

4

3

2

1

D

D

C

C

B

B

A

A

5

4

3

2

1

<Core Design>



Title : USB3.0

ASUSTek Computer INC.

Engineer:

Size	Project Name	Rev
C	1015P	1.1G

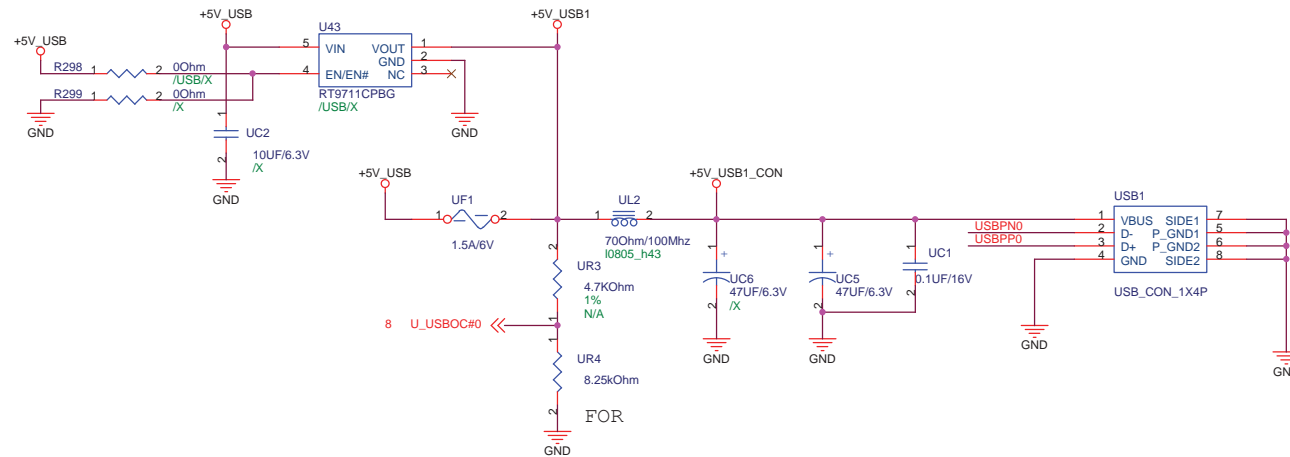
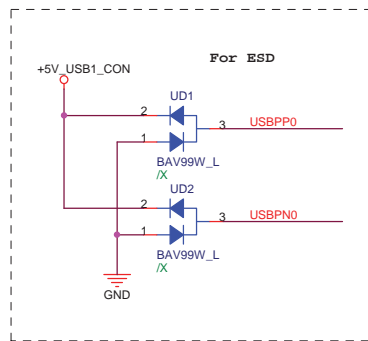
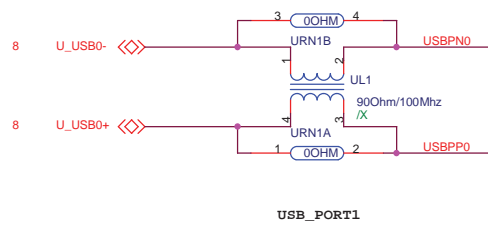
Date: Saturday, February 06, 2010 Sheet 21 of 42



<Core Design>

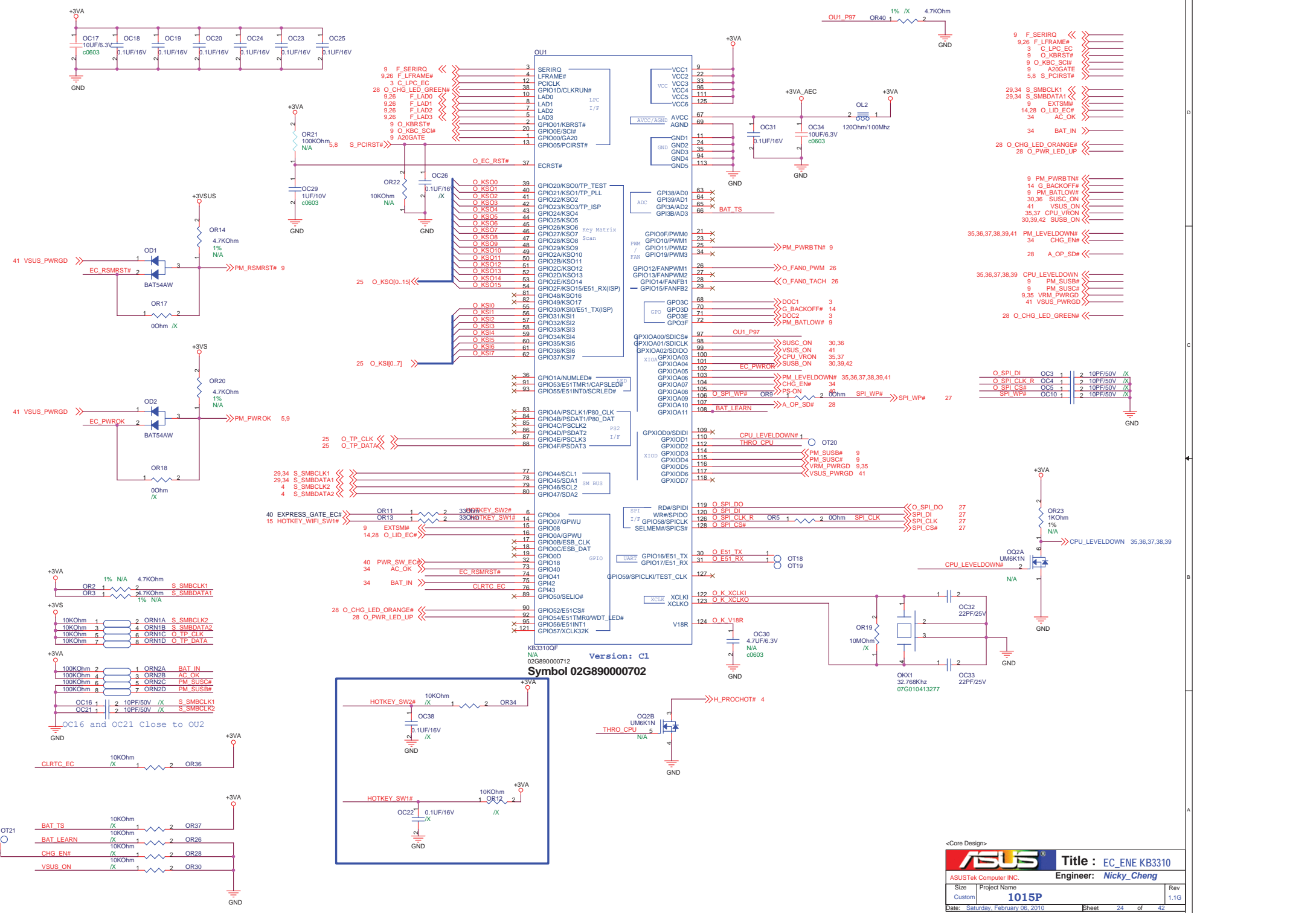
		<b>Title :</b> USB 3.0
ASUSTek Computer INC.		<b>Engineer:</b> <i>Nicky_Cheng</i>
Size	Project Name	Rev
A3	<b>1015P</b>	1.1G
Date: Saturday, February 06, 2010		Sheet 22 of 42



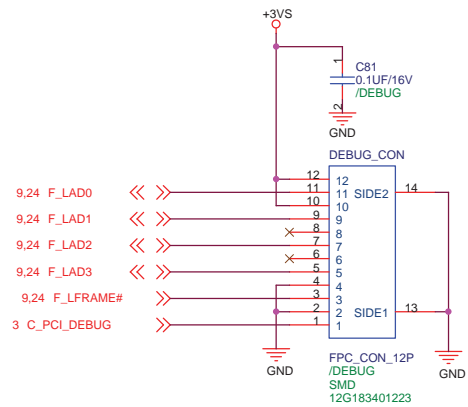
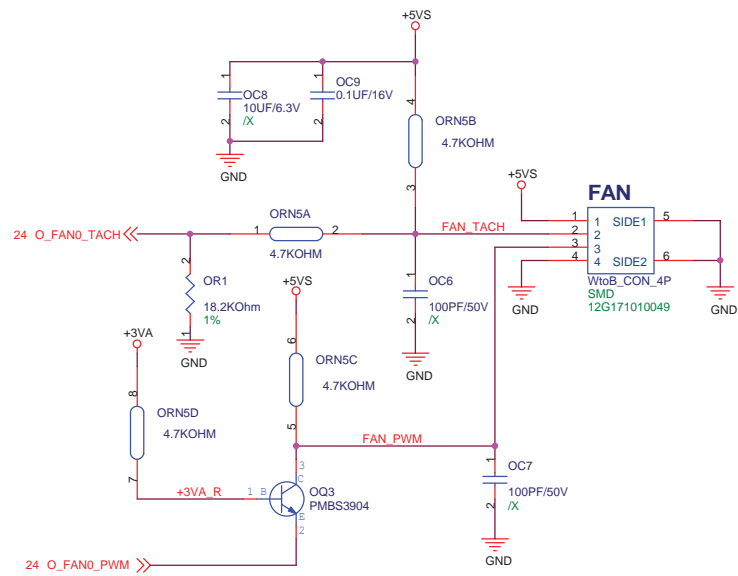


<Core Design>

<b>ASUS</b>		<b>Title : USB Port1</b>	
ASUSTek Computer INC.		Engineer: <i>Nicky_Cheng</i>	
Size	Project Name	Rev	
A3	<b>1015P</b>	1.1G	
Date: Saturday, February 06, 2010		Sheet	23 of 42

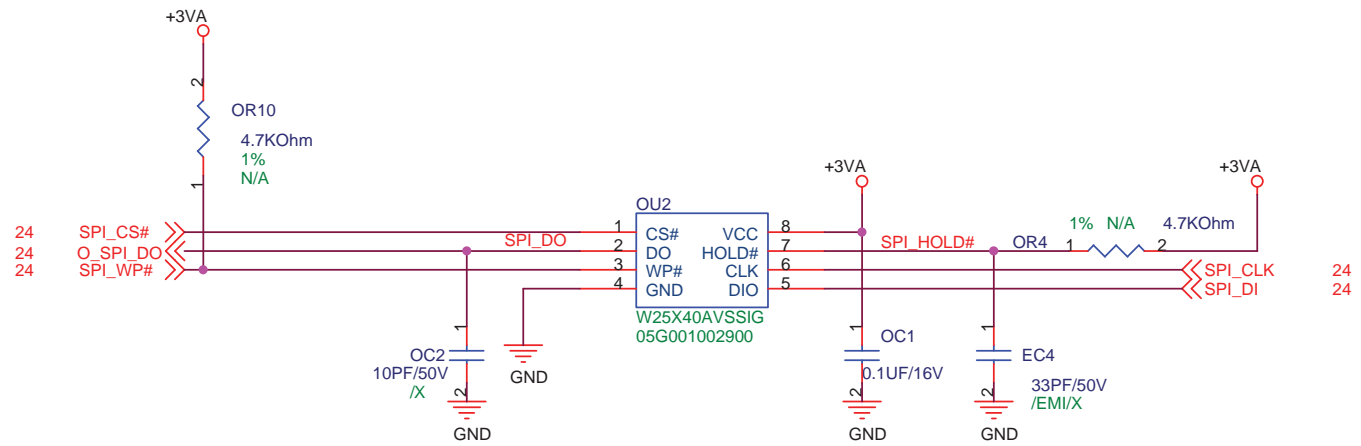






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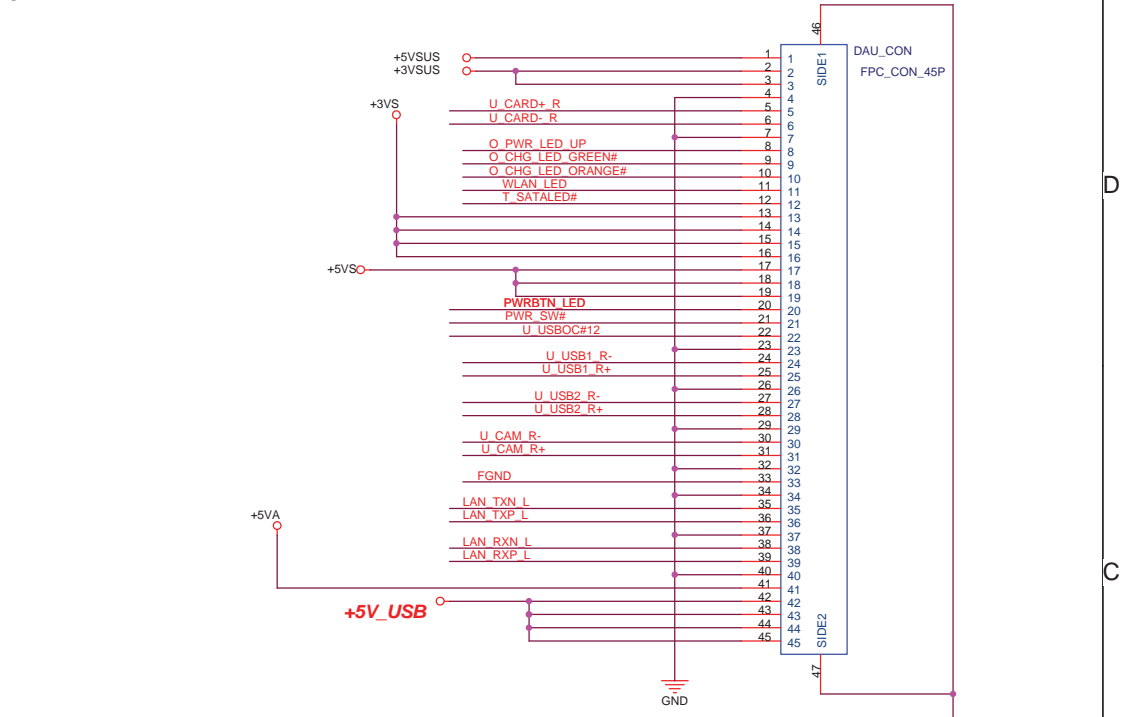
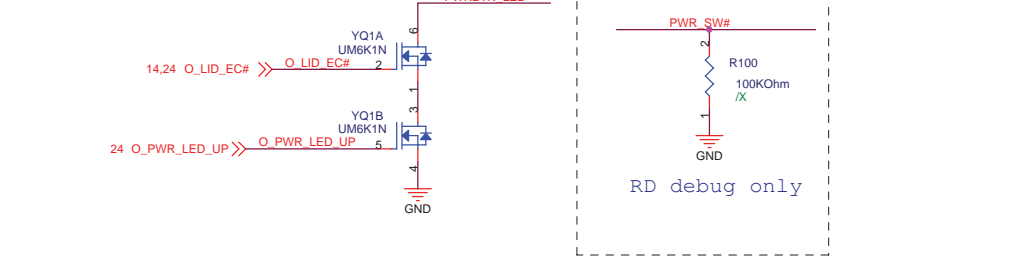
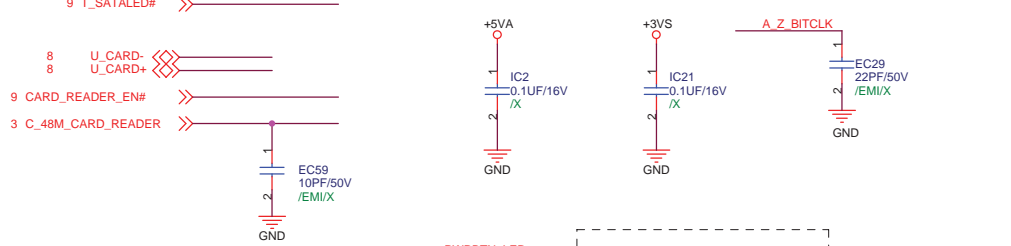
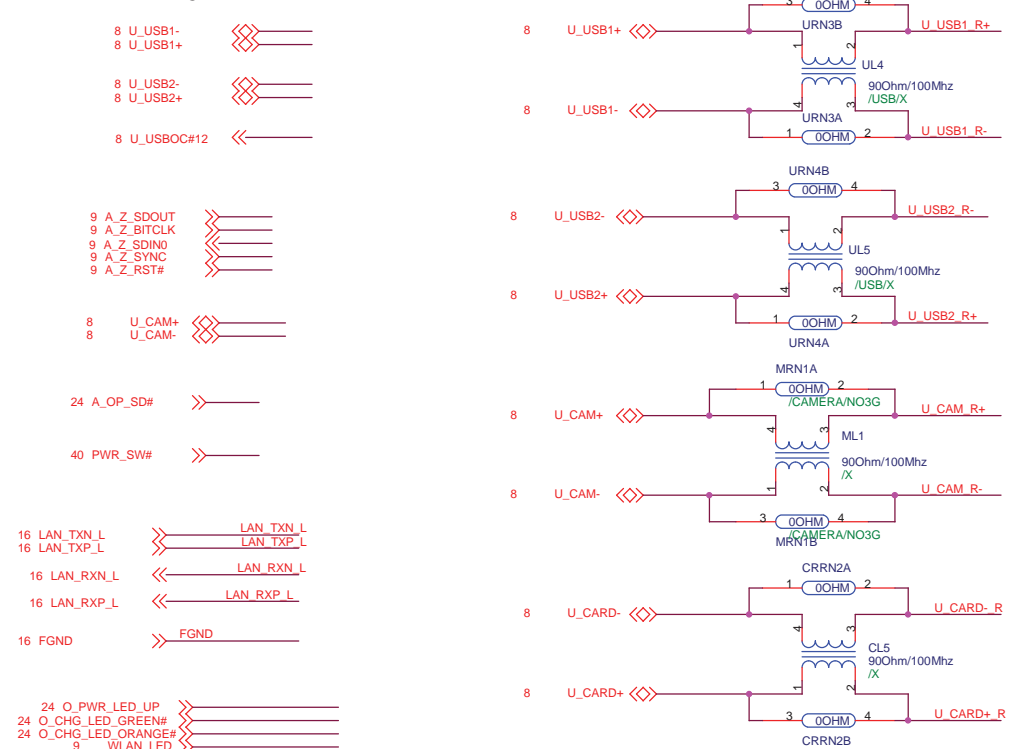
<b>ASUS</b>		<b>Title : Fan_Debug</b>	
ASUSTek Computer INC.		Engineer: <i>Nicky_Cheng</i>	
Size A3	Project Name <b>1015P</b>	Rev 1.1G	
Date: Saturday, February 06, 2010		Sheet	26 of 42



05G001002900;  
 05G00100F131;  
 05G00100F133

<Core Design>

		<b>Title :</b> SPI_ROM
ASUSTek Computer INC.		<b>Engineer:</b> Nicky_Cheng
Size A4	Project Name <b>1015P</b>	Rev 1.1G
Date: Saturday, February 06, 2010		Sheet 27 of 42



Mode	Adapater Mode	Battery Mode
Battery power is between 100%~40%	Orange ON	Green ON
Battery power is between 40%~10%	Orange Blinking Slowly	Green Blinking Slowly
Battery power is less than 10%	Orange Blinking Quickly	Green Blinking Quickly
S3/S5 Mode	Scenario the same as above	OFF

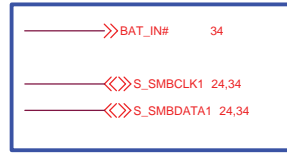
<Core Design>

**Title :** DUA\_CON  
**ASUSTek Computer INC. Engineer:** Nicky\_Cheng

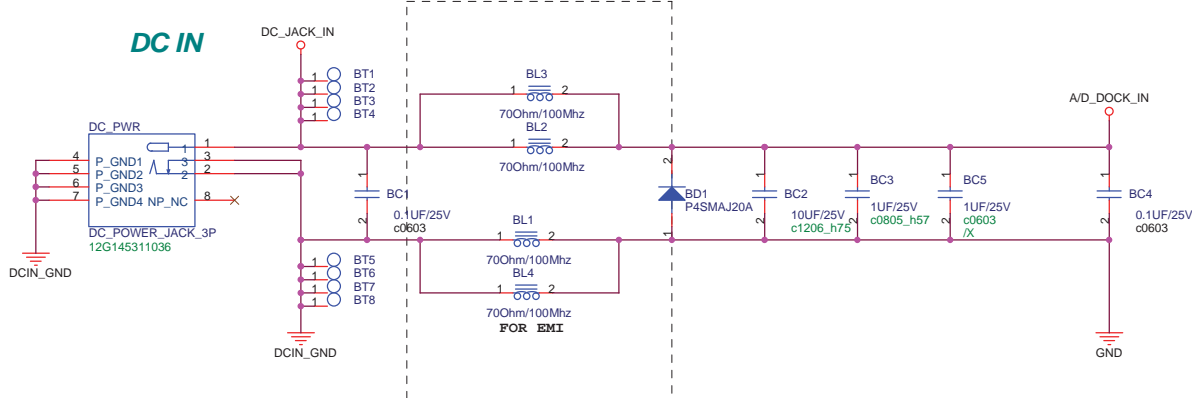
Size	Project Name	Rev
A3	1015P	1.1G

Date: Saturday, February 06, 2010 Sheet 28 of 42

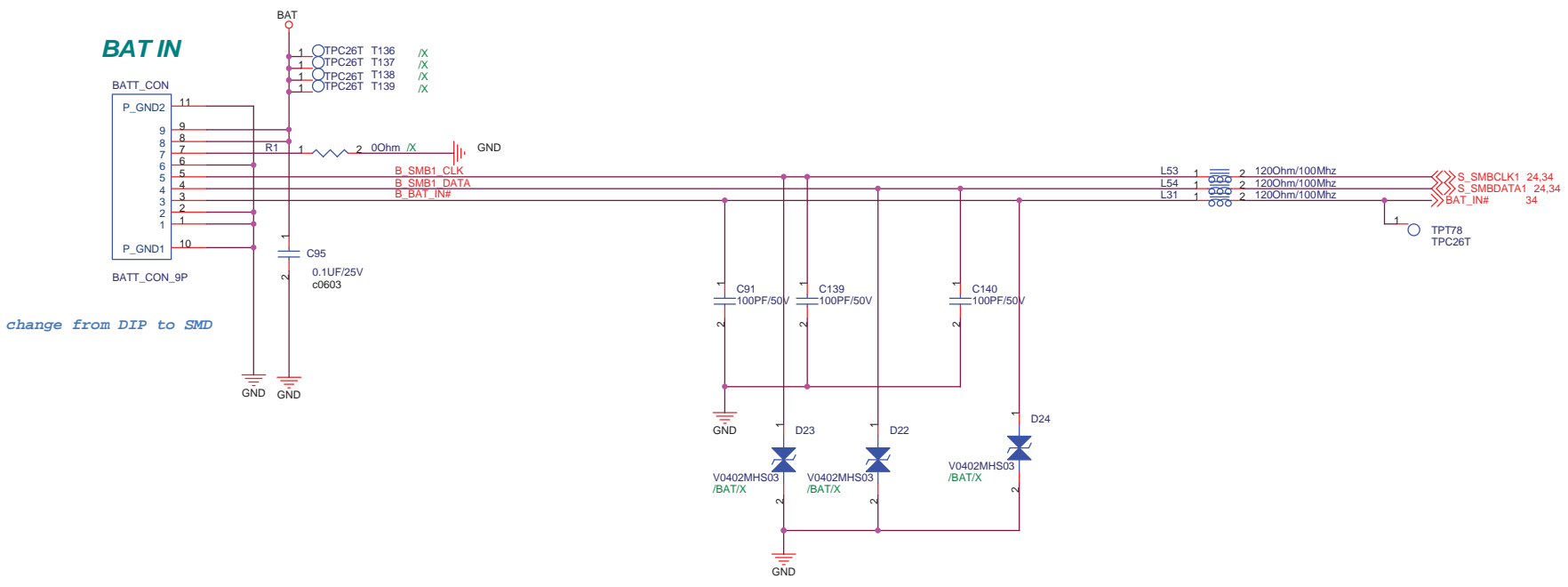
0.1B Beta



DC IN



BAT IN



change from DIP to SMD

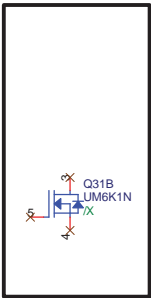
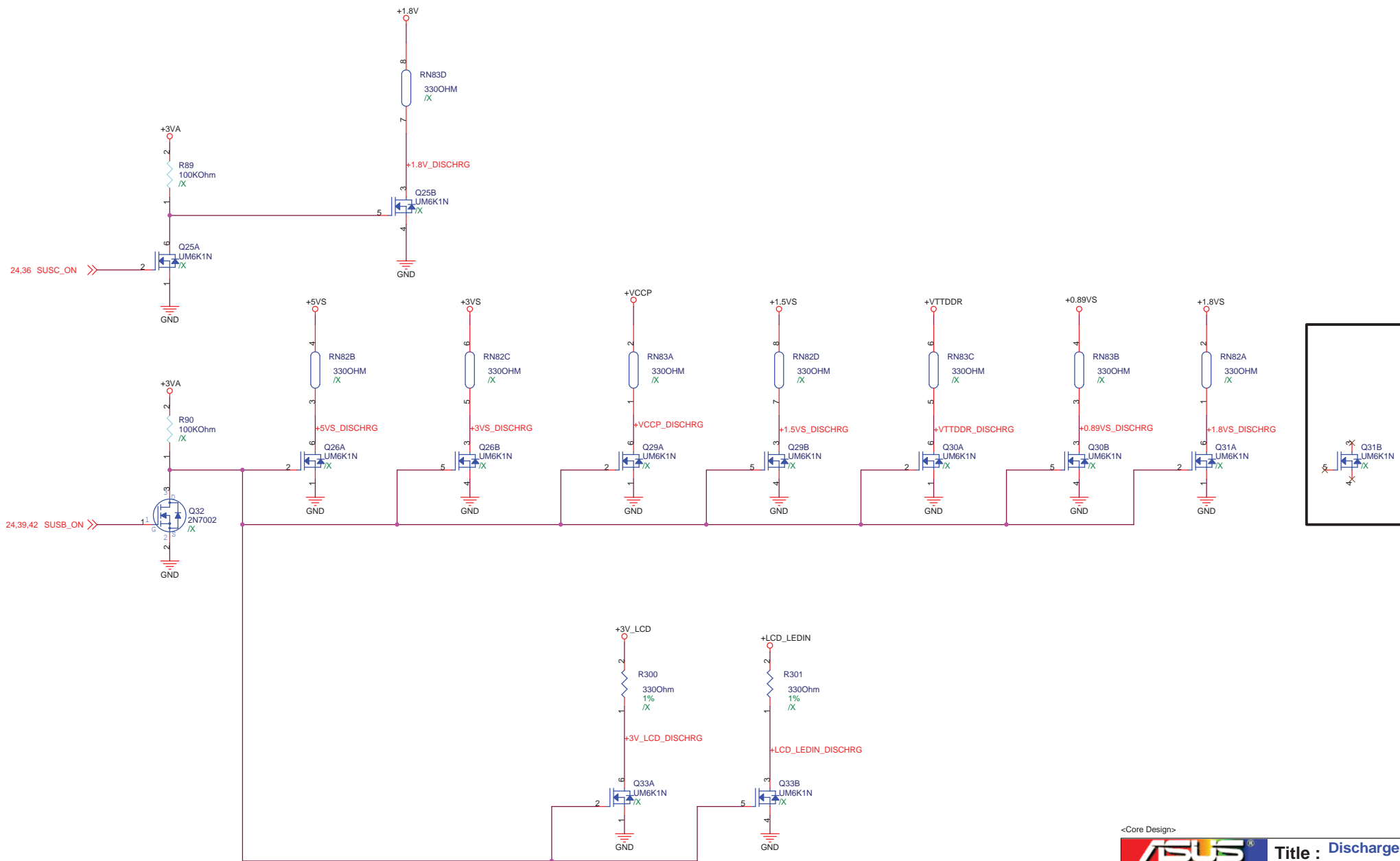
<Core Design>

**ASUS** Title : PWR Jack  
 ASUSTek Computer INC. Engineer: Nicky\_Cheng

Size	Project Name	Rev
A3	1015P	1.1G

Date: Saturday, February 06, 2010 Sheet 29 of 42






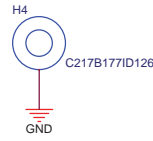
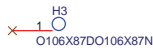
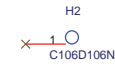
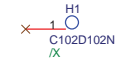
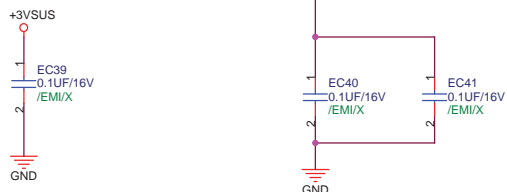
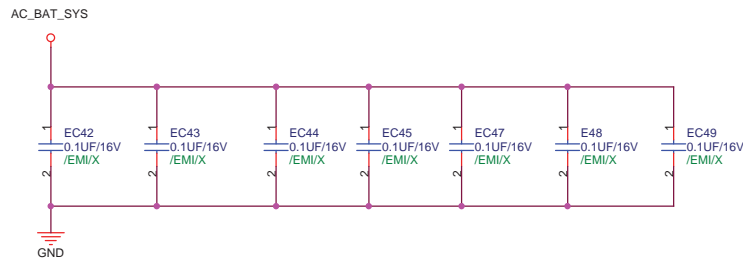
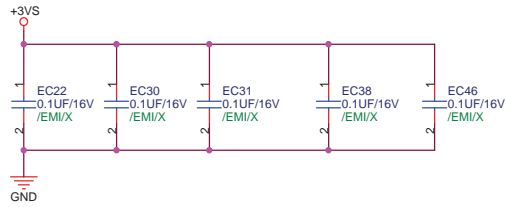
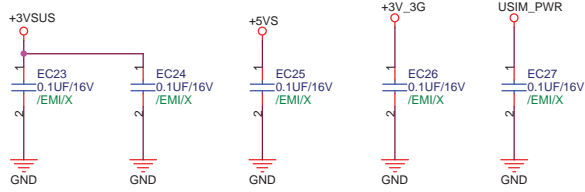
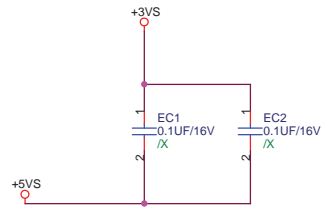
<Core Design>

<b>ASUS</b>		<b>Title : Discharge</b>	
ASUSTek Computer INC.		Engineer: <b>Nicky Cheng</b>	
Size A3	Project Name <b>1015P</b>	Rev 1.1G	
Date: Saturday, February 06, 2010		Sheet	30 of 42

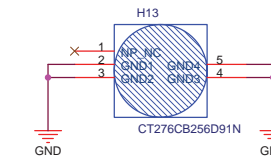
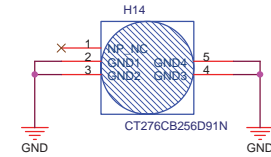
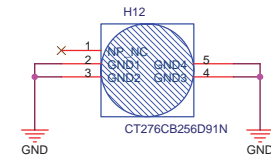
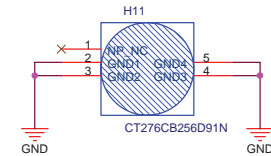
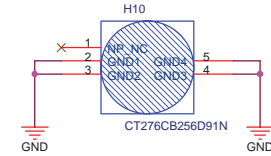
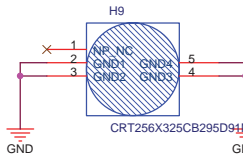
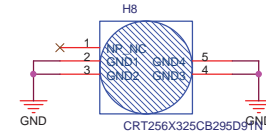
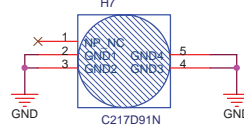
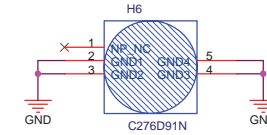
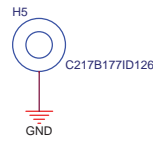


<Core Design>

		<b>Title : SD_CON</b>	
ASUSTek Computer INC.		Engineer: <i>Nicky Cheng</i>	
Size	Project Name		Rev
A3	<b>1015P</b>		1.1G
Date: Saturday, February 06, 2010		Sheet	31 of 42

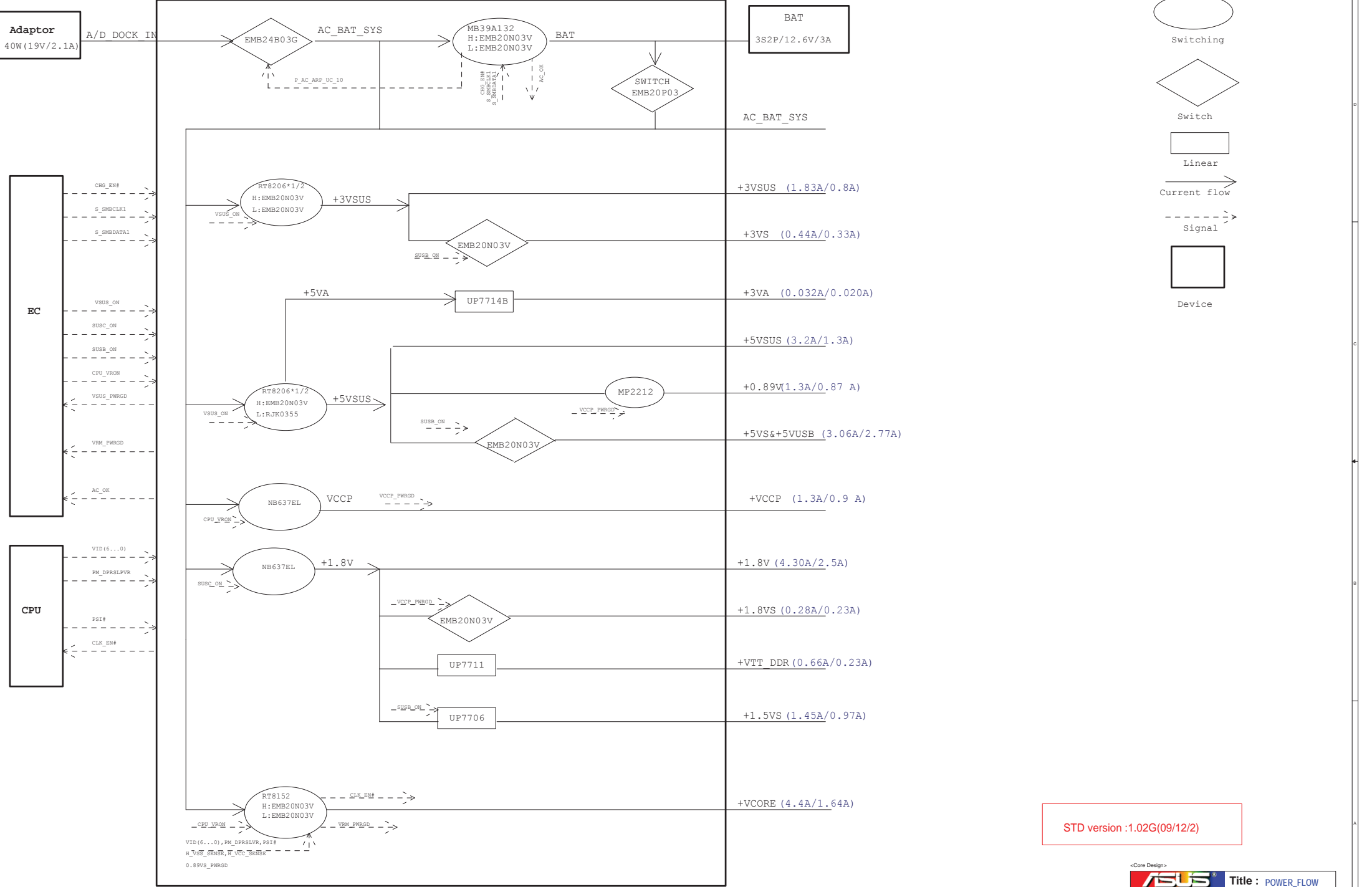


CPU Thermal HOLD

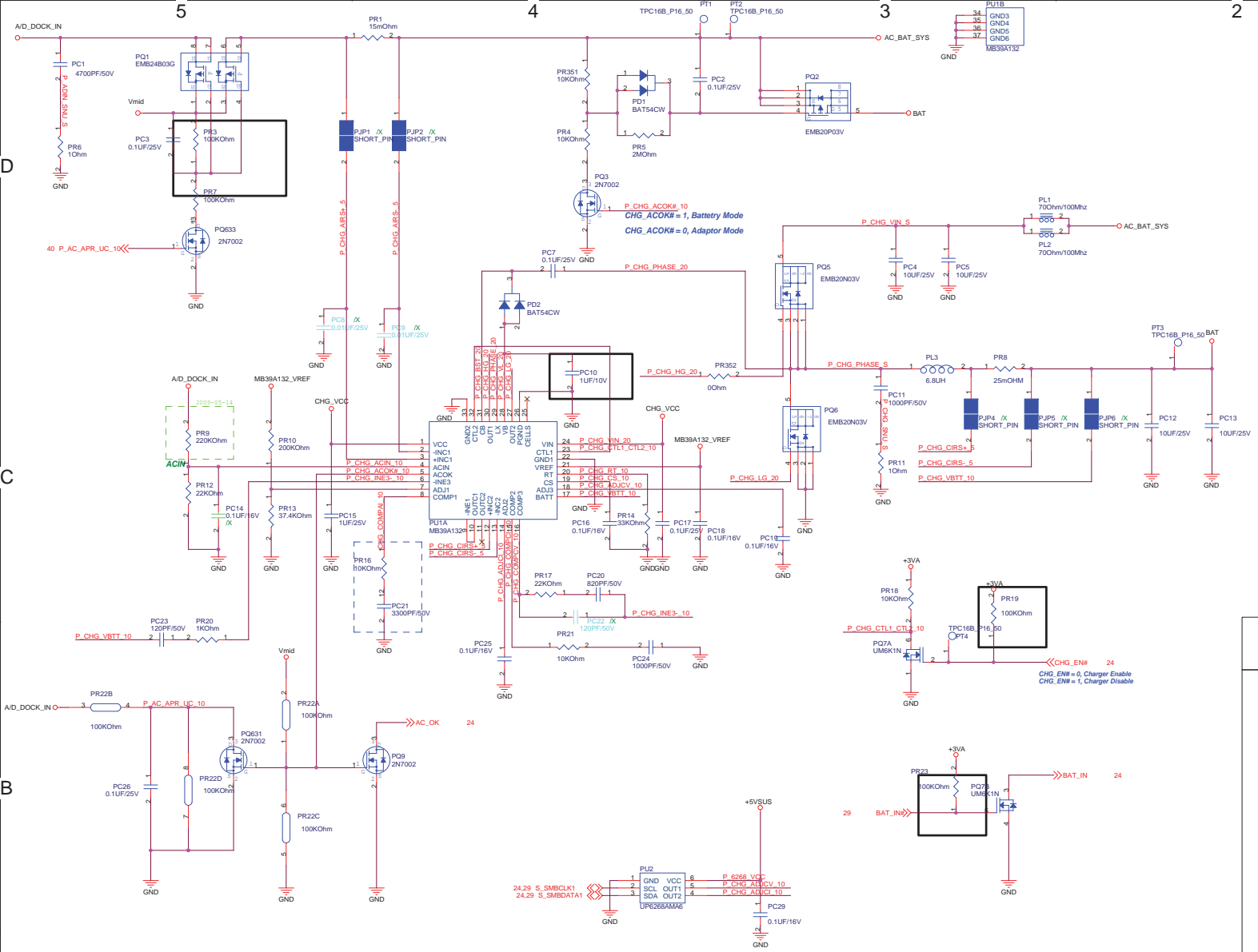


<Core Design>

<b>ASUS</b>		<b>Title : SREW HOLE&amp;EMI</b>	
ASUSTek Computer INC.		Engineer: <i>Nicky_Cheng</i>	
Size	Project Name	Rev	
A3	<b>1015P</b>	1.1G	
Date: Saturday, February 06, 2010		Sheet	32 of 42



STD version : 1.02G(09/12/2)

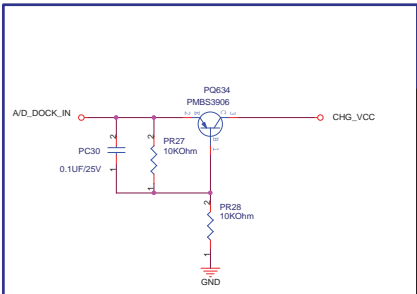


**Power stage**

- I/P Current:**  
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.64A$
- Ripple Current:**  
 $I_{rip} = 1.18A$   
 $I_{spec} = 2A$   
 $\phi 1 pcs$
- Inductor Spec:**  
 $I_{sat} = 10A$   
 $I_{dc} = 5.5A$   
 $DCR = 37m\Omega$
- MOSFET Spec:**  
**H-side MOSFET: SI7326DN\_T1\_E3**  
 $R_{ds(ON)} = 22 m\Omega$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 6.5A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 40A$  (Pause  $\leq 10\mu s$ )  
**L-side MOSFET: SI7326DN\_T1\_E3**  
 $R_{ds(ON)} = 22 m\Omega$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 6.5A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 40A$  (Pause  $\leq 10\mu s$ )

**Controller**

- Voltage & Current:**  
**+12.6V @2.5A**
- Frequency:**  
**PR122=33KOHM,**  
**Fosc=515KHz**
- OCp:**
- POR:**  
**POR Hysteresis = 0.1V**  
**V on = 7.5V**
- Enable Voltage:**  
**V = 2.9V**
- Soft start time:**  
**Tss=23ms**
- Phase selection:**  
**N/A**
- Inrush Current:**  
**C total = 20uF**  
**I inrush = 0.01A**

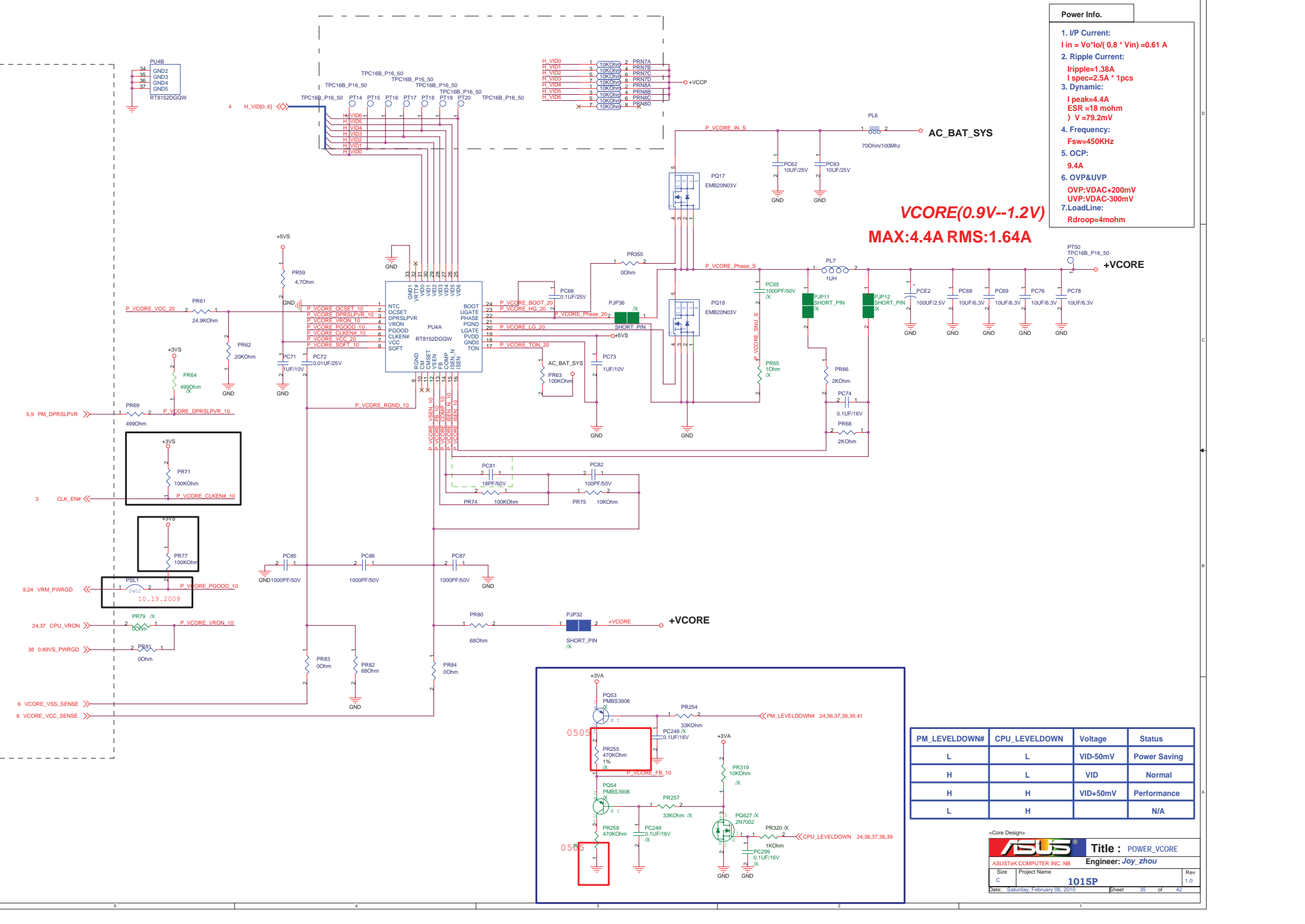


**Battery Charging Current :**  
 $4.4V > V_{adj2} \geq 0V \Rightarrow$   
 $I_{chg} = (V_{adj2} - 0.075) / (25 \cdot R_s)$   
 BATSEL\_2P# = 1,  $I_{ch} = 1.49A$   
 BATSEL\_2P# = 0,  $I_{ch} = 2.62A$   
**Input Adaptor Max. Current Limit :**  
 $I_{limit\_current} = (V_{adj1} - 0.075) / (25 \cdot R_s) = 1.90A$

**Pre-Charging Mode :**  
 Precharging current = 149.2mA  
 $V_{adj2} = 168mV$   
**ACIN Threshold = 1.25V**  
 Adaptor > 13.75V, System Powered by Adaptor  
 Adaptor < 13.75V, System Powered by Battery

**Battery Charging Voltage :**  
 $V_{adj3} : V_{REF} \Rightarrow V_{bat} = 4.2V / cell$   
 $3.9V > V_{adj3} > 2.4V \Rightarrow V_{bat} = 4.35V / cell$   
 $V_{adj3} : GND \Rightarrow V_{bat} = 4.0V / cell$   
 $2.2V > V_{adj3} > 1.1V \Rightarrow V_{bat} = 2 \cdot V_{adj3}$   
**Battery Cell Selection :**  
 CELLS: VREF  $\Rightarrow$  4 Cells;  
 CELLS: OPEN  $\Rightarrow$  3 Cells;  
 CELLS: GND  $\Rightarrow$  2 Cells;

**VREF = 5.0V**  
 $f_{osc}(KHz) = 17000 / RT (K\Omega)$   
 Soft start:  $ts(s) = 0.13 \cdot CS (\mu F)$

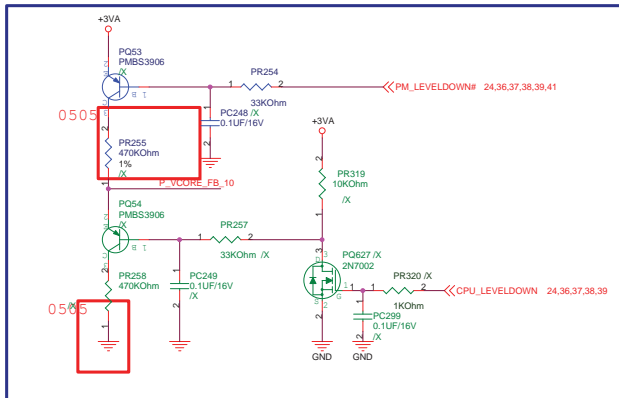


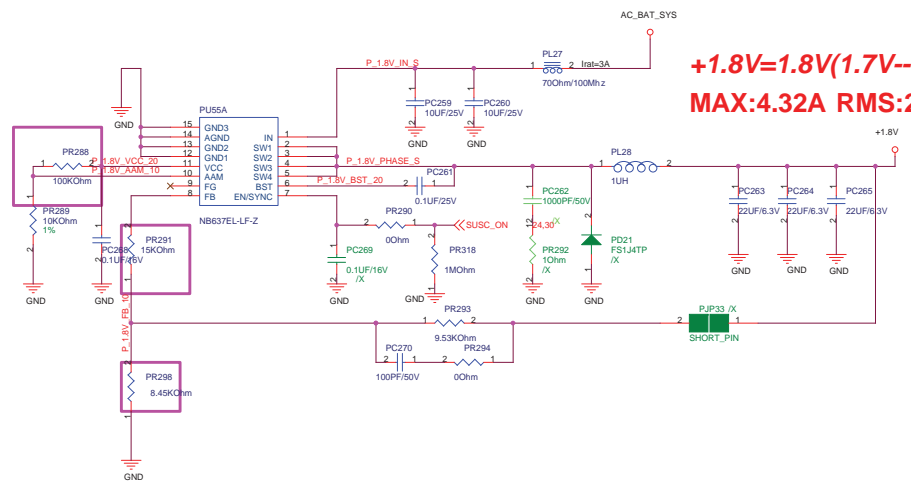
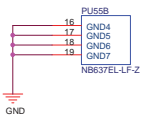
**Power Info.**

- I/P Current:  
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 0.61 \text{ A}$
- Ripple Current:  
 $I_{ripple} = 1.38 \text{ A}$   
 $I_{spec} = 2.5 \text{ A} \cdot 1 \text{ pcs}$
- Dynamic:  
 $I_{peak} = 4.4 \text{ A}$   
 $ESR = 18 \text{ mohm}$   
 $V = 79.2 \text{ mV}$
- Frequency:  
 $F_{sw} = 450 \text{ KHz}$
- OCP:  
 $9.4 \text{ A}$
- OVP&UVP  
 $OVP = V_{DAC} + 200 \text{ mV}$   
 $UVP = V_{DAC} - 300 \text{ mV}$
- LoadLine:  
 $R_{droop} = 4 \text{ mohm}$

**VCORE(0.9V--1.2V)**  
**MAX:4.4A RMS:1.64A**

PM_LEVELDOWN#	CPU_LEVELDOWN	Voltage	Status
L	L	VID-50mV	Power Saving
H	L	VID	Normal
H	H	VID+50mV	Performance
L	H		N/A



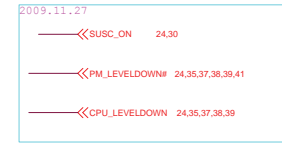


**Power Info.**

- I/P Current:**  
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.08A$
- Ripple Current:**  
 $I_{rip} = 1A$
- Frequency:**  
 $F_{osc} = 600KHz$
- Current Limit:**  
**6A**

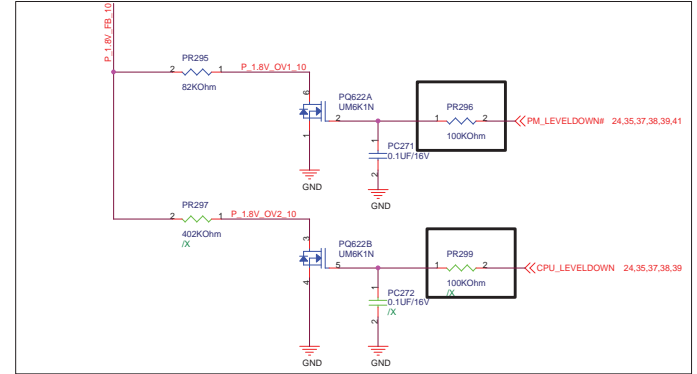
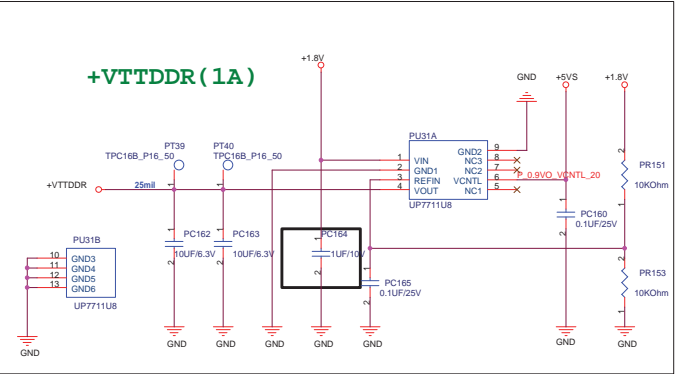
**0.9VS@1A**

- Dropout Voltage:**  
 $V = 0.3V (I_o = 2A)$
- Current Limit:**  
 $I_{limit} = 4A$
- Continue Current:**  
 $I_{cont} = 3A$
- Power Dissipation:**  
 $R_{thjc} = 52 /W$   
 $P_d = 1.9W$



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.670V	Power Saving
H	L	H	1.800V	Normal
H	H	L	1.912V	Performance
L	H	L		

**+VTTDDR (1A)**

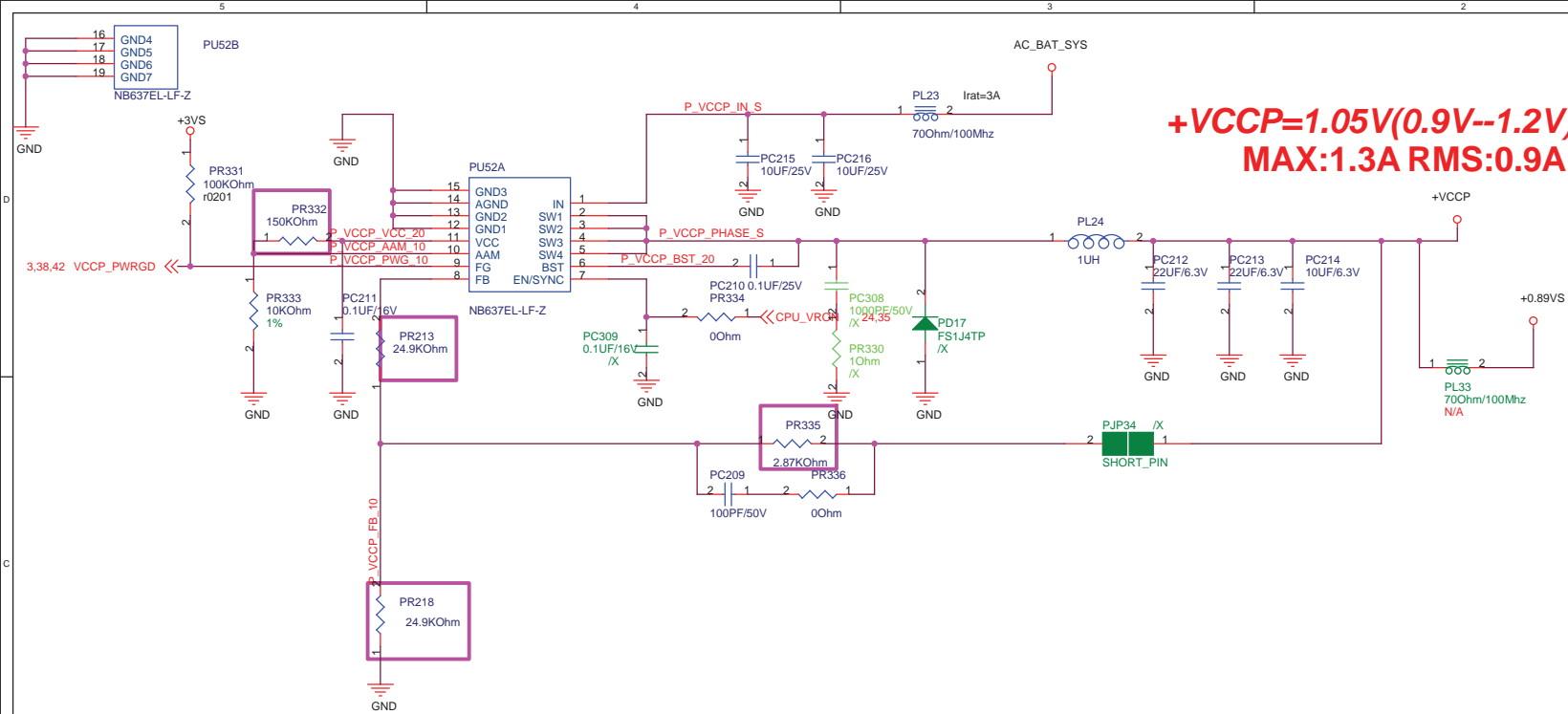


<Core Design>

**ASUS** Title: +1.8V&VTTDDR  
 ASUSTek Computer INC Engineer: Joy\_Zhou

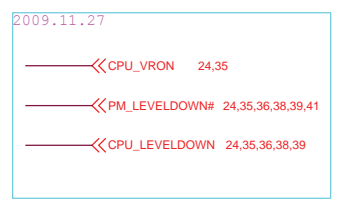
Size	Project Name	Rev
Custom	1015P	1.0

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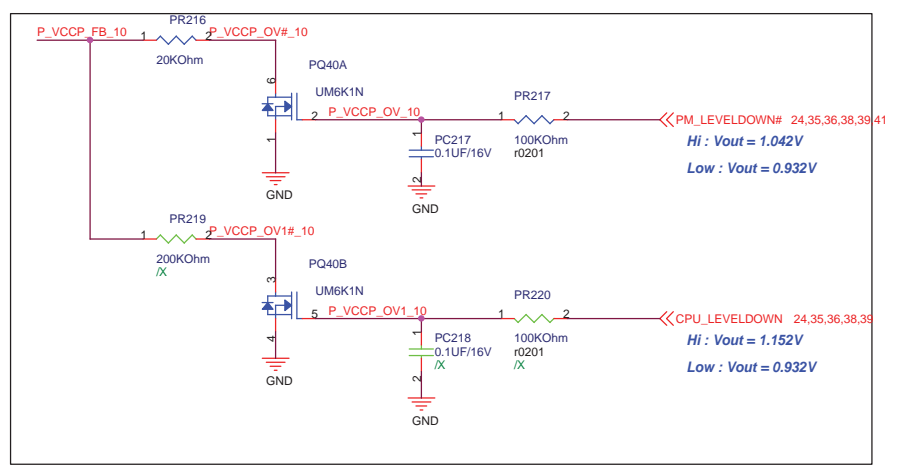


**Power Info.**

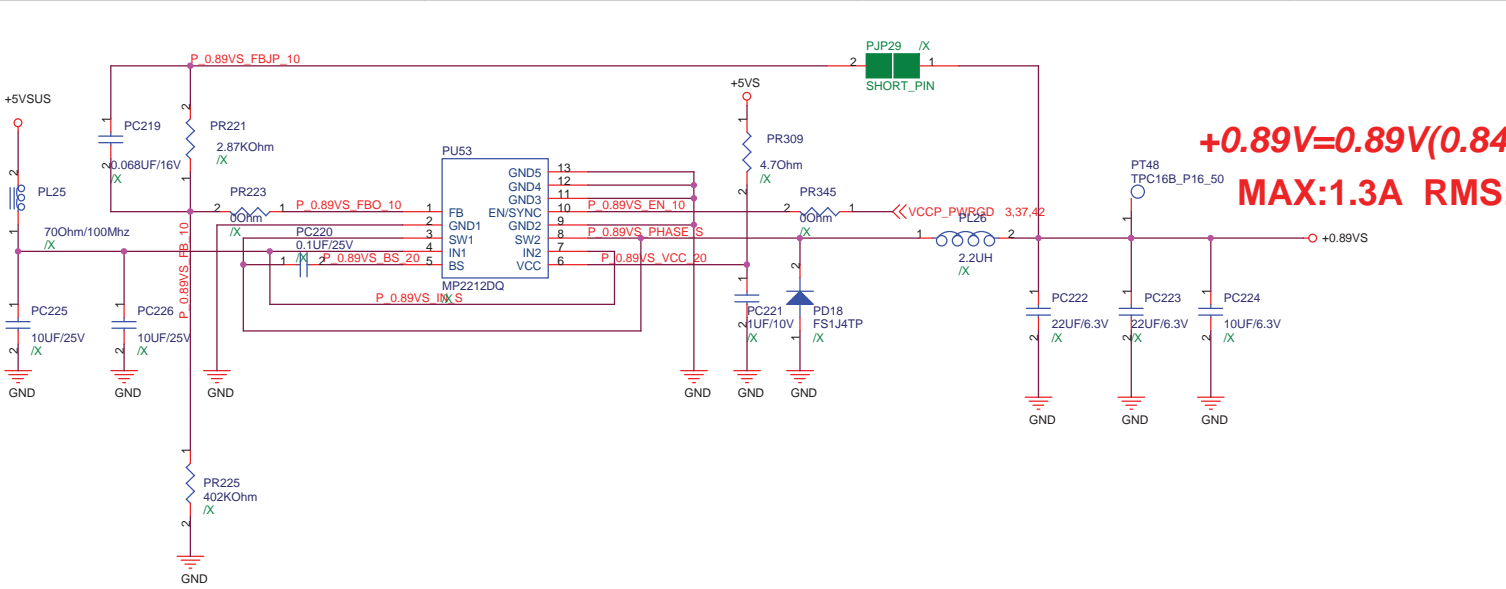
1. I/P Current:  
 $I_{in} = V_o * I_o / (0.8 * V_{in}) = 0.7A$
2. Ripple Current:  
 $I_{rip} = 1.08A$   
 $I_{spec} = 2.5A @ 1\%$
3. Frequency:  
 $F_{osc} = 600KHz$
4. Current Limit:  
**6A**



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.932V	Power Saving
H	L	H	1.042V	Normal
H	H	L	1.127V	Performance
L	H	L		N/A



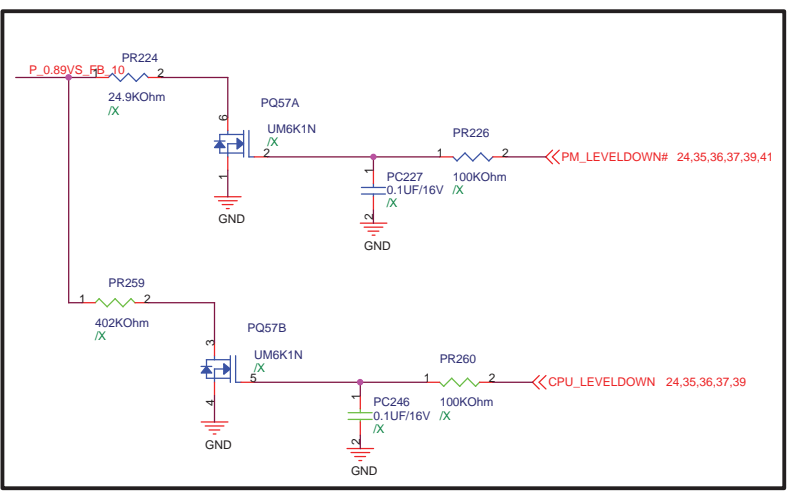
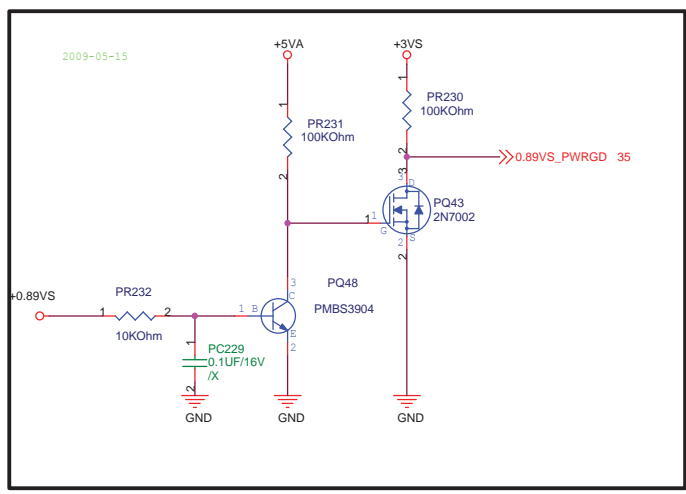
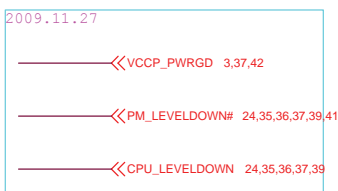




**+0.89V=0.89V(0.844V--0.95V)**  
**MAX:1.3A RMS:0.87A**

**Power Info.**

- I/P Current:**  
 $I_{in} = V_o * I_o / (0.8 * V_{in}) = 0.36A$
- Ripple Current:**  
 $I_{rip} = 0.61A$   
 $I_{spec} = 2.5A * 1pcs$
- Dynamic:**  
 $I_{peak} = 1.6A$   
 $ESR = 18\text{ mohm}$   
 $V = 28.8mV$
- Frequency:**  
 $F_{osc} = 600KHz$
- Current Limit:**  
**6A**



PM_LEVELDOWN#	CPU_LEVELDOWN	Voltage	Status
L	L	0.844V	Power Saving
H	L	0.897V	Normal
H	H	0.950V	Performance
L	H		N/A

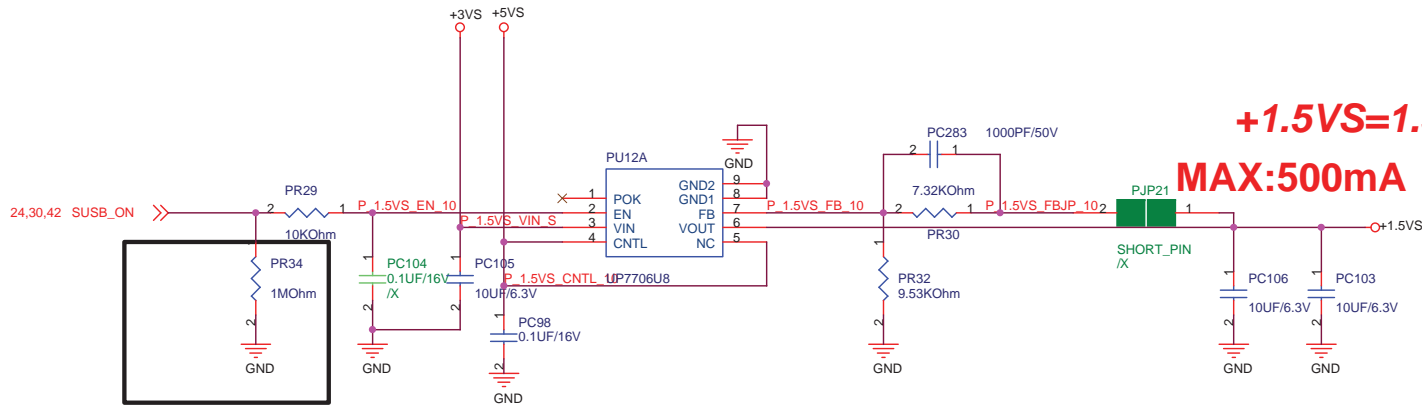
<Core Design>

**ASUS** Title : +1.5VS & +2.5VS

ASUSTek Computer INC Engineer: Joy\_Zhou

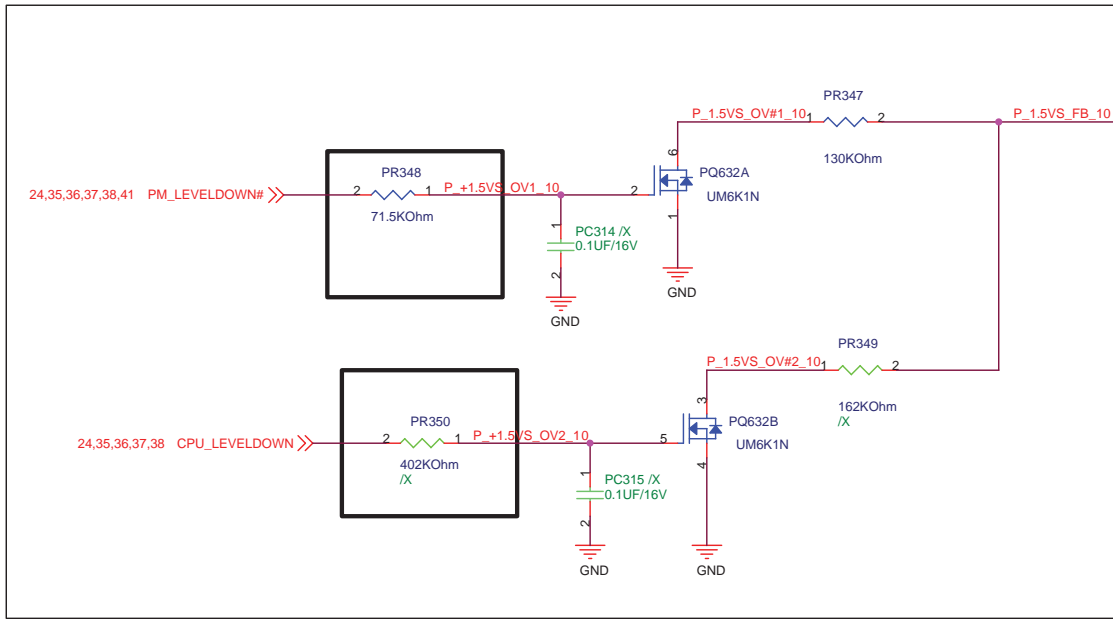
Size	Project Name	Rev
A3	1015P	1.0

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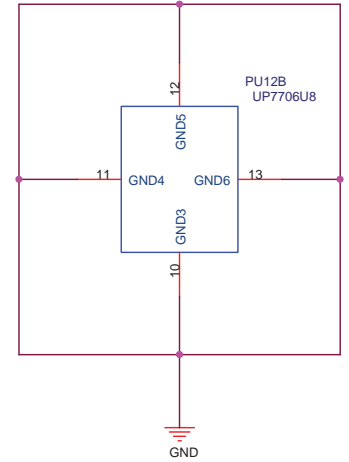


**+1.5VS=1.5V(1.44V--1.5V)**  
**MAX:500mA RMS:350mA**

- 1. Dropout Voltage:  
 $V = 300\text{ mV}$  ( $I_o = 2A$ )
- 2. Current Limit:  
 $I_{\text{limit}} = 2.8A$
- 3. Pd:  
 $R_{\text{thjc}} = 5\text{ C/W}$   
 $P_d = 1.9W$



2009.11.27  
 24,30,42 SUSB\_ON >>  
 24,35,36,37,38,41 PM\_LEVELDOWN# >>  
 24,35,36,37,38 CPU\_LEVELDOWN >>



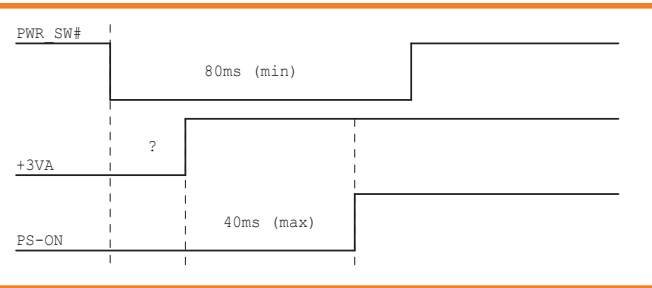
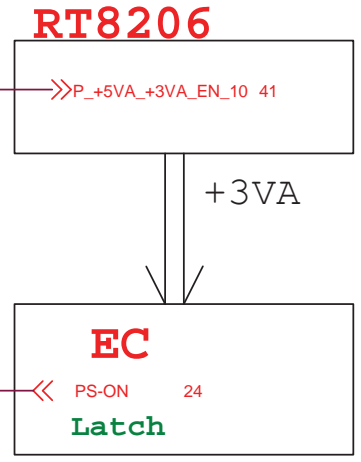
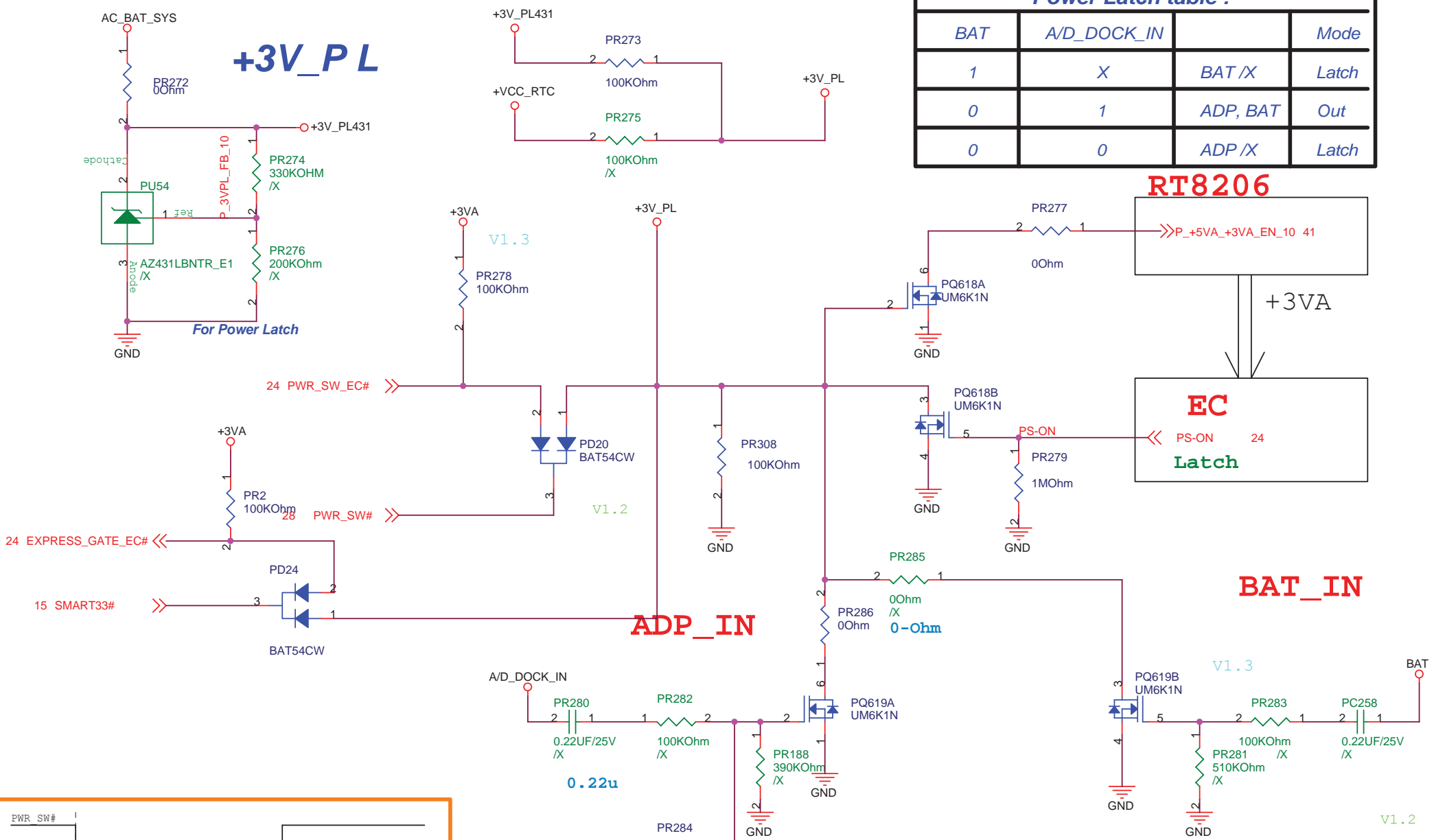
PM_LEVELDOWN#	CPU_LEVELDOWN	Voltage	Status
L	L	1.41V	Power Saving
H	L	1.49V	Normal
H	H	1.51V	Performance
L	H	1.50V	

<Core Design>

<b>ASUS</b>		<b>Title : +1.5VS &amp; +2.5VS</b>	
ASUSTek Computer INC		Engineer: <i>Joy_Zhou</i>	
Size B	Project Name <b>1015P</b>	Date: Saturday, February 06, 2010	Rev 1.0
		Sheet 39	of 42

**Power Latch table :**

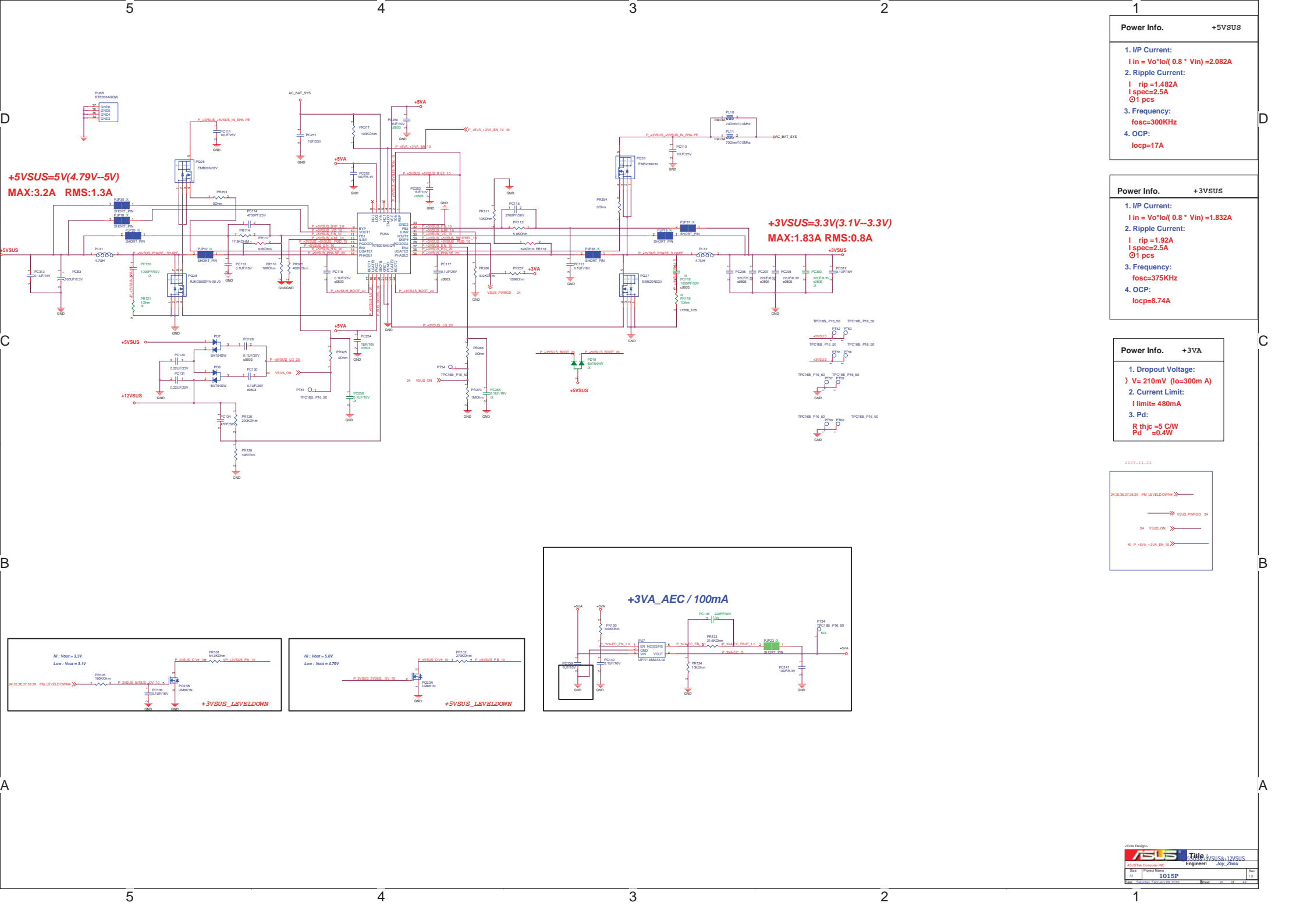
BAT	A/D_DOCK_IN		Mode
1	X	BAT /X	Latch
0	1	ADP, BAT	Out
0	0	ADP /X	Latch



V1.2 For ADP power latch

<Core Design>

<b>ASUS</b>		<b>Title : Power Latch</b>	
ASUSTek Computer INC.		Engineer: <i>River_Hsu</i>	
Size A4	Project Name <b>1015P</b>		Rev 1.0G
Date: Saturday, February 06, 2010		Sheet 40 of 42	



**Power Info. +5VSUS**

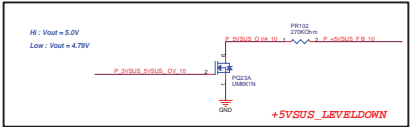
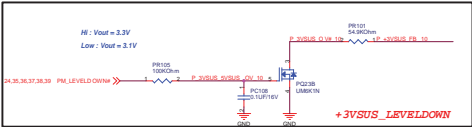
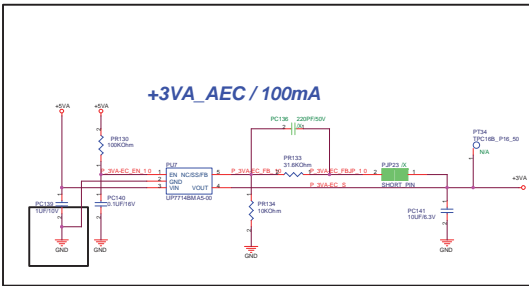
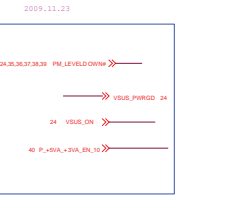
- I/P Current:**  
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 2.082A$
- Ripple Current:**  
 $I_{rip} = 1.482A$   
 $I_{spec} = 2.5A$   
 $\Delta t = 1 \mu s$
- Frequency:**  
 $f_{osc} = 300KHz$
- OCp:**  
 $I_{ocp} = 17A$

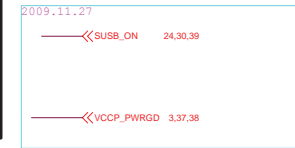
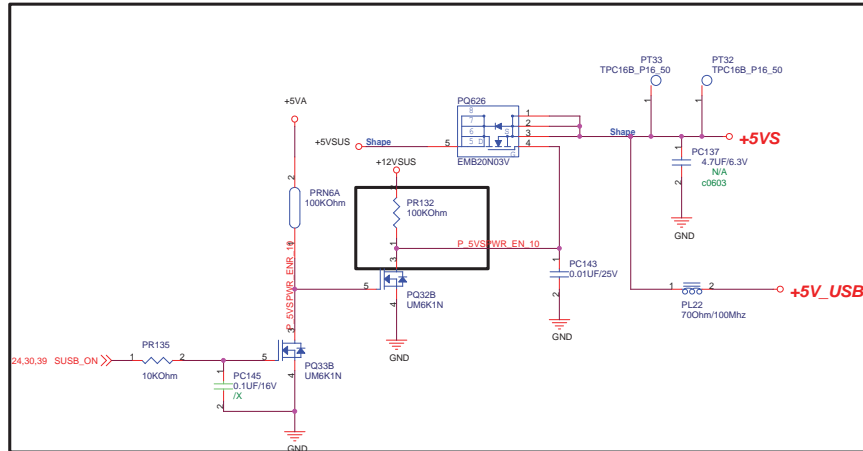
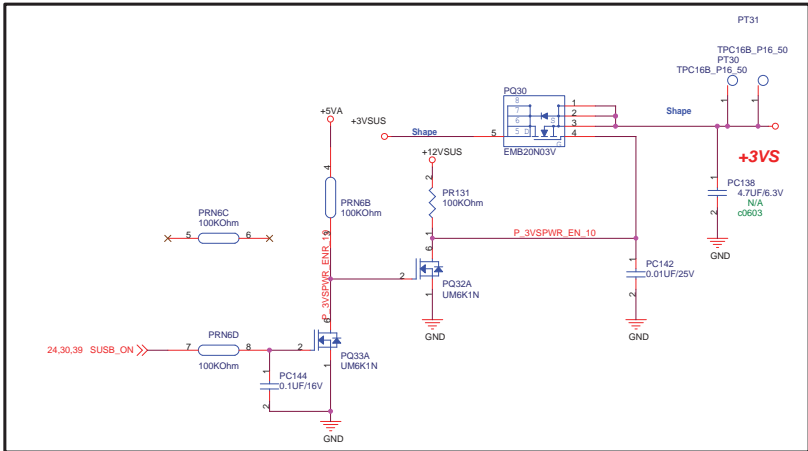
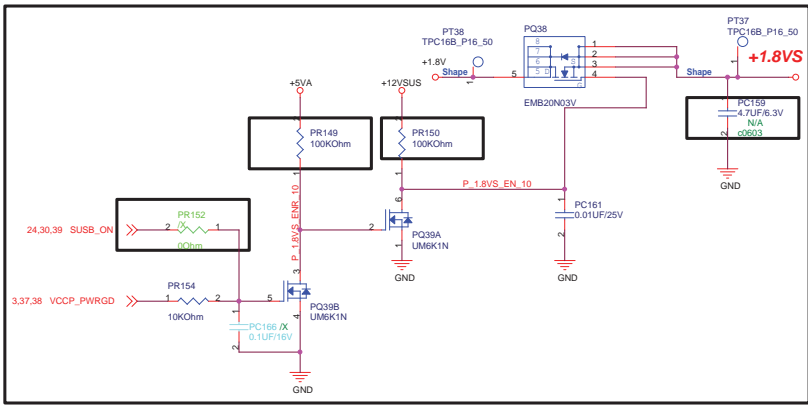
**Power Info. +3VSUS**

- I/P Current:**  
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.832A$
- Ripple Current:**  
 $I_{rip} = 1.92A$   
 $I_{spec} = 2.5A$   
 $\Delta t = 1 \mu s$
- Frequency:**  
 $f_{osc} = 375KHz$
- OCp:**  
 $I_{ocp} = 8.74A$

**Power Info. +3VA**

- Dropout Voltage:**  
 $V = 210mV (I_o = 300mA)$
- Current Limit:**  
 $I_{limit} = 480mA$
- Pd:**  
 $R_{thjc} = 5 \text{ } ^\circ C/W$   
 $P_d = 0.4W$





<Core Design>

		Title : load switch	
ASUSTek Computer INC		Engineer: Joy_Zhou	
Size	Project Name	Rev	
C	1015P	1.0	
Date: Saturday, February 06, 2010		Sheet 42 of 42	

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<http://radio-uchebnik.ru/txt/>

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