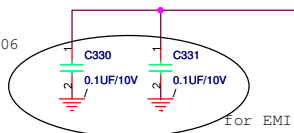
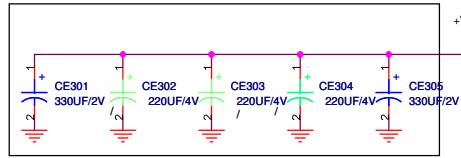
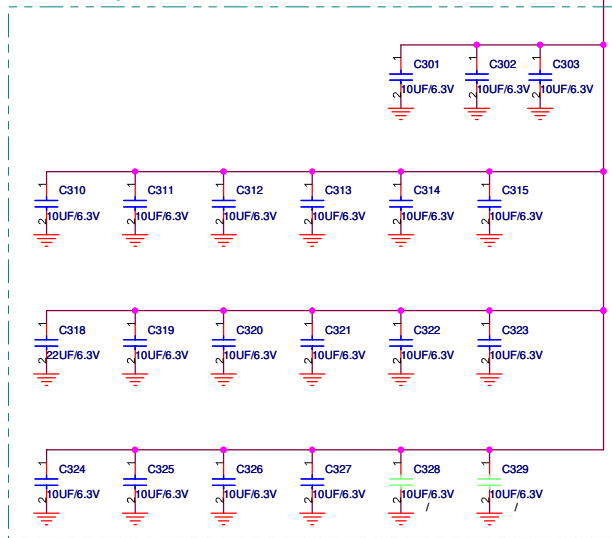


R1.1

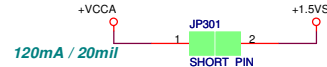
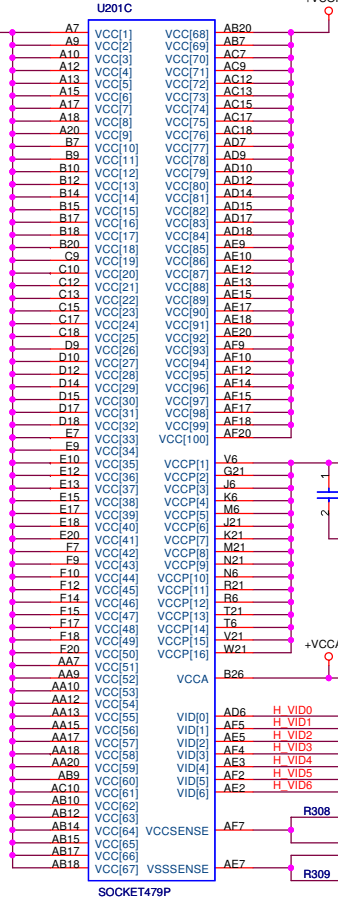


CPU +VCCORE
Mid-Frequency
Capacitors

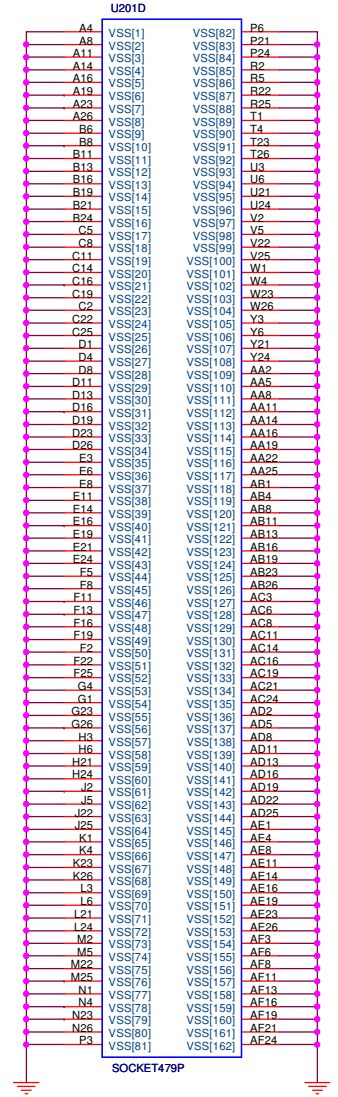
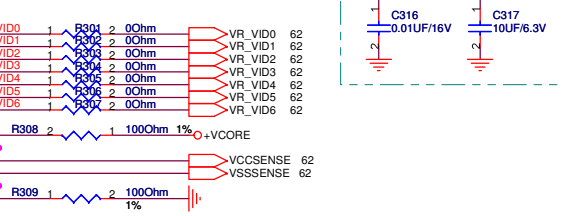


+VCCORE Low-Freq Capacitor

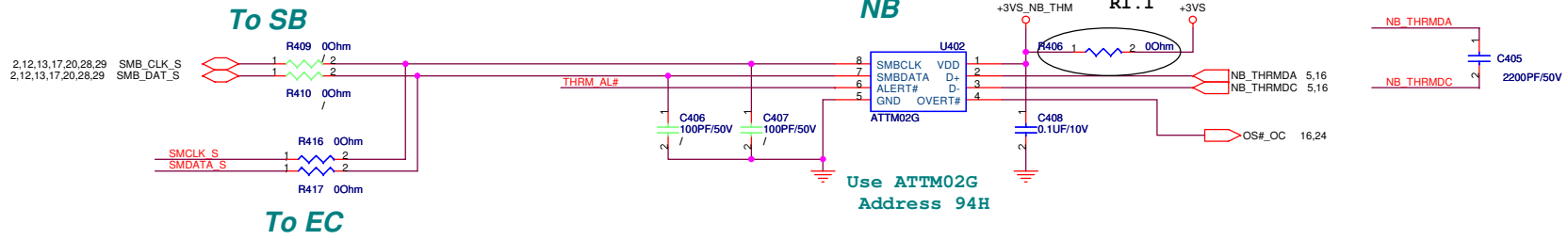
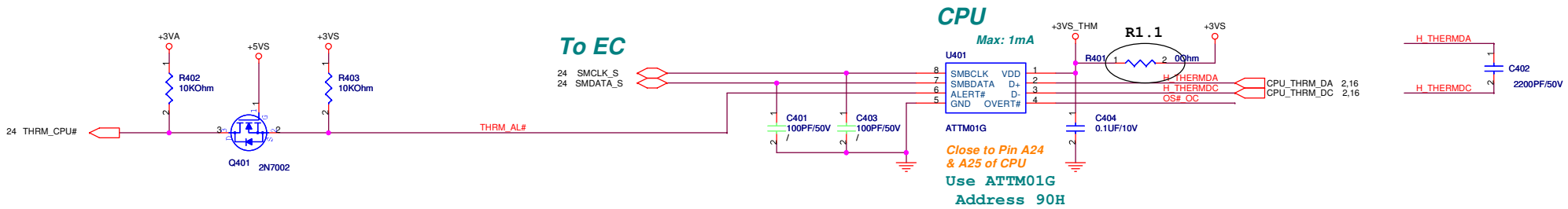
- Intel: 330UF *6
- ATI: 330UF *6
- R1F: 330UF *4
- A7J: 330UF *5
- F5X: 330UF *5
- +VCCORE Mid-Frequency Capacitor
- Intel: 22UF *32
- ATI: 10UF *26
- R1F: 22UF *16
- A7J: 22UF*29 use 19
- A6RF: 22UF*21 use 21
- F5X: 10UF *21 use 19
- +VCCP Decoupling Capacitor
- Intel: 270UF *1, 0.1UF *6
- R1F: 220UF *1, 0.1UF *4
- A7J: 220UF *1, 0.1UF *6
- A6RF: 220UF *1, 0.1UF *6
- F5X: 220UF *1, 0.1UF *6



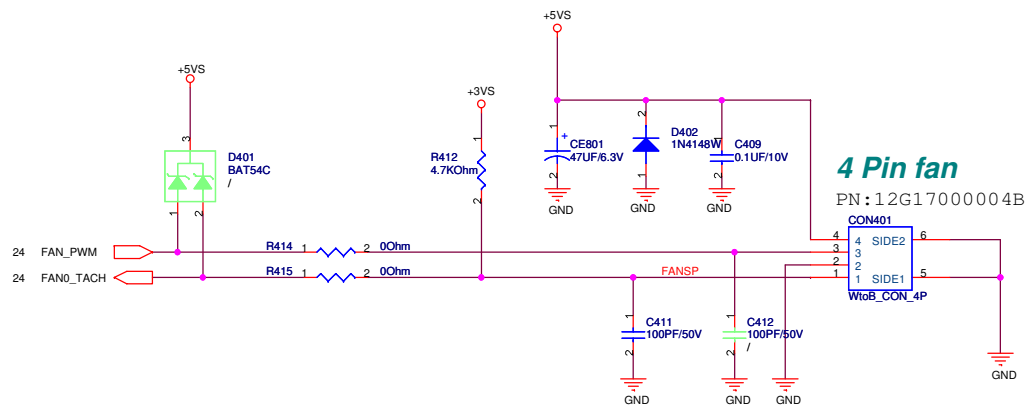
+VCCA
Decoupling
Capacitors



Thermal Sensor



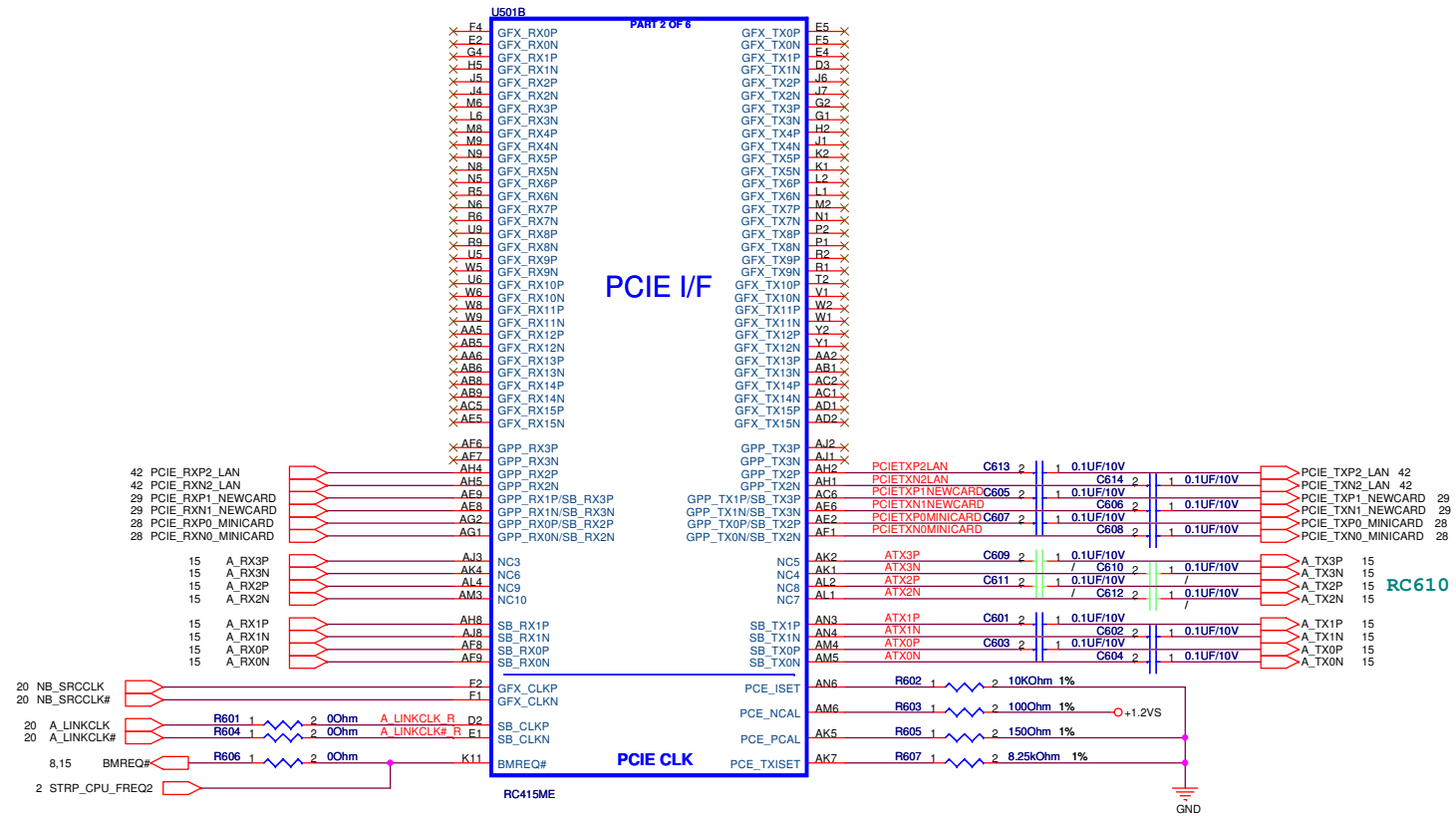
DC FAN Control

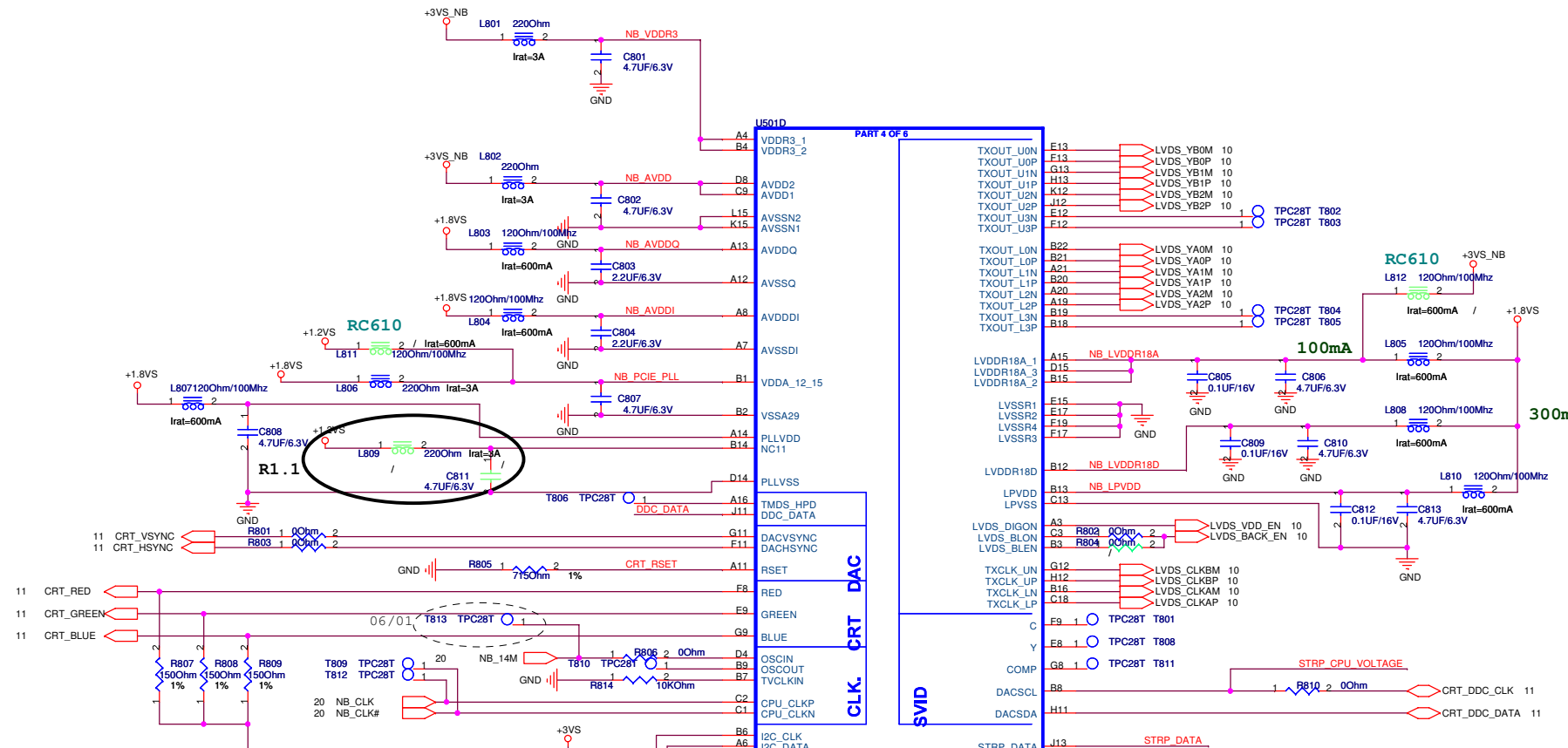


Route H_THERMDA and H_THERMDC on the same layer

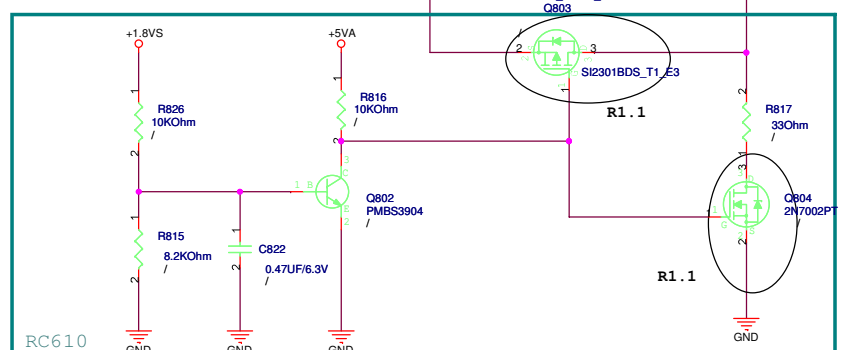
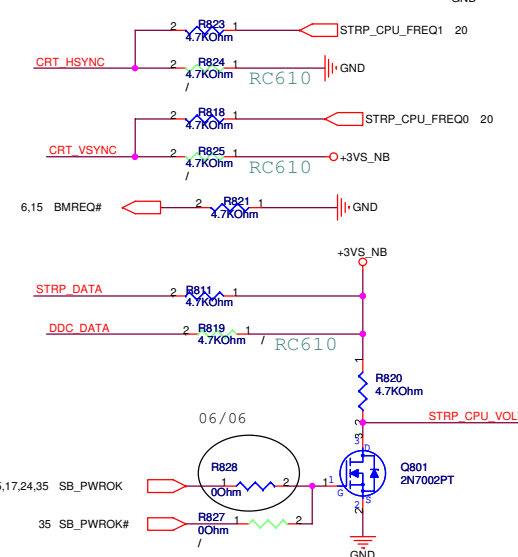
-----OTHER SIGNALS
15 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
15 mils
-----OTHER SIGNALS

Avoid FSB,Power





STRAPS

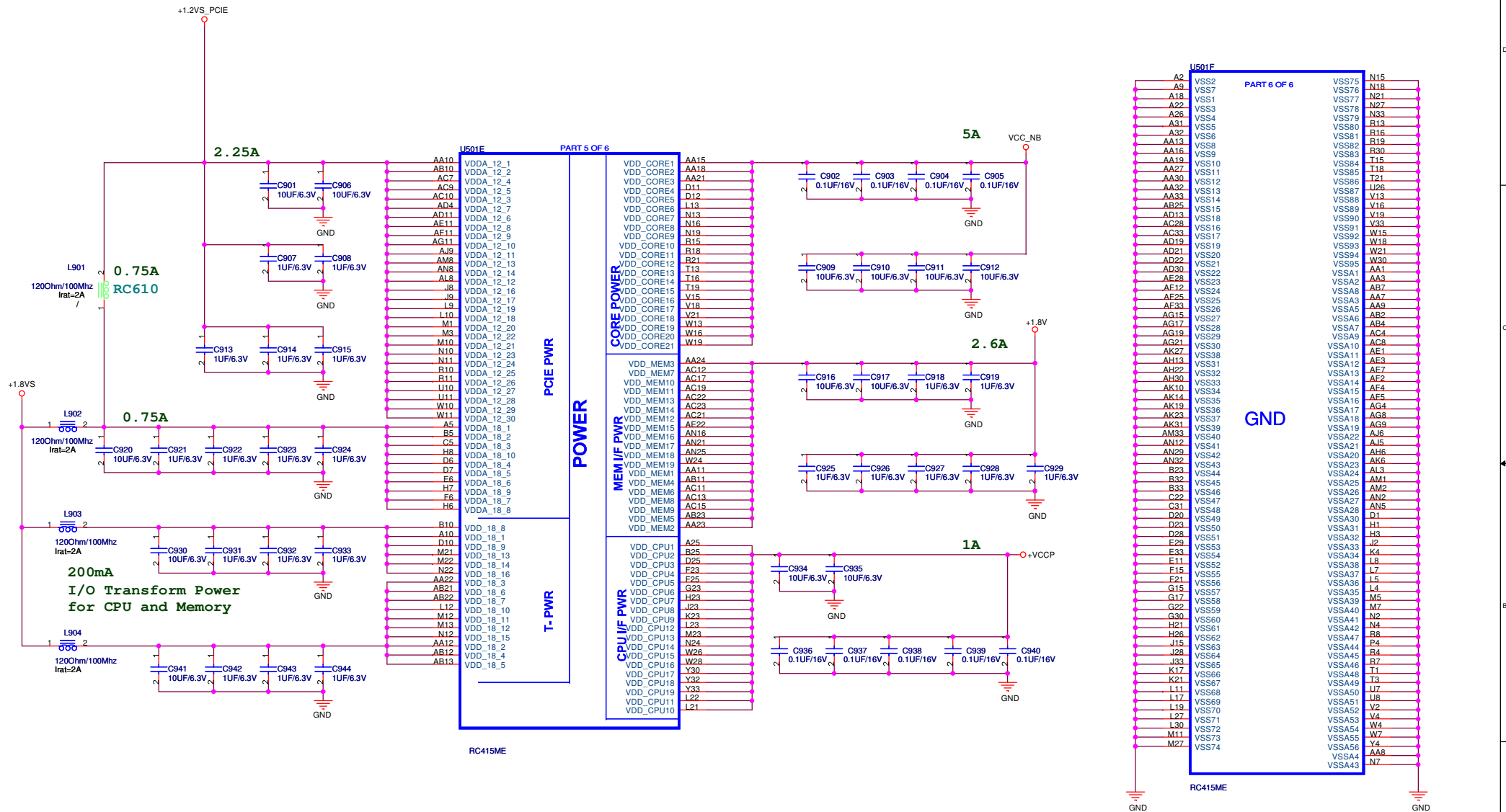


<Variant Name>

ASUS Title : **RC415M(4)**
 ASUSTeK COMPUTER INC Engineer: **Chris_Liu,Andy_guo**

Size	Project Name	Rev
Custom	F5R	2.0

Date: 星期三, 十月 11, 2006 Sheet 8 of 71



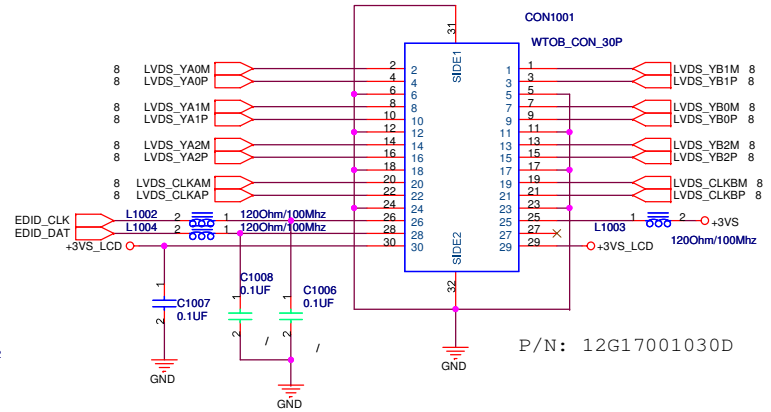
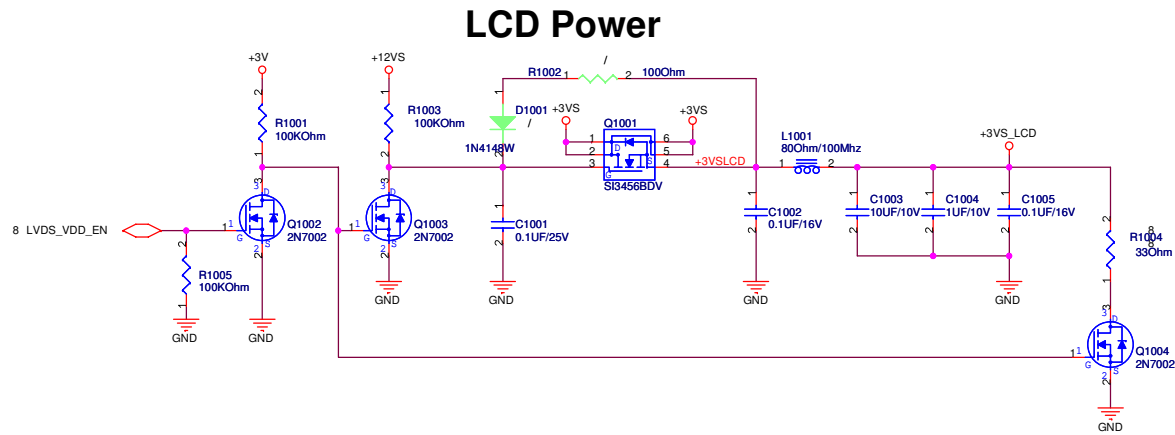
U501F

A2	VSS2	N15
A9	VSS7	N18
A18	VSS1	N21
A22	VSS3	N27
A26	VSS4	N33
A31	VSS5	R13
A32	VSS6	R16
AA13	VSS8	R19
AA16	VSS9	R30
AA19	VSS10	T15
AA27	VSS11	T18
AA30	VSS12	T21
AA32	VSS13	U26
AA33	VSS14	VSS8
AB05	VSS15	VSS89
AD13	VSS18	VSS90
AC28	VSS16	VSS91
AC33	VSS17	VSS92
AD19	VSS19	VSS93
AD21	VSS20	VSS94
AD22	VSS21	VSS95
AD30	VSS22	VSSA1
AE28	VSS23	VSSA2
AF12	VSS24	VSSA2
AE25	VSS25	VSSA8
AF33	VSS26	VSSA2
AG15	VSS27	VSSA6
AG17	VSS28	VSSA7
AG19	VSS29	VSSA9
AK21	VSS30	VSSA10
AK27	VSS31	VSSA11
AH13	VSS32	VSSA12
AH22	VSS33	VSSA13
AH30	VSS34	VSSA14
VSS35	VSS35	VSSA15
AK14	VSS36	VSSA16
AK19	VSS37	VSSA17
AK23	VSS38	VSSA18
AK31	VSS39	VSSA19
AM33	VSS40	VSSA22
AN12	VSS41	VSSA21
AN29	VSS42	VSSA20
AN32	VSS43	VSSA23
B23	VSS44	VSSA24
B32	VSS45	VSSA25
B33	VSS46	VSSA26
C22	VSS47	VSSA27
C31	VSS48	VSSA28
D20	VSS49	VSSA30
D23	VSS50	VSSA31
D28	VSS51	VSSA32
E29	VSS52	VSSA33
E33	VSS53	VSSA34
F11	VSS54	VSSA34
F15	VSS55	VSSA38
F21	VSS56	VSSA37
G15	VSS57	VSSA36
G17	VSS58	VSSA35
G22	VSS59	VSSA39
G30	VSS60	VSSA40
H21	VSS61	VSSA41
H26	VSS62	VSSA42
J15	VSS63	VSSA47
J28	VSS64	VSSA44
J33	VSS65	VSSA45
K17	VSS66	VSSA46
K21	VSS67	VSSA66
L11	VSS68	VSSA49
L17	VSS69	VSSA50
L19	VSS70	VSSA51
L27	VSS71	VSSA52
L30	VSS72	VSSA53
M11	VSS73	VSSA54
M27	VSS74	VSSA55
VSS75	VSS75	VSSA56
VSS76	VSS76	VSSA43
VSS77	VSS77	N7
VSS78	VSS78	AA8
VSS79	VSS79	Y4
VSS80	VSS80	W7
VSS81	VSS81	V4
VSS82	VSS82	V2
VSS83	VSS83	U8
VSS84	VSS84	T3
VSS85	VSS85	T1
VSS86	VSS86	B7
VSS87	VSS87	P4
VSS88	VSS88	R4
VSS89	VSS89	R8
VSS90	VSS90	N4
VSS91	VSS91	N2
VSS92	VSS92	M5
VSS93	VSS93	M7
VSS94	VSS94	L5
VSS95	VSS95	L7
VSS96	VSS96	L8
VSS97	VSS97	L4
VSS98	VSS98	M4
VSS99	VSS99	M5
VSS100	VSS100	M3
VSS101	VSS101	M2
VSS102	VSS102	AM1
VSS103	VSS103	AM2
VSS104	VSS104	AM3
VSS105	VSS105	AM4
VSS106	VSS106	AM5
VSS107	VSS107	AM6
VSS108	VSS108	AM7
VSS109	VSS109	AM8
VSS110	VSS110	AG9
VSS111	VSS111	AG4
VSS112	VSS112	AG8
VSS113	VSS113	AG4
VSS114	VSS114	AG4
VSS115	VSS115	AG4
VSS116	VSS116	AG4
VSS117	VSS117	AG4
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VSS119	VSS119	AG4
VSS120	VSS120	AG4
VSS121	VSS121	AG4
VSS122	VSS122	AG4
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VSS124	VSS124	AG4
VSS125	VSS125	AG4
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VSS190	VSS190	AG4
VSS191	VSS191	AG4
VSS192	VSS192	AG4
VSS193	VSS193	AG4
VSS194	VSS194	AG4
VSS195	VSS195	AG4
VSS196	VSS196	AG4
VSS197	VSS197	AG4
VSS198	VSS198	AG4
VSS199	VSS199	AG4
VSS200	VSS200	AG4

LCD Backlight Control

LCD LVDS Interface

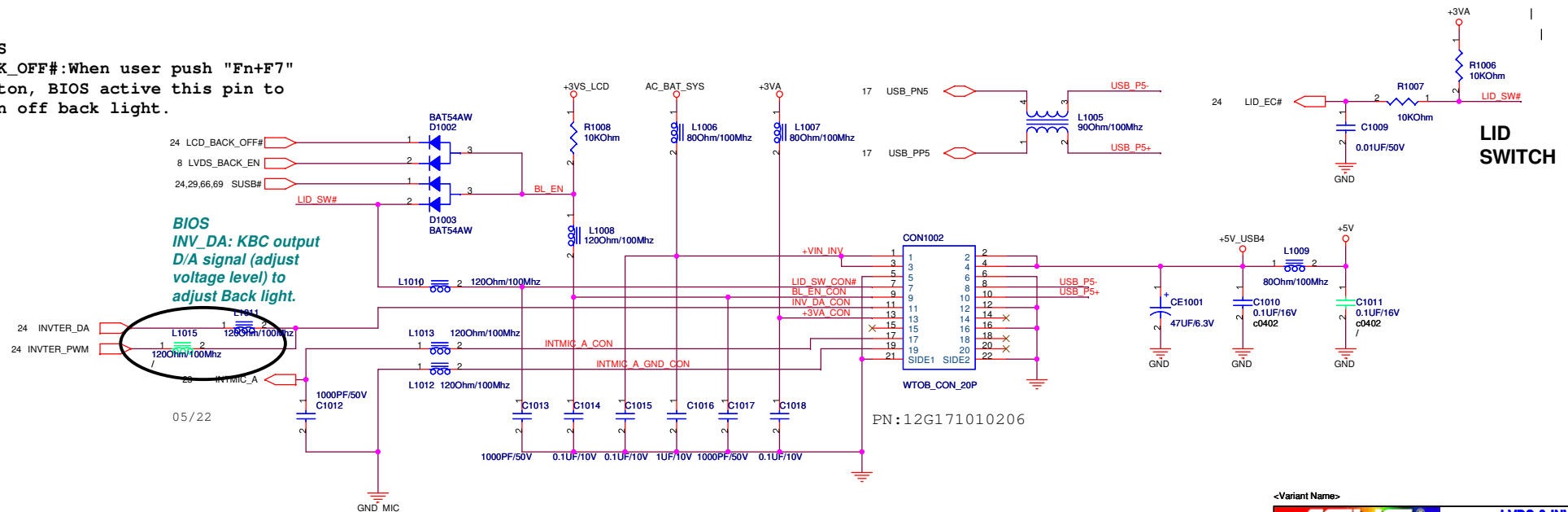
Cable Requirement:
 Impedence: 100 ohm +/- 10%
 Length Mismatch <= 10 mils
 Twisted Pair(Not Ribbon)
 Maximum Length <= 16"



INVERTER Interface

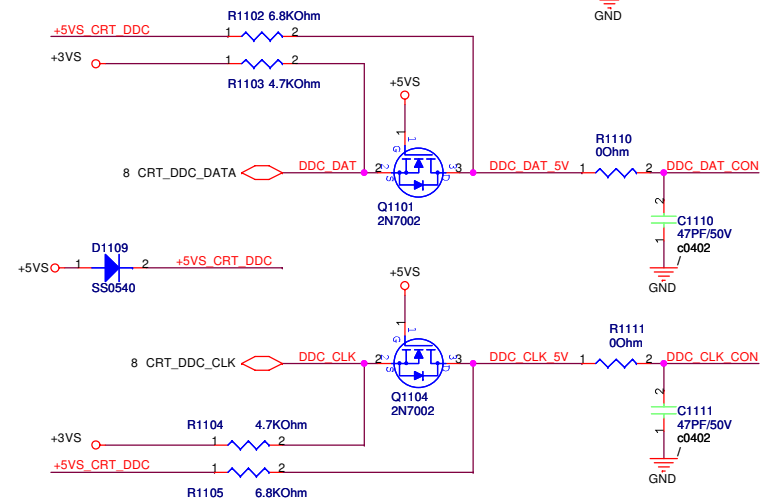
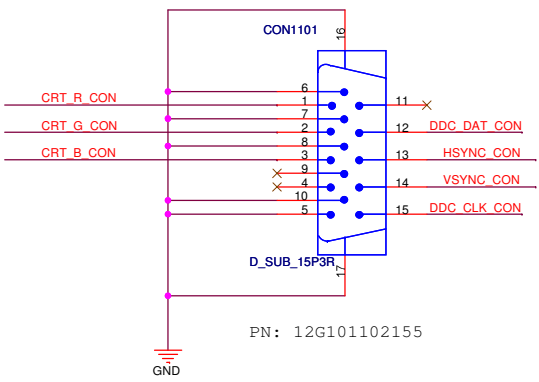
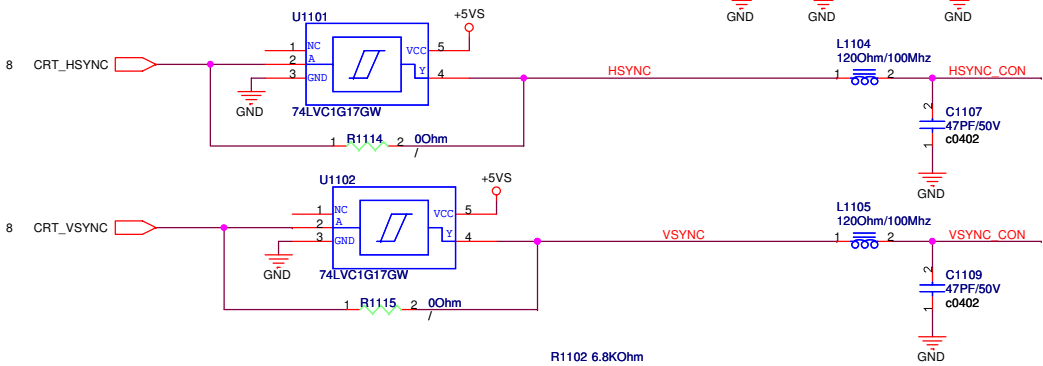
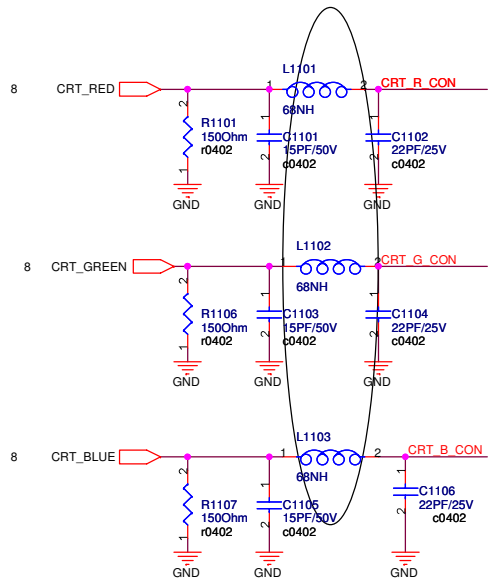
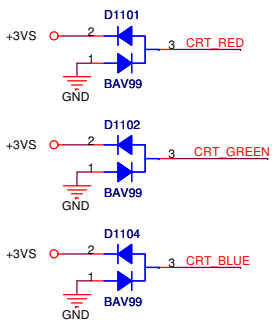
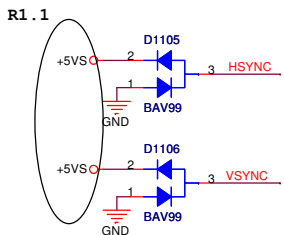
BIOS
BACK_OFF#: When user push "Fn+F7" button, BIOS active this pin to turn off back light.

BIOS
INV_DA: KBC output D/A signal (adjust voltage level) to adjust Back light.



ASUS Title : **LVDS & INVERTER**
 ASUSTeK COMPUTER INC Engineer: **Chris Liu, Andy Guo**
 Size Project Name
 Custom **F5R** Rev 2.0
 Date: 星期三, 十月 11, 2006 Sheet 10 of 71

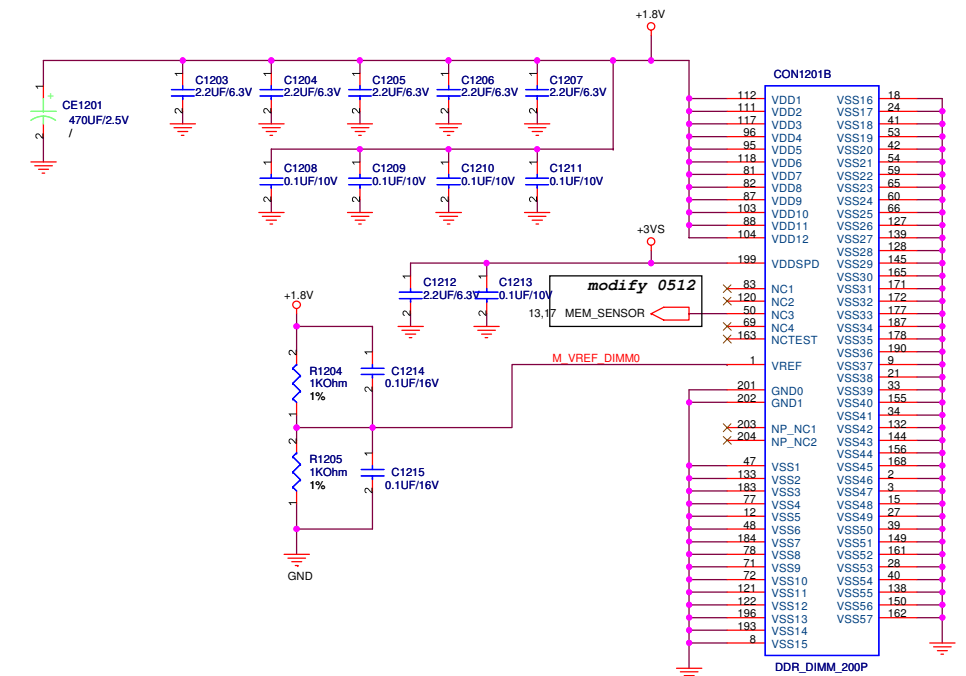
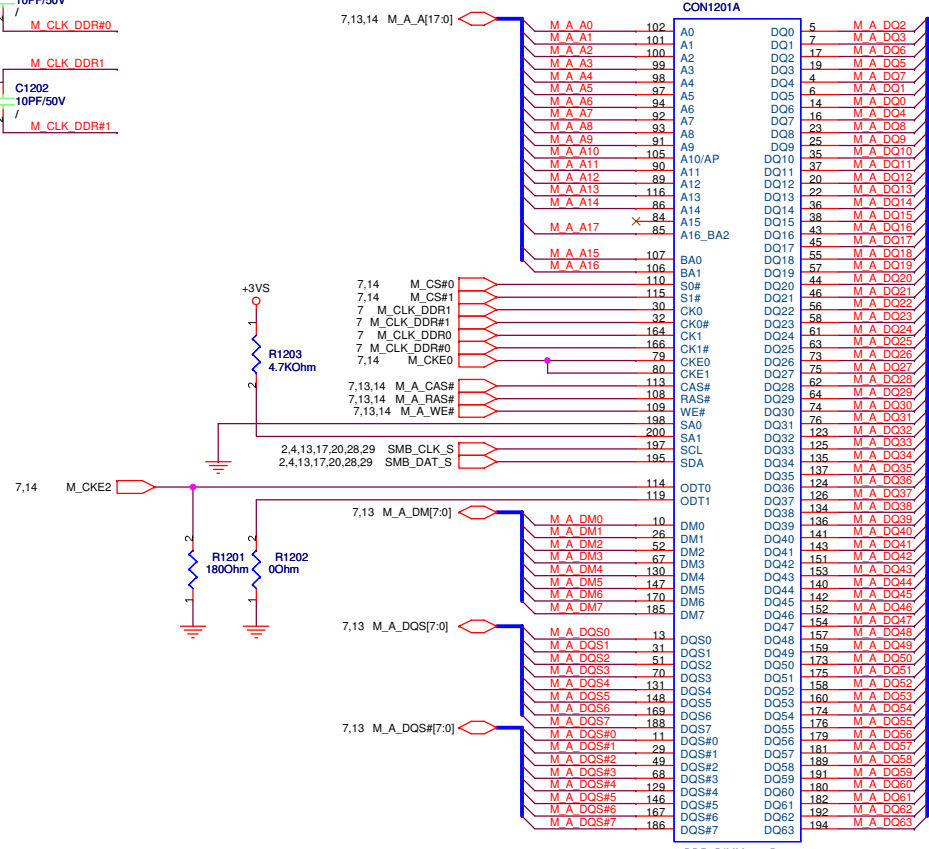
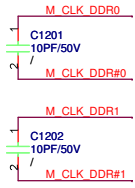
PLACE ESD Diodes near VGA port



<Variant Name>

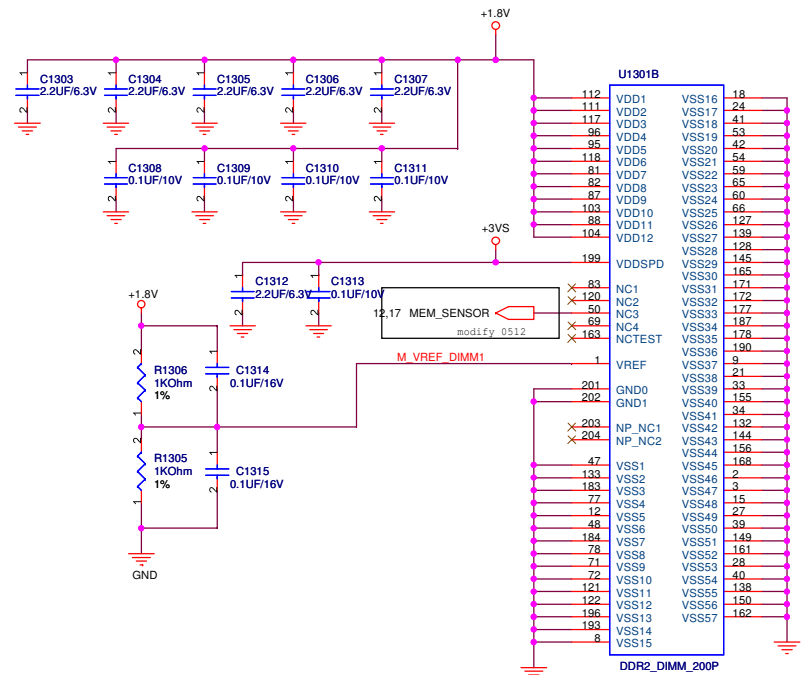
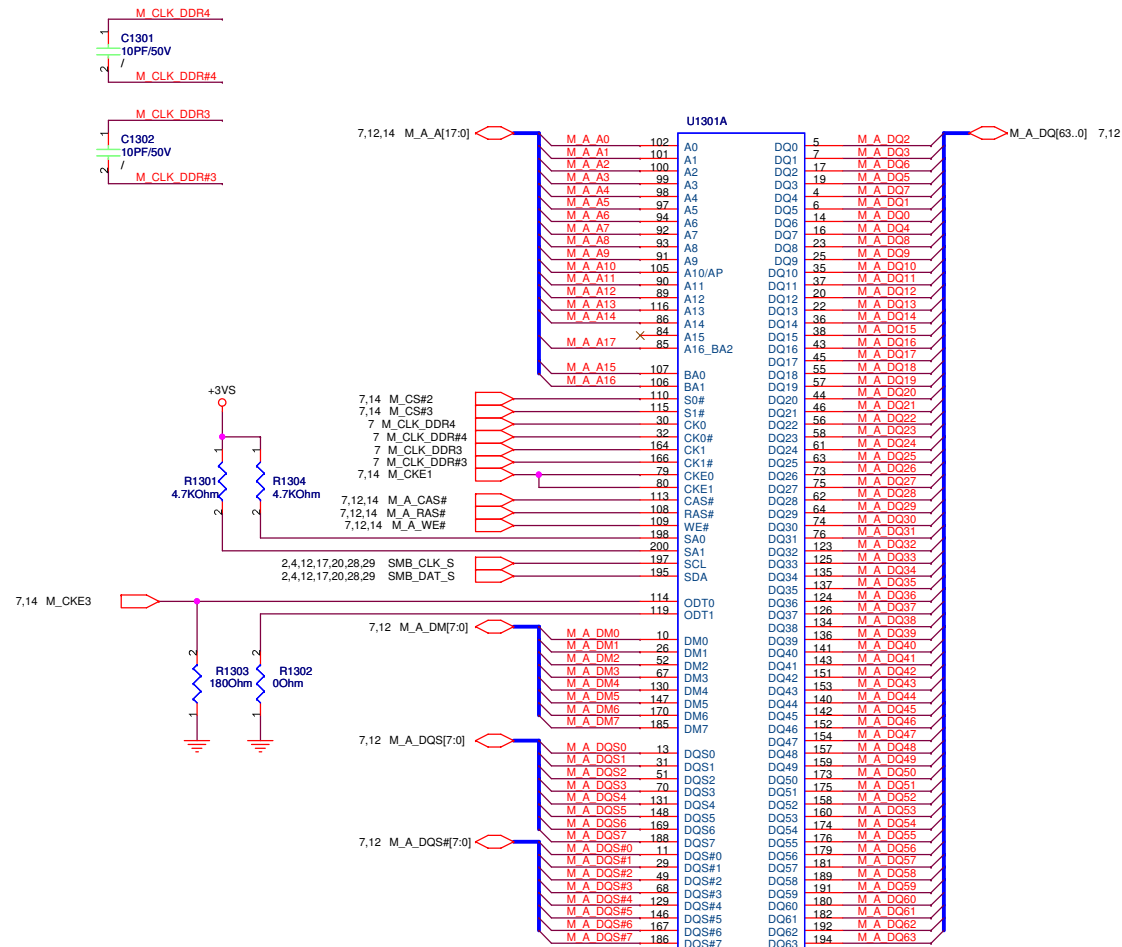
ASUS		Title : CRT	
ASUSTeK COMPUTER INC		Engineer: <i>Chris Liu, Andy Guo</i>	
Size	Project Name	Rev	2.0
Custom	F5R	Date:	星期三, 十月 11, 2006
Date: 星期三, 十月 11, 2006		Sheet	11 of 71

TOP



PN:12G025122006

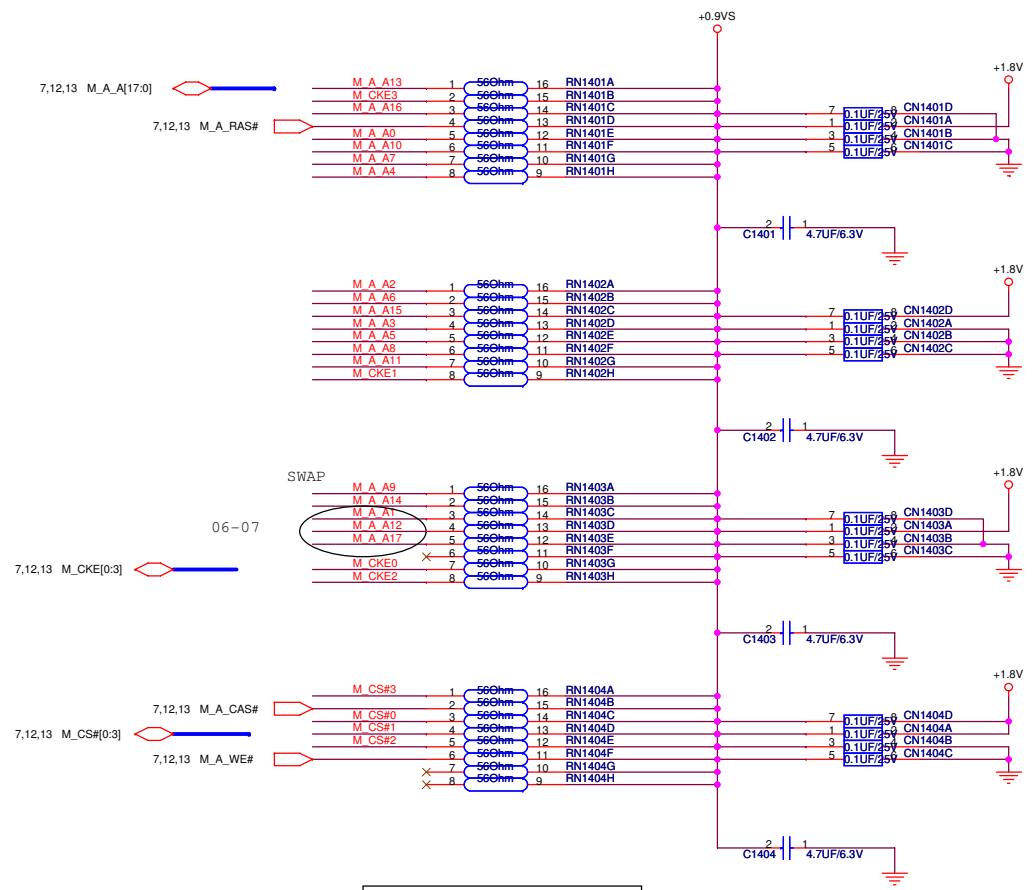
modify 05/24



PN:12G025C22002 REV.

<Variant Name>

		Title : DDR2 SO-DIMM	
ASUSTek COMPUTER INC		Engineer: Chris_Liu, Andy_Guo	
Size	Project Name		Rev
Custom	F5R		2.0
Date: 星期三, 十月 11, 2006	Sheet	13	of 71



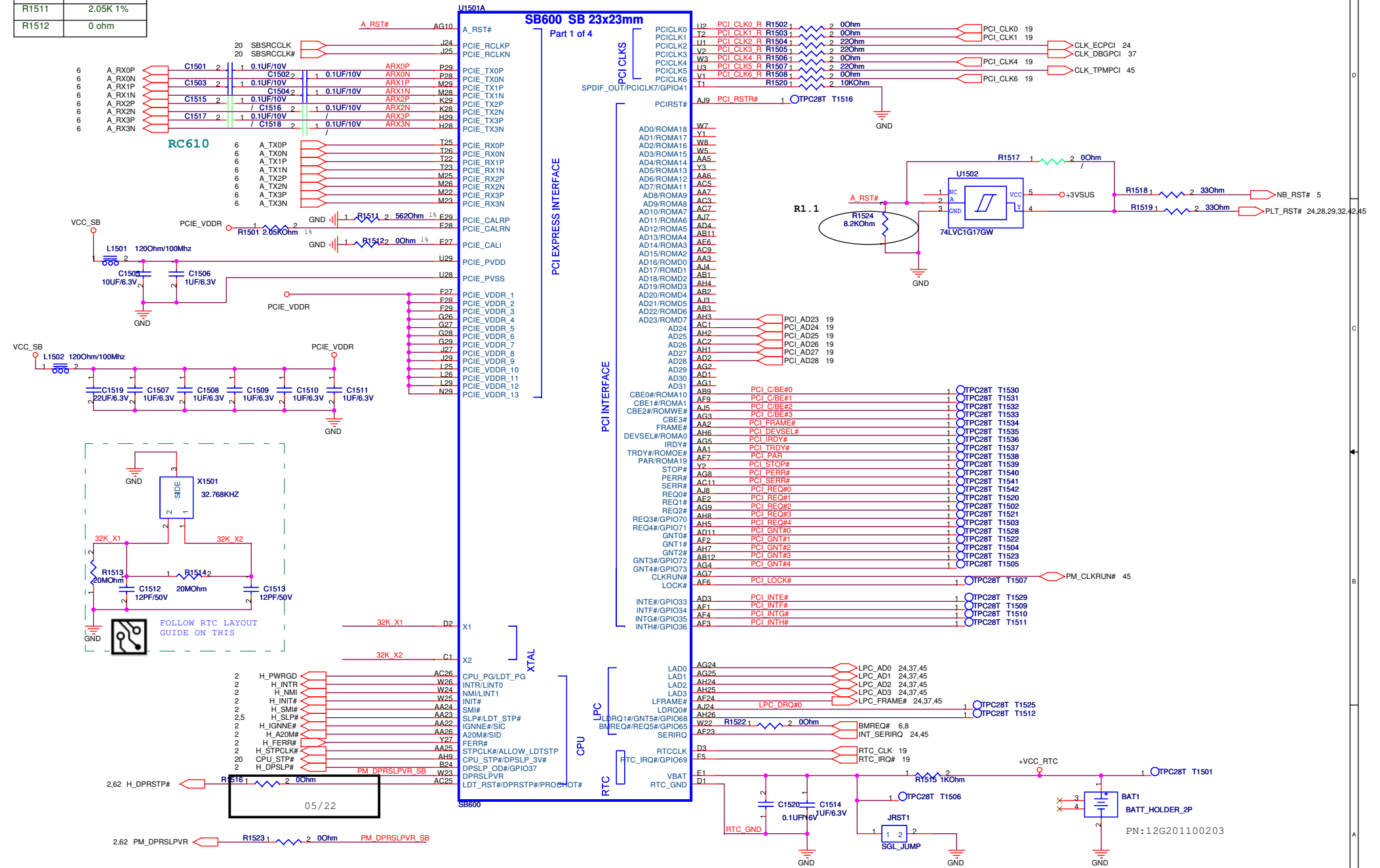
06-07

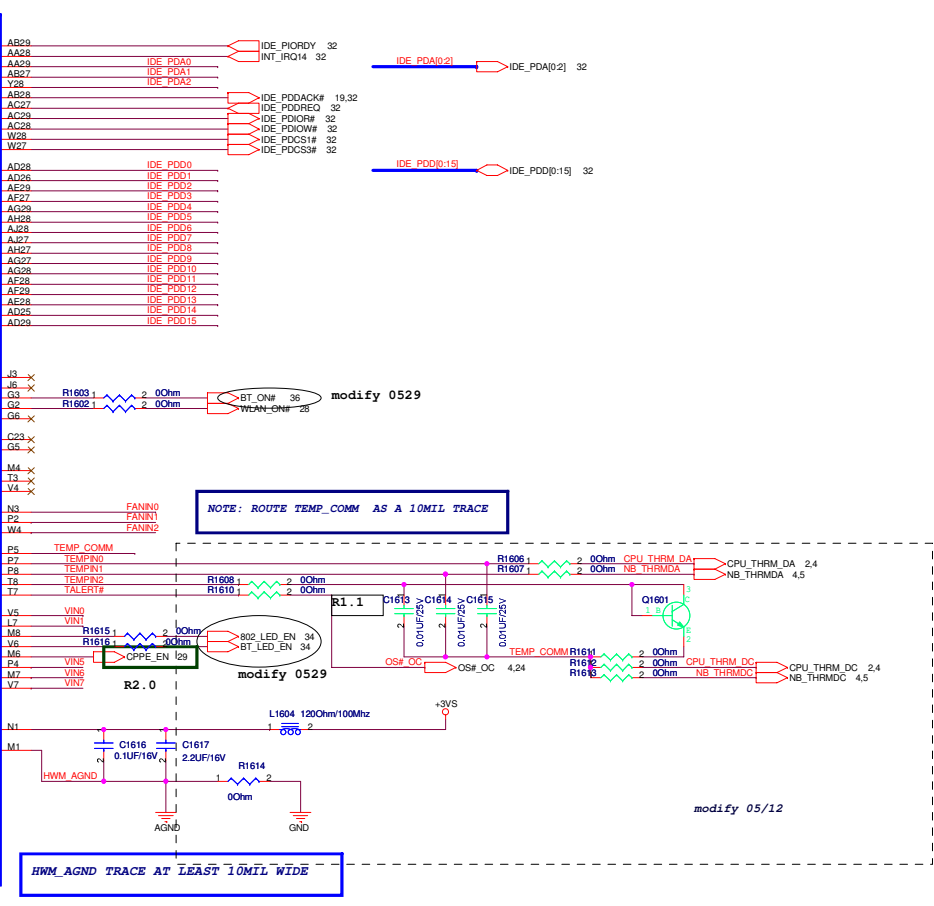
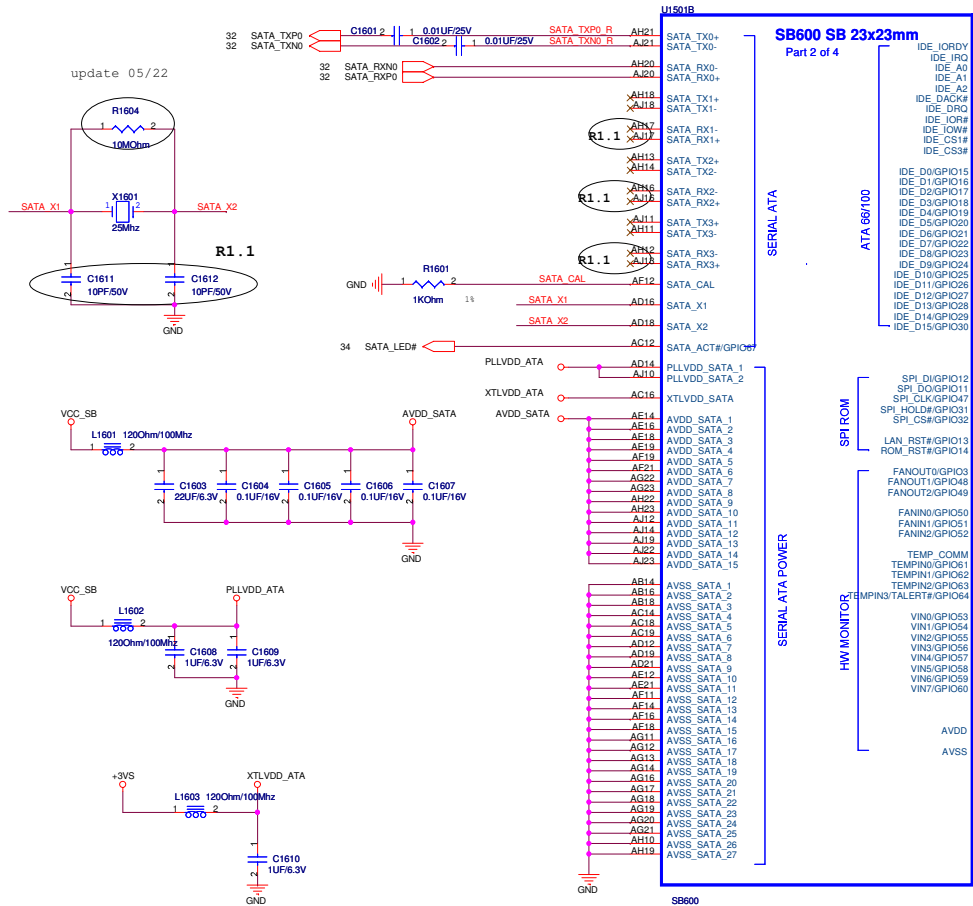
<Variant Name>

ASUS		Title : DDR2 TERMINATION
ASUSTeK COMPUTER INC		Engineer: <i>Chris_Liu,Andy_Guo</i>
Size	Project Name	Rev
Custom	F5R	2.0
Date: 星期三, 十月 11, 2006	Sheet	14 of 71

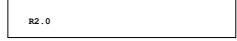
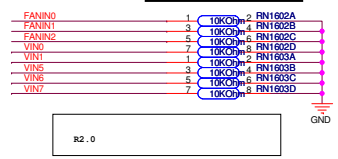
SB CALIBRATION RESISTOR VALUE

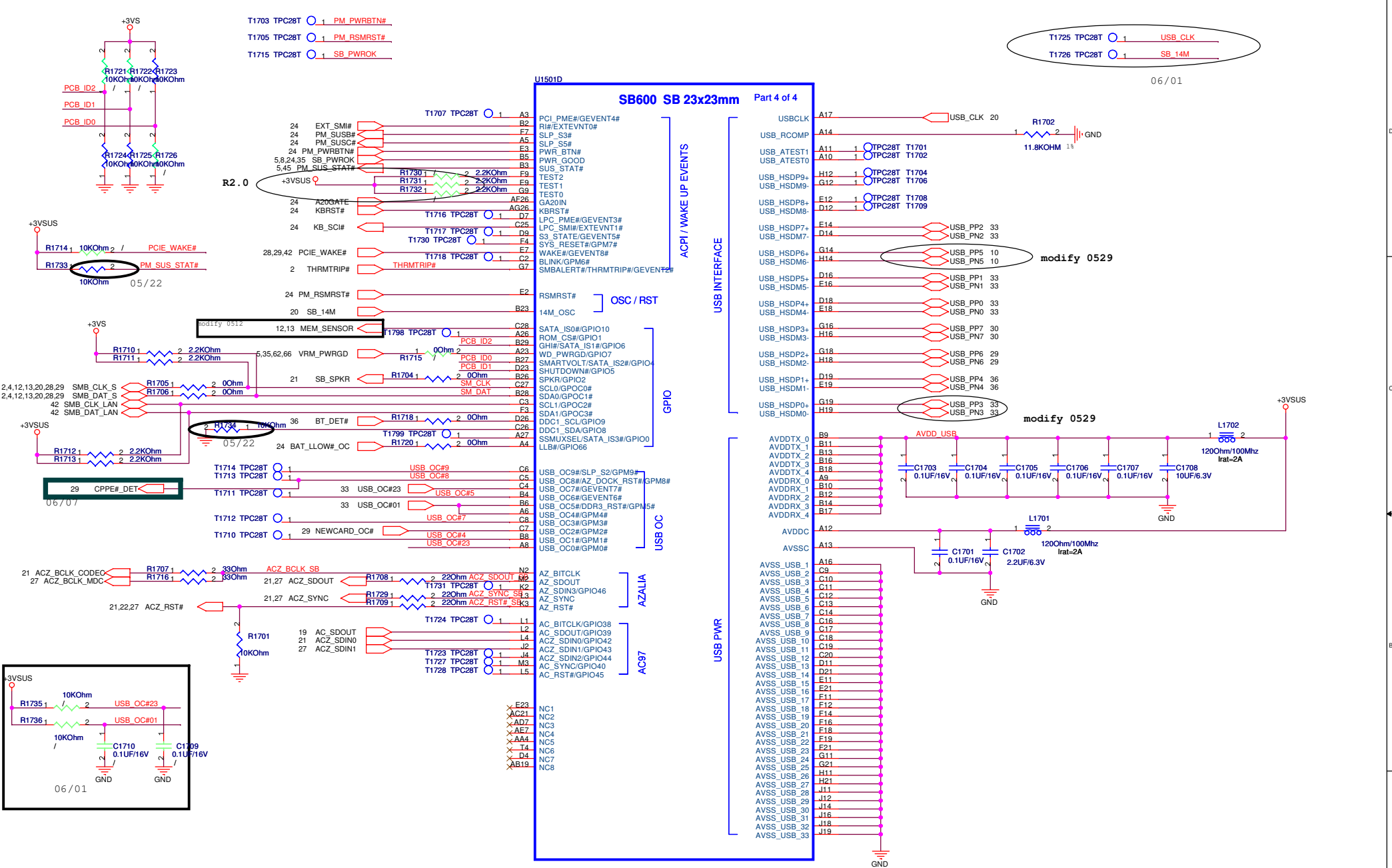
SB600	
R1501	562 OHM 1%
R1511	2.05K 1%
R1512	0 ohm

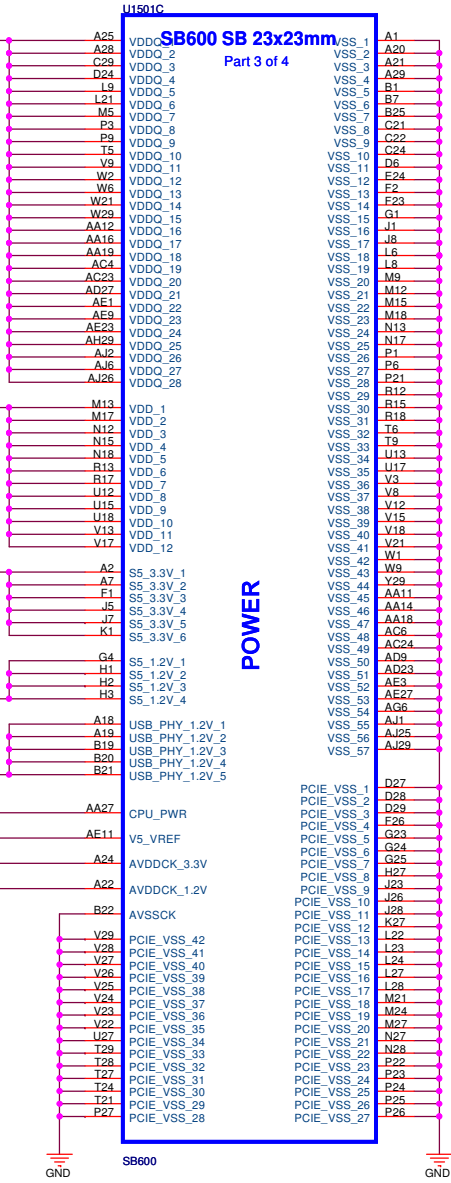
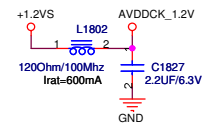
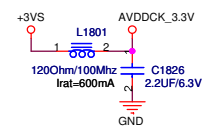
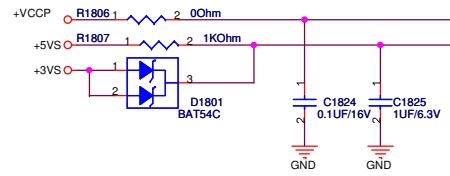
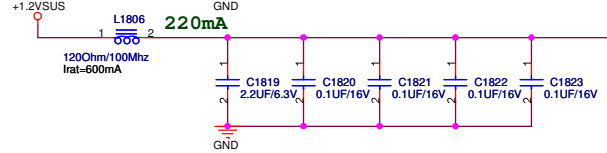
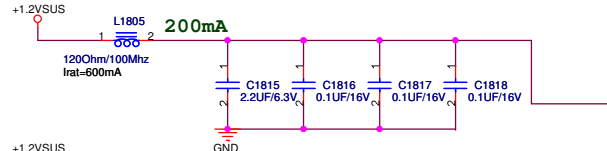
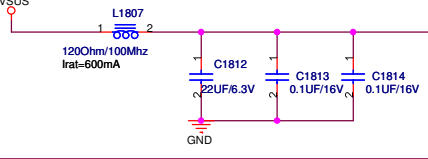
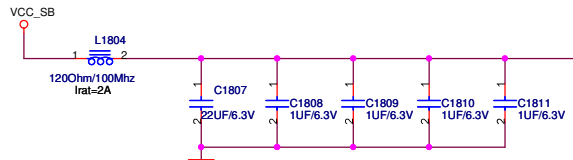
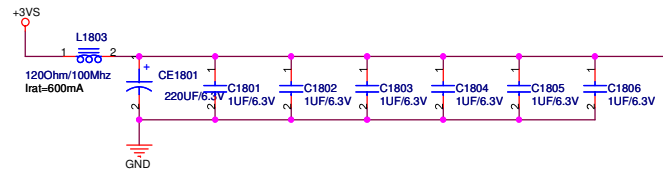
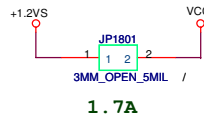




R1.1

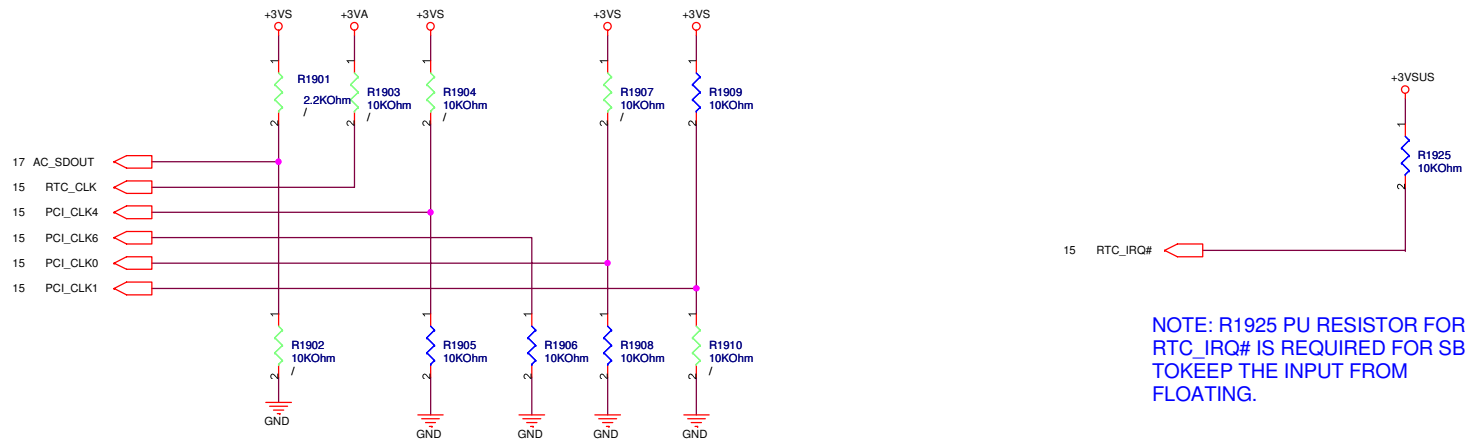






<Variant Name>

		Title : SB600(PWR)	
ASUSTeK COMPUTER INC		Engineer: Chris Liu, Andy Guo	
Size	Project Name		Rev
Custom	F5R		2.0
Date: 星期三, 十月 11, 2006		Sheet 18 of 71	



NOTE: R1925 PU RESISTOR FOR RTC_IRQ# IS REQUIRED FOR SB600 TO KEEP THE INPUT FROM FLOATING.

REQUIRED STRAPS

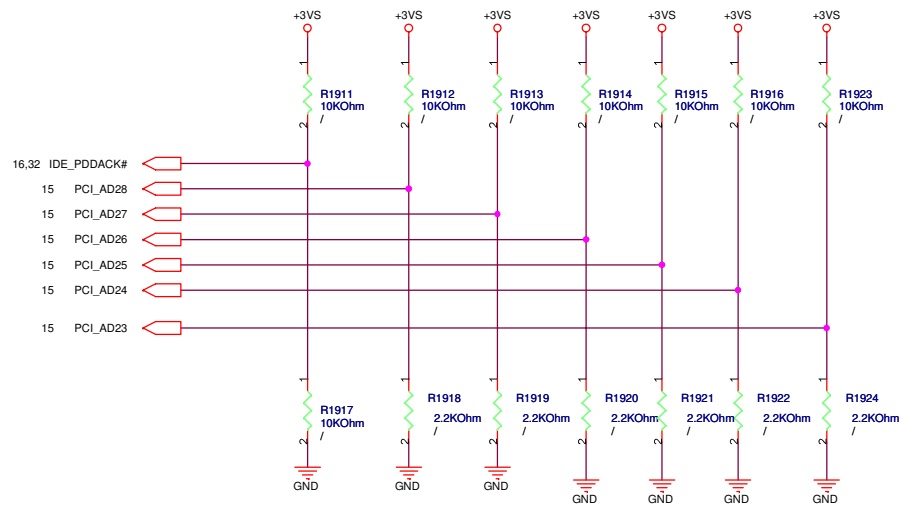
	SB600				SB460			
	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM		ROM TYPE: H, H = PCI ROM H, L = LPC I ROM L, H = LPC II ROM L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT			NOTE: FOR SB460, PCI_CLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCI_CLK[1:0]	

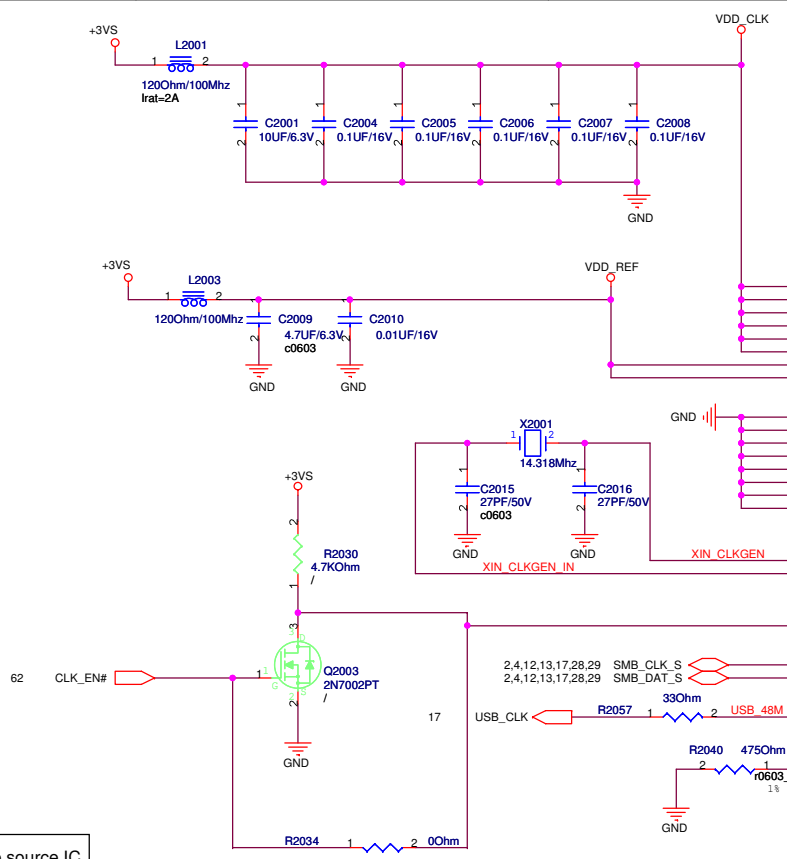
DEBUG STRAPS

	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SB460 ONLY SB600 ONLY

SB600 ONLY
NOTE: FOR SB460, PCI_AD23 IS RESERVED



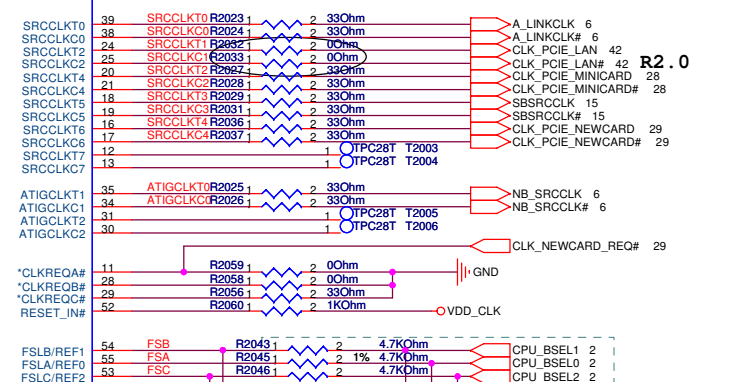
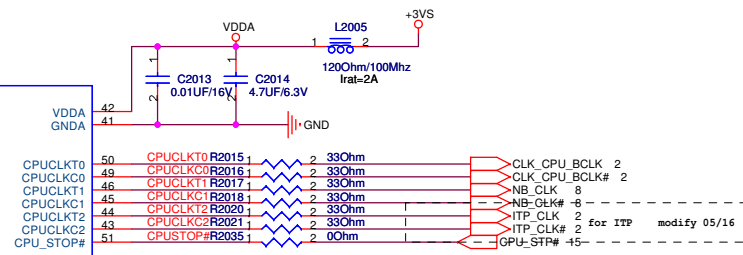
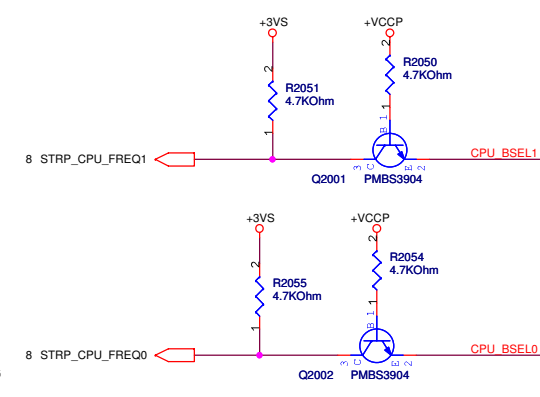


T2007
 O 1 CLK_EN#
 TPC28T

PLACE termination close to source IC

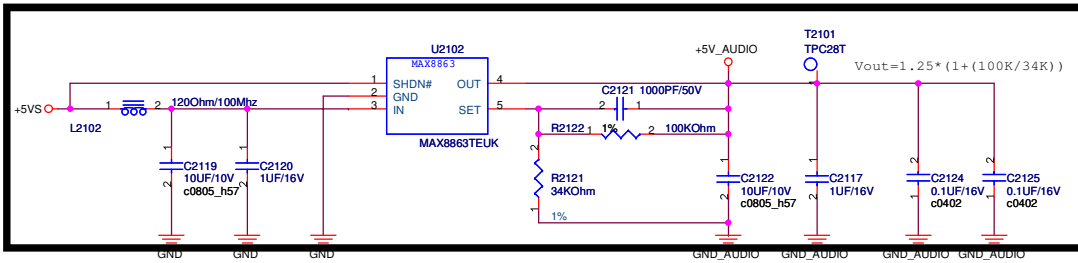
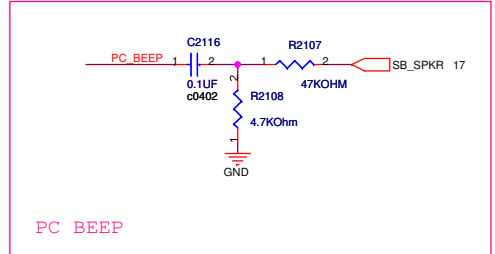
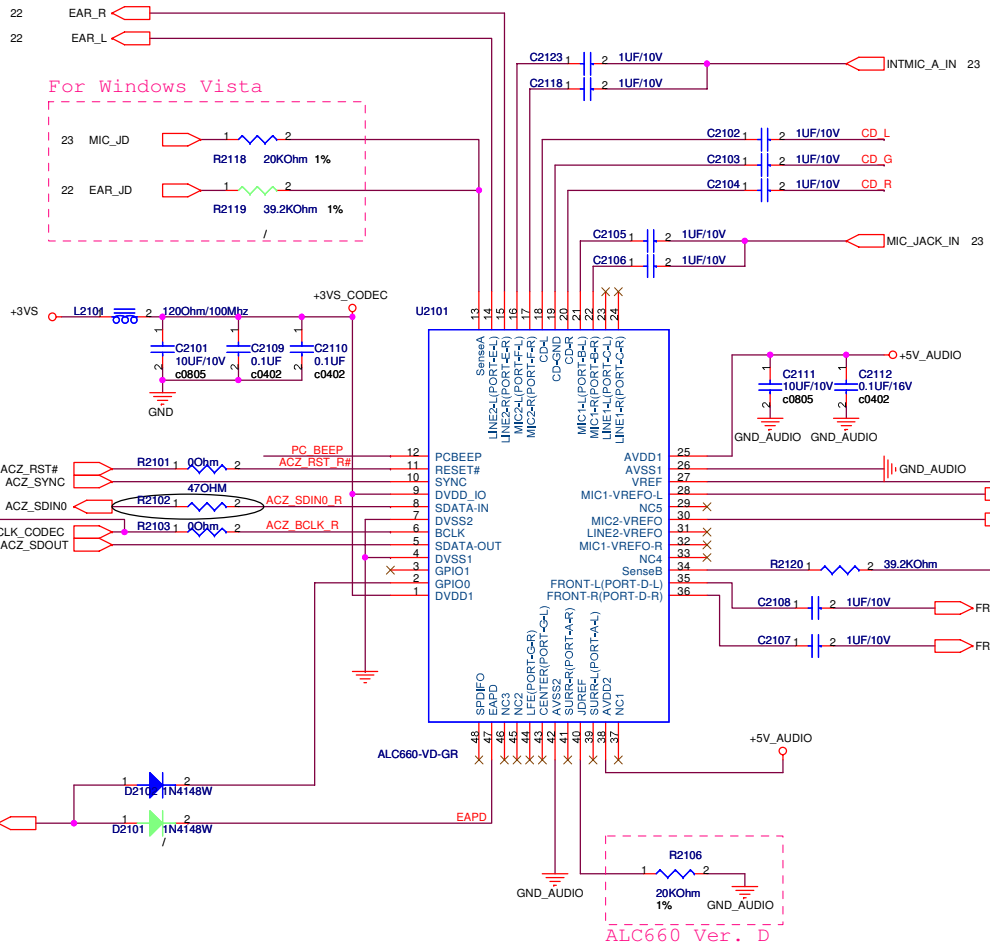
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- CLK_CPU_BCLK# R2002 1 2 49.9Ohm
- NB_CLK R2003 1 2 49.9Ohm
- NB_CLK# R2004 1 2 49.9Ohm
- A_LINKCLK R2005 1 2 49.9Ohm
- A_LINKCLK# R2006 1 2 49.9Ohm
- SBSRCLK R2007 1 2 49.9Ohm
- SBSRCLK# R2008 1 2 49.9Ohm
- CLK_PCIE_LAN R2009 1 2 100Ohm
- CLK_PCIE_LAN# R2010 1 2 100Ohm
- CLK_PCIE_MINICARD R2011 1 2 49.9Ohm
- CLK_PCIE_MINICARD# R2012 1 2 49.9Ohm
- CLK_PCIE_NEWCARD R2013 1 2 49.9Ohm
- CLK_PCIE_NEWCARD# R2014 1 2 49.9Ohm
- ITP_CLK R2062 1 2 49.9Ohm for ITP modify 05/15
- ITP_CLK# R2063 1 2 49.9Ohm
- NB_SRCLK R2019 1 2 49.9Ohm
- NB_SRCLK# R2022 1 2 49.9Ohm

R2.0

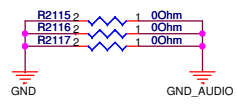
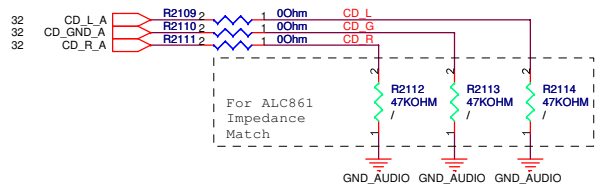


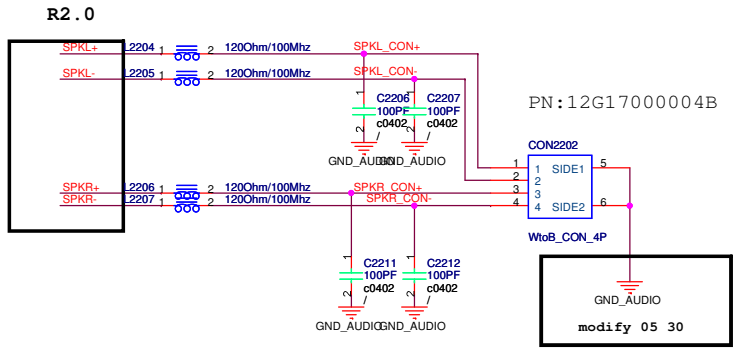
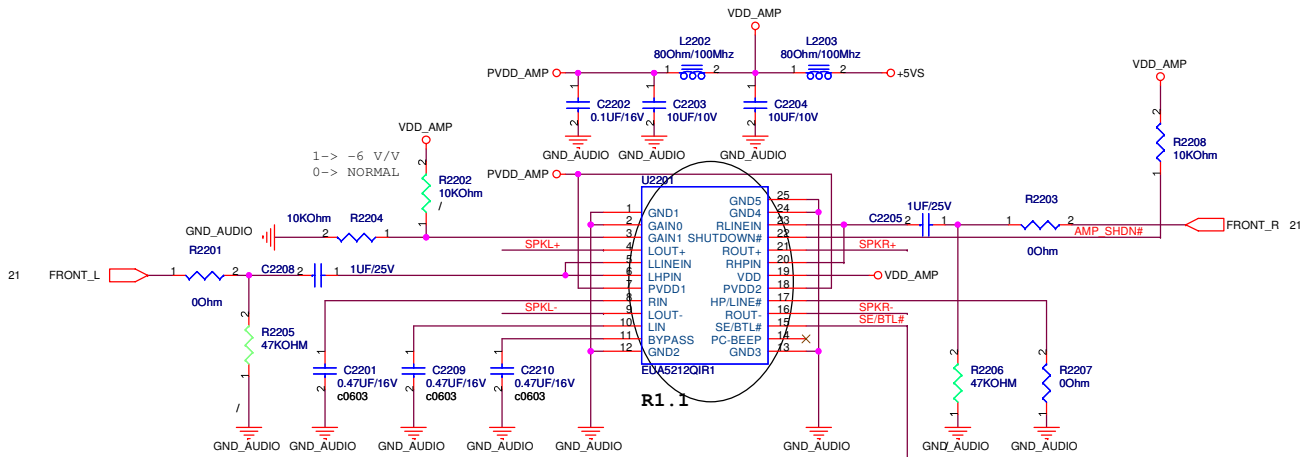
BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

ASUS Title :CLOCK GENERATOR
 ASUSTek COMPUTER INC Engineer: Chris_Liu,Andy_Guo
 Size Project Name Rev 2.0
 Custom F5R
 Date: 星期三, 十月 11, 2006 Sheet 20 of 71

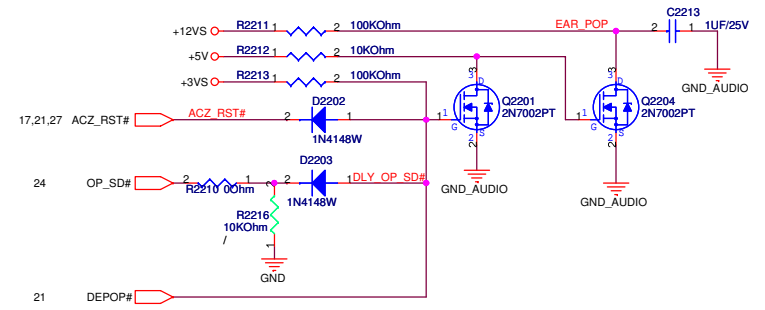
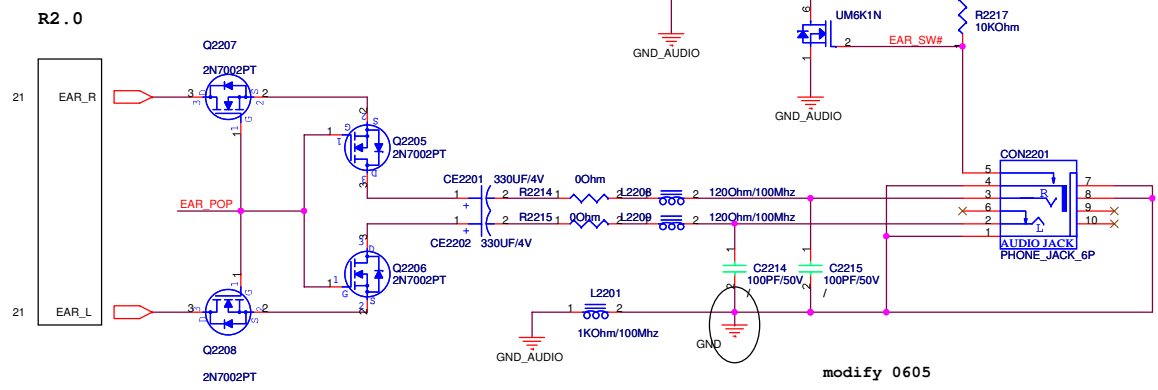
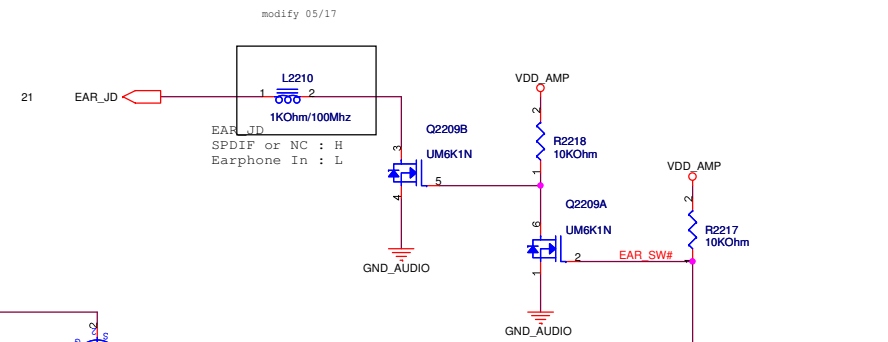
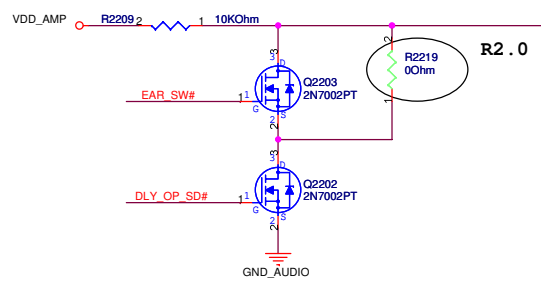


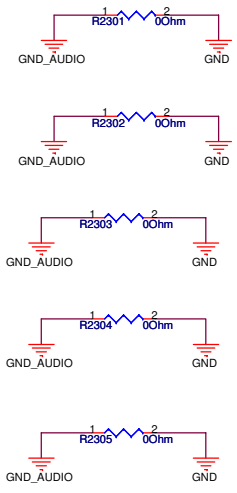
06/06 for cost down



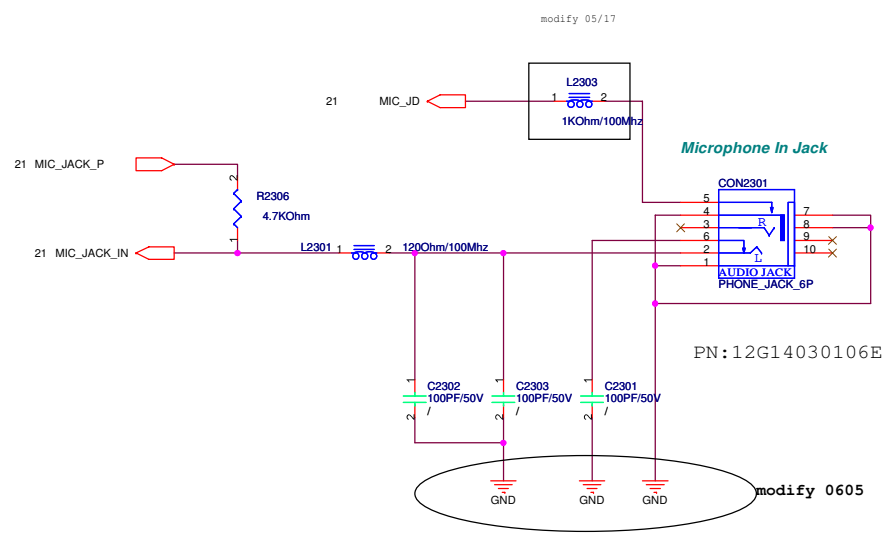
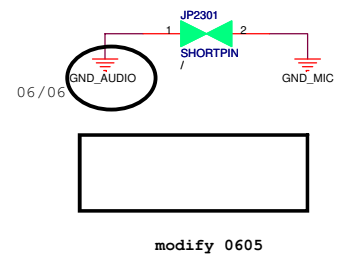


SPEAKER CONNENT

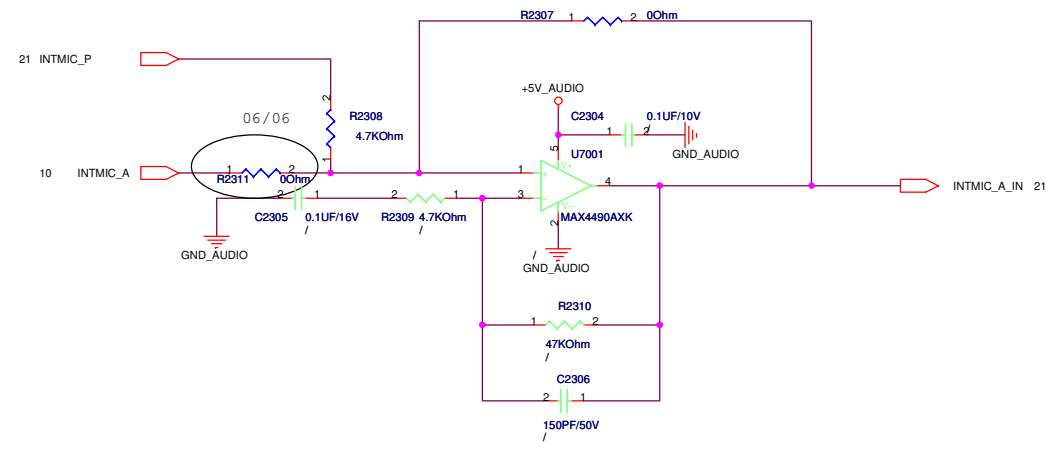


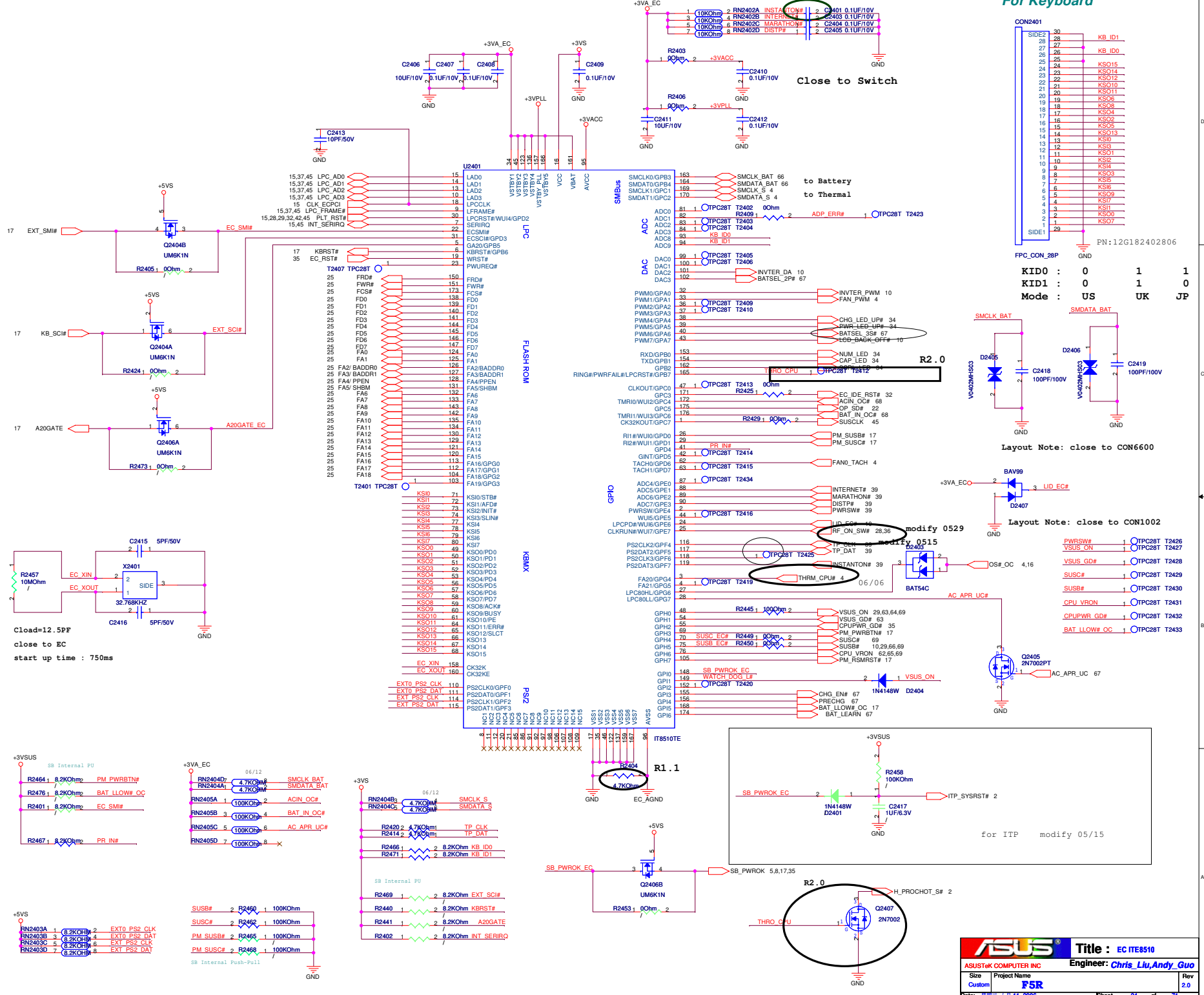


INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils

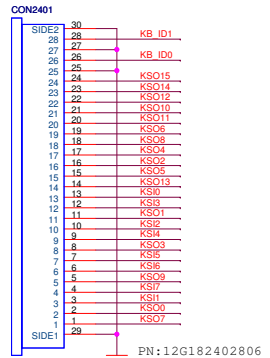


Pre-AMP For Test Function

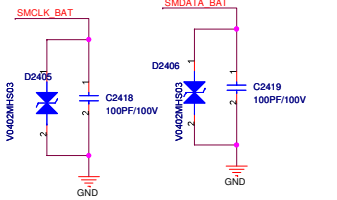




For Keyboard



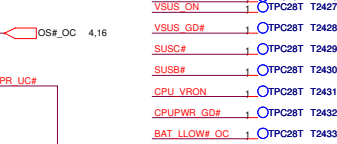
KIDO : 0 1 1
 KID1 : 0 1 0
 Mode : US UK JP



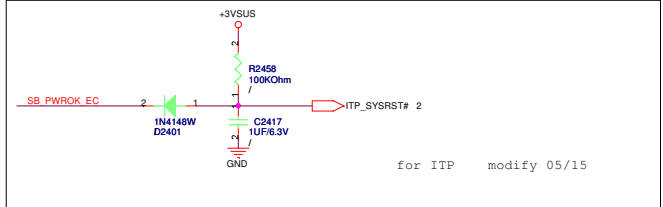
Layout Note: close to CON6600



Layout Note: close to CON1002



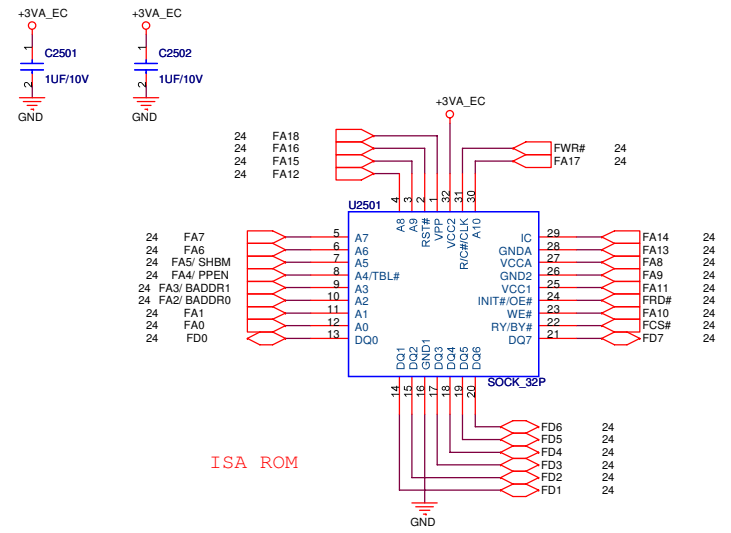
modify 0529
 modify 0515



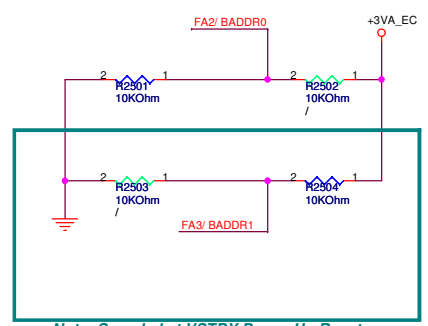
for ITP modify 05/15

ASUS Title : EC ITE8510
 ASUSTek COMPUTER INC Engineer: Chris_Liu, Andy_Guo
 Size Project Name
 Custom F5R
 Date: 2008年11月11日 Sheet 24 of 71

PLCC32 Socket PN:12G04300032F SST-PLCC32 4Mbits Flash ROM PN:05G001027221

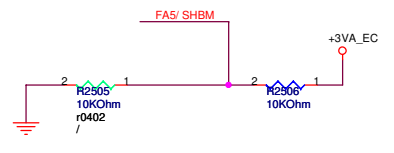


FA2/ BADDR0 & FA3/ BADDR1
 00: PNPENG Access Register Pair Are 002Eh and 002Fh
 10: PNPENG Access Register Pair Are 004Eh and 004Fh
 01: PNPENG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
 11: Reserved

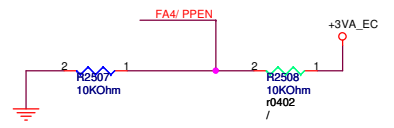


Note: Sampled at VSTBY Power Up Reset

FA5/ SHBM
 0: Disable Shared Memory with Host BIOS
 1: Enable Shared Memory with Host BIOS



FA4/ PPEN
 0: Normal
 1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



5

4

3

2

1

D

D

C


C

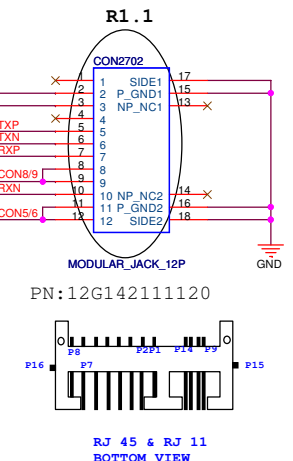
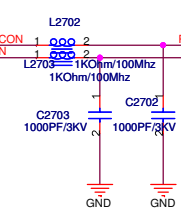
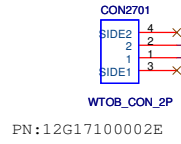
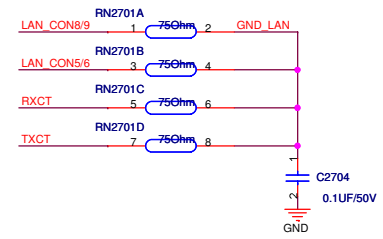
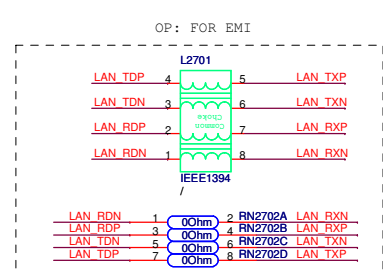
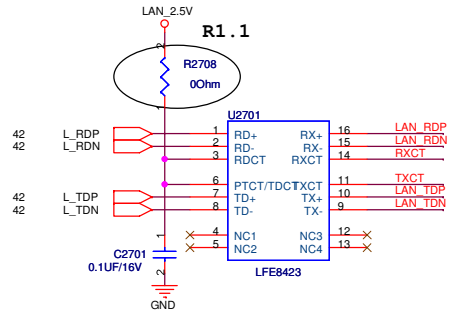
B

B

A

A

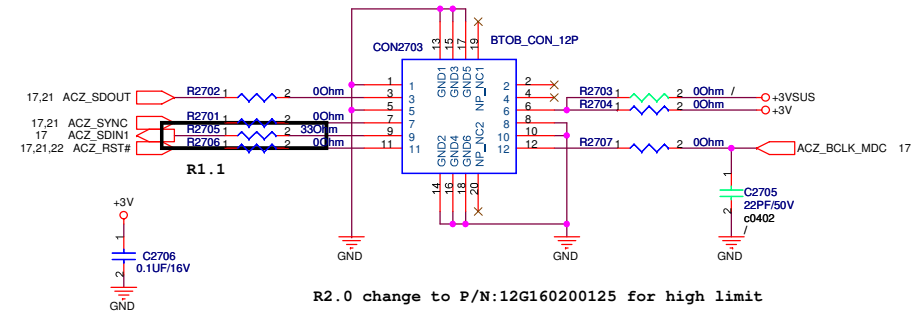
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ASUSTeK COMPUTER INC		Engineer: <i>Chris Liu, Andy Guo</i>	
Size	Project Name	Rev	
Custom	F5R	2.0	
Date:	星期三, 十月 11, 2006	Sheet	26 of 71

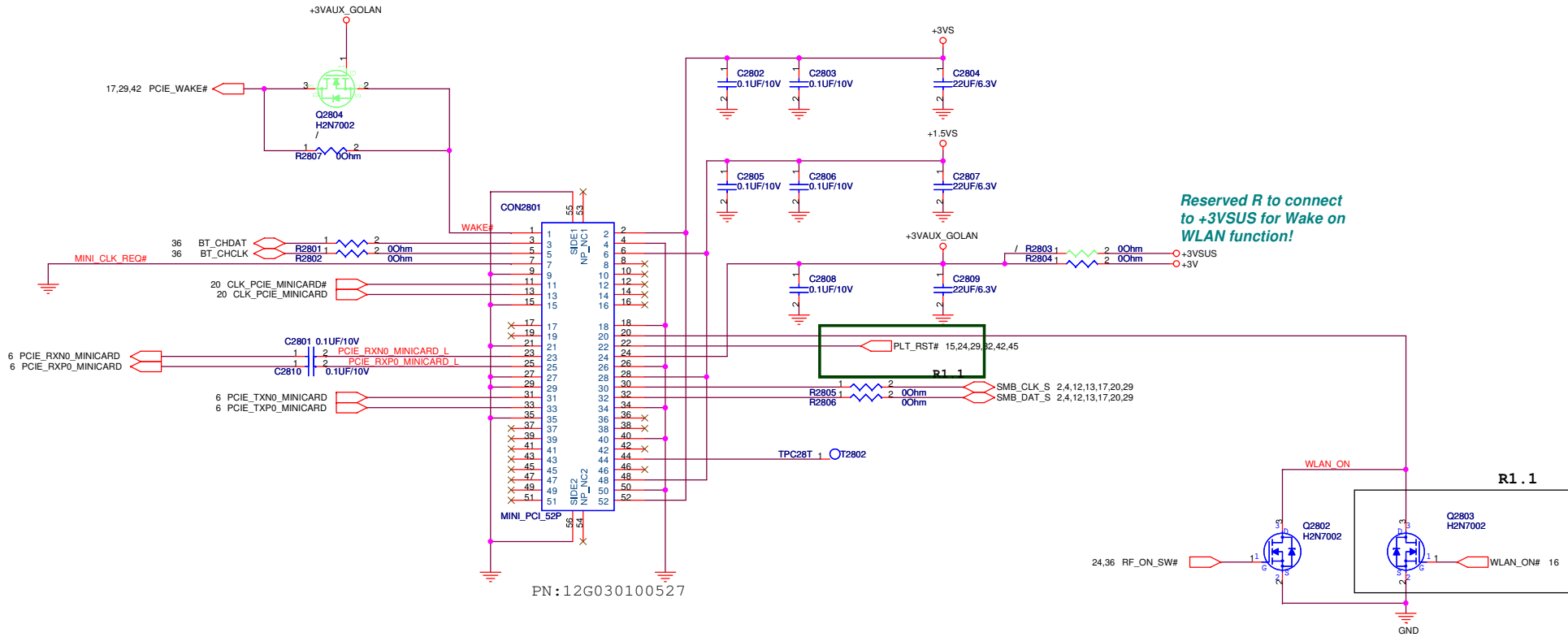


LAN PORT

MDC

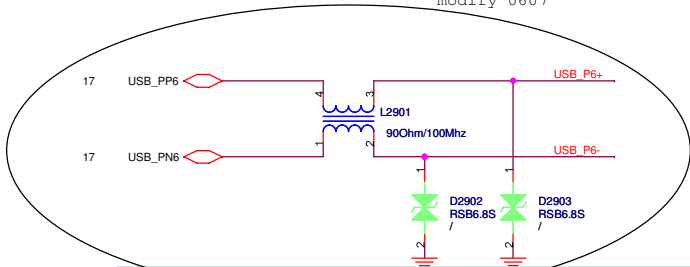
MDC



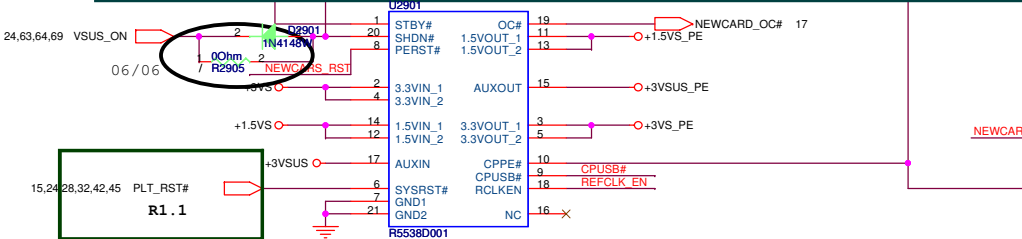
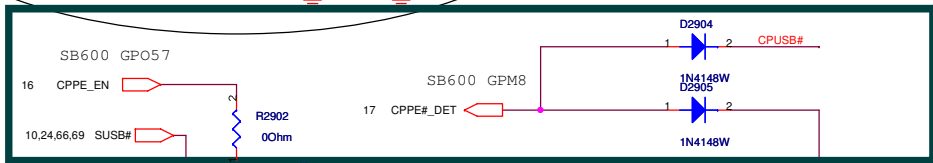


FOR SWAP

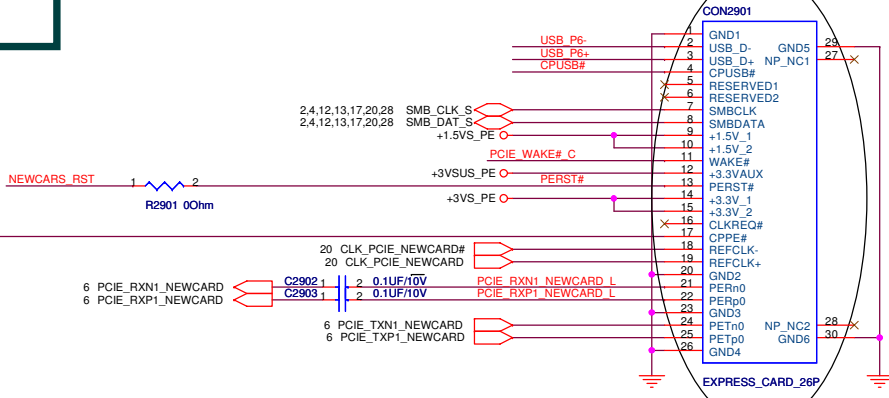
modify 0607



06/07

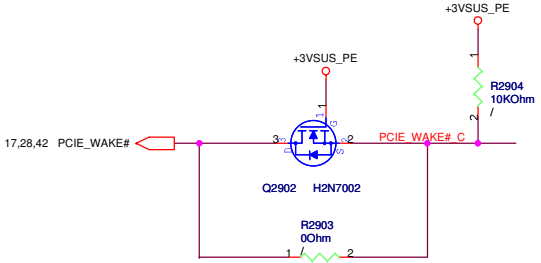
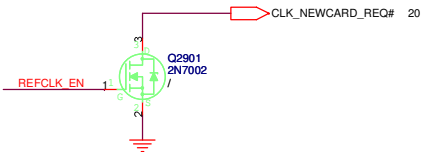


!ExpressCard Standard 1.0:
 Change Pin7 from RESERVED to SMBCLK
 Change Pin8 from SMBCLK to SMBDATA
 Change Pin9 from SMBDATA to +1.5V

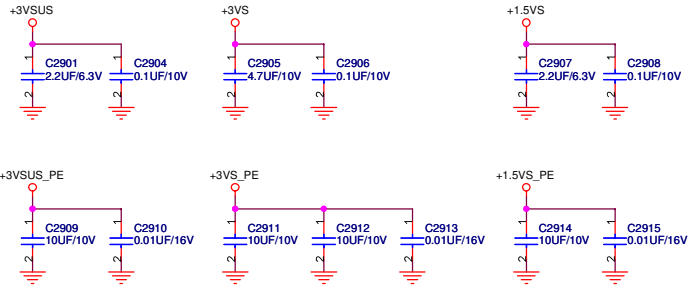


PN:12G161300261

06/07

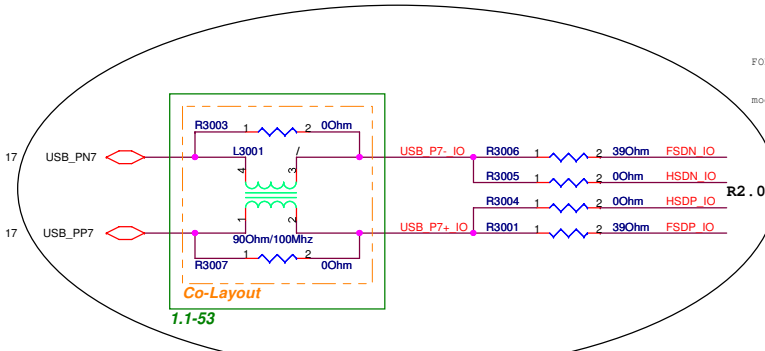


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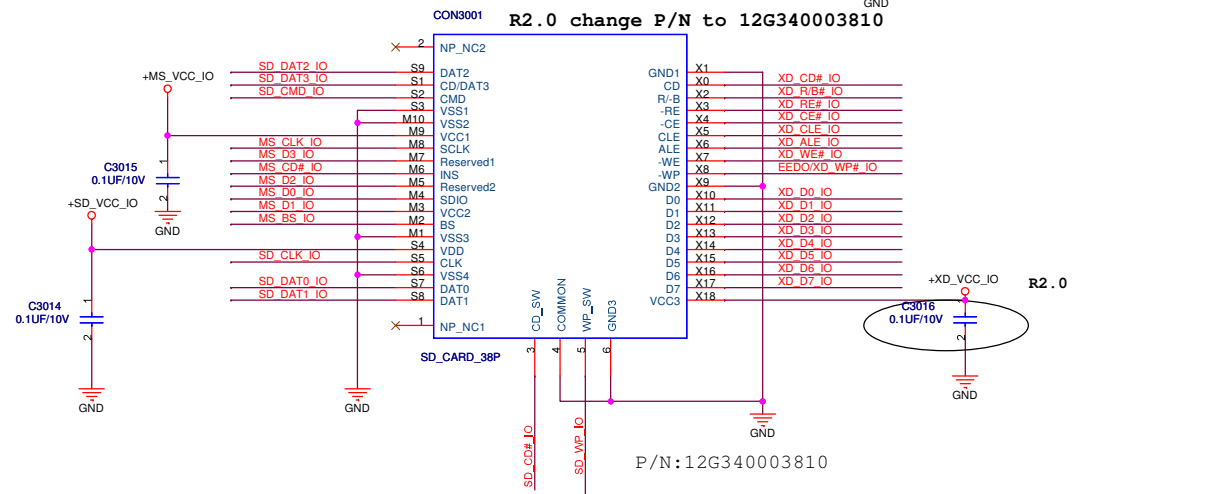
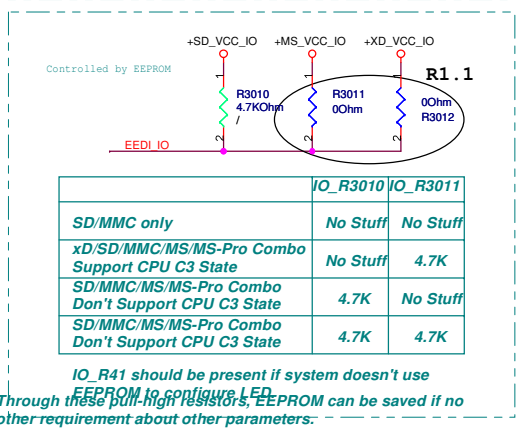
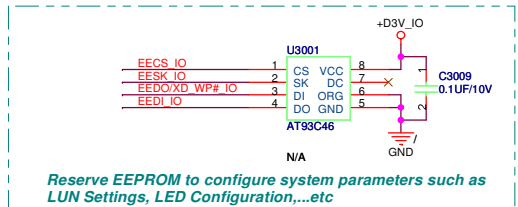
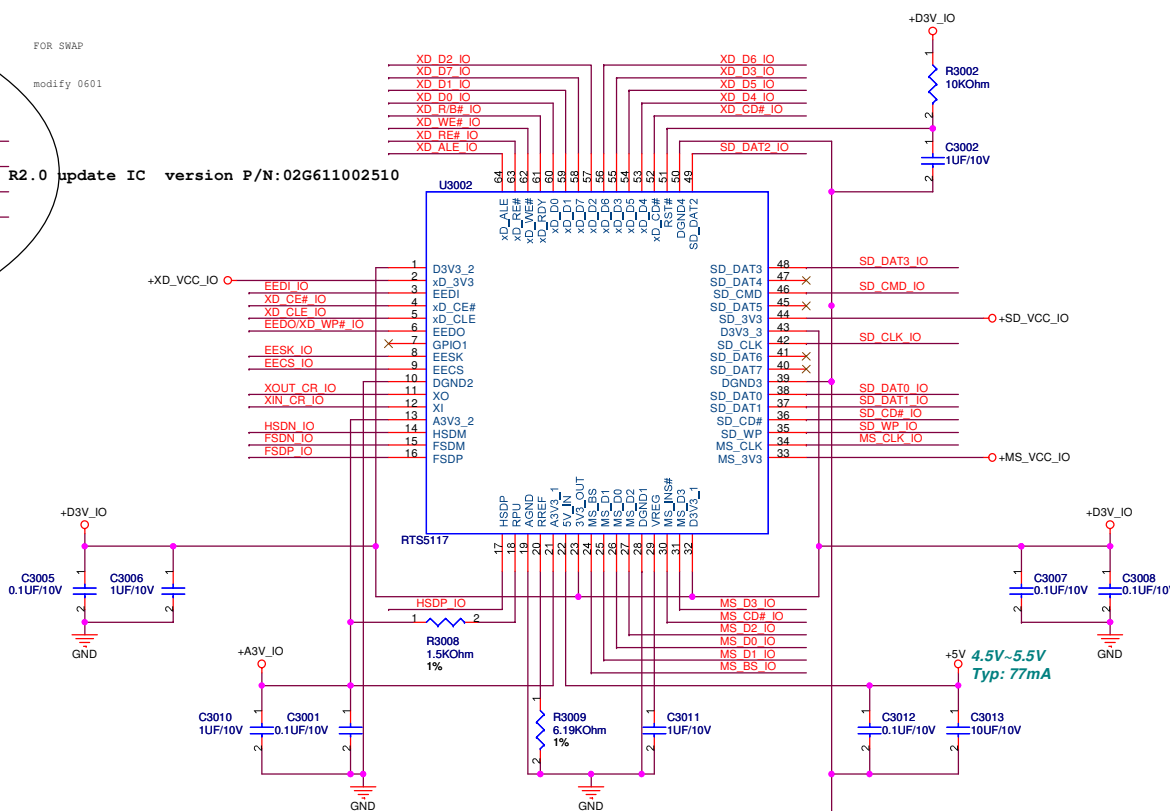


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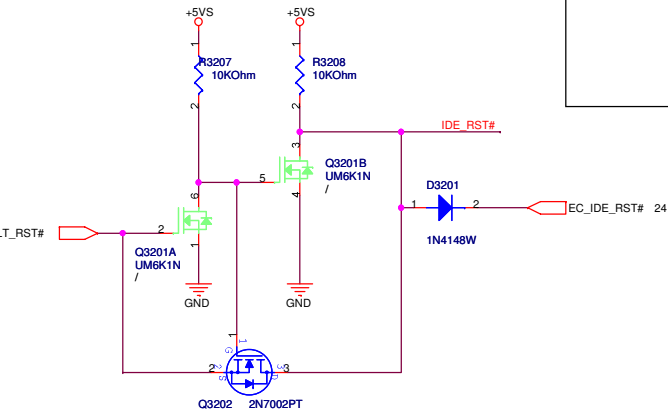
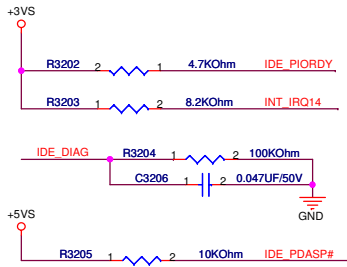
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ASUSTeK COMPUTER INC		Engineer: Chris Liu, Andy Guo	
Size	Project Name		Rev
Custom	F5R		2.0
Date: 星期三, 十月 11, 2006		Sheet 29 of 71	



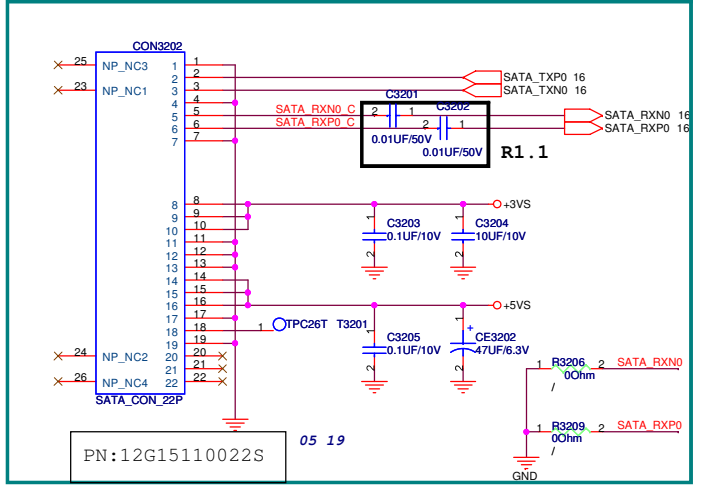
FOR SWAP
modify 0601
R2.0 update IC version P/N:02G611002510



P/N:12G340003810



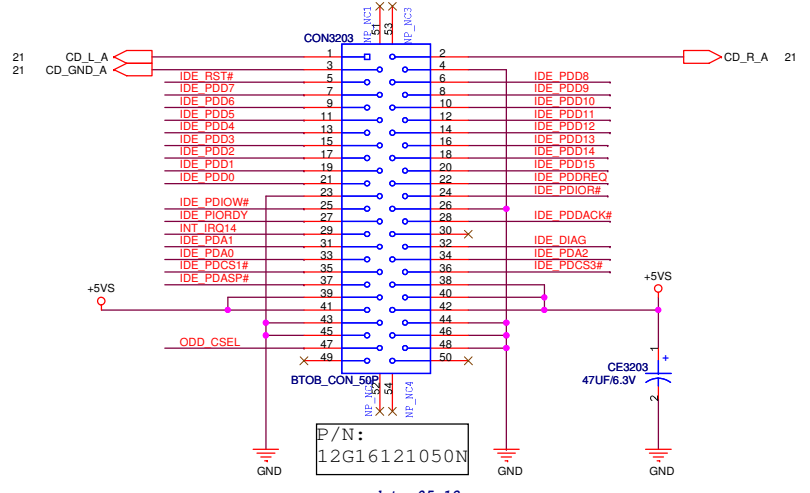
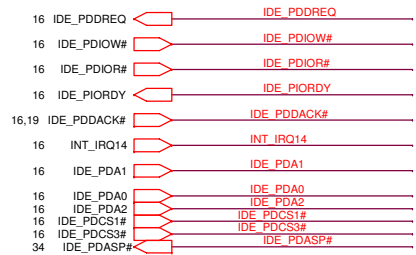
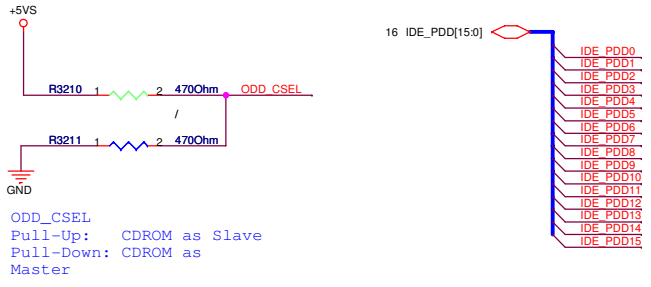
modify 0512



PATA

SATA

CD-ROM



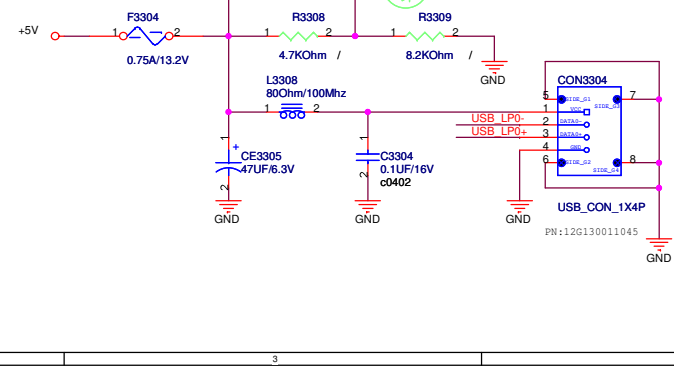
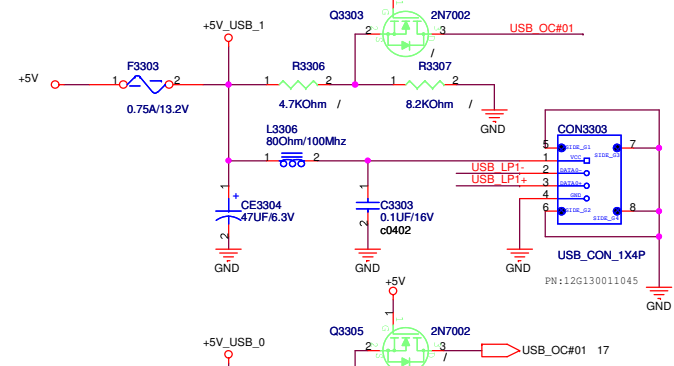
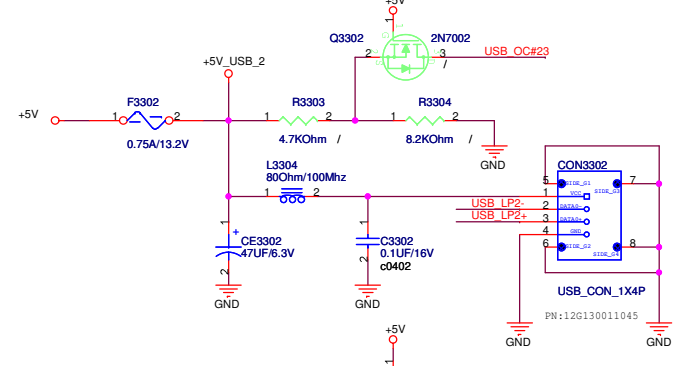
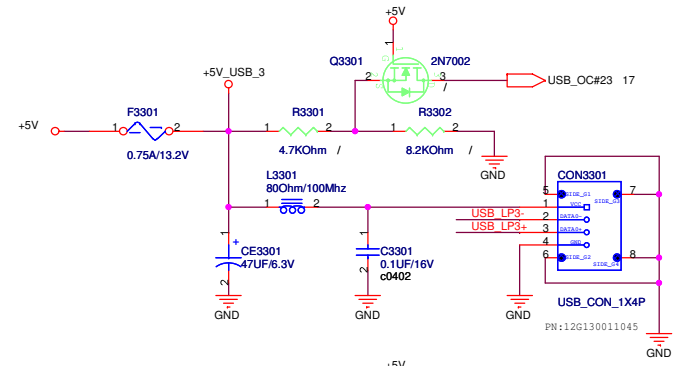
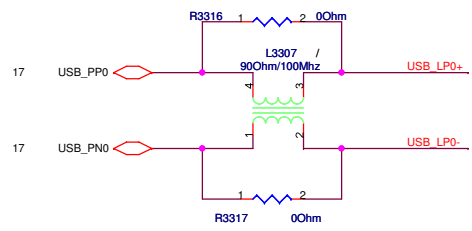
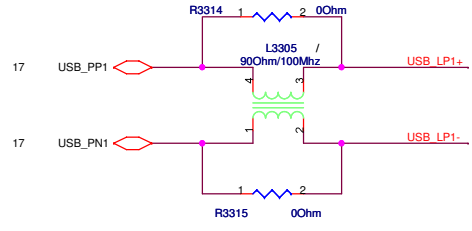
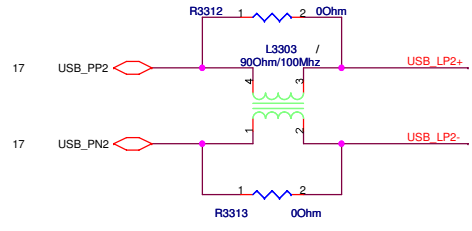
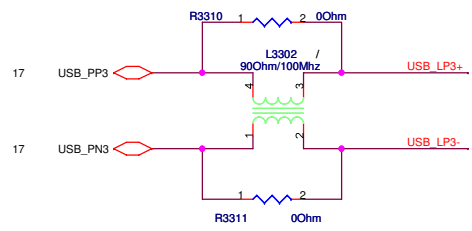
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Title : HDD & CD-ROM

ASUSTeK COMPUTER INC. Engineer: **Chris Liu, Andy Guo**

Size	Project Name	Rev
Custom	F5R	2.0
Date: 星期三, 十月 11, 2006	Sheet	32 of 71

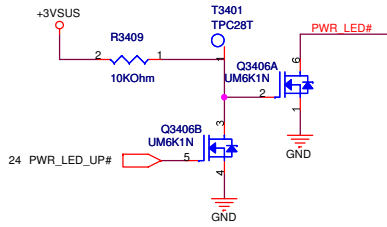
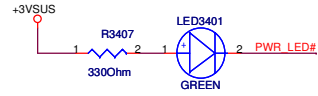
update 05 18



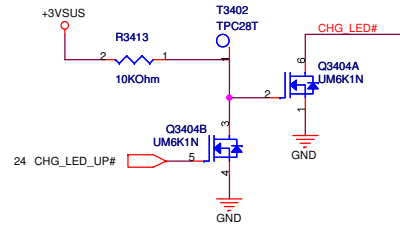
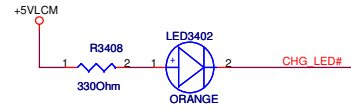
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ASUSTeK COMPUTER INC		Engineer: <i>Chris_Liu,Andy_Guo</i>	
Size	Project Name	Rev	
Custom	F5R	2.0	
Date: 星期三, 十月 11, 2006		Sheet	33 of 71

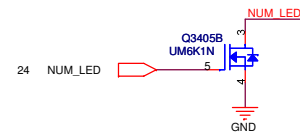
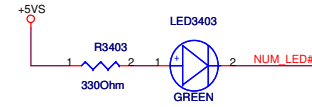
For POWER LED



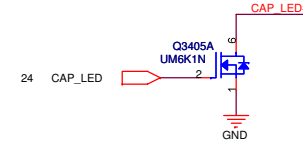
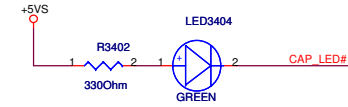
BATTERY LED



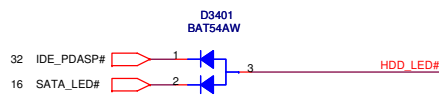
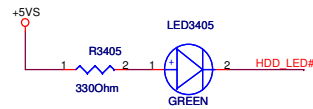
Num Lock



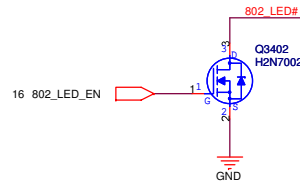
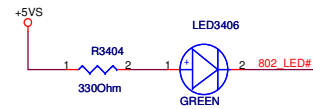
Cap Lock



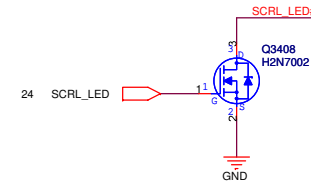
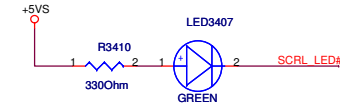
SATA/IDE LED



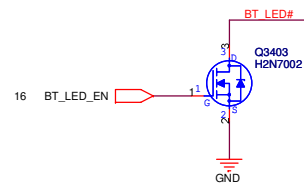
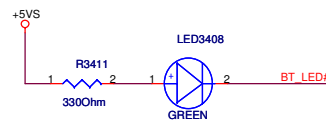
WireLess LED



Scroll Lock

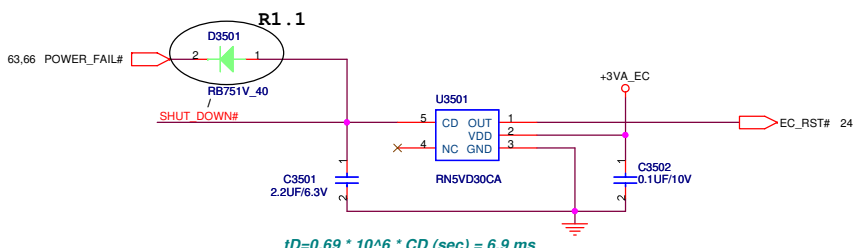


BT LED

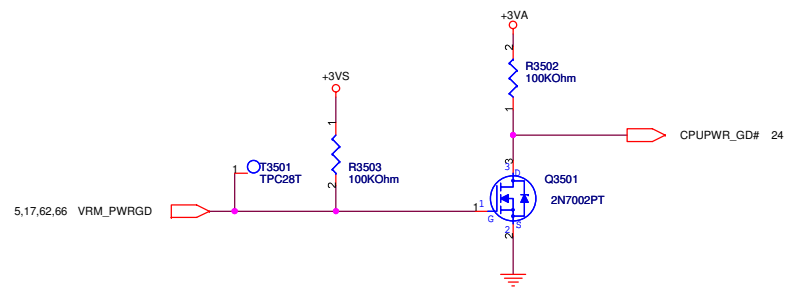


<Variant Name>

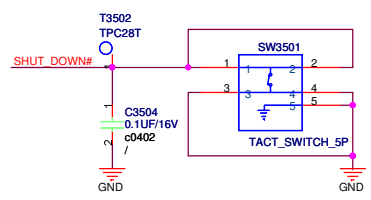
ASUS		Title : LED	
ASUSTeK COMPUTER INC		Engineer: <i>Chris Liu, Andy Guo</i>	
Size	Project Name	Rev	
Custom	F5R	2.0	
Date: 星期三, 十月 11, 2006		Sheet 34 of 71	



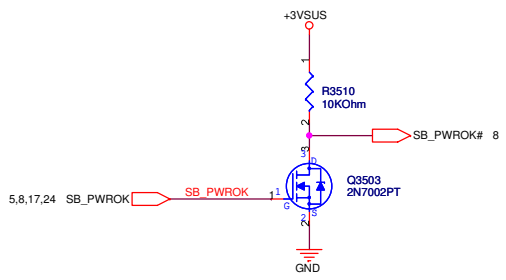
$tD = 0.69 * 10^6 * CD \text{ (sec)} = 6.9 \text{ ms}$
 $tD = 0.69 * 10^6 * CD \text{ pin sec}$ Change threshold = 2.9V



RESET SW.



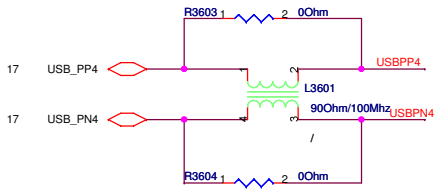
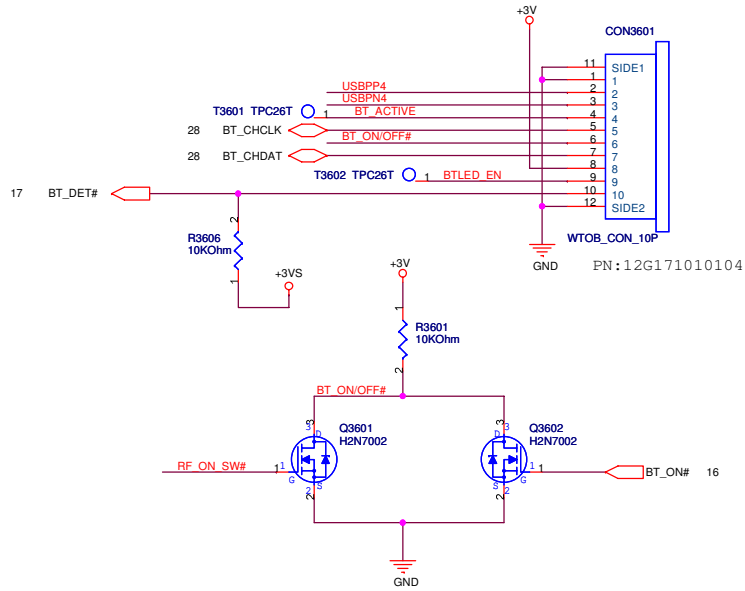
P/N: 12G091030050



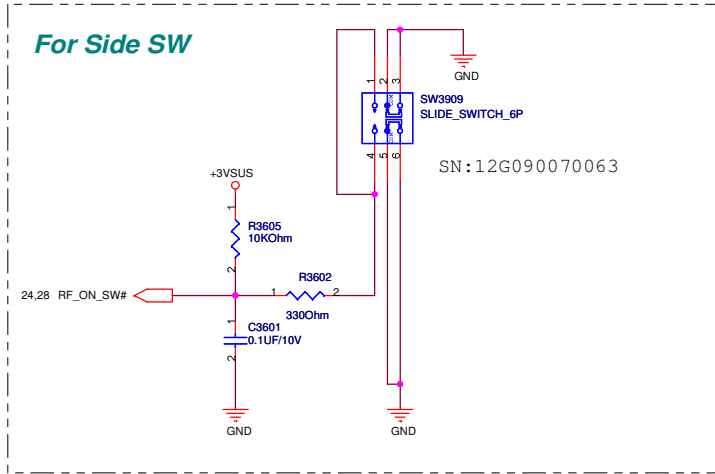
<Variant Name>

ASUS		Title : RST
ASUSTeK COMPUTER INC		Engineer: <i>Chris_Liu,Andy_Guo</i>
Size	Project Name	Rev
Custom	F5R	2.0
Date: 星期三, 十月 11, 2006	Sheet	35 of 71

For Bluetooth



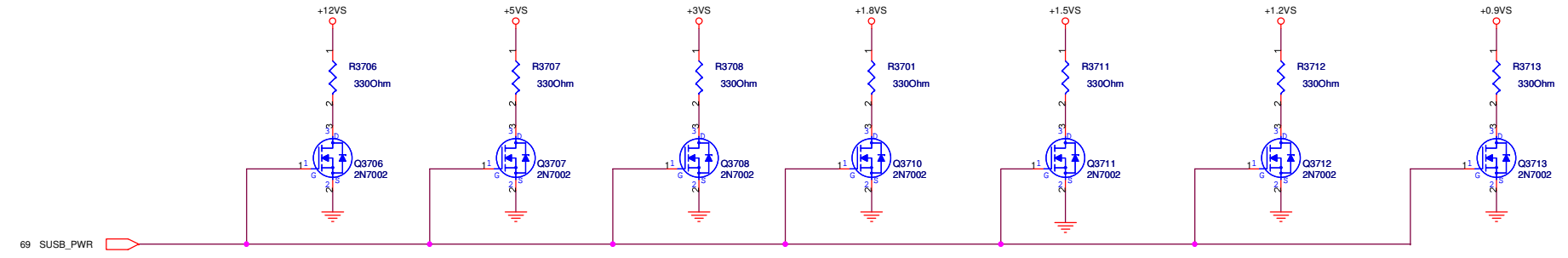
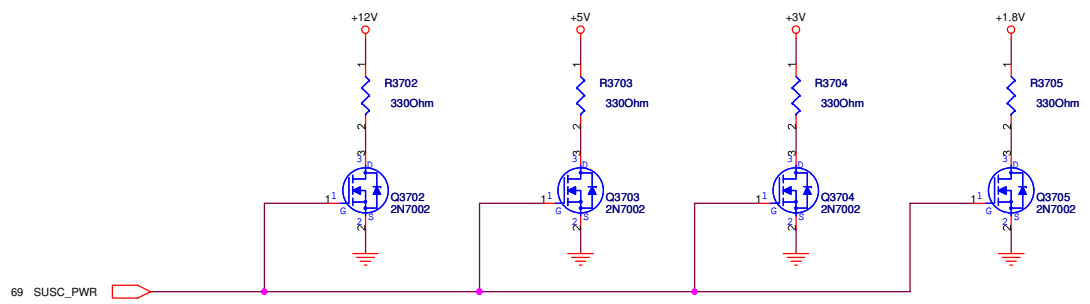
For Side SW



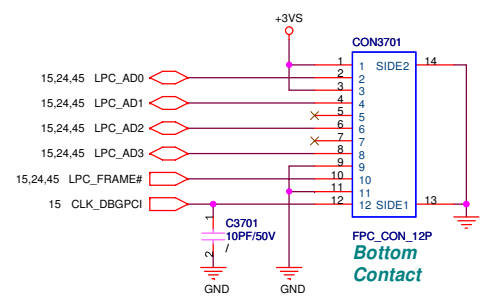
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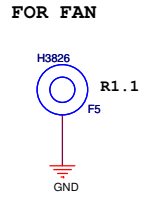
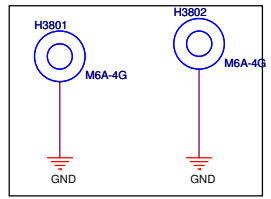
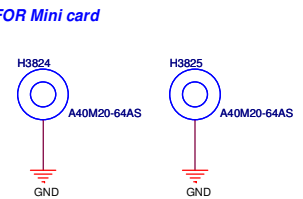
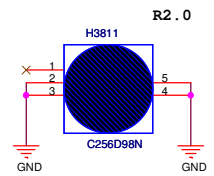
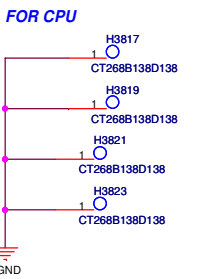
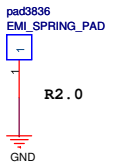
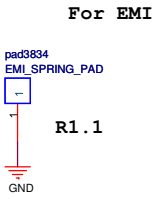
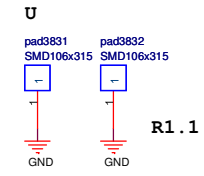
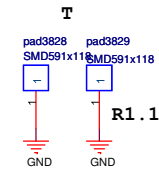
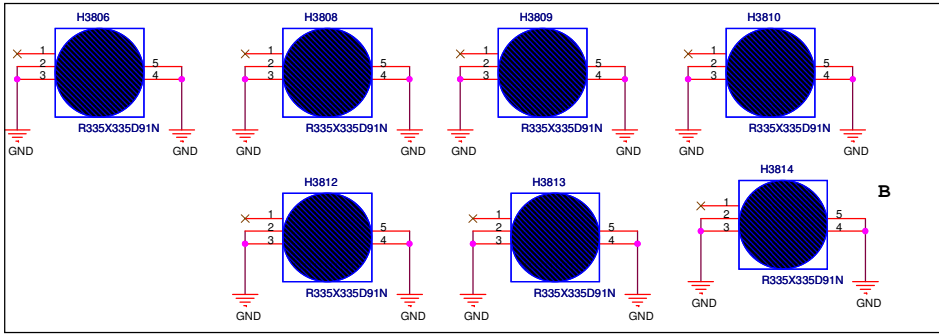
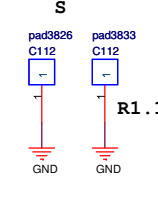
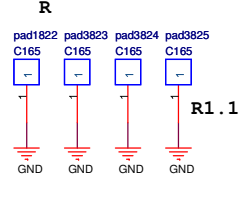
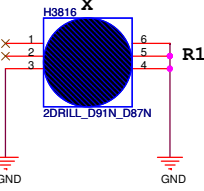
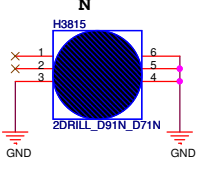
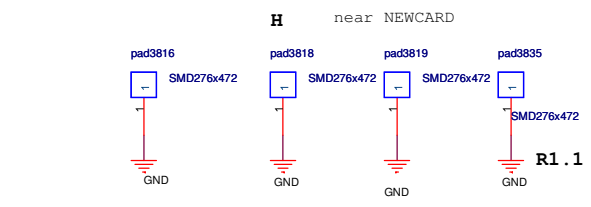
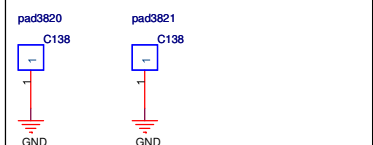
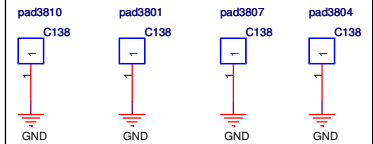
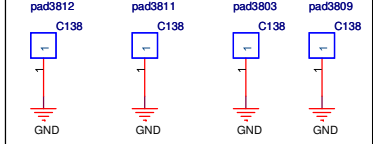
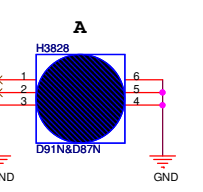
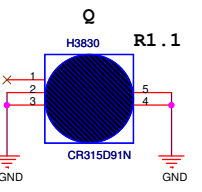
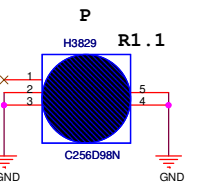
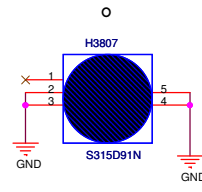
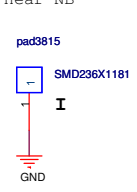
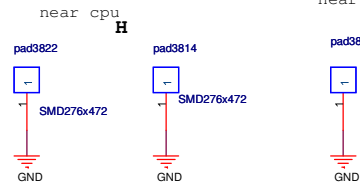
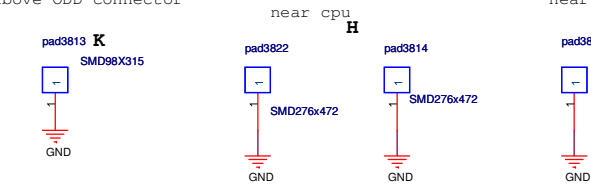
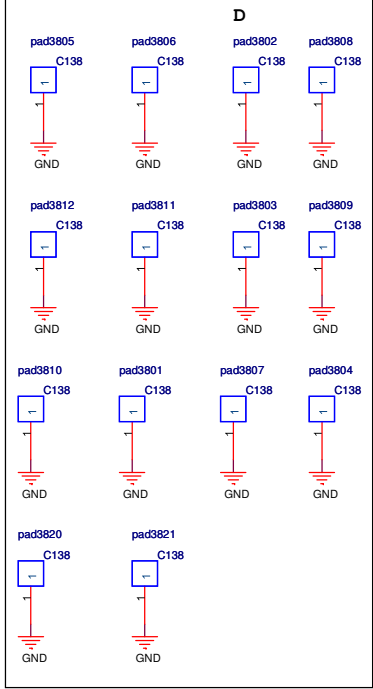
System Power Sequence
 +VCCRTC -> RTCRST# -> V5REFSUS -> 3.3/1.5VSUS->
 RSMRST#->SUSC#->SUBS#->VCCLAN->LANPWROK
 ->V5REF->PWROK->GMCH->VCCP->VCORE
 SUSSTAT#->PCIRST#

CPU : +VCORE, +VCCP, +1.05VS
 NB : +1.05VS, +1.2VS, +2.5V, +VCCP
 SB : +1.2VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
 DDR : +1.8V, +0.9VS



Debug Port

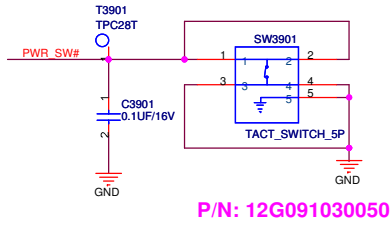




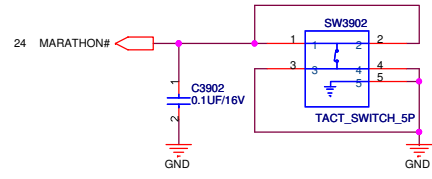
R2.0 change to P/N:13GN9980M090-1 for high limit

ASUS		Title : Screw Hole	
ASUSTeK COMPUTER INC		Engineer: <i>Chris_liu,Andy_Guo</i>	
Size	Project Name	Rev	
Custom	F5R	2.0	
Date: 星期三, 十月 11, 2006		Sheet 38 of 71	

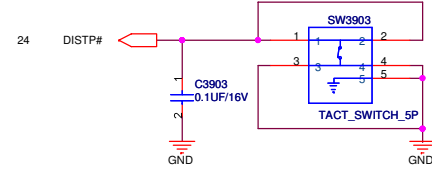
Power SW.



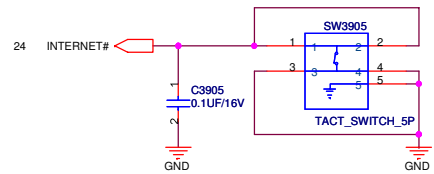
Marathon SW.



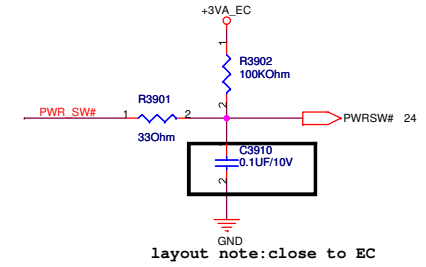
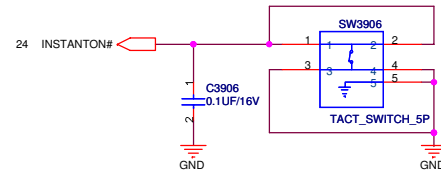
Disable Touch Pad SW.



Internet SW.

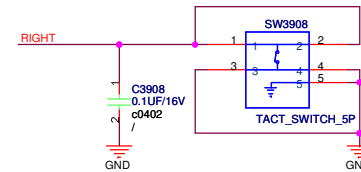
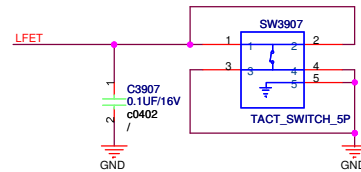
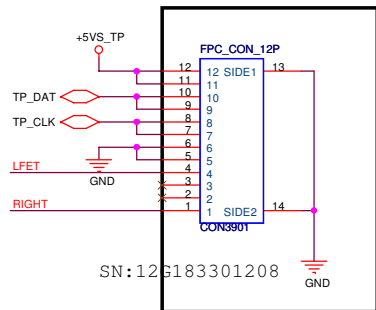
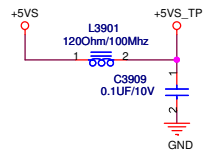


IstantON SW.



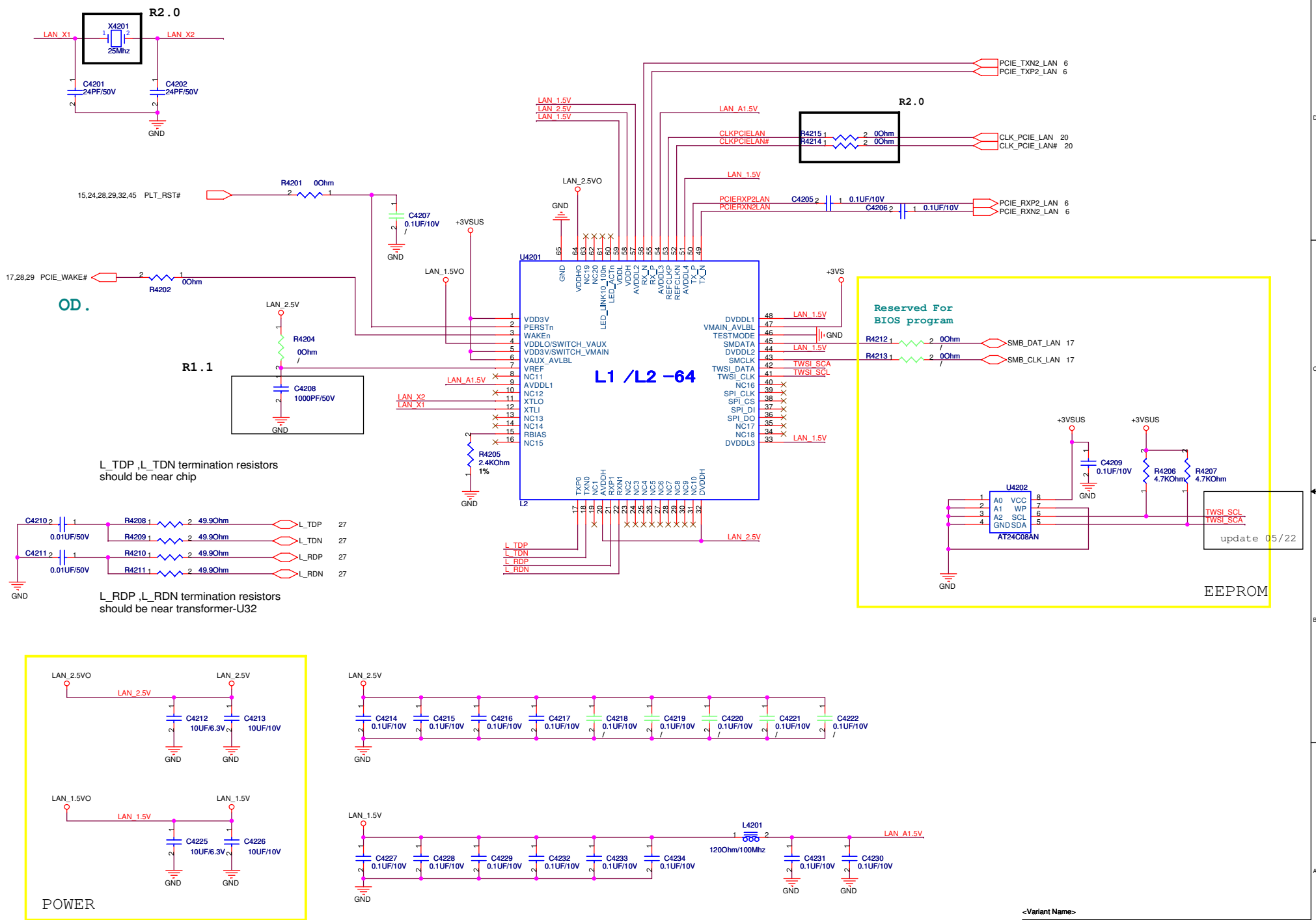
modify 05/17

Touch-Pad

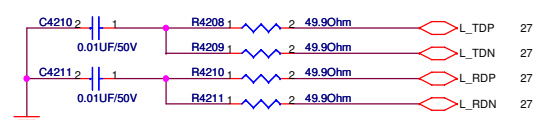


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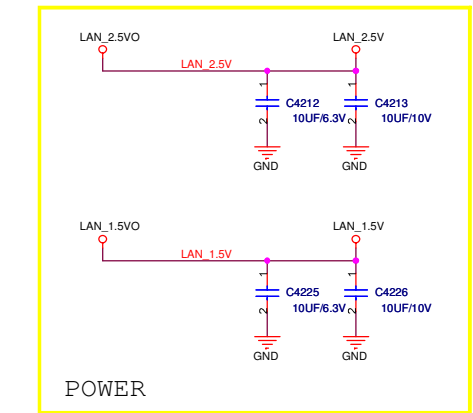
ASUS		Title : SWITCH & TP
ASUSTeK COMPUTER INC		Engineer: Chris_liu,Andy_Guo
Size	Project Name	Rev
Custom	F5R	2.0
Date: 星期三, 十月 11, 2006	Sheet	39 of 71



L_TDP, L_TDN termination resistors should be near chip



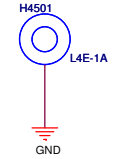
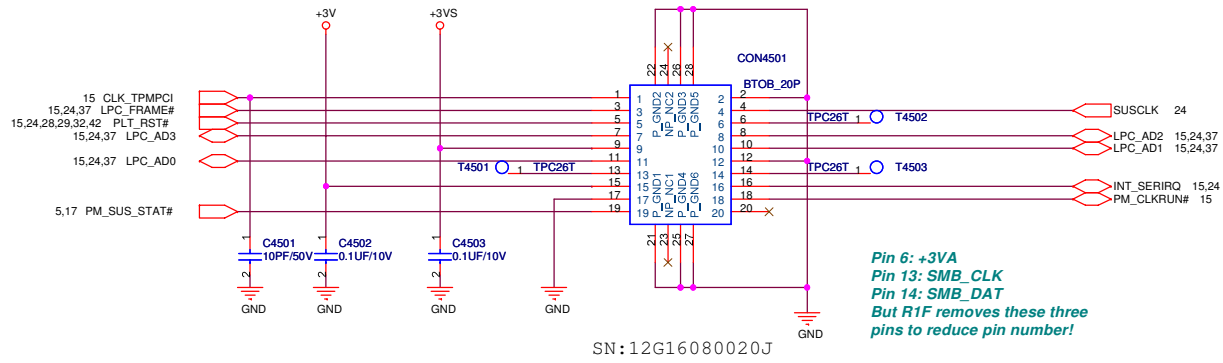
L_RDP, L_RDN termination resistors should be near transformer-U32



update 05/22

EEPROM

For TPM Module



change list:

06-05-12
 1. page16, add another thermal sensor schematic according to ATI demo schematic.
 2. page32. delete PATA HDD connector according to ME request
 3. page 12.13.17.add mem_sensor according to ATI demo schematic

06-05-15
 1.Add the ITP function on page 2,20,24.
 2. Page 24 delete the PWRLIMIT# net (power part has delete the power limit function)

06-05-16
 1.connect BATSEL_3S# to EC pin 40

05-06-17
 1.pag39 delete sw3904 according to markeeting spec
 2. page 22 add L2210 for layout request
 3.add L2303 for layout request

06-05-18
 1. page 32 update ODD connector CON3203 P/N
 2. PAGE 29 modify NEWCARD connector U2902 P/N

06-05-19
 1. page 32 update SATA connector CON3202 P/N

06-05-22
 1. page 5 change R510 to D501 according to F5X
 2. page5 ADD R513 according to F5X
 3. page 8 Remove L809,C811 according to ATI demo schematic
 4. page10 mount L1011,unmount L1015 due to using the D/A inverter
 5. page 15 remove R1524 due to SB600 (for Yonah)do not support H_PROCHOT
 6. page 16 mount R1604 according to ATI suggestion
 7. Page 17 add R1733,R1733 according to ATI suggestion
 8. Page 30mount U3001,C3009 according to F5X
 9. Page 38 add screw hole and pad
 10. Page 42 exchange TWSI_SCA and TWSI_SCL

06-05-23
 1. Page27 Add R2708 pull up resistor for Attansic request
 2. Page27 change C2702,C2703 to close to CON2702

06-05-24
 1. page12 modify CON1201 P/N

06-05-25
 1. Page38 add H3826 for lock fan
 2. delete some screw hole and add pad3820,pad3821

06-05-26
 1. page 38 add screw hole H3815 H3816

06-05-29
 1. page 17 exchange net USB_PP5 and USB_PP3,exchange net USB_PN5 and USB_PN3
 2. page 24 connect RF_ON_SW# to EC pin 25
 3. page16 connect net BT_ON# to SB600 GPIO47
 4. page 16connect net 802_LED_EN to GPIO55
 5. page 16 connect net BT_LED_EN to GPIO56

06-05-30
 1. page 22 connect con2202 pin 5,pin6 to GND_AUDIO

06-06-01
 1. Page 29 swap USB_PP6 and USB_PN6
 2. Page 30 swap USB_PP7 and USB_PN7
 3. Page 17 add pull up resistor R1735 and R1736,decoupling capacitor C1709 and C1710 on the USB_OC#01,USB_OC#23
 4. Page17 add test point T1725,T1726
 5. Page8 add test point T813

06-06-05
 1. page38 change H3807 P/N
 2. page22 delete net GND JACK
 3. page23 delete net GND JACK and JP2302

06-06-06
 Page 5 Add resistor R514 accordintg to Frank's suggestion
 Page 8 Add resistor R828 accordintg to Frank's suggestion
 Page 23 Add resistor R2311 for EMI request
 Page 23 change GND to GND_AUDIO for EMI request
 Page 3 Add C330 and C331 for EMI suggestion
 Page 65 connect PR6507 pin 2 to +12VS
 Page 24 delete Q2407 for repeat
 Page 29 Add R2905,unmout d2901 for cost down
 Page 21 change U2102 for cost down
 Page 20 change U2001 for thermal request

06-06-07
 Page 29 Modify the CON2901 schematic
 Page 14 delete RN1405,CN1405
 Page 16 connect VIN4 to R2902 for newcard shut down
 Page 17 connect USB_OC#8 to D2904,D2905 FOR NEW CARD DETECT
 Page 29 ADD R2902, D2904,D2905
 page 38 change pad3819 connect to GND for EMI request
 Page 29 swap USB_PP6 and USB_PN6

06-08
 page4 change CE401 P/N for hight limit


R1.1

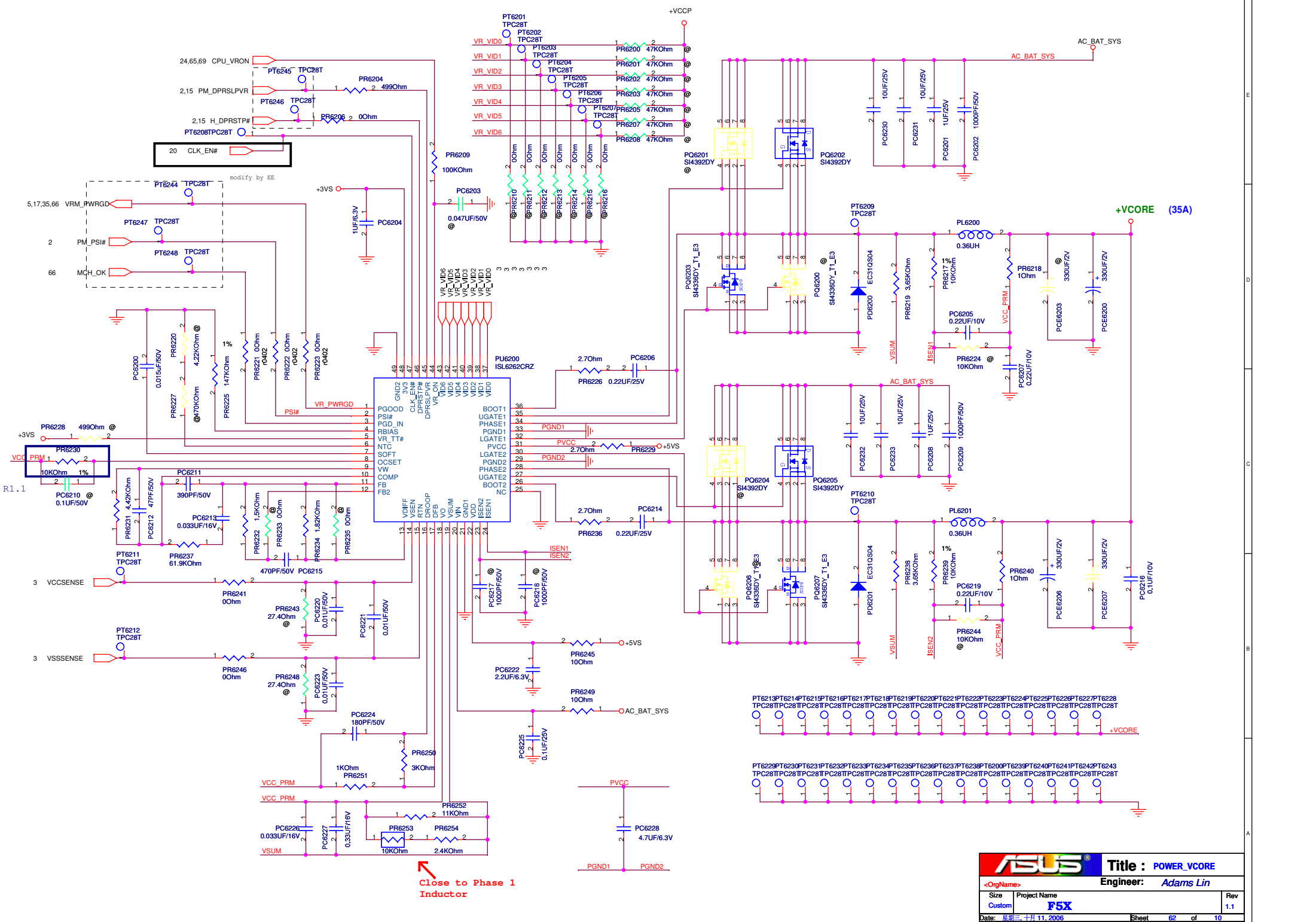
Page3 DNI CE301,CE302,CE303,CE304,CE305
 Page4 R401,R406 change to 0 ohm
 Page5 R513 cahnge to 220K ohm,Mount R514, DNI R511
 Page8 add (L809 and C811)DNI for RC610
 Page16 X1601 change to PN:07G010Q02501 for cost
 Page22 R2201,R2203 change to 0ohm DNI R2205,R2206 chenge U2201 P/N for cost down
 page 24 R2404 change to 4.7Kohm
 Page27 R2708 change to 0 ohm,change CON2702 P/N
 Page28 Mount Q2803 for BIOS request
 Page30 R3011,R3012 change to 0 ohm according to attansic demo schematic
 Page32 C3201,C3202 change to 0.01u
 Page39 Reverse CON3901 pin definition for ME request
 Page42 X4201 change to PN:07G010Q02501 for cost down
 Page 2 change R227 pull-up resistor from 200 ohm resistor to 470 ohm resistor according ATI suggestion
 Page 5 remove D502 (for SB600,it is no need)
 Page 8 chang Q803 from N-MOS to P-MOS,add Q804 for correction
 Page11 correct HSYNC YSYNC the ESD protection diodes connect to +5VS instead of +3vs.
 page 15 add 8.2Kohm 5% pull-down resistor on A_RST# to ensure a logic low at initial power-on.
 Page 16 Please leave pin SATA_RX1/2/3+/- unconnected, do not connected them to ground according to ATI suggestion
 Page 16 remove R1609,RN1601according to ATI suggestion
 Page 17 change R1730,R1731,R1732 pull-up resistor to +3.3VSUS
 page 38 add EMI finger
 page 16 change C1611,C1612 from 24pf to 10pf

R2.0

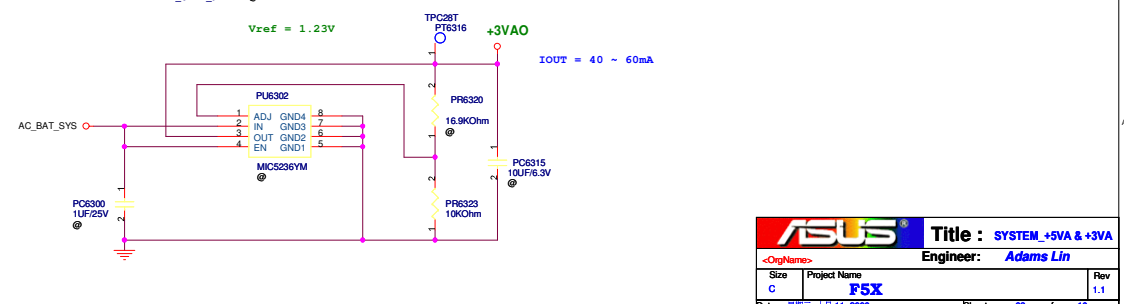
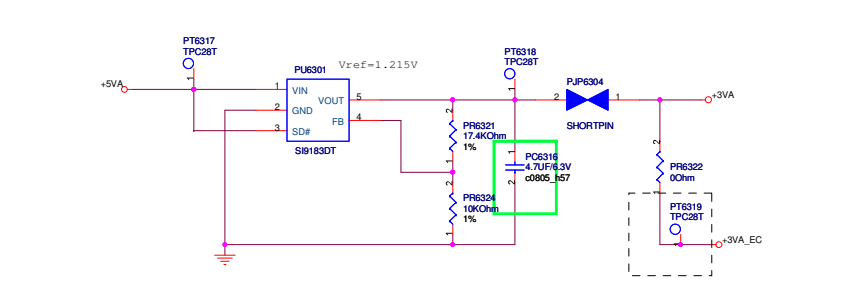
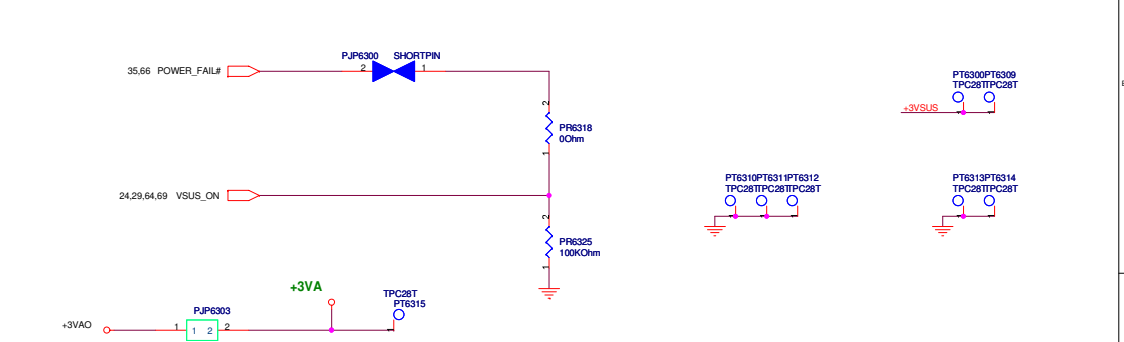
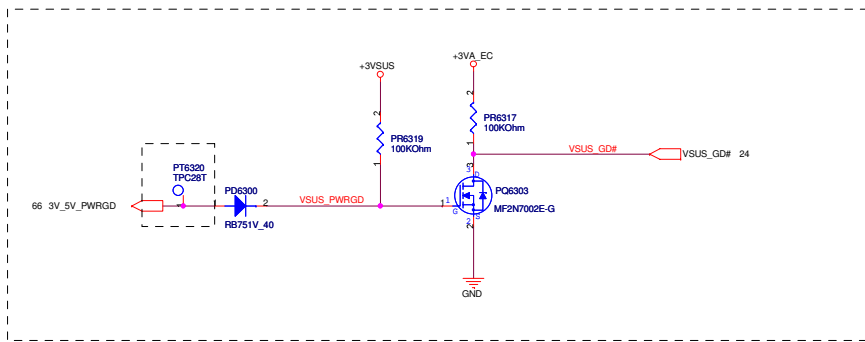
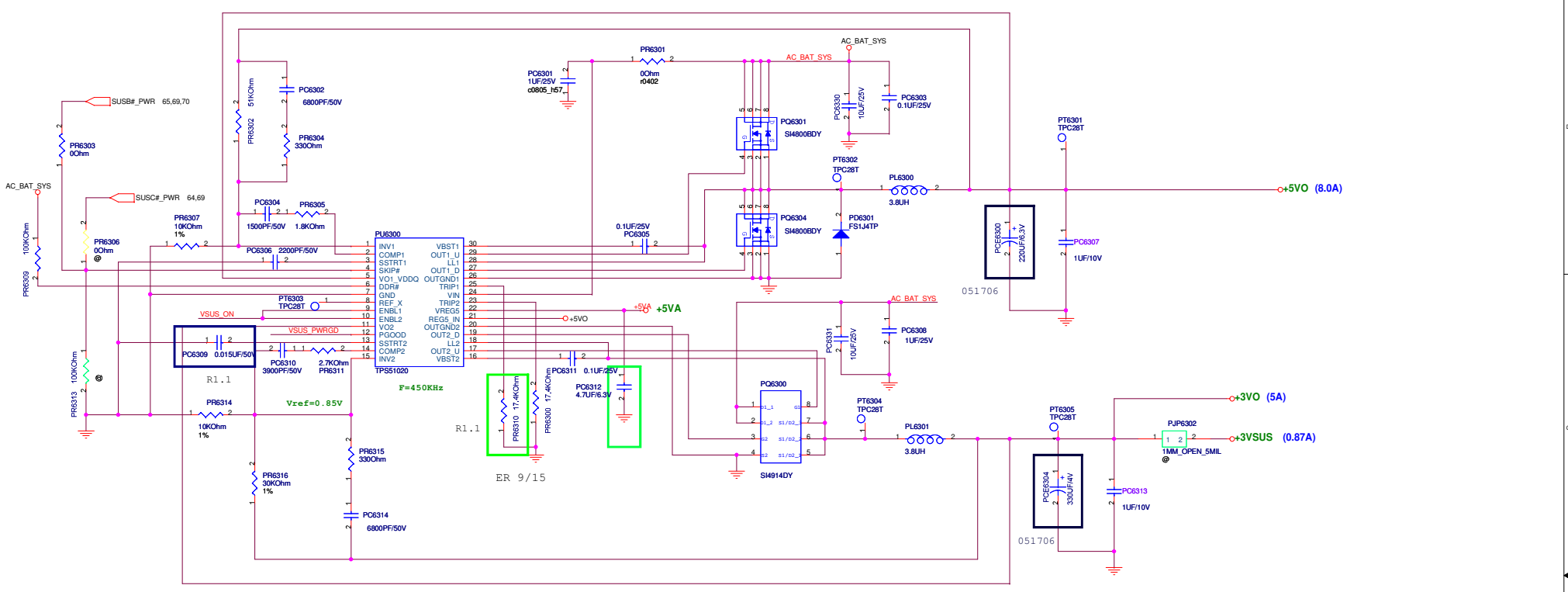
page 2 ,24 add CPU throttle function for power team request (add Q2407)
 page16 delete change net name CPPE_EN,and delete its pull down resistor RN1604
 page17 change net name CPPE_DET#, unmount R1730,R1731,R1732 for fix bug :cannot find ODD
 page 22 exchange SPKL+ SPKL-,SPKR+ SPKR-,EAR_R EAR_L for correction, add R2219 for vista option
 Modify CON3001,CON2801,CON2703,H3801,H3802 P/N
 Modify R2102 value from 33ohm to 47ohm for correcting AC_SDINO slew rate.
 Modify L1101,L1102,L1103 from bead to inductor 68nH for correction R G B signal rise time falling time and amplitude

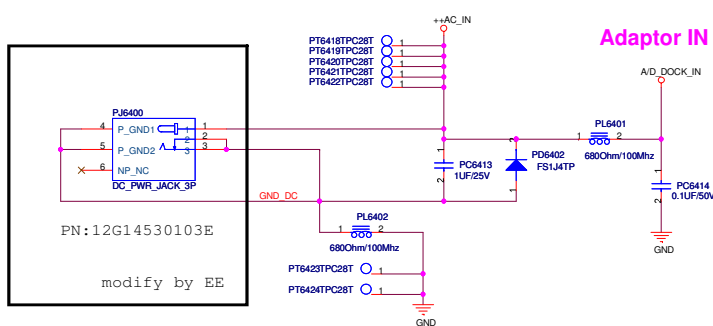
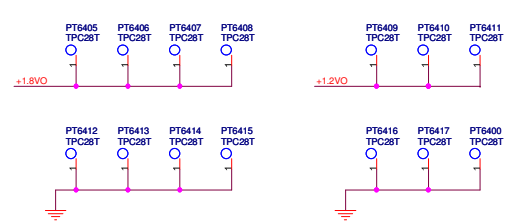
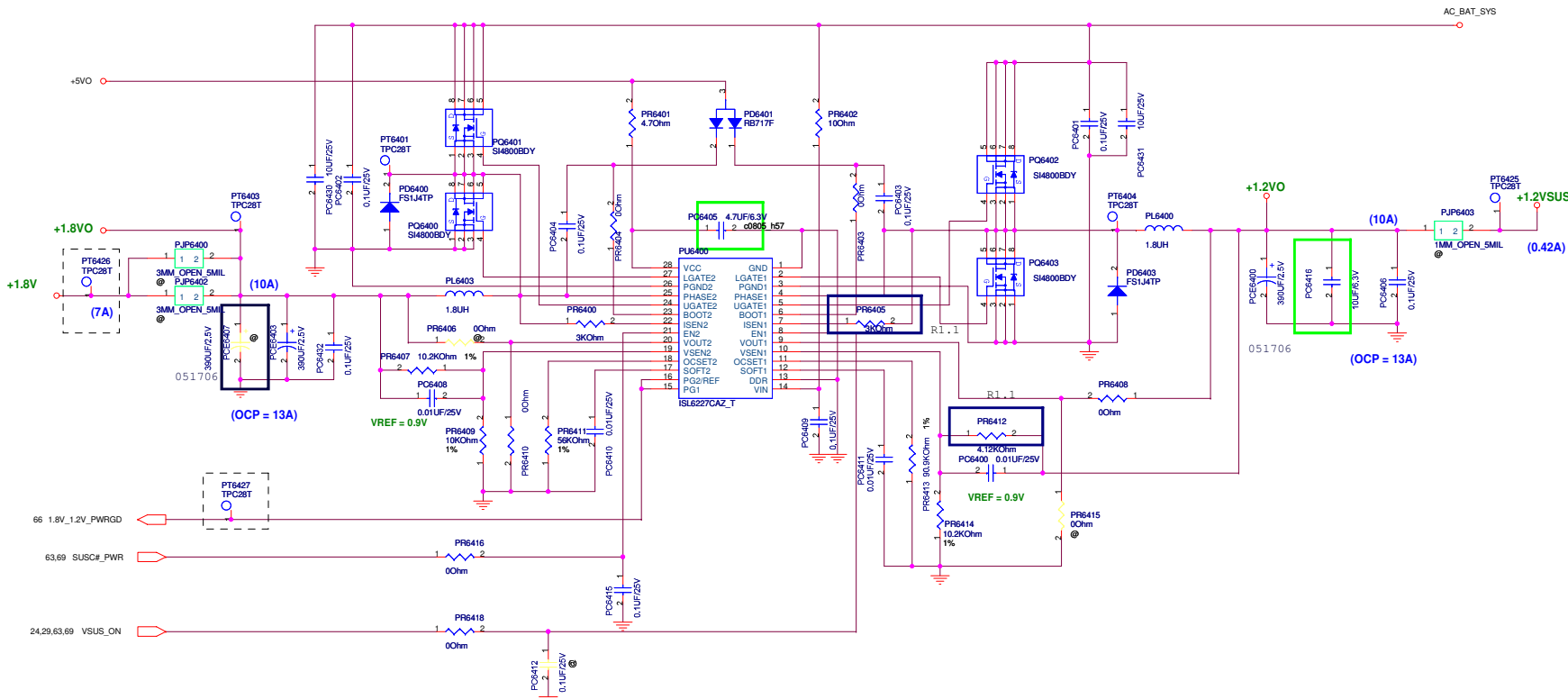
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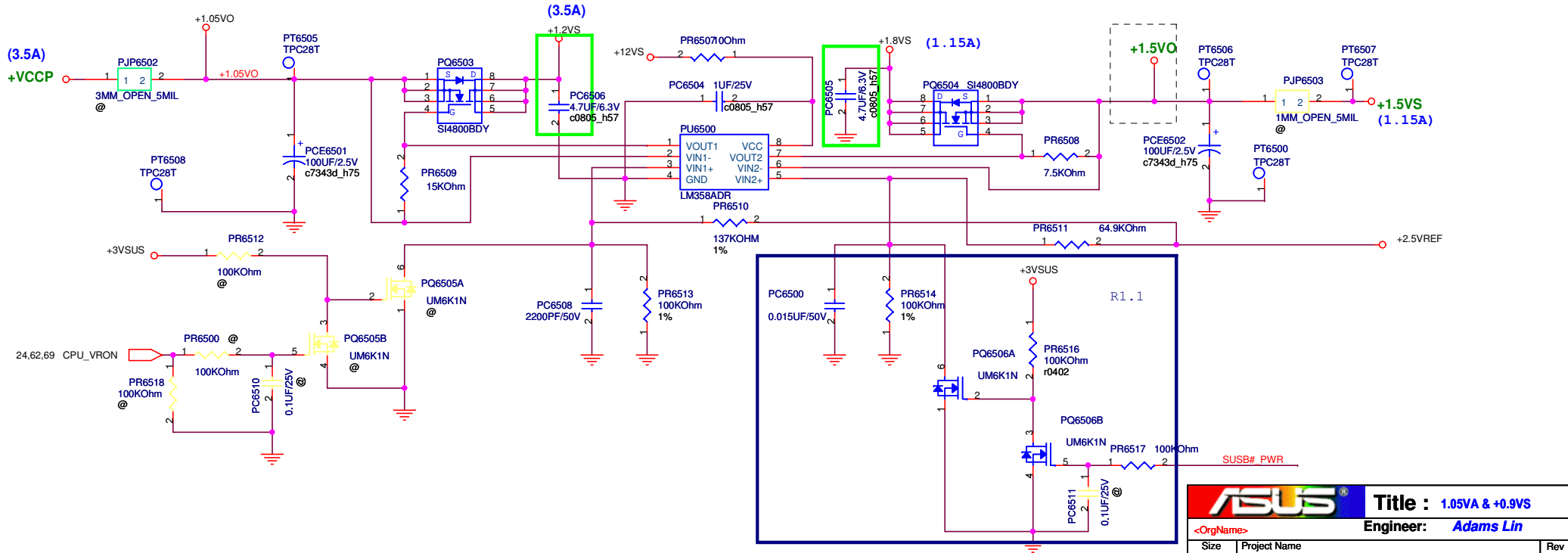
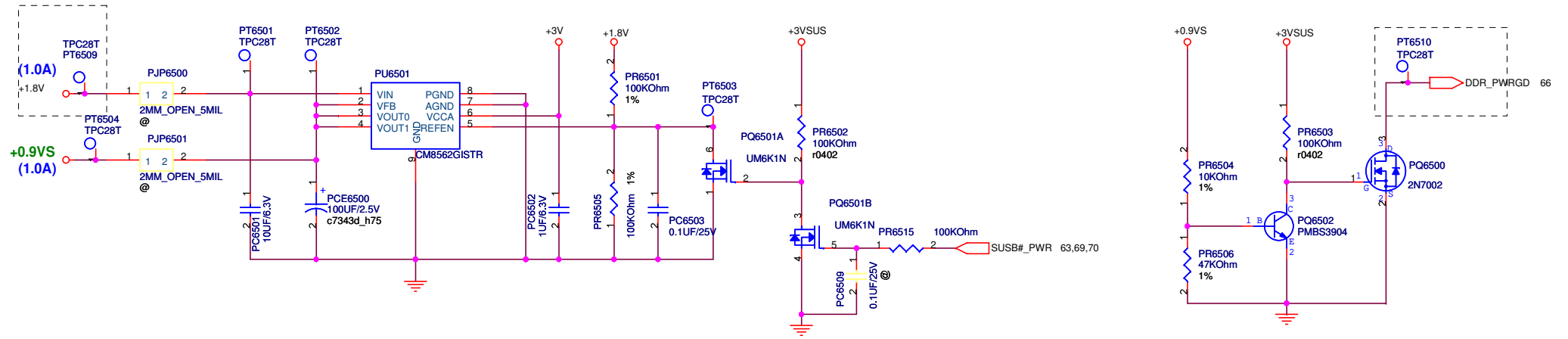
		Title : change list	
ASUSTeK COMPUTER INC		Engineer: Chris_liu,Andy_Guo	
Size Custom	Project Name F5R	Rev 2.0	
Date: 星期五, 十月 11, 2006		Sheet	46 of 71



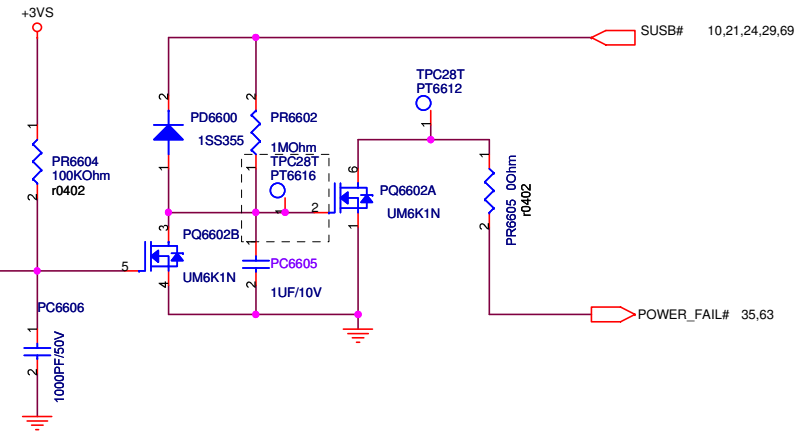
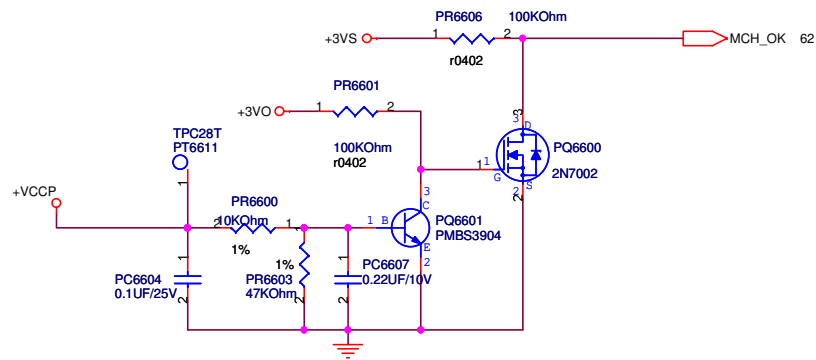
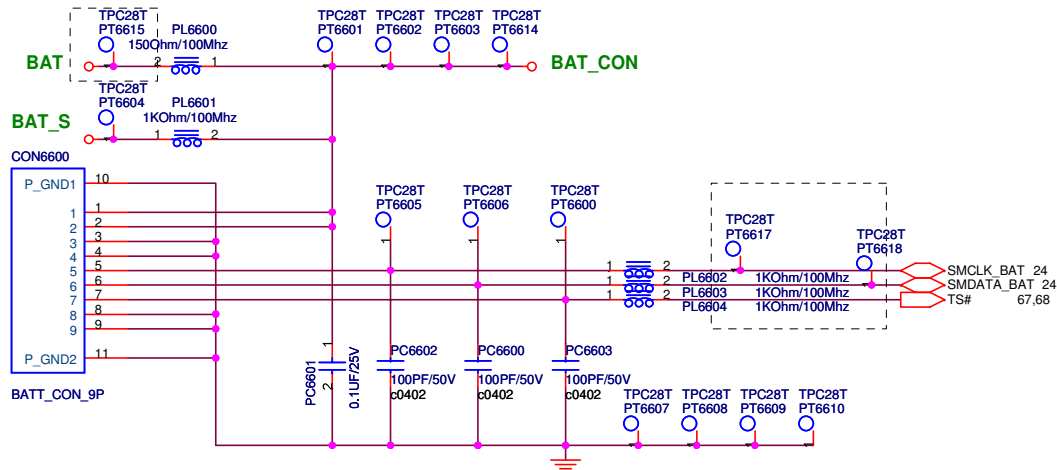
Close to Phase 1 Inductor



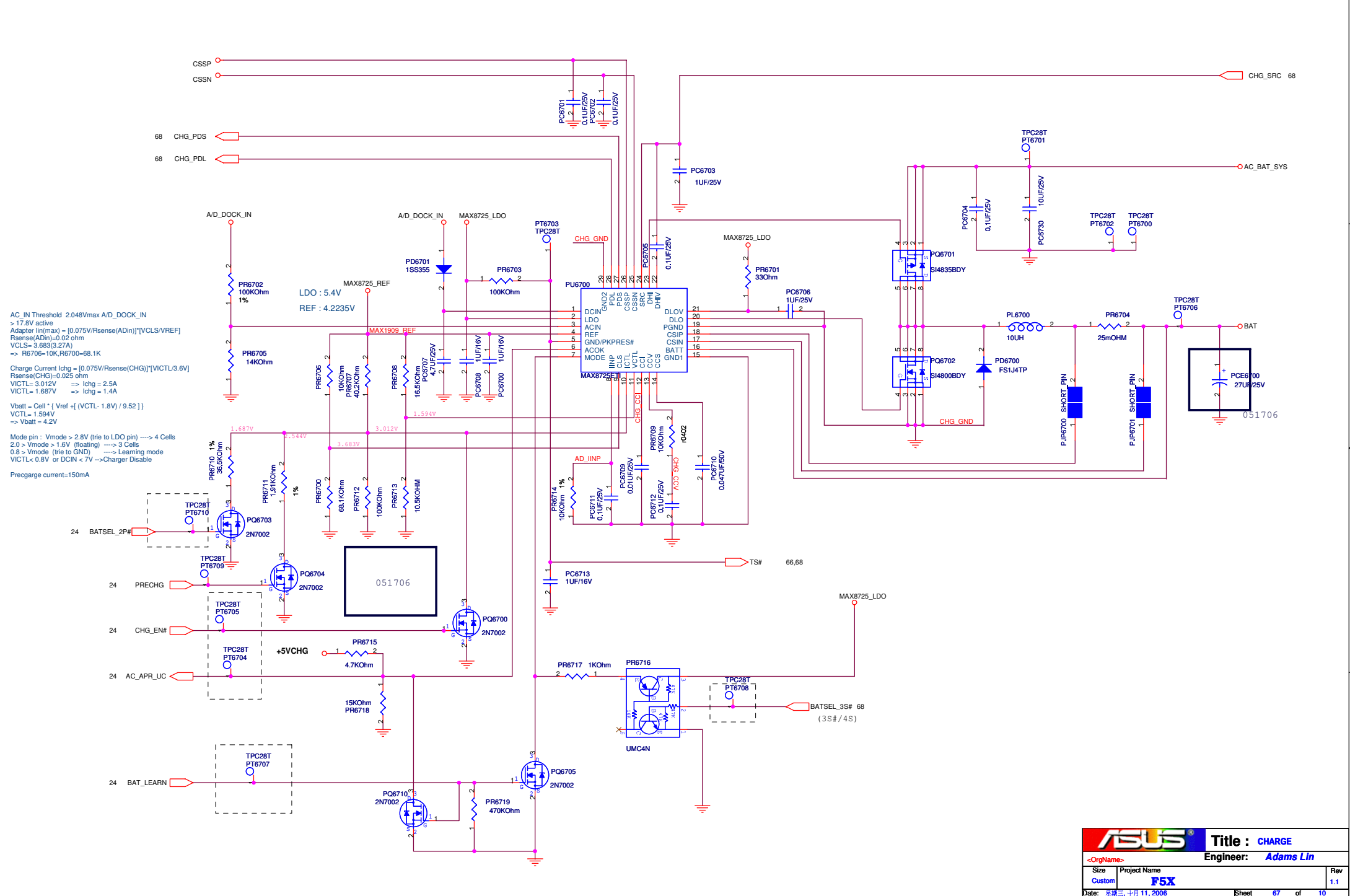




ASUS Title : 1.05VA & +0.9VS
 Engineer: Adams Lin
 Size B Project Name **FSX** Rev 1.1
 Date: 星期三, 十月 11, 2006 Sheet 65 of 10



ASUS		Title : BAT CON/PWOK	
<OrgName>		Engineer: Adams Lin	
Size	Project Name		Rev
B	F5X		1.1
Date:	星期三, 十月 11, 2006		Sheet 66 of 10



AC_IN Threshold 2.048Vmax A/D_DOCK_IN
 > 17.8V active
 Adapter lin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
 Rsense(ADin)=0.02 ohm
 VCLS= 3.683(3.27A)
 => R6706=10K,R6700=68.1K

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
 Rsense(CHG)=0.025 ohm
 VICTL= 3.012V => Ichg = 2.5A
 VICTL= 1.687V => Ichg = 1.4A

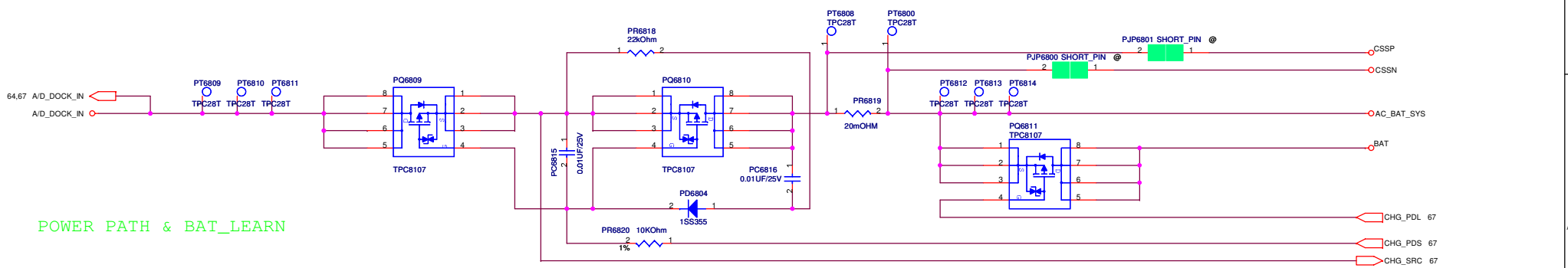
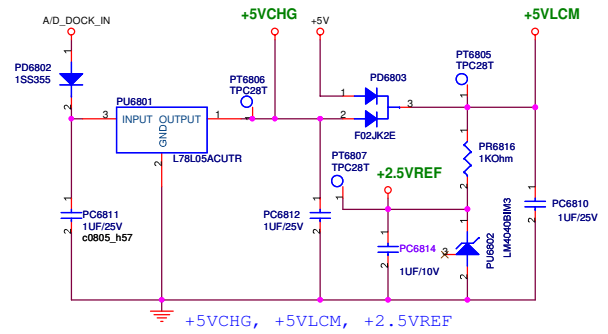
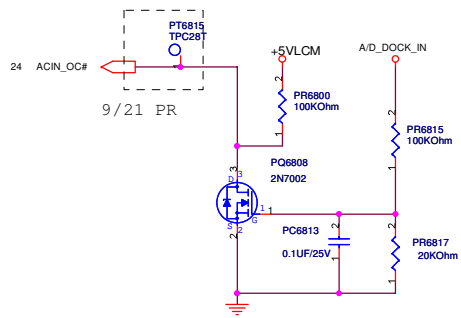
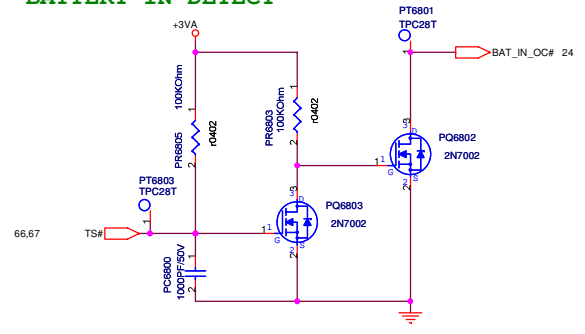
Vbatt = Cell * [Vref + (VCTL - 1.8V) / 9.52]
 VCTL= 1.594V
 => Vbatt = 4.2V

Mode pin : Vmode > 2.8V (try to LDO pin) ----> 4 Cells
 2.0 > Vmode > 1.6V (flucting) ----> 3 Cells
 0.8 > Vmode (try to GND) ----> Learning mode
 VICTL < 0.8V or DCIN < 7V ----> Charger Disable

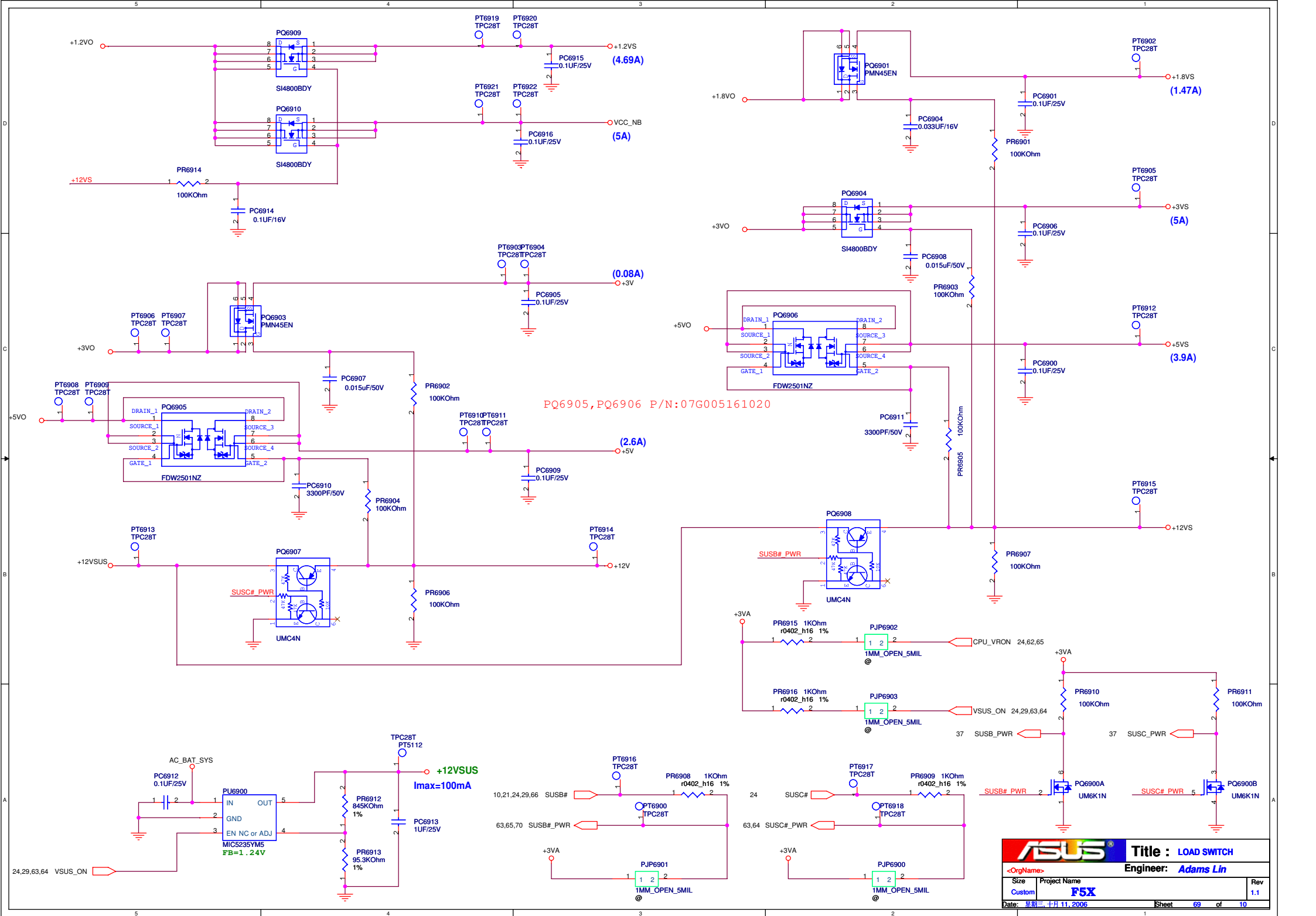
Precharge current=150mA

ASUS		Title : CHARGE
<OrgName>		Engineer: Adams Lin
Size Custom	Project Name FSX	Rev 1.1
Date: 星期三, 十月 11, 2006	Sheet 67	of 10

BATTERY IN DETECT

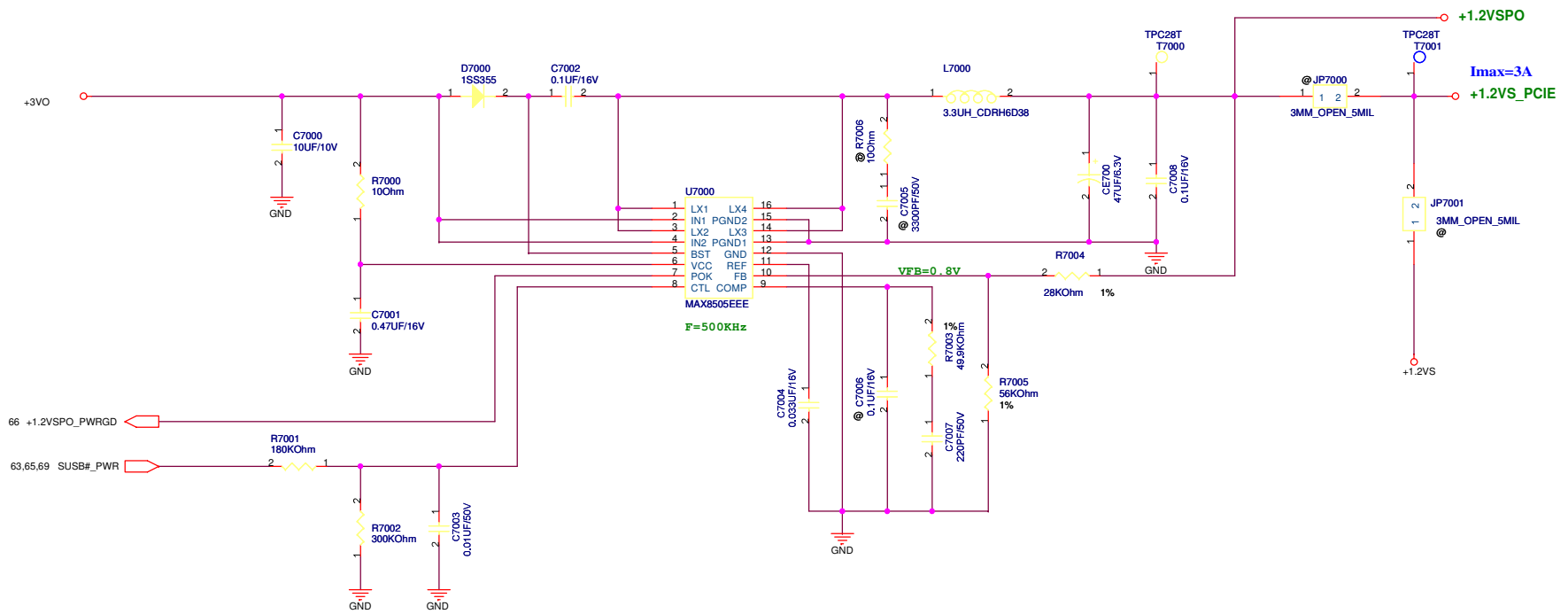


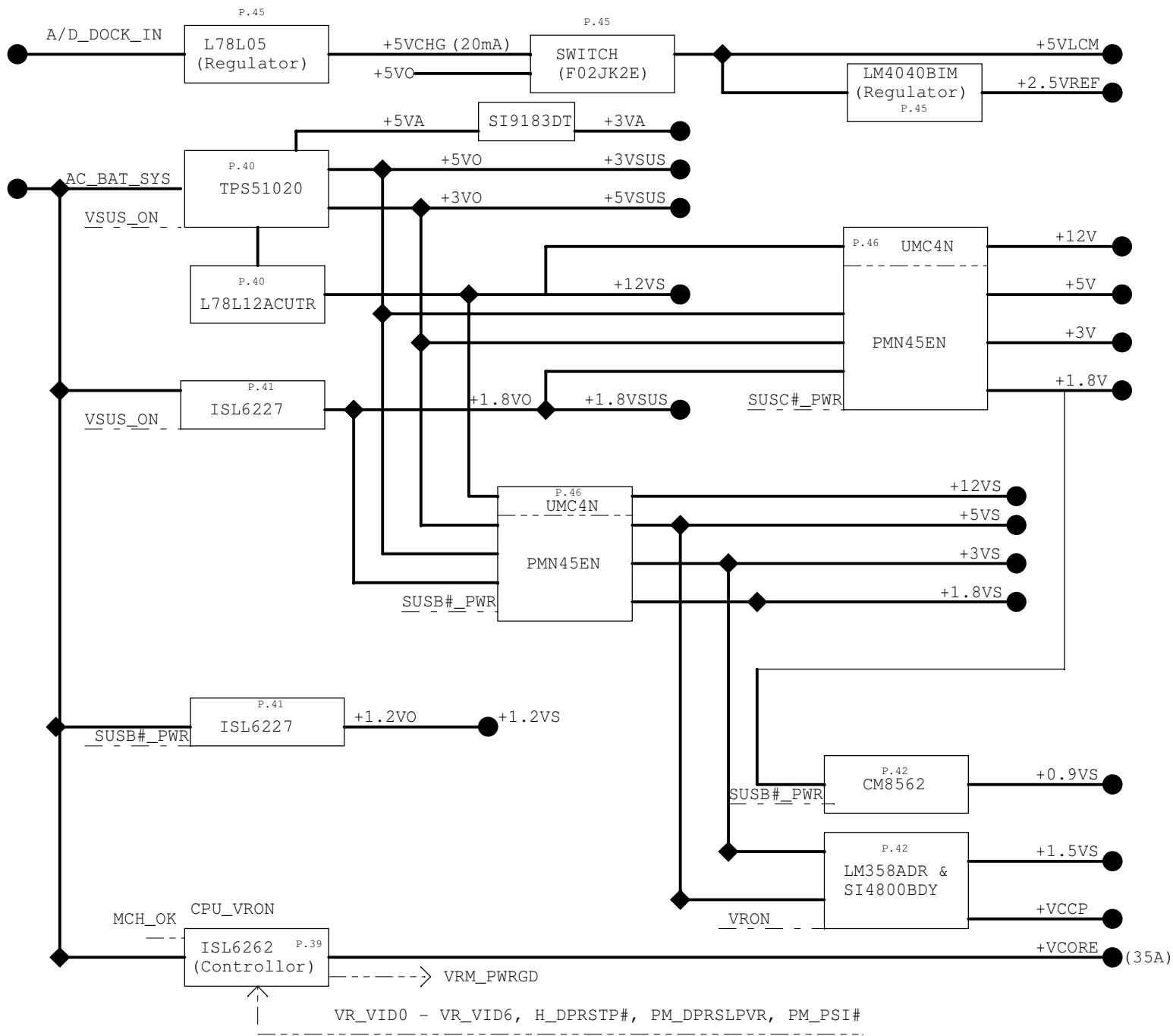
POWER PATH & BAT_LEARN



PQ6905, PQ6906 P/N: 07G005161020

ASUS		Title : LOAD SWITCH	
<OrgName>		Engineer: Adams Lin	
Size	Project Name		Rev
Custom	FSX		1.1
Date: 星期二, 十月 11, 2006		Sheet 69 of 10	





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