Compal Confidential

QBL50 Schematics Document

AMD Sabine

APU Llano / Hudson M2_M3 / Vancouver Whistler

UMA only / PX Muxless with BACO

2011-04-25

Rev:1.0

Security Classification	Compal Secret Data		
Issued Date	2011/03/04	Deciphered Date	2011/12/31

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Title: Cover Page

Size: B | Document Number: QBL50 LA-7551P | Rev: 1.0

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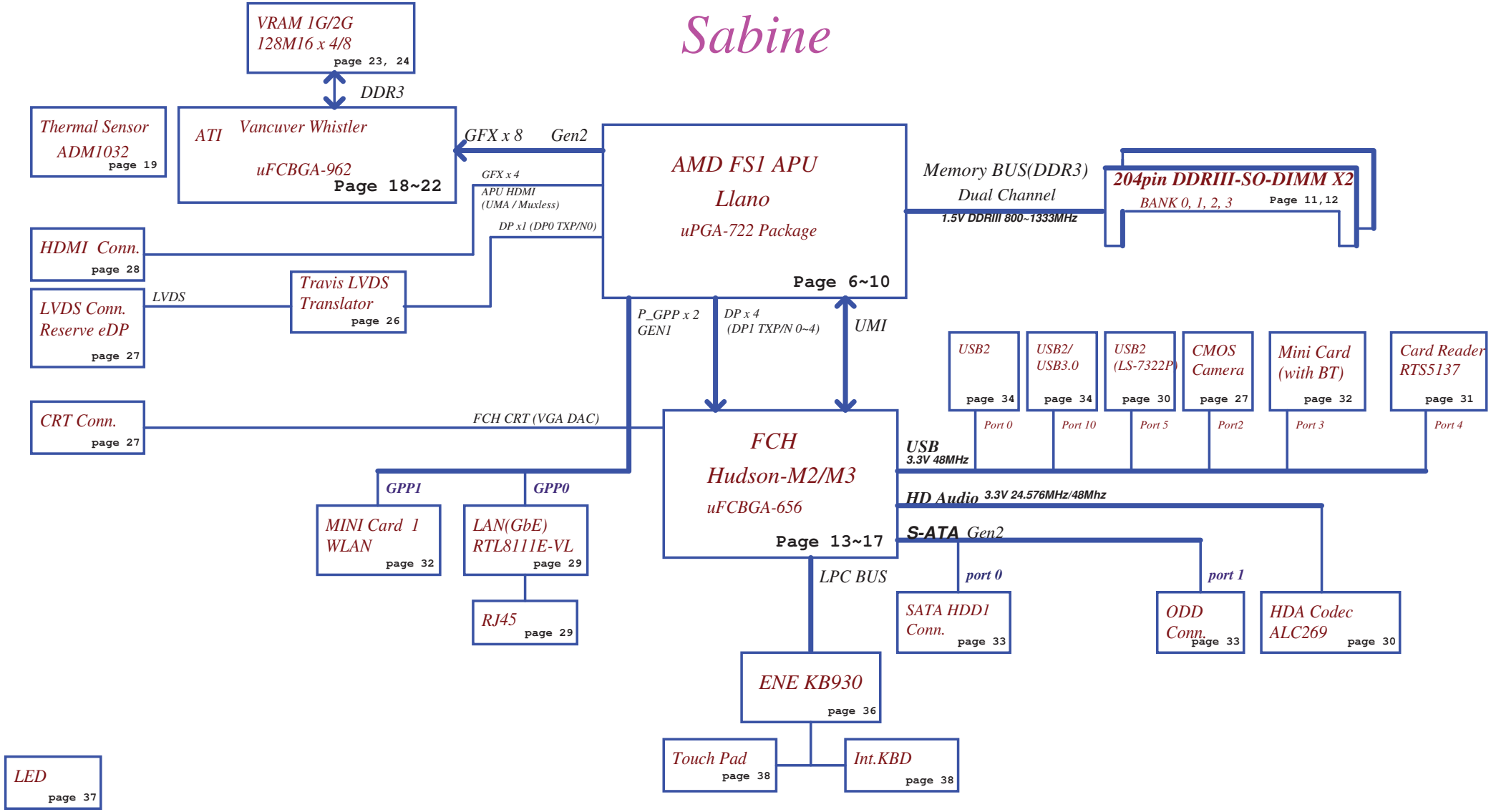
Model Name : QBL50



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Title: Block Diagrams

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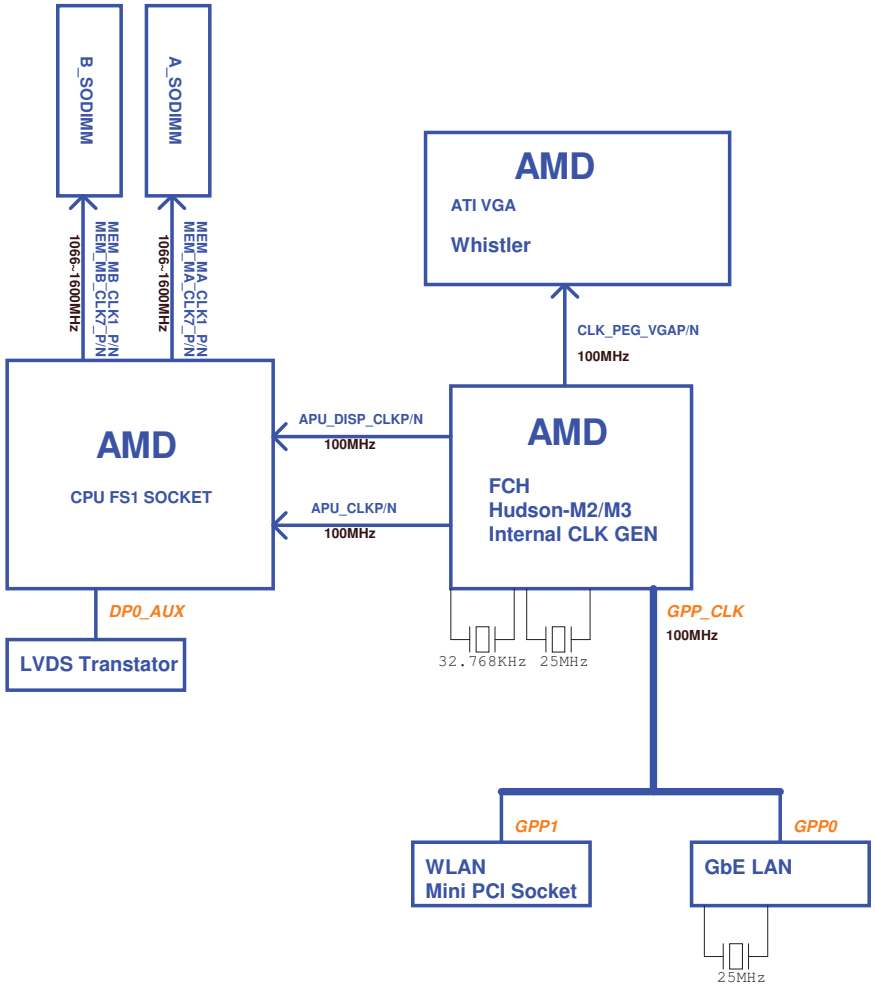
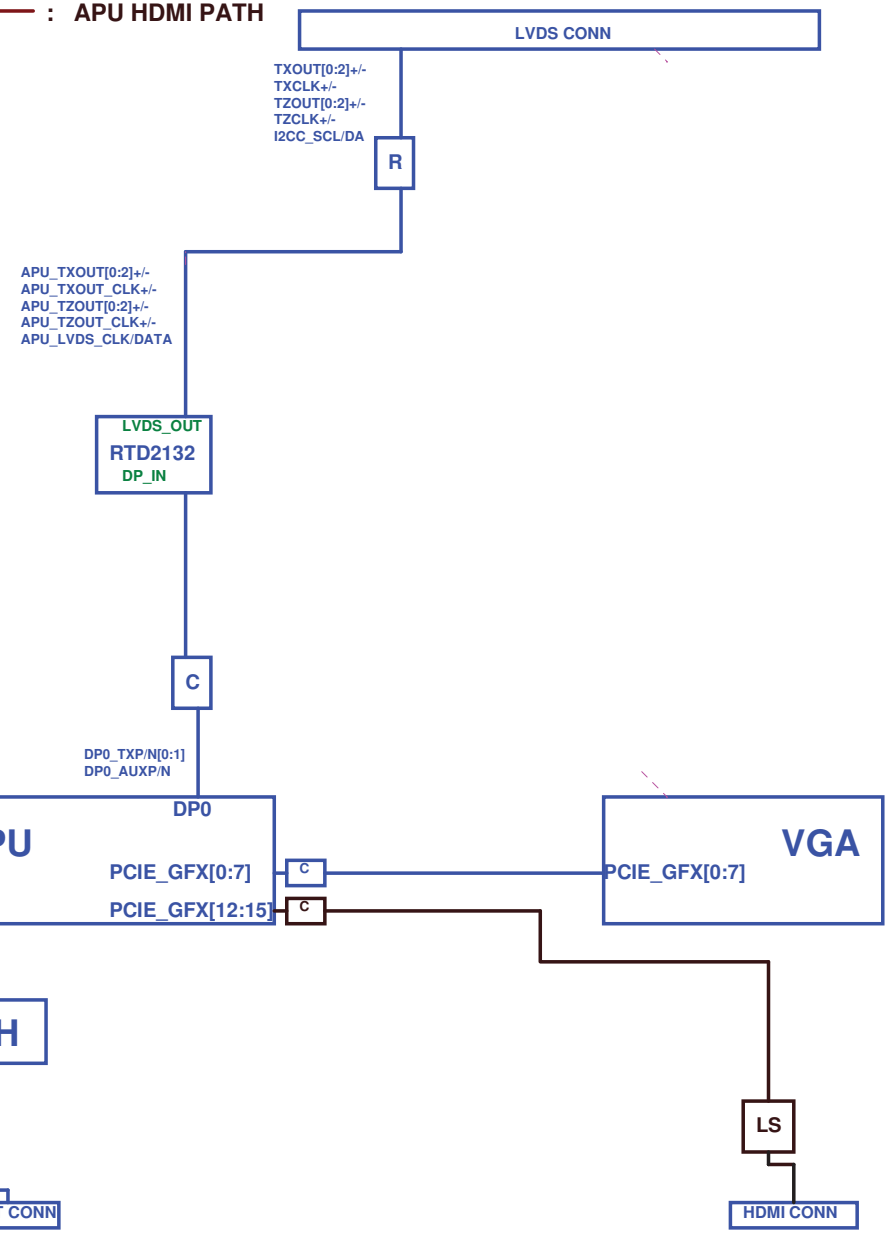
CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION

: LVDS PATH

: APU HDMI PATH



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Title	CLOCK / DISPLAY DISTRIBUTION	
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_IO	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

BOM Structure	BTO Item
VGA@	Use VGA (Mux)
X76@	VRAM ID Table
M2@	Use Hudson-M2
M3@	Use Hudson-M3
USB30@	USB30 on M/B
USB20@	USB20 on M/B

M3@ U25

FCH M3
Part Number = SA000043ID0

BOM Config

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (VGA)	1001 101X b	9AH
(APU)		
RTD2132S (TL)		

FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1101 000X b	D0
DDR DIMM2	1101 001X b	D2

FCH SM Bus 1 address

Device	Address	HEX

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Title: Notes List

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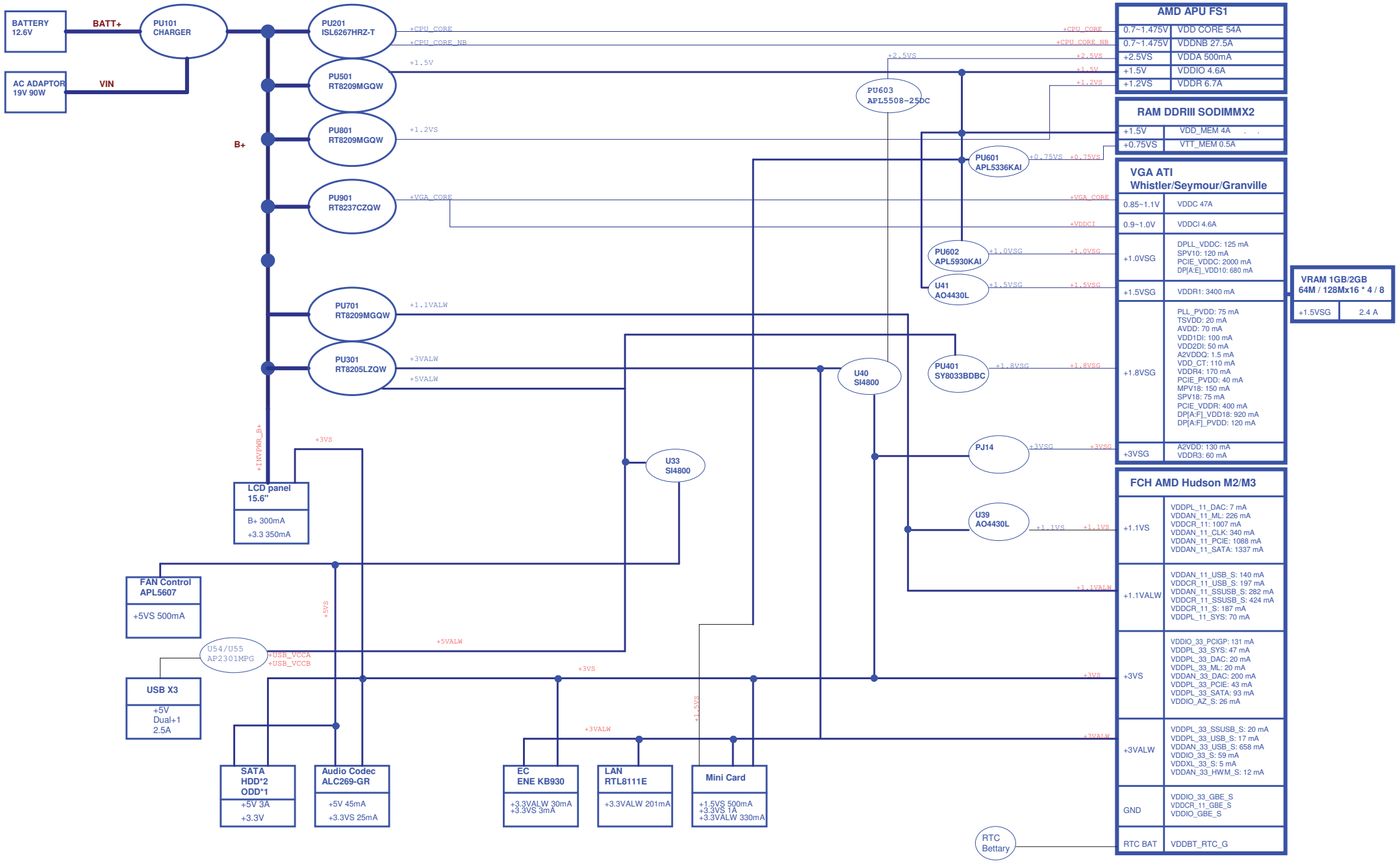
Date: Friday, April 29, 2011 | Sheet 4 of 53



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Title: POWER DELIVERY CHART

Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

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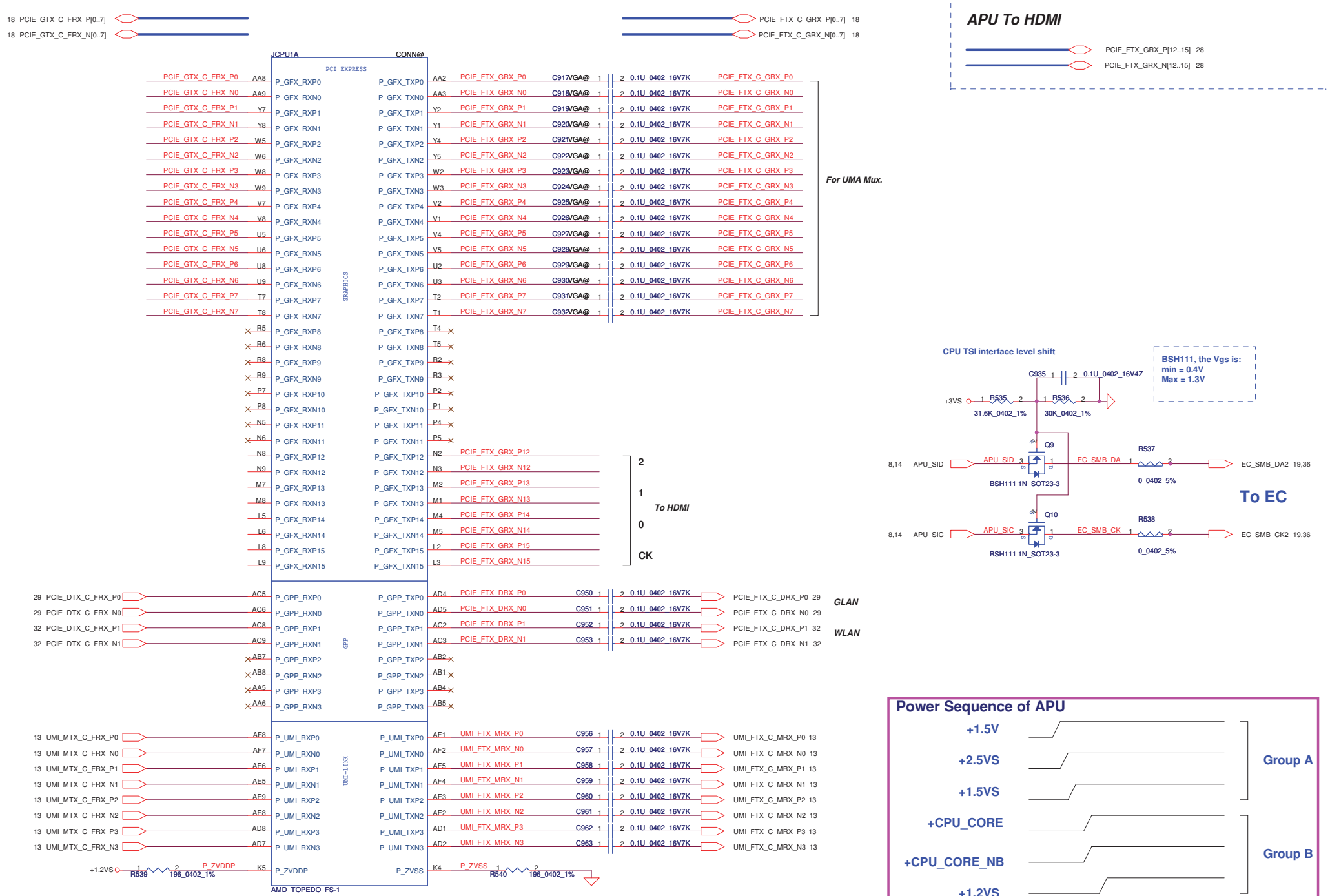

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Compal Electronics, Inc.

Title: AMD FS1 PCIE / UMI / TSI

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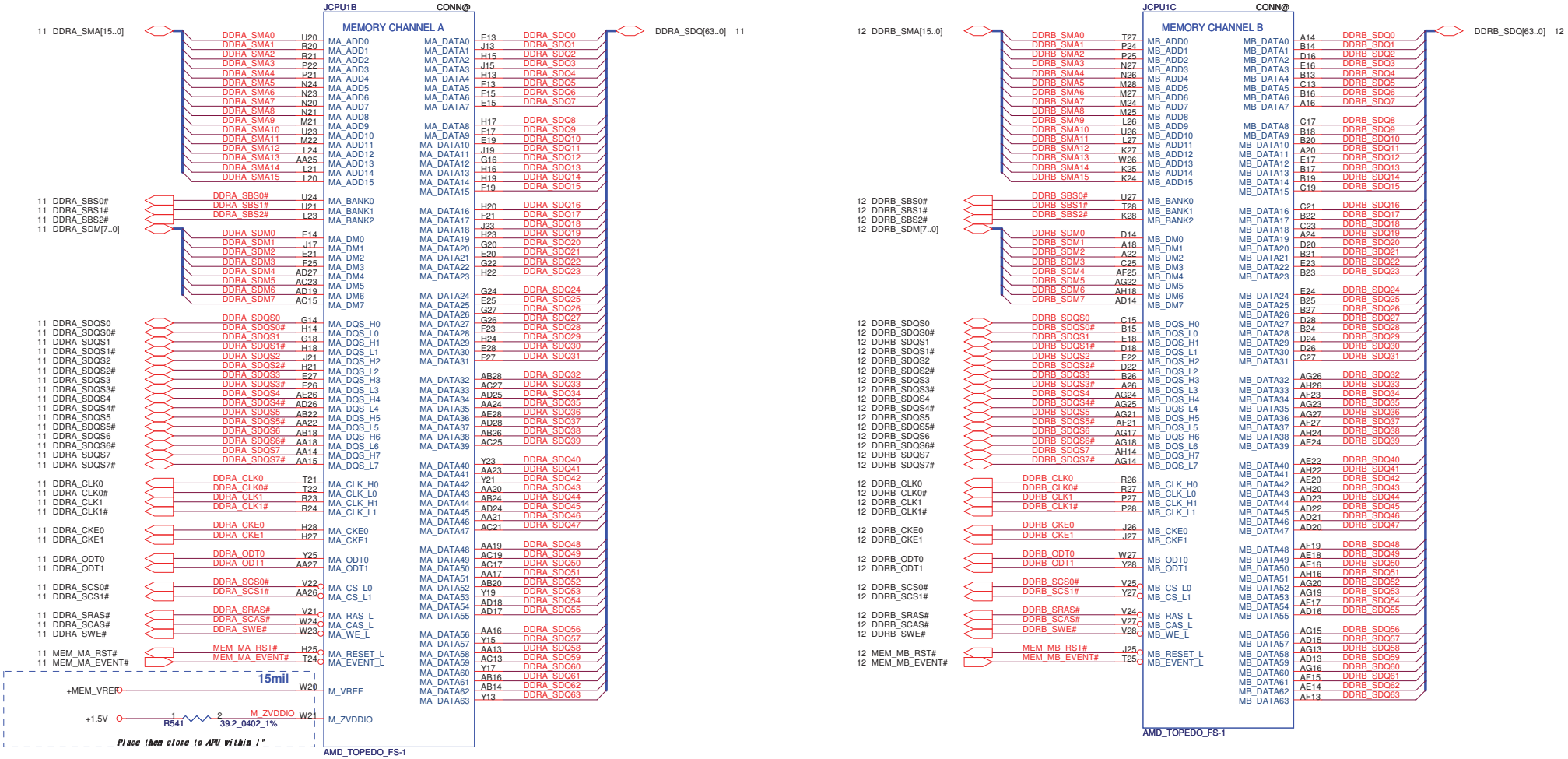
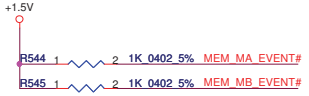
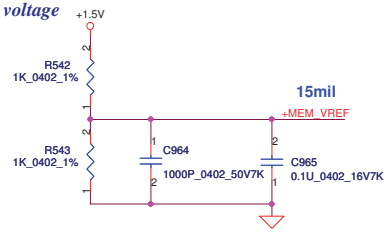


EVENT# pull high



0.75V reference voltage



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Title: AMD FS1 DDRIII I/F

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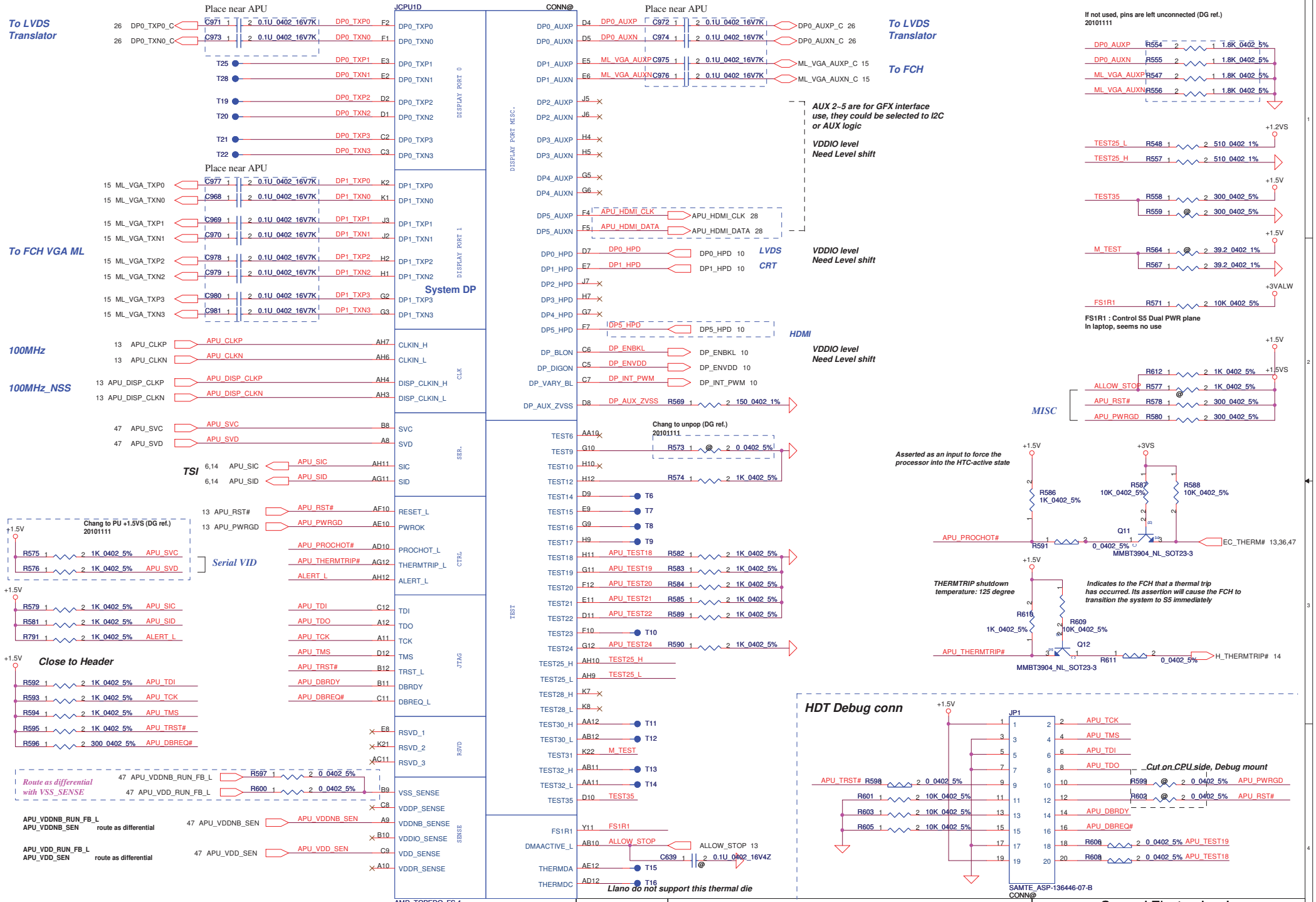

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Title: AMD FS1 Display / MISC / HDT

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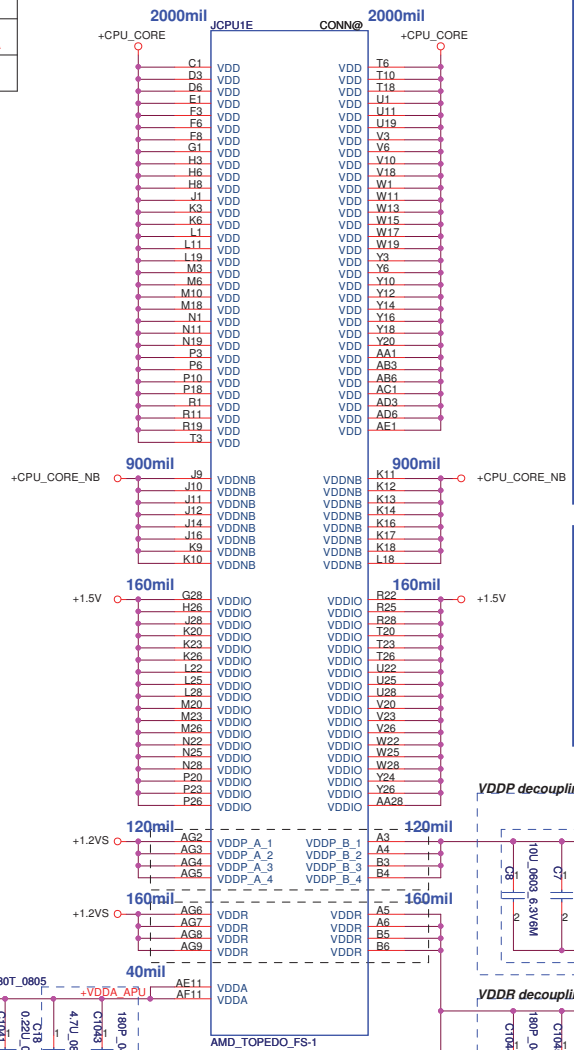
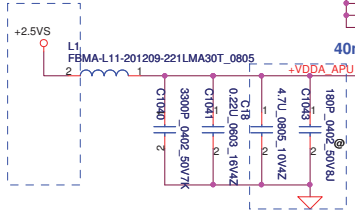
Power Name	Consumption
VDD +CPU_CORE	50A
VDDNB +CPU_CORE_NB	22.5A
VDDIO +1.5V	4A
VDDP / VDDR +1.2VS	3A / 3.5A
VDDA +2.5VS	0.75A

CORE_NB	CPU_CORE
330uF X 2	330uF X 4
22uF X 4	22uF X 11



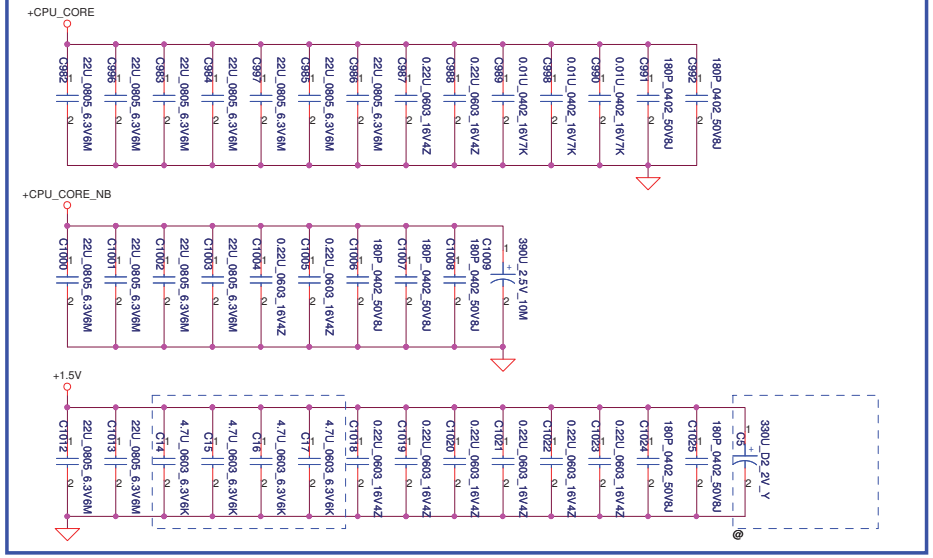
Keep trace from resistor to APU within 0.6"

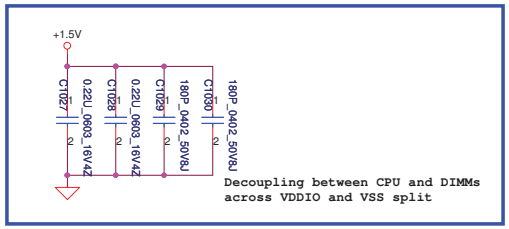
Keep trace from Caps to APU within 1.2"

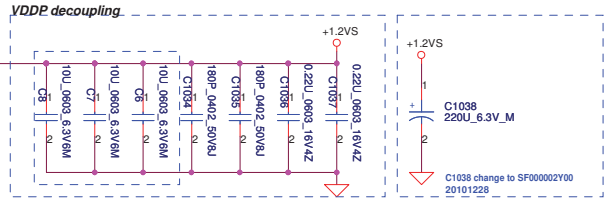


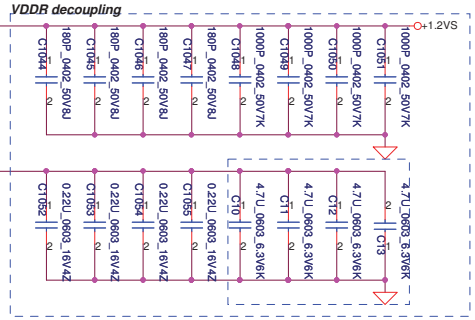
C18 & C1043 follow AMD request 201012061900

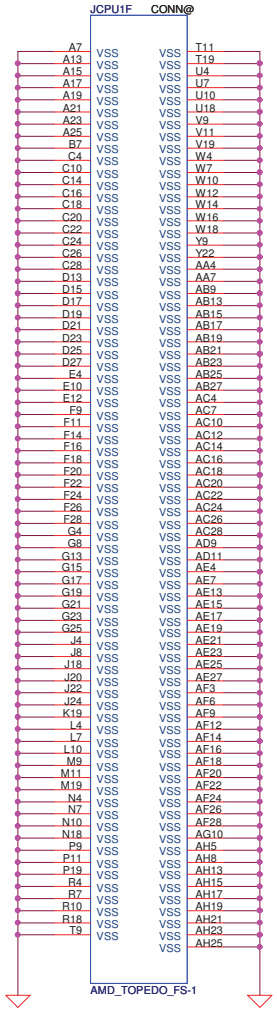
CPU BOTTOM SIDE DECOUPLING











Demo Board Capacitor (include PWM side)

CPU_CORE	CORE_NB	VDDIO_SUS (CPU side)	VDDIO_SUS (DIMM x2)	VDDP/R_PWM	VDDP	VDDR
470uF x 6	470uF x 4	680uF x 1	100uF x 4	470uF x 2	10uF x 3	4.7uF x 4
22uF x 9	22uF x 6	330uF x 1	0.1uF	10uF x 1	0.22uF x 2	0.22uF x 4
0.22uF x 2	0.22uF x 2	22uF x 3			180pF x 2	1nF x 4
180pF x 2	180uF x 3	4.7uF x 4				180pF x 4
10nF x 3		0.22uF x 6				
		180pF x 4				

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Title: AMD FS1 PWR / GND

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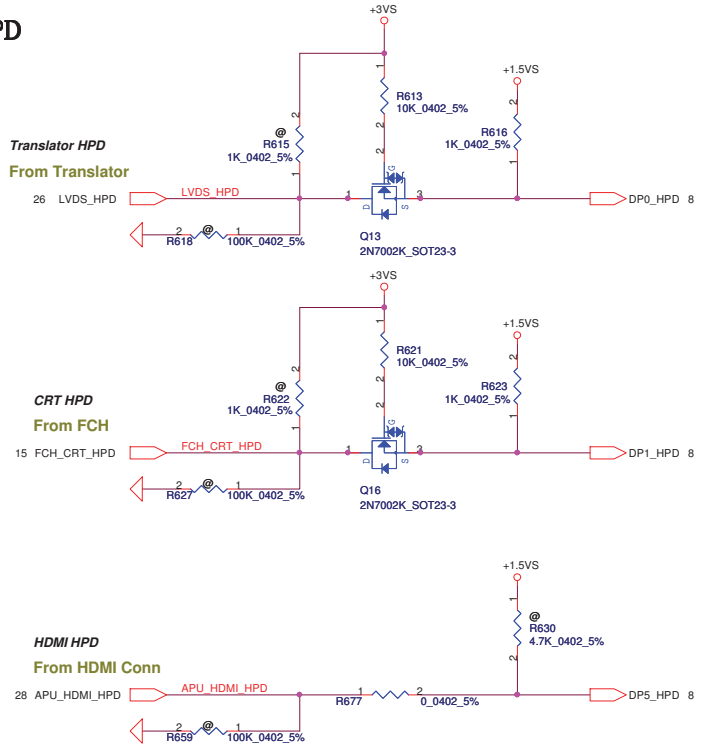
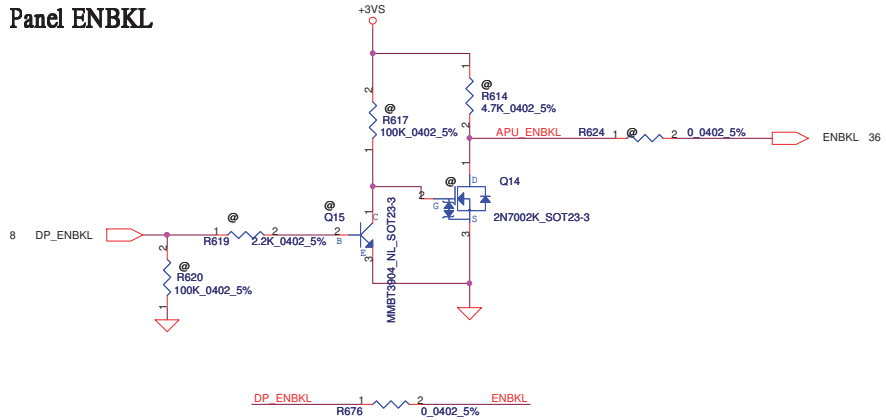
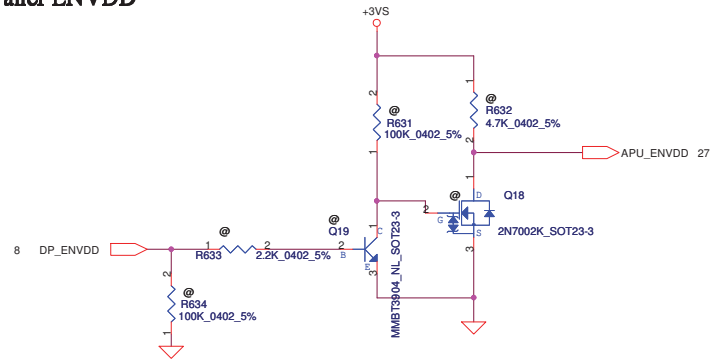
HPD



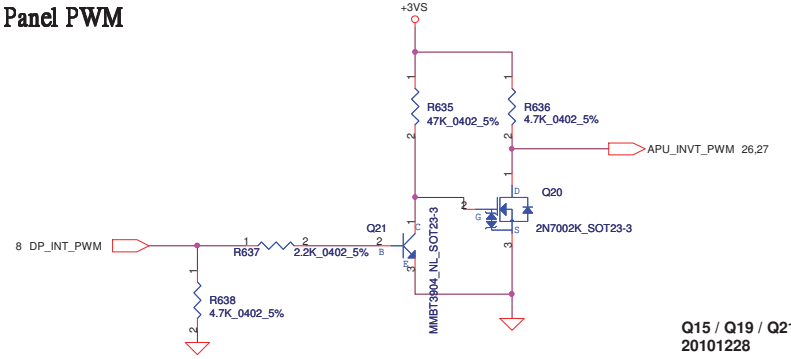
Panel ENBKL



Panel ENVDD



Panel PWM



Q15 / Q19 / Q21 change to SB000006A00
20101228

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Title: AMD FS1 Singal Level Shifter

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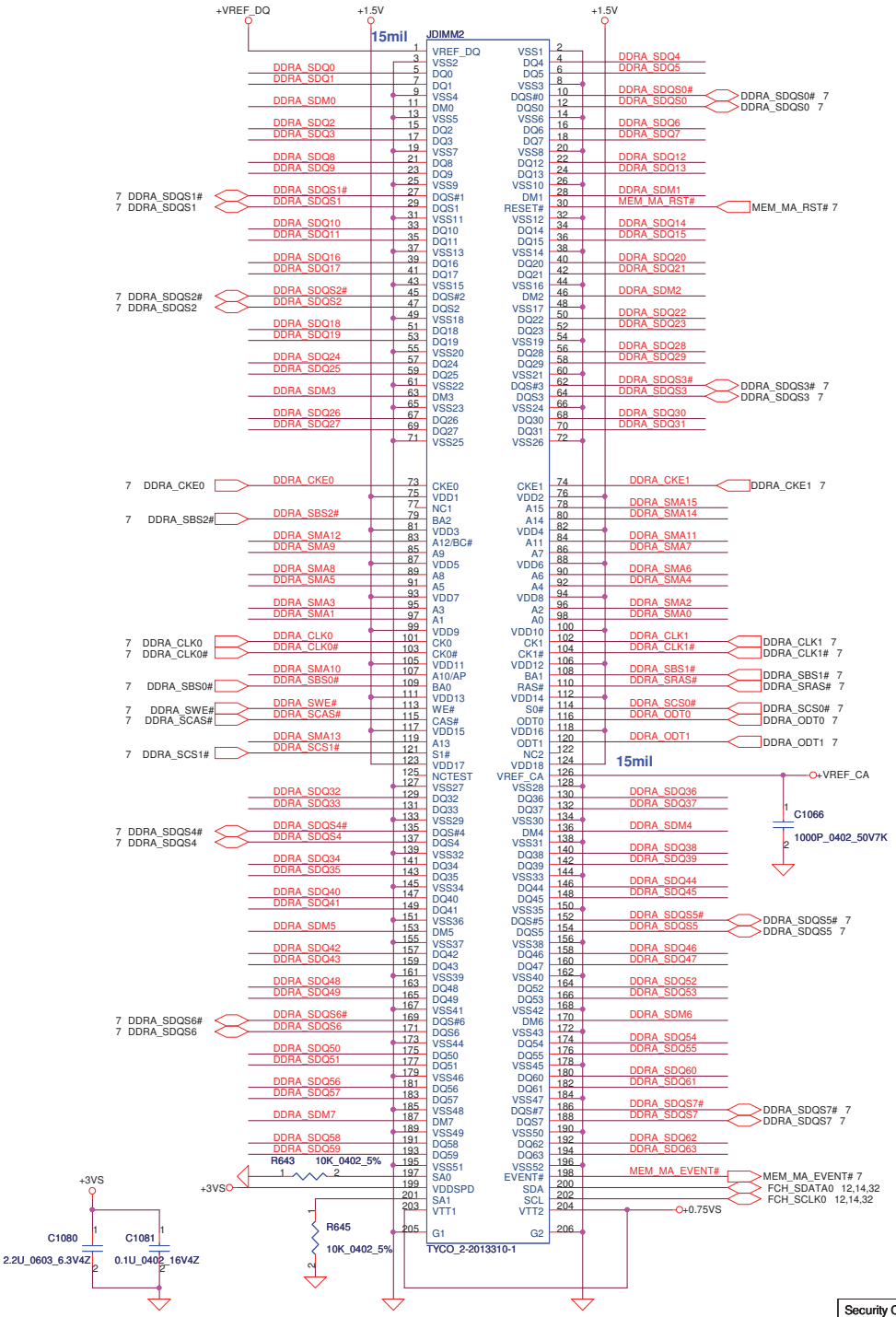
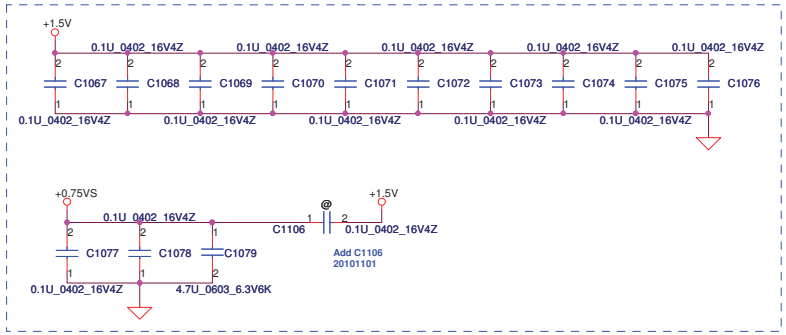
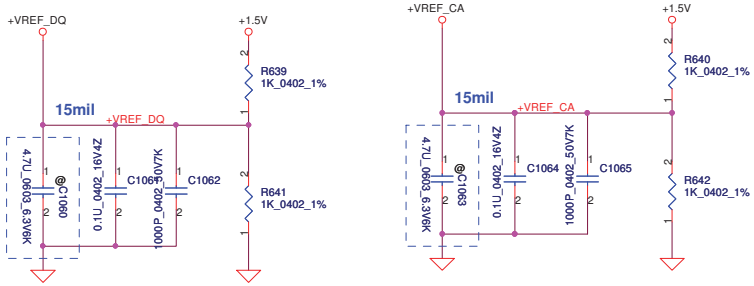


Place near DIMM1





DIMM_A STD H:9.2mm

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Title: DDRIII SO-DIMM 1

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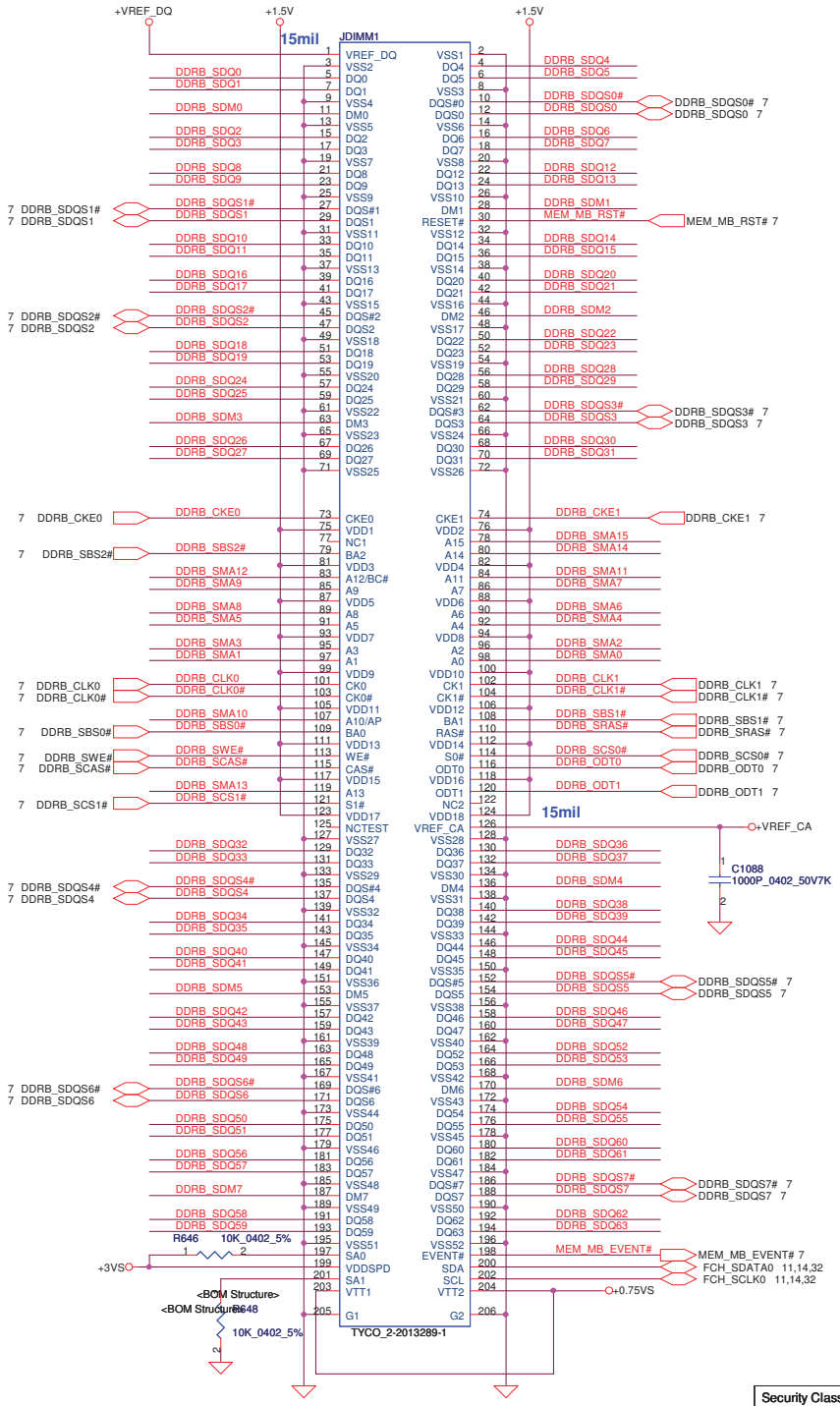

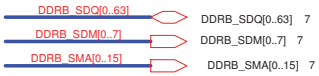

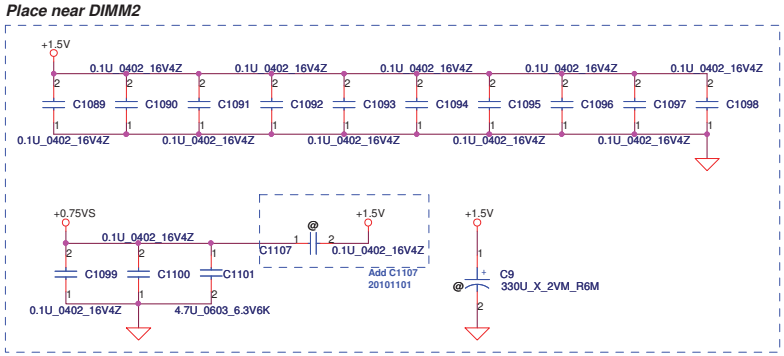

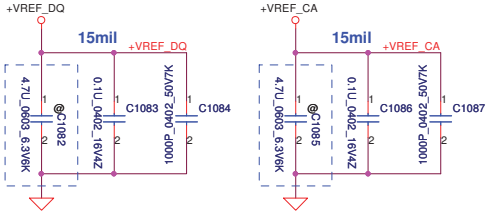

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Title: DDRIII SO-DIMM 2

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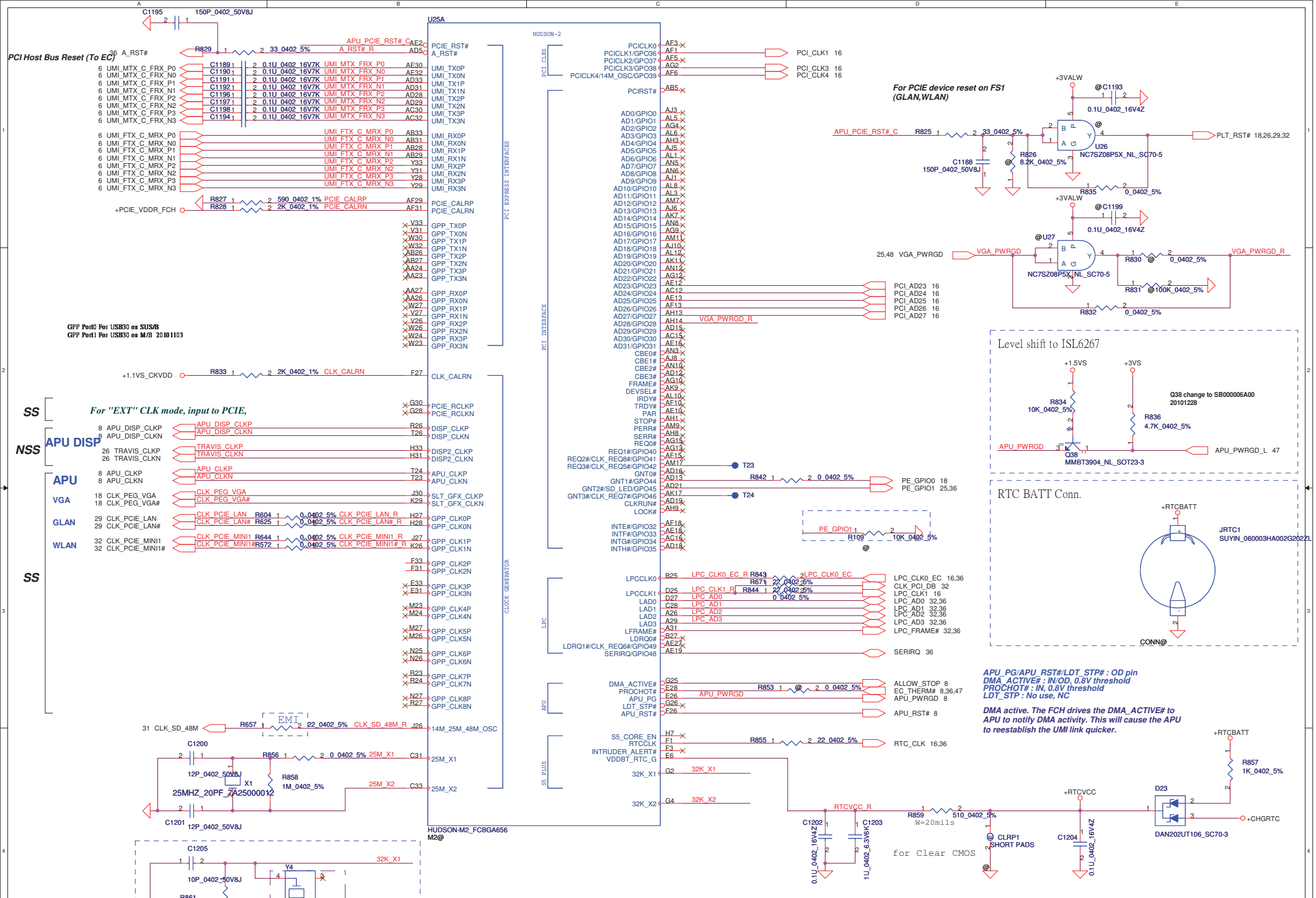

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Compal Electronics, Inc.

Title: Hudson-M2/M3-UMI/PCI/CLOCK/LPC/RTC

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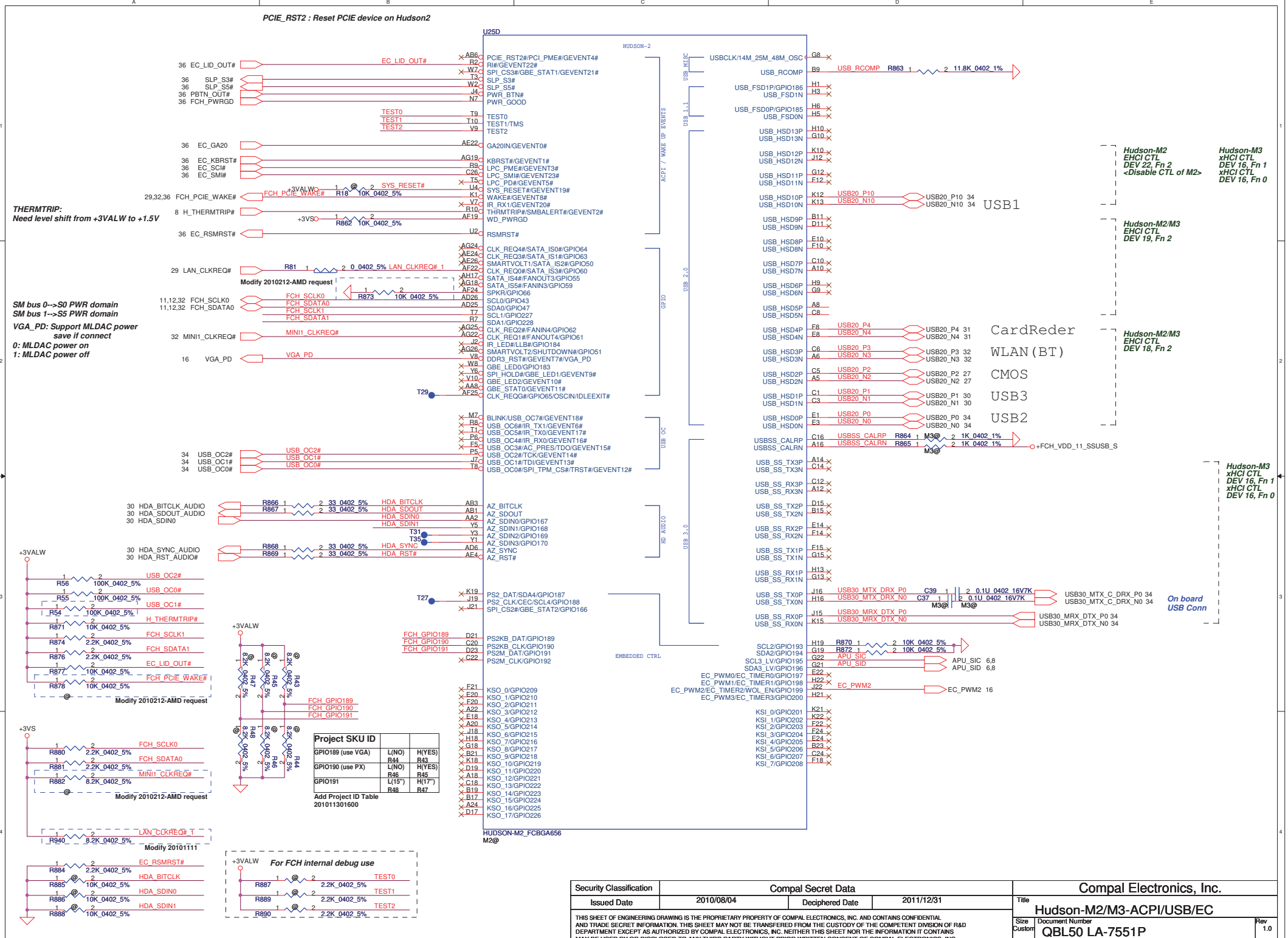

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Compal Electronics, Inc.

Title: Hudson-M2/M3-ACPI/USB/EC

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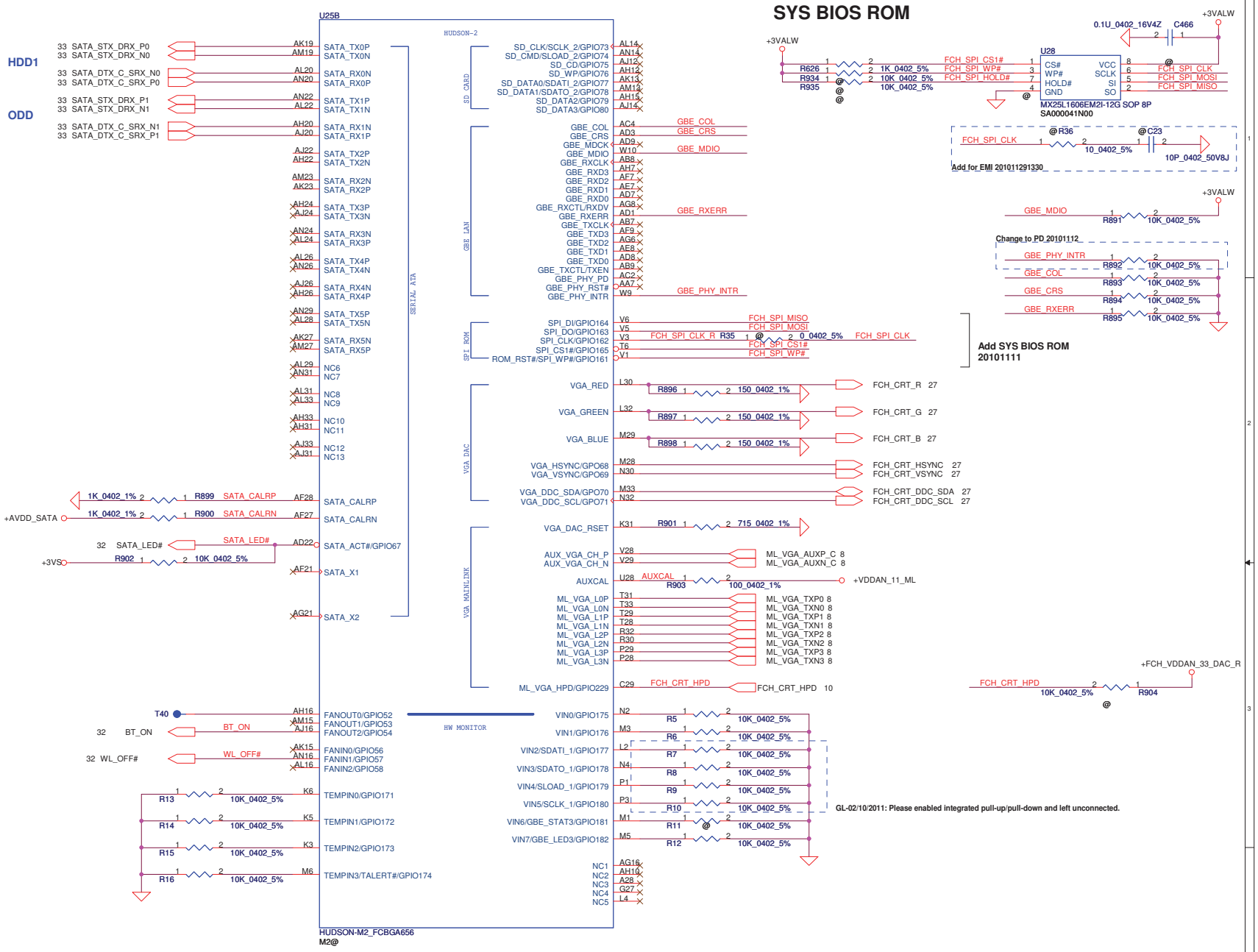
SYS BIOS ROM



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Compal Electronics, Inc.

Title: Hudson-M2/M3-SATA/GBE/HWM

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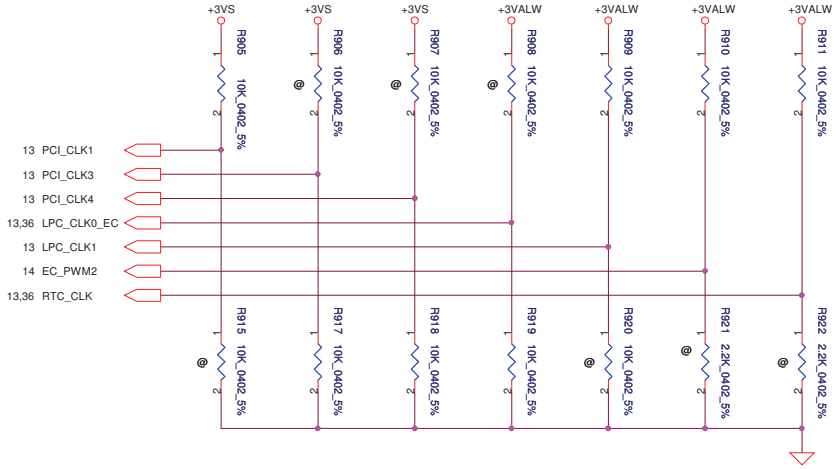
STRAP PINS

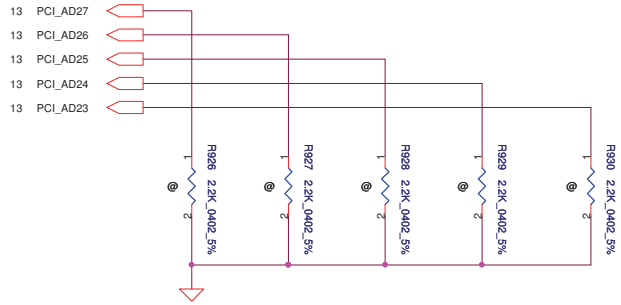
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM	S5 PLUS MODE ENABLED

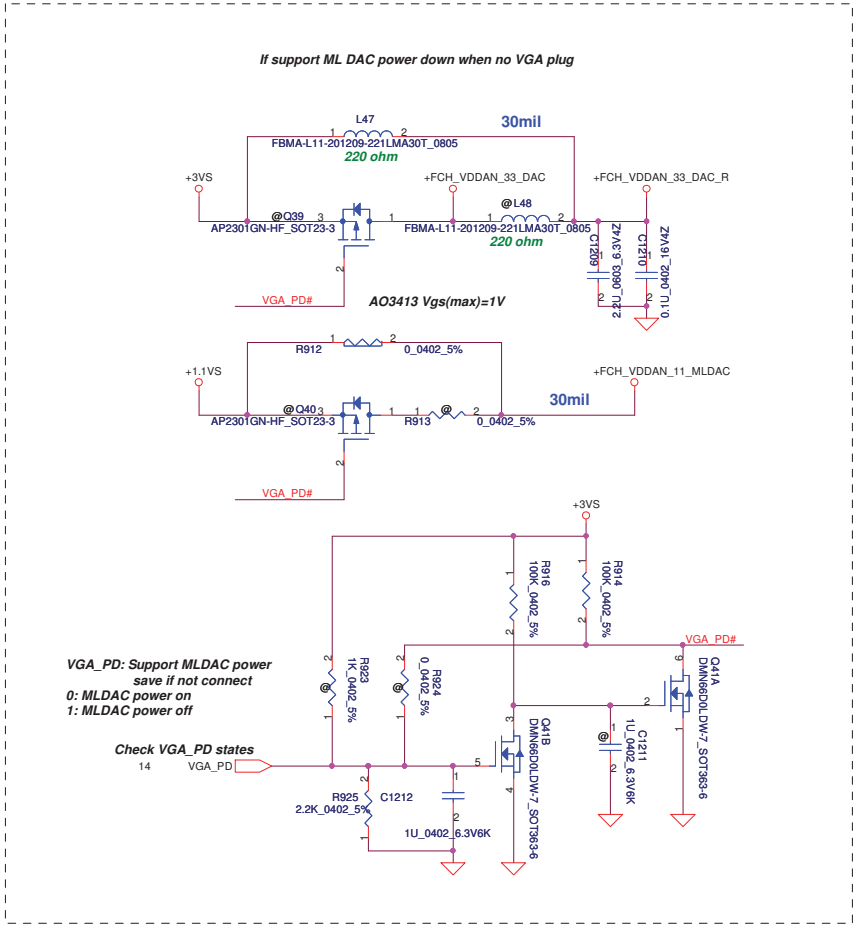


DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PCI_AD26	PCI_AD27		PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





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Compal Electronics, Inc.

Title: Hudson-M2/M3-STRAP

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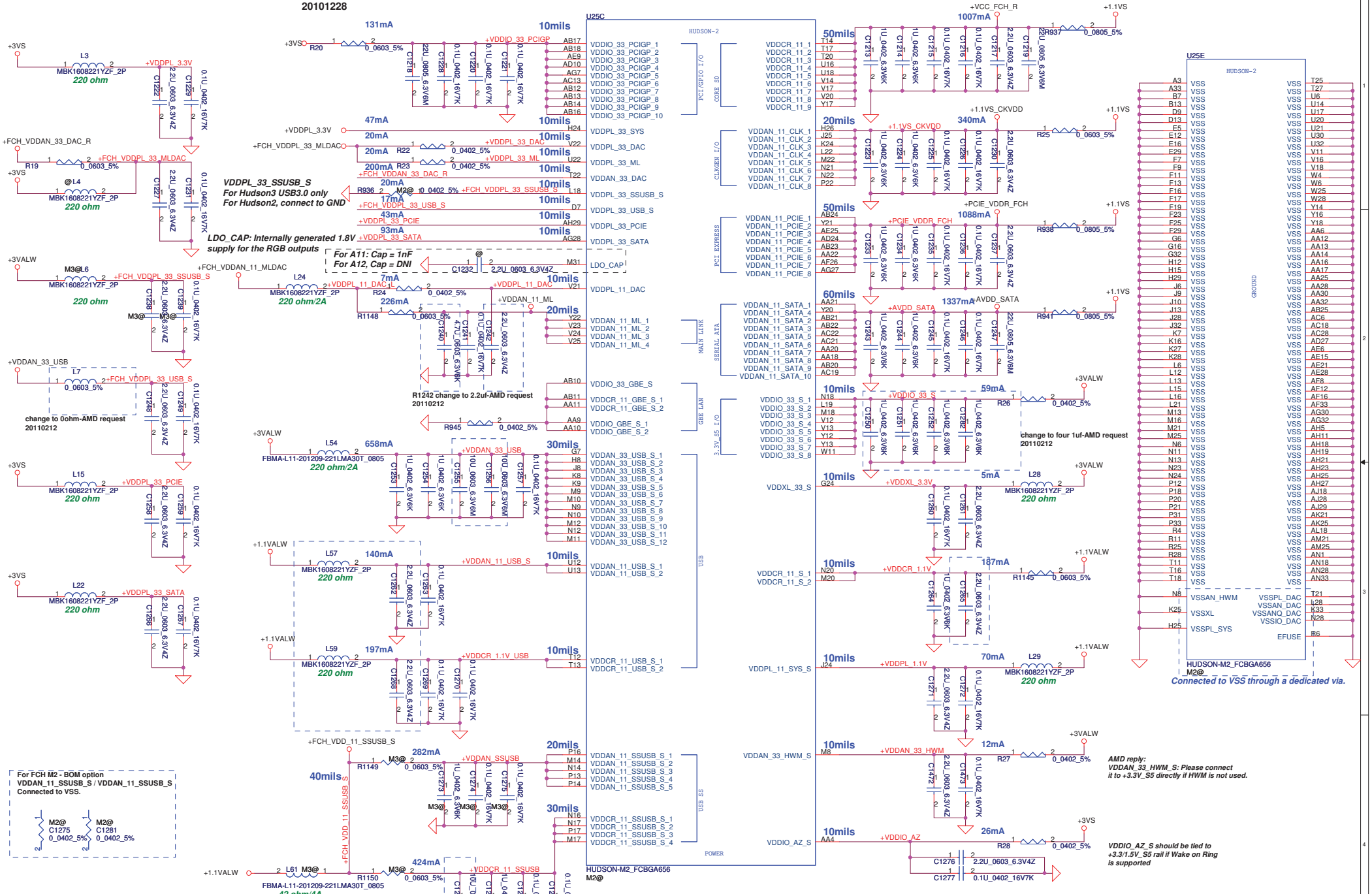
C1218 / C1219 / C1247 Change to SE00000I10
20101228



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Compal Electronics, Inc.

Title: Hudson-M2/M3-POWER/GND

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GFX PCIE LANE REVERSAL

<DIGON>
Controls panel digital power on/off.
Active High ,external PD need

<VARY_BL>
LCD PWM (pulse width modulated)
output to adjust LCD brightness
Active High ,external PD need

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Compal Electronics, Inc.

Title: Vancouver_ PCIE / LVDS

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Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis diabled 1: Tx de-emphasis enabled	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : (Internal PD) a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 * 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device (Internal PD) 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	00
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this strap on Whistler and Seymour

NC on Park, Robson and Seymour
NC on Park, Robson

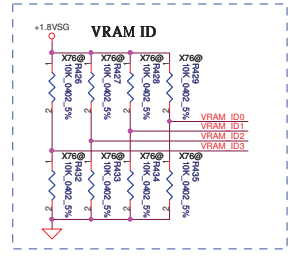
NC on Park, Robson and Seymour

Global Swap Lock on Multiple GPUs

NC on Park, Robson and Seymour

Not share via for other GND

VRAM ID



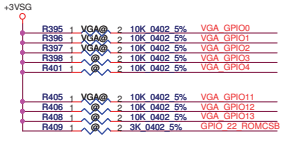
GPIO5 fast-power reduction:
HW control will casue display disturb
should use SW method control
GPIO6 voltage control signal ,No use can NC

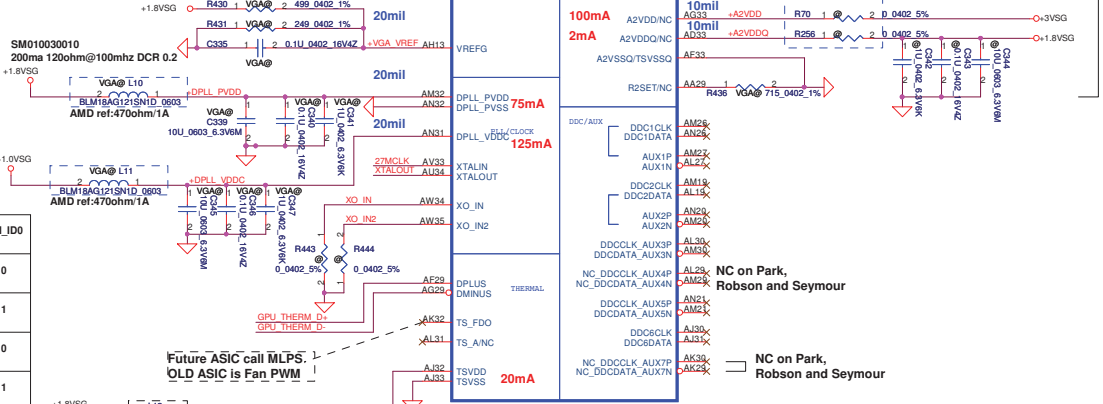
Move to DDCCLK_AUX3P,DDCDATA_AUX3N,

GPIO7 Controls backlight on/off.
Active High ,need external PD
If GPIO22 High ,GPIO 11-13->CFG[0:2]
Config ROM type ,GPU has internal PD

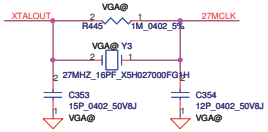
GPIO6,15,16,20
Voltage control signal
GPIO6,15 no use can NC
Thermal monitor interrupt
Critical temperature fault
Reserved

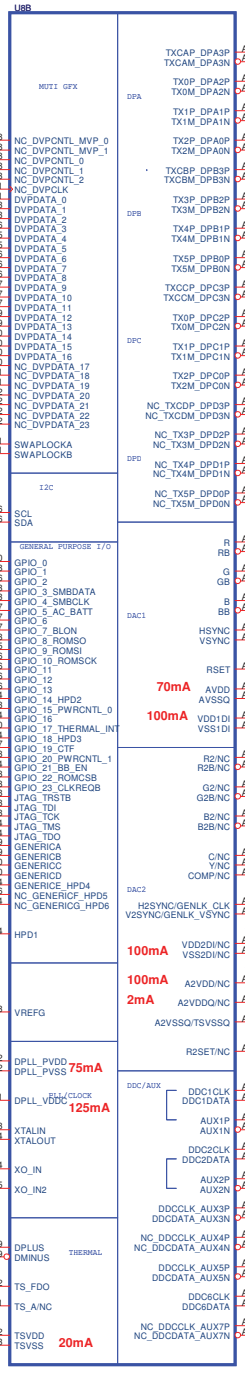
External BIOS device
ON(1)/OFF(0) inter PD
Internal Debug
no use can floating
ON(1)/OFF(0)
Stereo Sync
no use can NC
For ATI Cross fire
no use can NC

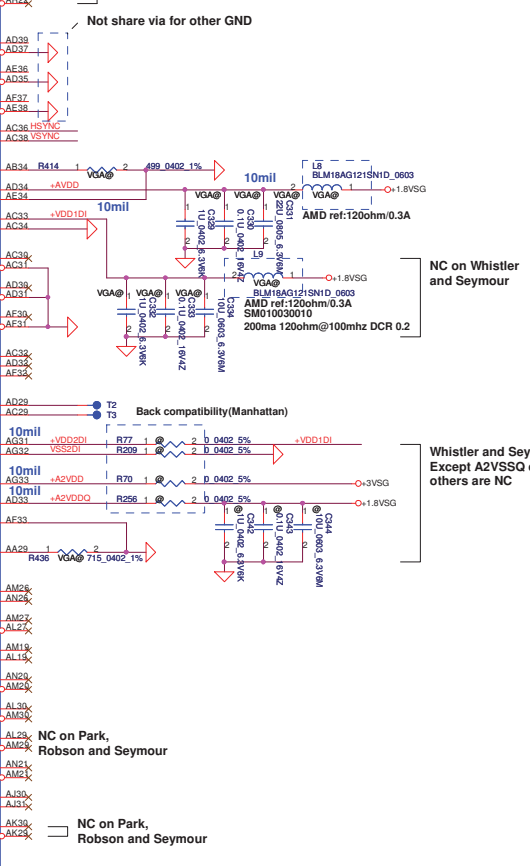




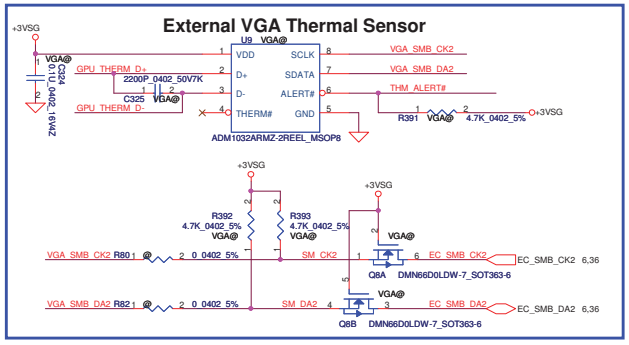
VRAM \ Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung SA00004G530 64M16x8 K4W1G1646G-BC11	0	0	0	0
Samsung SA00004TQA0 128M16x8 K4W2G1646C-HC11	0	0	0	1
Hynix SA00041S60 64M16x8 H5TQ1G63DFR-11C	0	1	0	0
Hynix SA00003YO30 128M16x8 H5TQ2G63BFR-11C	0	1	0	1



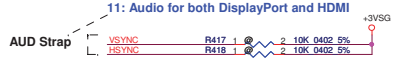




External VGA Thermal Sensor



HSYNC:VSYNC
11: Audio for both DisplayPort and HDMI



GPIO8 Serial-ROM output from ROM GPIO9 Serial-ROM input to ROM. GPIO10 Serial-ROM clock to ROM. GPIO22 erternal BIOS-ROM enable	if GPIO22 High ,GPIO 11-13->CFG[0:2] Config ROM type ,GPU has internal PD if GPIO22 Low ,GPIO 11-13->CFG[0:2] Config Primary memory-aperture size CFG[3:0] 128MB 000 256MB 001 * 64MB 010
GPIO8,GPIO9,GPIO10 no use can NC GPIO22 Enable need 3K PH ,no use must NC	

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Compal Electronics, Inc.

Title: Vancouver_Strape/DP/HDMI//CRT

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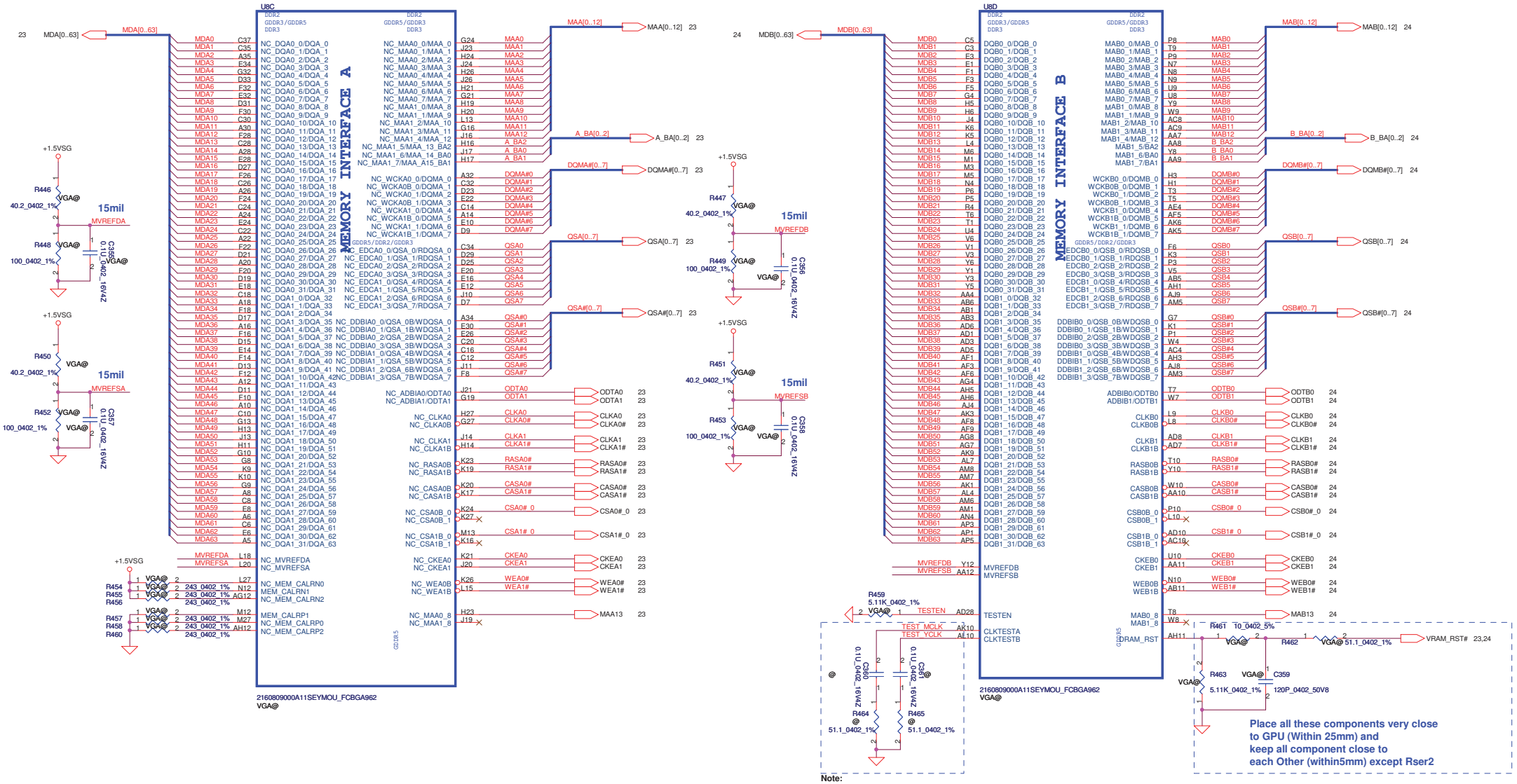

Park&Seymour is single channel for memory (channel B only)

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Compal Electronics, Inc.

Title: Vancouver_Memory

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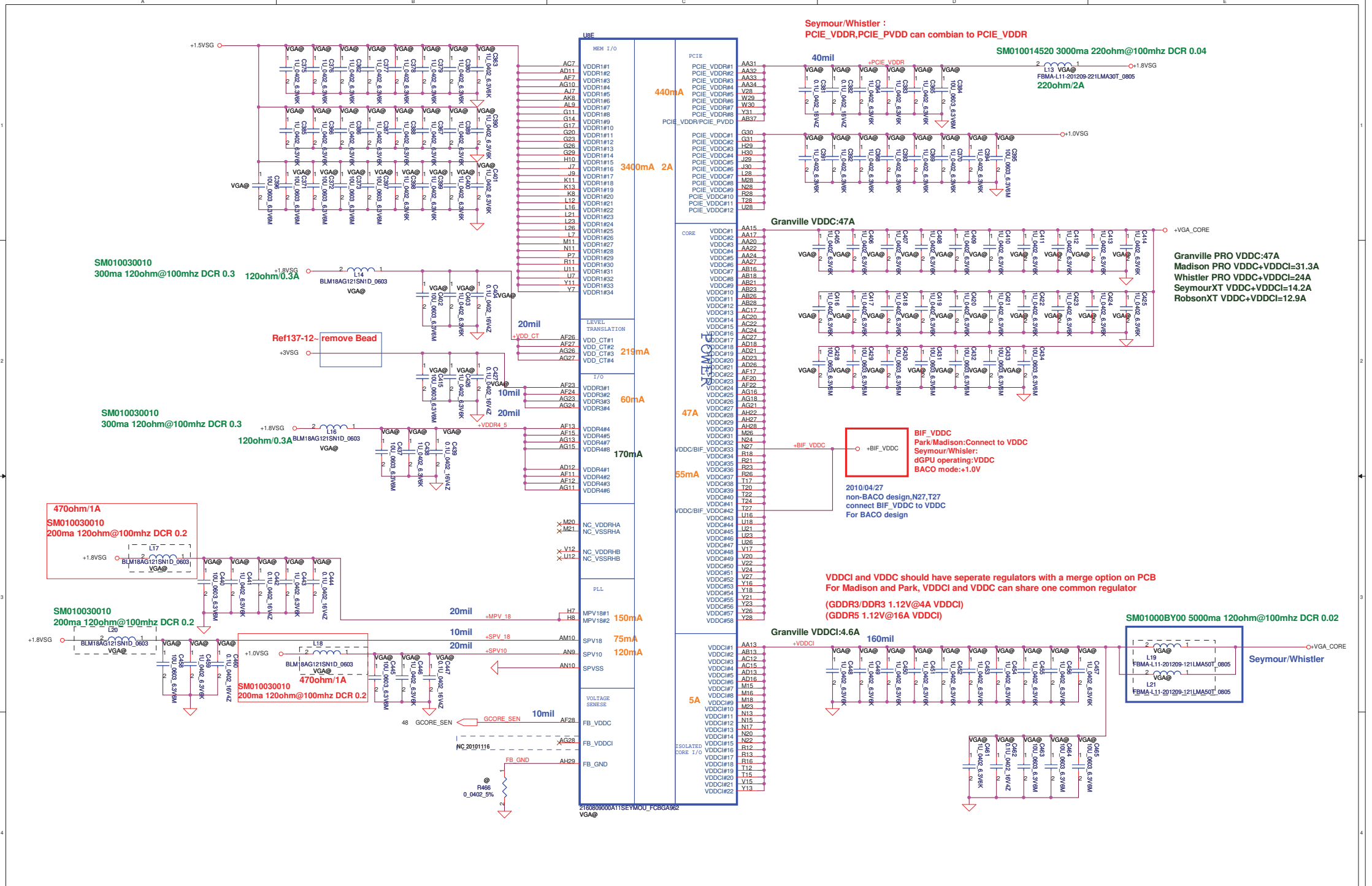

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Compal Electronics, Inc.

Title: Vancouver_Power/GND

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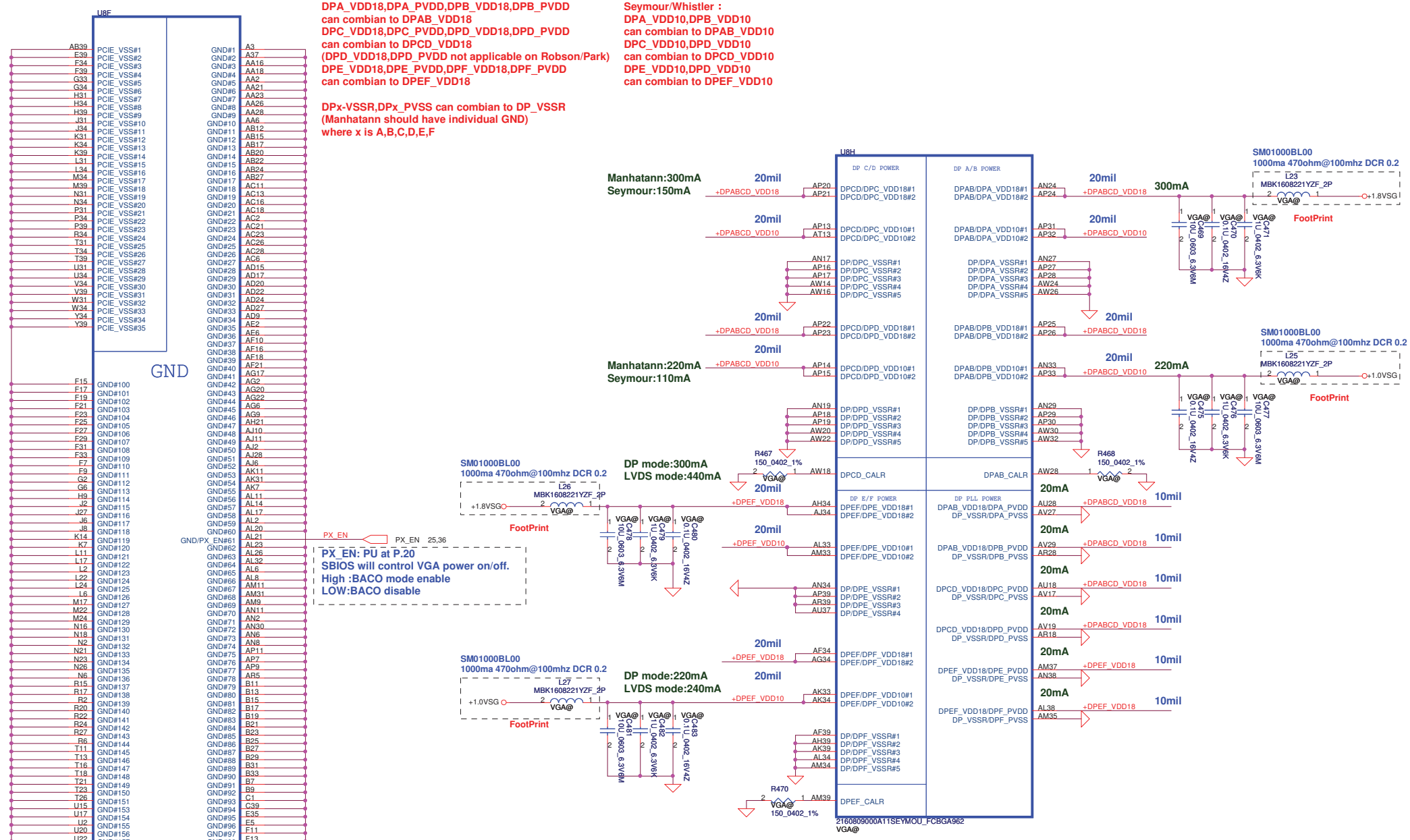

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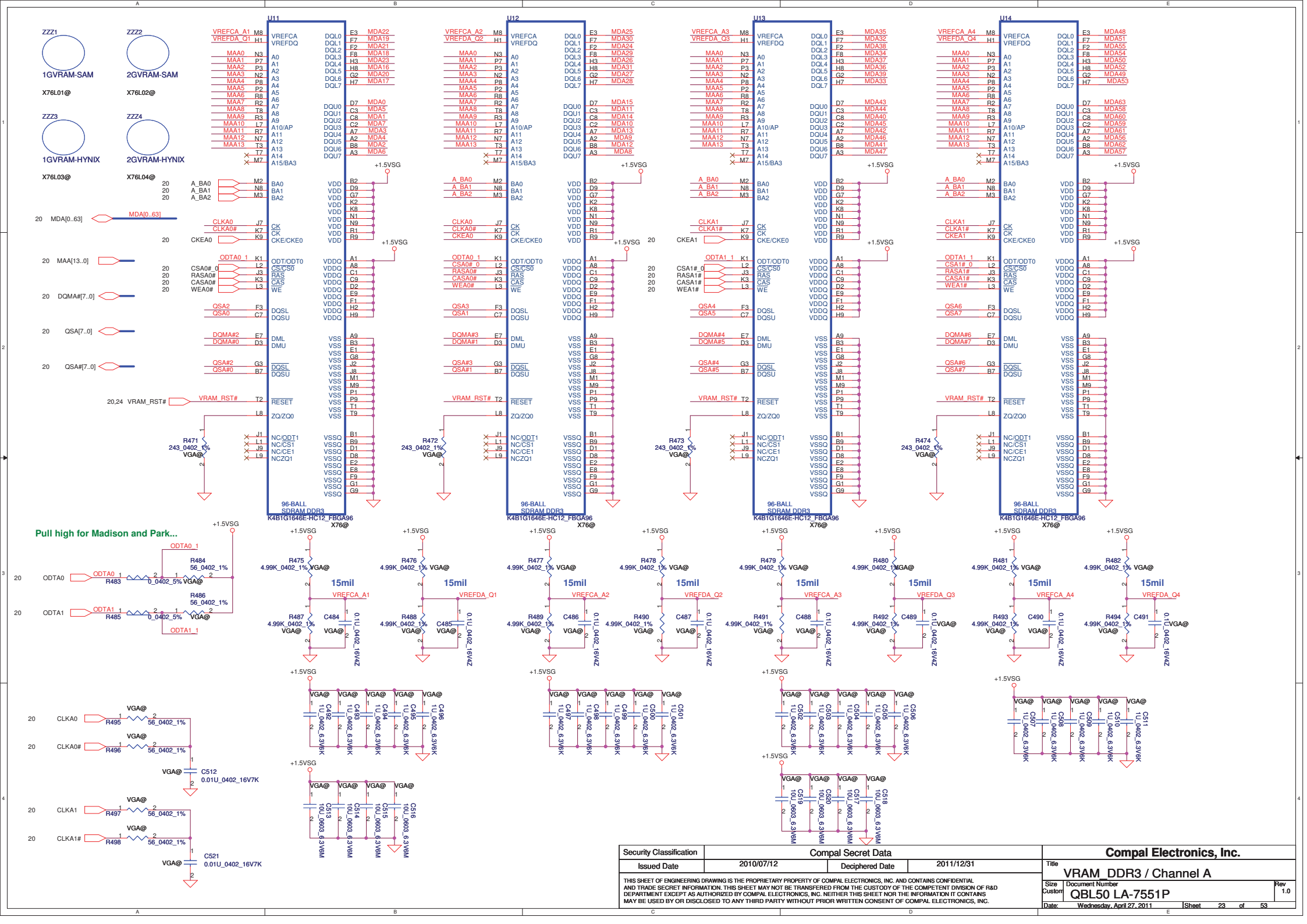

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Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel A

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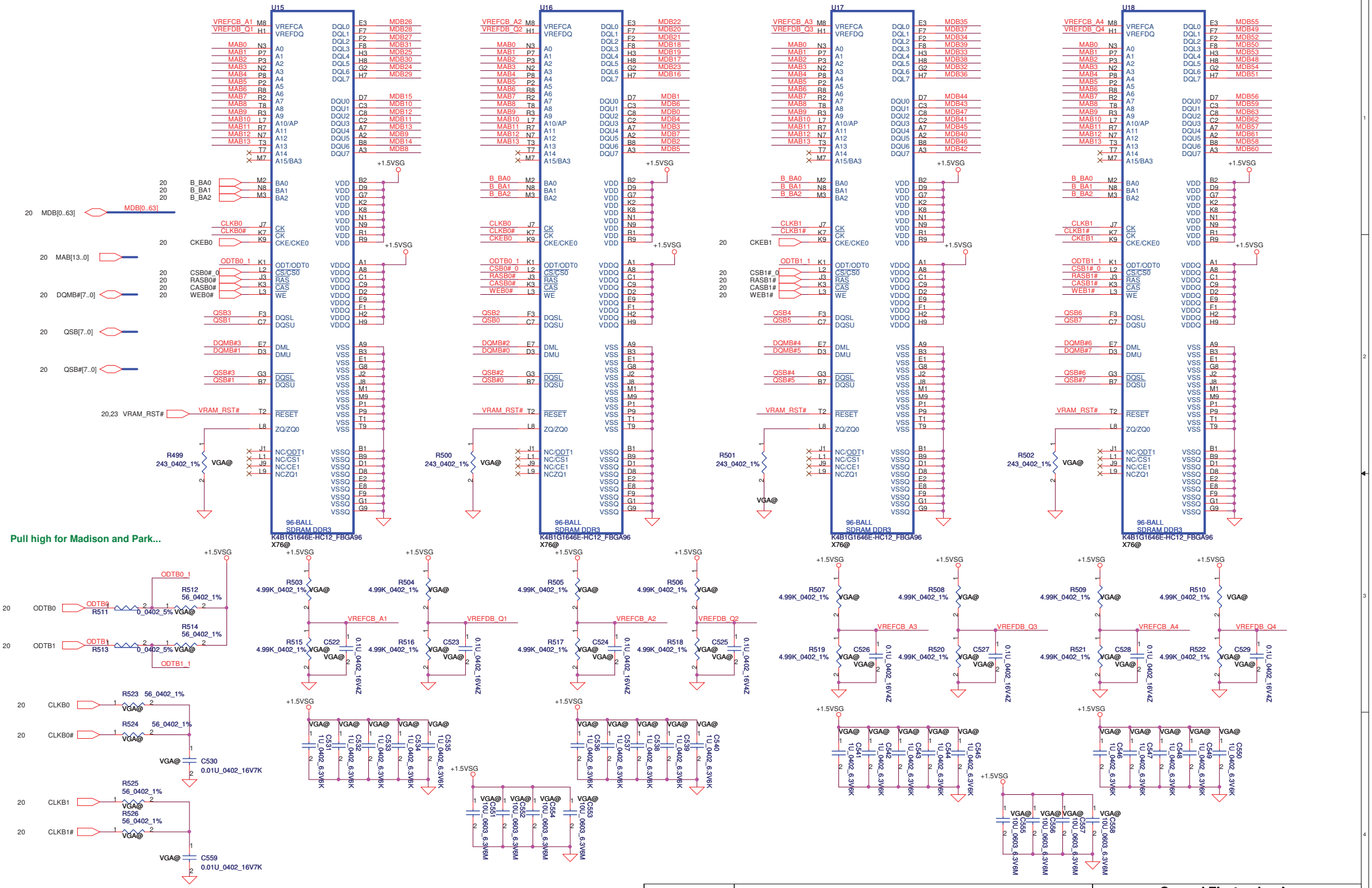

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Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel B

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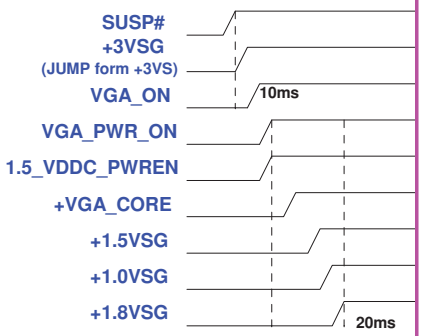
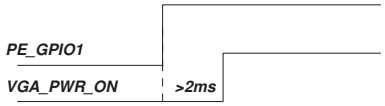
Power Sequence of Whistler and Seymour

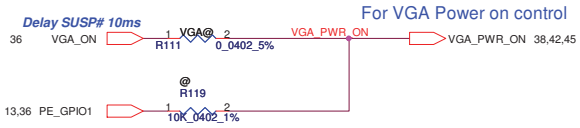


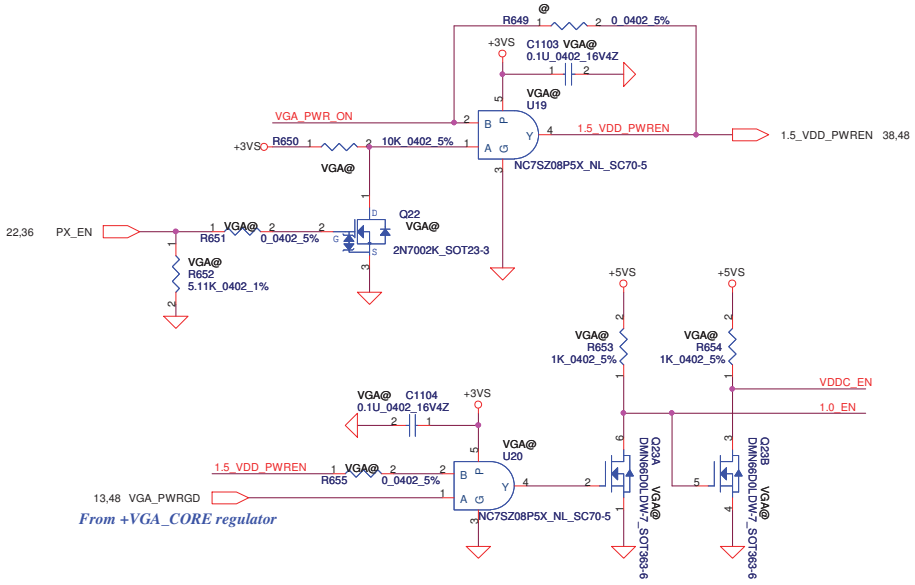
For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON

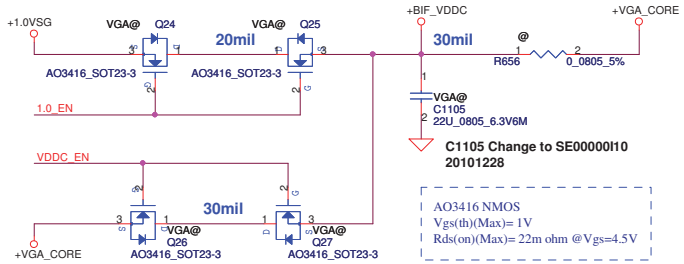


VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table	
	Whislter
VGA_PWR_ON source signal	VGA_ON
+3.3VSG	SUSP#
+1.8VSG	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN







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Issued Date	2010/08/04	Deciphered Date	2011/12/31

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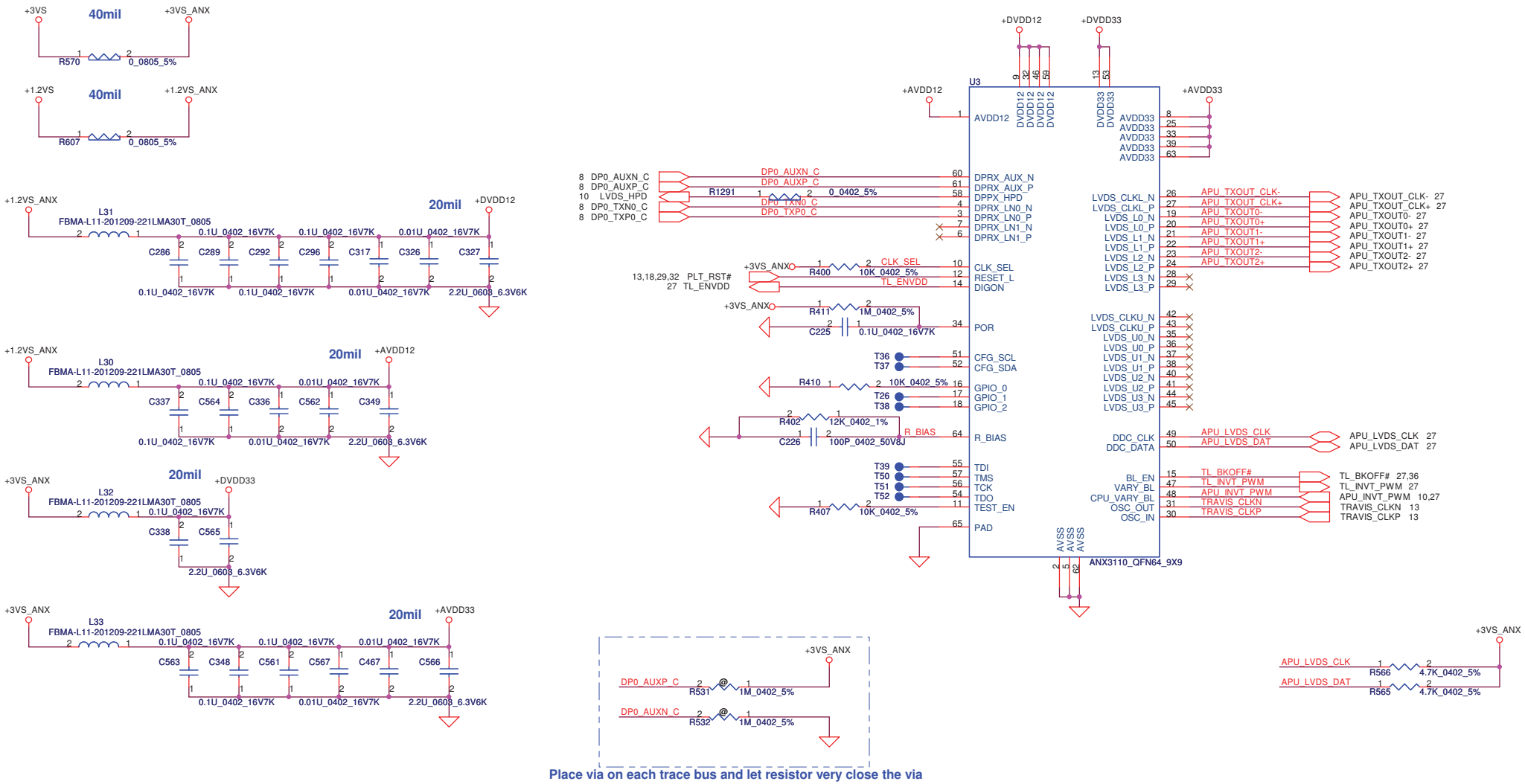
Compal Electronics, Inc.

Title: VGA power sequence and BACO

Size: Custom | Document Number: QBL50 LA-7551P | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 25 of 53



Place via on each trace bus and let resistor very close the via

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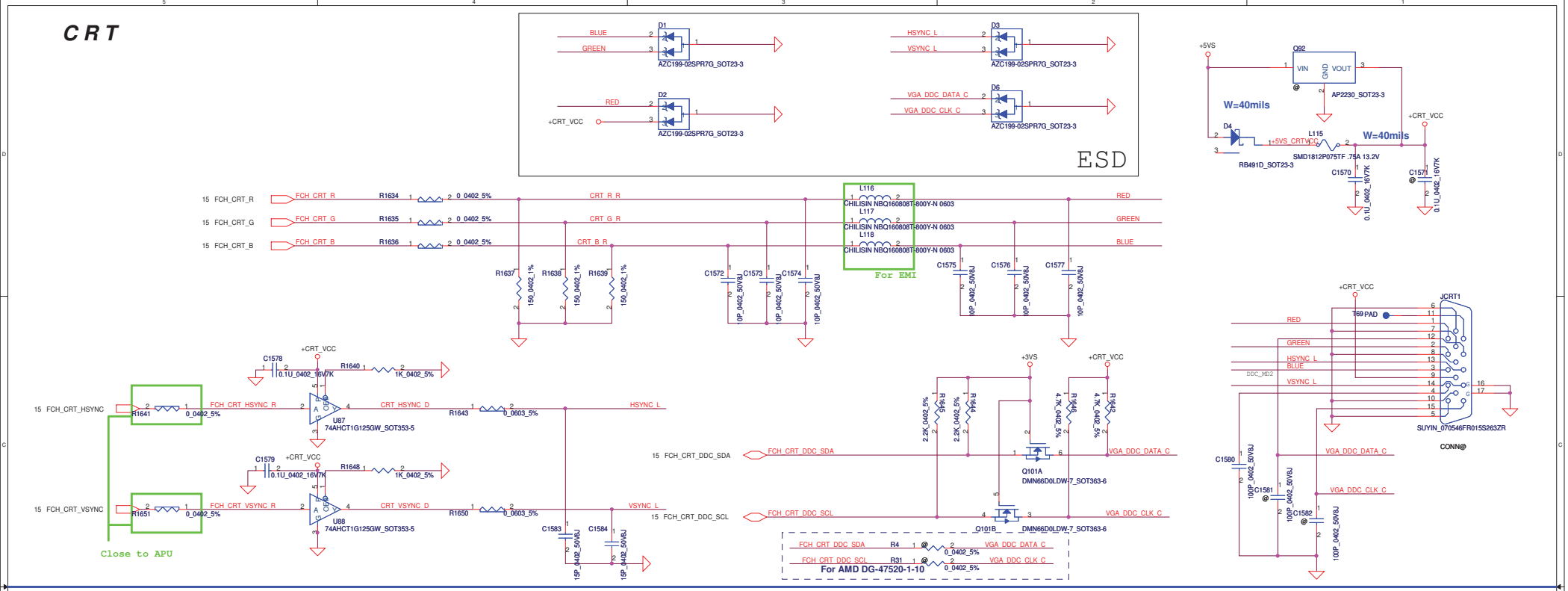
Compal Electronics, Inc.

Title: ***LVDS Translator-ANX3110***

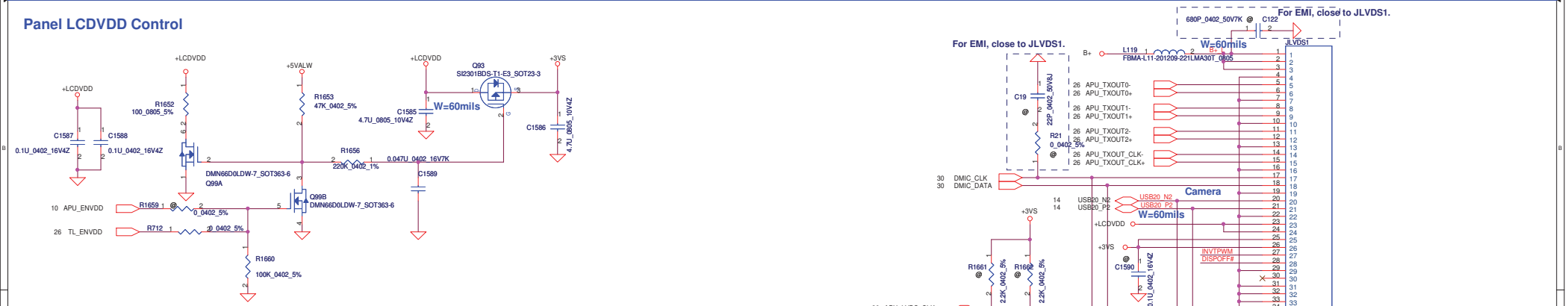
Size: Custom | Document Number: **QBL50 LA-7551P** | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 26 of 53

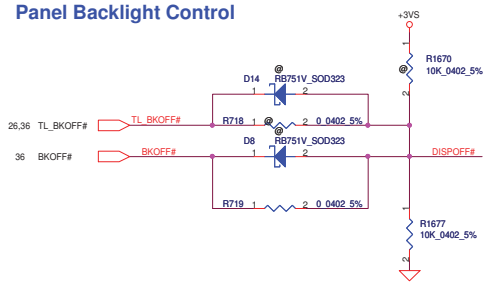
CRT



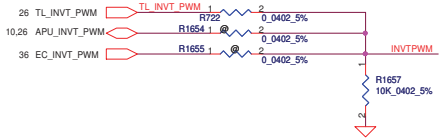
Panel LCDVDD Control



Panel Backlight Control



Panel PWM Control



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2011/12/31

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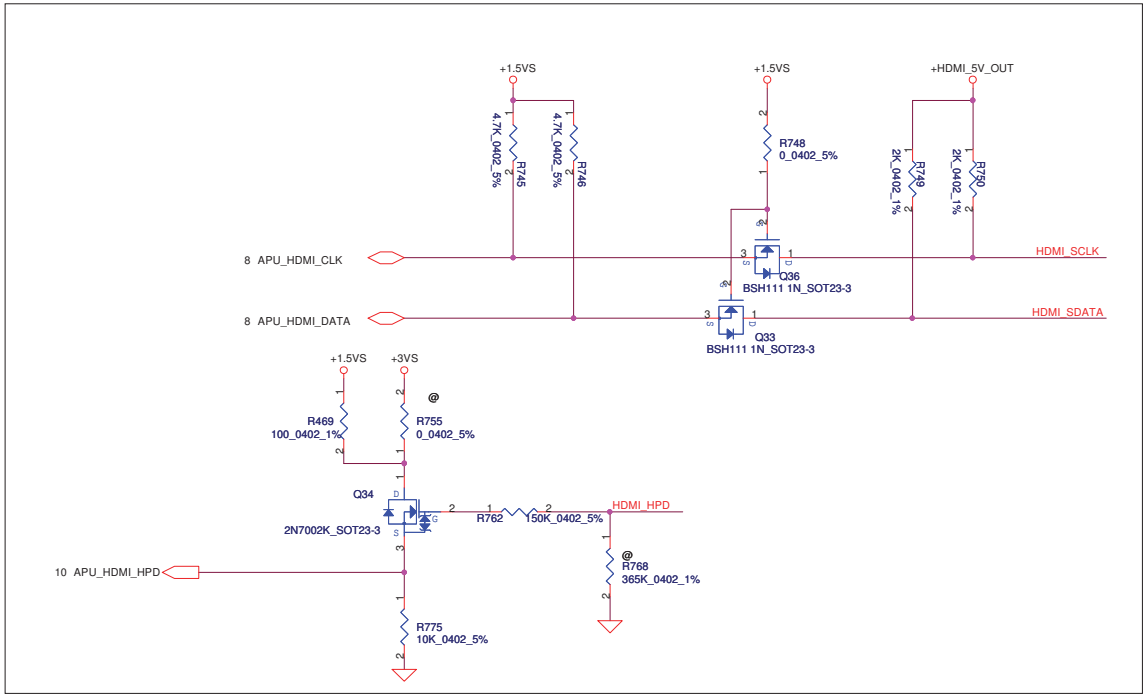
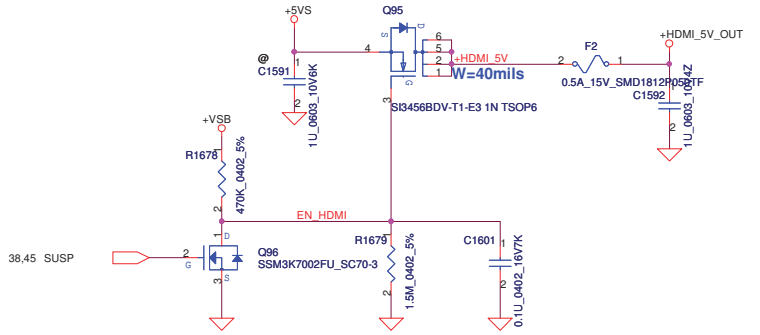
Compal Electronics, Inc.

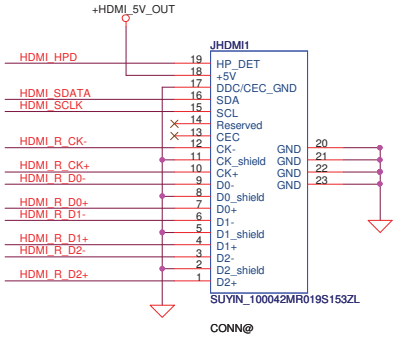
Title: P10-LVDS/CRT CONN

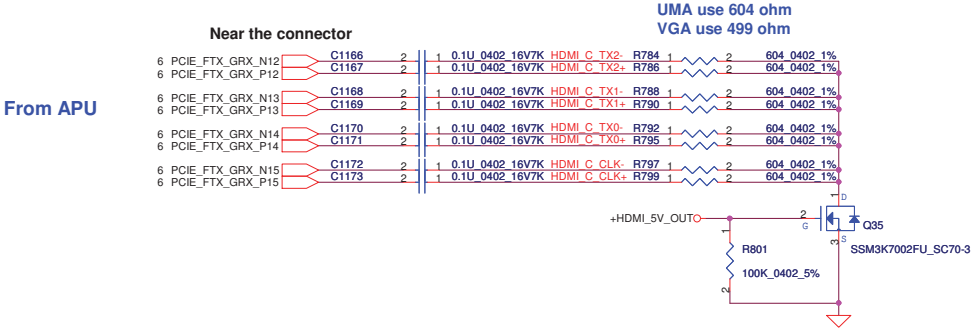
Size: C | Document Number: QBL50 LA-7551P | Rev: 1.0

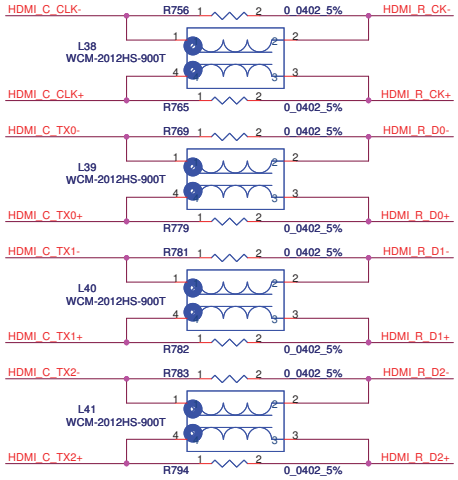
Date: Wednesday, April 27, 2011 | Sheet 27 of 53

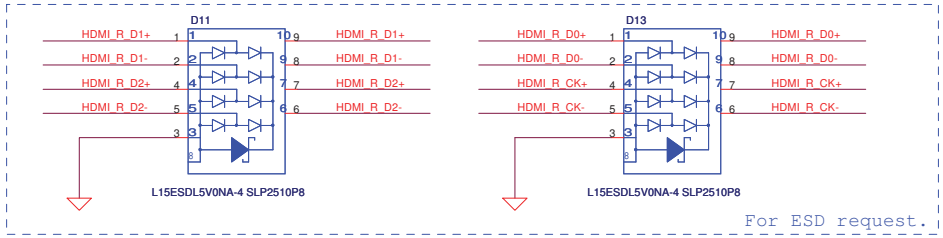


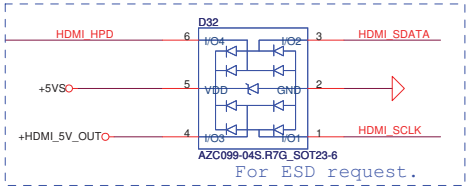












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Issued Date	2010/08/04	Deciphered Date	2011/12/31

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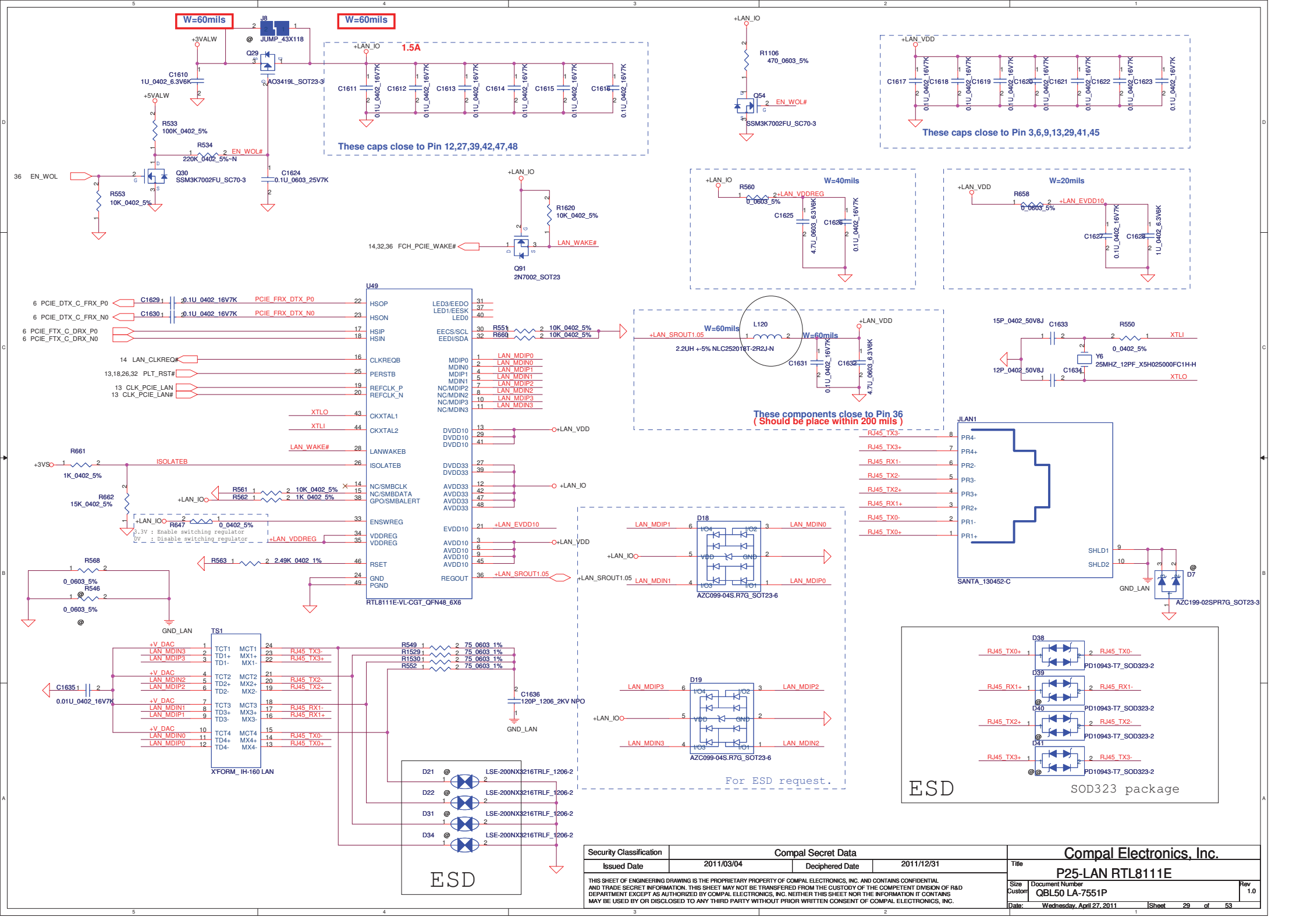
Compal Electronics, Inc.

Title: HDMI Connector

Size: Custom | Document Number: QBL50 LA-7551P | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 28 of 53



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Issued Date	2011/03/04	Deciphered Date	2011/12/31

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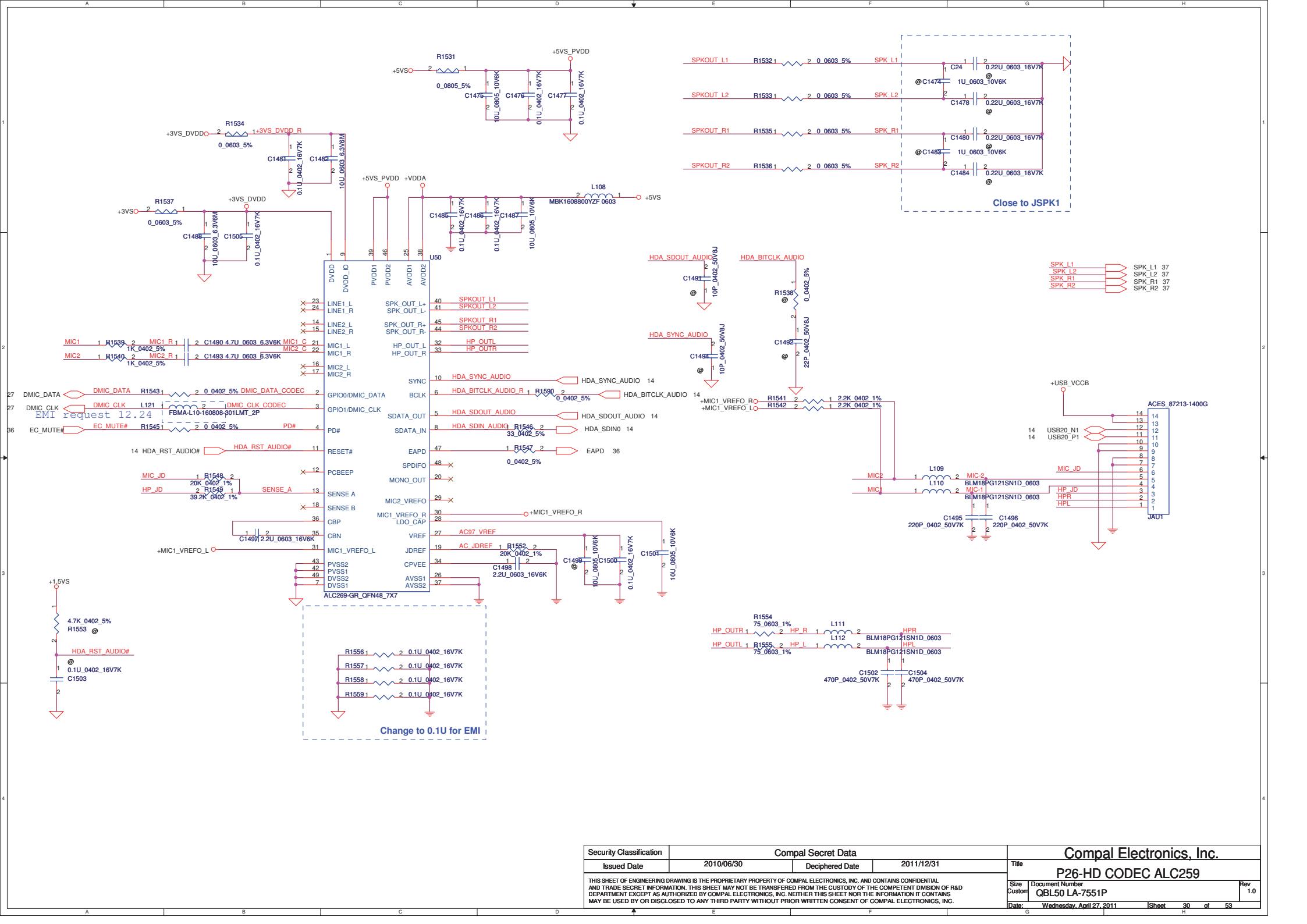
Compal Electronics, Inc.

Title: P25-LAN RTL8111E

Size: Custom | Document Number: QBL50 LA-7551P | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 29 of 53



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2011/12/31

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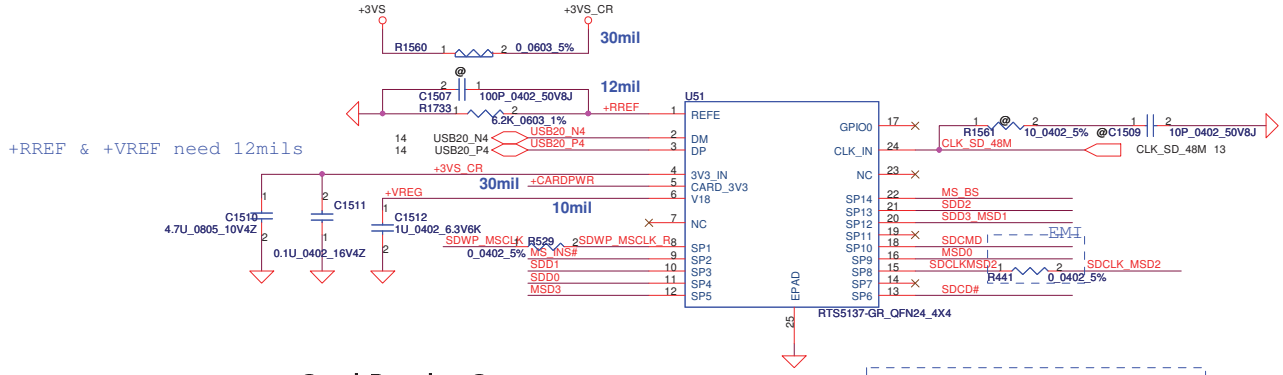
Compal Electronics, Inc.

Title: P26-HD CODEC ALC259

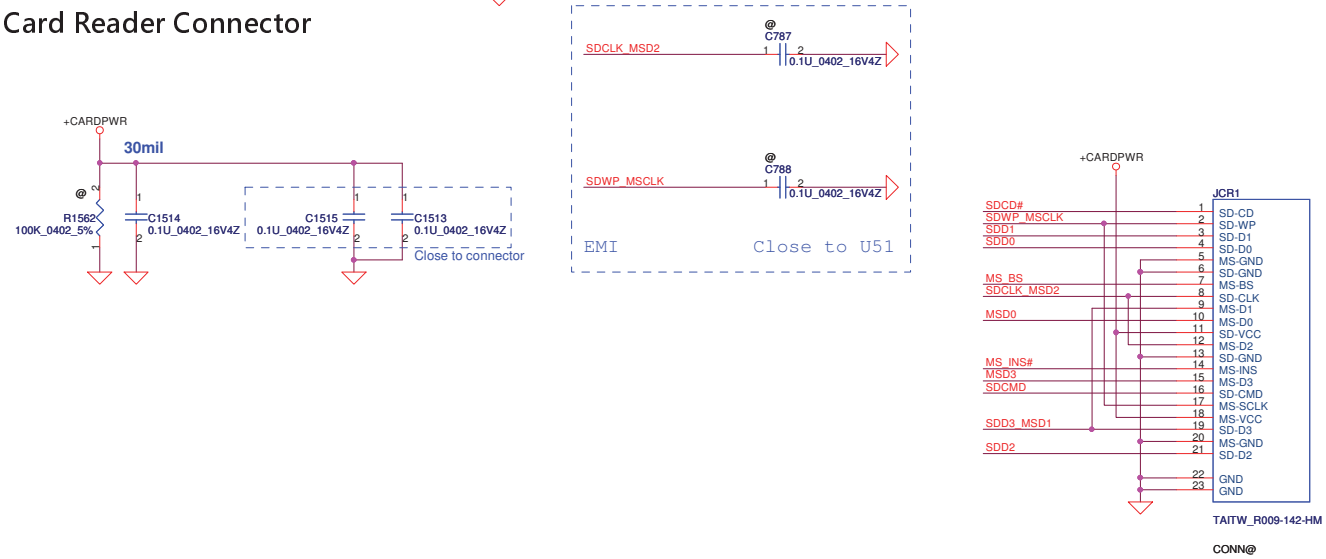
Size: Custom | Document Number: QBL50 LA-7551P | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 30 of 53

Card Reader RTS5137
(only SD/MMC/MS function)



Card Reader Connector



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/06/30	Deciphered Date	2011/12/31	Title: P27-RTS5137 Media Card Controller
				Size: Custom; Document Number: QBL50 LA-7551P; Rev: 1.0
				Date: Wednesday, April 27, 2011; Sheet 31 of 53

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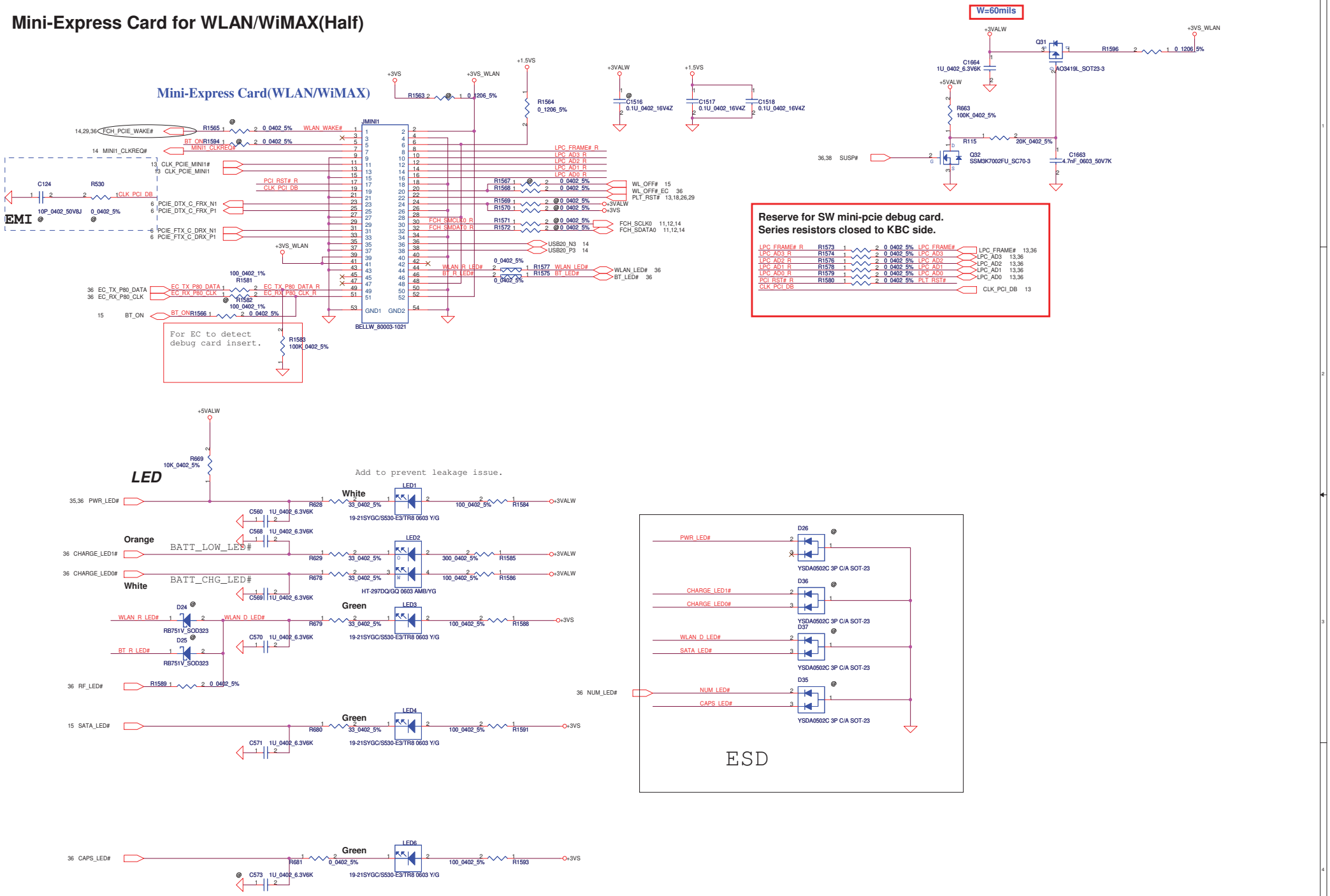
Mini-Express Card for WLAN/WiMAX(Half)



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2011/12/31

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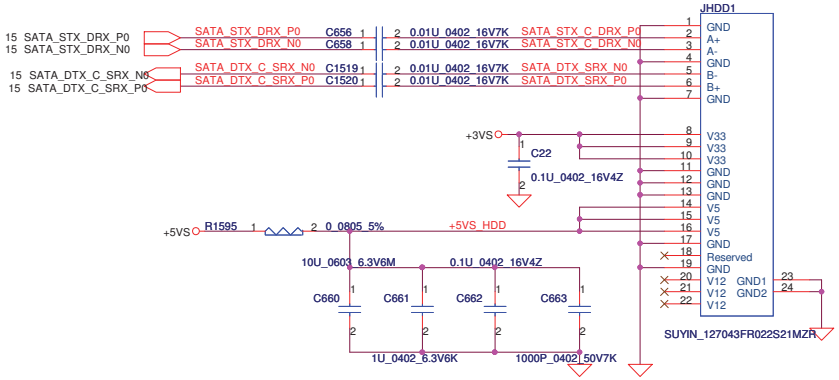
Compal Electronics, Inc.

Title: P28-Mini PCIE/LED

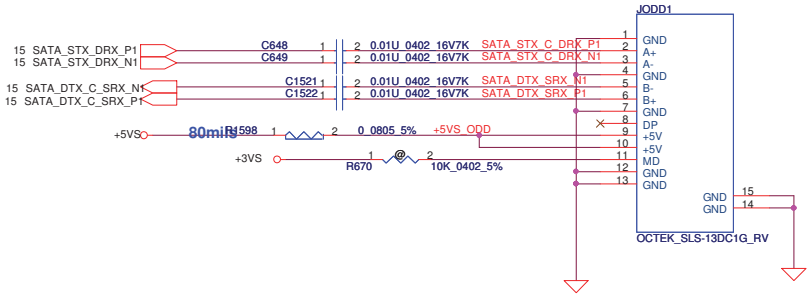
Size | Document Number: QBL50 LA-7551P | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 32 of 53

SATA HDD Conn.



SATA ODD FFC Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2011/12/31

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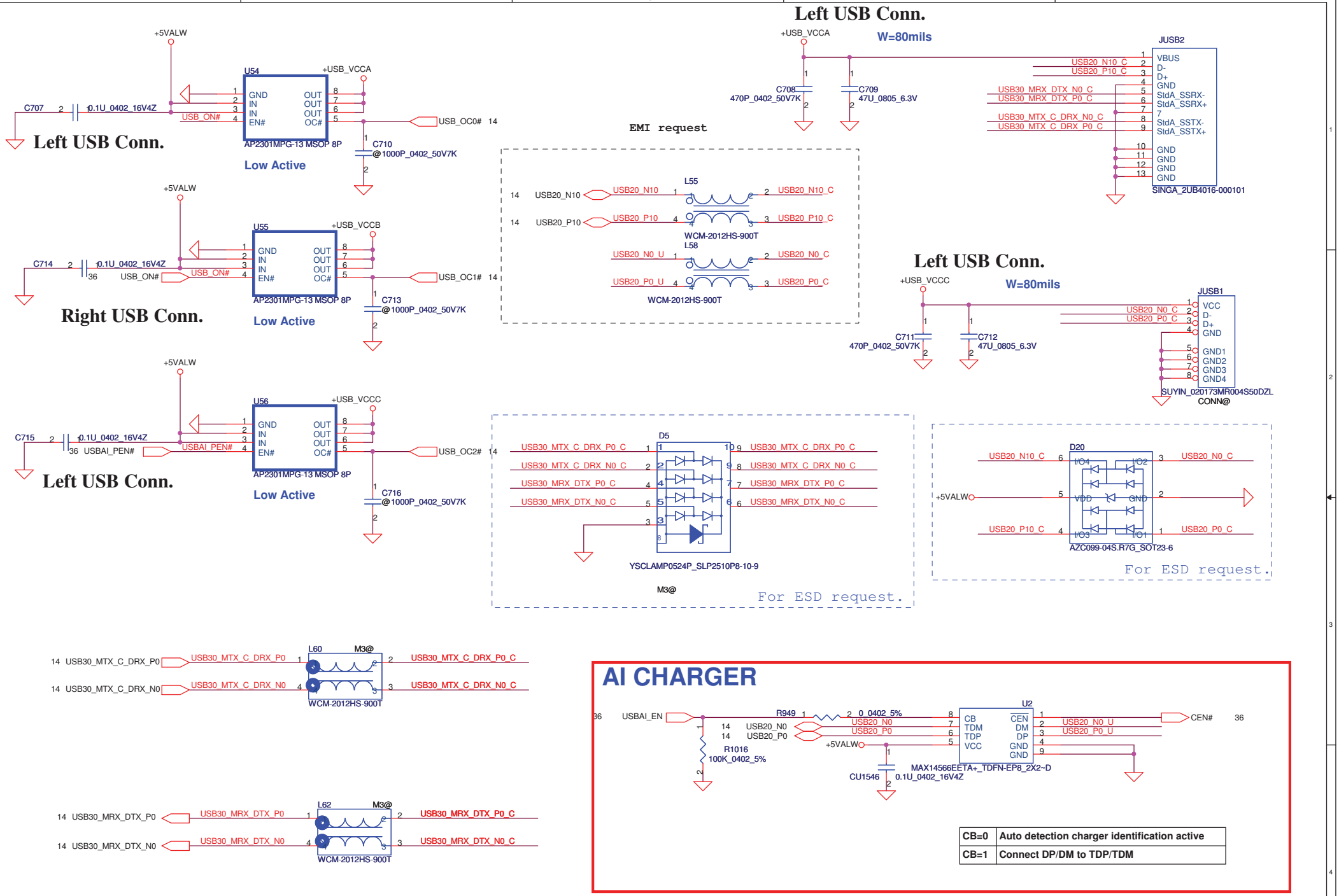
Compal Electronics, Inc.

Title: P29-HDD & ODD CONN

Size: B | Document Number: QBL50 LA-7551P | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 33 of 53



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2011/12/31

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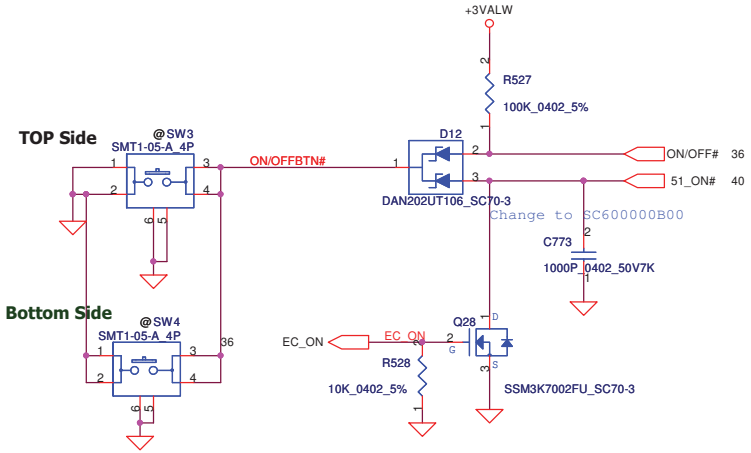
Compal Electronics, Inc.

Title: P32-USB/BT/USBsub

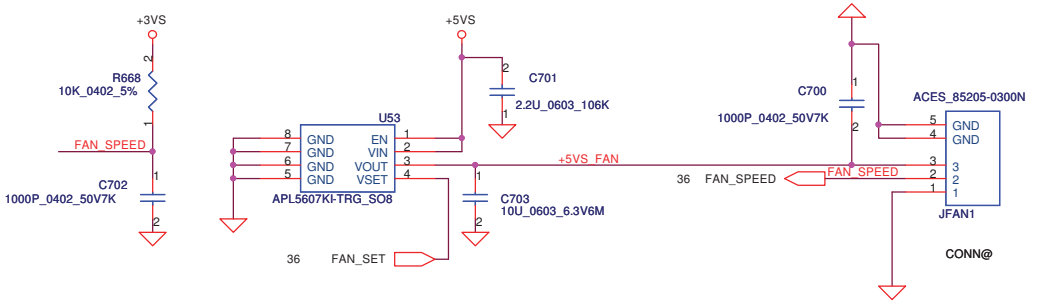
Size: Custom | Document Number: QBL50 LA-7551P | Rev: 1.0

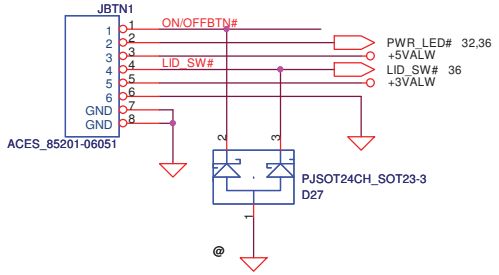
Date: Friday, April 29, 2011 | Sheet 34 of 53

ON/OFF switch **Power Button**

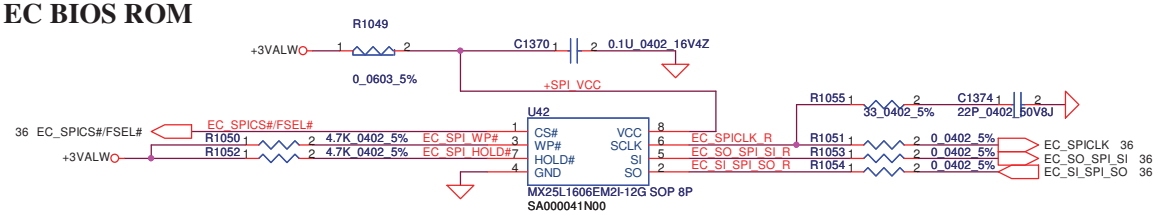


Fan Control Circuit





EC BIOS ROM



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2011/12/31

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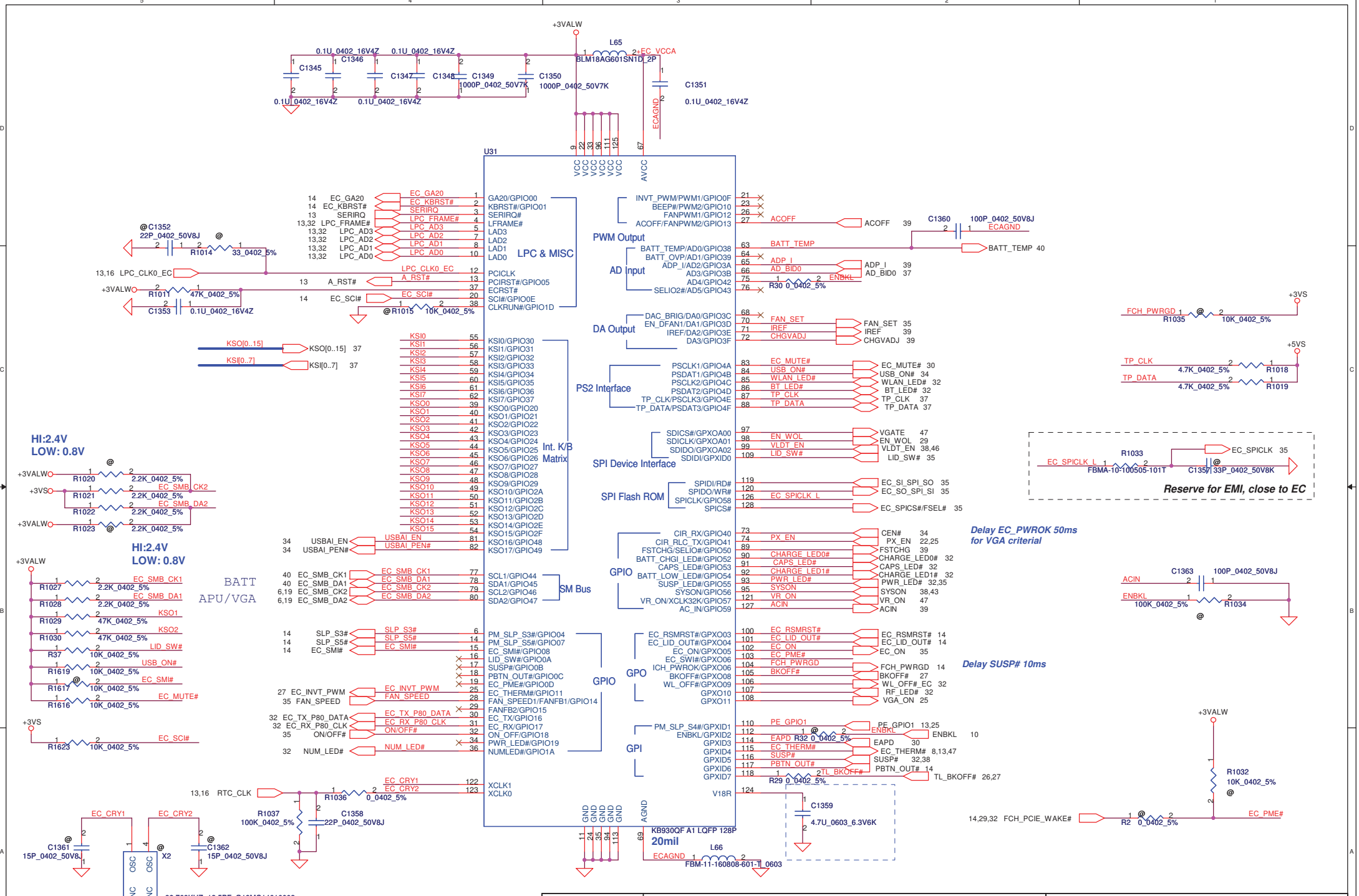
Compal Electronics, Inc.

Title: P31-KB /SW/TP/Lid

Size: B | Document Number: QBL50 LA-7551P | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 35 of 53



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2011/12/31

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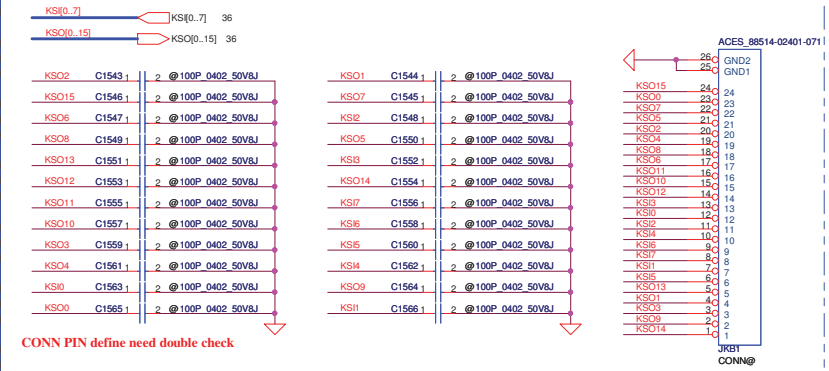
Compal Electronics, Inc.

Title: EC ENE KB930

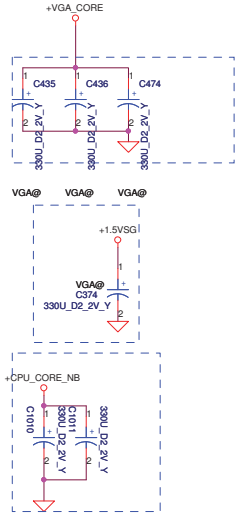
Size: B | Document Number: QBL50 LA-7551P | Rev: 1.0

Date: Friday, April 29, 2011 | Sheet 36 of 53

INT_KBD Conn.

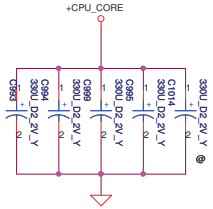


CONN PIN define need double check

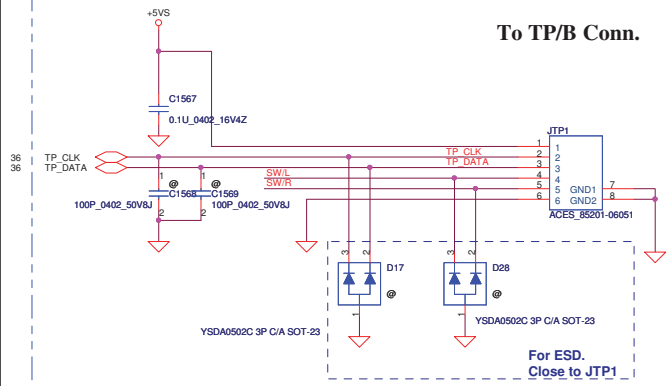


ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R10 MP	100K	18K	0.5V
3	Reserve	100K	33K	0.82V

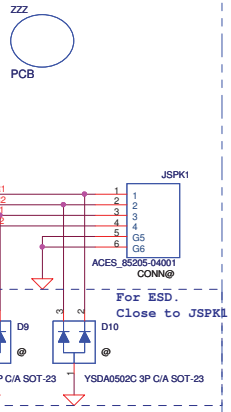
P9 FS1 PWR/GND



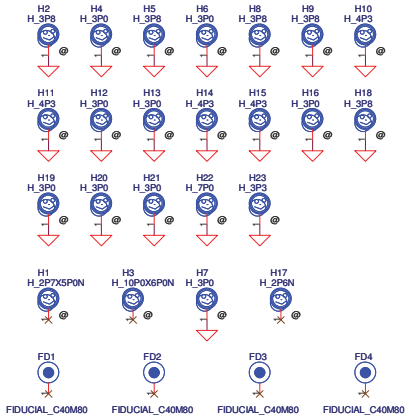
To TP/B Conn.



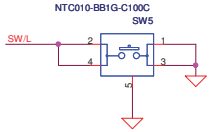
For ESD.
Close to JTP1



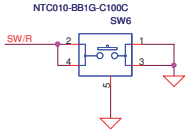
For ESD.
Close to JSPK1

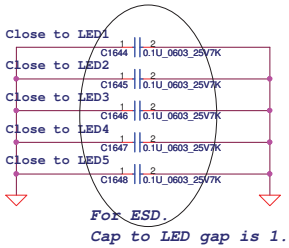


Left side Button



Right side Button





For ESD.
Cap to LED gap is 1.2mm.

Note: Differential page:
P1,P2,P9,P29,P37
And Power schematic.

Security Classification	Compal Secret Data		
Issued Date	2011/03/04	Deciphered Date	2011/12/31

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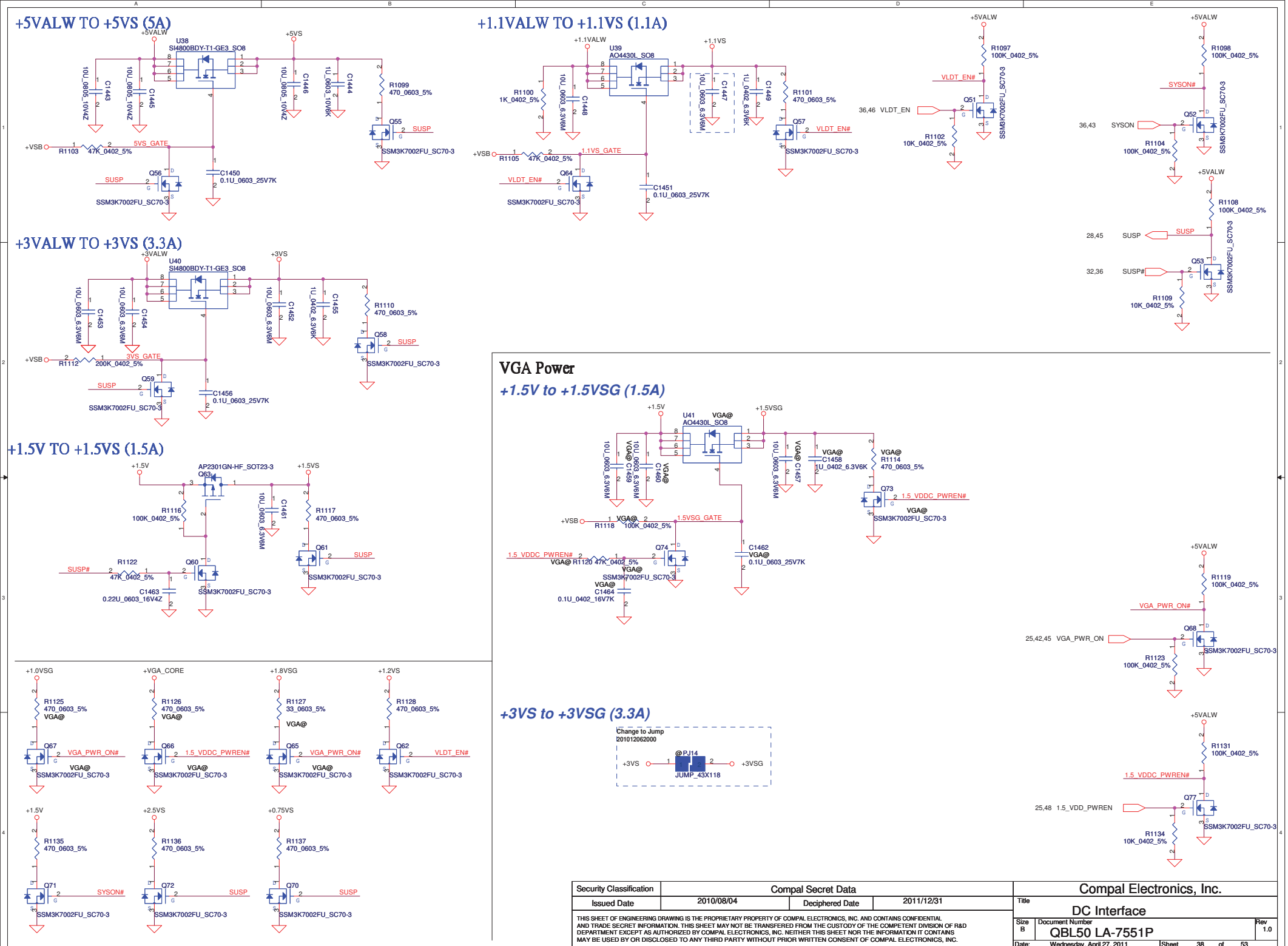
Compal Electronics, Inc.

Title: P33-Other IO/USB (right)

Size: Custom | Document Number: QBL50 LA-7551P | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 37 of 53



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2011/12/31

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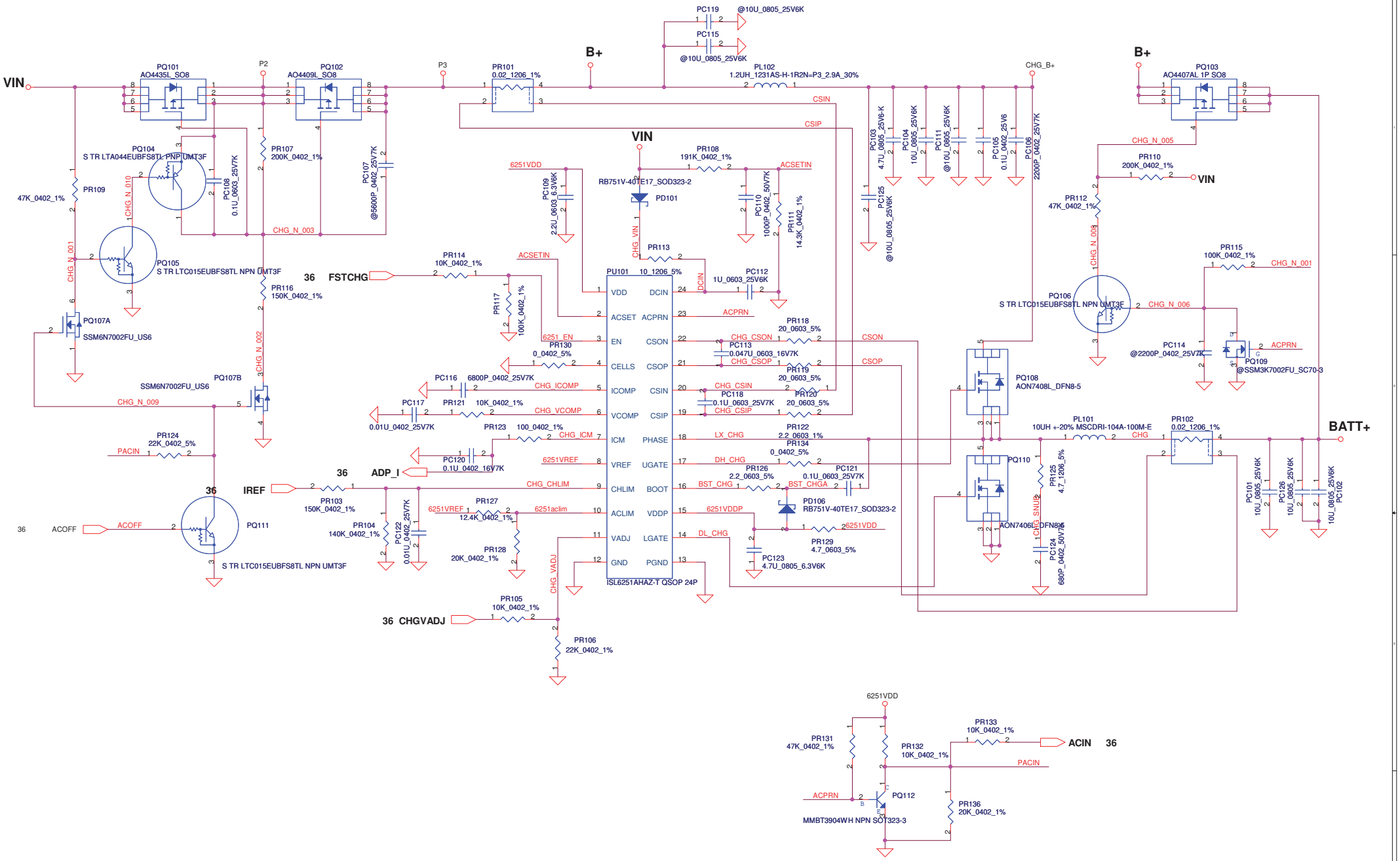
Compal Electronics, Inc.

Title: DC Interface

Size: B | Document Number: QBL50 LA-7551P | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 38 of 53



Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2011/12/31

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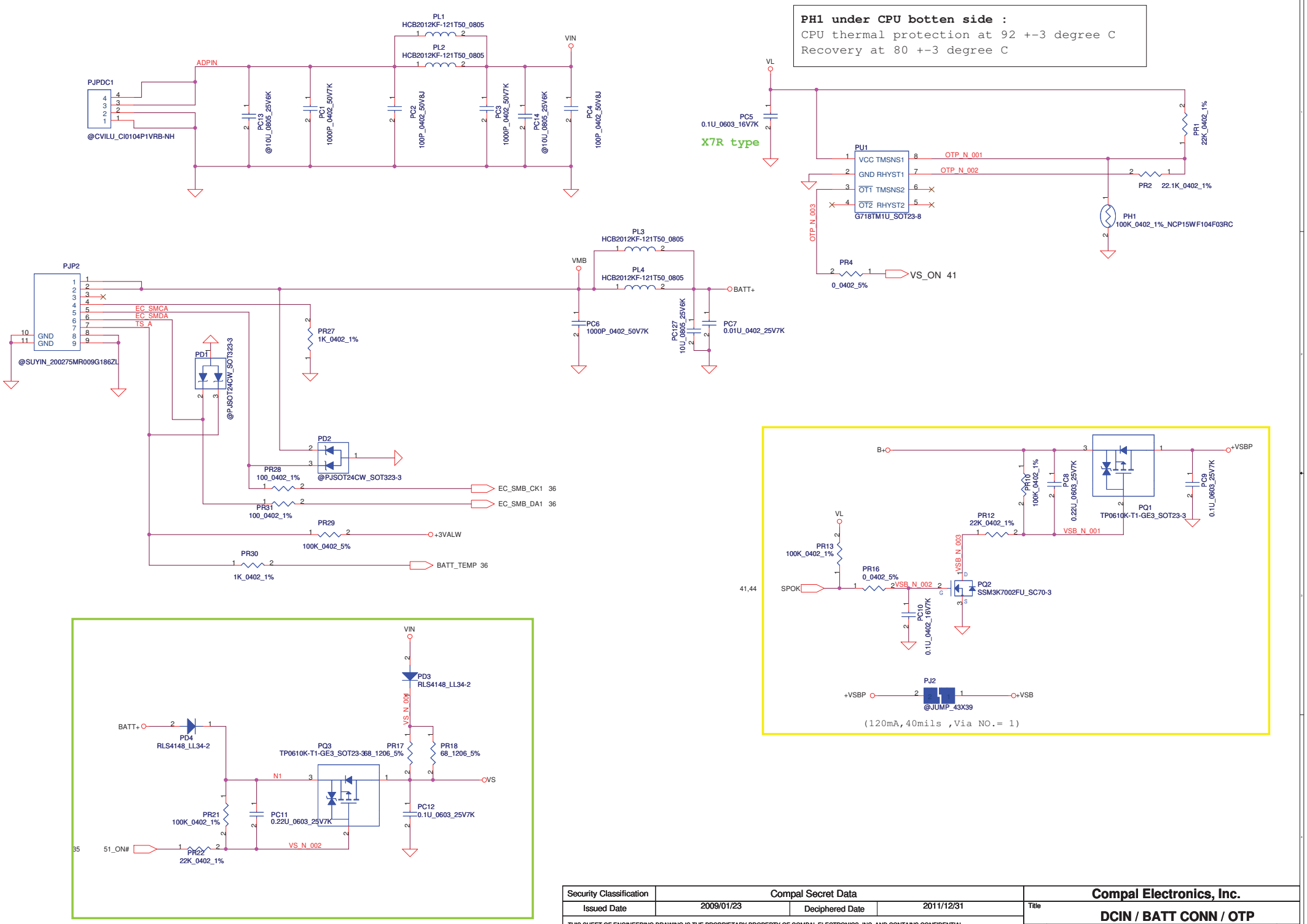
Compal Electronics, Inc.

Title: **CHARGER**

Size: | Document Number: | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 39 of 53



Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2011/12/31

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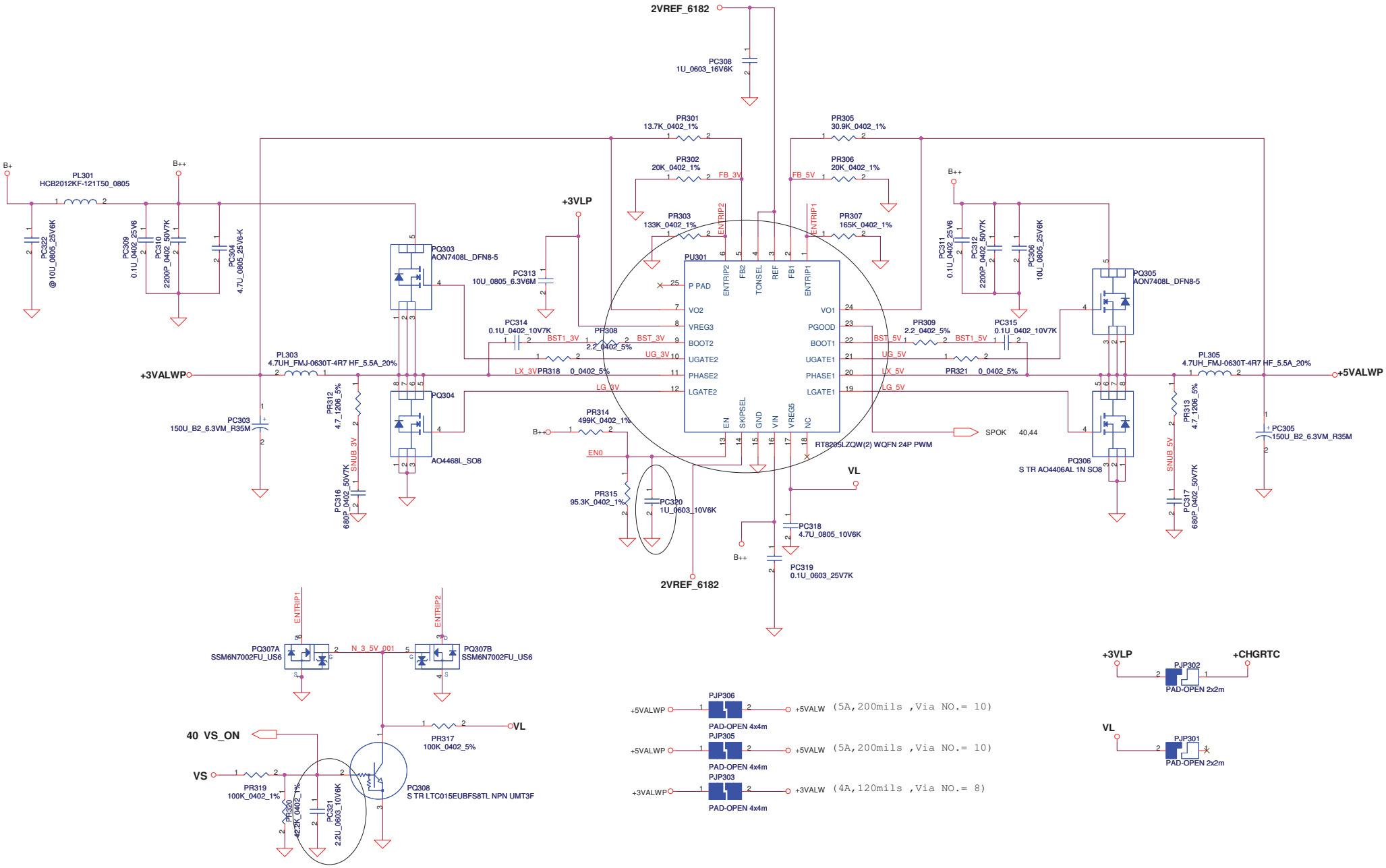
Compal Electronics, Inc.

Title: **DCIN / BATT CONN / OTP**

Size | Document Number: NCL61 LA-6321P M/B | Rev 1.0

Date: Wednesday, April 27, 2011 | Sheet 40 of 53



EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2011/12/31

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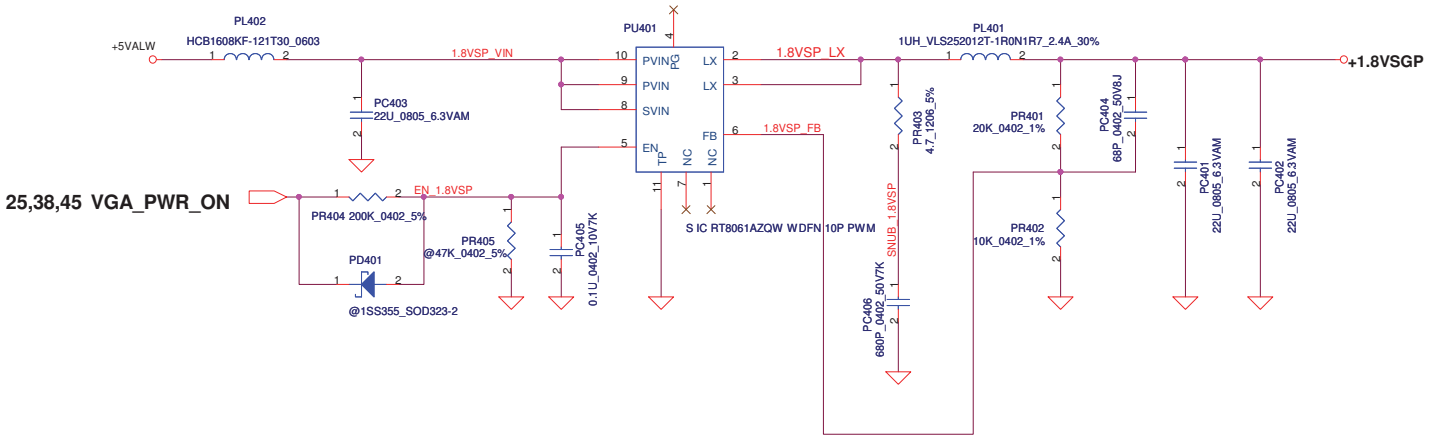
Compal Electronics, Inc.

Title: **3.3VALWP/5VALWP**

Size: Custom | Document Number: QBL50 LA-7551P | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 41 of 53



<Vo=1.8V> VFB=0.6V
Vo=VFB*(1+PR401/PR402)=0.6*(1+20K/10K)=1.8V

(2A, 80mils, Via NO.= 4)

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2009/01/23	Deciphered Date	2011/12/31	Title: +1.8VSGP
				Size: Document Number: NCL61 LA-6321P M/B — Rev: 1.0
				Date: Wednesday, April 27, 2011 — Sheet 42 of 53

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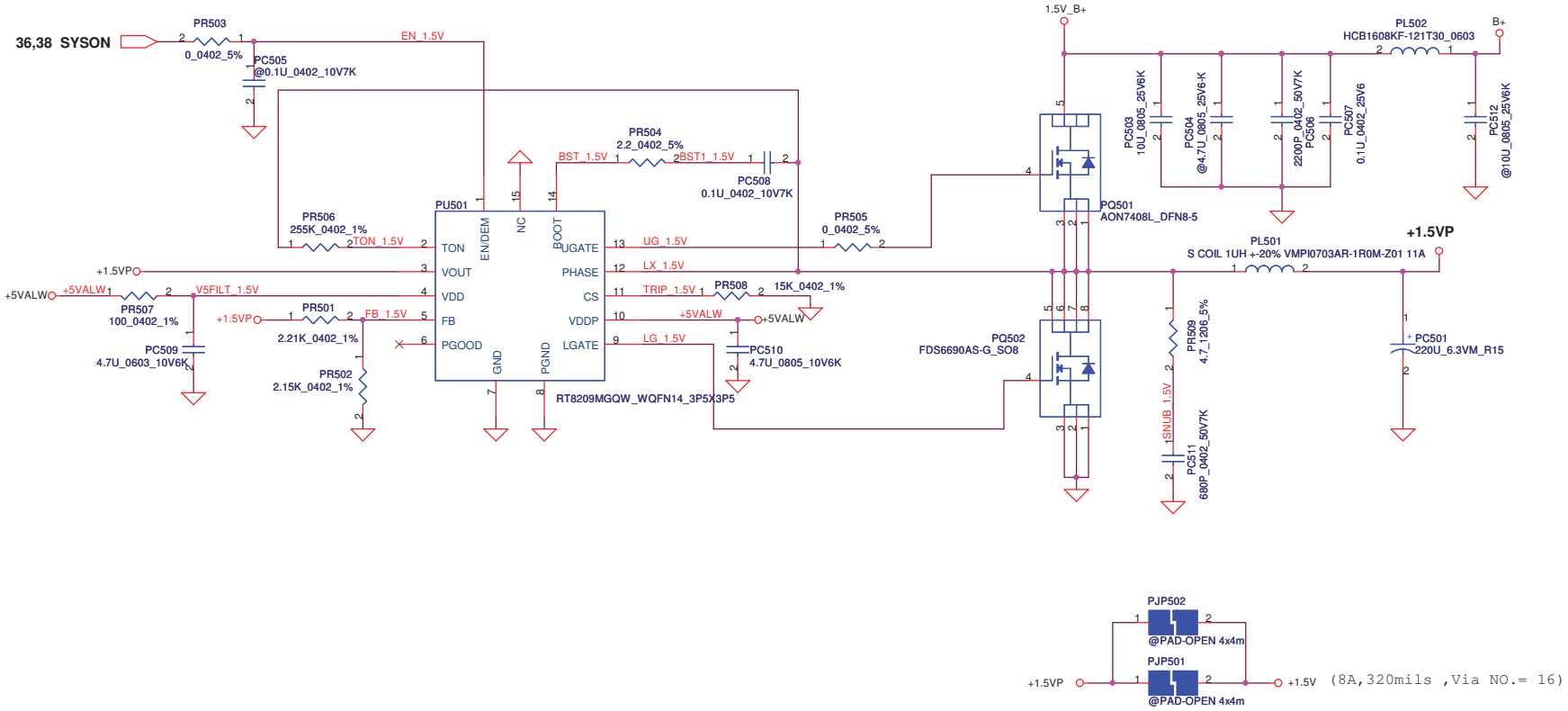

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2011/12/31

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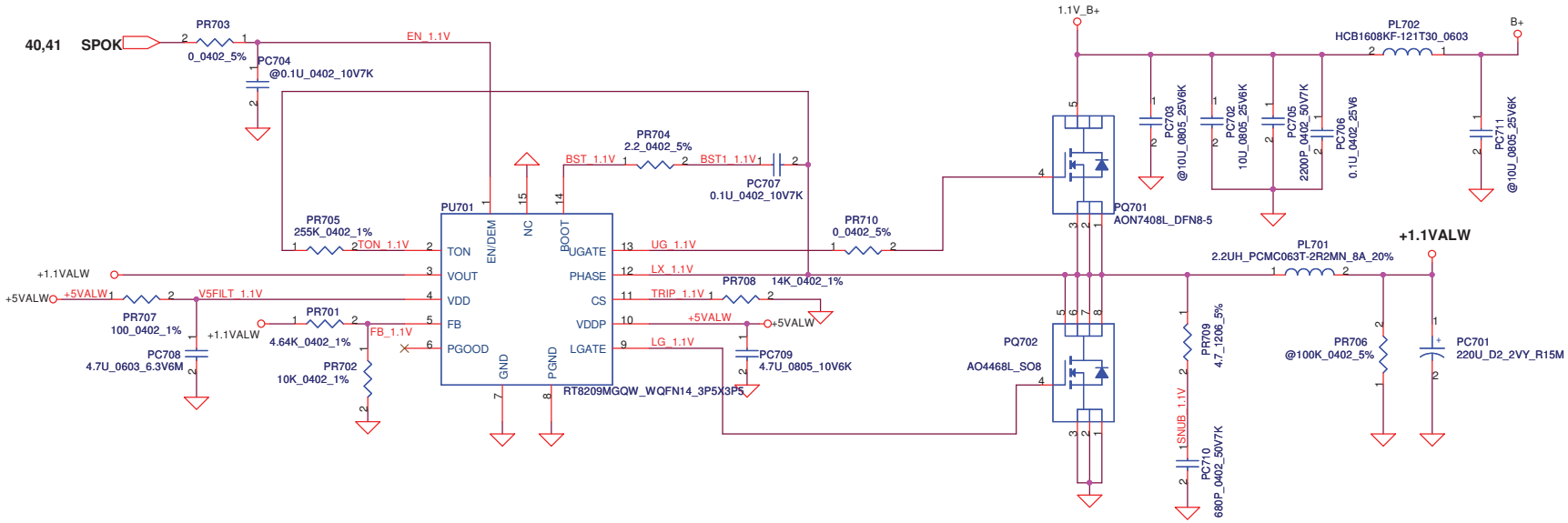
Compal Electronics, Inc.

Title: **+1.5VP**

Size | Document Number: *QBL50 LA-7551P* | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 43 of 53



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/31

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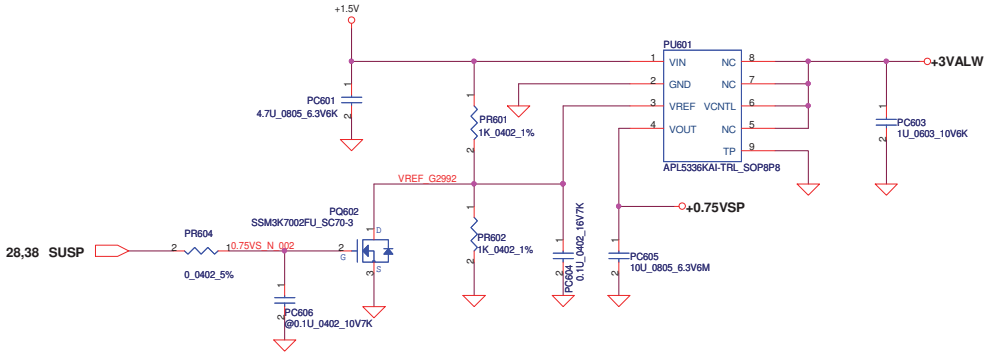
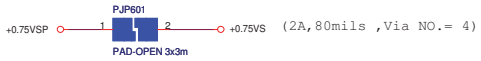
Compal Electronics, Inc.

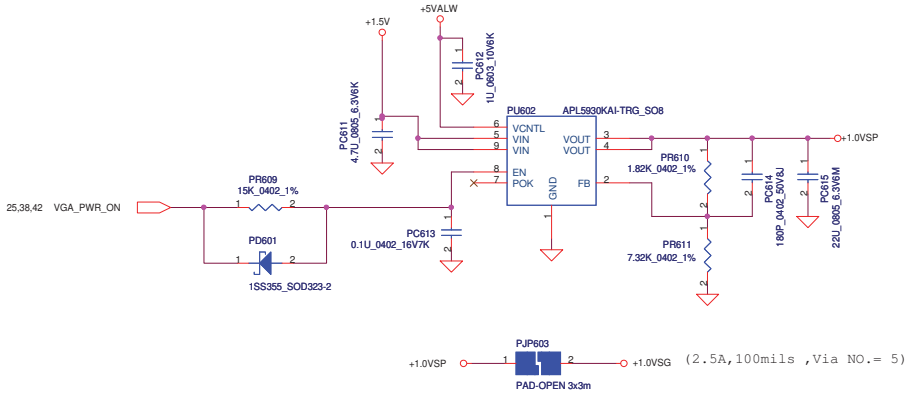
Title: **PWR+1.1VALWP**

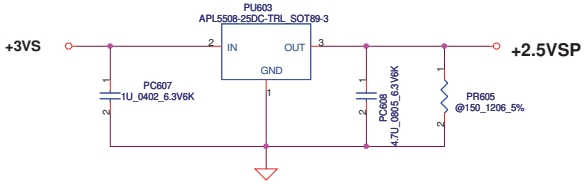
Size: Custom | Document Number: **QBL50 LA-7551P** | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 44 of 53









Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2011/12/31

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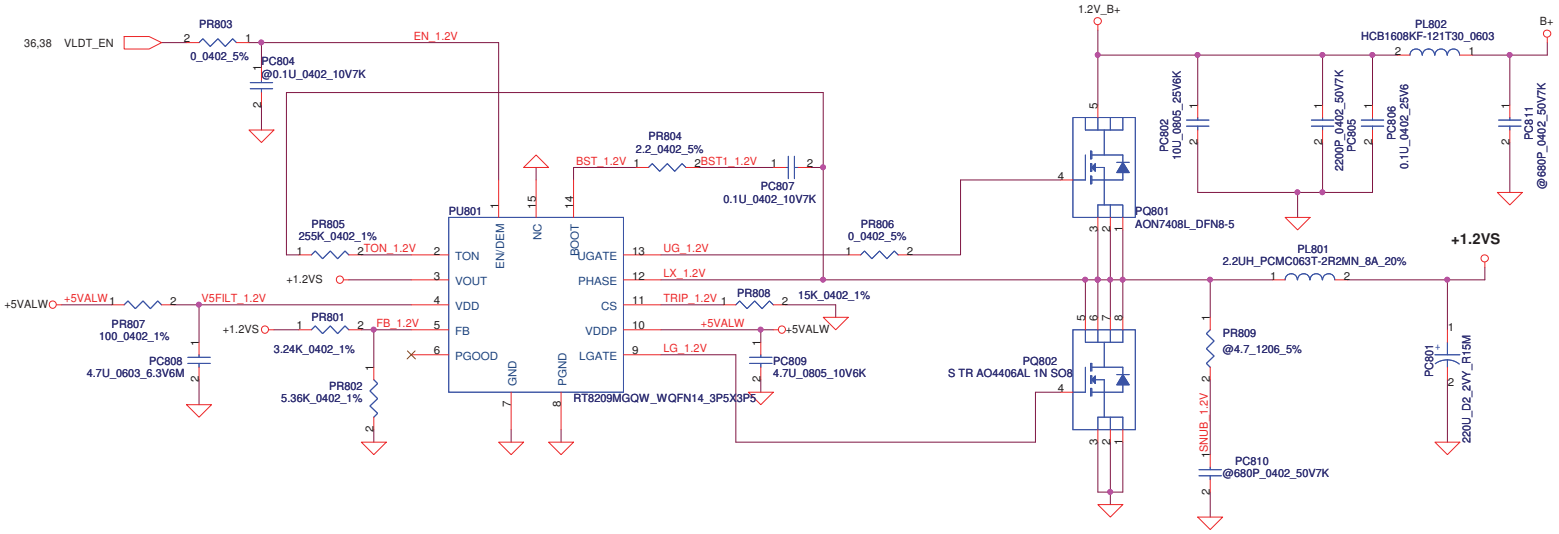
Compal Electronics, Inc.

Title: **PWR 0.75VSP/1.0VSP/2.5VSP**

Size | Document Number: *QBL50 LA-7551P* | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 45 of 53



Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2011/12/31

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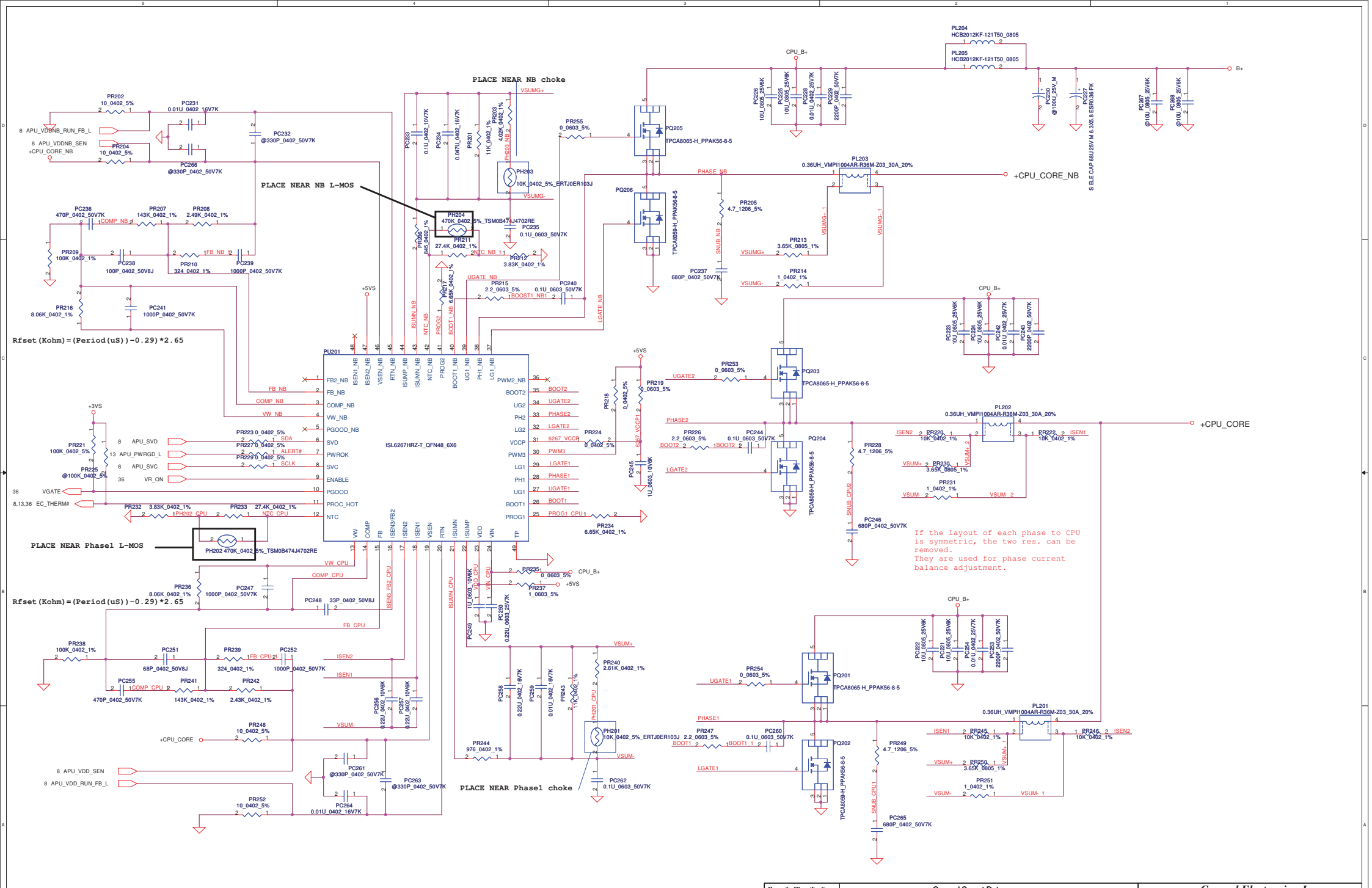
Compal Electronics, Inc.

Title: **+1.2VSP**

Size | Document Number: NCL61 LA-6321P M/B | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 46 of 53



Security Classification	Compal Secret Data		
Issued Date	2010/11/11	Deciphered Date	2011/12/31

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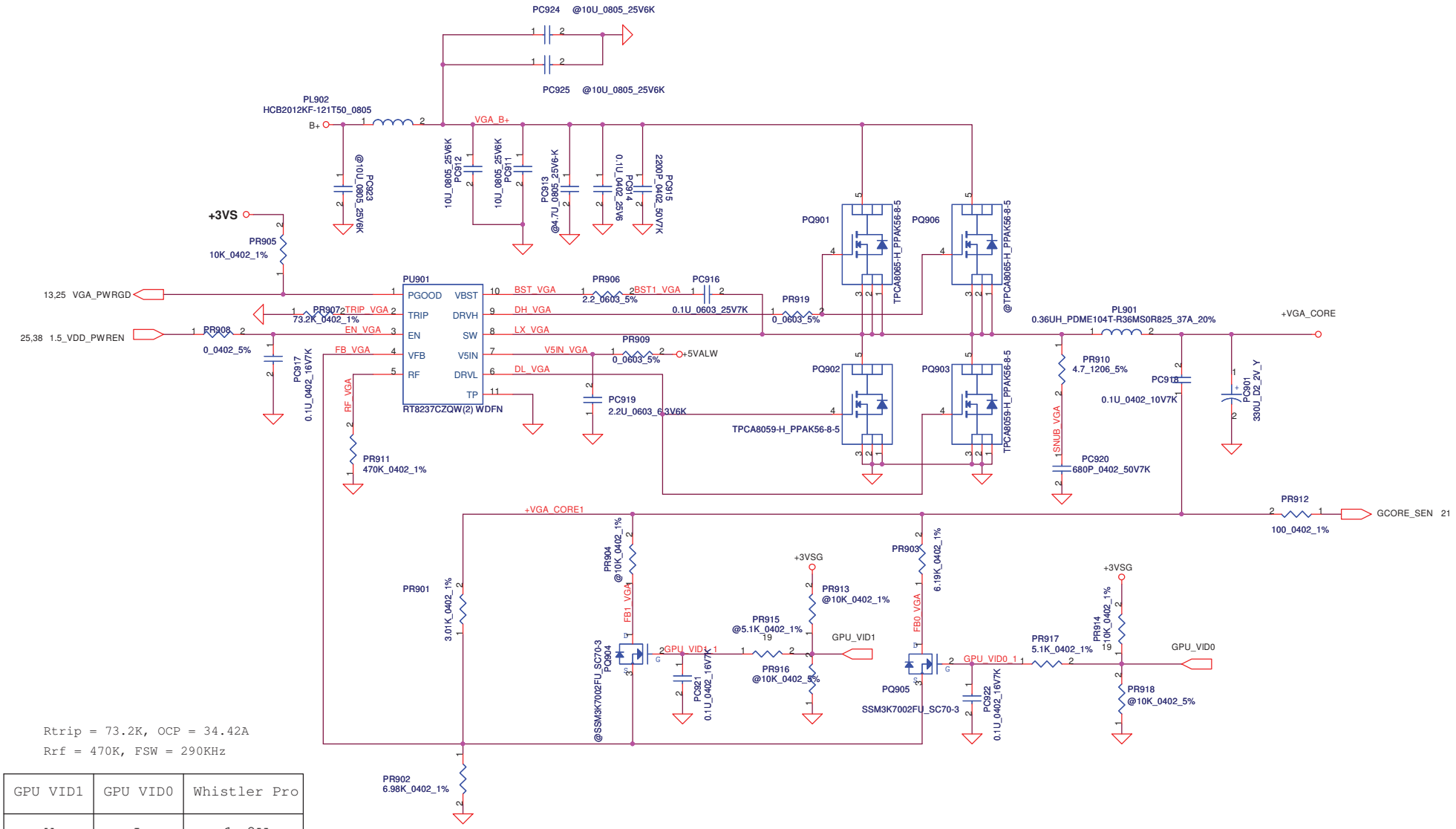
Compal Electronics, Inc.

Title: **PWR_+CPU_CORE/+CPU_CORE_NB**

Size | Document Number: **QBL50 LA-7551P** | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 47 of 53



Rtrip = 73.2K, OCP = 34.42A

Rrf = 470K, FSW = 290KHz

GPU VID1	GPU VID0	Whistler Pro
X	L	1.0V
X	H	0.9V
H	L	
H	H	

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2011/12/31

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Compal Electronics, Inc.

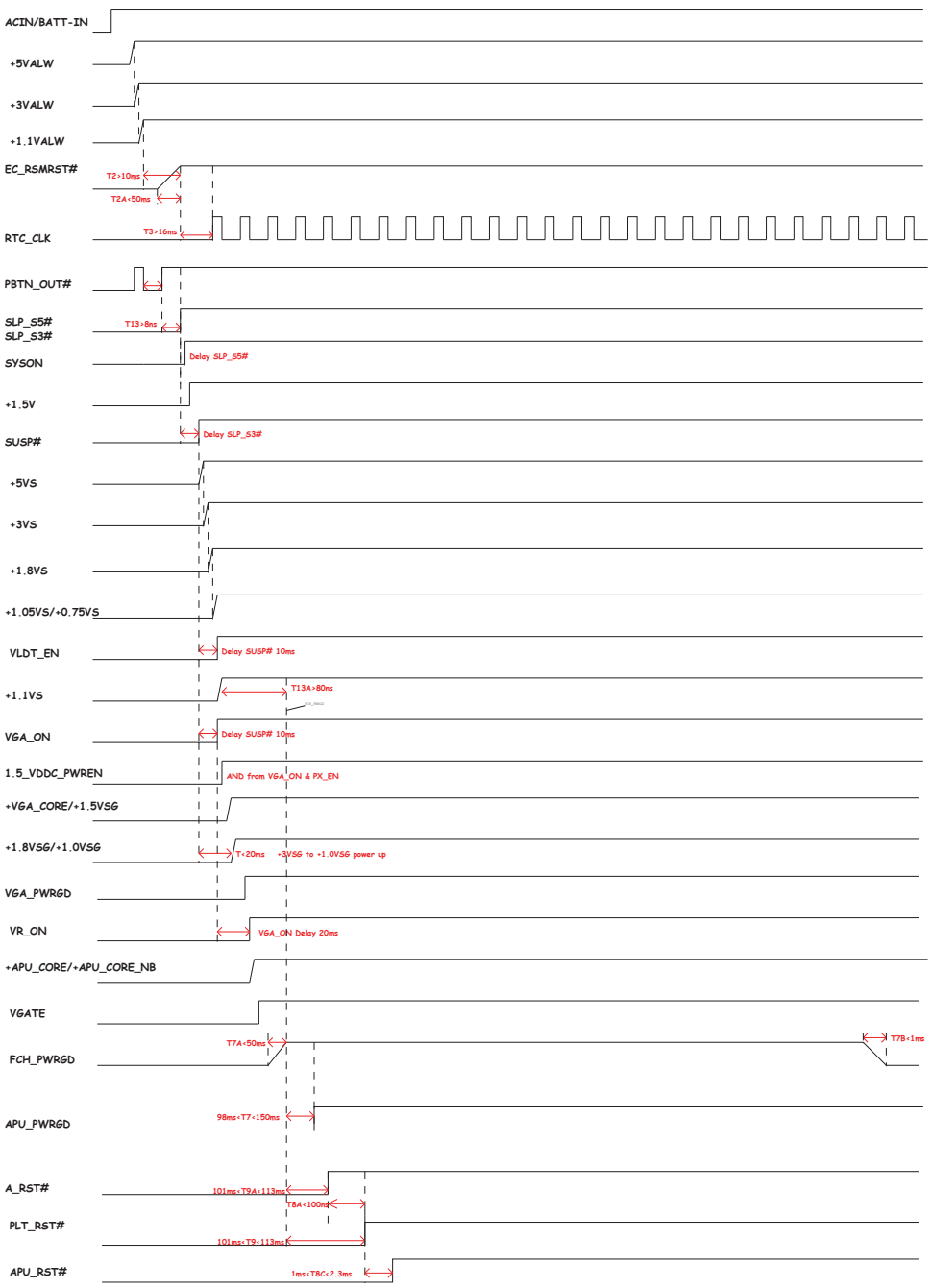
Title: VGA_CORE

Size | Document Number: QBL50 LA-7551P | Rev 1.0

Date: Wednesday, April 27, 2011 | Sheet 48 of 53

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					

POWER SEQUENCE



Security Classification	Compal Secret Data		
Issued Date	2010/08/30	Deciphered Date	2011/12/31

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Title: Power Sequence

Size	Document Number	Rev
	QBL50 LA-7551P	1.0

Date: Wednesday, April 27, 2011 Sheet of

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For AMD reuqest	0.11	PG#26	Translator change to ANX3110	03/15	ER
2		For AI charge function	0.11	PG#34	Add U2 & U56	03/15	ER
3		For PBL60 MEMO	0.11	PG#32	Change LED1 to Green color.	03/15	ER
4		For switch quality of ME.	0.11	PG#37	Change SW5,SW6 to 100g switch for ME.	03/15	ER
5		For LED brightness.	0.11	PG#32	Change R1584 to 200 ohm. Change R1586,R1588,R1591,R1592,R1593 to 100 ohm	03/15	ER
6		For DFB.	0.12	PG#11	JDIMM1 footprint change to FOX_AS0A626-J8SG-7H_204P-T	03/17	ER
7		For USB3.0 & AI charge.	0.12	PG#34	USBP0 connect to JUSB1 and USBP10 connect to JUSB2.	03/17	ER
8		For Back light function.	0.12	PG#36	U31.15 connect to ENBKL from APU.	03/17	ER
9		For HDMI HPD issue.	0.12	PG#10	Q34 change to 2N7002(ESD) Add R469 to +1.5VS.	03/19	ER
10		For DP0_HPD & DP1_HPD from AMD recommend.	0.12	PG#10	Swap Q13.1 & Q13.3, R618 unmount. Swap Q16.1 & Q16.3, R627 unmount.	03/19	ER
11		For Travis Vendor request	0.12	PG#26	Del DP0_TXN0_C & DP0_TXP0_C	03/22	ER
12		For LED1	0.12	PG#32	LED1 connect to +3VALW	03/22	ER
13		For EC SMBUS	0.2	PG#36	R1021,R1022 change to install.	03/24	ER
14		For Sourcer recommend	0.2		SE100105Z80 change to SE000000K80	03/24	ER
15		For Sourcer recommend	0.2		SE103225Z80 change to SE000008880	03/24	ER
16		For Sourcer recommend	0.2		SB000006A00 change to SB000006A10	03/24	ER
17		For Thermal	0.2	PG#37	Del H4	03/24	ER
18		For +5VS rising time	0.2	PG#38	R1103 change to 47K	03/24	ER
19		For Crystal EA	0.2	PG#29	C1634 change to 12P & C1633 change to 15P	03/24	ER
20		For Crystal EA	0.2	PG#13	C1200 & C1201 change to 12P	03/24	ER
21		For Crystal EA	0.2	PG#19	C353 change to 15P & C354 change to 12P	03/24	ER
22		For EMI request	0.2	PG#36	R1033 change to SM01000DI00 R1055 change to 33 ohm	03/24	ER
23		For EMI request	0.2	PG#28	L38,L39,L40,L41 change to SM070001S00	03/24	ER
24		For EMI request	0.2	PG#27	D1,D2,D3,D6 change to install	03/24	ER
25		For Crystal EA	0.2	PG#13	C1205,C1206 change to 10P	03/24	ER
26		For AI charge	0.2	PG#36 PG#34	U2 reserve CEN# to EC	03/25	ER
27		For AMD spec	0.2	PG#27	R1642 & R1646 change to 4.6K ohm	03/29	ER

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2011/12/31

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Compal Electronics, Inc.

Title: HW-PIR

Size: Custom | Document Number: QBL50 LA-7551P | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 51 of 53

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For EMI reuqest	0.2	PG#30	R1555,R1556,R1557,R1558 change to 0.1uf	03/29	ER
2		For share ROM reuqest	0.2	PG#15 PG#16	U28,R626,R934,R935,R35 change to Un-install R921 change un-install & U910 change to install	03/29	ER
3		For EMI reuqest	0.2	PG#34	D5 change to SC300001Y00 (YSCLAMP0524P)	03/29	ER
4		For Crystal vendor recommend	0.21	PG#13	Y4 change to SJ100007N00 (32.768K 7PF)	04/07	PR
5		For EMI recommend	0.21	PG#29	TS1 change to SP050006F00 (IH-160)	04/07	PR
6		For discharge EA	0.21	PG#38	R1127 change from 470 ohm to 33 ohm	04/07	PR
7		For leakage current	0.21	PG#27	R1644,R1645,Q101 change to install R4,R31 change to un-install	04/07	PR
8		For EMI recommend	0.21	PG#29	C1636 change from 1000P to 120P	04/08	PR
9		For thermal recommend	0.21	PG#19	Add R78, R79, R80, R82	04/18	PR
10		Reserve PX_EN signal	0.21	PG#36	Reserve signal PX_EN to EC pin 74	04/18	PR
11		Swap JDIMM1 & JDIMM2 location	0.21	PG#11 PG#12	Follow ME BOM	04/18	PR
12		Do not use for MP	0.21	PG#35	Del SW3 SW4	04/18	PR
13		Change Boarrd ID to PR10	0.21	PG#37	Change R1036 to 18k	04/18	PR
14		For DFB request del co-lay schematiic	0.21	PG#34	Del R672~R675, R664~R667	04/18	PR
15		For EMI request	0.22	PG#29	ADD D7	04/19	PR
16		For EMI request	1.0	PG#13	unstuff C1193	04/25	PR
17		For Customer change FCH P/N	1.0	PG#13 ~17	location U25, for M2 change to SA000042C80, M3 change to SA000043ID0	04/25	PR
18		For ESD request	1.0	PG#32	R628,R629,R678,R679,R680,R681 change from 0ohm to 33ohm & Add 1uF for C560,C568,C569,C570,C573,C571	04/27	PR
19							
20							
21							
22							
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27							

Security Classification: Compal Secret Data
Issued Date: 2010/06/30 Deciphered Date: 2011/12/31

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For MP cost down	1.0		As picture	03/15	PR
2							
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21							
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23							
24							
25							
26							
27							

Reference	Value	Source Part	Source Library	Page	Schematic
R22	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R23	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R24	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R26	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R27	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R28	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R81	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P14-HUD...	SCHEMA...
R483	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P23-VRA...	SCHEMA...
R485	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P23-VRA...	SCHEMA...
R511	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P24-VRA...	SCHEMA...
R513	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P24-VRA...	SCHEMA...
R537	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P06-FS1 ...	SCHEMA...
R538	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P06-FS1 ...	SCHEMA...
R591	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P08-FS1 ...	SCHEMA...
R598	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P08-FS1 ...	SCHEMA...
R606	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P08-FS1 ...	SCHEMA...
R608	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P08-FS1 ...	SCHEMA...
R611	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P08-FS1 ...	SCHEMA...
R647	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P29-LAN ...	SCHEMA...
R912	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P16-HUD...	SCHEMA...
R945	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R1291	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P26-LVD...	SCHEMA...
R1575	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P32-Mini...	SCHEMA...
R1577	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P32-Mini...	SCHEMA...
R1634	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P27-LVD...	SCHEMA...
R1635	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P27-LVD...	SCHEMA...
R1636	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P27-LVD...	SCHEMA...
R1641	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P27-LVD...	SCHEMA...
R1651	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P27-LVD...	SCHEMA...
R19	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R20	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R25	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R560	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P29-LAN ...	SCHEMA...
R658	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P29-LAN ...	SCHEMA...
R1049	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P35-FAN ...	SCHEMA...
R1145	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R1148	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R1534	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P30-HD ...	SCHEMA...
R1537	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P30-HD ...	SCHEMA...
R1560	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P31-RTS...	SCHEMA...
R1643	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P27-LVD...	SCHEMA...
R1650	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P27-LVD...	SCHEMA...
R570	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P26-LVD...	SCHEMA...
R607	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P26-LVD...	SCHEMA...
R937	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R938	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R941	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R1531	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P30-HD ...	SCHEMA...
R1595	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P33-HDD...	SCHEMA...
R1598	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P33-HDD...	SCHEMA...

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