

Compal Confidential

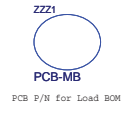
QCL40 MB Schematic Document

LA-8221P

Rev: 0.2

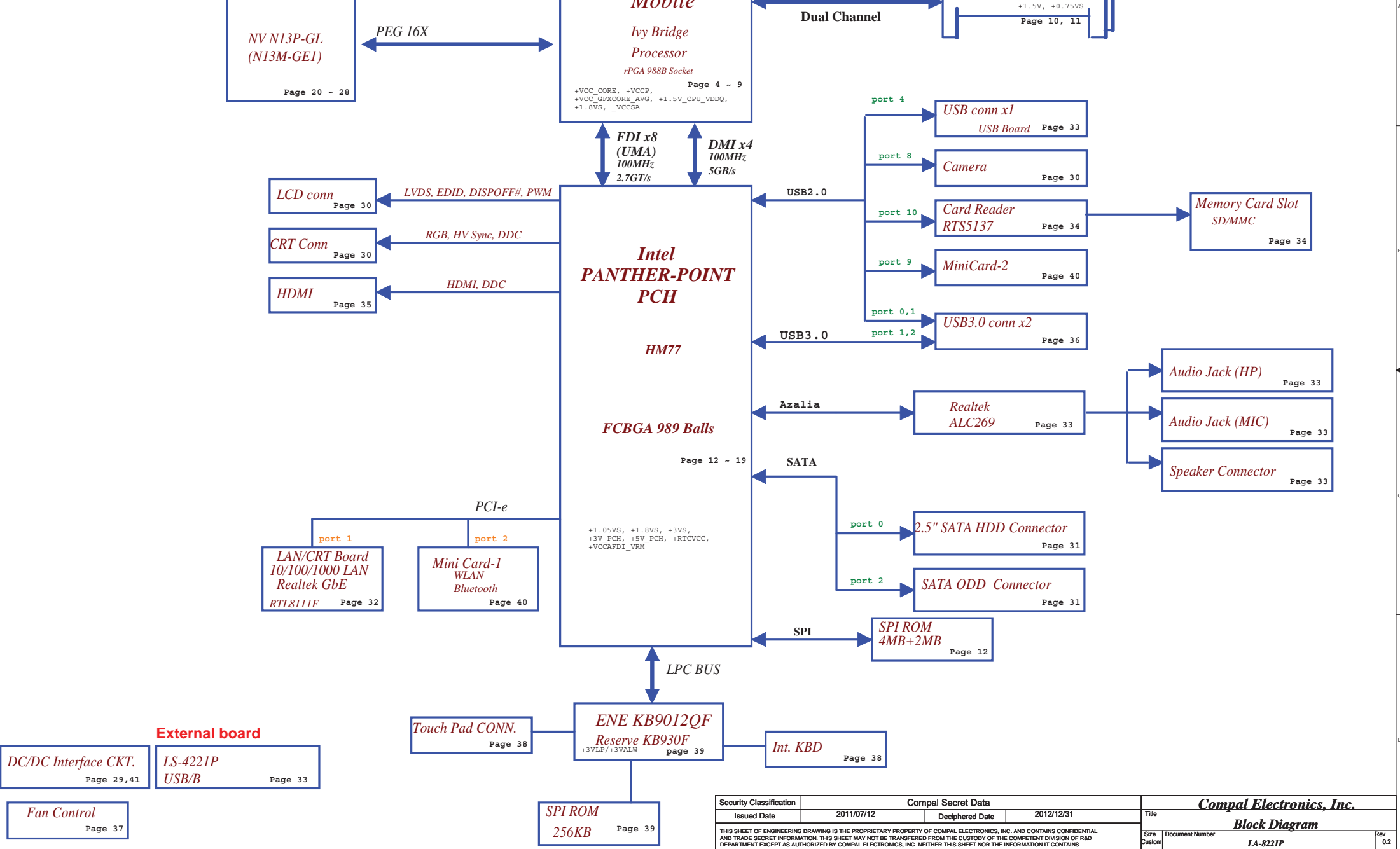
2011.09.28

Security Classification	Compal Secret Data			Title <i>Compal Electronics, Inc.</i>		
Issued Date	2011/07/12	Deciphered Date	2012/12/31	Size	Document Number	Rev
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				Date:	Wednesday, October 26, 2011	Sheet



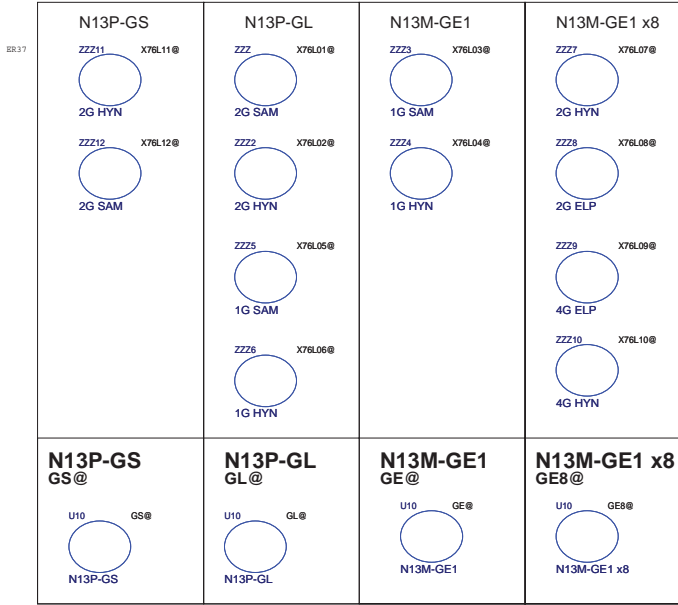
QCL40

PCB P/N for Load BOM



Security Classification	Compal Secret Data		Title	
Issued Date	2011/07/12	Deciphered Date	2012/12/31	Block Diagram
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X76 @: VRAMX16X8 VRAMX16X4 VRAMX8X8



CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	LPC Debug Port
PCI4	None

PCH	USB3 PORT	DESTINATION
	1	USB2.0+3.0
	2	USB2.0+3.0
	3	None
	4	None

PCH	USB2 PORT	DESTINATION
	0	USB2.0+3.0
	1	USB2.0+3.0
	2	None
	3	None
	4	JMINI1 (WLAN) Bluetooth
	5	None
	6	None
	7	None
	8	CAMERA
	9	USB2
	10	Card Reader
	11	None
	12	None
13	None	

Voltage Rails

Power Plane	Description	S1	S3	Deep S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+3VLP	3.3V power rail for 510N power management	ON	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+LAN_IO	3.3V power rail for ethernet	ON	ON	OFF	OFF
+3VS_WLAN	3.3V power rail for WLAN/BT Combo	ON	OFF	OFF	OFF
+3V_PCH	3.3V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+3VS	3.3V power rail for DDR SPI,PCH,HDD,Audio,Card Reader	ON	OFF	OFF	OFF
+3VSG	3.3V power rail for VGA	ON	OFF	OFF	OFF
+LCDVDD	3.3V power rail for LCD	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+5V_PCH	5V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+5VS	5V power rail for HDD,AUDIO,FAN,Touch PAD	ON	OFF	OFF	OFF
+5VS_ODD	5V power rail for SATA ODD	ON	OFF	OFF	OFF
+1.8VS	1.8V power rail for CPU,PCH	ON	OFF	OFF	OFF
+1.05VS	1.05V power rail for PCH	ON	OFF	OFF	OFF
+VCCP	1.05V power rail for CPU VCCIO,PCH	ON	OFF	OFF	OFF
+1.05VSG	1.05V power rail for N13P	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR3 system memory	ON	ON	ON	OFF
+1.5V_CPU_VDDQ	1.5V power rail CPU VDDQ	ON	OFF	OFF	OFF
+1.5VSG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+1.5VS	1.5V power rail for PCH,WLAN/BT combo	ON	OFF	OFF	OFF
+0.75VS	0.75V power rail for DDR VREF	ON	OFF	OFF	OFF
+VCCSA	VCCSA for CPU system agent	ON	OFF	OFF	OFF
+VCC_CORE	CORE Voltage for CPU	ON	OFF	OFF	OFF
+VCC_GFXCORE_AXG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+VGA_CORE	CORE Voltage for N13P Graphics ON OFF OFF	ON	OFF	OFF	OFF

DIS @: VGA componet
GSL @: N13P-GL or N13M-GE1
GSL @: N13P-GL or N13P-GS
GS @: N13P-GS

930 @: EC(ENE 930 chip)
XDP @: Intel debug port

IU3 @: USB3.0 by PCH
USB30 @: USB3.0 controller IC

AI @: AI Charger
NAI @: Non AI Charger

9012 @: EC(ENE 9012 chip)

SMBUS Control Table

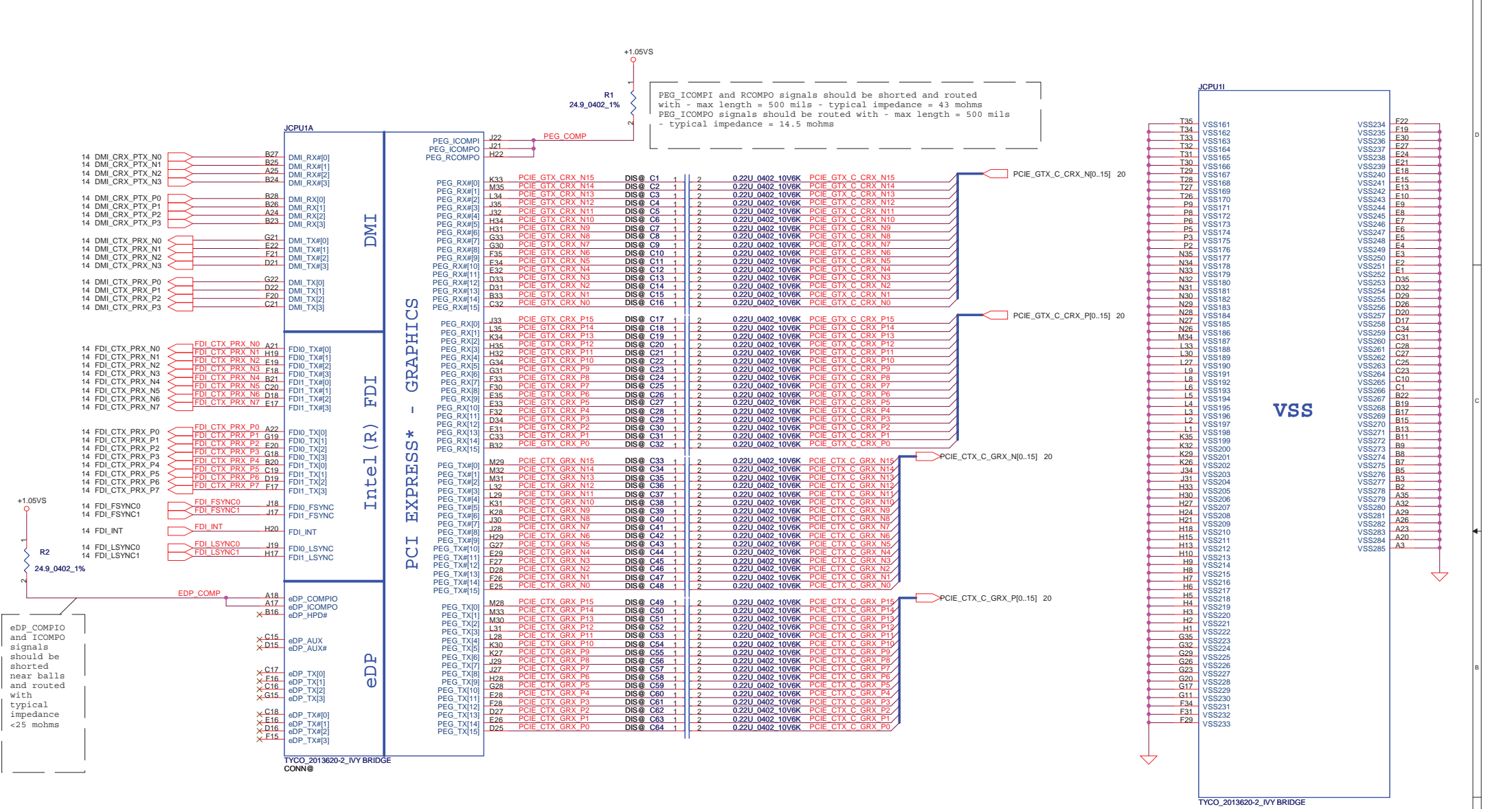
	SOURCE	MINI1	BATT	PCH	EC	SODIMM	DGPU
EC_SMB_CK1 EC_SMB_DAI	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DAI2	KB930	X	X	V	X	X	V
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	X	X	V	X
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	V	X	V

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	CLK_SD_48M
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	USB3.0 controller	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :
 : means Digital Ground
 : means Analog Ground

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD WLAN
Lane 3	None
Lane 4	USB3.0 controller
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None



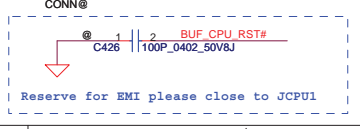
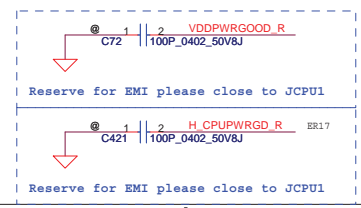
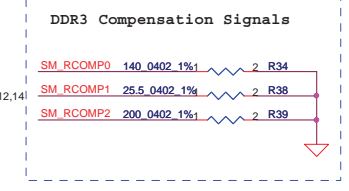
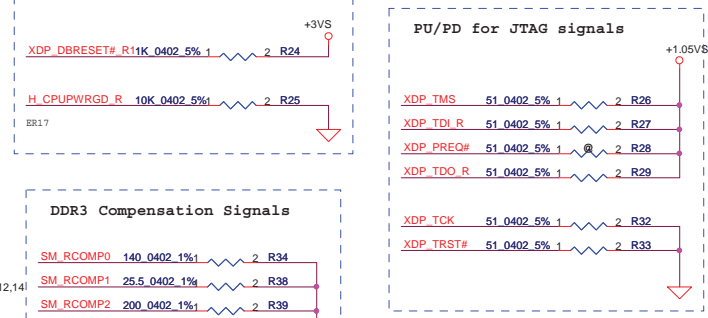
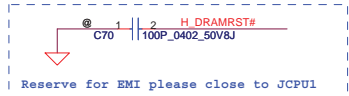
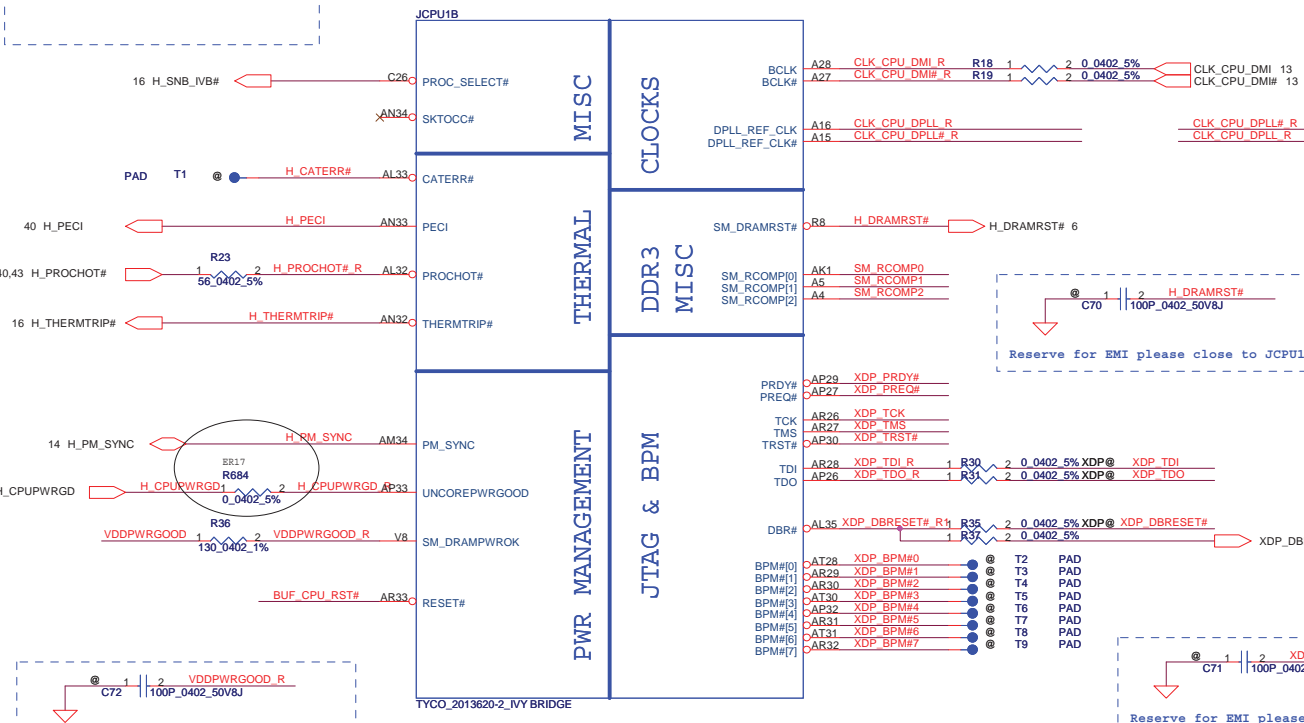
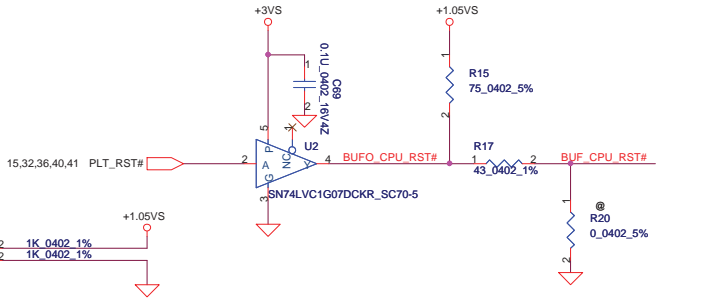
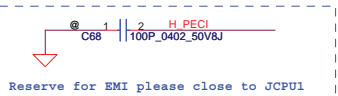
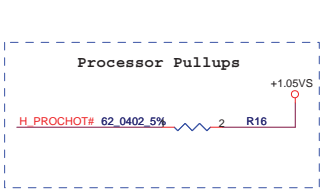
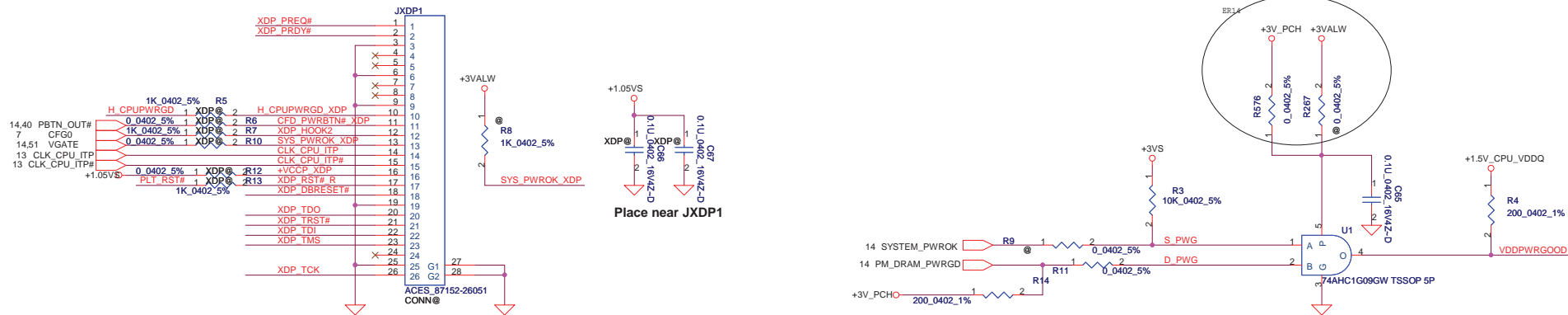
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Signal	Pin	Dis	Dir	Rate	Imp	Target
PEG_RX[0]	K33	PCIE GTX CRX N15	DIS@ C1	1	2	0.22u 0402 10V6K PCIE GTX C CRX N15
PEG_RX[1]	M33	PCIE GTX CRX N14	DIS@ C2	2	2	0.22u 0402 10V6K PCIE GTX C CRX N14
PEG_RX[2]	L34	PCIE GTX CRX N13	DIS@ C3	1	2	0.22u 0402 10V6K PCIE GTX C CRX N13
PEG_RX[3]	J35	PCIE GTX CRX N12	DIS@ C4	1	2	0.22u 0402 10V6K PCIE GTX C CRX N12
PEG_RX[4]	J32	PCIE GTX CRX N11	DIS@ C5	1	2	0.22u 0402 10V6K PCIE GTX C CRX N11
PEG_RX[5]	H34	PCIE GTX CRX N10	DIS@ C6	1	2	0.22u 0402 10V6K PCIE GTX C CRX N10
PEG_RX[6]	H31	PCIE GTX CRX N9	DIS@ C7	1	2	0.22u 0402 10V6K PCIE GTX C CRX N9
PEG_RX[7]	G33	PCIE GTX CRX N8	DIS@ C8	1	2	0.22u 0402 10V6K PCIE GTX C CRX N8
PEG_RX[8]	G30	PCIE GTX CRX N7	DIS@ C9	1	2	0.22u 0402 10V6K PCIE GTX C CRX N7
PEG_RX[9]	F34	PCIE GTX CRX N6	DIS@ C10	1	2	0.22u 0402 10V6K PCIE GTX C CRX N6
PEG_RX[10]	F32	PCIE GTX CRX N5	DIS@ C11	1	2	0.22u 0402 10V6K PCIE GTX C CRX N5
PEG_RX[11]	E32	PCIE GTX CRX N4	DIS@ C12	1	2	0.22u 0402 10V6K PCIE GTX C CRX N4
PEG_RX[12]	D33	PCIE GTX CRX N3	DIS@ C13	1	2	0.22u 0402 10V6K PCIE GTX C CRX N3
PEG_RX[13]	D31	PCIE GTX CRX N2	DIS@ C14	1	2	0.22u 0402 10V6K PCIE GTX C CRX N2
PEG_RX[14]	B33	PCIE GTX CRX N1	DIS@ C15	1	2	0.22u 0402 10V6K PCIE GTX C CRX N1
PEG_RX[15]	C32	PCIE GTX CRX N0	DIS@ C16	1	2	0.22u 0402 10V6K PCIE GTX C CRX N0
PEG_RX[0]	J33	PCIE GTX CRX P15	DIS@ C17	1	2	0.22u 0402 10V6K PCIE GTX C CRX P15
PEG_RX[1]	K34	PCIE GTX CRX P14	DIS@ C18	1	2	0.22u 0402 10V6K PCIE GTX C CRX P14
PEG_RX[2]	J34	PCIE GTX CRX P13	DIS@ C19	1	2	0.22u 0402 10V6K PCIE GTX C CRX P13
PEG_RX[3]	H35	PCIE GTX CRX P12	DIS@ C20	1	2	0.22u 0402 10V6K PCIE GTX C CRX P12
PEG_RX[4]	H32	PCIE GTX CRX P11	DIS@ C21	1	2	0.22u 0402 10V6K PCIE GTX C CRX P11
PEG_RX[5]	G34	PCIE GTX CRX P10	DIS@ C22	1	2	0.22u 0402 10V6K PCIE GTX C CRX P10
PEG_RX[6]	G31	PCIE GTX CRX P9	DIS@ C23	1	2	0.22u 0402 10V6K PCIE GTX C CRX P9
PEG_RX[7]	F33	PCIE GTX CRX P8	DIS@ C24	1	2	0.22u 0402 10V6K PCIE GTX C CRX P8
PEG_RX[8]	F30	PCIE GTX CRX P7	DIS@ C25	1	2	0.22u 0402 10V6K PCIE GTX C CRX P7
PEG_RX[9]	E35	PCIE GTX CRX P6	DIS@ C26	1	2	0.22u 0402 10V6K PCIE GTX C CRX P6
PEG_RX[10]	E33	PCIE GTX CRX P5	DIS@ C27	1	2	0.22u 0402 10V6K PCIE GTX C CRX P5
PEG_RX[11]	F32	PCIE GTX CRX P4	DIS@ C28	1	2	0.22u 0402 10V6K PCIE GTX C CRX P4
PEG_RX[12]	D34	PCIE GTX CRX P3	DIS@ C29	1	2	0.22u 0402 10V6K PCIE GTX C CRX P3
PEG_RX[13]	E31	PCIE GTX CRX P2	DIS@ C30	1	2	0.22u 0402 10V6K PCIE GTX C CRX P2
PEG_RX[14]	C33	PCIE GTX CRX P1	DIS@ C31	1	2	0.22u 0402 10V6K PCIE GTX C CRX P1
PEG_RX[15]	B32	PCIE GTX CRX P0	DIS@ C32	1	2	0.22u 0402 10V6K PCIE GTX C CRX P0
PEG_TX[0]	M29	PCIE CTX GRX N15	DIS@ C33	1	2	0.22u 0402 10V6K PCIE CTX C GRX N15
PEG_TX[1]	M32	PCIE CTX GRX N14	DIS@ C34	1	2	0.22u 0402 10V6K PCIE CTX C GRX N14
PEG_TX[2]	M31	PCIE CTX GRX N13	DIS@ C35	1	2	0.22u 0402 10V6K PCIE CTX C GRX N13
PEG_TX[3]	L32	PCIE CTX GRX N12	DIS@ C36	1	2	0.22u 0402 10V6K PCIE CTX C GRX N12
PEG_TX[4]	L29	PCIE CTX GRX N11	DIS@ C37	1	2	0.22u 0402 10V6K PCIE CTX C GRX N11
PEG_TX[5]	K31	PCIE CTX GRX N10	DIS@ C38	1	2	0.22u 0402 10V6K PCIE CTX C GRX N10
PEG_TX[6]	K28	PCIE CTX GRX N9	DIS@ C39	1	2	0.22u 0402 10V6K PCIE CTX C GRX N9
PEG_TX[7]	J30	PCIE CTX GRX N8	DIS@ C40	1	2	0.22u 0402 10V6K PCIE CTX C GRX N8
PEG_TX[8]	J28	PCIE CTX GRX N7	DIS@ C41	1	2	0.22u 0402 10V6K PCIE CTX C GRX N7
PEG_TX[9]	H29	PCIE CTX GRX N6	DIS@ C42	1	2	0.22u 0402 10V6K PCIE CTX C GRX N6
PEG_TX[10]	G27	PCIE CTX GRX N5	DIS@ C43	1	2	0.22u 0402 10V6K PCIE CTX C GRX N5
PEG_TX[11]	E29	PCIE CTX GRX N4	DIS@ C44	1	2	0.22u 0402 10V6K PCIE CTX C GRX N4
PEG_TX[12]	F27	PCIE CTX GRX N3	DIS@ C45	1	2	0.22u 0402 10V6K PCIE CTX C GRX N3
PEG_TX[13]	D28	PCIE CTX GRX N2	DIS@ C46	1	2	0.22u 0402 10V6K PCIE CTX C GRX N2
PEG_TX[14]	F26	PCIE CTX GRX N1	DIS@ C47	1	2	0.22u 0402 10V6K PCIE CTX C GRX N1
PEG_TX[15]	E25	PCIE CTX GRX N0	DIS@ C48	1	2	0.22u 0402 10V6K PCIE CTX C GRX N0
PEG_TX[0]	M28	PCIE CTX GRX P15	DIS@ C49	1	2	0.22u 0402 10V6K PCIE CTX C GRX P15
PEG_TX[1]	M33	PCIE CTX GRX P14	DIS@ C50	1	2	0.22u 0402 10V6K PCIE CTX C GRX P14
PEG_TX[2]	M30	PCIE CTX GRX P13	DIS@ C51	1	2	0.22u 0402 10V6K PCIE CTX C GRX P13
PEG_TX[3]	L31	PCIE CTX GRX P12	DIS@ C52	1	2	0.22u 0402 10V6K PCIE CTX C GRX P12
PEG_TX[4]	L28	PCIE CTX GRX P11	DIS@ C53	1	2	0.22u 0402 10V6K PCIE CTX C GRX P11
PEG_TX[5]	K30	PCIE CTX GRX P10	DIS@ C54	1	2	0.22u 0402 10V6K PCIE CTX C GRX P10
PEG_TX[6]	K27	PCIE CTX GRX P9	DIS@ C55	1	2	0.22u 0402 10V6K PCIE CTX C GRX P9
PEG_TX[7]	J29	PCIE CTX GRX P8	DIS@ C56	1	2	0.22u 0402 10V6K PCIE CTX C GRX P8
PEG_TX[8]	J27	PCIE CTX GRX P7	DIS@ C57	1	2	0.22u 0402 10V6K PCIE CTX C GRX P7
PEG_TX[9]	G28	PCIE CTX GRX P6	DIS@ C58	1	2	0.22u 0402 10V6K PCIE CTX C GRX P6
PEG_TX[10]	G28	PCIE CTX GRX P5	DIS@ C59	1	2	0.22u 0402 10V6K PCIE CTX C GRX P5
PEG_TX[11]	E28	PCIE CTX GRX P4	DIS@ C60	1	2	0.22u 0402 10V6K PCIE CTX C GRX P4
PEG_TX[12]	F28	PCIE CTX GRX P3	DIS@ C61	1	2	0.22u 0402 10V6K PCIE CTX C GRX P3
PEG_TX[13]	D27	PCIE CTX GRX P2	DIS@ C62	1	2	0.22u 0402 10V6K PCIE CTX C GRX P2
PEG_TX[14]	E26	PCIE CTX GRX P1	DIS@ C63	1	2	0.22u 0402 10V6K PCIE CTX C GRX P1
PEG_TX[15]	D25	PCIE CTX GRX P0	DIS@ C64	1	2	0.22u 0402 10V6K PCIE CTX C GRX P0

TYCO_2013620-2_IVY BRIDGE

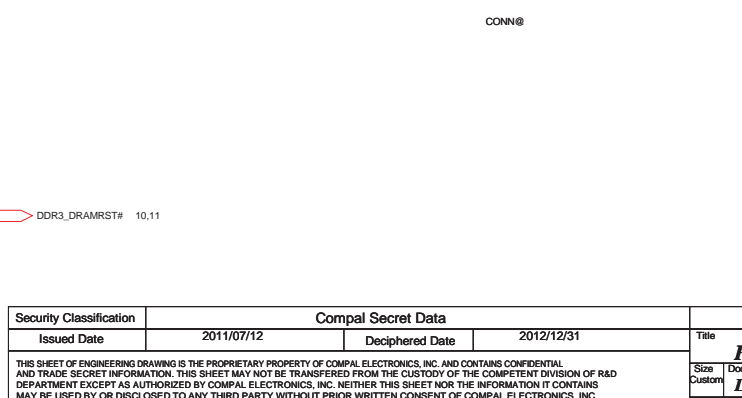
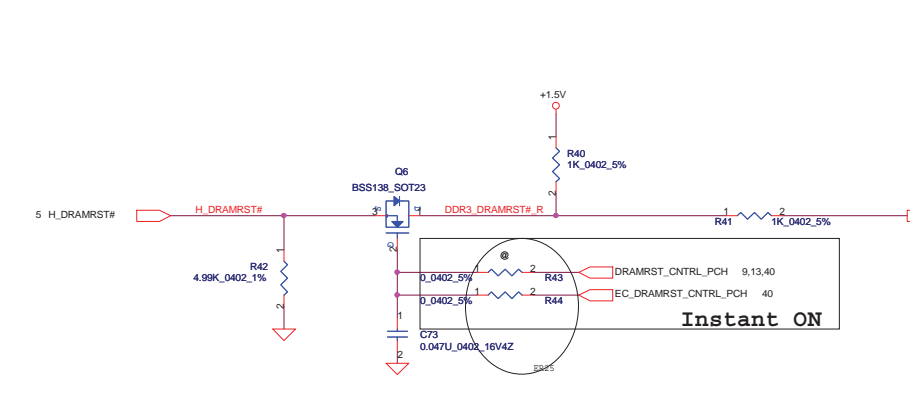
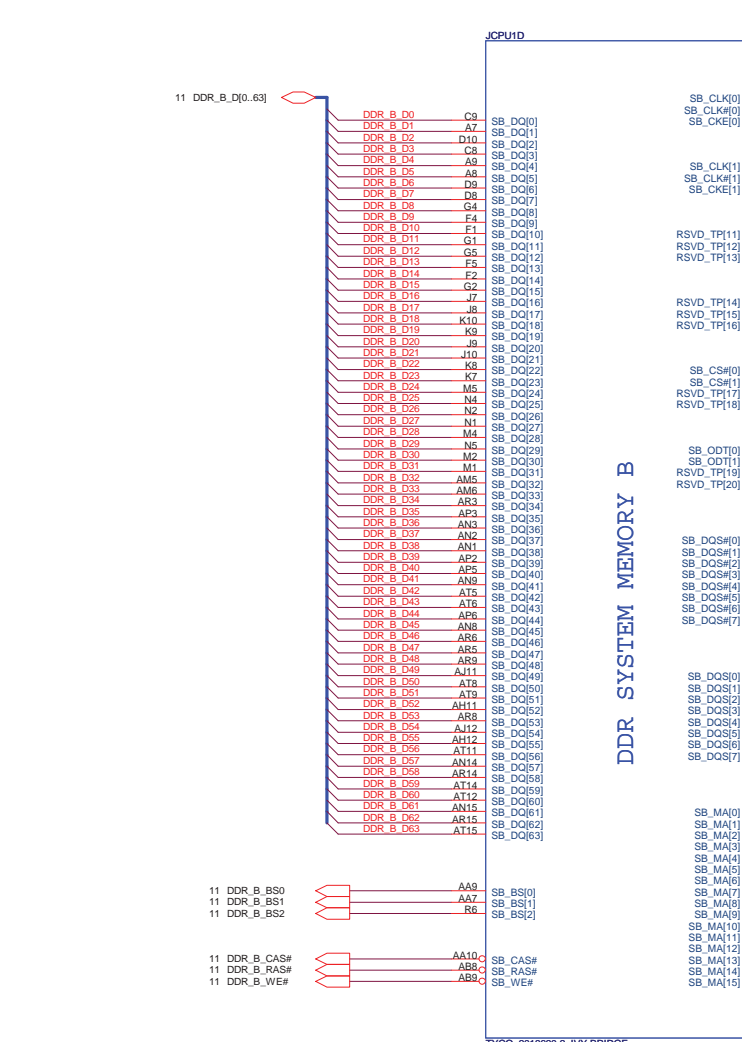
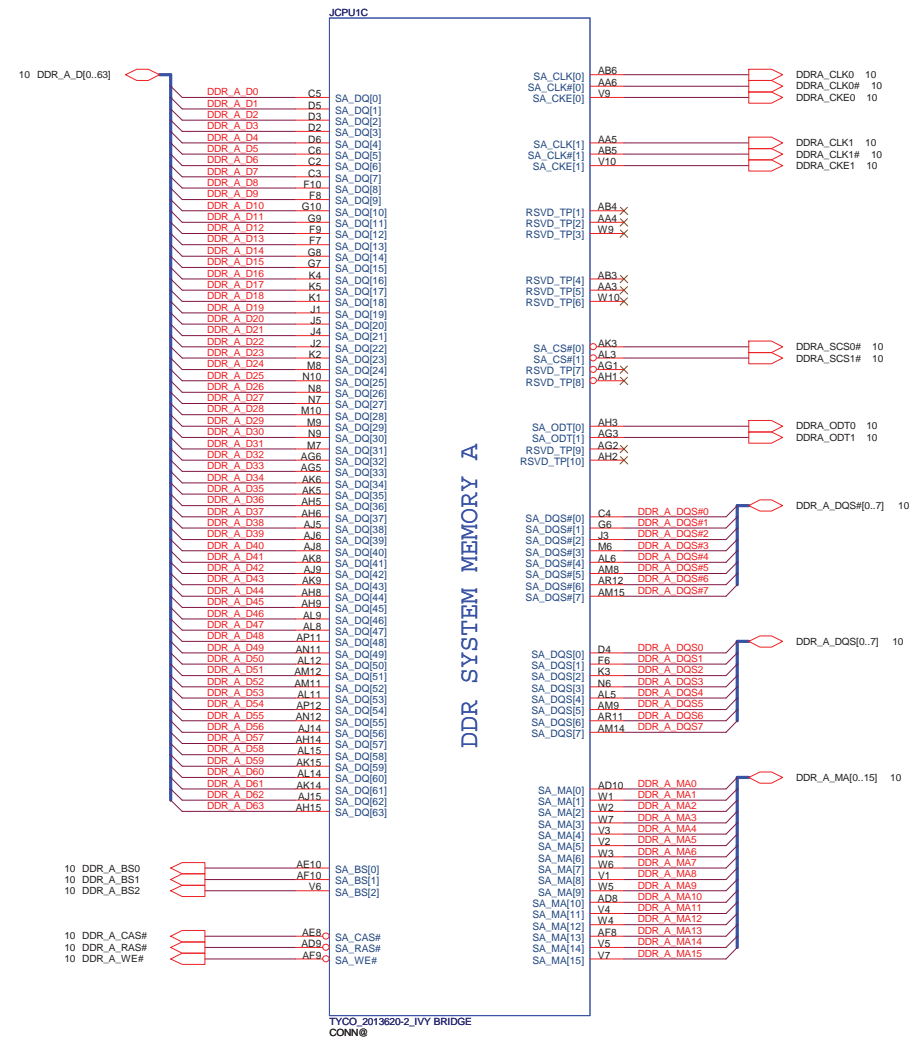
CONN@



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Issued Date	2011/07/12	Deciphered Date
		2012/12/31

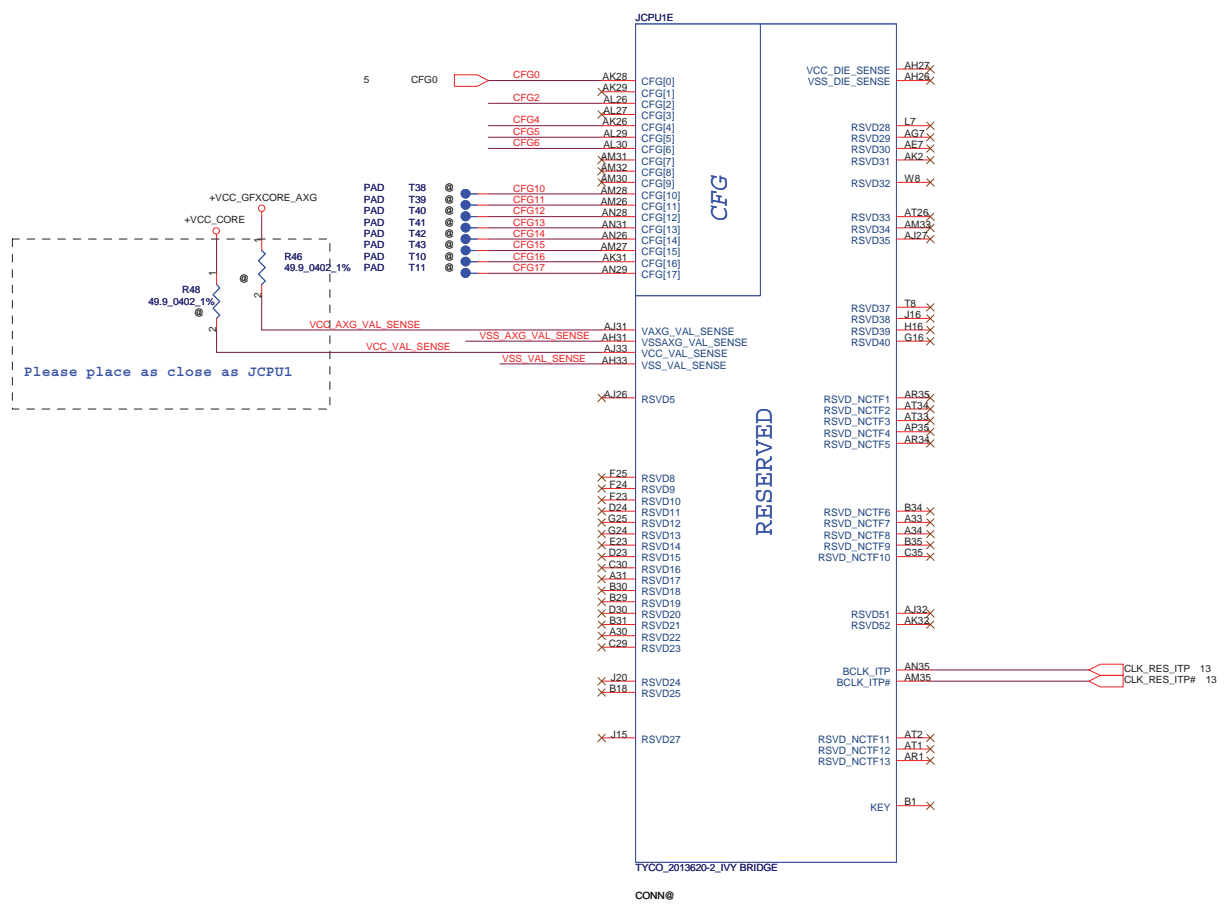
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Compal Electronics, Inc.		
PROCESSOR(2/6) PM,XDP,CLK		
Size Custom	Document Number LA-8221P	Rev 0.2
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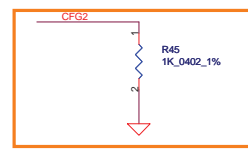


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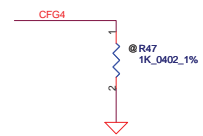
Title		Compal Electronics, Inc.	
PROCESSOR(3/6) DDRIII			
Size	Document Number	Rev	
Custom	LA-8221P	0.2	
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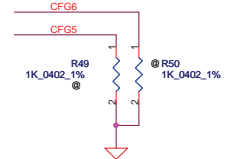
CFG Straps for Processor



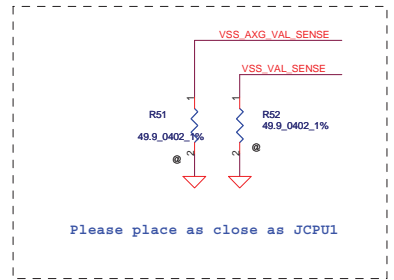
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



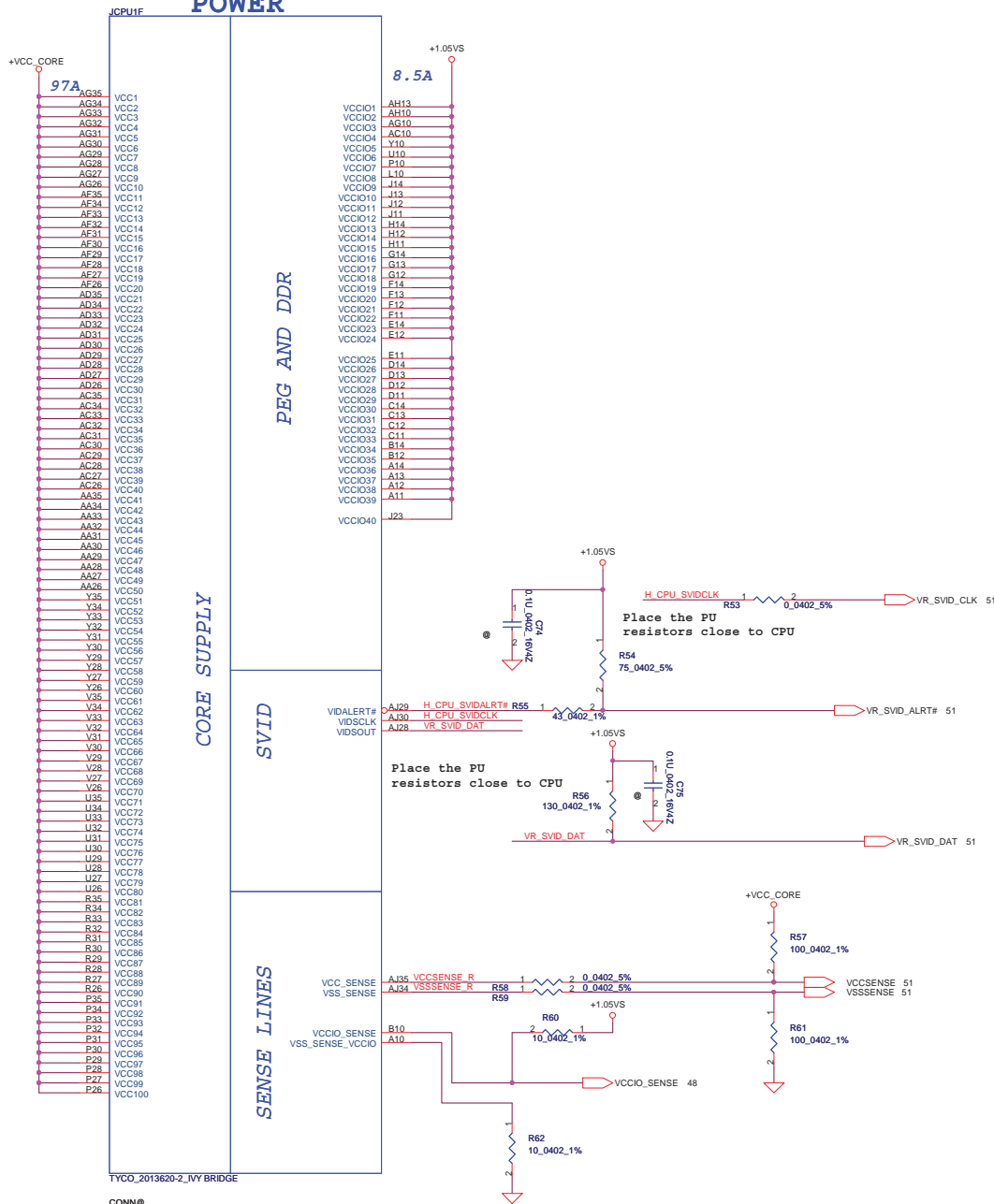
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



POWER



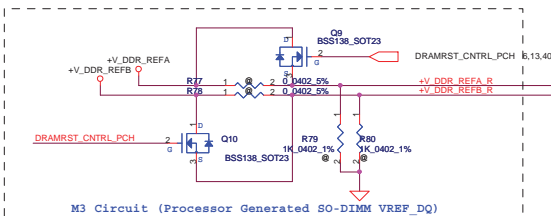
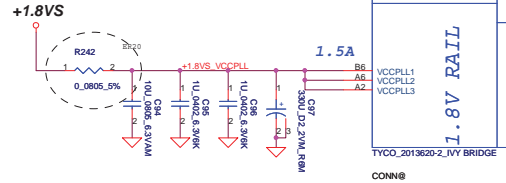
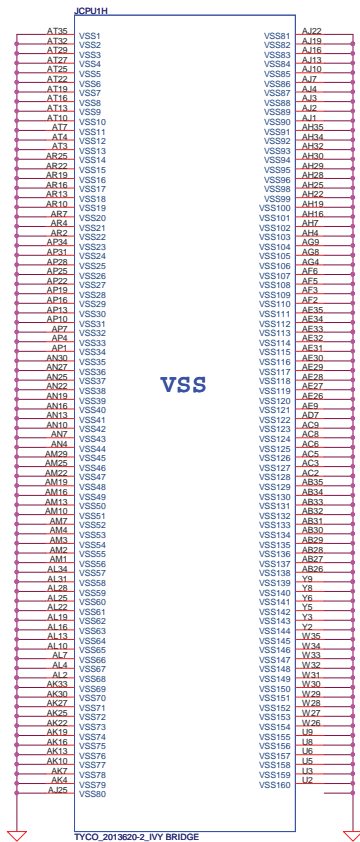
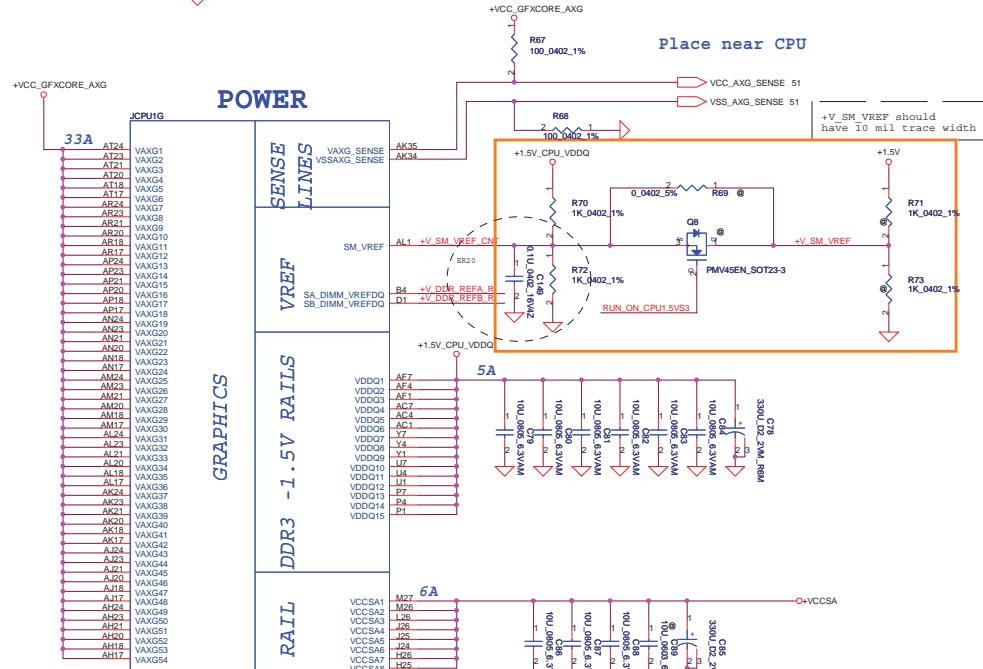
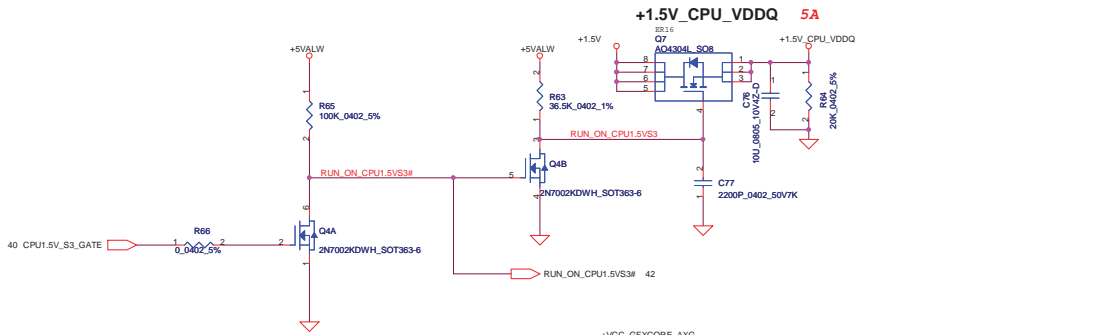
CORE SUPPLY

SVID

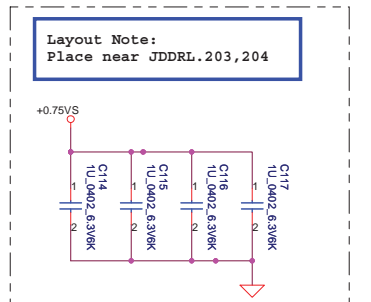
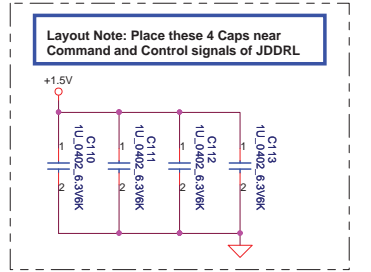
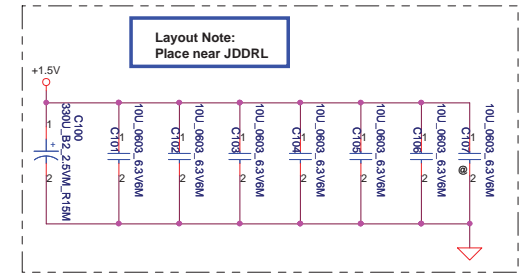
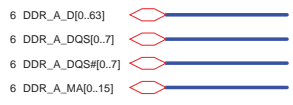
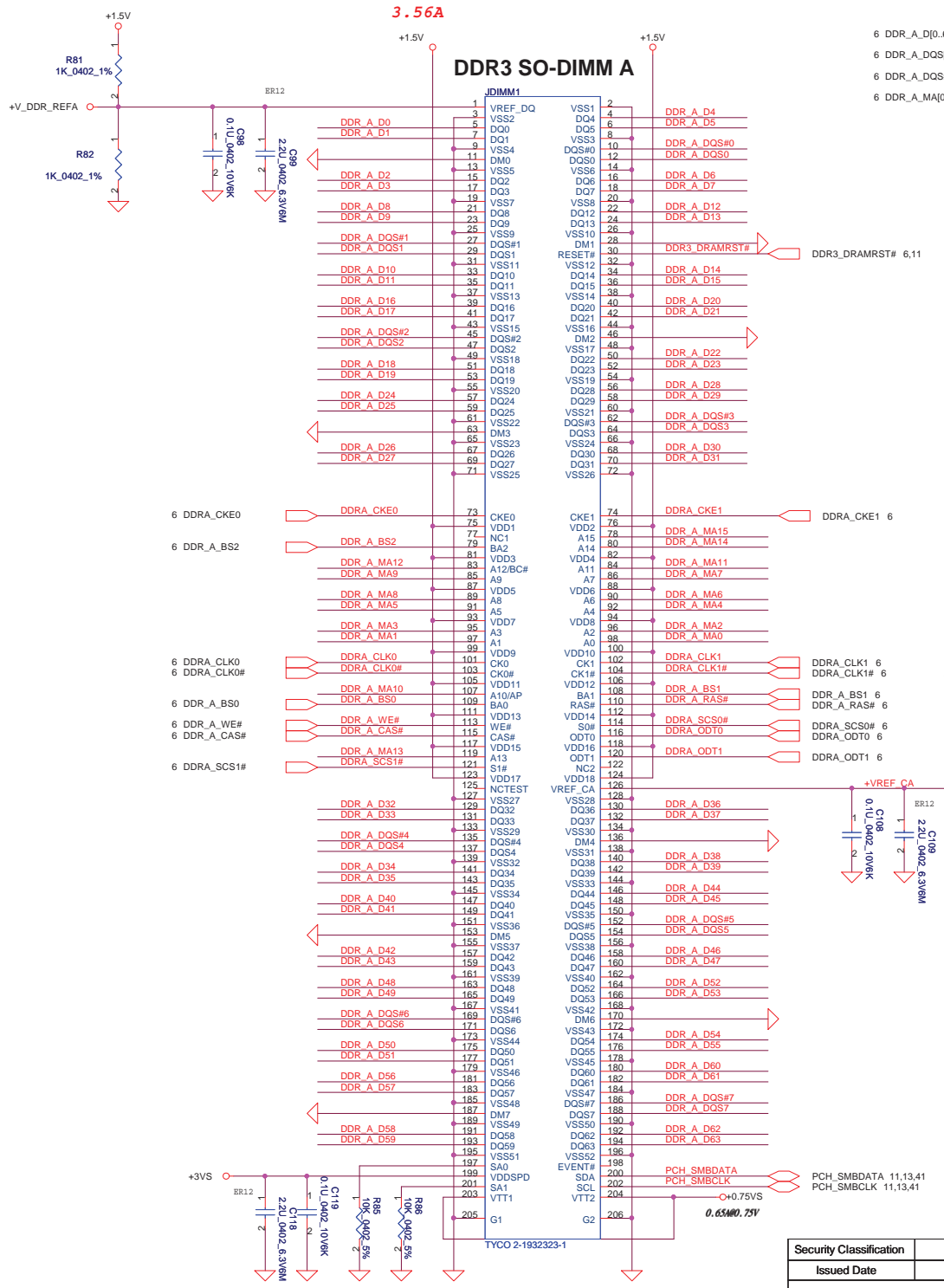
SENSE LINES

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Size	Document Number
Custom	LA-8221P
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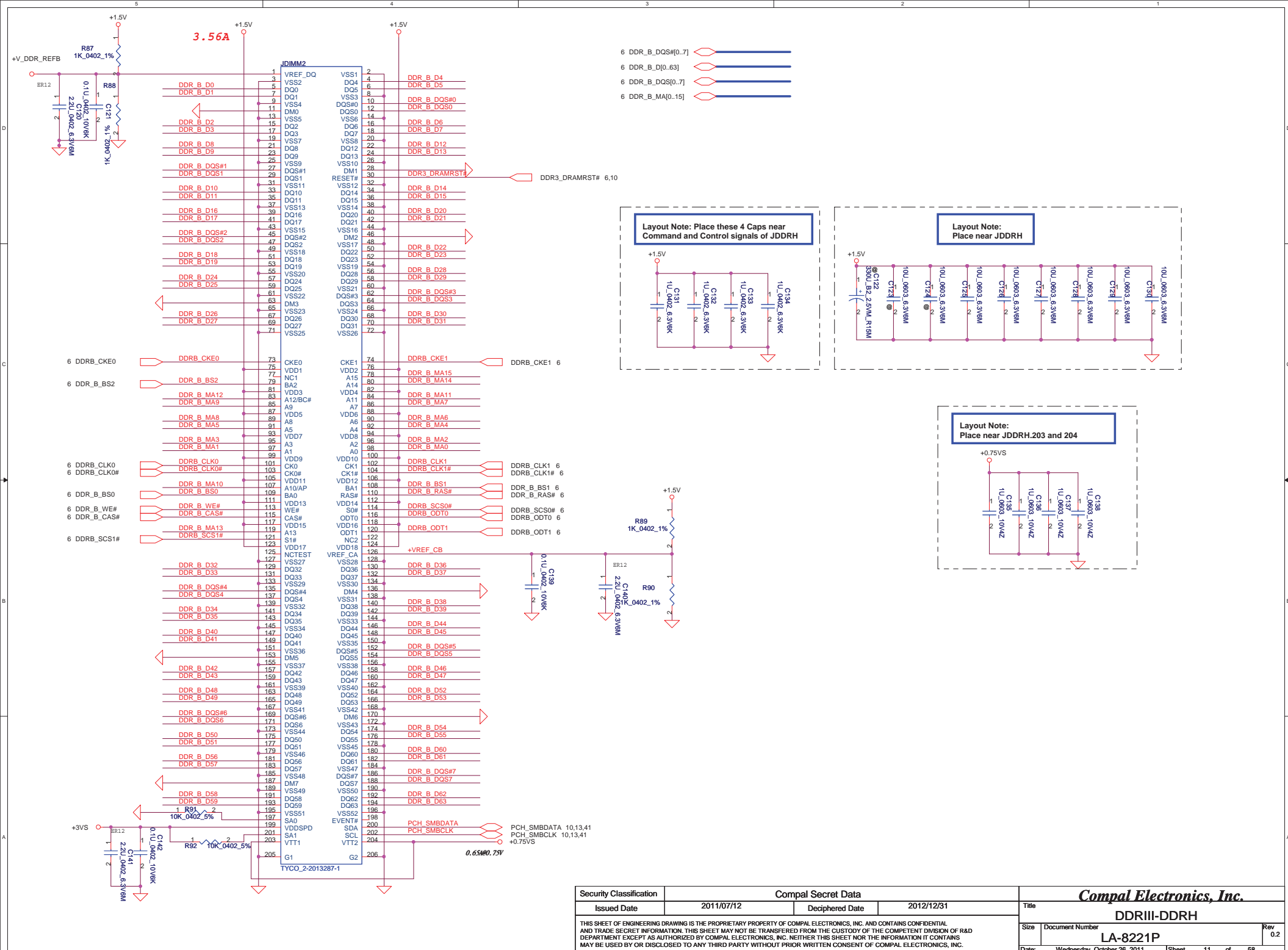
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Compal Electronics, Inc.

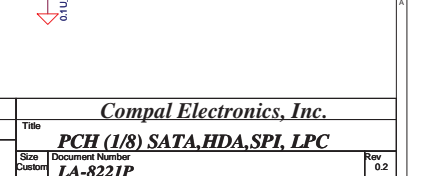
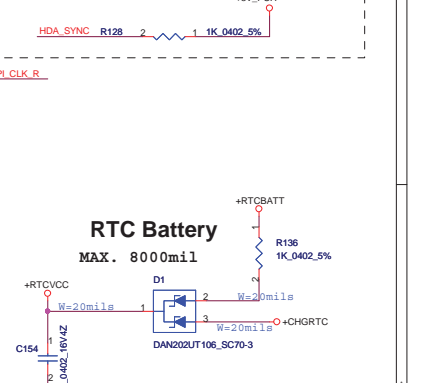
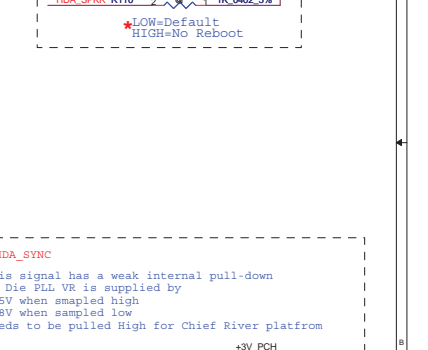
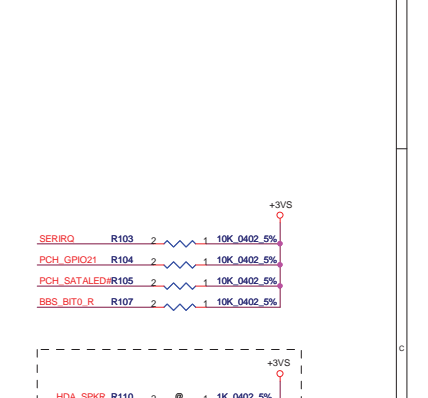
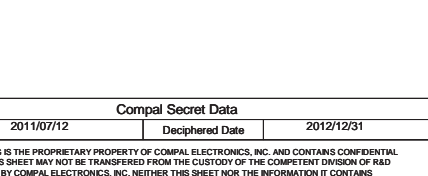
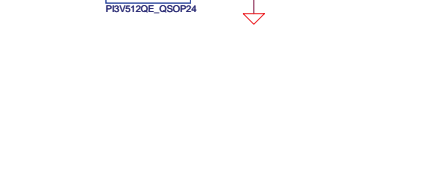
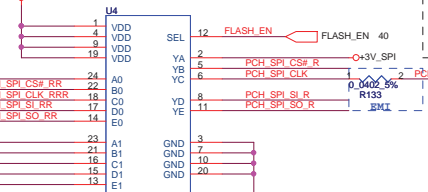
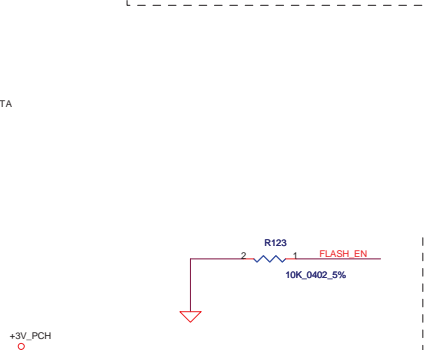
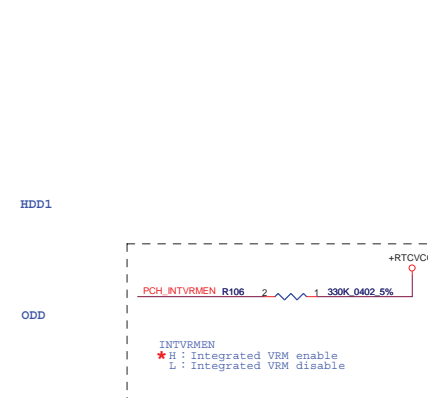
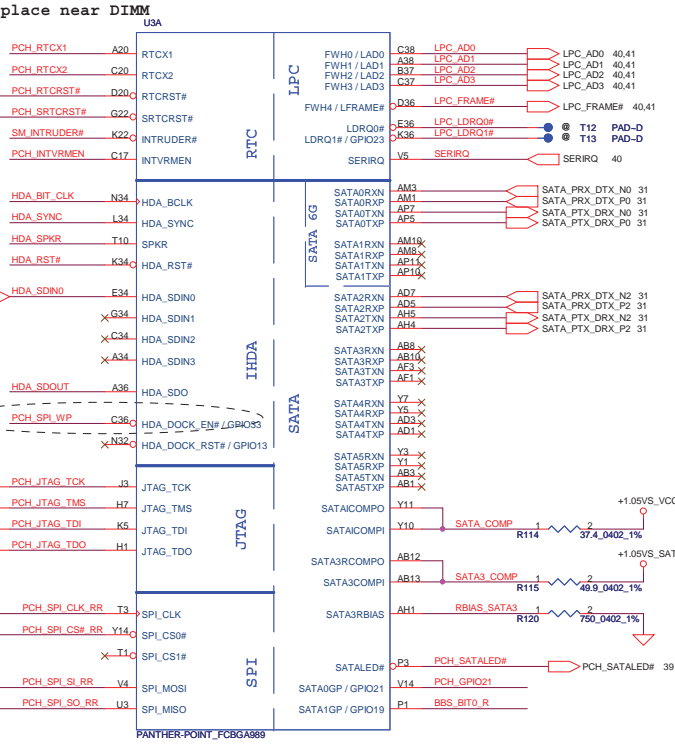
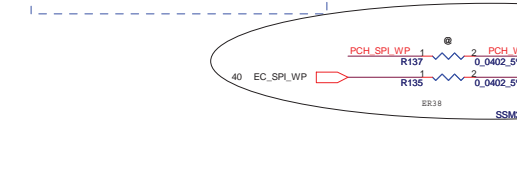
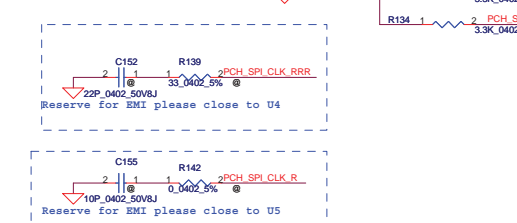
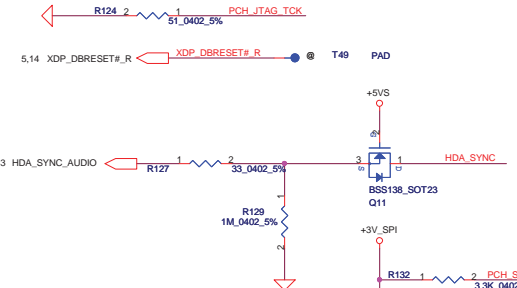
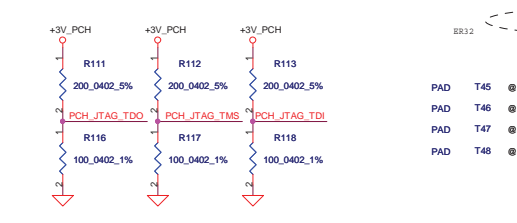
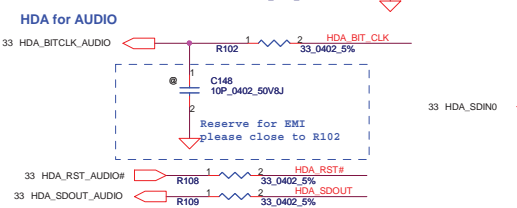
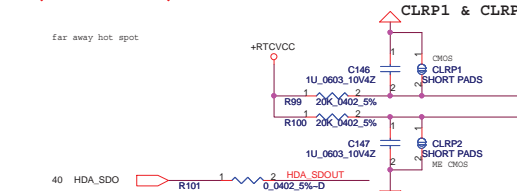
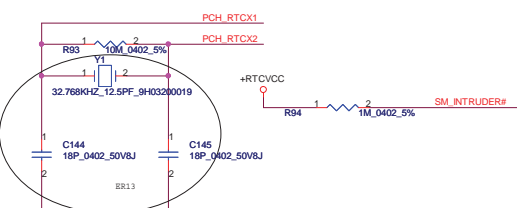
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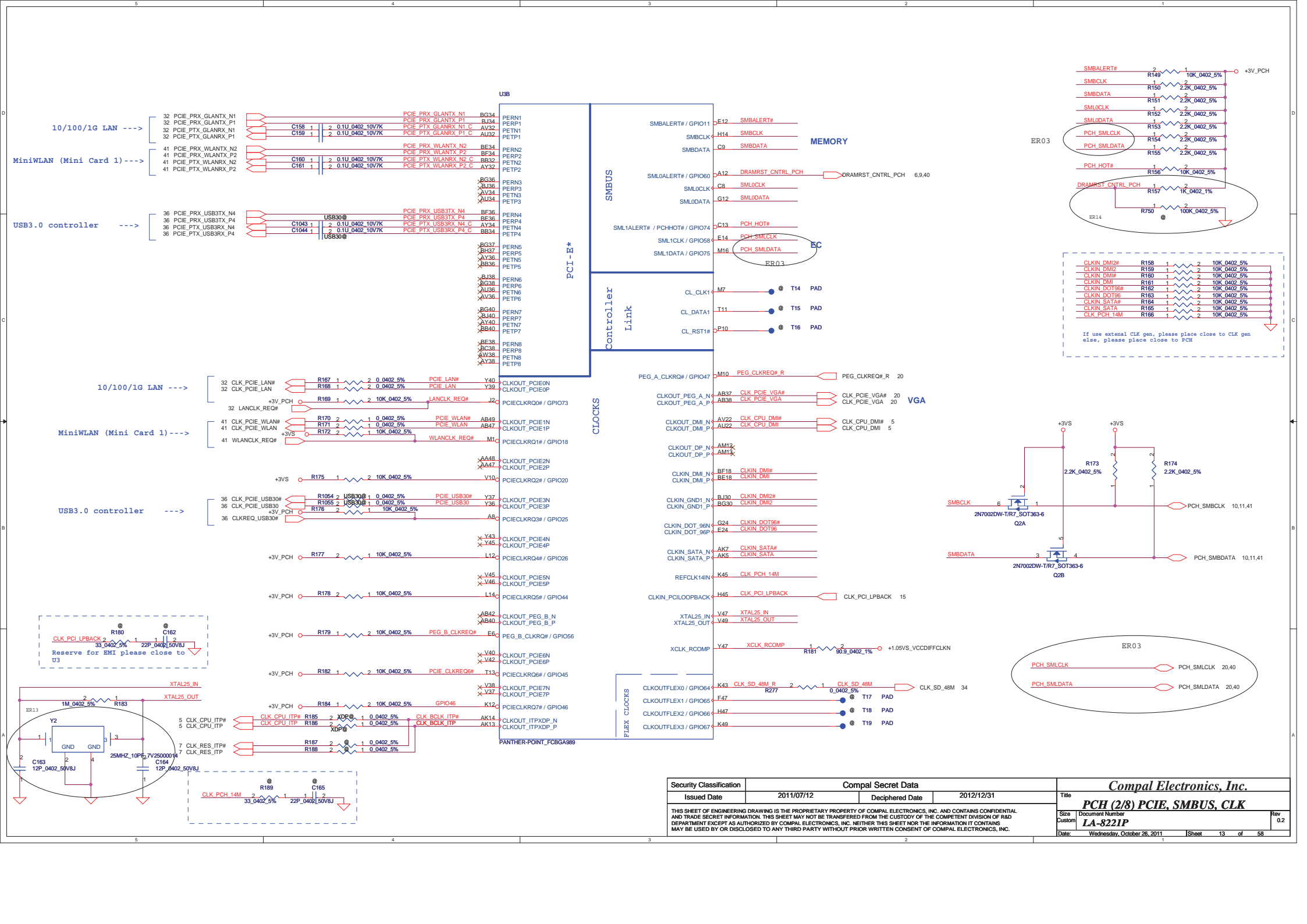
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Customer	LA-8221P	Date	Wednesday, October 26, 2011	Sheet	12 of 58



10/100/1G LAN ---->

MiniWLAN (Mini Card 1)---->

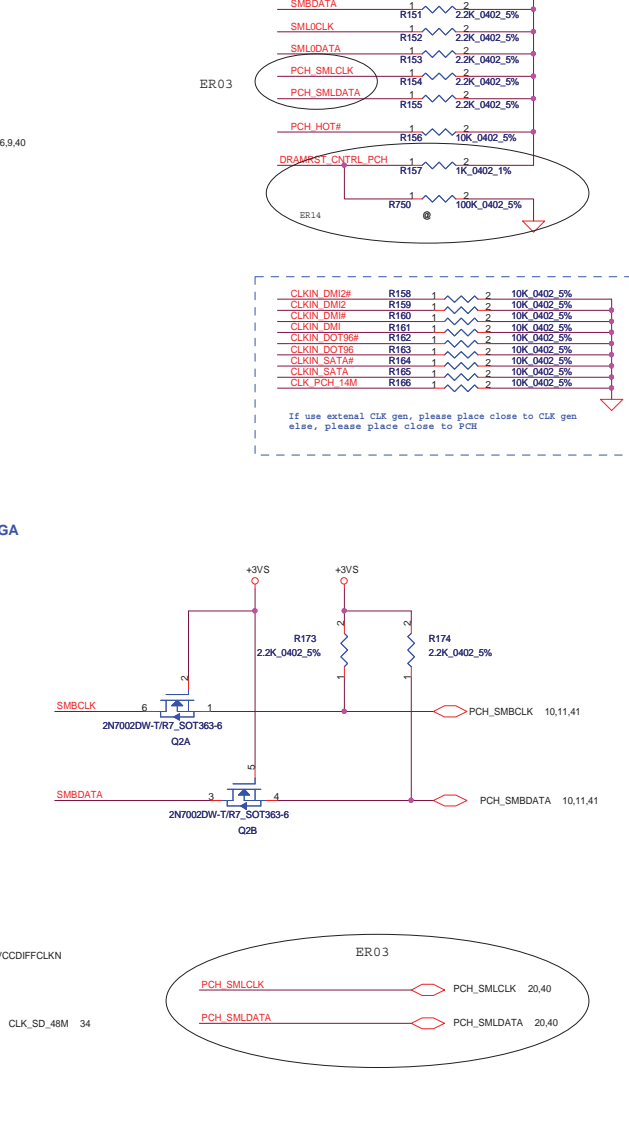
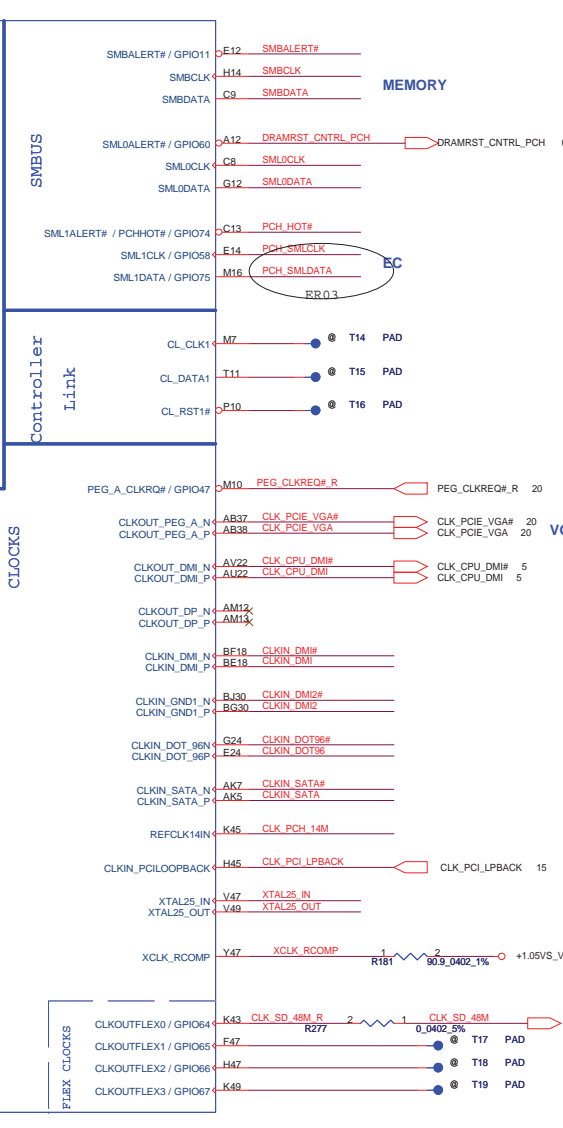
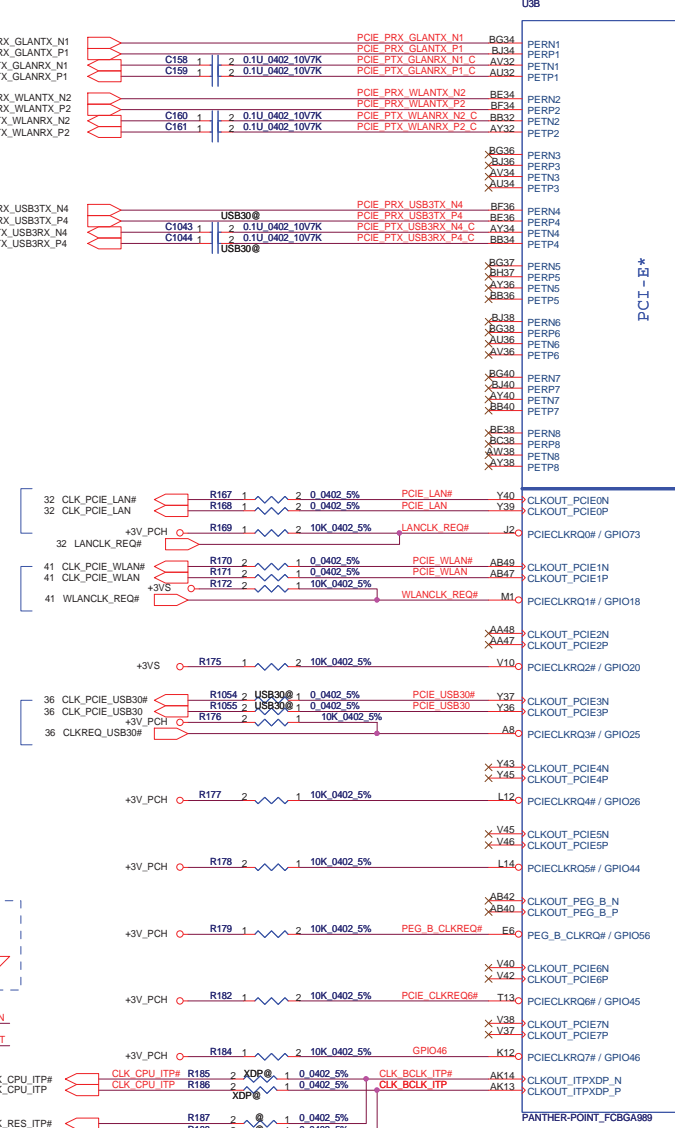
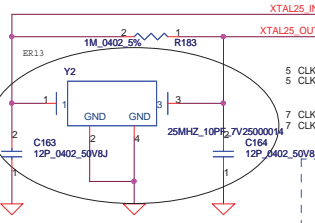
USB3.0 controller ---->

10/100/1G LAN ---->

MiniWLAN (Mini Card 1)---->

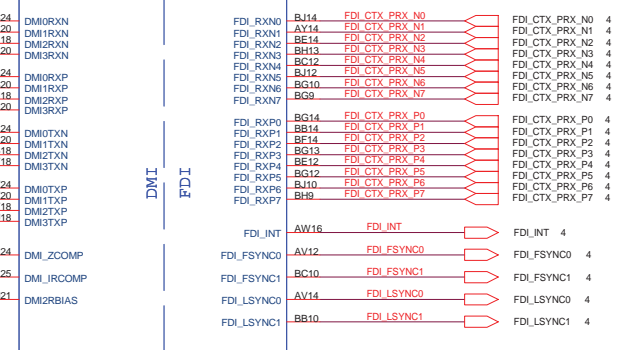
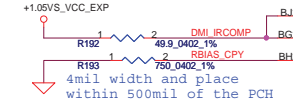
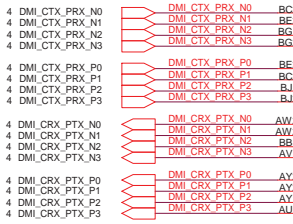
USB3.0 controller ---->

CLK_PCI_LPBACK
Reserve for EMI please close to U3

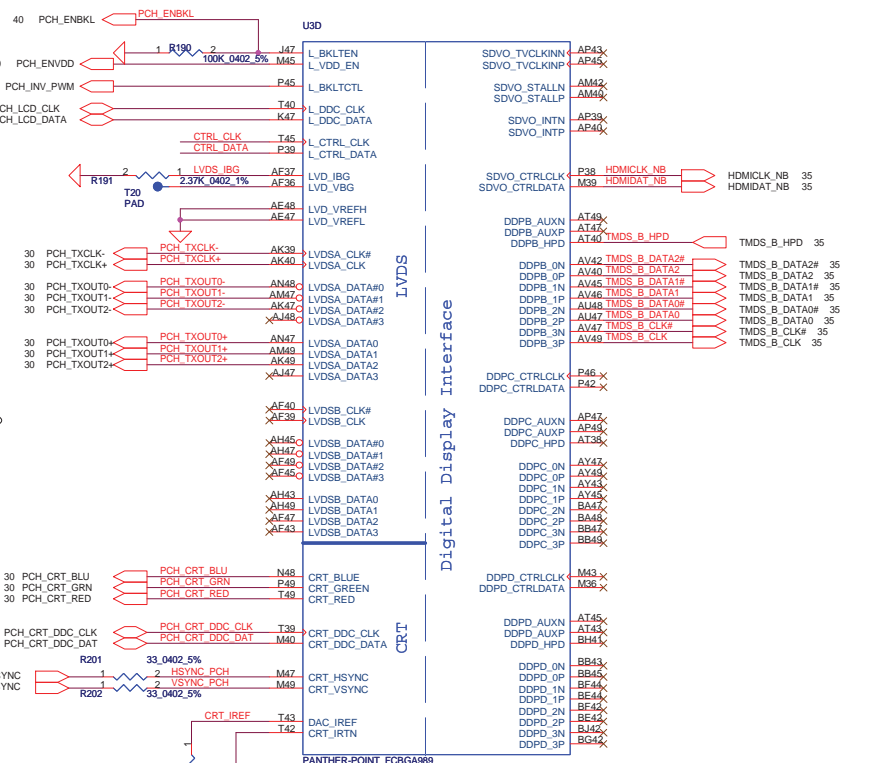
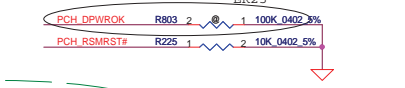
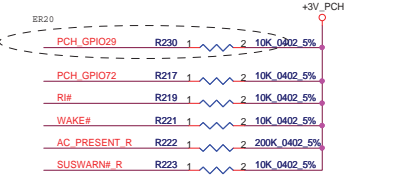
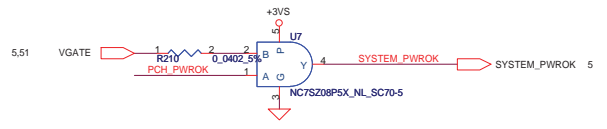
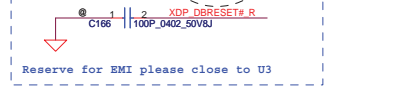
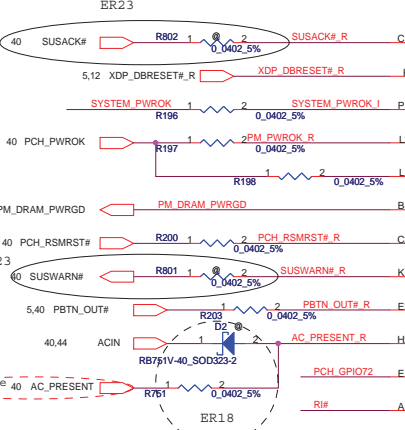


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Custom	LA-8221P	PCH (2/8) PCIE, SMBUS, CLK	
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USC

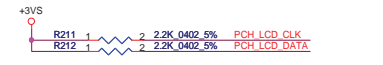
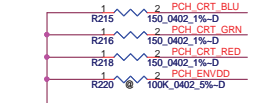
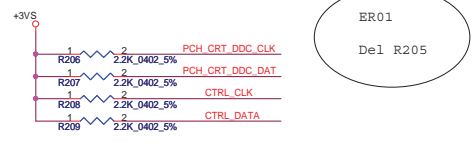


System Power Management

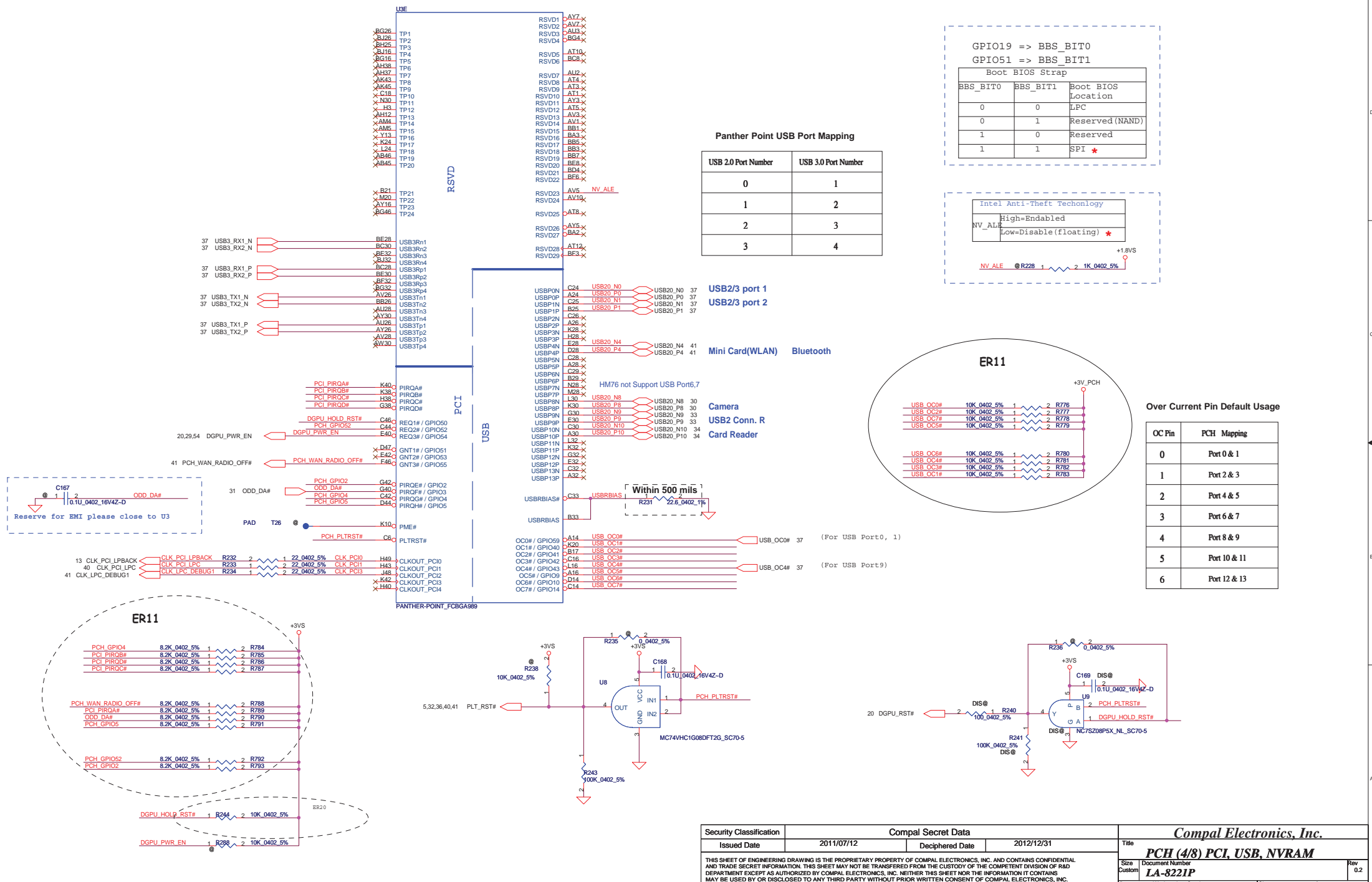


Digital Display Interface

CRT



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Panther Point USB Port Mapping

USB 2.0 Port Number	USB 3.0 Port Number
0	1
1	2
2	3
3	4

GPIO19 => BBS_BIT0
GPIO51 => BBS_BIT1

Boot BIOS Strap		
BBS_BIT0	BBS_BIT1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	Reserved
1	1	SPT *

Intel Anti-Theft Technology

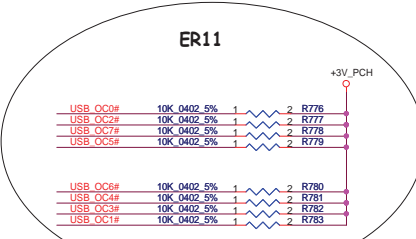
NV_ALE	High-Enabled
Low=Disable(floating) *	

NV_ALE @ R228 1 1K 0402 5% +1.8VS

**USB/3 port 1
USB/3 port 2**

Mini Card(WLAN) Bluetooth

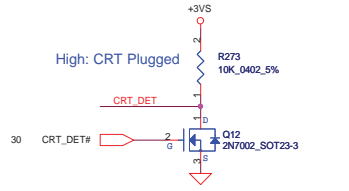
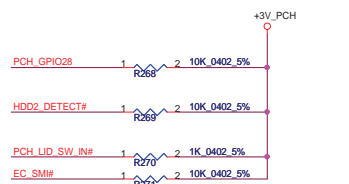
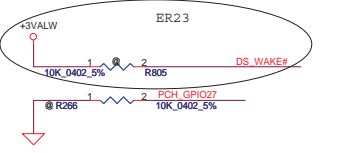
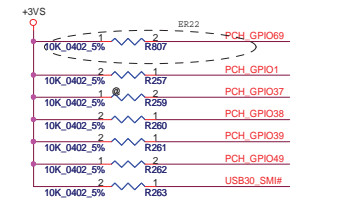
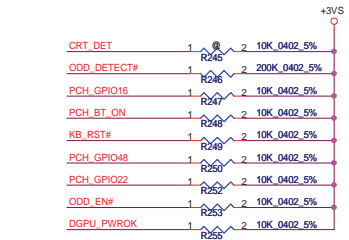
**Camera
USB2 Conn. R
Card Reader**



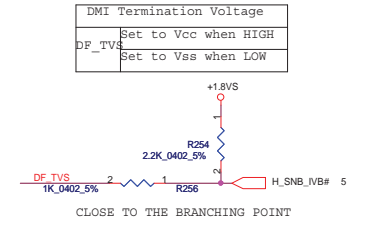
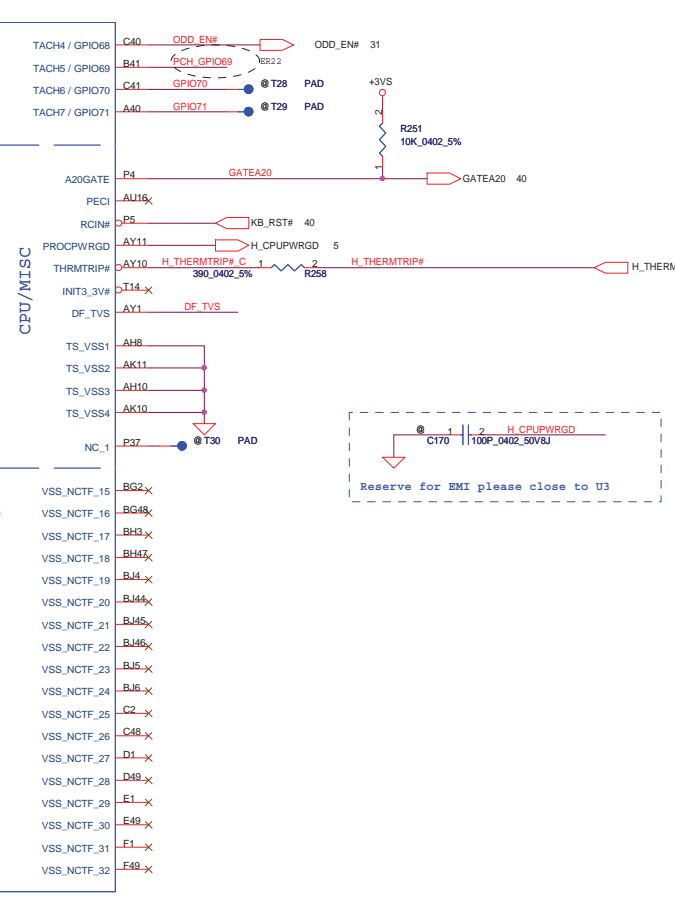
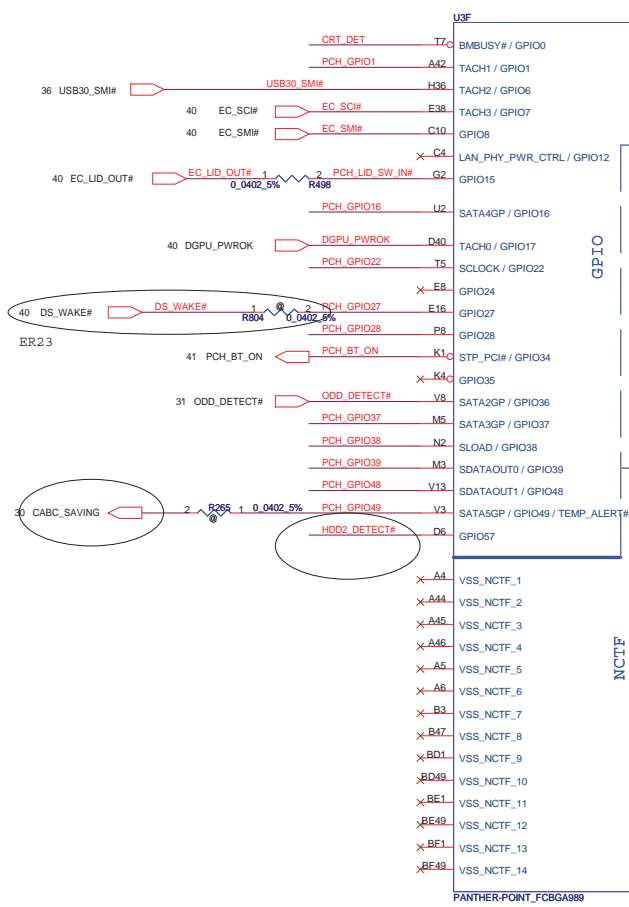
Over Current Pin Default Usage

OC Pin	PCH Mapping
0	Port 0 & 1
1	Port 2 & 3
2	Port 4 & 5
3	Port 6 & 7
4	Port 8 & 9
5	Port 10 & 11
6	Port 12 & 13

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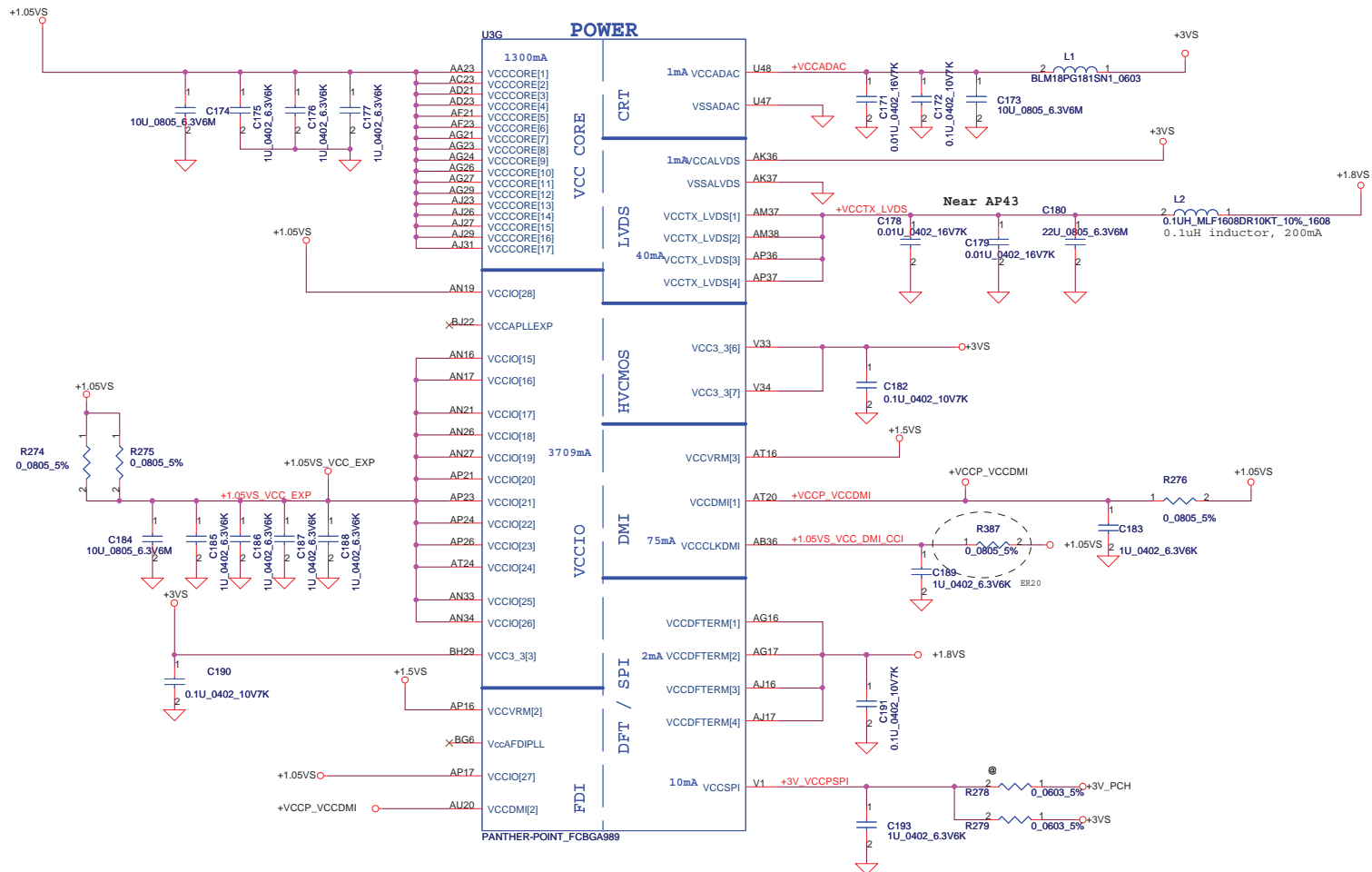


GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
* L : On-Die PLL Voltage Regulator disable

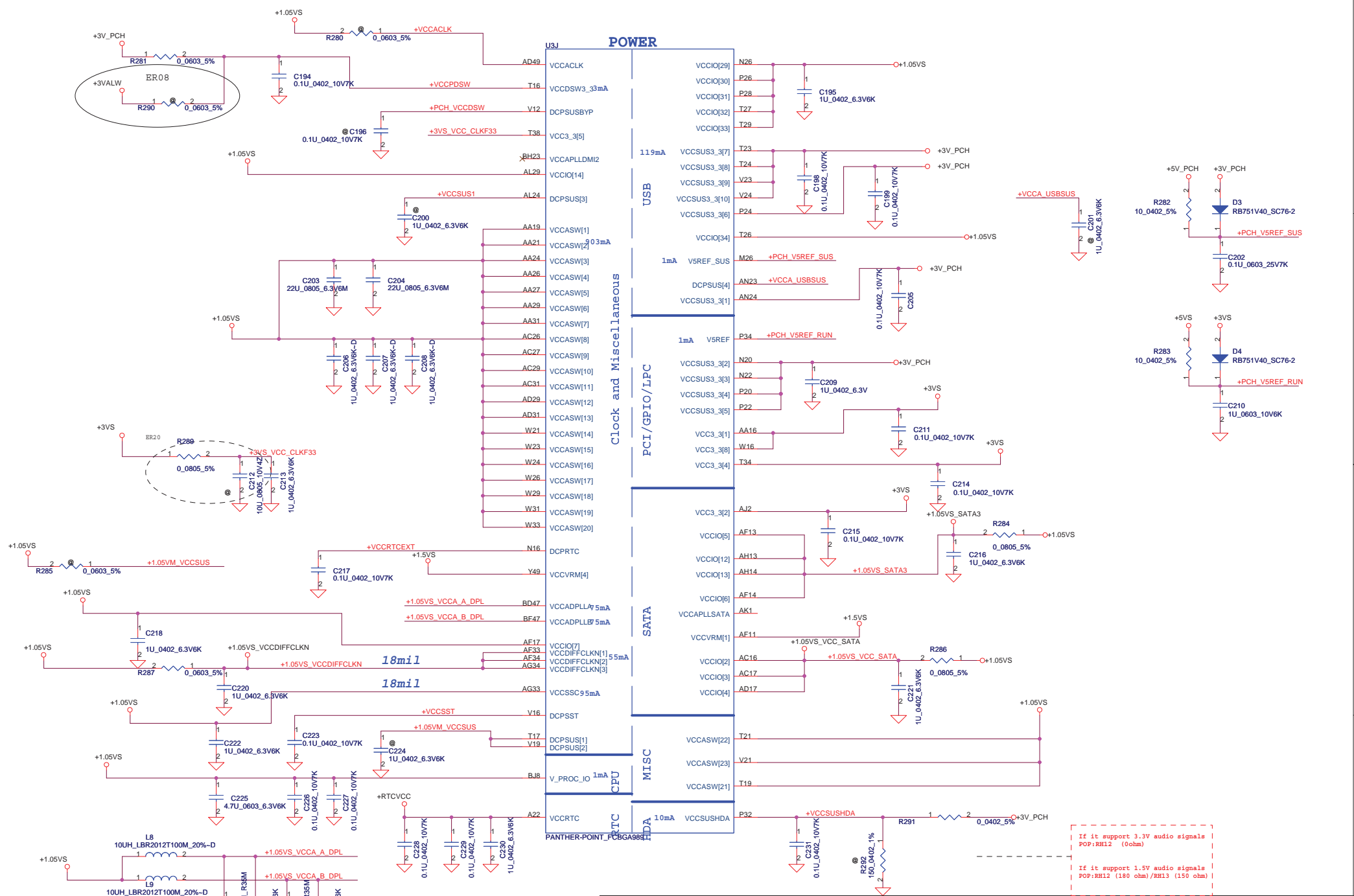


Reserve for EMI please close to U3

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PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	80 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04



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If it support 3.3V audio signals
POP:RH12 (0ohm)

If it support 1.5V audio signals
POP:RH12 (180 ohm)/RH13 (150 ohm)

Compal Electronics, Inc.		
PCH (7/8) PWR		
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Custom	LA-8221P	0.2
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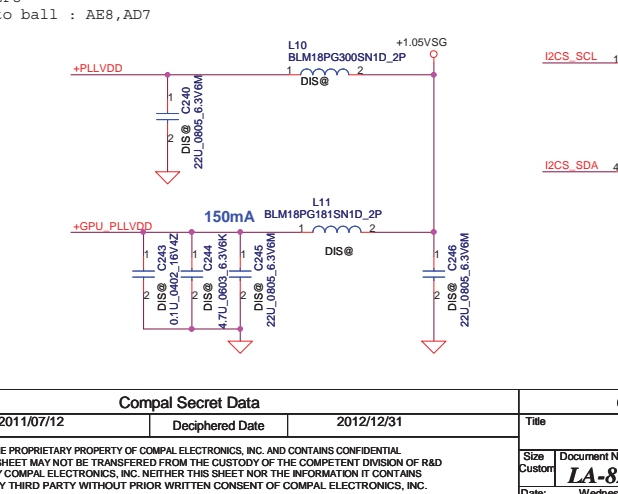
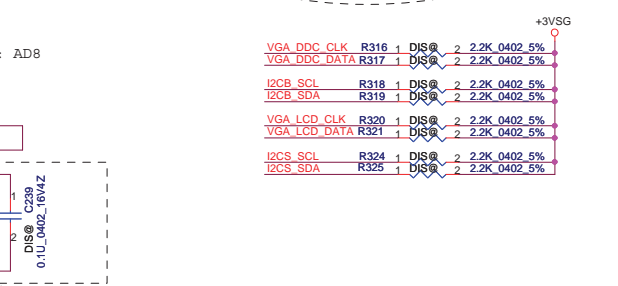
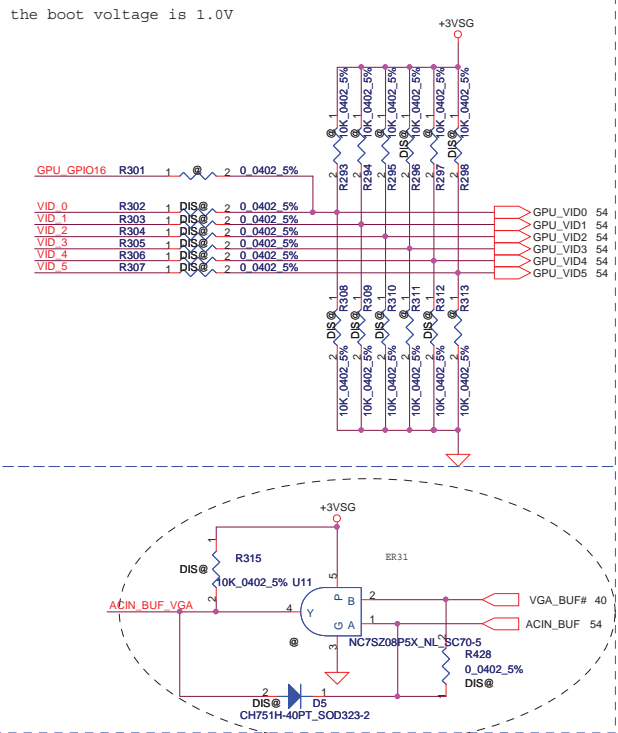
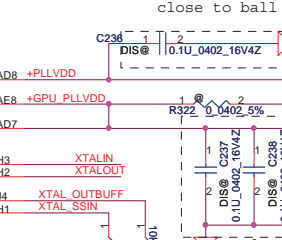
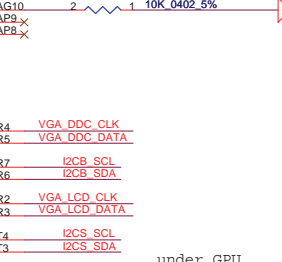
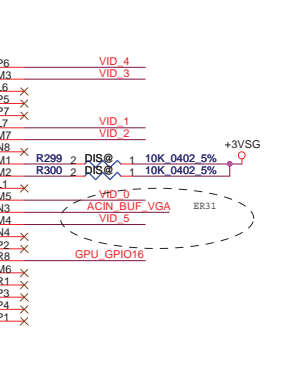
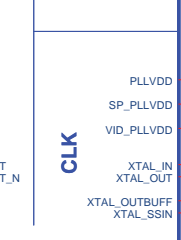
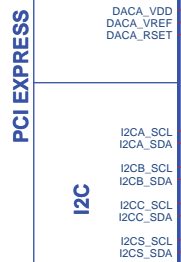
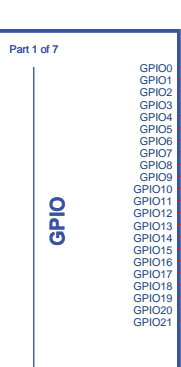
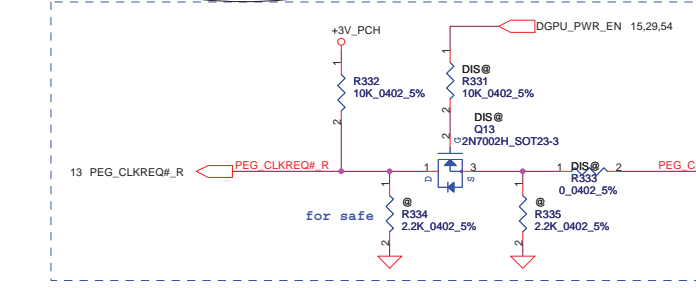
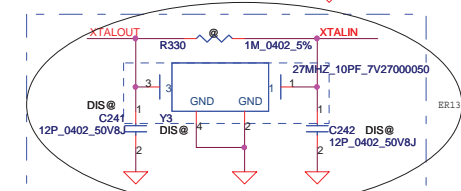
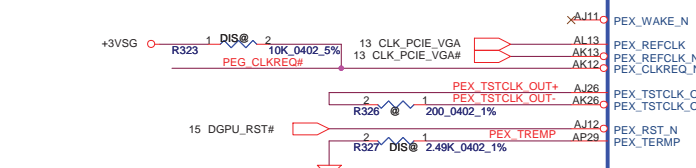
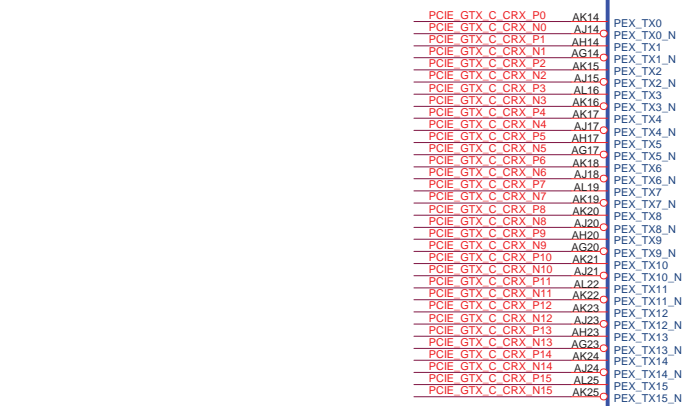
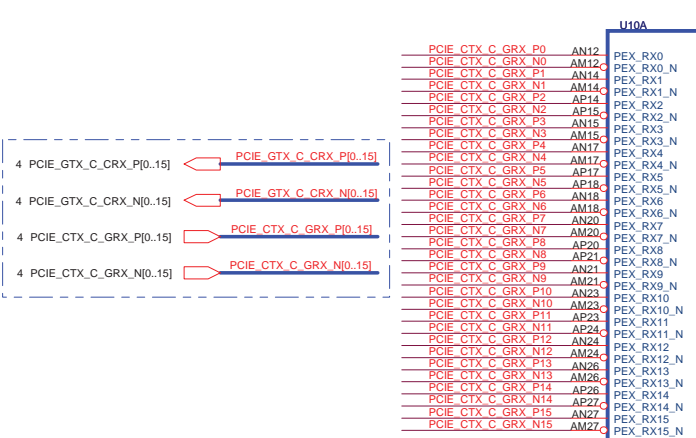
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AA2	VSS[2]	VSS[81] AK4
AA3	VSS[3]	VSS[82] AK42
AA33	VSS[4]	VSS[83] AK46
AA34	VSS[5]	VSS[84] AK6
AB11	VSS[6]	VSS[85] AL16
AB14	VSS[7]	VSS[86] AL17
AB39	VSS[8]	VSS[87] AL19
AB4	VSS[9]	VSS[88] AL2
AB43	VSS[10]	VSS[89] AL21
AB5	VSS[11]	VSS[90] AL23
AB7	VSS[12]	VSS[91] AL26
AC19	VSS[13]	VSS[92] AL27
AC2	VSS[14]	VSS[93] AL31
AC21	VSS[15]	VSS[94] AL33
AC24	VSS[16]	VSS[95] AL34
AC33	VSS[17]	VSS[96] AL48
AC34	VSS[18]	VSS[97] AM11
AC48	VSS[19]	VSS[98] AM14
AD10	VSS[20]	VSS[99] AM36
AD11	VSS[21]	VSS[100] AM39
AD12	VSS[22]	VSS[101] AM43
AD13	VSS[23]	VSS[102] AM45
AD19	VSS[24]	VSS[103] AM46
AD24	VSS[25]	VSS[104] AM7
AD26	VSS[26]	VSS[105] AN2
AD27	VSS[27]	VSS[106] AN29
AD33	VSS[28]	VSS[107] AN3
AD34	VSS[29]	VSS[108] AN31
AD36	VSS[30]	VSS[109] AP12
AD37	VSS[31]	VSS[110] AP19
AD38	VSS[32]	VSS[111] AP28
AD39	VSS[33]	VSS[112] AP30
AD4	VSS[34]	VSS[113] AP32
AD40	VSS[35]	VSS[114] AP38
AD42	VSS[36]	VSS[115] AP4
AD43	VSS[37]	VSS[116] AP42
AD45	VSS[38]	VSS[117] AP46
AD46	VSS[39]	VSS[118] AP8
AD8	VSS[40]	VSS[119] AR2
AE2	VSS[41]	VSS[120] AR48
AE3	VSS[42]	VSS[121] AT11
AE10	VSS[43]	VSS[122] AT13
AE12	VSS[44]	VSS[123] AT18
AD14	VSS[45]	VSS[124] AT22
AD16	VSS[46]	VSS[125] AT26
AE18	VSS[47]	VSS[126] AT28
AE19	VSS[48]	VSS[127] AT30
AF24	VSS[49]	VSS[128] AT32
AF26	VSS[50]	VSS[129] AT34
AF27	VSS[51]	VSS[130] AT39
AF29	VSS[52]	VSS[131] AT42
AF31	VSS[53]	VSS[132] AT46
AF38	VSS[54]	VSS[133] AT7
AF4	VSS[55]	VSS[134] AU24
AF42	VSS[56]	VSS[135] AU00
AF46	VSS[57]	VSS[136] AV16
AF5	VSS[58]	VSS[137] AV20
AF7	VSS[59]	VSS[138] AV24
AF8	VSS[60]	VSS[139] AV30
AG19	VSS[61]	VSS[140] AV38
AG2	VSS[62]	VSS[141] AV4
AG31	VSS[63]	VSS[142] AV43
AG48	VSS[64]	VSS[143] AV8
AH11	VSS[65]	VSS[144] AW14
AH3	VSS[66]	VSS[145] AW18
AH36	VSS[67]	VSS[146] AW2
AH39	VSS[68]	VSS[147] AW22
AH40	VSS[69]	VSS[148] AW26
AH42	VSS[70]	VSS[149] AW28
AH46	VSS[71]	VSS[150] AW32
AH7	VSS[72]	VSS[151] AW34
A19	VSS[73]	VSS[152] AW38
A121	VSS[74]	VSS[153] AW40
A124	VSS[75]	VSS[154] AW48
A133	VSS[76]	VSS[155] AV11
A134	VSS[77]	VSS[156] AY12
AK12	VSS[78]	VSS[157] AY22
AK3	VSS[79]	VSS[158] AY28

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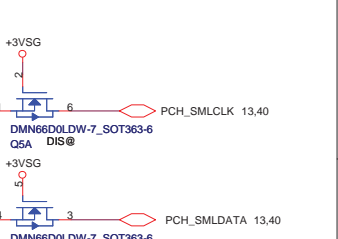
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AY4	VSS[159]	VSS[259] H46
AY42	VSS[160]	VSS[260] K18
AY46	VSS[161]	VSS[261] K26
AY8	VSS[162]	VSS[262] K39
B11	VSS[163]	VSS[263] K46
B15	VSS[164]	VSS[264] K7
B19	VSS[165]	VSS[265] L18
B23	VSS[166]	VSS[266] L2
B27	VSS[167]	VSS[267] L20
B31	VSS[168]	VSS[268] L26
B35	VSS[169]	VSS[269] L28
B39	VSS[170]	VSS[270] L36
B7	VSS[171]	VSS[271] L48
F45	VSS[172]	VSS[272] M12
BB12	VSS[173]	VSS[273] M16
BB16	VSS[174]	VSS[274] M22
BB20	VSS[175]	VSS[275] M24
BB22	VSS[176]	VSS[276] M30
BB24	VSS[177]	VSS[277] M32
BB28	VSS[178]	VSS[278] M34
BB30	VSS[179]	VSS[279] M38
BB38	VSS[180]	VSS[280] M4
BB4	VSS[181]	VSS[281] M42
BB46	VSS[182]	VSS[282] M46
BC14	VSS[183]	VSS[283] M8
BC18	VSS[184]	VSS[284] M18
BC2	VSS[185]	VSS[285] M30
BC22	VSS[186]	VSS[286] M47
BC26	VSS[187]	VSS[287] P11
BC32	VSS[188]	VSS[288] P18
BC34	VSS[189]	VSS[289] P30
BC36	VSS[190]	VSS[290] P43
BC40	VSS[191]	VSS[291] P47
BC42	VSS[192]	VSS[292] P7
BC48	VSS[193]	VSS[293] R2
BD46	VSS[194]	VSS[294] R48
BD5	VSS[195]	VSS[295] T12
BE22	VSS[196]	VSS[296] T12
BE26	VSS[197]	VSS[297] T31
BE40	VSS[198]	VSS[298] T4
BE10	VSS[199]	VSS[299] T47
BF12	VSS[200]	VSS[300] W34
BF16	VSS[201]	VSS[301] T46
BF20	VSS[202]	VSS[302] T8
BF22	VSS[203]	VSS[303] V11
BF24	VSS[204]	VSS[304] V17
BF26	VSS[205]	VSS[305] V26
BF28	VSS[206]	VSS[306] V27
BF3	VSS[207]	VSS[307] V29
BF30	VSS[208]	VSS[308] V36
BF38	VSS[209]	VSS[309] V39
BF40	VSS[210]	VSS[310] V43
BF4	VSS[211]	VSS[311] W17
BG17	VSS[212]	VSS[312] W19
BG21	VSS[213]	VSS[313] W2
BG33	VSS[214]	VSS[314] W27
BG44	VSS[215]	VSS[315] W48
BG8	VSS[216]	VSS[316] Y12
BH11	VSS[217]	VSS[317] Y4
BH15	VSS[218]	VSS[318] Y46
BH17	VSS[219]	VSS[319] Y8
BH19	VSS[220]	VSS[320] Y8
H10	VSS[221]	VSS[321] Y4
BH27	VSS[222]	VSS[322] Y46
BH31	VSS[223]	VSS[323] Y8
BH33	VSS[224]	VSS[324] BG29
BH35	VSS[225]	VSS[325] N24
BH39	VSS[226]	VSS[326] A13
BH43	VSS[227]	VSS[327] AD47
D3	VSS[228]	VSS[328] B43
D12	VSS[229]	VSS[329] BE10
D16	VSS[230]	VSS[330] BG41
D18	VSS[231]	VSS[331] G14
D22	VSS[232]	VSS[332] H16
D24	VSS[233]	VSS[333] T36
D26	VSS[234]	VSS[334] BG22
D30	VSS[235]	VSS[335] BG24
D32	VSS[236]	VSS[336] C22
D34	VSS[237]	VSS[337] AP13
D38	VSS[238]	VSS[338] M14
D38	VSS[239]	VSS[339] AP3
D42	VSS[240]	VSS[340] AP1
D8	VSS[241]	VSS[341] BE16
E18	VSS[242]	VSS[342] BC16
E26	VSS[243]	VSS[343] BG28
G18	VSS[244]	VSS[344] BJ28
G20	VSS[245]	VSS[345]
G26	VSS[246]	VSS[346]
G28	VSS[247]	VSS[347]
G36	VSS[248]	VSS[348]
G48	VSS[249]	VSS[349]
H12	VSS[250]	VSS[350]
H18	VSS[251]	VSS[351]
H22	VSS[252]	VSS[352]
H24	VSS[253]	
H26	VSS[254]	
H30	VSS[255]	
H32	VSS[256]	
H34	VSS[257]	
F3	VSS[258]	

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GPIO	I/O	USAGE
GPIO0	O	GPU_VID4
GPIO1	O	GPU_VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	GPU_VID1
GPIO6	O	GPU_VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	MEM_VDD_CTL(PES) GPU_VID0(Real N13P)
GPIO12	I	PWR_LEVEL
GPIO13	O	THERM_LOAD_STEP_DOWN
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	THERM_LOAD_STEP_UP
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved
GPIO22	I/O	SLI_RASTER_SYNC
GPIO23	O	SLI_SWAPRDY
GPIO24		

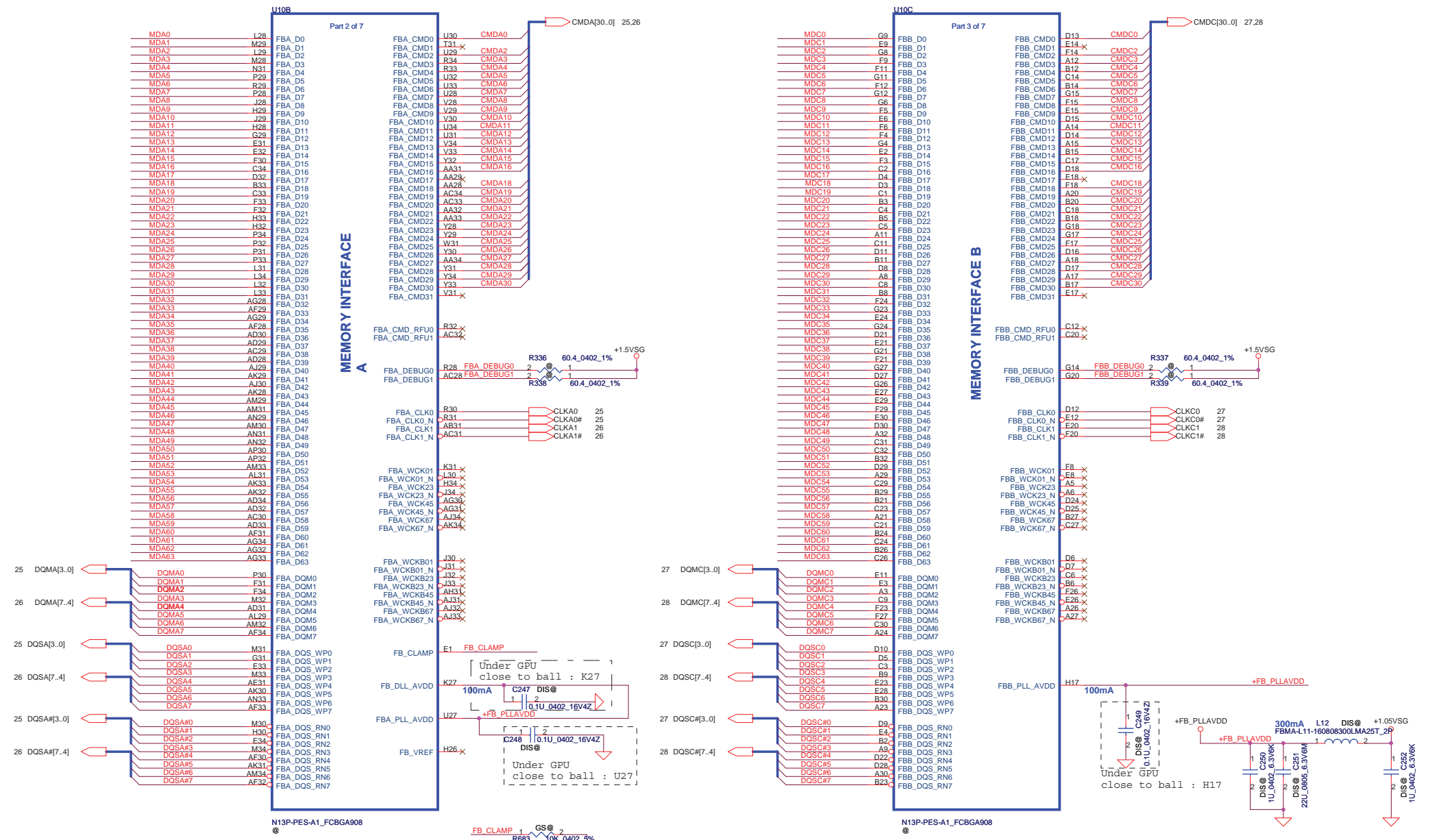
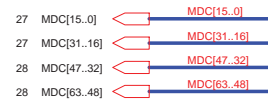
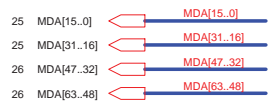


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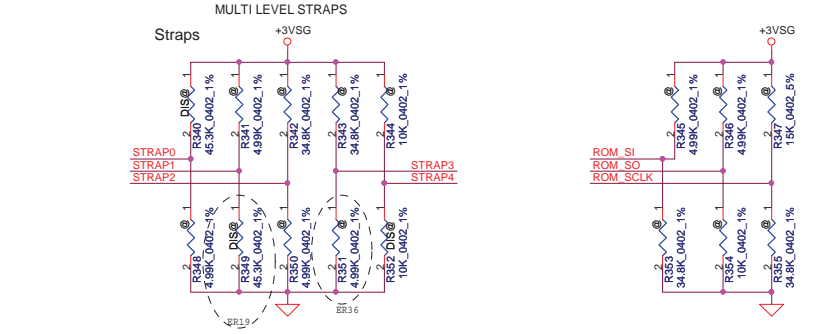
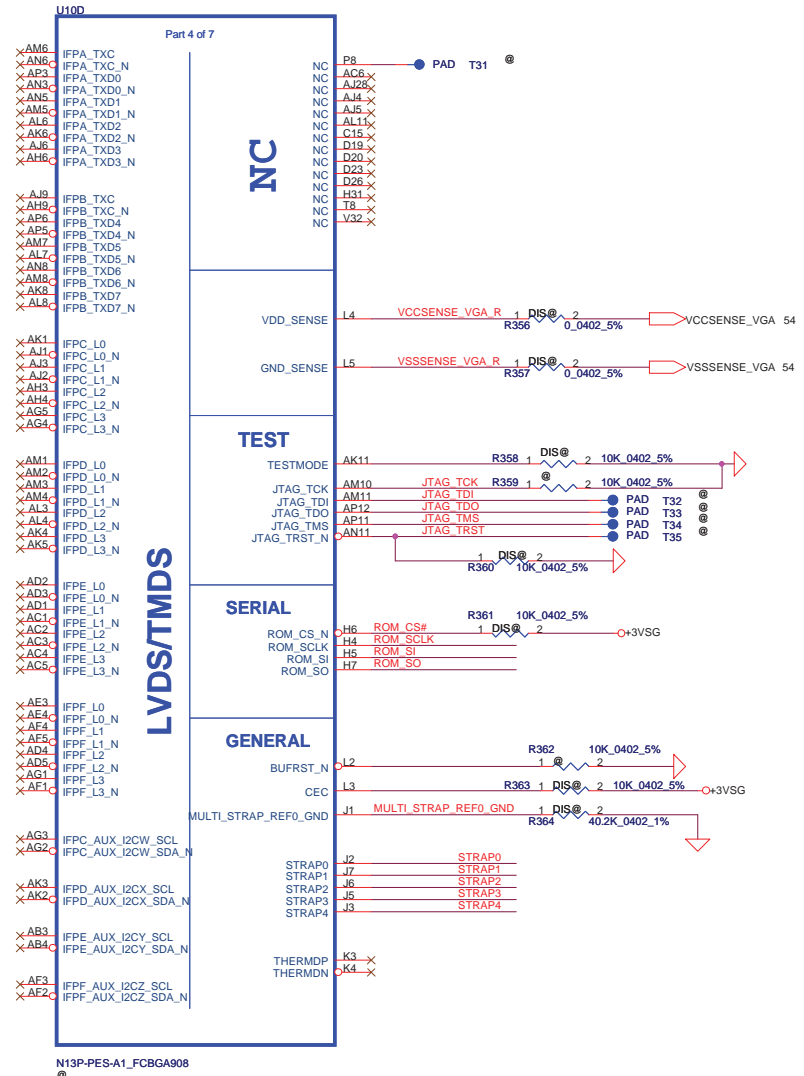
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VRAM Interface



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Need check with NVIDIA

For N13P-GS strap table

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	128M*16*8	Samsung SA000047QA0	R	R	PU 20K	PD 25K	PD 10K	R	R	R
N13P-GS	900 MHz	128M*16*8	Hynix SA00003YO30	R	R	PU 20K	PD 25K	PD 10K	R	R	R
N13P-GS	900 MHz	64M*16*8	Samsung SA00004GS30	R	R	PU 20K	PD 25K	PD 10K	R	R	R
N13P-GS	900 MHz	64M*16*8	Hynix SA000041S60	R	R	PU 20K	PD 25K	PD 10K	R	R	R

For N13P-GL strap table

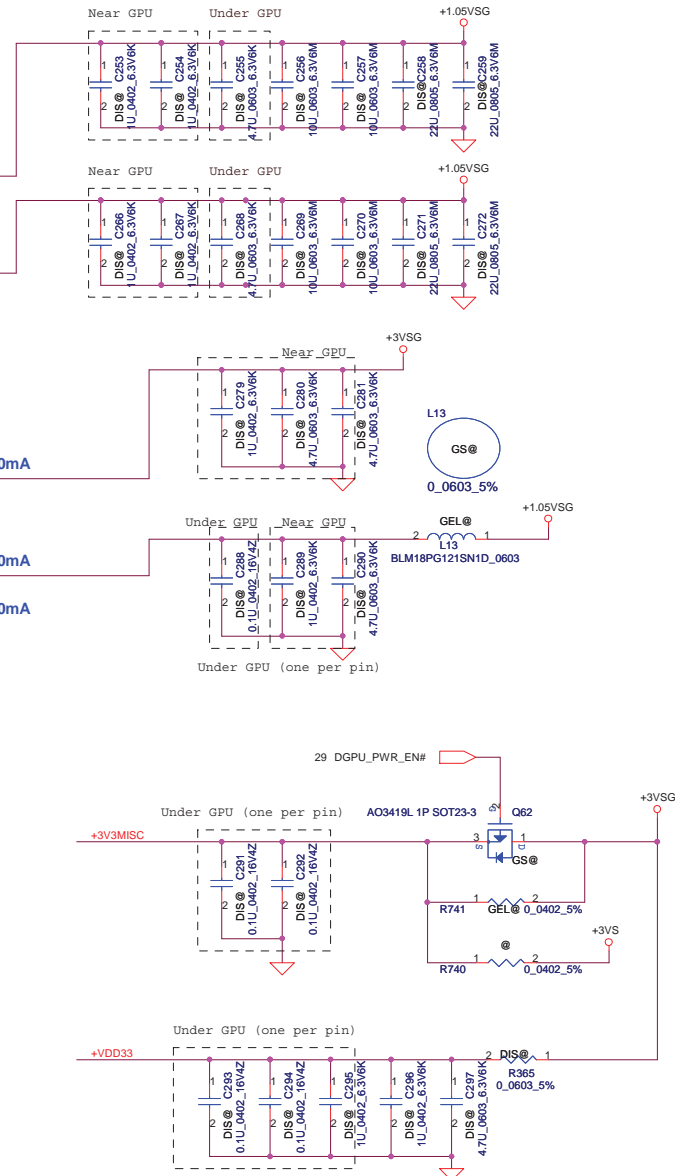
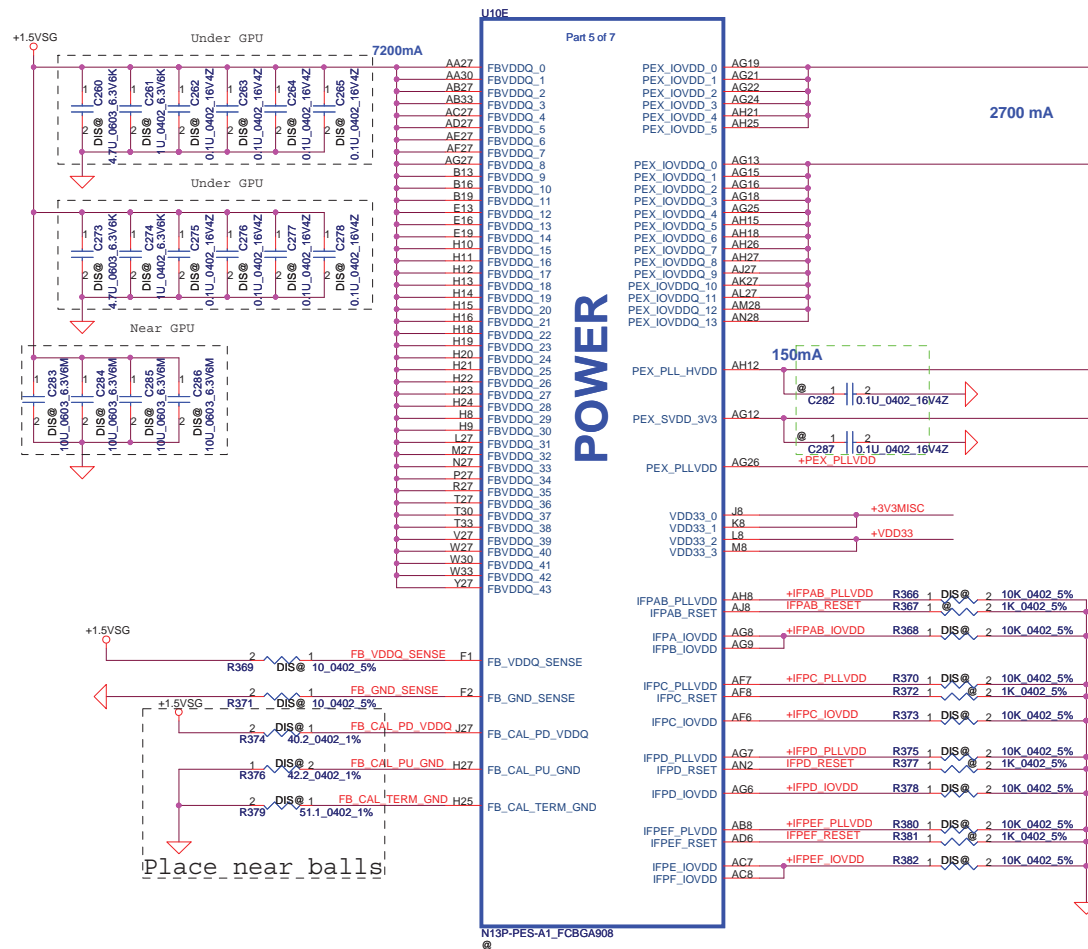
GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GL	900 MHz	128M*16*8	Samsung SA000047QA0	R	R	PU 10K	PD 5K	PD 10K	R	R	R
N13P-GL	900 MHz	128M*16*8	Hynix SA00003YO30	R	R	PU 10K	PD 5K	PD 10K	R	R	R
N13P-GL	900 MHz	64M*16*8	Samsung SA00004GS30	R	R	PU 10K	PD 5K	PD 10K	R	R	R
N13P-GL	900 MHz	64M*16*8	Hynix SA000041S60	R	R	PU 10K	PD 5K	PD 10K	R	R	R

For N13M-GE1 strap table

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GE1	900 MHz	128M*16*4	Samsung SA000047QA0	R	R	PU 5K	PD 5K	PD 10K	R	R	R
N13M-GE1	900 MHz	128M*16*4	Hynix SA00003YO30	R	R	PU 5K	PD 5K	PD 10K	R	R	R

For N13M-GE1 GB1b-64 strap table

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GE1	900 MHz	256M*8*8	ELPIDA SA000056P00	R	R	PU 5K	PD 5K	PD 10K	R	R	R
N13M-GE1	900 MHz	256M*8*8	Hynix SA000056C00	R	R	PU 5K	PD 5K	PD 10K	R	R	R
N13M-GE1	900 MHz	512M*8*8	HYNIX SA00005BL00	R	R	PU 5K	PD 5K	PD 10K	R	R	R
N13M-GE1	900 MHz	512M*8*8	ELPIDA SA00005AA00	R	R	PU 5K	PD 5K	PD 10K	R	R	R



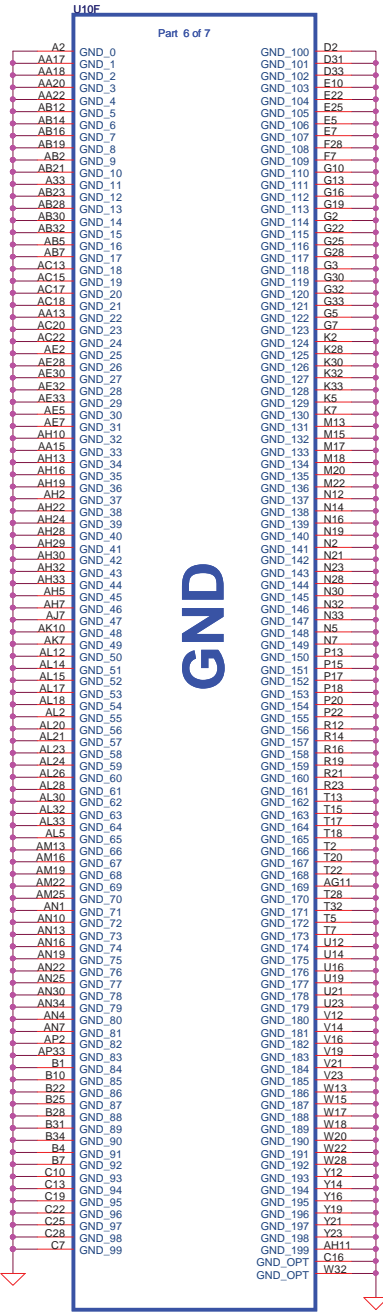
Place near balls

N13P-PES-A1_FCBGA908

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		2012/12/31

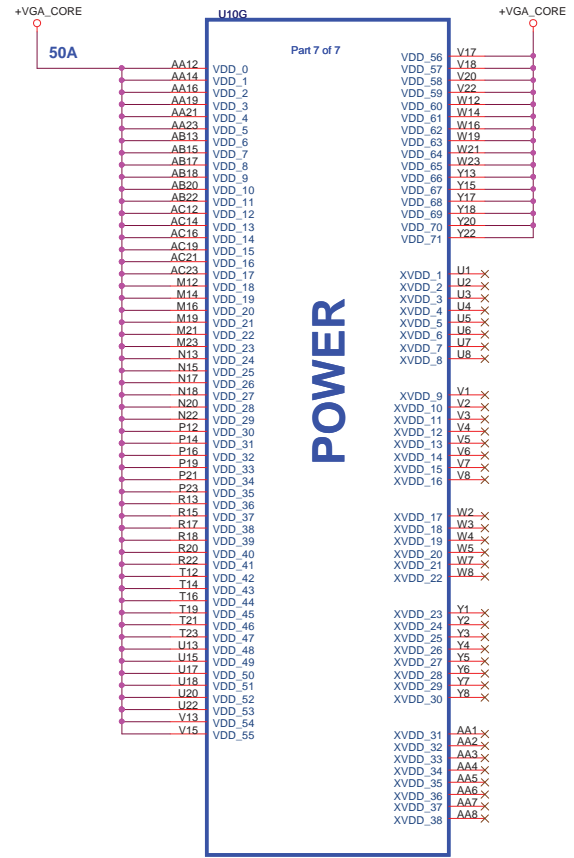
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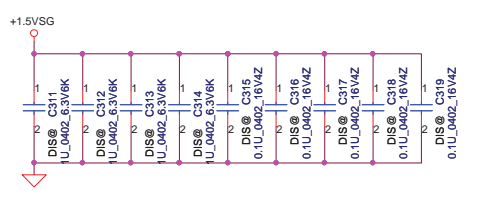
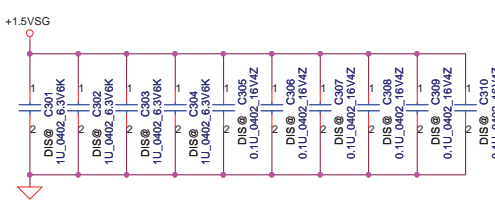
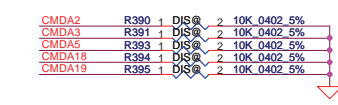
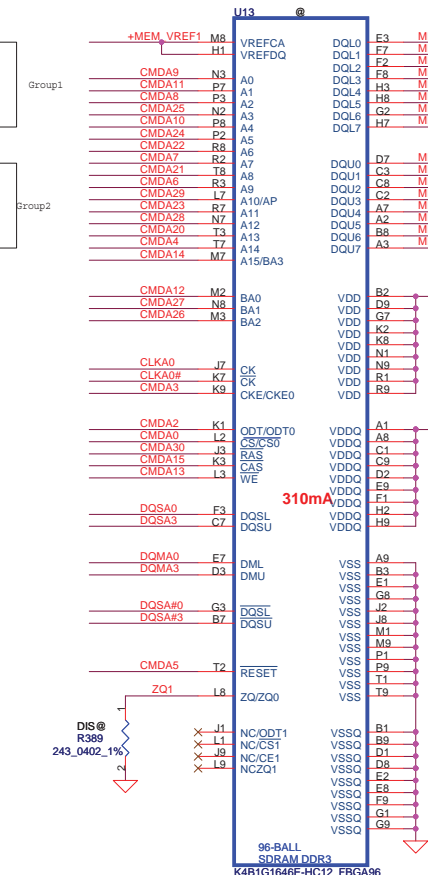
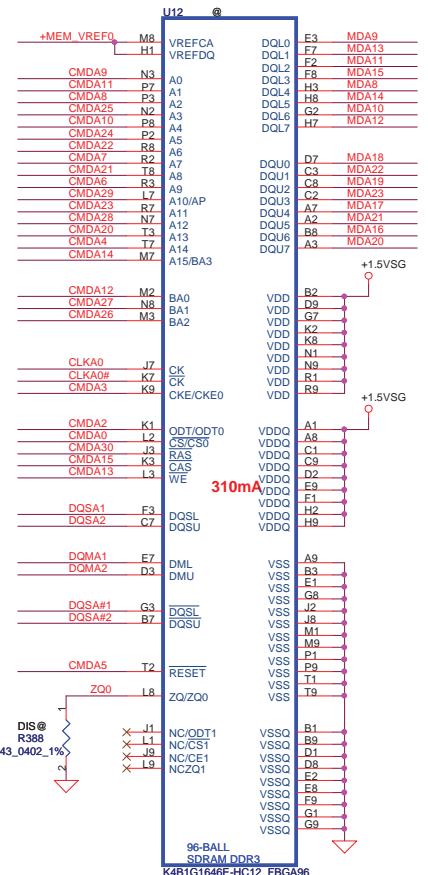
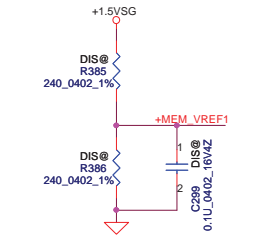
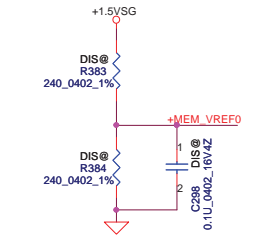
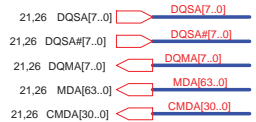


N13P-PES-A1_FCBGA908

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Date: Wednesday, October 26, 2011				Sheet	24 of 58

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available	LOW	HIGH

Command Bit	Default Pull-down
ODT#	10k
CKE	10k
RST	10k
CS*	No Termination

Samsung : SA000035700 (S IC D3 64Mx16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64Mx16 H5TQ1G63BFR-12C FBGA 1.5V)
AMD : SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFPGA 96P 1.5V)

Security Classification: **Compal Secret Data**

Issued Date	2011/07/12	Deciphered Date	2012/12/31
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Compal Electronics, Inc.

Title: **N13P DDR3 6/9**

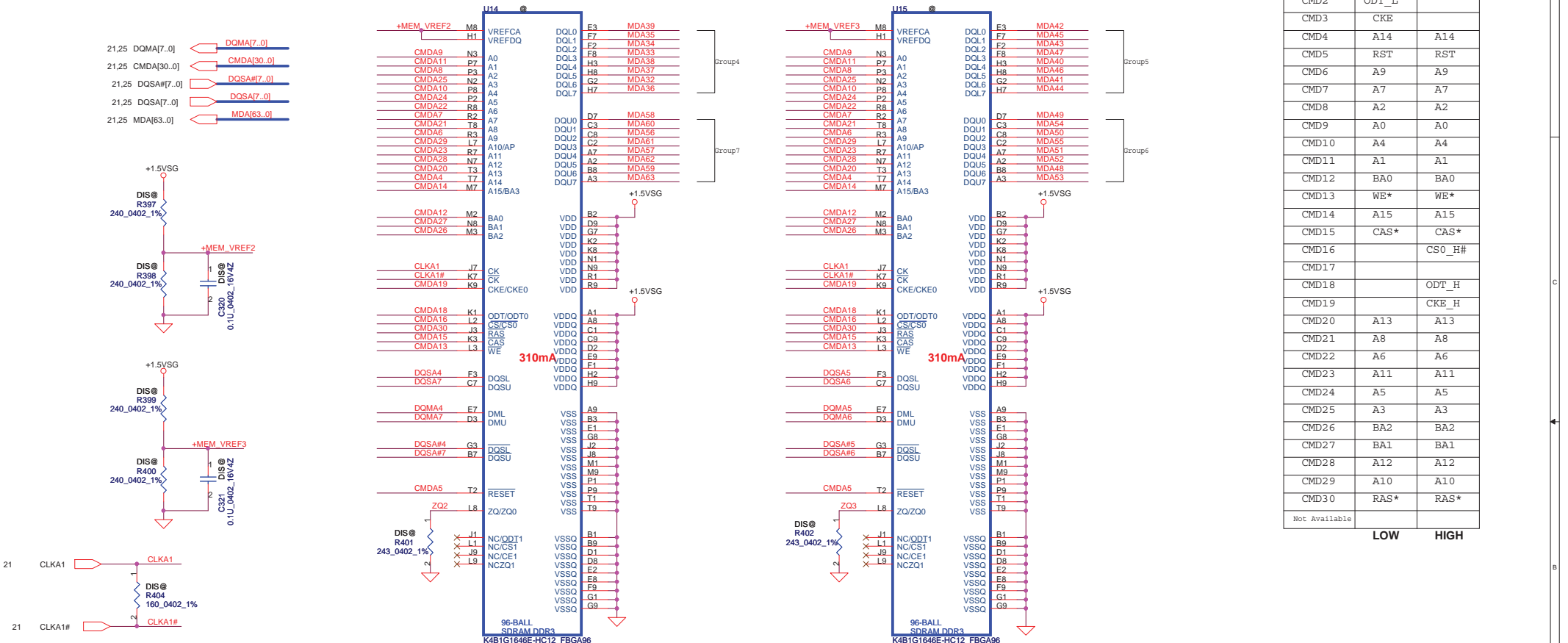
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Customer: **LA-8221P**

Date: Wednesday, October 26, 2011 | Sheet 25 of 58

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*

Not Available
LOW HIGH

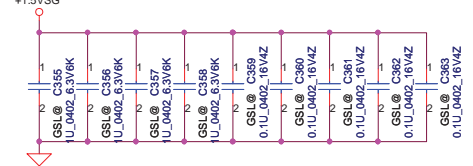
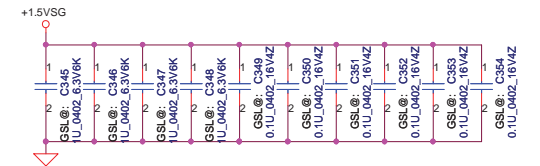
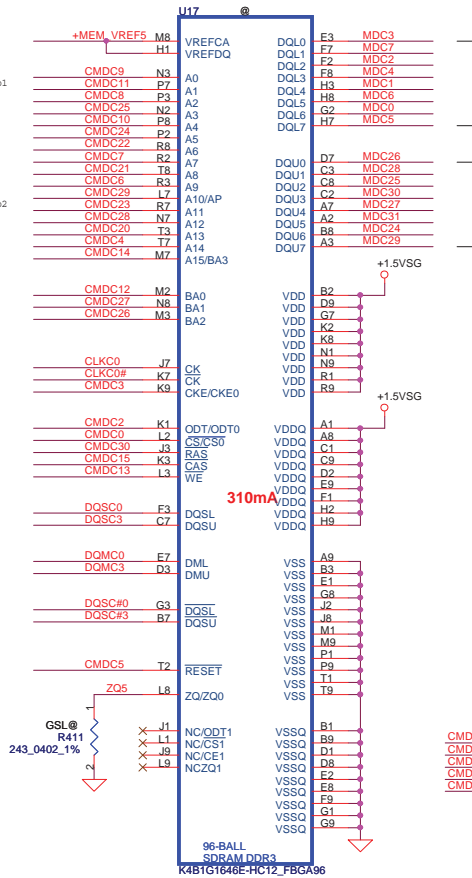
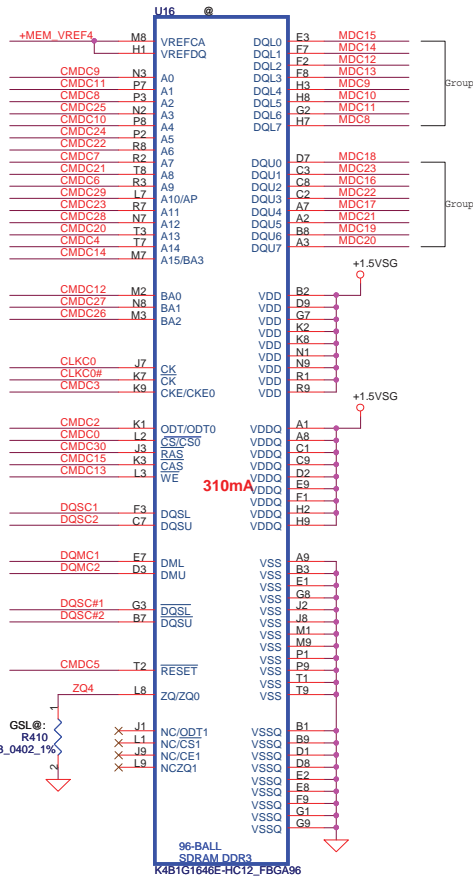
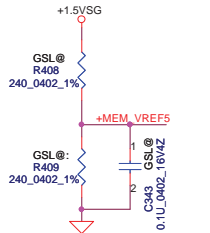
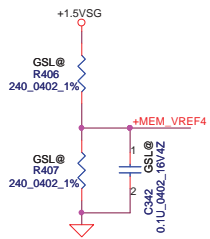
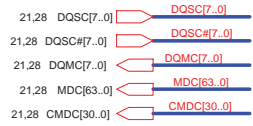
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Issued Date	2011/07/12	Deciphered Date	

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VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available	LOW	HIGH

Command Bit	Default Pull-down
ODTX	10k
CKEX	10k
RST	10k
CS*	No Termination

Security Classification	Compal Secret Data	
Issued Date	2011/07/12	Deciphered Date
		2012/12/31

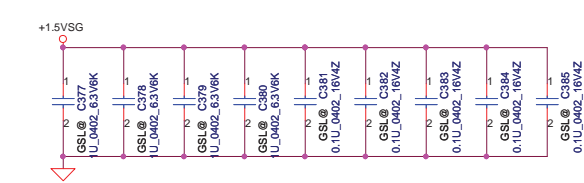
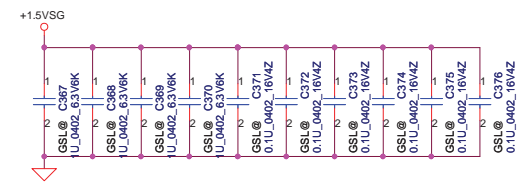
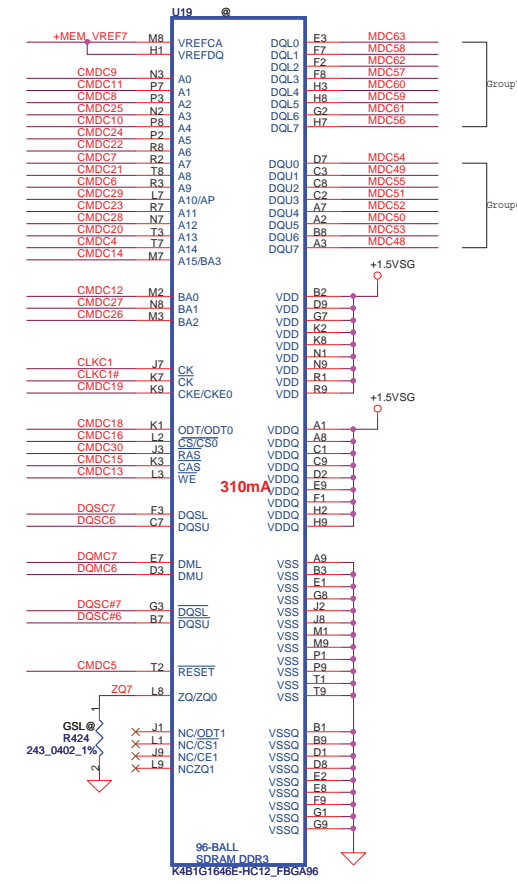
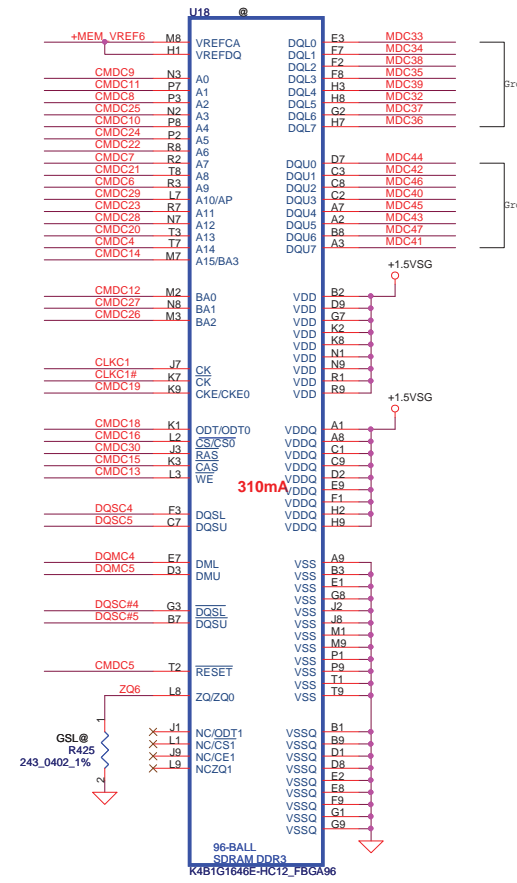
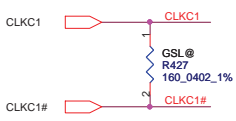
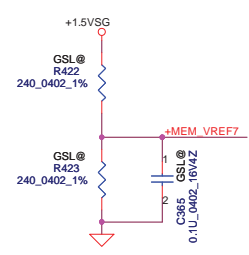
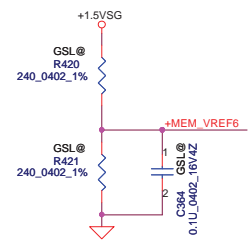
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Title	N13P DDR3 8/9	
Size	Document Number	Rev
Custom	LA-8221P	0.2
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VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

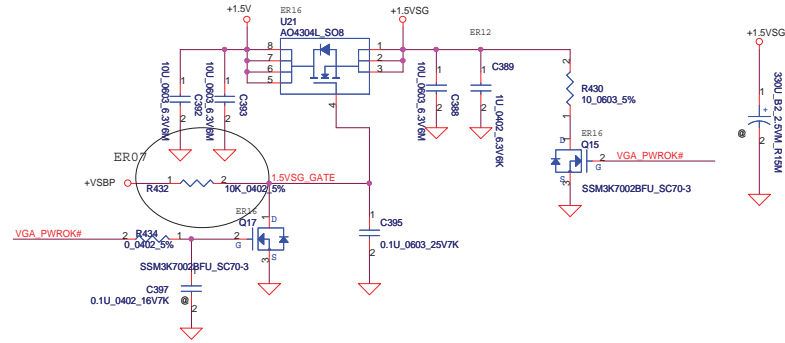
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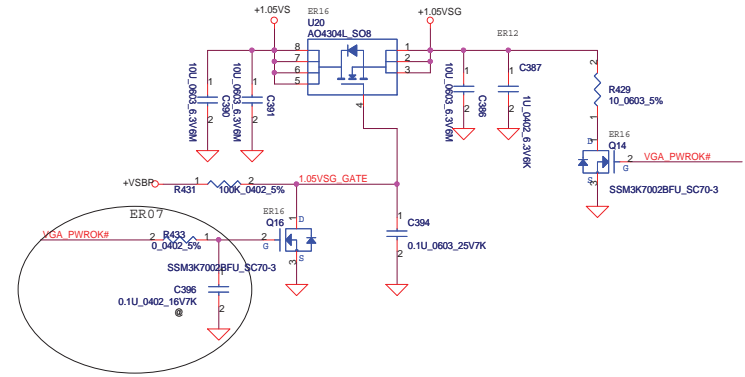
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CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

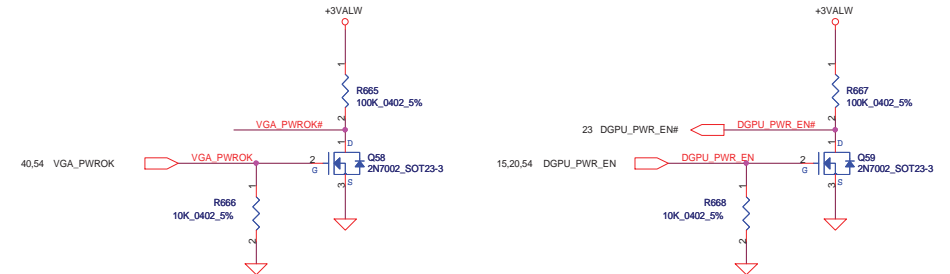
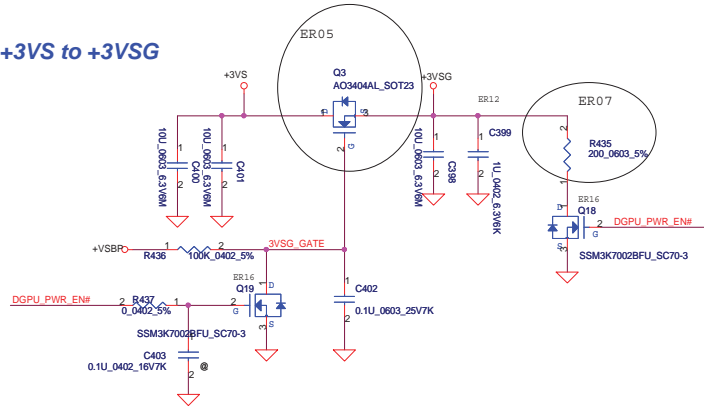
+1.5V to +1.5VSG



+VCCP to +1.05VSG

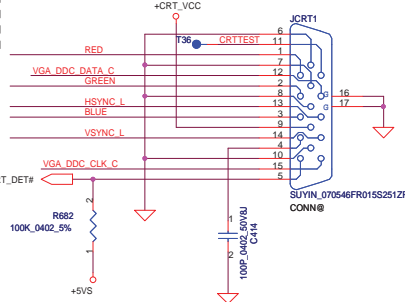
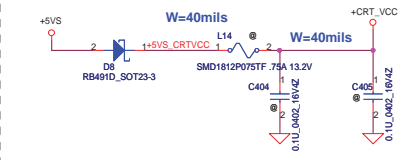
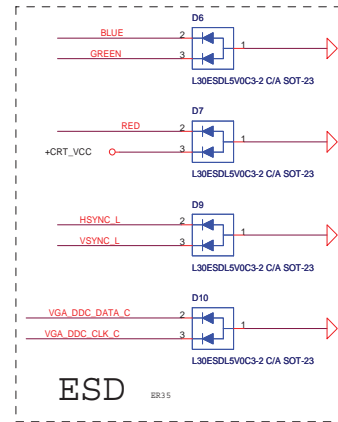
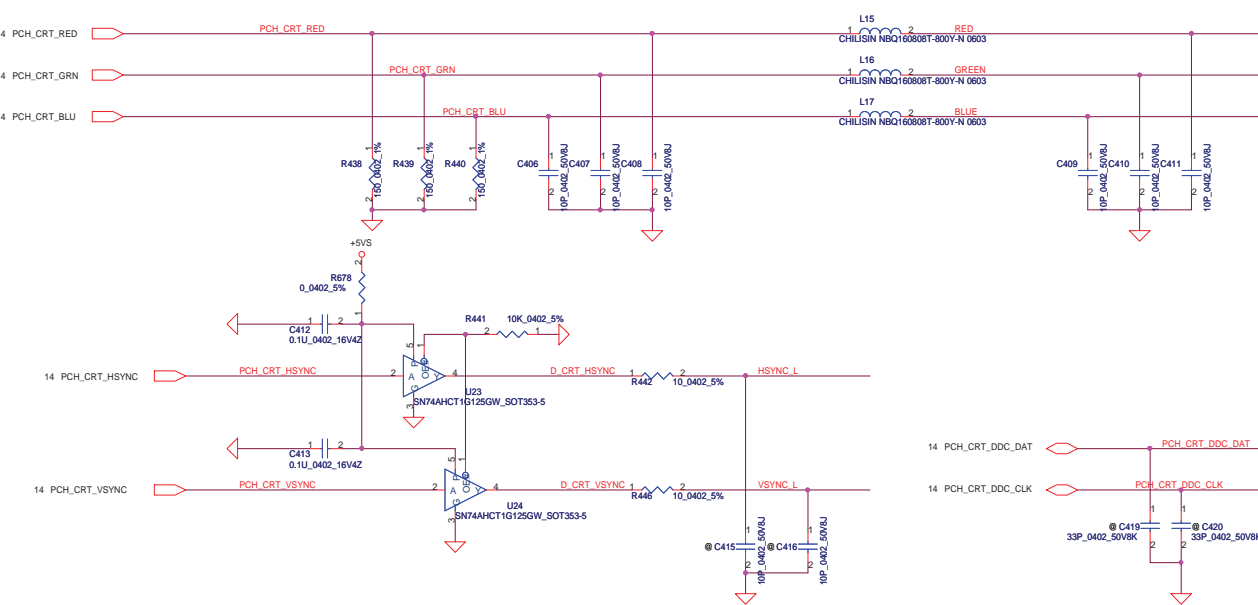


+3VS to +3VSG

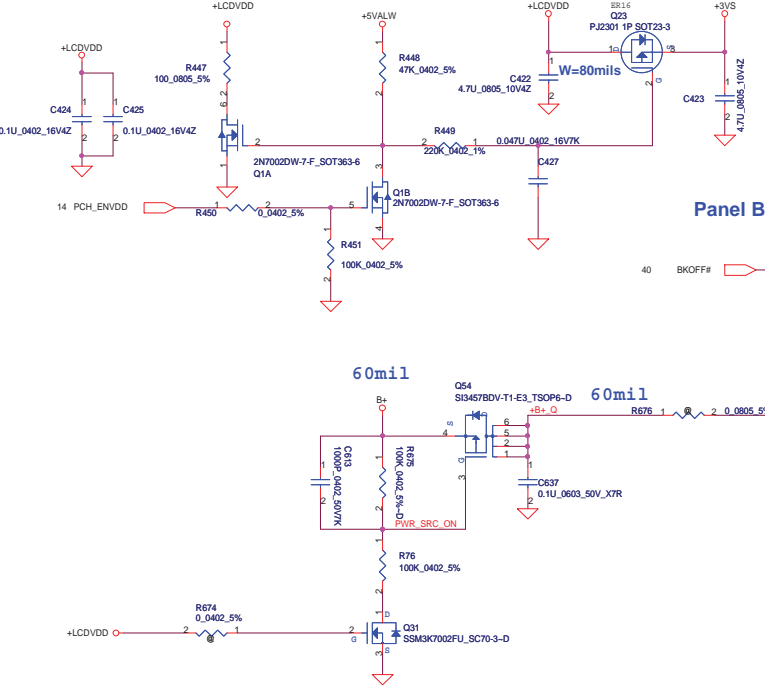


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Size	Document Number	Date		Rev
Custom	LA-8221P	Wednesday, October 26, 2011		02
		Sheet	29 of 58	

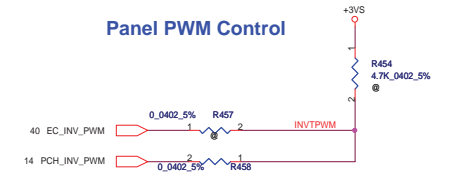
CRT



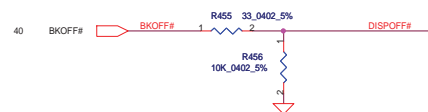
LCD POWER CIRCUIT



Panel PWM Control

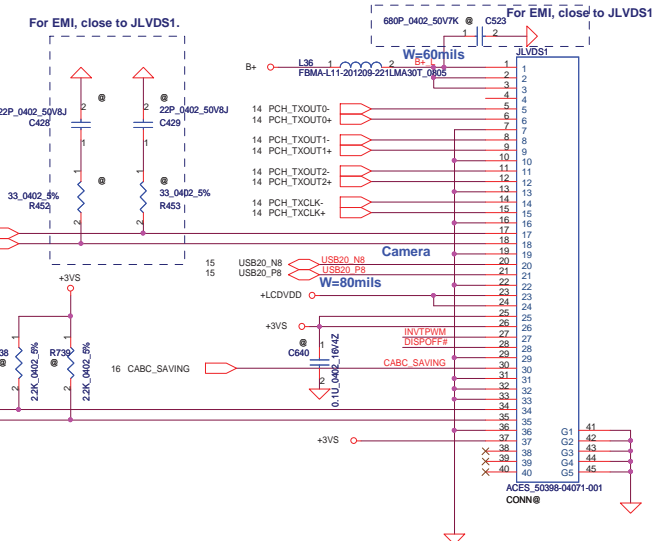
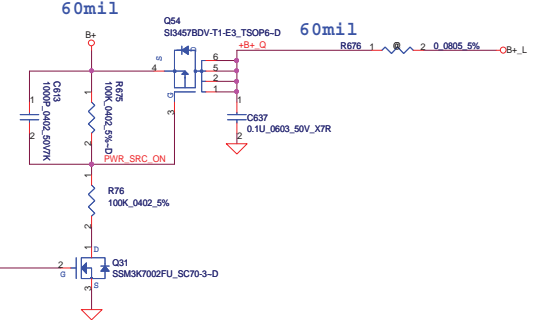


Panel Backlight Control



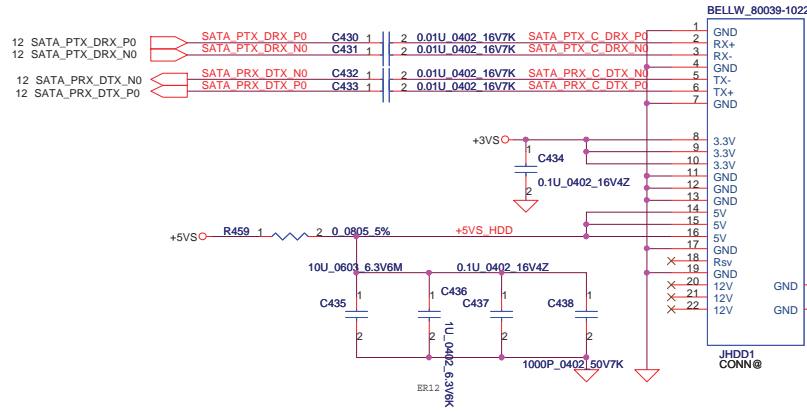
60mil

60mil

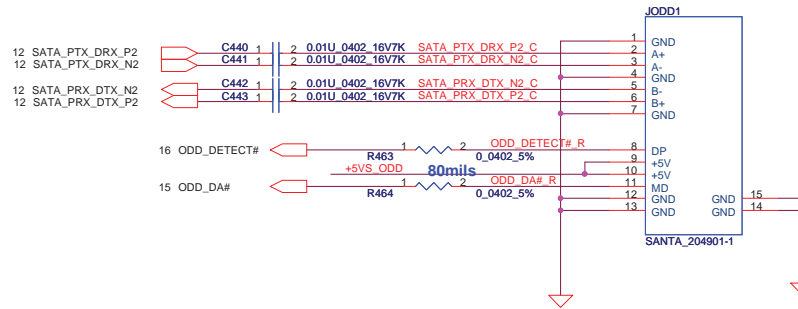


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Date:	Wednesday, October 26, 2011	Sheet	30 of 58	

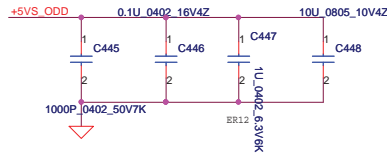
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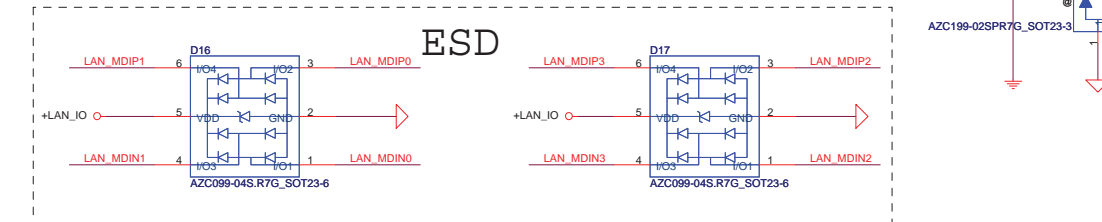
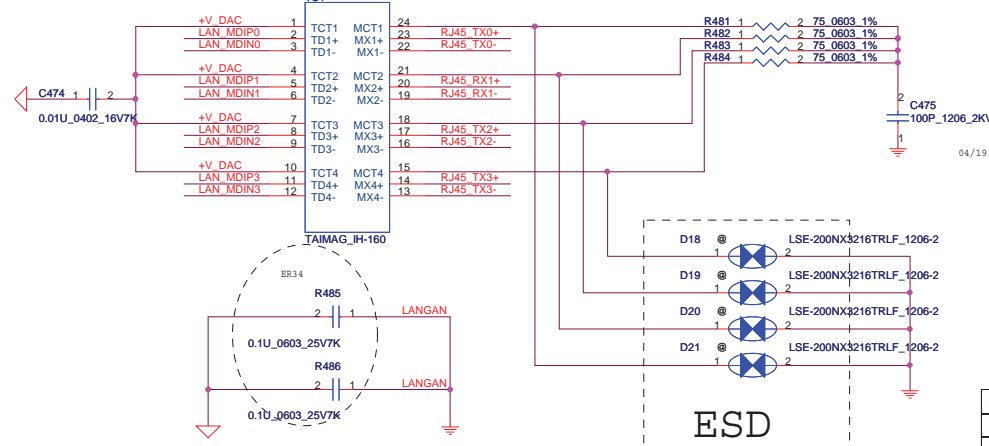
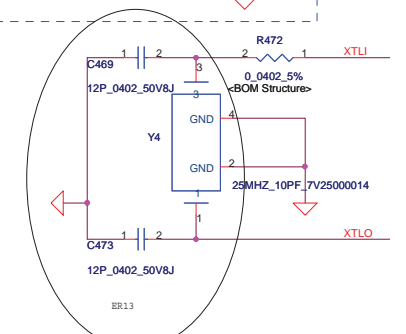
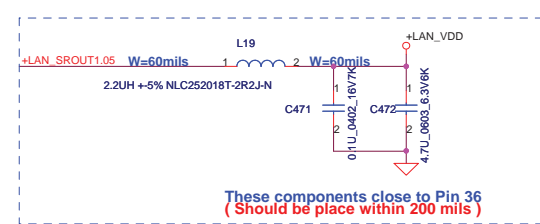
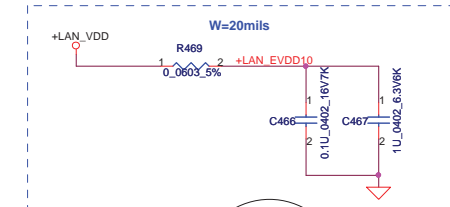
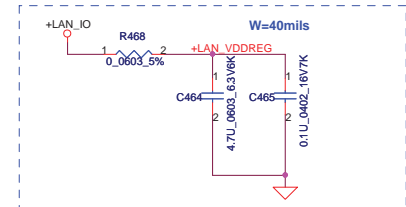
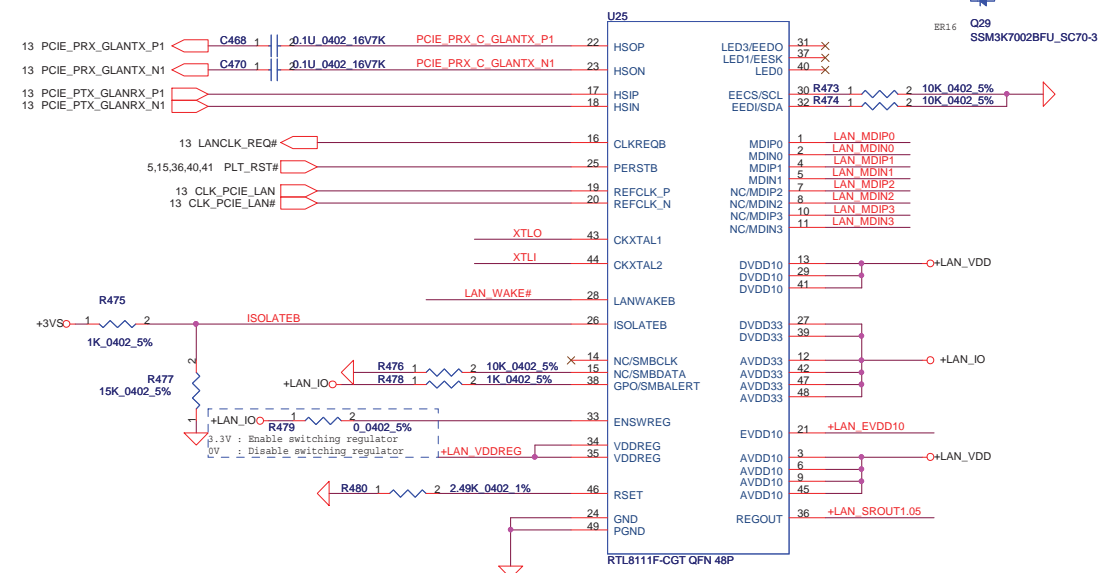
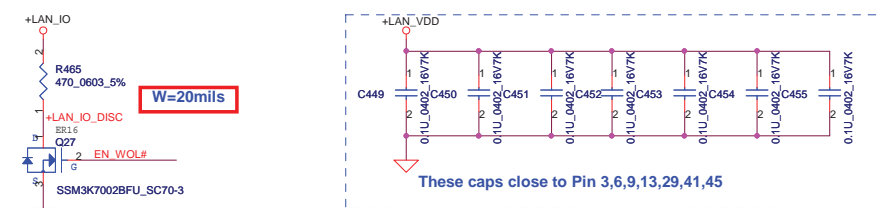
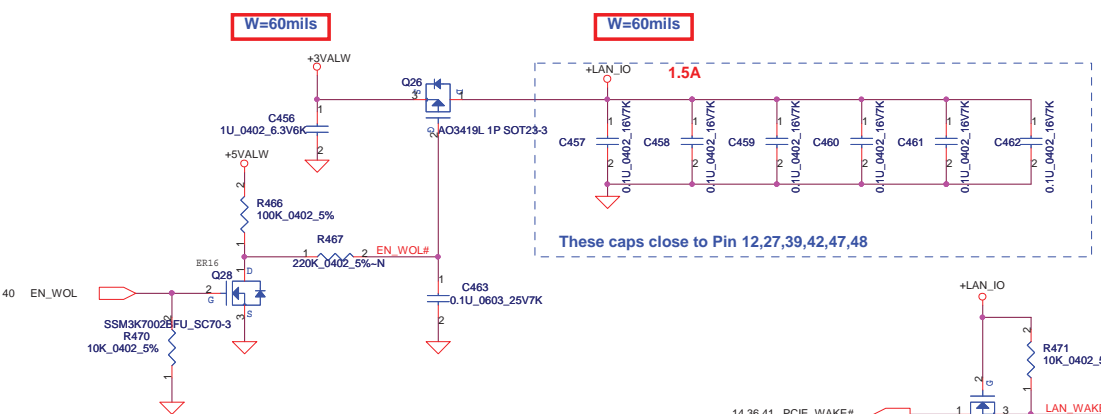
SATA ODD Conn.



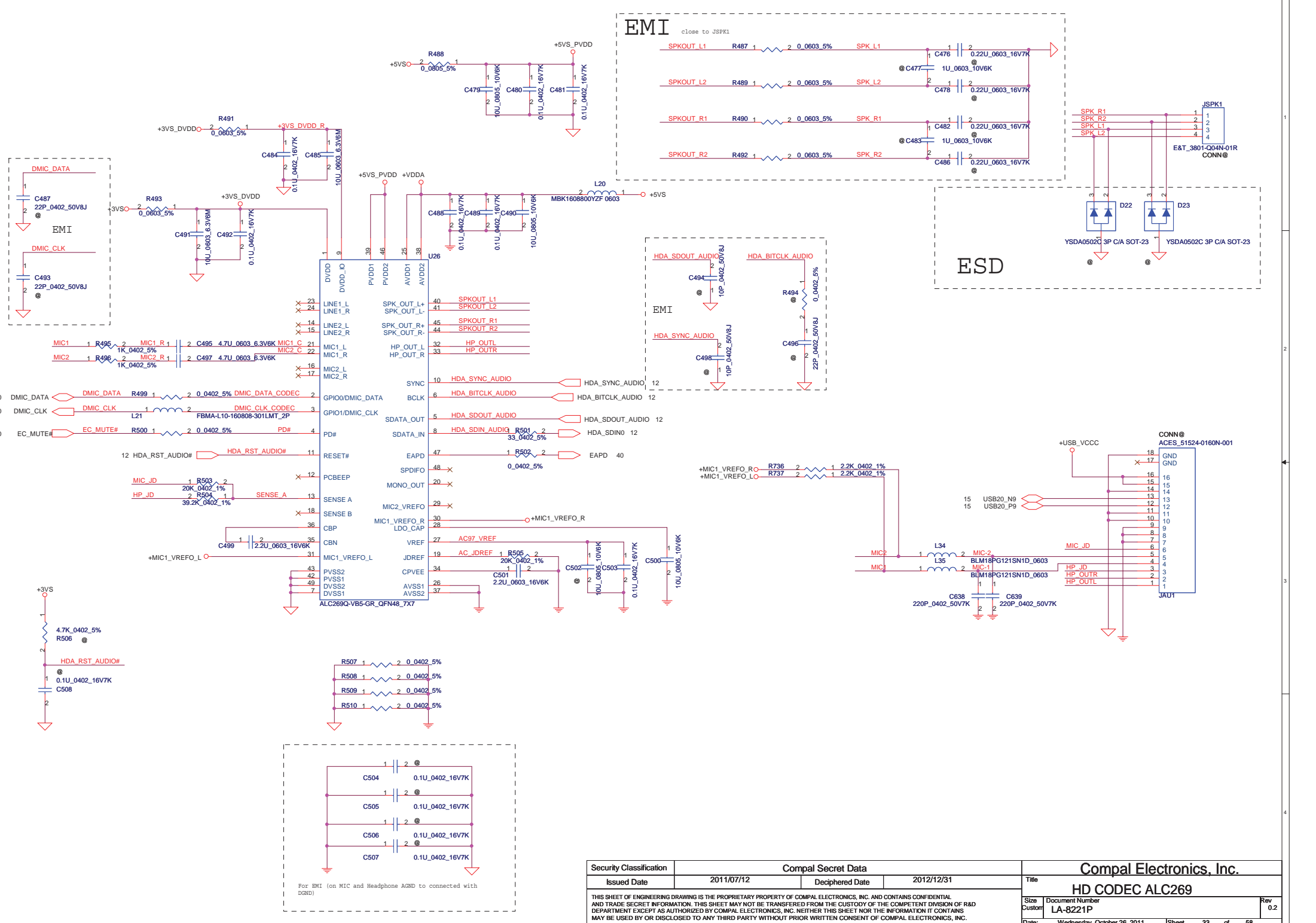
Place caps. near ODD CONN.



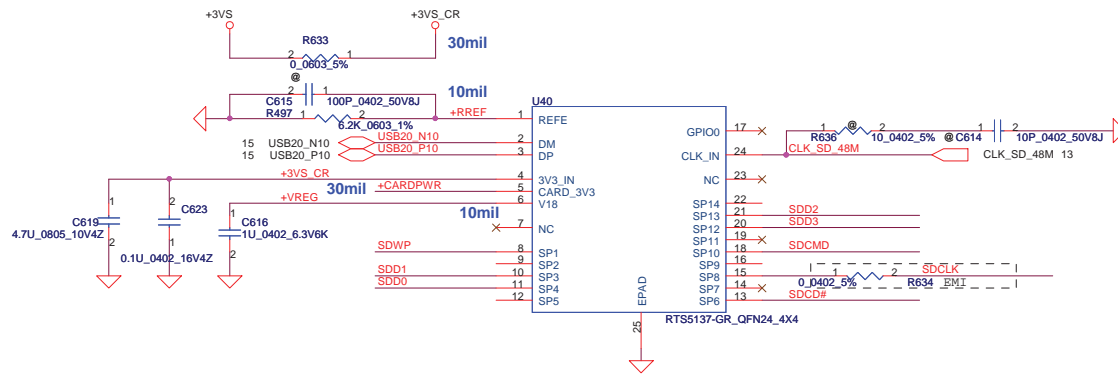
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Date: Wednesday, October 26, 2011				Sheet 31	of 58	



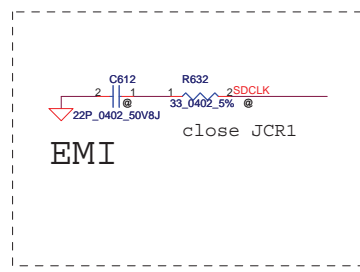
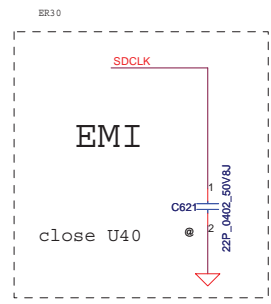
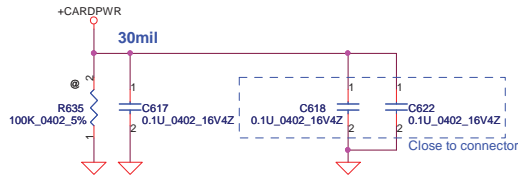
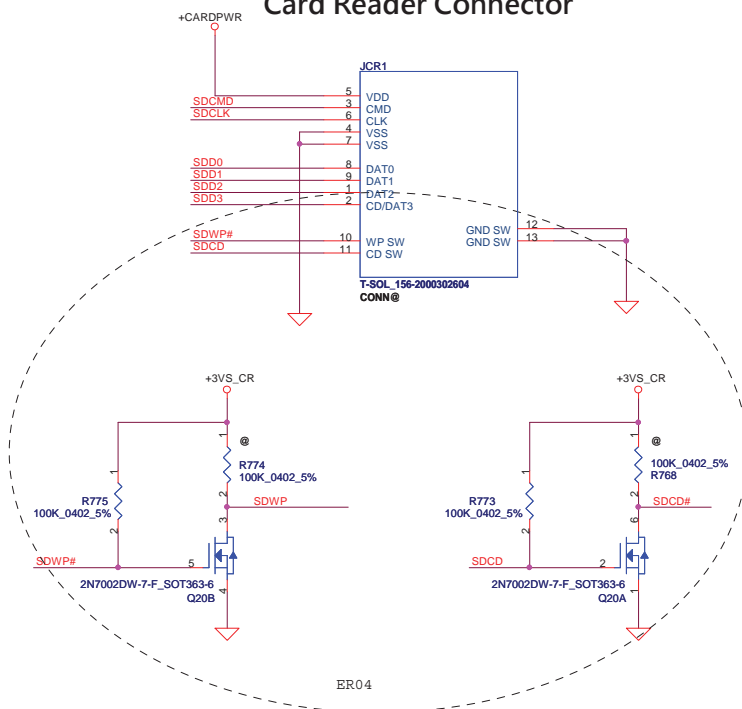
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Size	Document Number			Rev	
Custom	LA-8221P			0.2	
Date:	Wednesday, October 26, 2011	Sheet	32	of	58



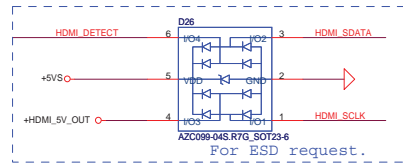
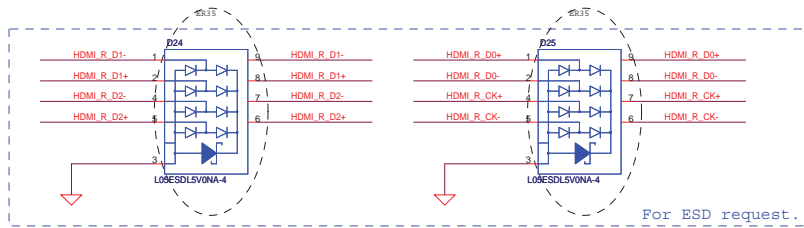
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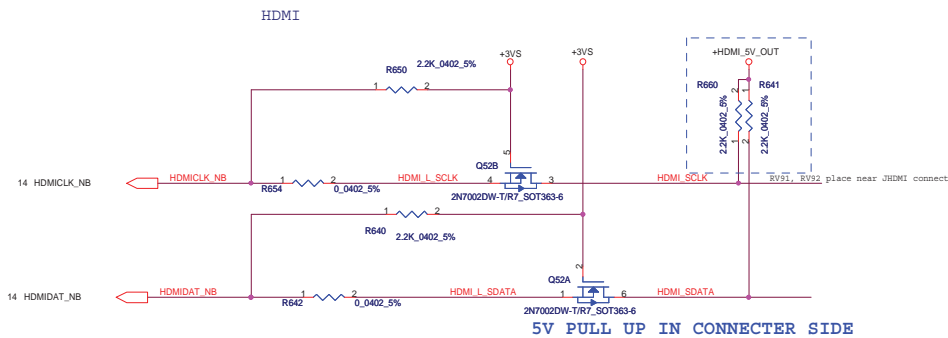
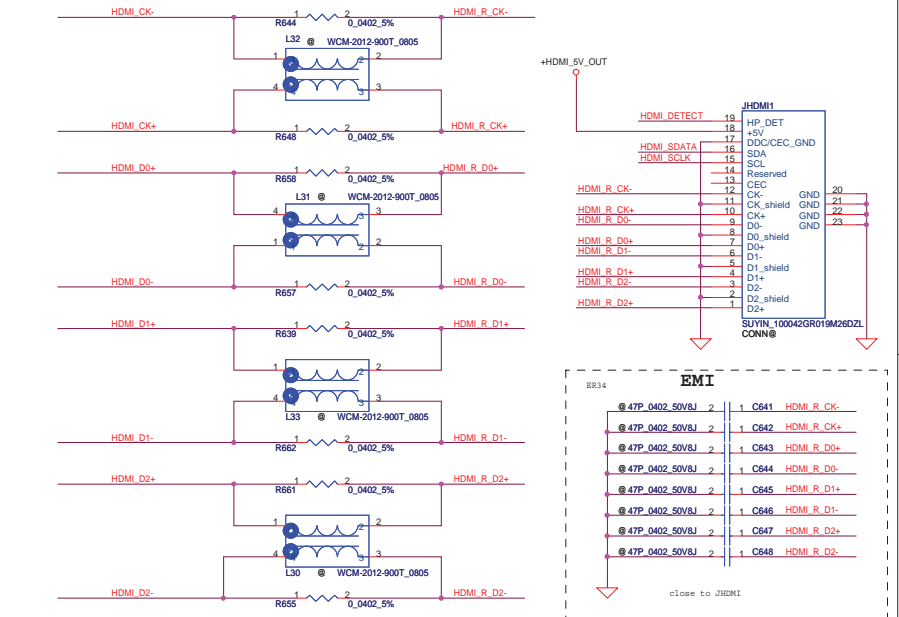
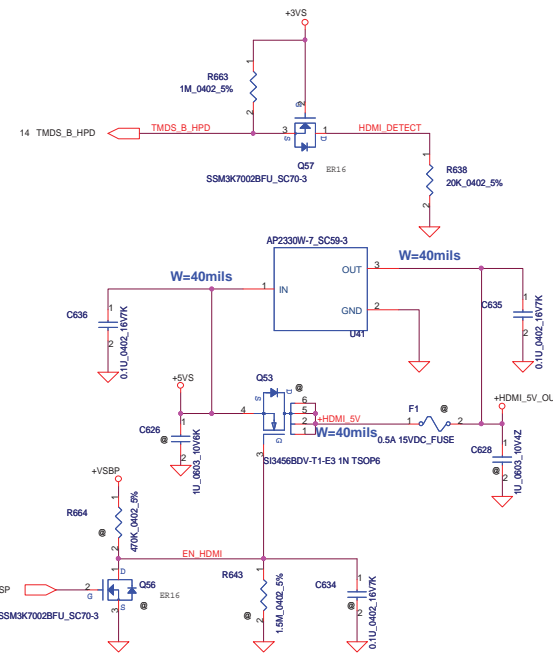
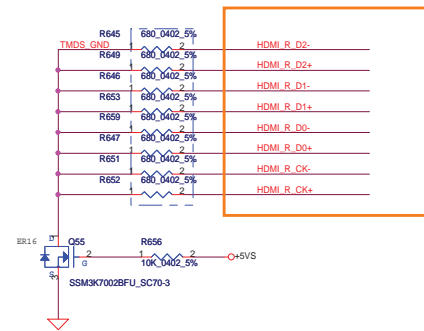
Card Reader Connector



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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title RTS5137 Media Card Controller	
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14	TMDS_B_CLK	TMDS_B_CLK	2	1	HDMI_CK+
14	TMDS_B_CLK#	0.1U_0402_16V7K	2	1	C625 HDMI_CK-
14	TMDS_B_DATA0	TMDS_B_DATA0	2	1	HDMI_D0+
14	TMDS_B_DATA0#	0.1U_0402_16V7K	2	1	C630 HDMI_D0-
14	TMDS_B_DATA1	TMDS_B_DATA1	2	1	HDMI_D1+
14	TMDS_B_DATA1#	0.1U_0402_16V7K	2	1	C633 HDMI_D1-
14	TMDS_B_DATA2	TMDS_B_DATA2	2	1	HDMI_D2+
14	TMDS_B_DATA2#	0.1U_0402_16V7K	2	1	C629 HDMI_D2-
					C632

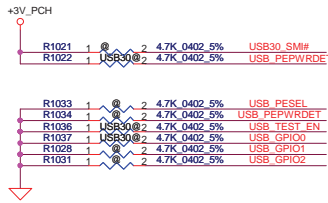
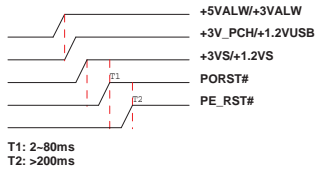


ER02 Add USB3.0 (ASM1042)

	S3	S4/S5
+3V_PCH	V	X
+3VS	X	X
+1.2VUSB	V	X
+1.2VS	X	X

Power Sequence

ASM1042



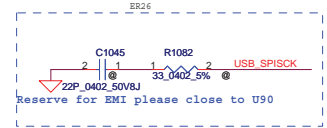
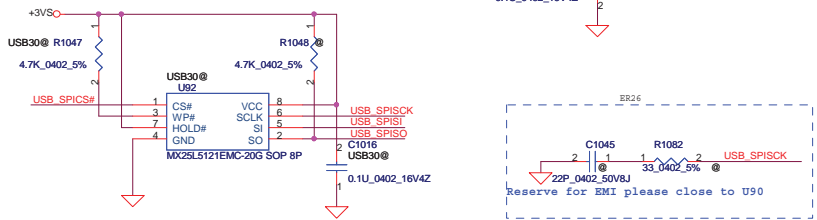
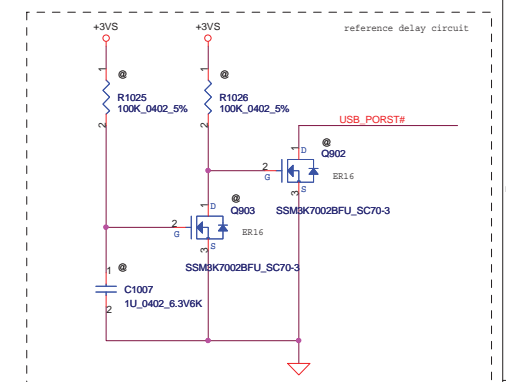
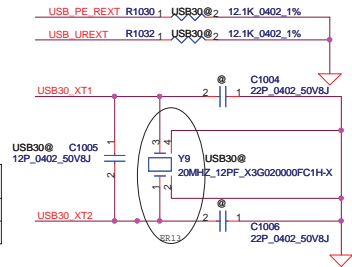
For WAKE Function

USB_PEPWRDET

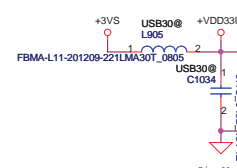
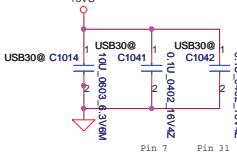
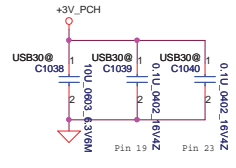
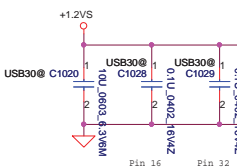
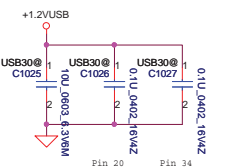
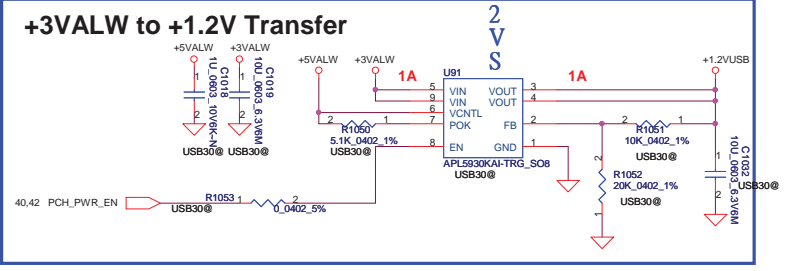
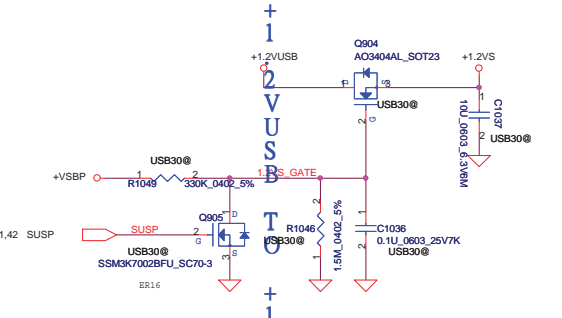
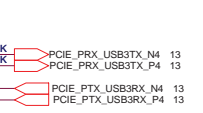
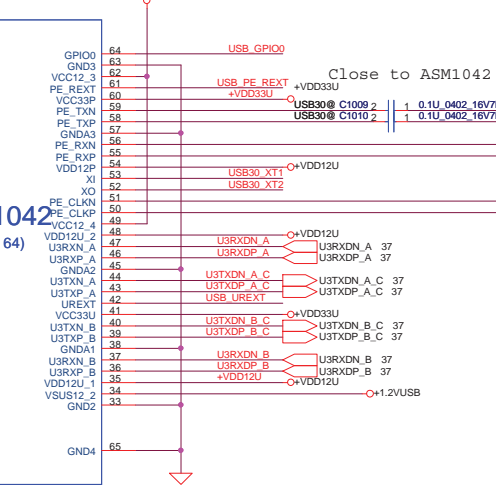
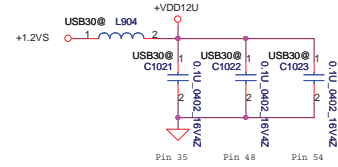
	R1034	R1022
S1	Mount	@
* S3	@	Mount

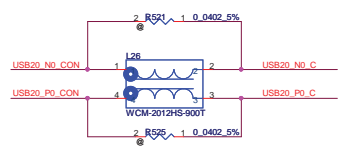
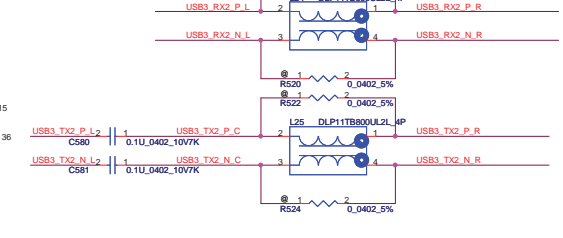
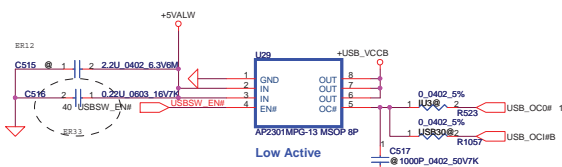
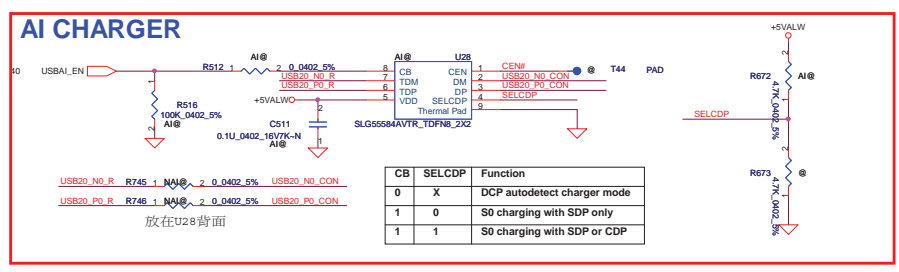
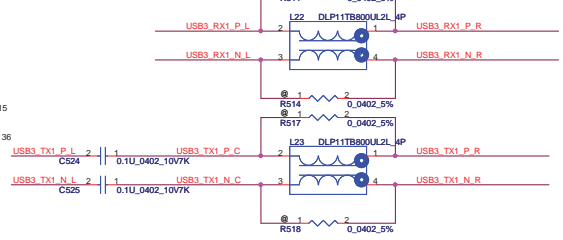
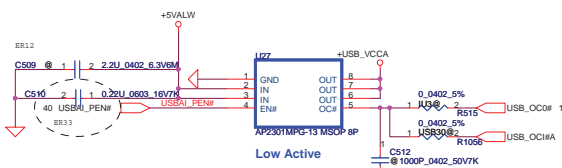
USB_PESEL

	R1033
* Other application	@
Express Card/Mini Card	Mount

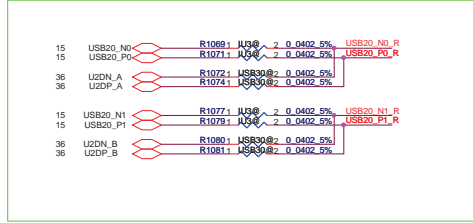
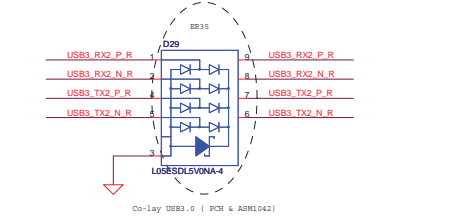
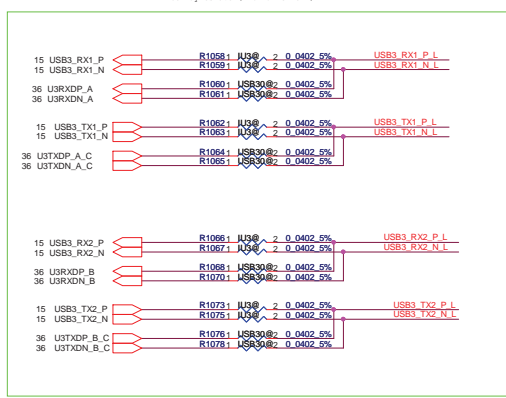
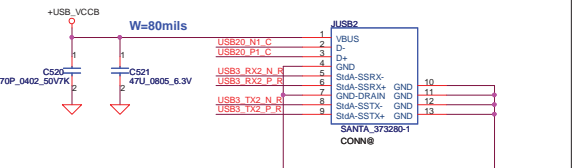
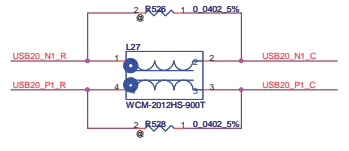
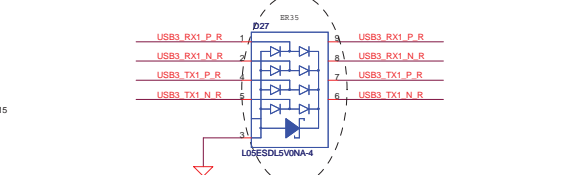
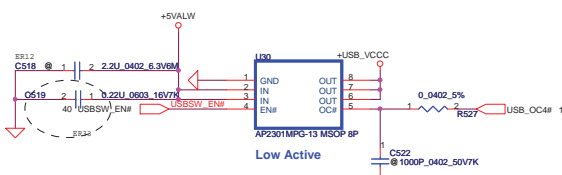
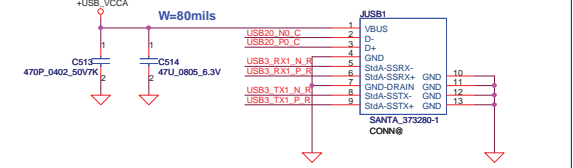


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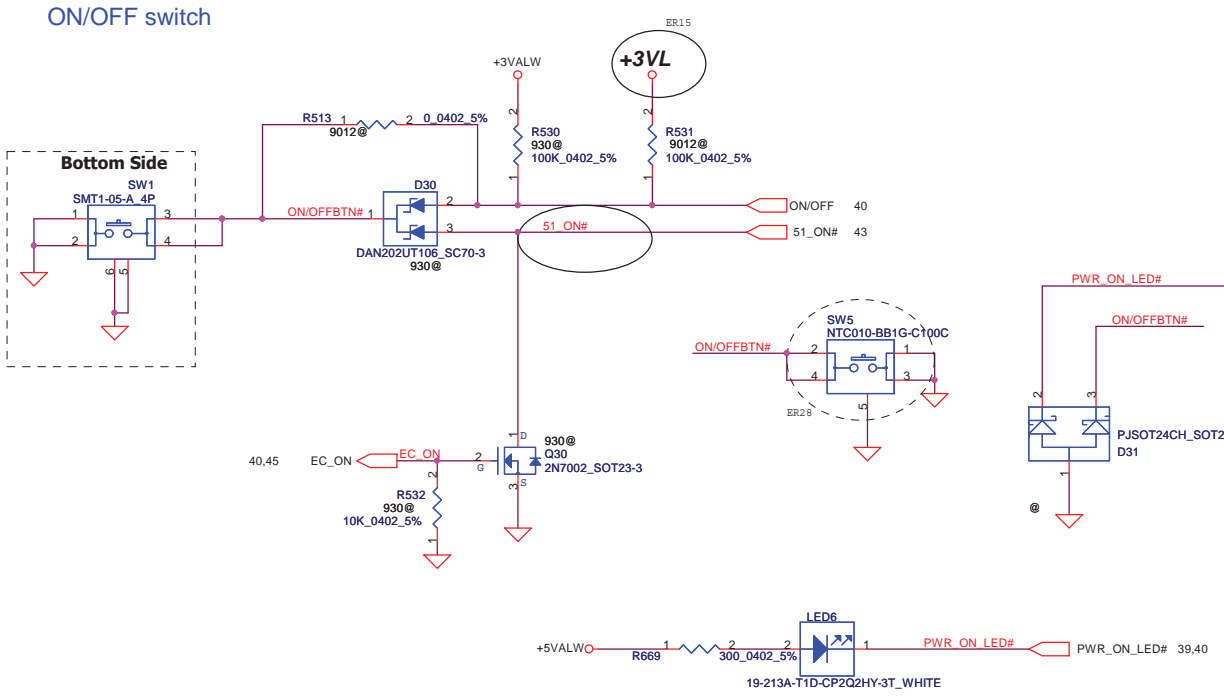
charger port: left side & near user



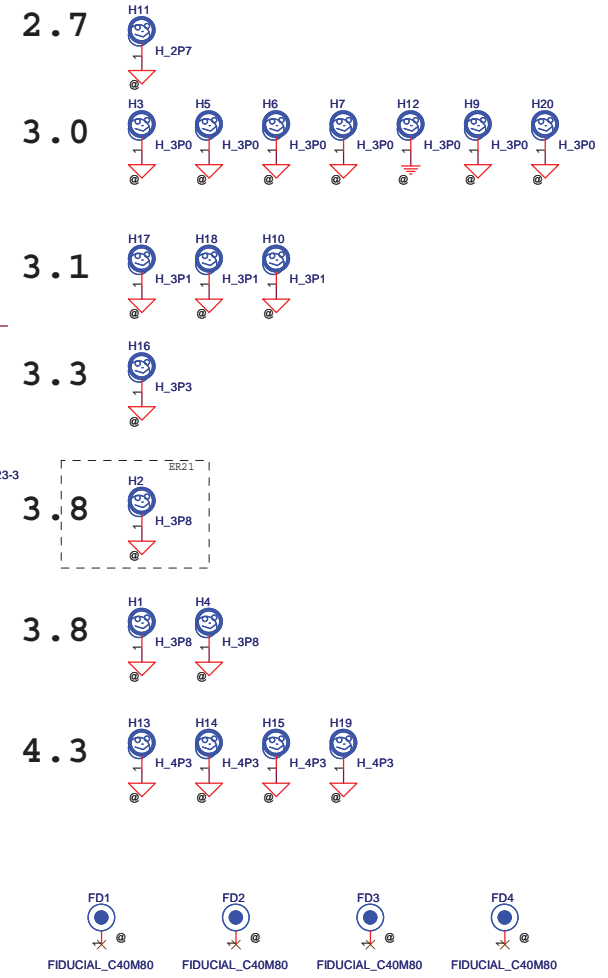
ER02 Add USB3.0 (ASM1042)

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				Document Number
				LA-8221P
				Rev
				0.2
				Date: Wednesday, October 26, 2011
				Sheet 37 of 58

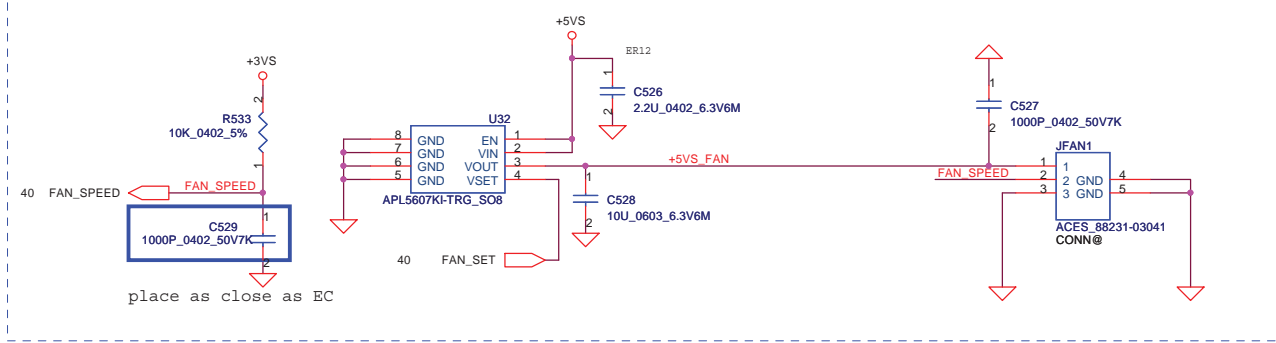
Power Button



Screw Hole



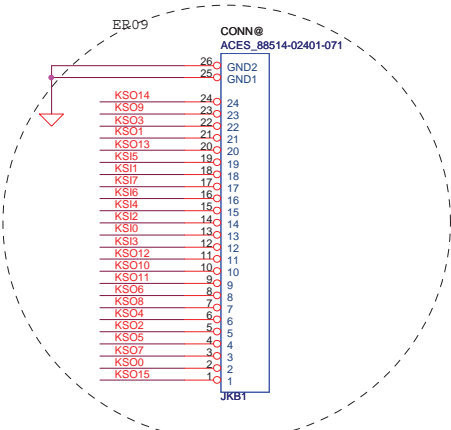
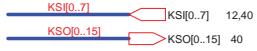
Fan Control Circuit



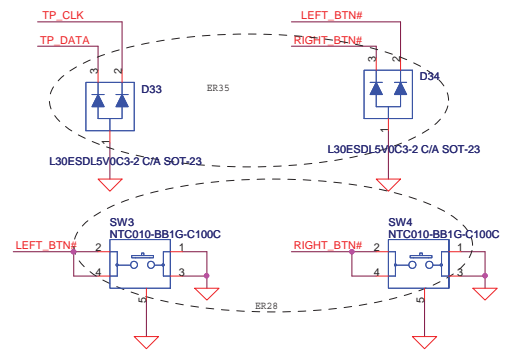
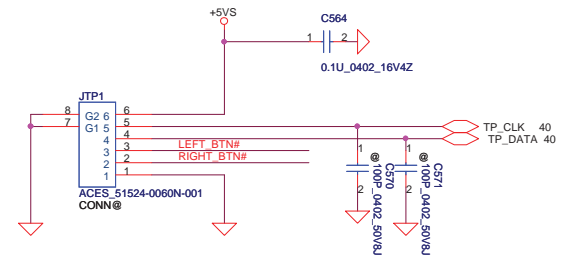
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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INT_KBD Conn.

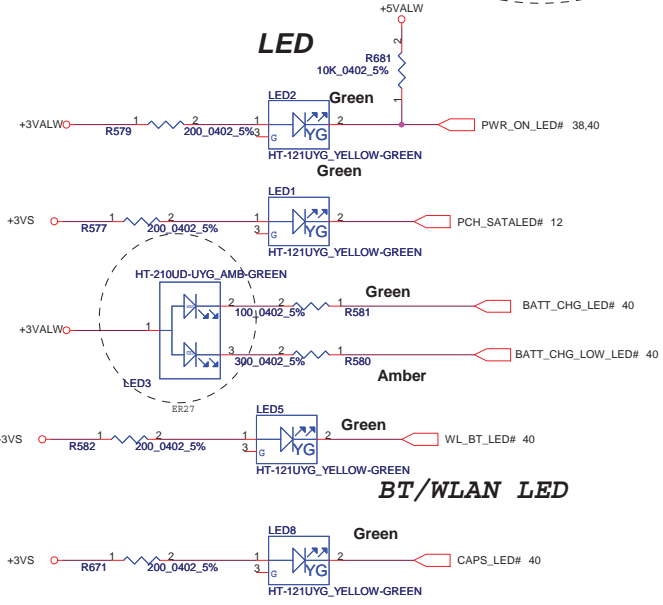
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KSO11	@	1	2
KSO12	@	1	2
KSO15	@	1	2
KSI7	@	1	2
KSI2	@	1	2
KSI3	@	1	2
KSI4	@	1	2
KSI0	@	1	2
KSI5	@	1	2
KSI6	@	1	2
KSI1	@	1	2
KSO2	@	1	2
KSO1	@	1	2
KSO0	@	1	2
KSO4	@	1	2
KSO3	@	1	2
KSO5	@	1	2
KSO14	@	1	2
KSO6	@	1	2
KSO7	@	1	2
KSO13	@	1	2
KSO8	@	1	2
KSO9	@	1	2



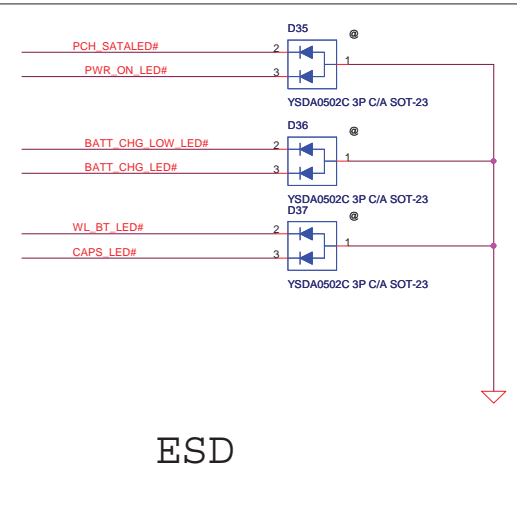
Touch/B Connector



LED

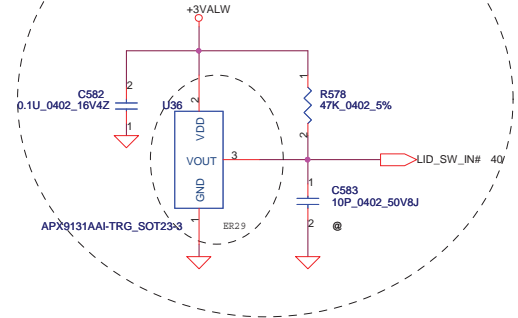


BT/WLAN LED

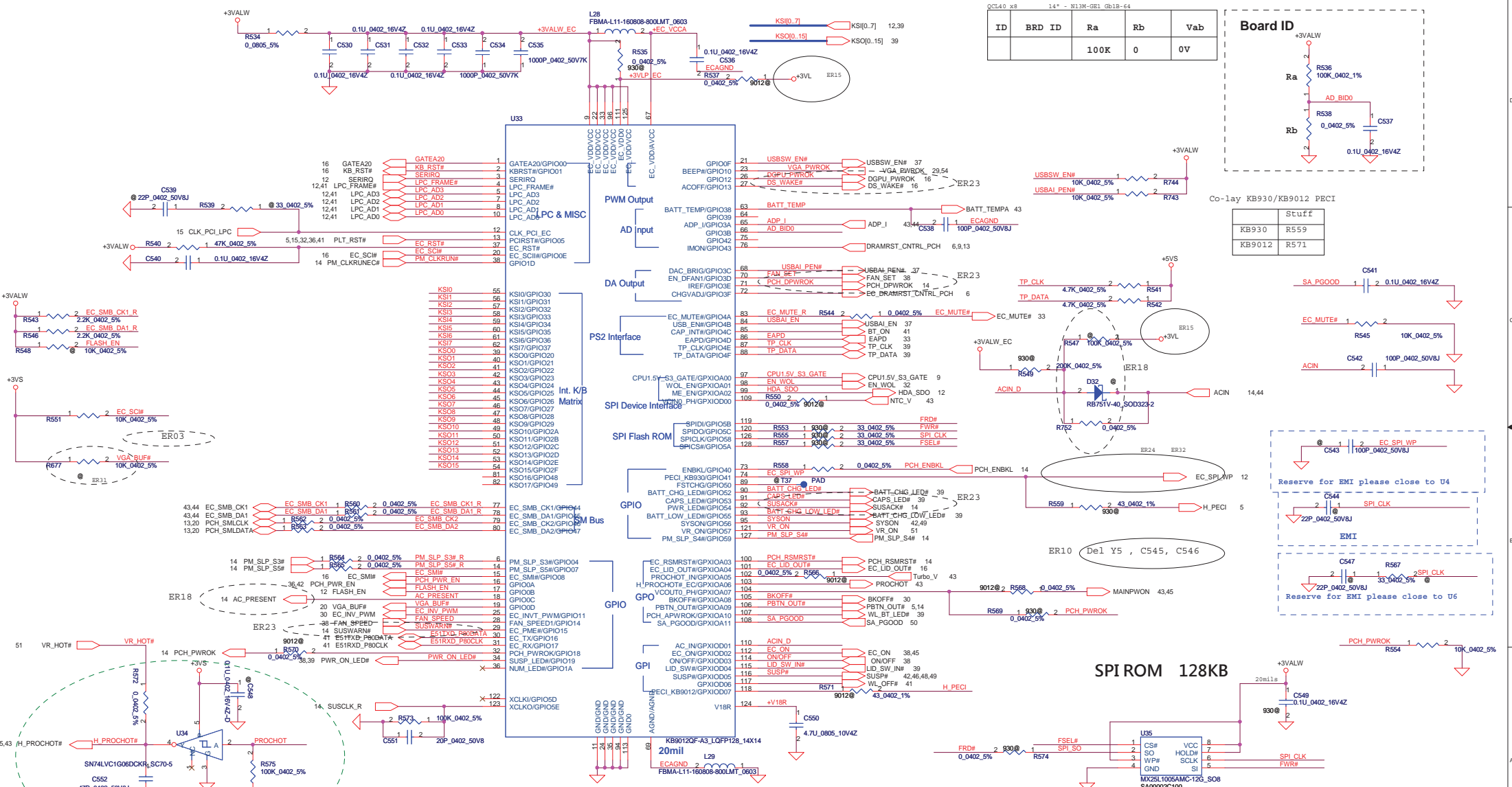


ESD

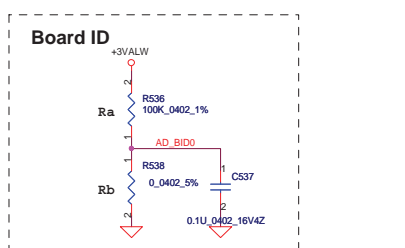
Lid Switch (Hall Effect Switch)



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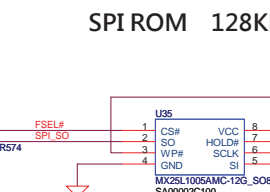
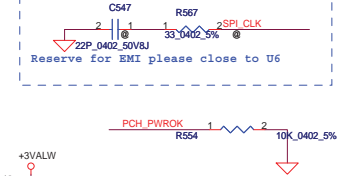
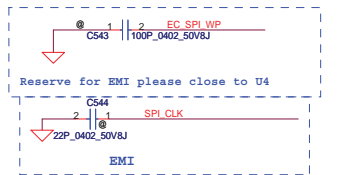
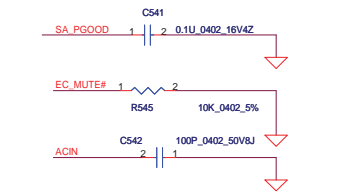


ID	BRD ID	Ra	Rb	Vab
		100K	0	0V



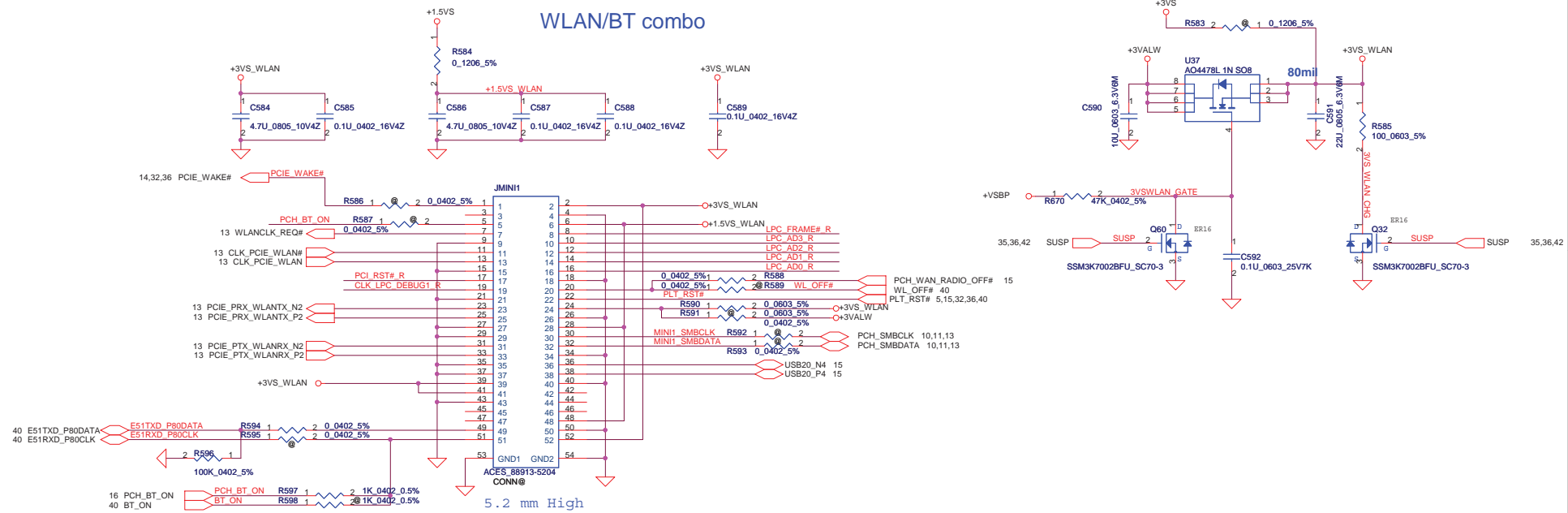
Co-lay KB930/KB9012 PCB1

Stuiff
KB930
R559
KB9012
R571



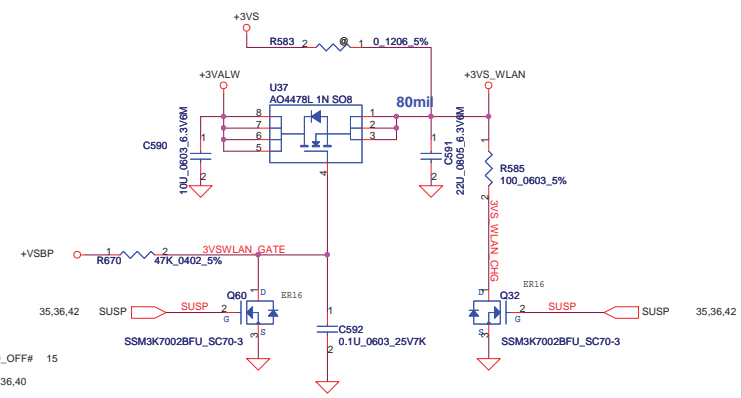
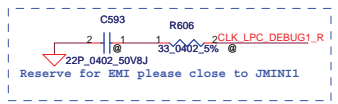
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Title			Rev
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Size	Document Number	Date	
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WLAN/BT combo

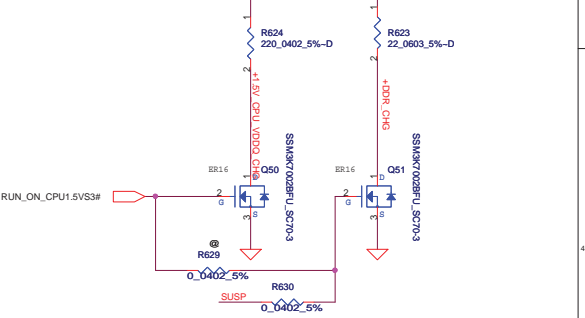
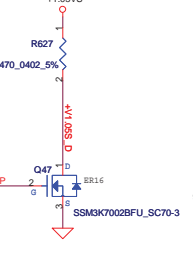
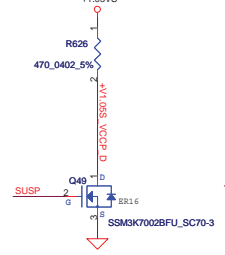
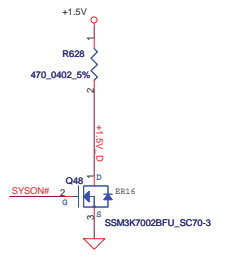
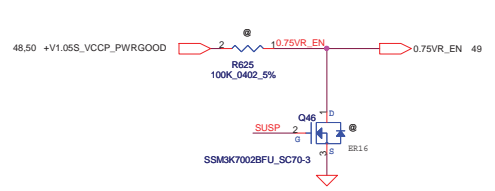
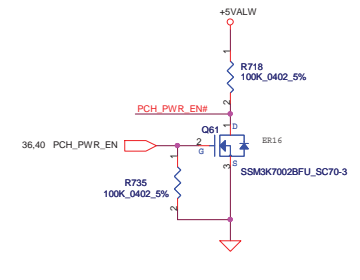
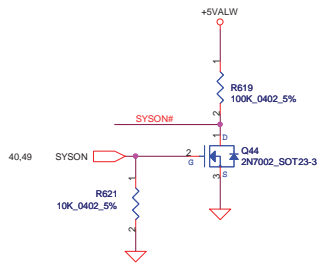
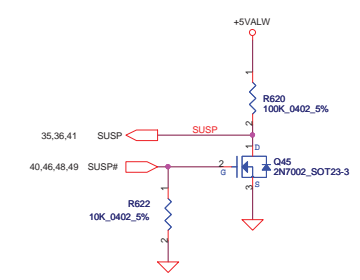
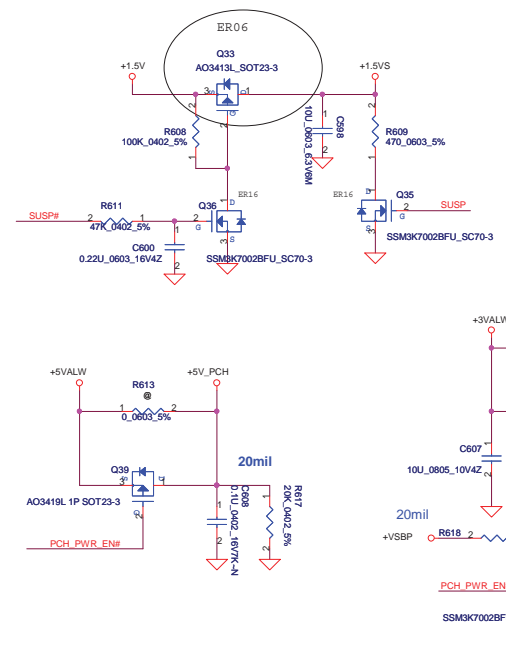
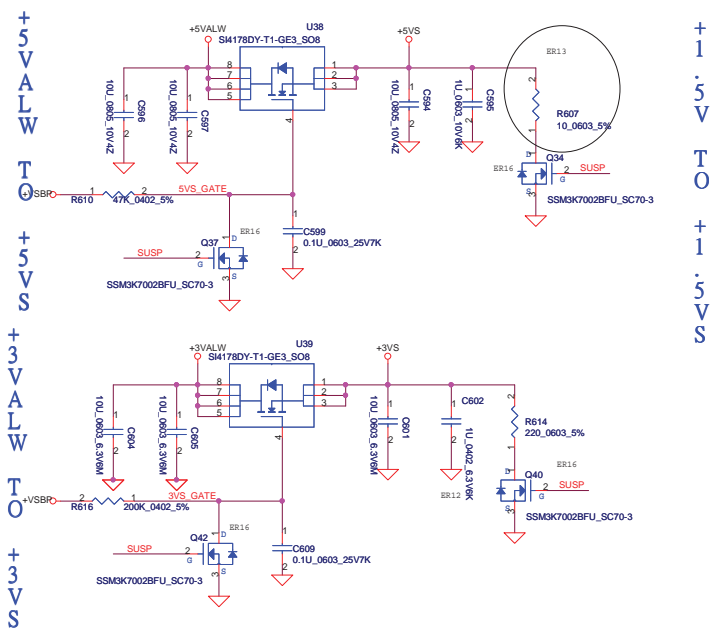


**Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.**

LPC_FRAME#_R	R599	1	2	0.0402_5%	LPC_FRAME#	12,40
LPC_AD3_R	R600	1	2	0.0402_5%	LPC_AD3	12,40
LPC_AD2_R	R601	1	2	0.0402_5%	LPC_AD2	12,40
LPC_AD1_R	R602	1	2	0.0402_5%	LPC_AD1	12,40
LPC_AD0_R	R603	1	2	0.0402_5%	LPC_AD0	12,40
PLT_RST#_R	R604	1	2	0.0402_5%	PLT_RST#	12,40
CLK_LPC_DEBUG1_R	R605	1	2	0.0402_5%	CLK_LPC_DEBUG1	15

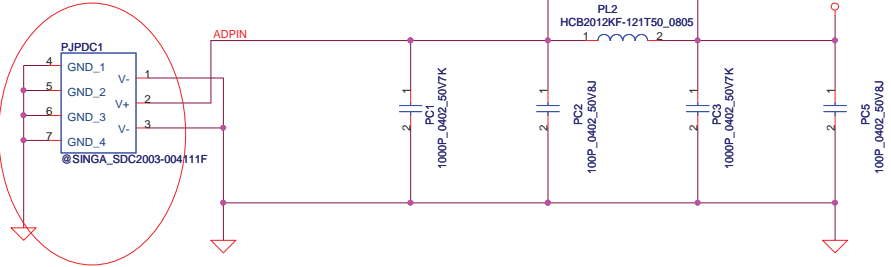


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				Sheet 41 of 58

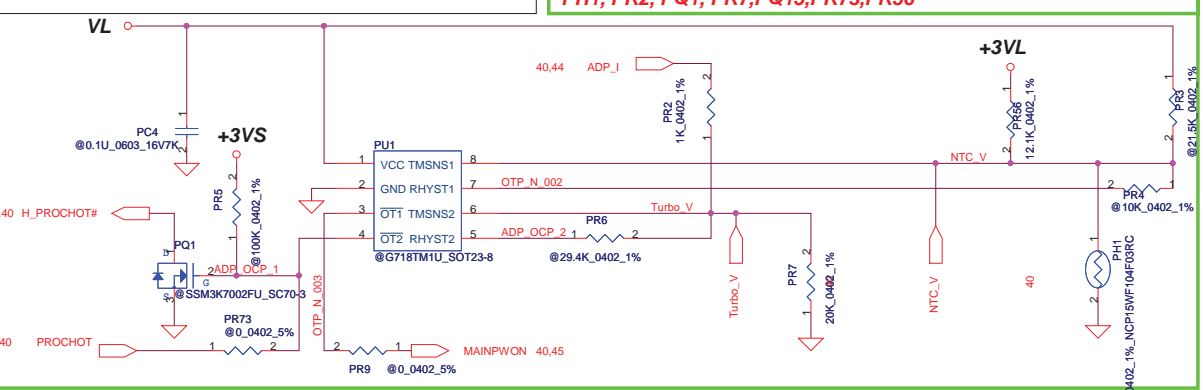


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Size	Document Number	Rev	0.2	
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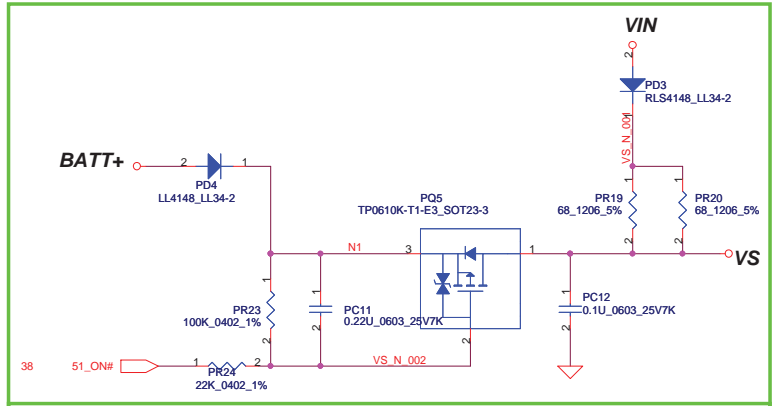
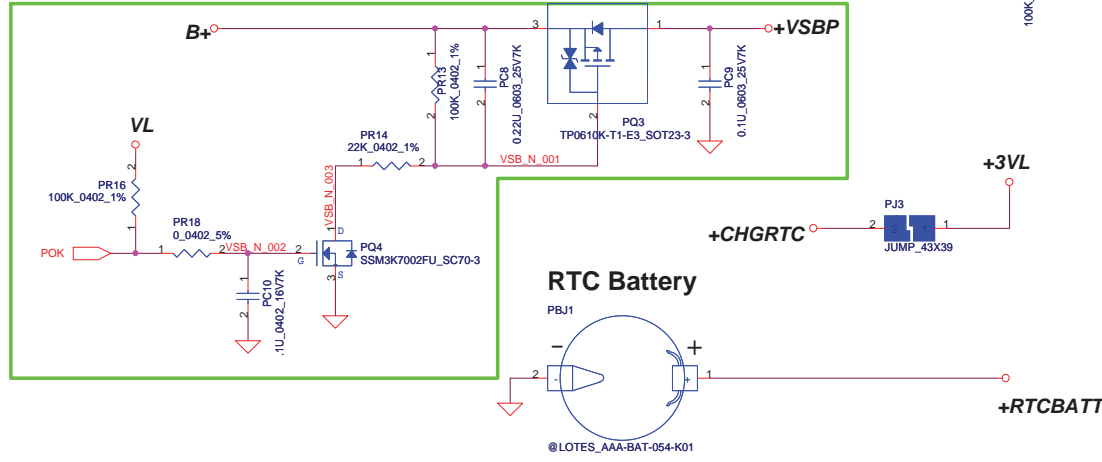
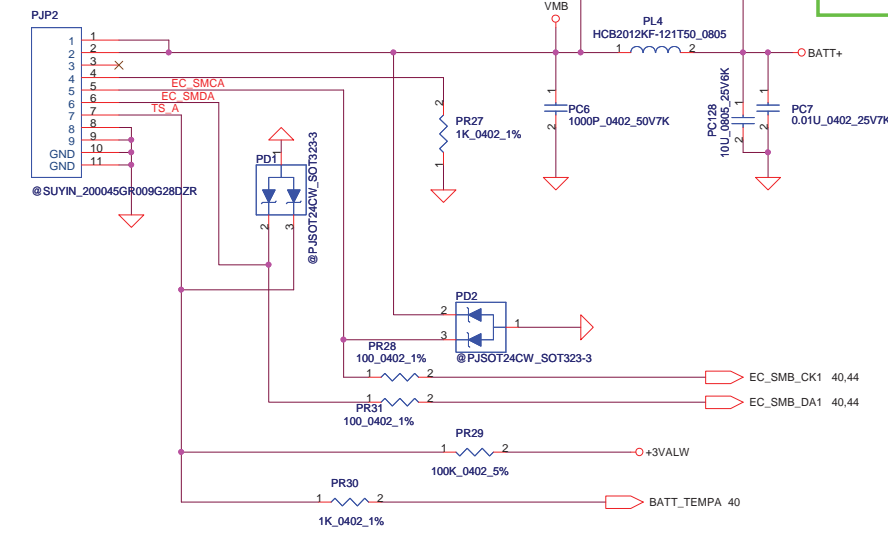
DCIN jack P/N:DC301008L00,
need double confirm P/N with ME



PH1 under CPU bottom side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C



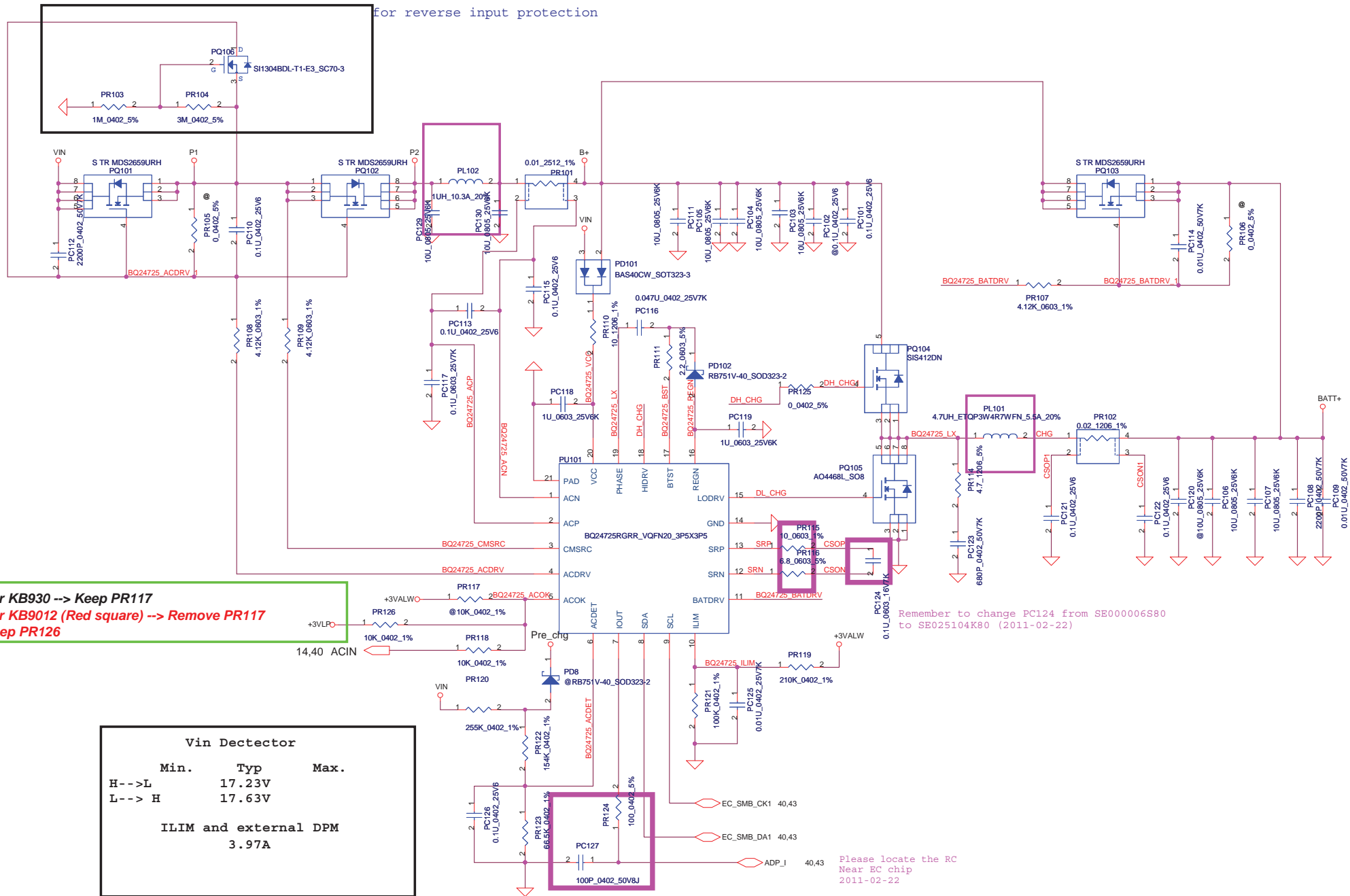
For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU1 circuit, but keep PR56
PH1, PR2, PQ1, PR7, PQ15, PR73, PR56



For KB9012 --> Remove all 51_ON# circuit

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Compal Electronics, Inc.		
PWR-DCIN / BATT CONN / OTP		
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Date:	Wednesday, October 26, 2011	Sheet 43 of 58



for reverse input protection

For KB930 --> Keep PR117
 For KB9012 (Red square) --> Remove PR117
 Keep PR126

Vin Detector

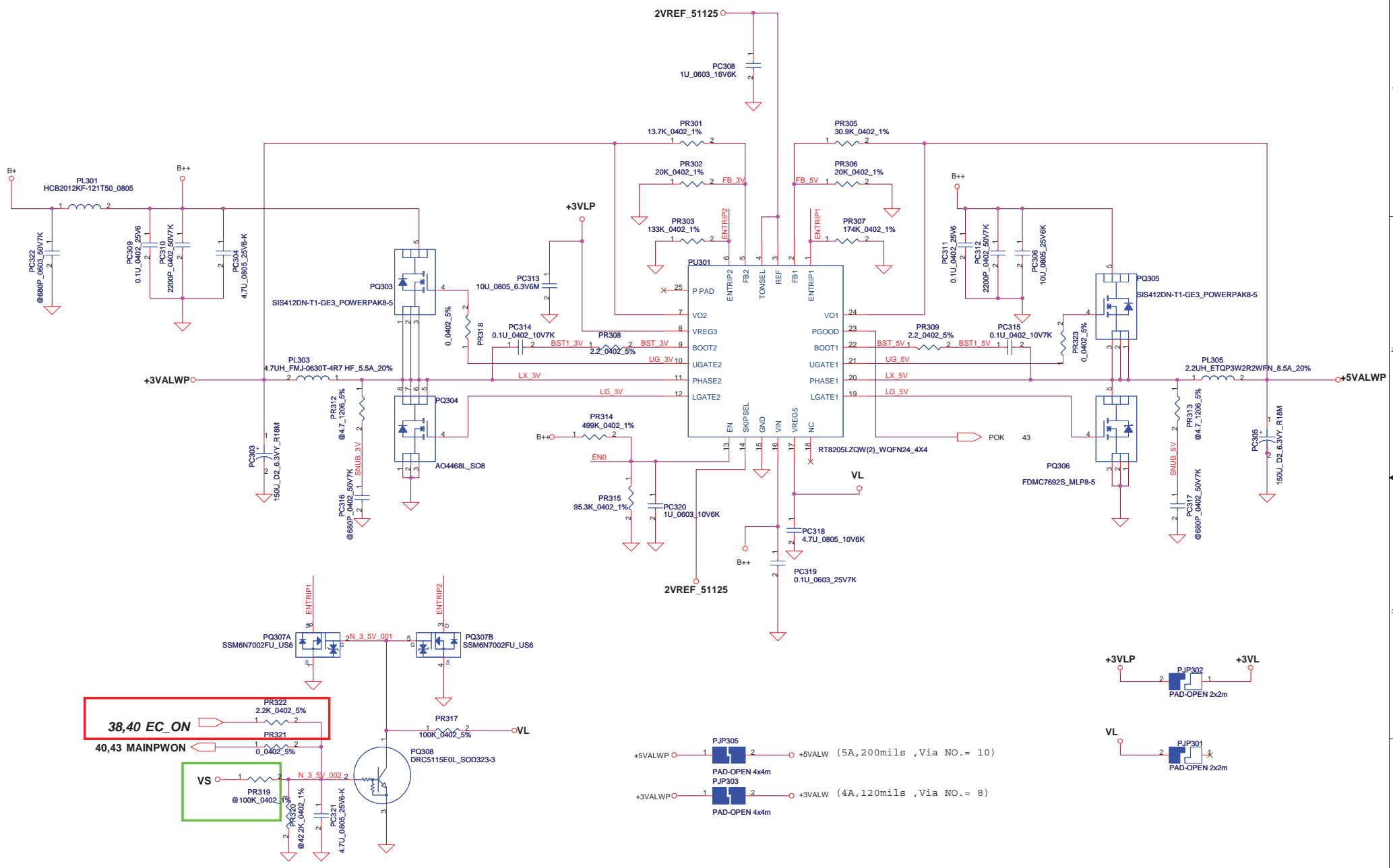
	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	

ILIM and external DPM
 3.97A

Remember to change PC124 from SE000006S80 to SE025104K80 (2011-02-22)

Please locate the RC Near EC chip 2011-02-22

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Date:	Wednesday, October 26, 2011	Sheet	44 of 58		



38,40 EC_ON
40,43 MAINPWON

VS
 PR319 @100K_0402_1%

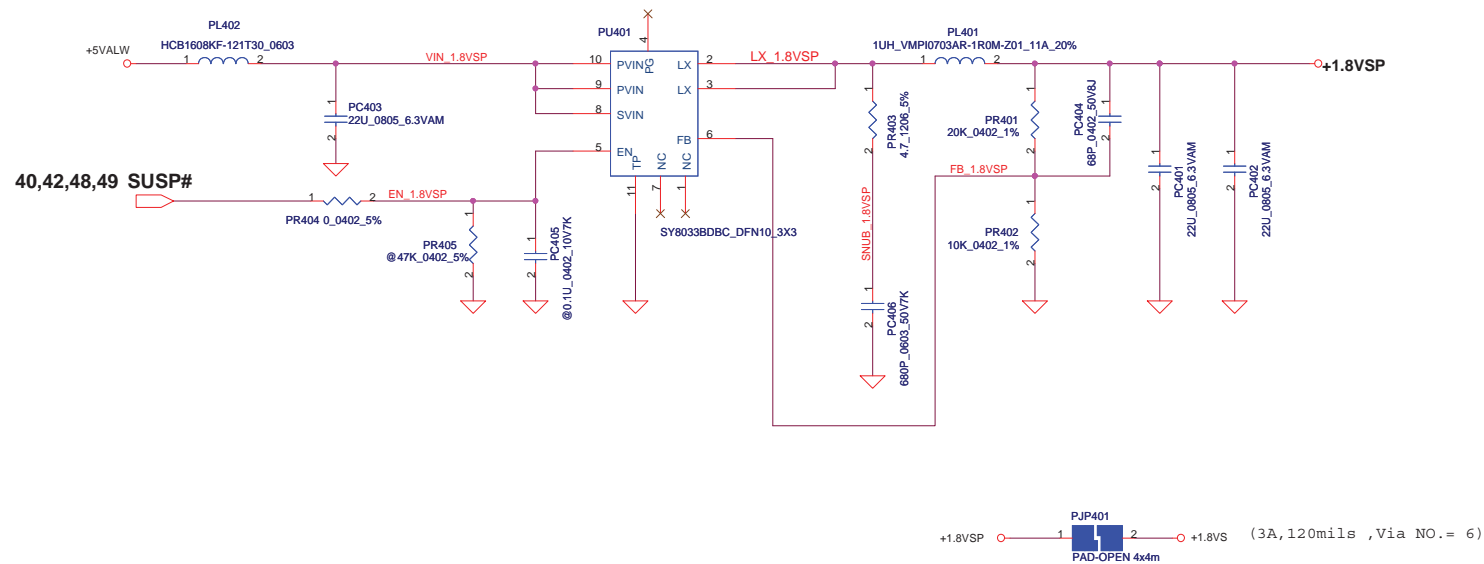
For KB930 --> Keep PR319, Remove PR322
For KB9012 (Red square) --> Remove PR319
Keep PR322

+5VALWP 1 PJP305 2 +5VALW (5A,200mils ,Via NO.= 10)
 PAD-OPEN 4x4m
 PJP303
 +3VALWP 1 PJP301 2 +3VALW (4A,120mils ,Via NO.= 8)
 PAD-OPEN 4x4m

+3VLP 2 PJP302 1 PAD-OPEN 2x2m
 VL 2 PJP301 1 PAD-OPEN 2x2m

Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	Compal Electronics, Inc.	
				PWR-3.3VALWP/SVALWP	
Size	Document Number			Rev	0.2
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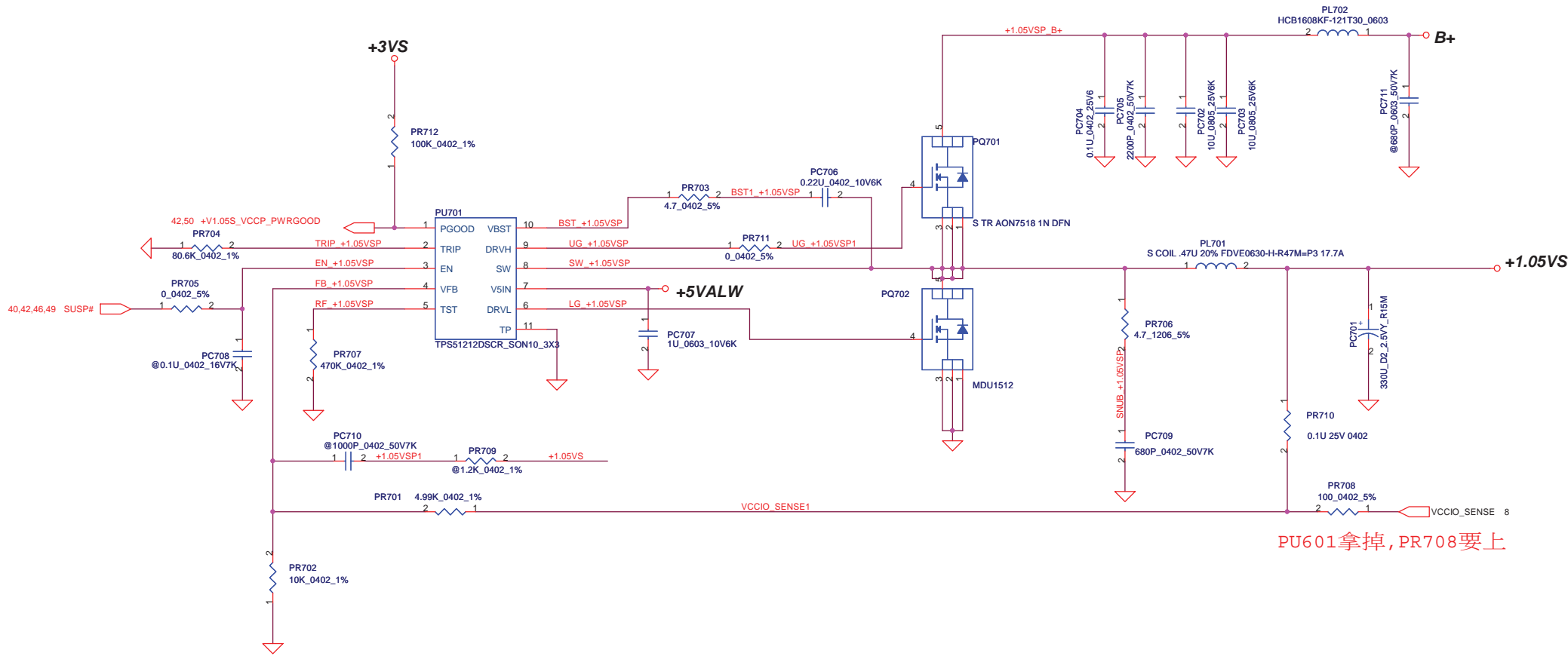
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Issued Date	2009/01/23	Deciphered Date	2012/12/31
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Compal Electronics, Inc.		
PWR-1.8VSP		
Size	Document Number	Rev
	PBL22 LA-7391P M/B	0.2
Date:	Wednesday, October 26, 2011	Sheet 46 of 58

(8.5A,360mils ,Via NO.= 17)

PJP606 ,PJP607先斷開,確定拿掉PU605再接上

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2010/07/20	Deciphered Date	2012/12/31	Title	PWR-V1.05S VCCP	
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				Custom	PBL22 LA-7391P M/B	0.2
Date:	Wednesday, October 26, 2011	Sheet	47	of	58	

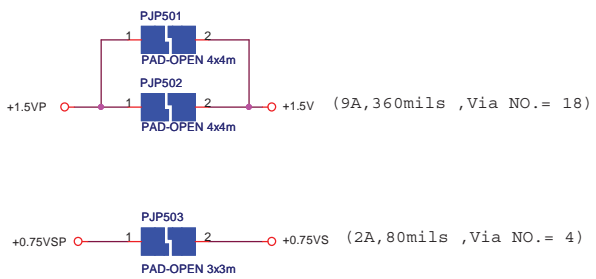
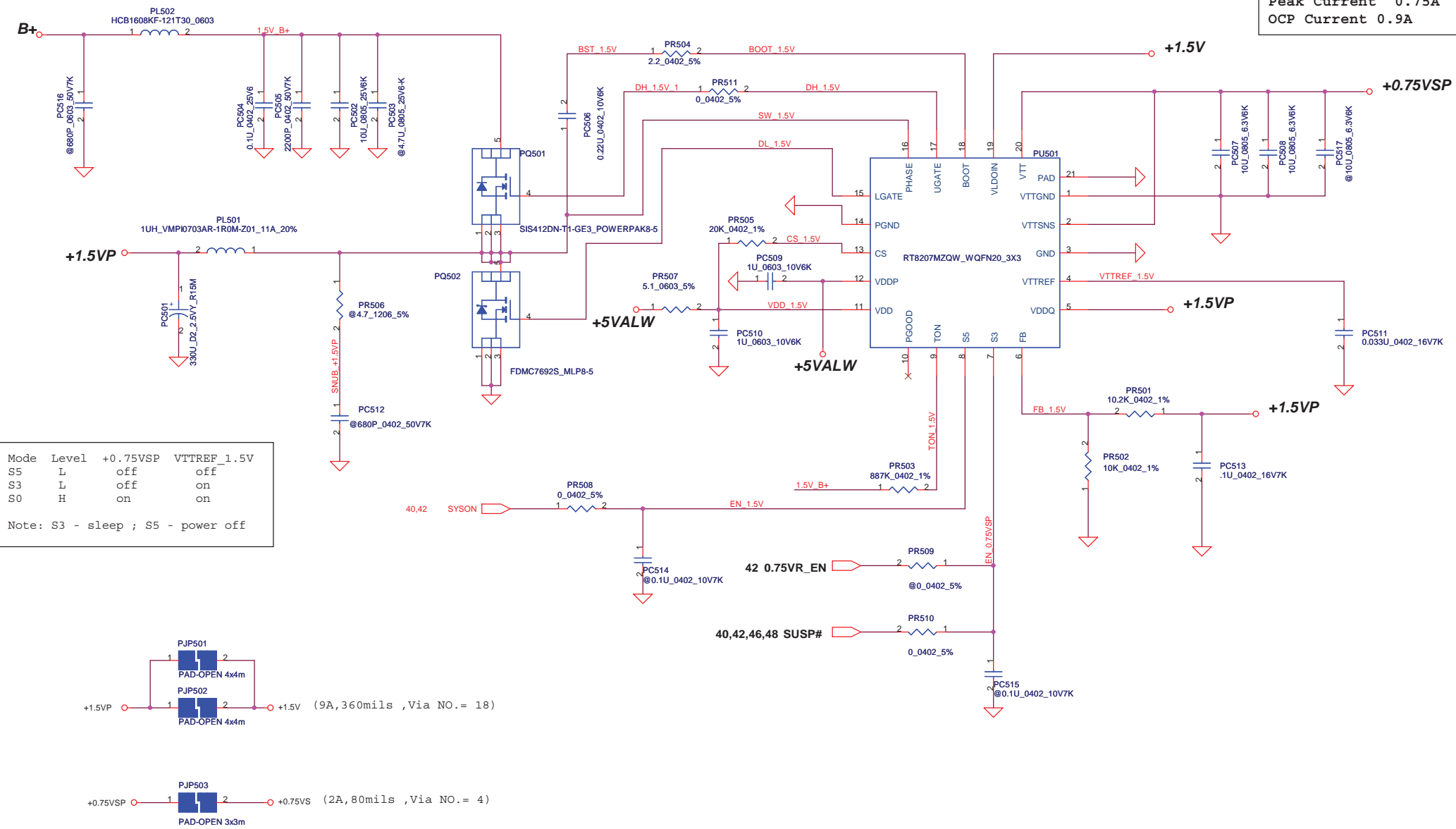


PU601拿掉, PR708要上

(12A, 480mils , Via NO. = 24)

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Size	Document Number	Date:		Rev	
Custom	PBL22 LA-7391P M/B	Wednesday, October 26, 2011		0.2	
			Sheet	48 of 58	

0.75Volt +/- 5%
 TDC 0.525A
 Peak Current 0.75A
 OCP Current 0.9A



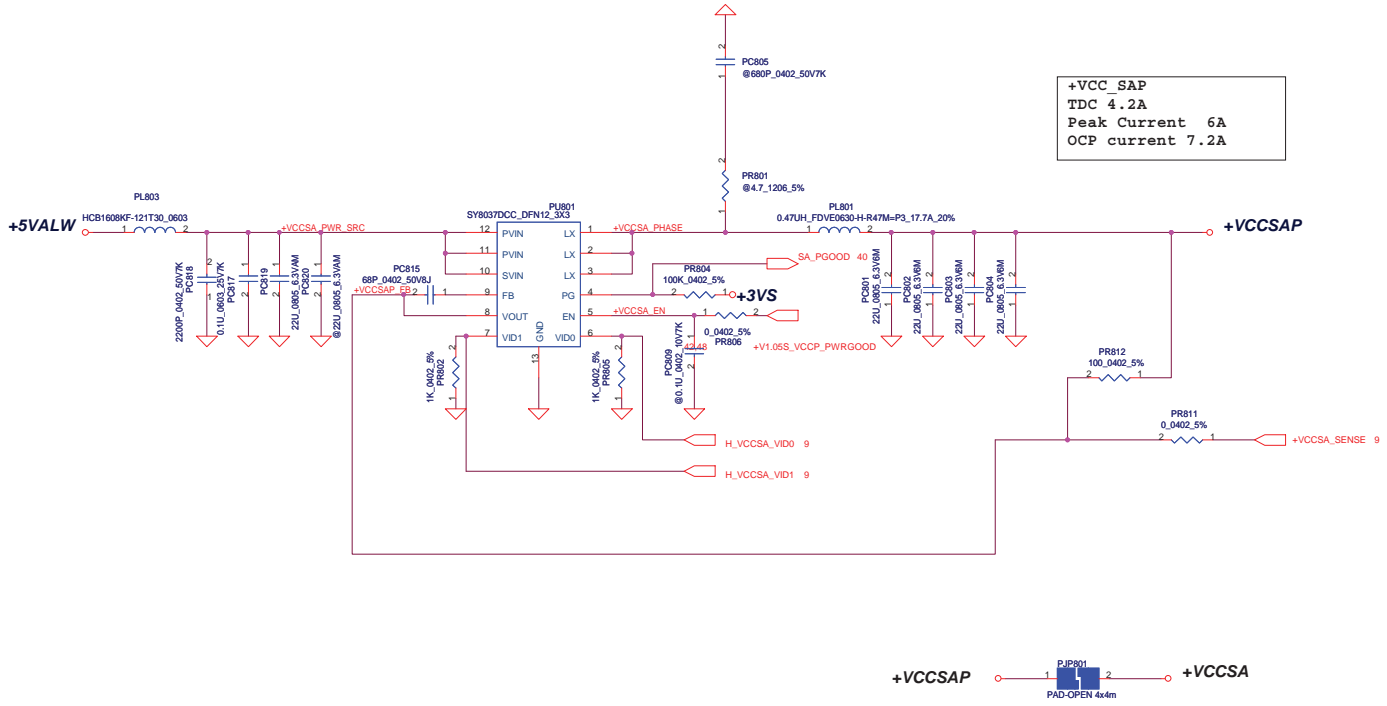
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/20	Deciphered Date	2012/12/31	Title	
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Size	Document Number			Rev	
Custom	PBL22 LA-7391P M/B			0.2	
Date:	Wednesday, October 26, 2011	Sheet	49	of	58

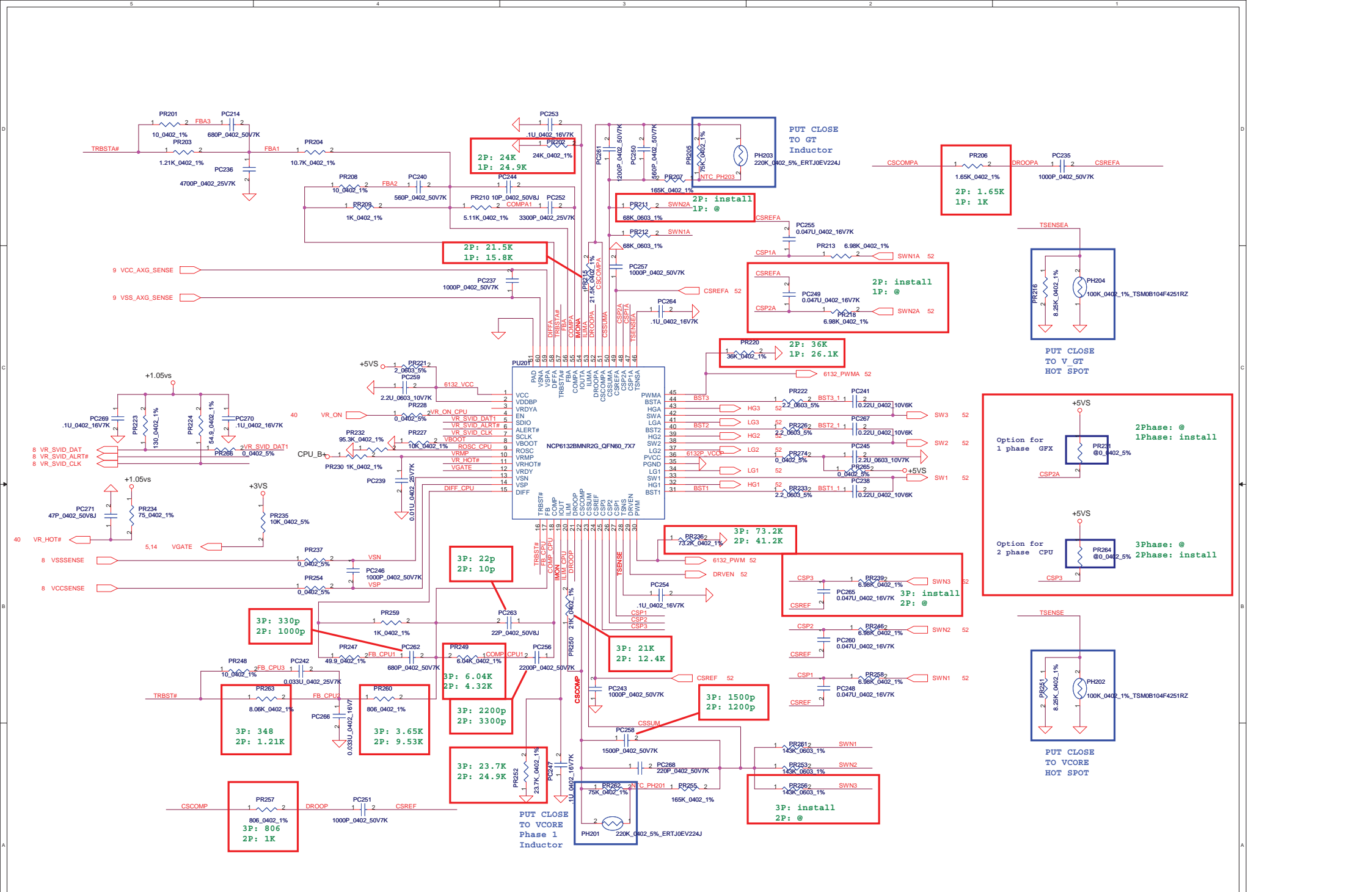
The 1k PD on the VCCSA VIDs are empty.
 These should be stuffed to ensure that
 VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID [1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

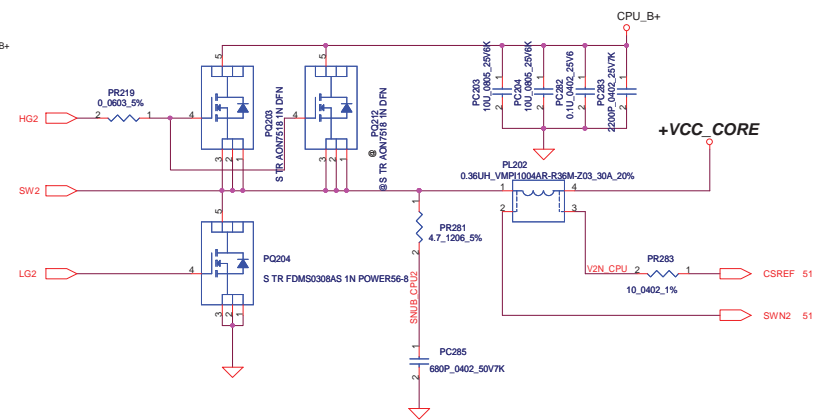
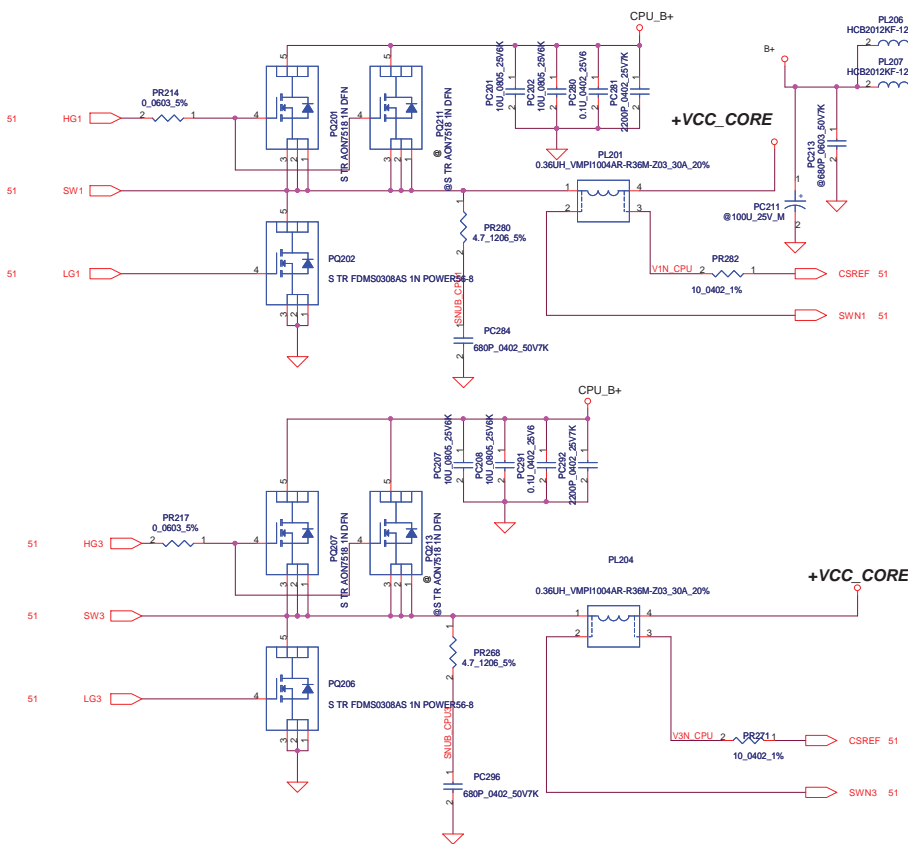
+VCC SAP
 TDC 4.2A
 Peak Current 6A
 OCP current 7.2A





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Compal Electronics, Inc.		
PWR-CPU_CORE		
Size Custom	Document Number	Rev
	PBL22 LA-7391P M/B	0.2
Date:	Wednesday, October 26, 2011	Sheet 51 of 58

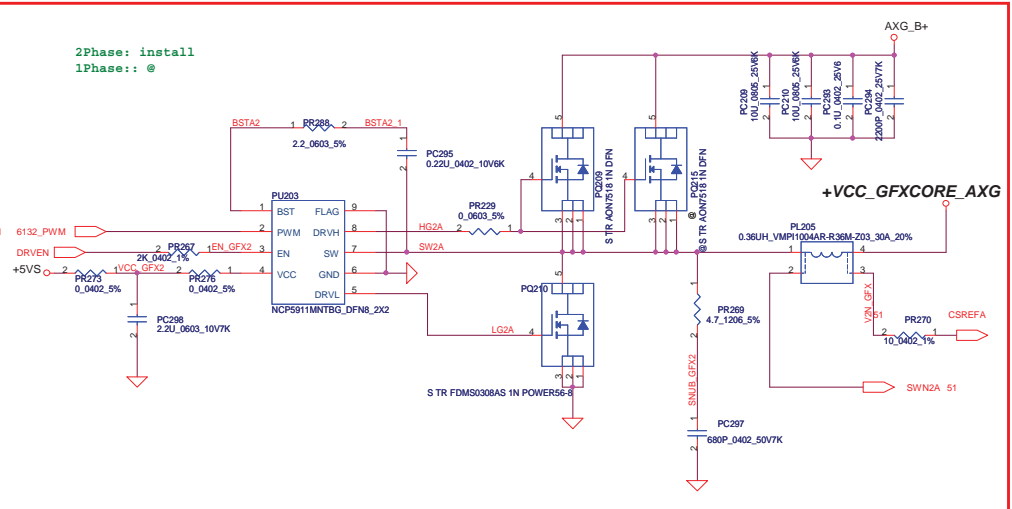
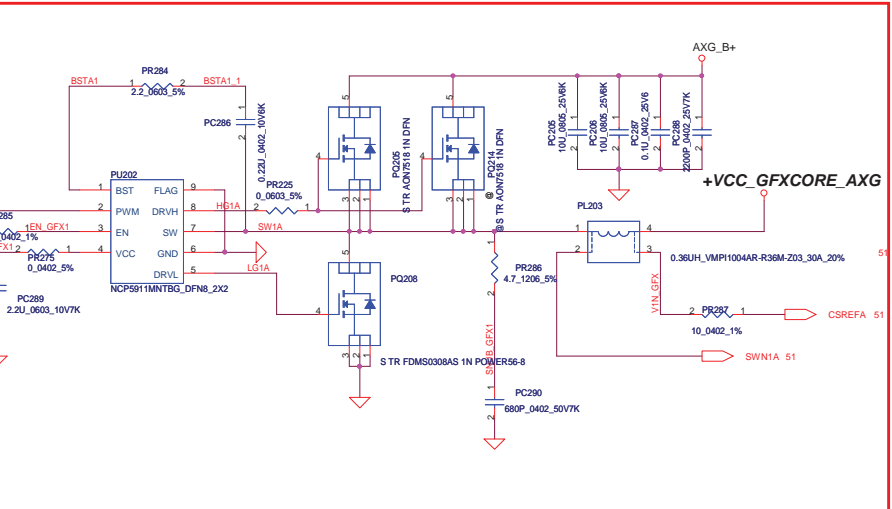


QC 45W CPU
 solution: 3+2
 MOS: cpu_core --> 上1(CSD17308) 下1(TPCA8059)
 Gfx_core --> 上1(CSD17308) 下1(TPCA8059)

DC 35W CPU
 solution: 2+1
 MOS: cpu_core --> 上1(CSD17308) 下1(TPCA8059)
 Gfx_core --> 上1(CSD17308) 下1(TPCA8057)

QC 45W CPU
 VID1=0.9V
 lccMax=94A
 lcc_Dyn=66A
 R_TDC=56A
 R_LL=1.9m ohm
 OCP=110A

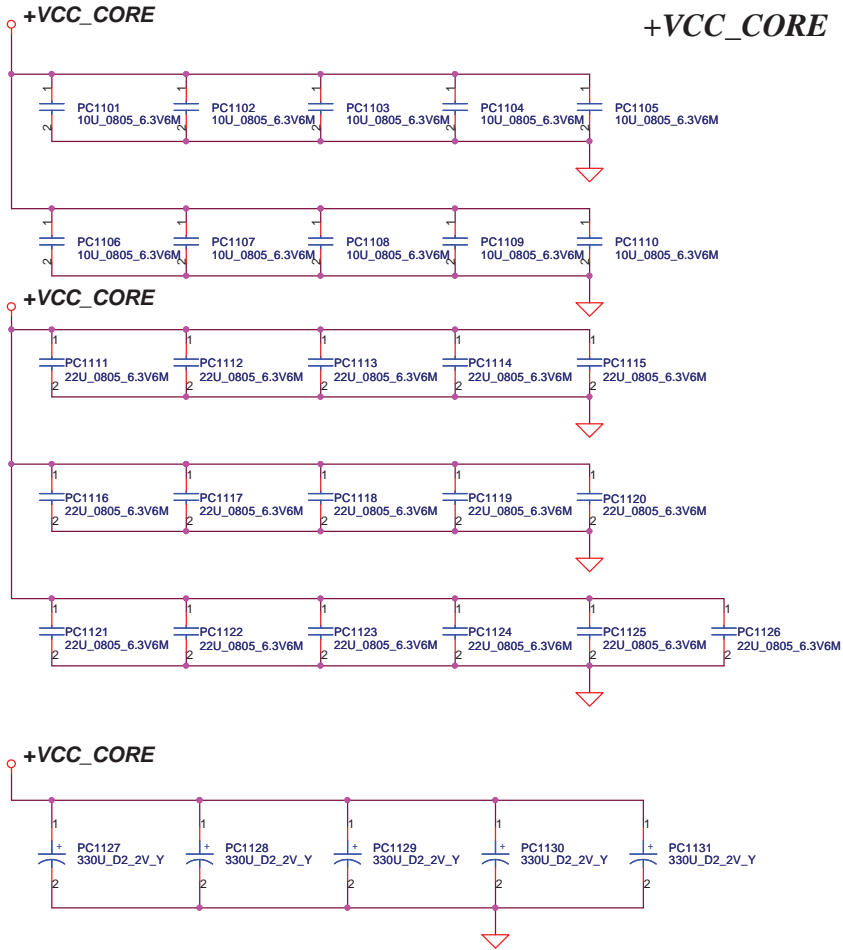
DC 35W CPU
 VID1=1.05V
 lccMax=53A
 lcc_Dyn=43A
 R_TDC=33A
 R_LL=1.9m ohm
 OCP=65A



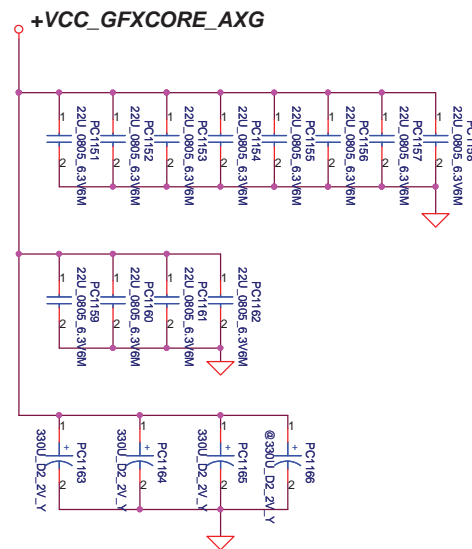
QC 45W GT2
 VID1=1.23V
 lccMax=46A
 lcc_Dyn=37A
 lcc_TDC=38A
 R_LL=3.9m ohm
 OCP=55A

DC 35W GT2
 VID1=1.23V
 lccMax=33A
 lcc_Dyn=20.2A
 lcc_TDC=21.5A
 R_LL=3.9m ohm
 OCP=40A

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Compal Electronics, Inc.			PWR-CPU CORE
PBL22 LA-7391P M/B			
Date	Wednesday, October 26, 2011	Sheet	52 of 58

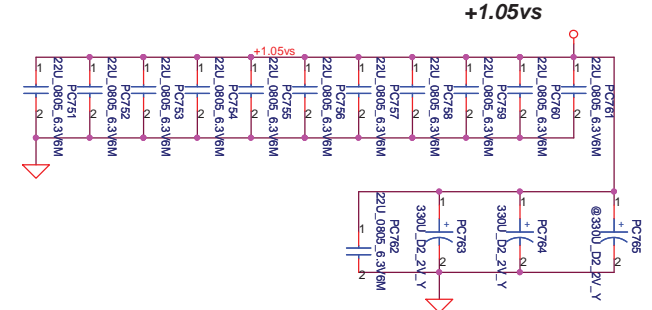


+VCC_GFXCORE_AXG



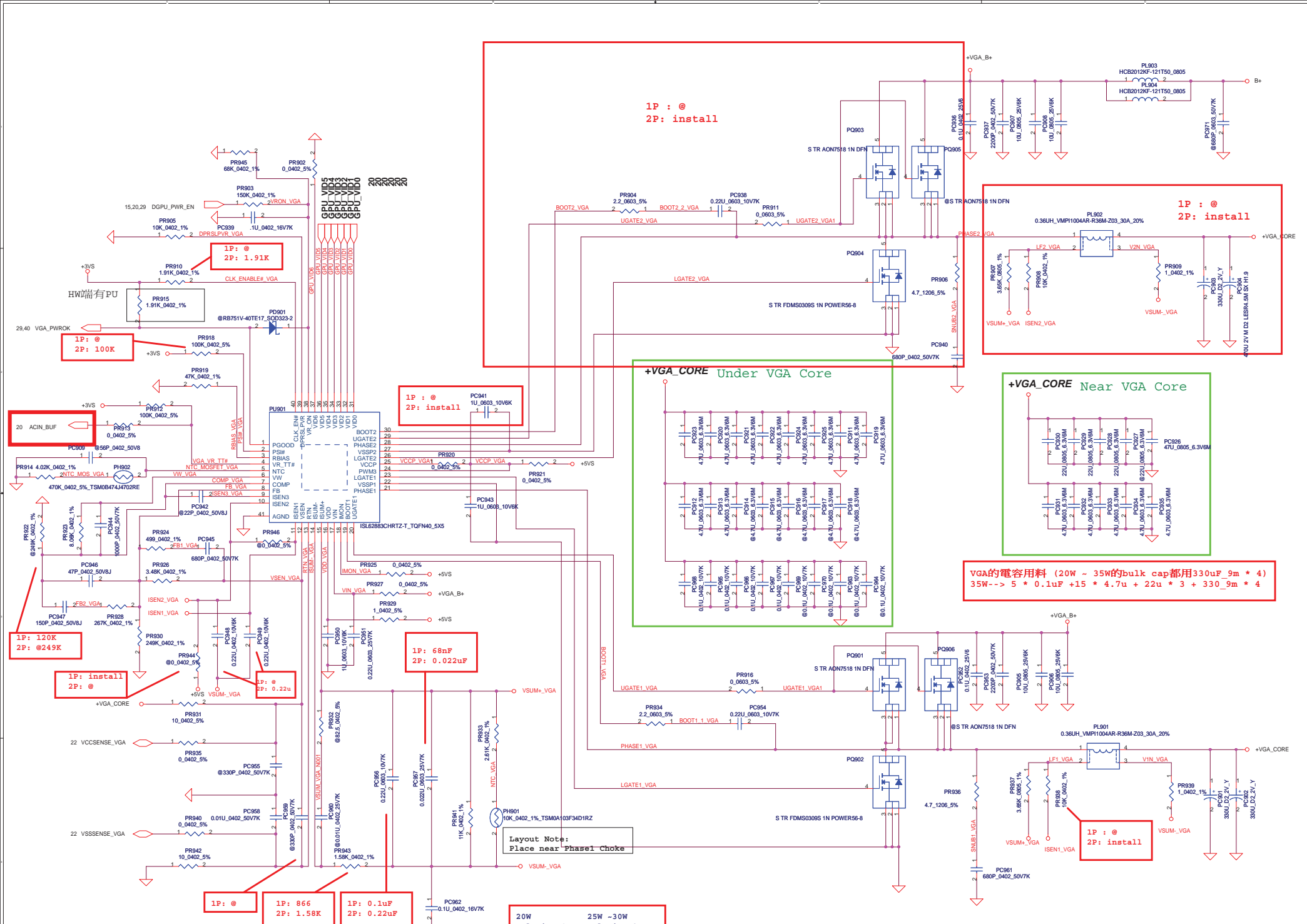
Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites



	330uF*9m	470uF*4.5m	22uF	10uF
Chief River				
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2012/12/31	Title PWR - PROCESSOR DECOUPLING	
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				Date	Wednesday, October 26, 2011



1P : @
2P: install

1P: @
2P: 1.91K

1P: @
2P: 100K

1P: @
2P: install

1P: 120K
2P: @249K

1P: install
2P: @

1P: @
2P: 0.22uF

1P: 68nF
2P: 0.022uF

1P: @

1P: 866
2P: 1.58K

1P: 0.1uF
2P: 0.22uF

20W solution: 1P
OCP: 38A

25W ~30W solution: 2P
OCP: 75A

Layout Note:
Place near Phase1 Choke

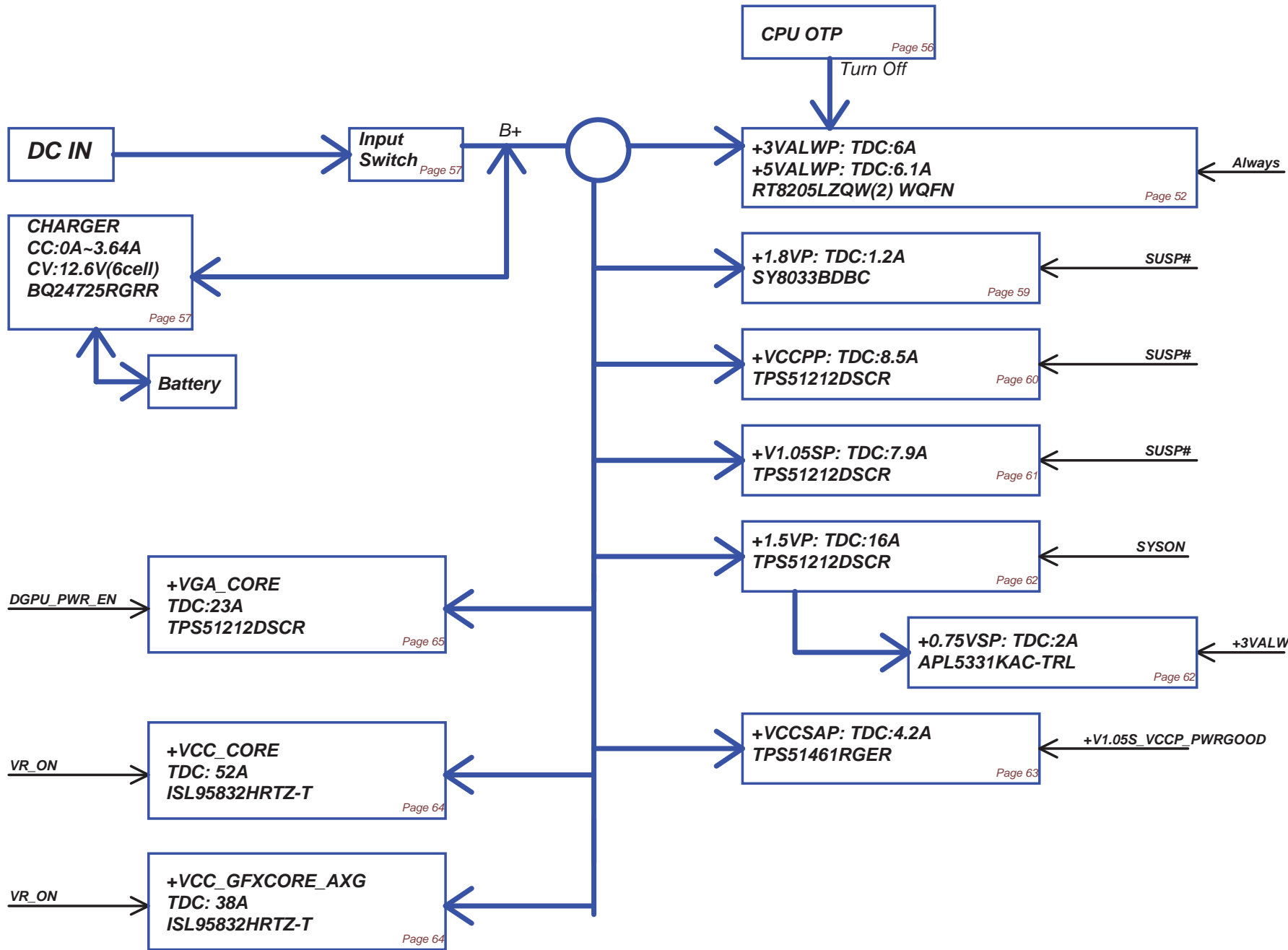
VGAの電容用料 (20W ~ 35Wのbulk cap都用330uF_9m * 4)
35W-> 5 * 0.1uF + 15 * 4.7u + 22u * 3 + 330_9m * 4

1P: @
2P: install

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Compal Electronics, Inc.
PWR - VGA COREP

Power block

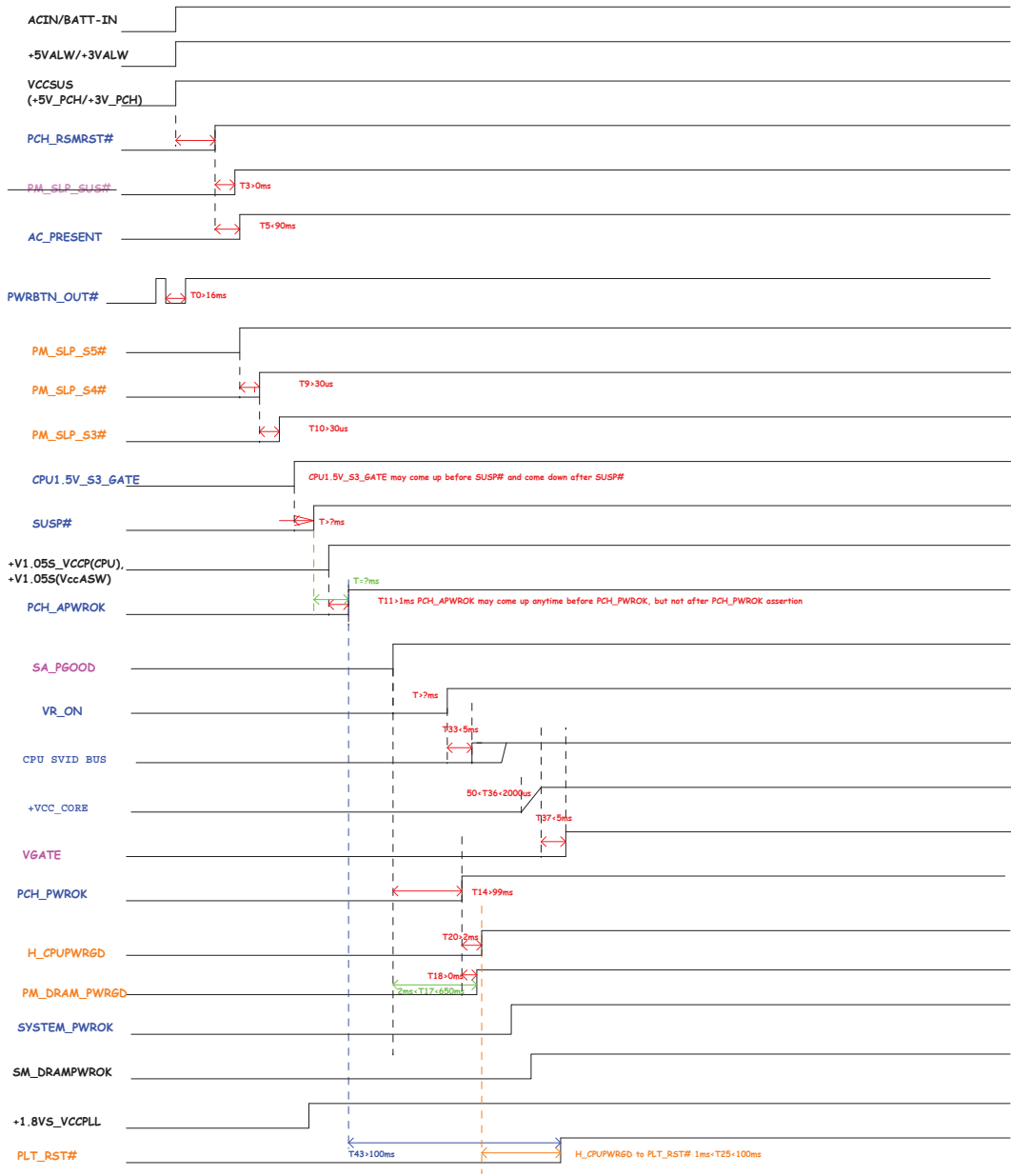


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				LA-8221P		0.2
				Date:	Wednesday, October 26, 2011	Sheet 55 of 58

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
<hr style="border-top: 1px dashed black;"/>							

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Issued Date	2008/09/15	Deciphered Date	2012/12/31	Size		Document Number	Rev
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				Date: Wednesday, October 26, 2011		Sheet 56 of 58	

Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER01		HW Design (TMDS_B_HPD)	0.2	14	Delete R205	09/21	
ER02		Add USB3.0(ASM1042) & non AI co-lay	0.2	36	Add ASM1042 co-lay	09/21	
ER03	+3VS Leakage	HW Design (SMBus leakage)	0.2	13	Delete Q3. (connect pin S & D) remove R135, R137	09/21	
ER04		Design change for card reader	0.2	40	Del R552, R556	09/21	
ER05		HW Design (PURC demand)	0.2	34	Add Q20, R773, R775 Reserve R768, R774. Change Net name at Card reader Conn	09/21	
ER06		HW Design (PURC demand)	0.2	29	Change to Q3(AO3404L) from U22(AO4430L)	09/21	
ER07		HW Design (PURC demand)	0.2	42	Change Q33 to AO3413L from AP2301GN	09/21	
ER08		Fine-tune GPU timing	0.2	29	Change R433 to 0 ohm un-stuff C396 Change R432 to 10K Change R435 to 200 ohm	09/21	
ER09	KB connector reverse	HW Design (reserve)	0.2	18	Reserve R290	09/21	
ER10		HW Design (change)	0.2	39	Reverse JKB1 connector	09/30	
ER11		HW Design	0.2	40	Del Y5 , C545 , C546	09/30	
ER12		HW Design (PURC demand)	0.2	15	Del R229, R230 (10K) Add R776-R783 (10K) Del R237, R239, R242 (8.2K) Add R784-R793 (8.2K)	09/30	
ER13		HW Design (PURC demand)	0.2	29, 31 10, 11	Change P/N C387, C389, C399, C436, C447, C602 Change C915, C518, C526. (0402) Change P/N C99, C109, C118, C120, C140, C141. (0402)	10/03	
ER14		HW Design (XTAL fine-tune)	0.2	42, 12 13, 32 20, 36	Change R607 to 10 ohm Change Y3, C241, C242. Change Y1, C144, C145 Change Y4, C469, C473. Change Y2, C163, C164 Change Y9	10/07	
ER15		HW Design for instant on function	0.2	13 5	Reserve R750 R576 pin2 change to +3V_PCH from +3VS Change R576 to 0	10/07	
ER16		HW Design (power jumper change to +3VL)	0.2	38 40	jumper PJP302 (change +3VLP to +3VL @P38, P40)	10/07	
ER17		HW Design (PURC demand)	0.2		Change P/N Q7, U20, U21. Change P/N Q14-Q19, Q25, Q27-Q29, Q32, Q34-Q37, Q40-Q43, Q46-Q51, Q55-Q57, Q60, Q61, Q902, Q903, Q905. Change P/N Q23	10/14	
ER18		EMI solution	0.2	5	Add R684 to 0 (H_CPUPWRGD)	10/14	
ER19		Refer to ORB design	0.2	14	un-stuff D2, Add R751 un-stuff D32, R547, Add R752 Assign U33.18 to AC_PRESENT signal.	10/14	
ER20		change for GPU H/W strapping STRAP1 to PL 45K ohm to enhanced the PCIe PEG driving.	0.2	22	Change R349 from 34.8K to 45.3K	10/14	
ER21		modify parts for Intel review feedback message.	0.2	09 18 17 14 15	Add R242 Add C149 0.1uF Del L6, Add R289 , un-stuff C212 Del L4, Add R387 Add R230 Stuff R244	10/14	
ER21		Modify H2 size	0.2	38	Modify H2 size	10/17	

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				EE-PIR-1
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER22		Refer to Intel review feedback item 45.	0.2	16	Add R807	10/19	
ER23		Reserve for Deep Sx	0.2	14, 16 40	Add unstuff R800, R801, R802, R803, R804, R805 Add PCH_DPWROK, DS_WAKE#, SUSACK#, SUSWARN#	10/19	
ER24		Reserve for ROM protect	0.2	40	Add unstuff R806	10/19	
ER25		For Instant On function control by EC	0.2	06	Stuff R44, Unstuff R43	10/19	
ER26		For EMI request	0.2	36	Reserve R1082 , C1045	10/19	
ER27		For LED issue	0.2	39	change LED3 footprint to LED_HT-210UD-UYG_3P	10/20	
ER28		For PRUC request	0.2	38 39	Change SW3, SW4, SW5 P/N	10/20	
ER29		For PRUC request	0.2	39	Change U36 P/N	10/20	
ER30		For EMI request (without MS_CLK)	0.2	34	Remove R637, C611, R631, C620.	10/20	
ER31		dGPU thermal throttling.	0.2	20 40	Add R428, Revise U11 I/O signal. Un-stuff R730.	10/20	
ER32		SPI flash data crisis prevention.	0.2	12 40	Add Q63, R135, R137. Change U33.41 net to EC_SPI_WP. remove R806.	10/20	
ER33		Power switch EOS issue prevention.	0.2	37	Change C510, C516, C519 to 0.22uF/16V.	10/20	
ER34		For EMI request	0.2	32 35	Change R485 , R486 to 0.1uF Reserve C641-C648	10/20	
ER35		For ESD request	0.2	37, 35 30, 39	Change D27, D29, D24, D25. Change D6, D7, D9, D10, D33, D34.	10/20	
ER36		Modify X76 table (N13P-GS)	0.2	22	update X76 table (Strap1, Strap2, Strap3)	10/24	
ER37		Modify X76 table (N13P-GS & N13M-GE1 x8)	0.2	3	update X76 table (add ZZZ9 -ZZZ12 for N13P-GS & N13M-GE1 x8) & update P/N	10/25	
ER38		Modify PCH_SPI_WP# singal control by EC	0.2	12	Stuff R135	10/26	

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