

MODEL NAME: *NAP00*  
PCB NAME: *LA-5811P MB*  
COMPAL P/N: *DAA00001P00*

# Compal confidential

## Schematics Document

Intel CULV (SFF)

Penryn + Cantiga + ICH9-M

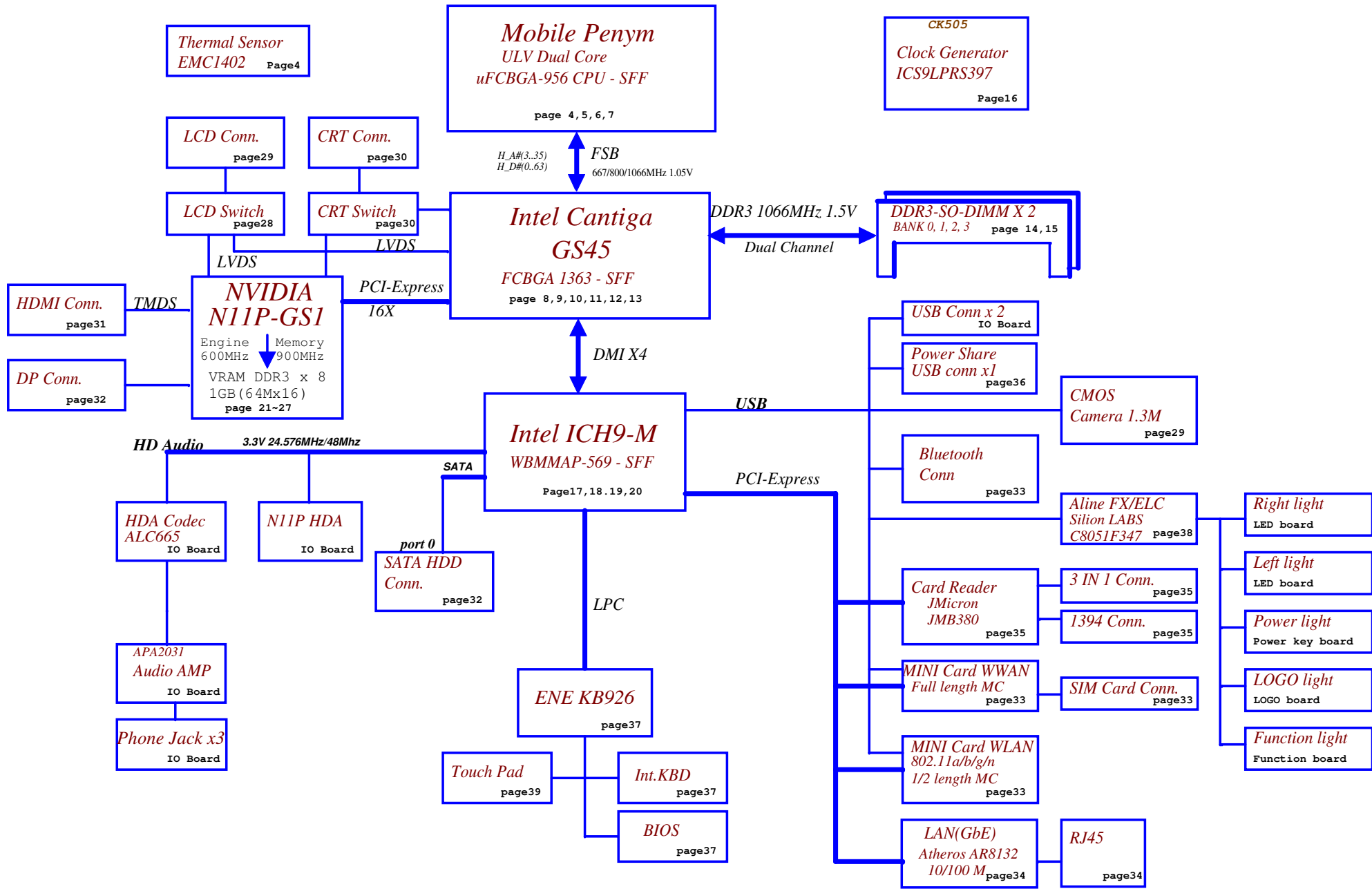
DISCRETE VGA N11P-GS1 (Switchable Graphics)

2009-12-16

Rev: 1.0

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# ULV

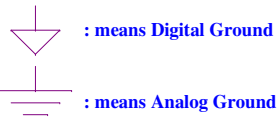


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**Voltage Rails** ( O MEANS ON X MEANS OFF )

power plane State	B+	+5VALW +3VALW VL	+1.8V +1.5V	+5VS +3VS +0.75VS +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

**Symbol Note :**



@ : means just reserve , no build  
 CONN@ : means ME part.  
 45@ : means install after SMT.

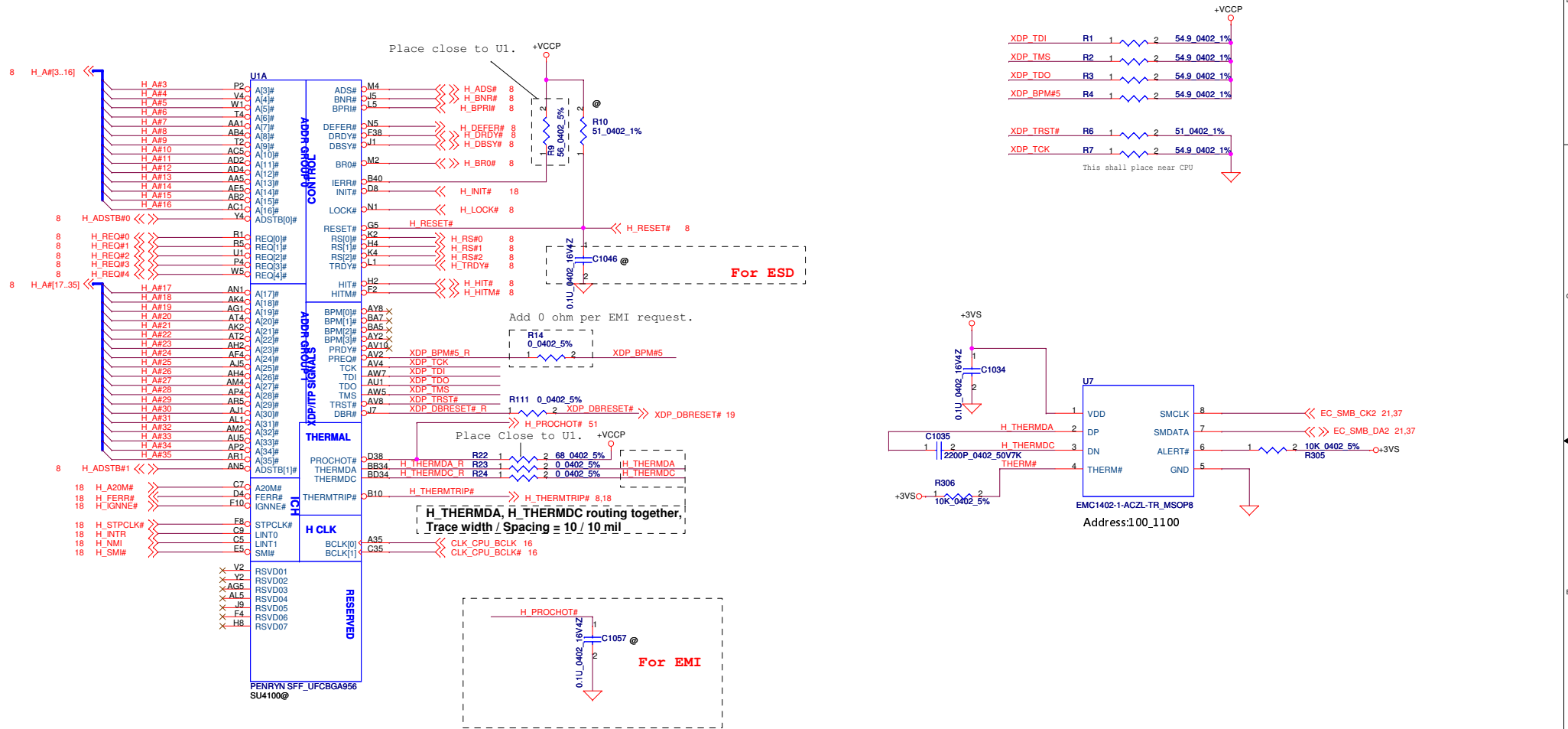
**I2C / SMBUS ADDRESSING**

DEVICE	HEX	ADDRESS
EC_SMB_CK1 EC_SMB_DA1 Battery		
EC_SMB_CK2 EC_SMB_DA2 CPU THERMAL SENSOR (EMC1402-1-ACZL)	4C	01001100
GPU THERMAL SENSOR (ADM1032ARMZ)	4D	01001101
GPU INTERNAL THERMAL SENSOR	9E	10011110
ICH_SMBCLK ICH_SMBDATA CLOCK GENERATOR (EXT.)	D2	11010010
Free Fall Sensor	38	00111000

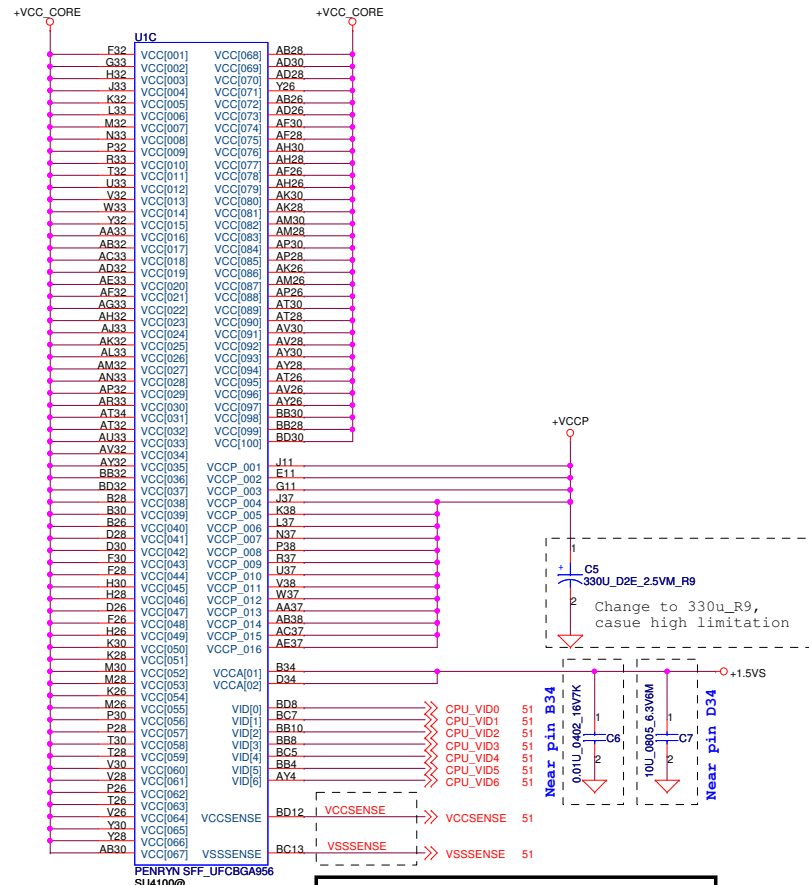
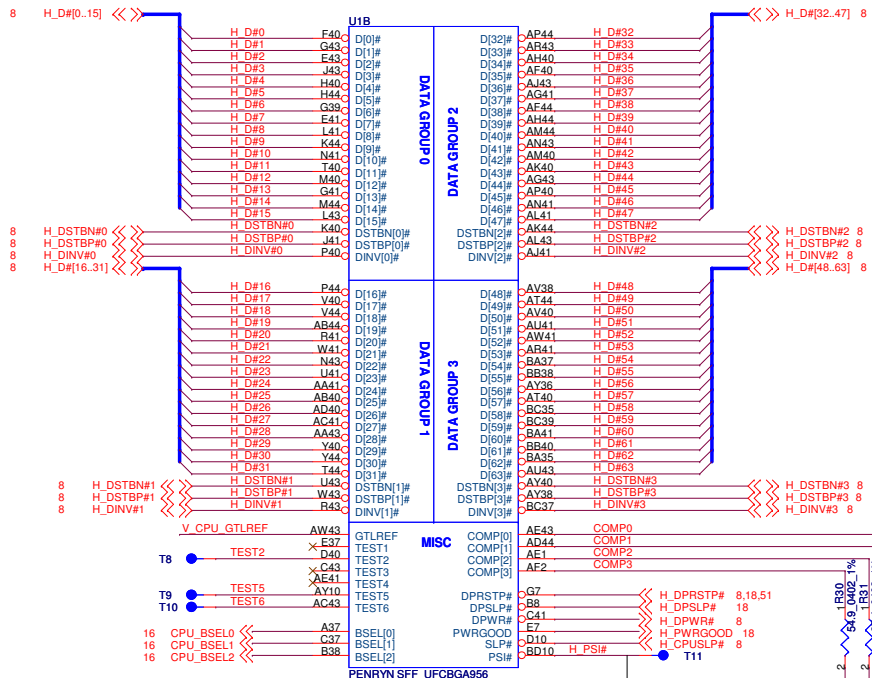
**Compal R1 PN**

CPU-->SA00003I91L(S IC AV80577UG0132M SLGS4 R0 1.3G FCBGA)----->SU4100  
 CPU-->SA00003IA1L(S IC AV80577UG0133M SLGS6 R0 1.3G FCBGA)----->SU7300  
 NB-->SA00002RQ1L(S IC AC82GS45 SLB92 B3 FCBGA 1363)----->45180131L03,45180131L04  
 SB-->SA00001YC4L(S IC AM82801IUX SLB8N A FCBGA 569P ICH9M)--->45180131L03,45180131L04  
 VRAM-->SA00003240L(S IC D3 64M16 H5TQ1G63BFR-12C FBGA 96P)-->45180131L03,45180131L04  
 VRAM-->SA00003570L(S IC D3 64M16 K4W1G1646E-HC12 FBGA 96P)-->45180131L03,45180131L04  
 Compal R3 PN  
 CPU-->SA00003I92L(S IC AV80577UG0132M SLGS4 R0 1.3G A31!)----->SU4100  
 CPU-->SA00003IA2L( S IC AV80577UG0133ML SLGYV R0 1.3G A31!)----->SU7300  
 NB-->SA00002RQ0L(S IC AC82GS45 SLB92 B3 FCBGA 1363 A31 !)->45180131L01,45180131L02  
 SB-->SA00001YC3L(S IC AM82801IUX SLB8N A FCBGA ICH9M A31 !)->45180131L01,45180131L02  
 VRAM-->SA00003241L(S IC D3 64M16 H5TQ1G63BFR-12C FBGA A31!)->45180131L01,45180131L02  
 VRAM-->SA00003571L(S IC D3 64M16 K4W1G1646E-HC12 FBGA A31!)->45180131L01,45180131L02

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				Penryn(1/4)-AGTLA/ITP-XDP	
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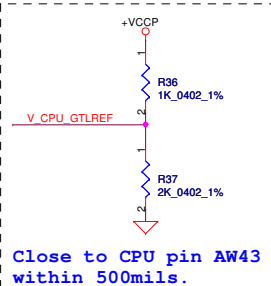
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

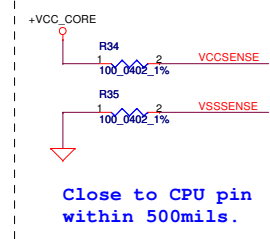
Cause CPU core power change to 1 phase, and not need support the pin, leave it as TP. 10/02

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

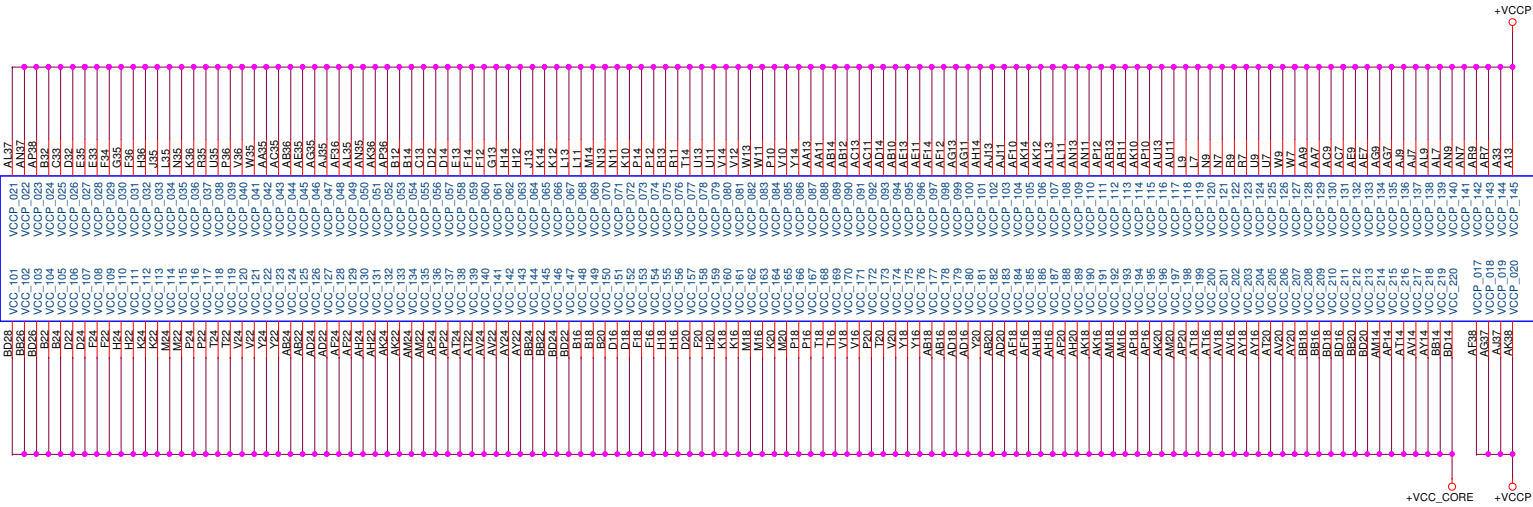
Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin AW43 within 500mils.



Close to CPU pin within 500mils.



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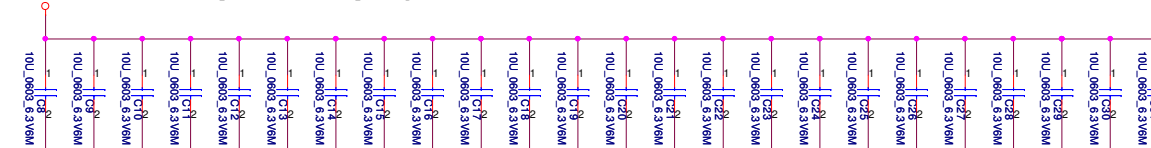
UID		
B42	VSS001	VSS082
F44	VSS002	VSS083
D44	VSS003	VSS084
F42	VSS004	VSS085
H42	VSS005	VSS086
K42	VSS006	VSS087
M42	VSS007	VSS088
P42	VSS008	VSS089
T42	VSS009	VSS090
Y42	VSS010	VSS091
AA2	VSS011	VSS092
AB42	VSS012	VSS093
AD42	VSS013	VSS094
AE42	VSS014	VSS095
AH42	VSS015	VSS096
AK42	VSS016	VSS097
AM42	VSS018	VSS099
AY44	VSS019	VSS100
AV44	VSS020	VSS101
AX42	VSS021	VSS102
AT42	VSS022	VSS103
AV42	VSS023	VSS104
AA42	VSS024	VSS105
BB42	VSS026	VSS107
CA2	VSS027	VSS108
G37	VSS028	VSS109
H38	VSS029	VSS110
L39	VSS030	VSS111
M38	VSS031	VSS112
N39	VSS032	VSS113
R39	VSS033	VSS114
T38	VSS034	VSS115
U39	VSS035	VSS116
W39	VSS036	VSS117
Y38	VSS037	VSS118
AA39	VSS038	VSS119
AC39	VSS039	VSS120
AD38	VSS040	VSS121
AE39	VSS041	VSS122
AG39	VSS042	VSS123
AH38	VSS043	VSS124
AI39	VSS044	VSS125
AL39	VSS045	VSS126
AM38	VSS046	VSS127
AN39	VSS047	VSS128
AR37	VSS048	VSS129
AT38	VSS049	VSS130
AW39	VSS050	VSS131
AX39	VSS051	VSS132
AY37	VSS052	VSS133
BA39	VSS053	VSS134
BC41	VSS054	VSS135
BD40	VSS055	VSS136
BE40	VSS056	VSS137
BF40	VSS057	VSS138
BG40	VSS058	VSS139
BH40	VSS059	VSS140
BI40	VSS060	VSS141
BJ40	VSS061	VSS142
BK40	VSS062	VSS143
BL40	VSS063	VSS144
BM40	VSS064	VSS145
BN40	VSS065	VSS146
BP40	VSS066	VSS147
BQ40	VSS067	VSS148
BR40	VSS068	VSS149
BS40	VSS069	VSS150
BT40	VSS070	VSS151
BV40	VSS071	VSS152
BW40	VSS072	VSS153
BY40	VSS073	VSS154
CA40	VSS074	VSS155
CB40	VSS075	VSS156
CC40	VSS076	VSS157
CD40	VSS077	VSS158
CE40	VSS078	VSS159
CF40	VSS079	VSS160
CG40	VSS080	VSS161
CH40	VSS081	VSS162
CI40	VSS082	VSS163

PENRYN SFF\_UFCBGA956  
SU4100@

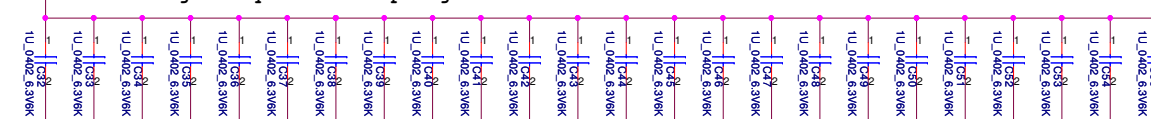
UIE		
G25	VSS_164	VSS_280
AR35	VSS_165	VSS_281
G21	VSS_166	VSS_282
J25	VSS_167	VSS_283
AW35	VSS_168	VSS_284
J23	VSS_169	VSS_285
L21	VSS_170	VSS_286
L25	VSS_171	VSS_287
N25	VSS_172	VSS_288
NO3	VSS_173	VSS_289
N21	VSS_174	VSS_290
R25	VSS_175	VSS_291
R23	VSS_176	VSS_292
U25	VSS_177	VSS_293
U23	VSS_178	VSS_294
E29	VSS_179	VSS_295
E27	VSS_180	VSS_296
W25	VSS_181	VSS_297
W23	VSS_182	VSS_298
W21	VSS_183	VSS_299
W19	VSS_184	VSS_300
AA25	VSS_185	VSS_301
AA23	VSS_186	VSS_302
AA21	VSS_187	VSS_303
AC25	VSS_188	VSS_304
AC23	VSS_189	VSS_305
AC21	VSS_190	VSS_306
AE25	VSS_191	VSS_307
AE23	VSS_192	VSS_308
AE21	VSS_193	VSS_309
AG25	VSS_194	VSS_310
AG23	VSS_195	VSS_311
AG21	VSS_196	VSS_312
AJ25	VSS_197	VSS_313
AJ23	VSS_198	VSS_314
AJ21	VSS_199	VSS_315
AL25	VSS_200	VSS_316
AL23	VSS_201	VSS_317
AL21	VSS_202	VSS_318
AN25	VSS_203	VSS_319
AN23	VSS_204	VSS_320
AN21	VSS_205	VSS_321
AR25	VSS_206	VSS_322
AR23	VSS_207	VSS_323
AR21	VSS_208	VSS_324
AU25	VSS_209	VSS_325
AU23	VSS_210	VSS_326
AU21	VSS_211	VSS_327
AW25	VSS_212	VSS_328
AW23	VSS_213	VSS_329
AW21	VSS_214	VSS_330
BA25	VSS_215	VSS_331
BA23	VSS_216	VSS_332
BA21	VSS_217	VSS_333
BC25	VSS_218	VSS_334
BC23	VSS_219	VSS_335
BC21	VSS_220	VSS_336
C17	VSS_221	VSS_337
C19	VSS_222	VSS_338
F19	VSS_223	VSS_339
F17	VSS_224	VSS_340
G19	VSS_225	VSS_341
G17	VSS_226	VSS_342
J19	VSS_227	VSS_343
J17	VSS_228	VSS_344
L19	VSS_229	VSS_345
L17	VSS_230	VSS_346
N19	VSS_231	VSS_347
N17	VSS_232	VSS_348
R19	VSS_233	VSS_349
R17	VSS_234	VSS_350
U19	VSS_235	VSS_351
U17	VSS_236	VSS_352
W19	VSS_237	VSS_353
W17	VSS_238	VSS_354
AA19	VSS_239	VSS_355
AA17	VSS_240	VSS_356
AC19	VSS_241	VSS_357
AC17	VSS_242	VSS_358
AE19	VSS_243	VSS_359
AE17	VSS_244	VSS_360
AG19	VSS_245	VSS_361
AG17	VSS_246	VSS_362
AJ19	VSS_247	VSS_363
AJ17	VSS_248	VSS_364
AL19	VSS_249	VSS_365
AL17	VSS_250	VSS_366
AN19	VSS_251	VSS_367
AN17	VSS_252	VSS_368
AR19	VSS_253	VSS_369
AR17	VSS_254	VSS_370
AU19	VSS_255	VSS_371
AU17	VSS_256	VSS_372
AW19	VSS_257	VSS_373
AW17	VSS_258	VSS_374
BA19	VSS_259	VSS_375
BA17	VSS_260	VSS_376
BC19	VSS_261	VSS_377
BC17	VSS_262	VSS_378
C11	VSS_263	VSS_379
C15	VSS_264	VSS_380
E15	VSS_265	VSS_381
H10	VSS_266	VSS_382
M12	VSS_267	VSS_383
G15	VSS_268	VSS_384
L15	VSS_269	VSS_385
L15	VSS_270	VSS_386
N15	VSS_271	VSS_387
M10	VSS_272	VSS_388
T12	VSS_273	VSS_389
R15	VSS_274	VSS_390
U15	VSS_275	VSS_391
W15	VSS_276	VSS_392
T10	VSS_277	VSS_393
Y12	VSS_278	VSS_394
AD12	VSS_279	VSS_395

PENRYN SFF\_UFCBGA956  
SU4100@

### Mid Frequency Decoupling



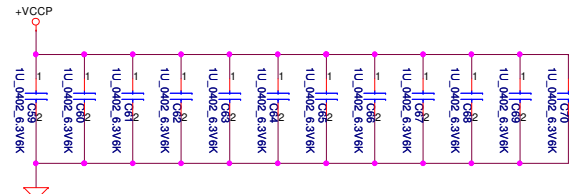
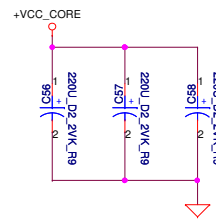
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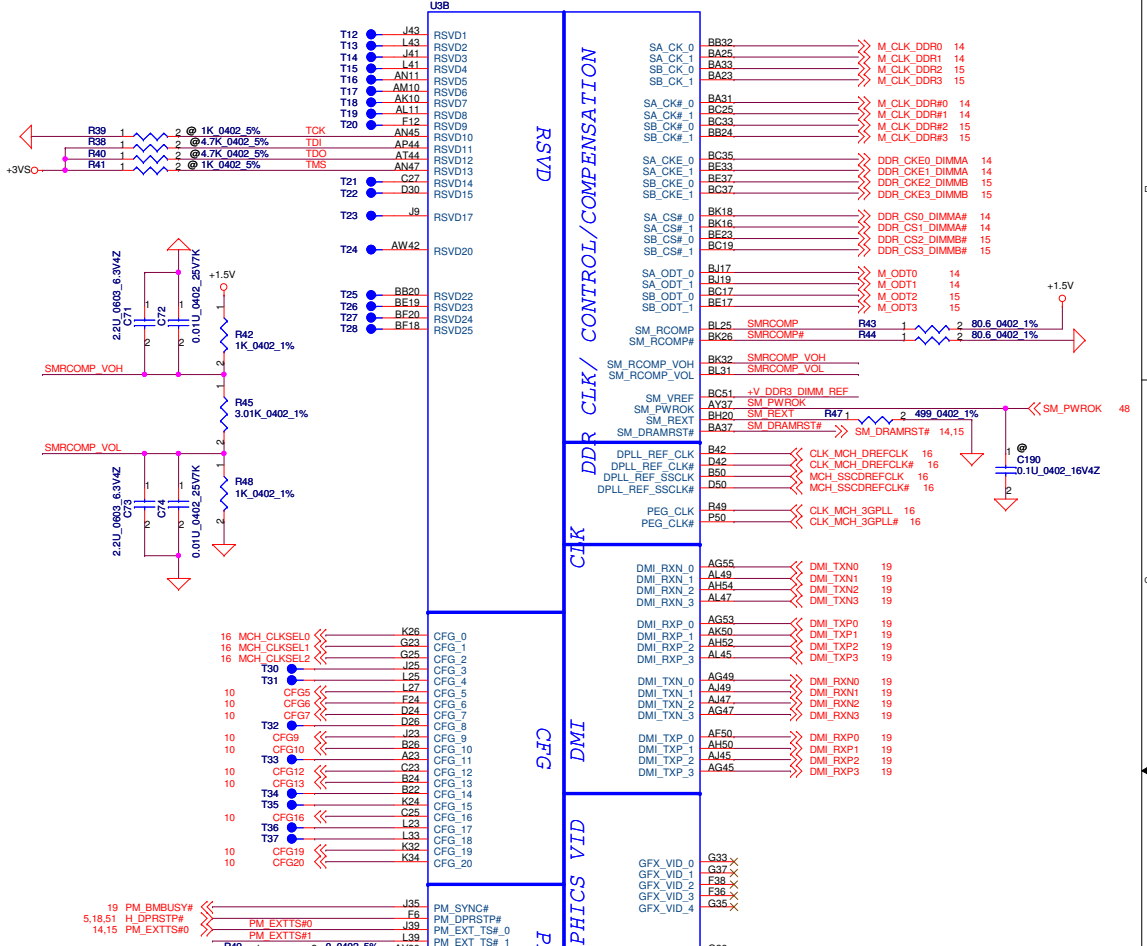
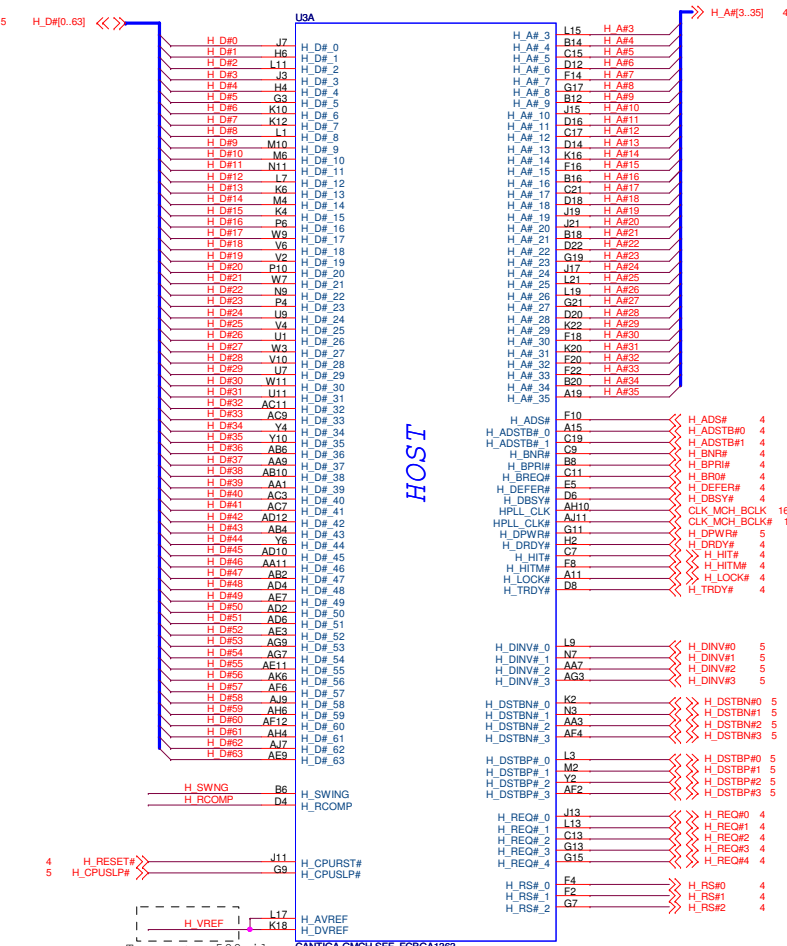
6/14 :Replace 12pcs 10uF\_0805 to 24 pcs 1uF\_0402 for CPU transient fail issue.

### ESR <= 9m ohm (For CPU)

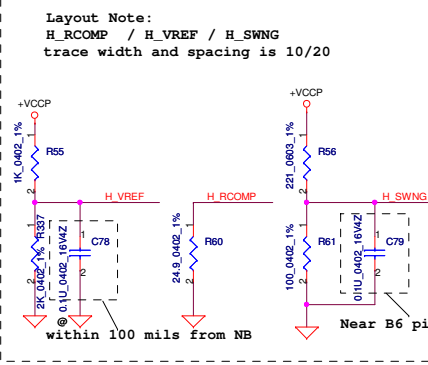
#### Near CPU CORE regulator



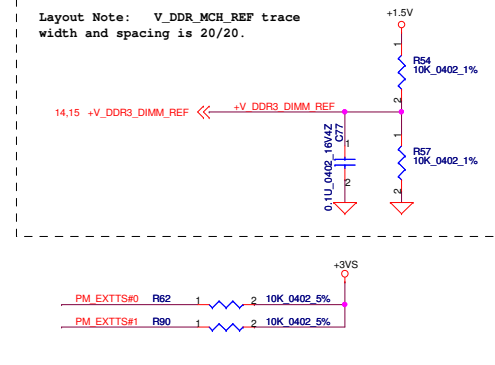
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layout note:  
Route H\_SCOMP and H\_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

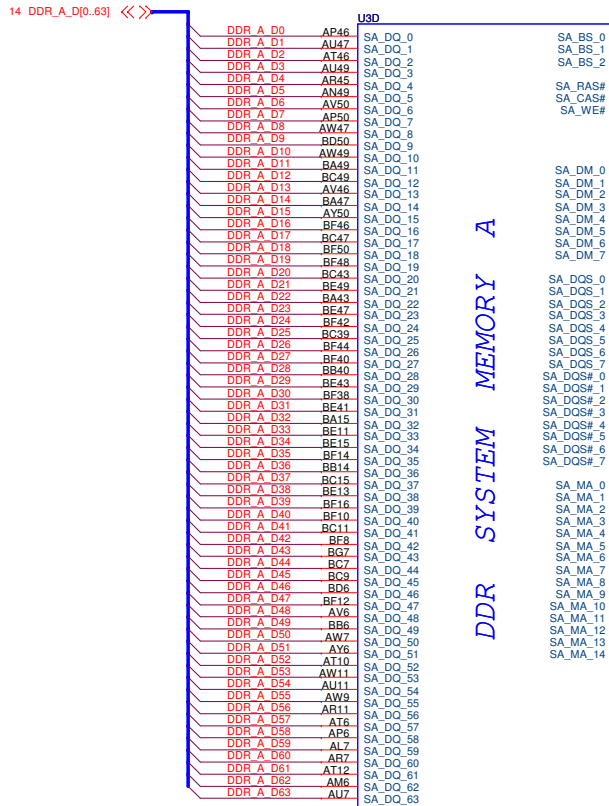


layout note:  
Place them close to U4 pin BC51.

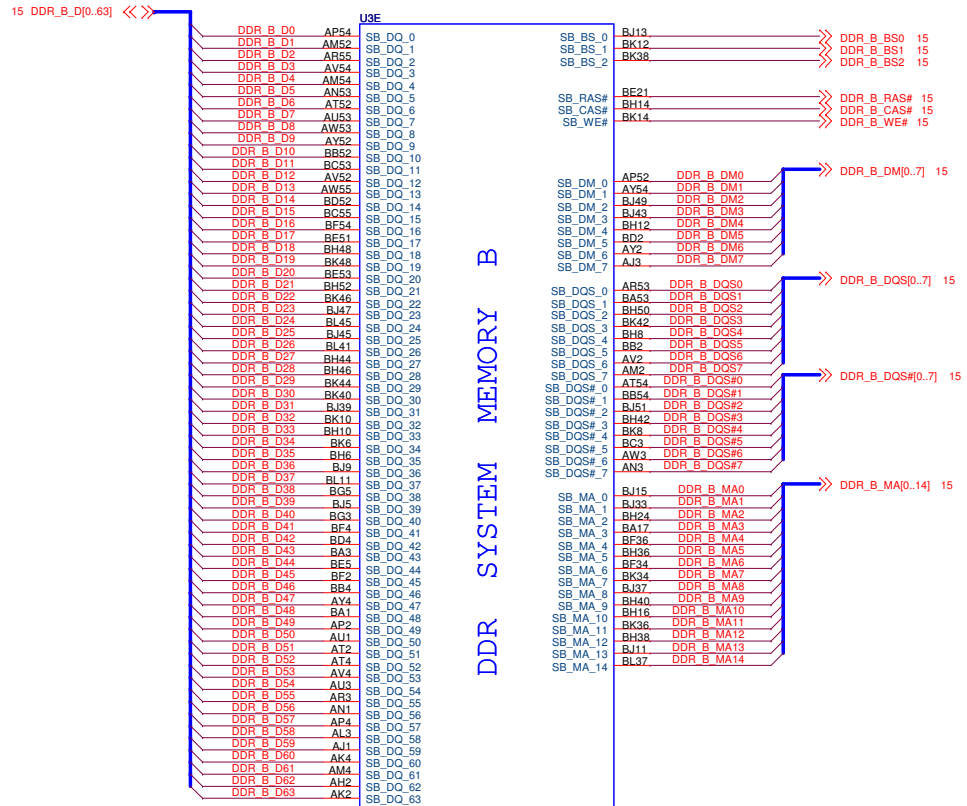


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CANTIGA GMCH SFF\_FCBGA1363



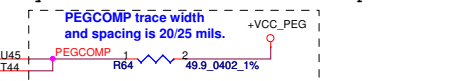
CANTIGA GMCH SFF\_FCBGA1363

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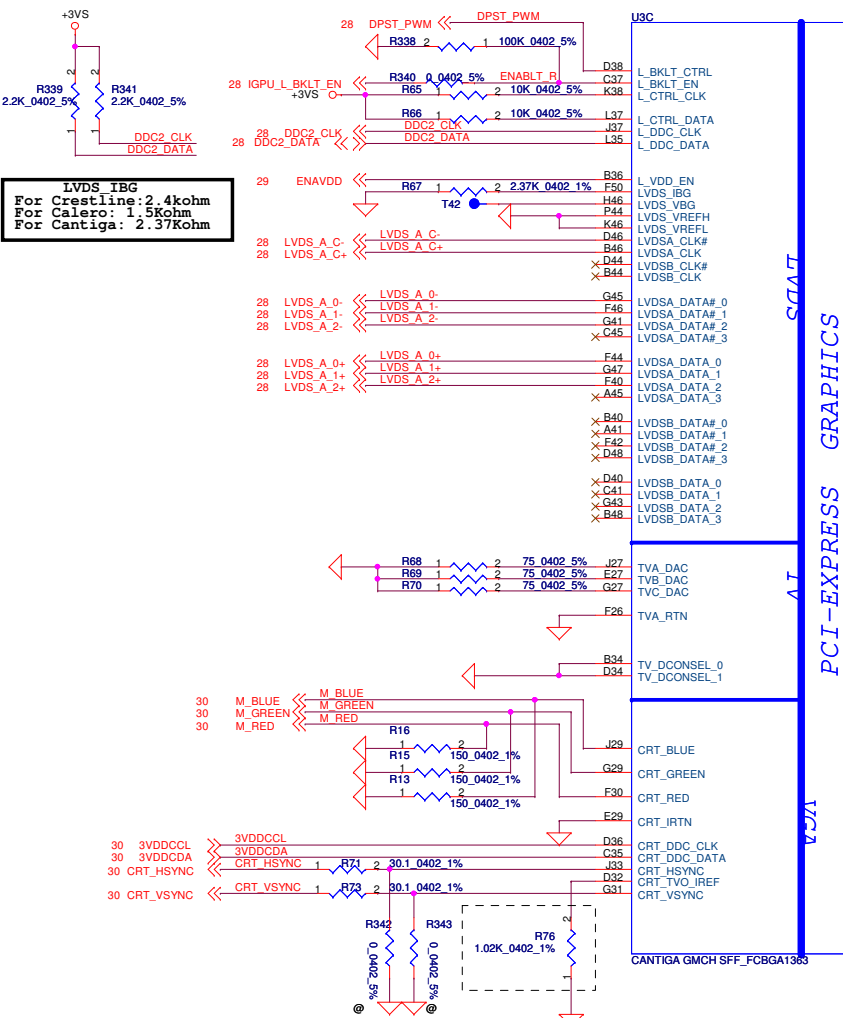
**Strap Pin Table**

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable 1 = The ITPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0=(TLS)chiper suite with no confidentiality 1=(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

layout note:Place R64 <500mils to U4 pin U45&T44.

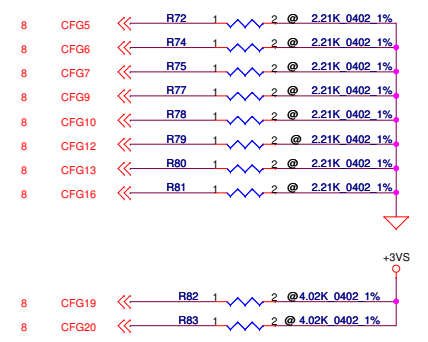


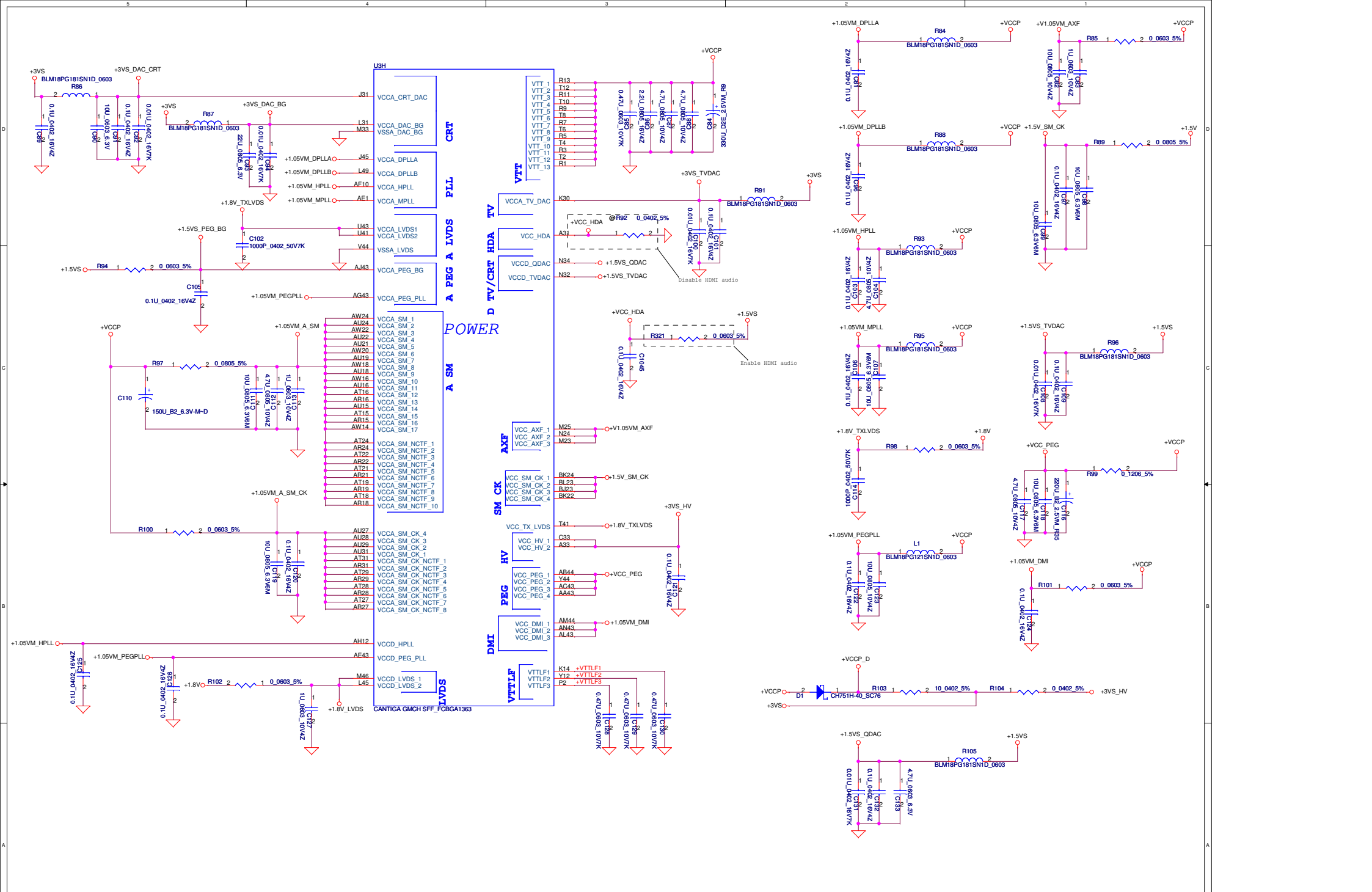
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PEG_RX#_1	G49	PCIE GTX_C_MRX_N1 21
PEG_RX#_2	K54	PCIE GTX_C_MRX_N2 21
PEG_RX#_3	J50	PCIE GTX_C_MRX_N3 21
PEG_RX#_4	N49	PCIE GTX_C_MRX_N4 21
PEG_RX#_5	M52	PCIE GTX_C_MRX_N5 21
PEG_RX#_6	P54	PCIE GTX_C_MRX_N6 21
PEG_RX#_7	V46	PCIE GTX_C_MRX_N7 21
PEG_RX#_8	S50	PCIE GTX_C_MRX_N8 21
PEG_RX#_9	V52	PCIE GTX_C_MRX_N9 21
PEG_RX#_10	W49	PCIE GTX_C_MRX_N10 21
PEG_RX#_11	AB84	PCIE GTX_C_MRX_N11 21
PEG_RX#_12	AC55	PCIE GTX_C_MRX_N12 21
PEG_RX#_13	AE49	PCIE GTX_C_MRX_N13 21
PEG_RX#_14	AF54	PCIE GTX_C_MRX_N14 21
PEG_RX#_15	AF54	PCIE GTX_C_MRX_N15 21
PEG_RX#_0	E51	PCIE GTX_C_MRX_P0 21
PEG_RX#_1	F48	PCIE GTX_C_MRX_P1 21
PEG_RX#_2	J55	PCIE GTX_C_MRX_P2 21
PEG_RX#_3	J49	PCIE GTX_C_MRX_P3 21
PEG_RX#_4	M54	PCIE GTX_C_MRX_P4 21
PEG_RX#_5	M50	PCIE GTX_C_MRX_P5 21
PEG_RX#_6	P52	PCIE GTX_C_MRX_P6 21
PEG_RX#_7	U47	PCIE GTX_C_MRX_P7 21
PEG_RX#_8	V54	PCIE GTX_C_MRX_P8 21
PEG_RX#_9	V50	PCIE GTX_C_MRX_P9 21
PEG_RX#_10	V50	PCIE GTX_C_MRX_P10 21
PEG_RX#_11	AB82	PCIE GTX_C_MRX_P11 21
PEG_RX#_12	AC33	PCIE GTX_C_MRX_P12 21
PEG_RX#_13	AC53	PCIE GTX_C_MRX_P13 21
PEG_RX#_14	AD50	PCIE GTX_C_MRX_P14 21
PEG_RX#_15	AF52	PCIE GTX_C_MRX_P15 21
PEG_TX#_0	L47	PEG_TXN0 C1073 1 2 0.1U 0402 16V7K
PEG_TX#_1	F52	PEG_TXN1 C1074 1 2 0.1U 0402 16V7K
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PEG_TX#_3	J54	PEG_TXN3 C1076 1 2 0.1U 0402 16V7K
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PEG_TX#_8	W47	PEG_TXP8 C1098 1 2 0.1U 0402 16V7K
PEG_TX#_9	AA47	PEG_TXP9 C1099 1 2 0.1U 0402 16V7K
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PEG_TX#_12	AB50	PEG_TXP12 C1102 1 2 0.1U 0402 16V7K
PEG_TX#_13	AE47	PEG_TXP13 C1103 1 2 0.1U 0402 16V7K
PEG_TX#_14	AD52	PEG_TXP14 C1104 1 2 0.1U 0402 16V7K
PEG_TX#_15	AD52	PEG_TXP15 C1104 1 2 0.1U 0402 16V7K



LVDS IBG  
For Crestline: 2.4kohm  
For Calero: 1.5kohm  
For Cantiga: 2.37kohm

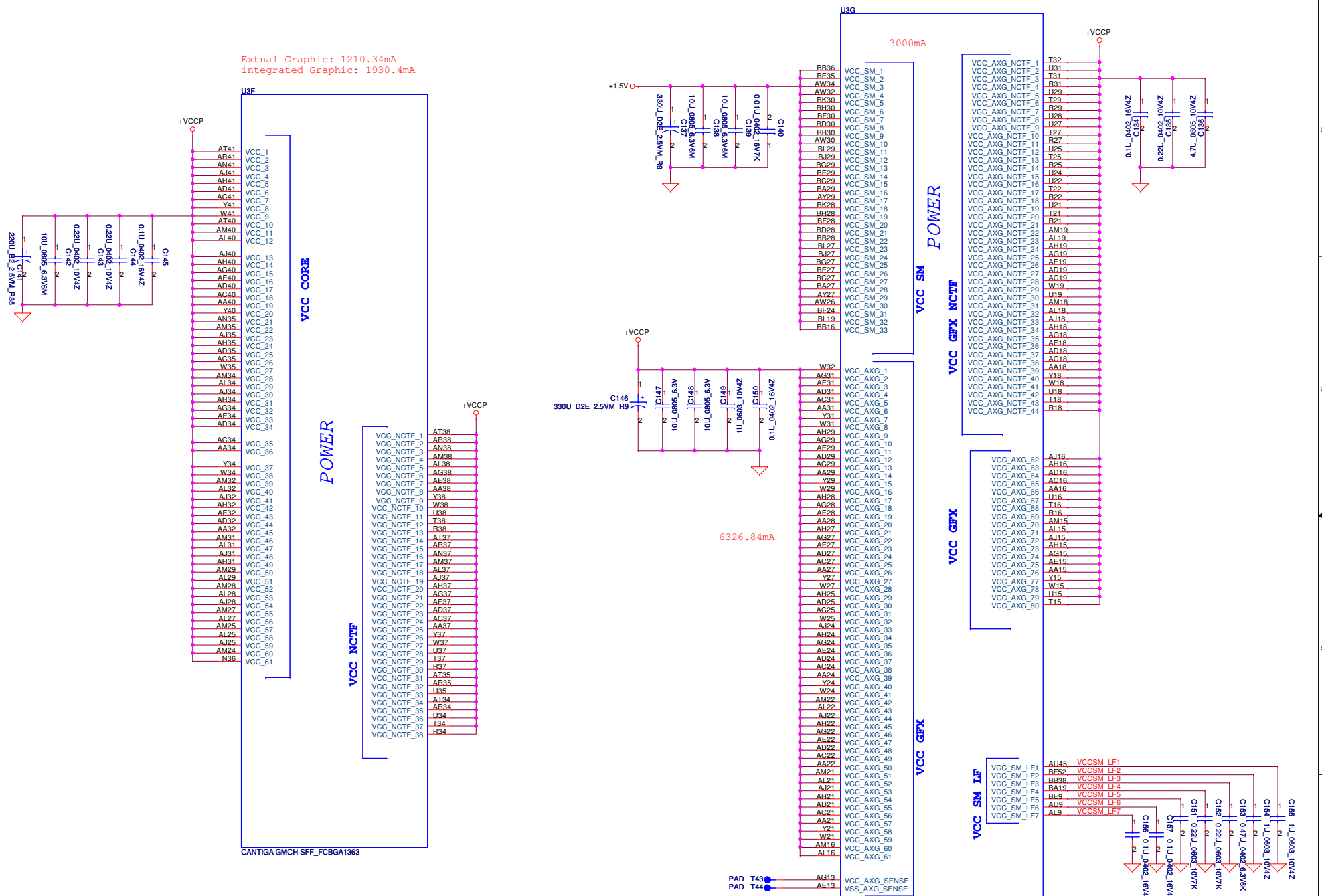
Close to pin D32 and keep 30mil space to other part/trace.





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				LA-5811P	1.0
				Date: Tuesday, December 29, 2009	Sheet 11 of 58

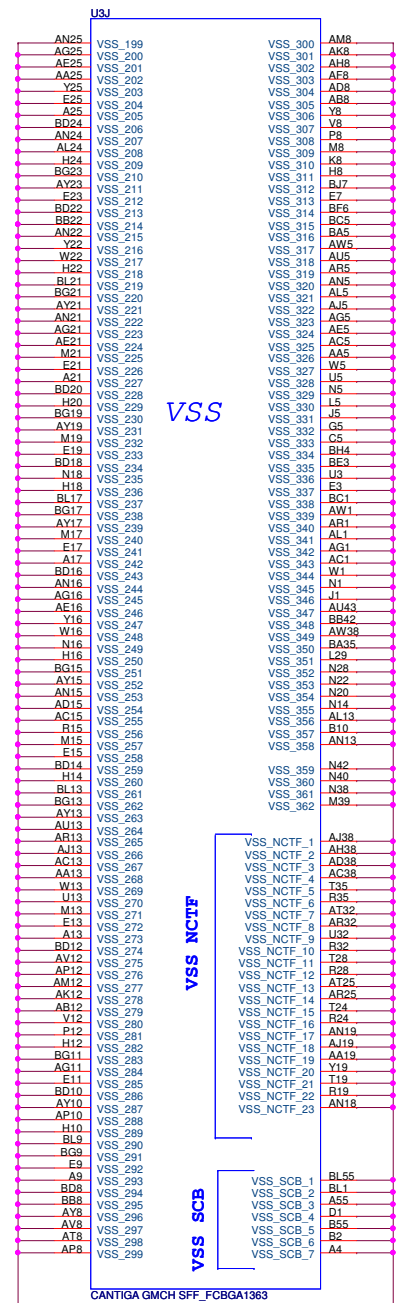
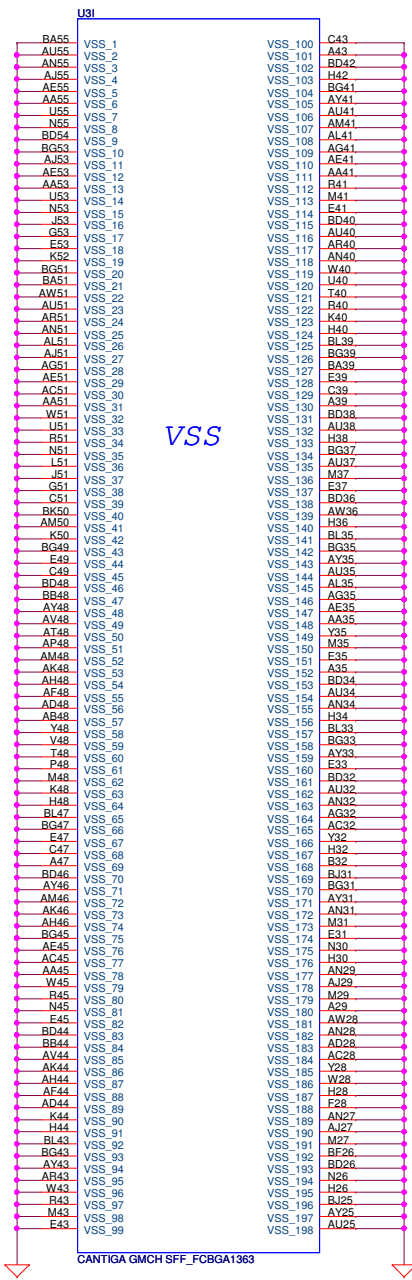
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 Integrated Graphic: 1930.4mA



CANTIGA GMCH SFF\_FCBGA1363

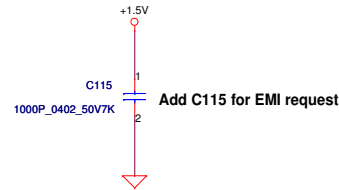
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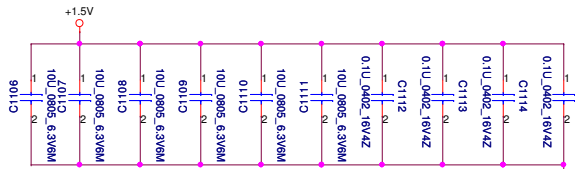
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- 9 DDR\_A\_DQS#[0..7] <<>>
- 9 DDR\_A\_D[0..63] <<>>
- 9 DDR\_A\_DM[0..7] <<>>
- 9 DDR\_A\_DQS#[0..7] <<>>
- 9 DDR\_A\_MA[0..14] <<>>

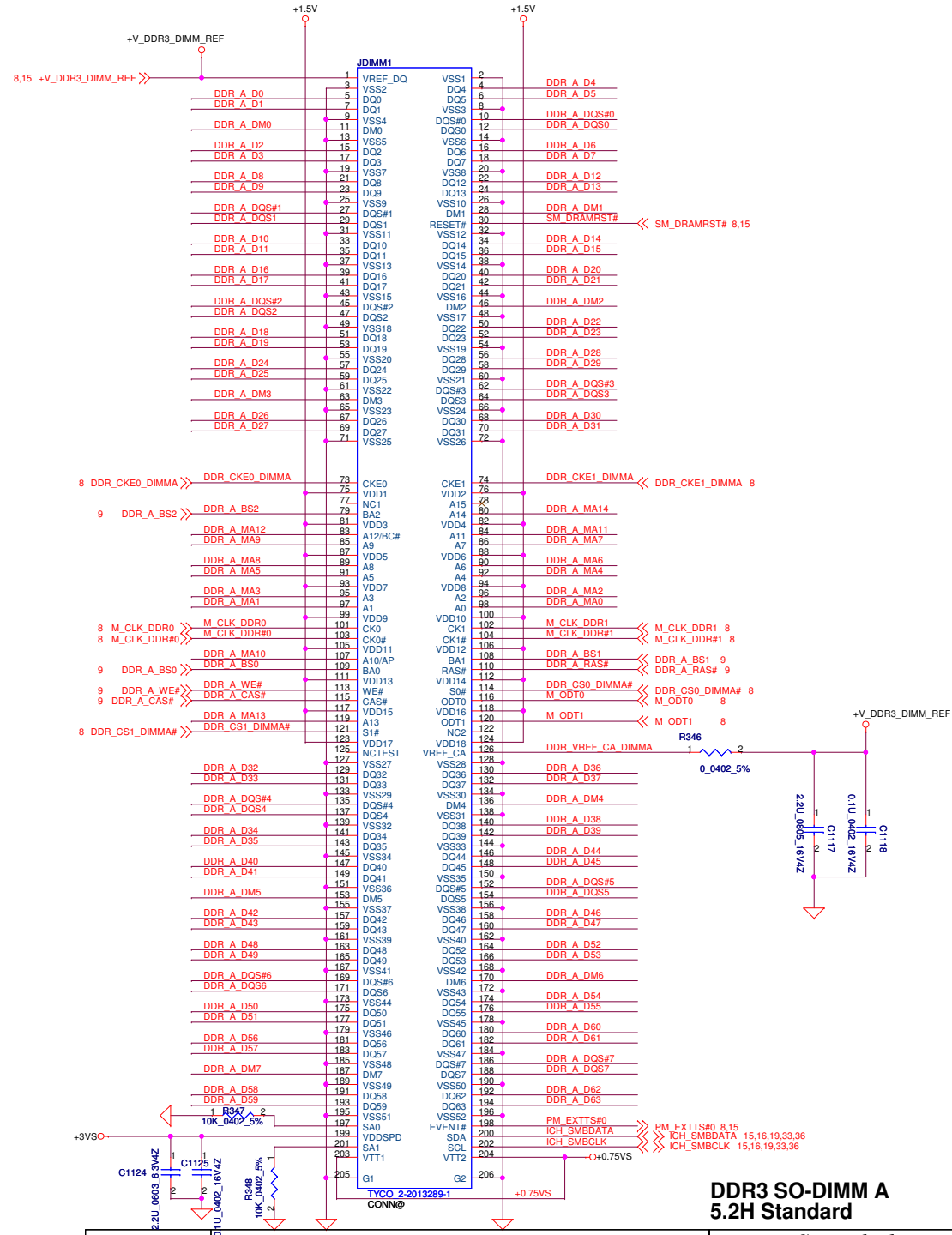
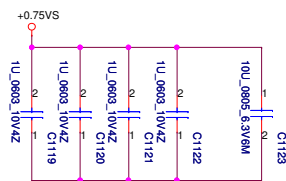


**Layout Note:  
Place near JDIMM1**

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



**Layout Note:  
Place near JDIMM1.203 & JDIMM1.204**



**DDR3 SO-DIMM A  
5.2H Standard**

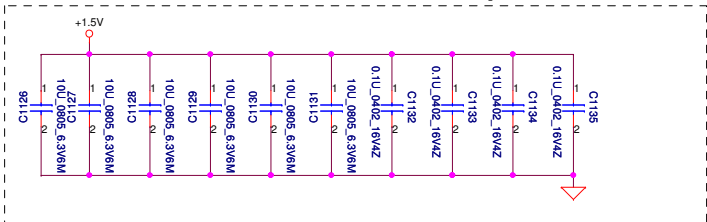
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Title			
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<b>DDR3-SODIMM A</b>			
Size	Document Number	Rev	
Custor	<b>LA-581P</b>	1.0	
Date:	Tuesday, December 29, 2009	Sheet	14 of 58

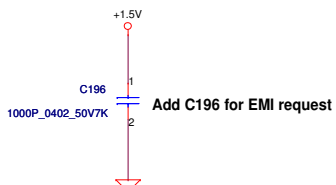
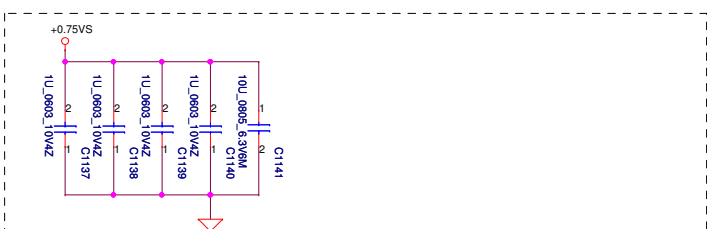
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- 9 DDR\_B\_D(0..63) <<>
- 9 DDR\_B\_DM(0..7) <<>
- 9 DDR\_B\_DQS(0..7) <<>
- 9 DDR\_B\_MA(0..14) <<>

**Layout Note:**  
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB



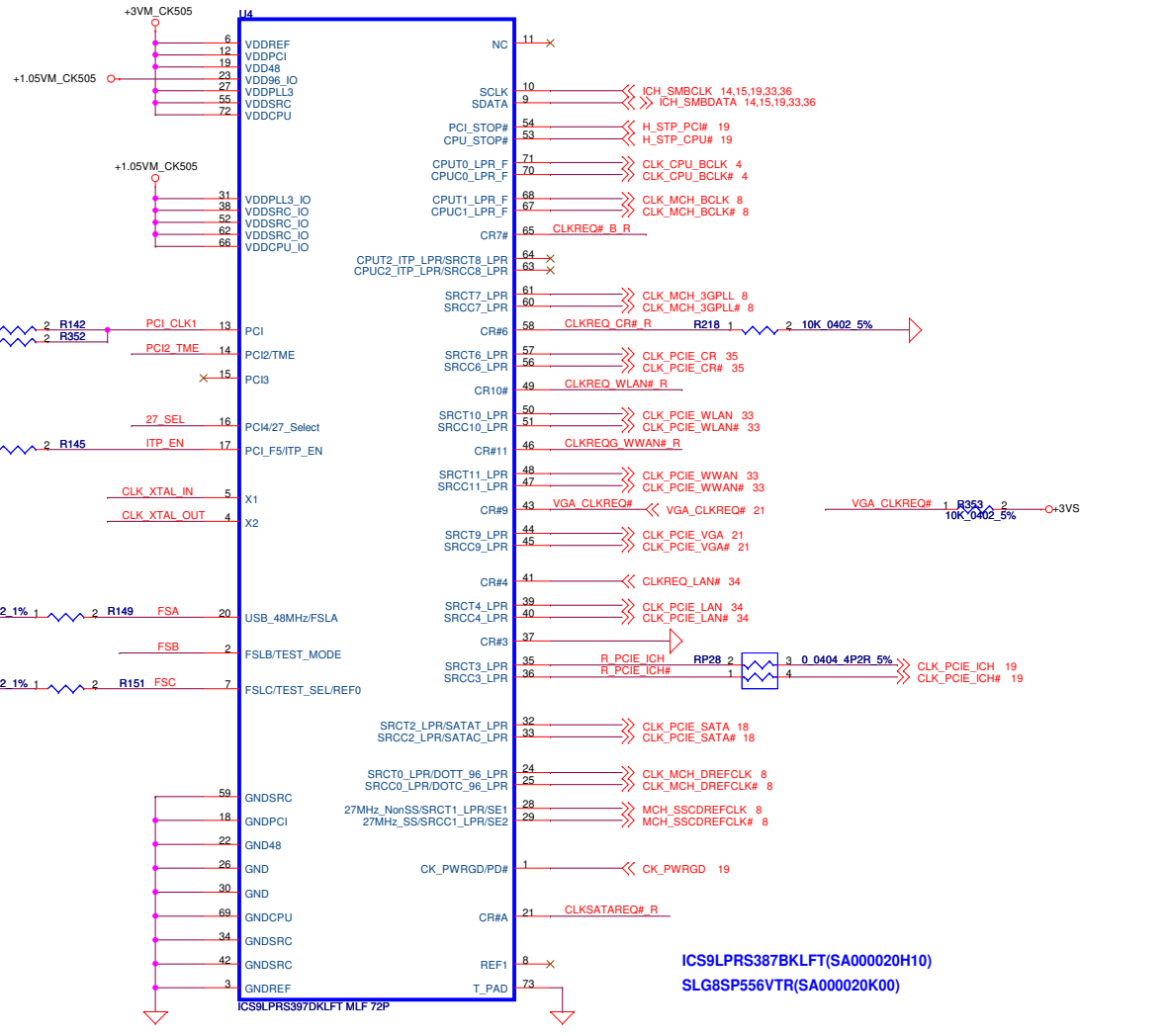
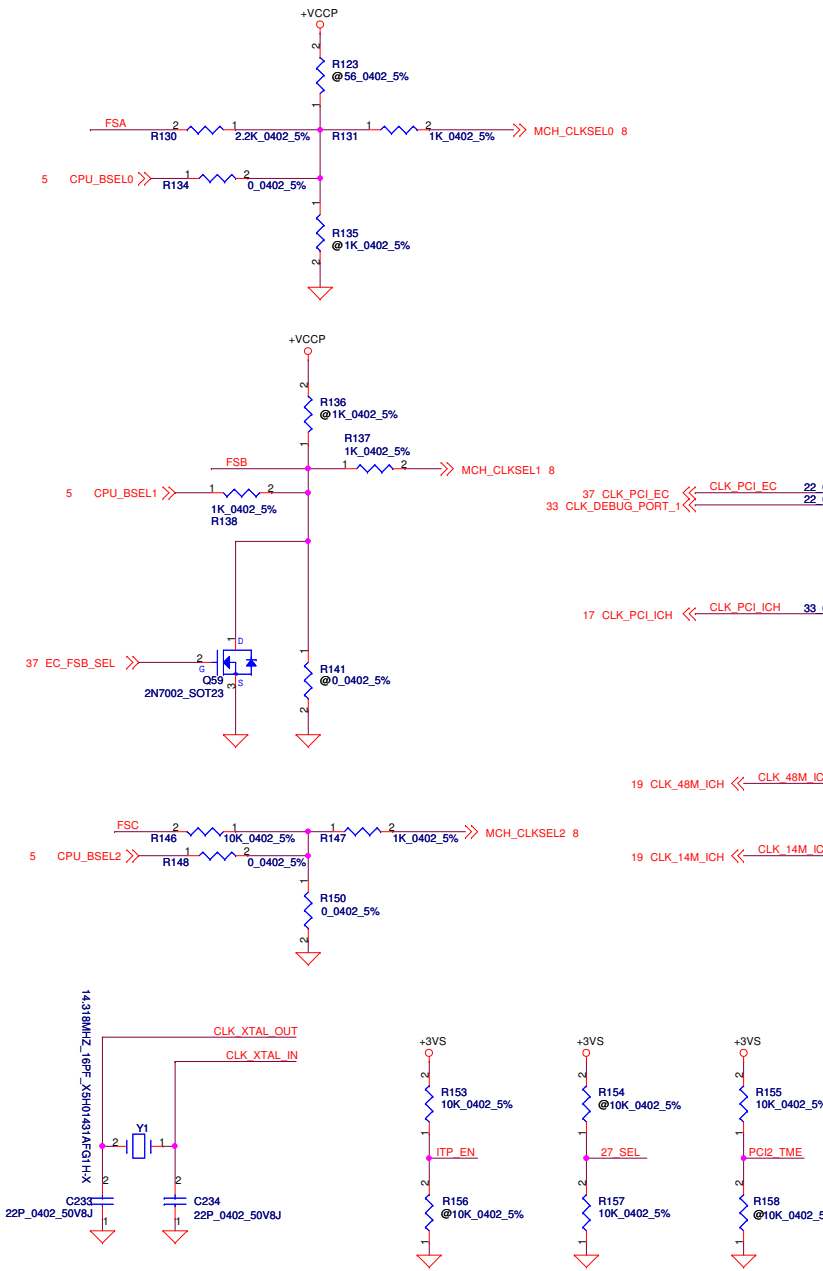
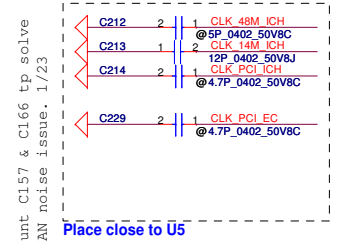
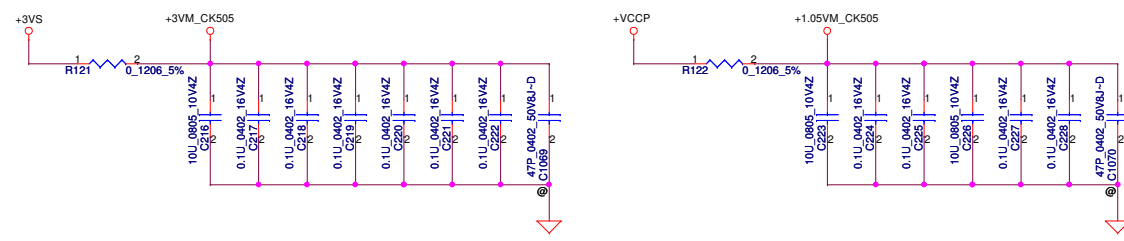
**Layout Note:**  
Place near JDIMM2.203 & JDIMM2.204



**DDR3 SO-DIMM B  
9.2H Standard**

Security Classification		Compal Secret Data		Title	
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				<b>DDR3-SODIMM B</b>	
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				LA-5811P	
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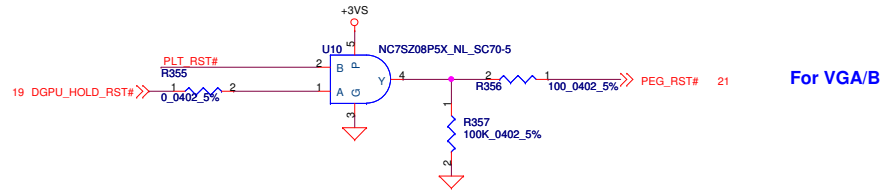
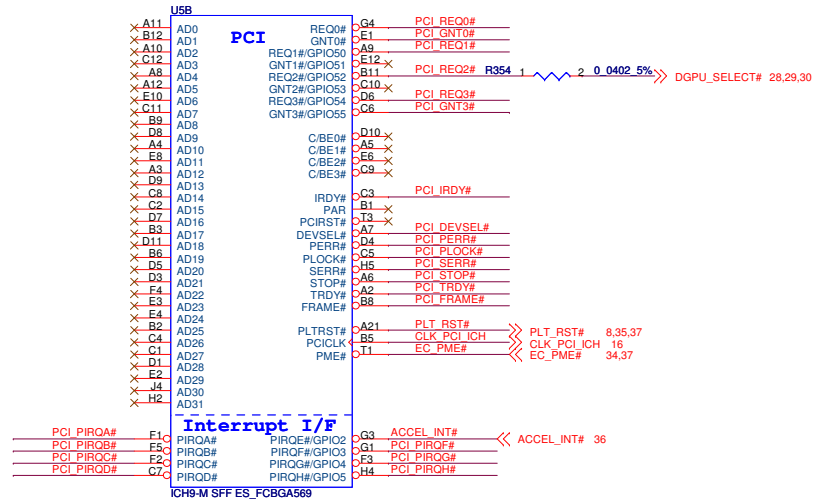
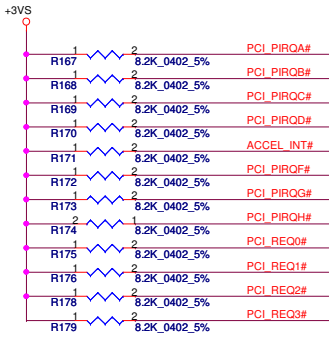
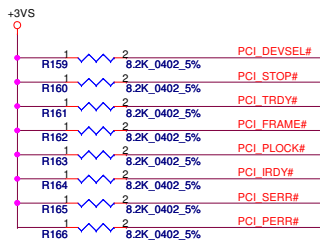
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CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz
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0	1	0	200	800	100	33.3
0	1	1	166	667	100	33.3



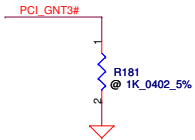
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				<b>CLOCK GENERATOR</b>
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Date: Tuesday, December 29, 2009				Sheet 16 of 58

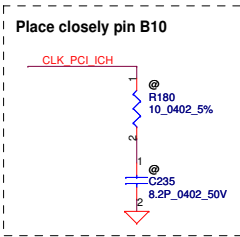
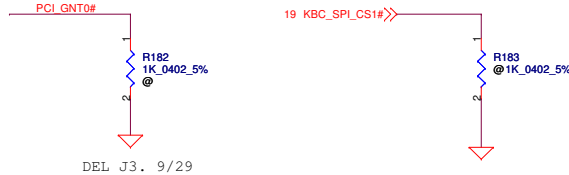




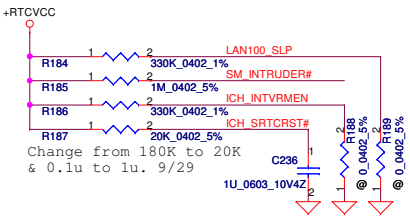
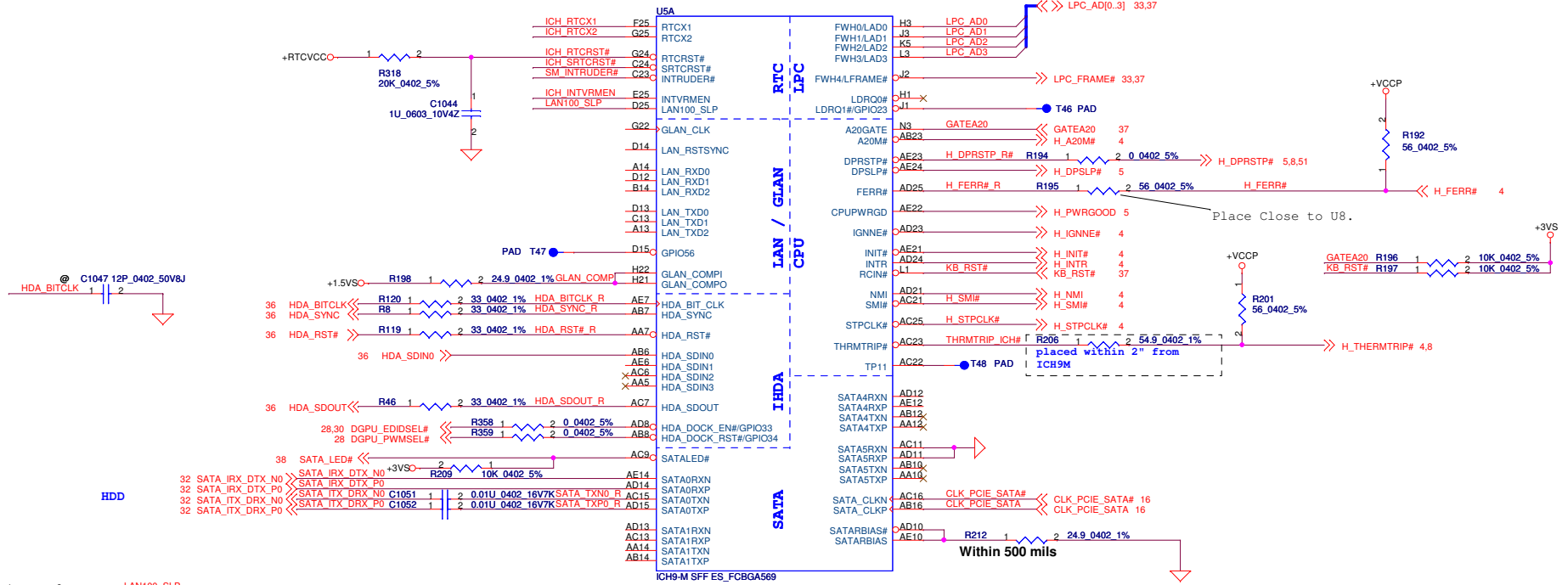
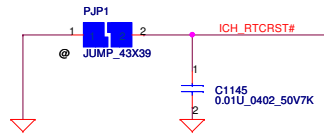
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*



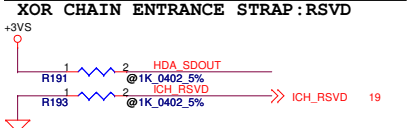
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



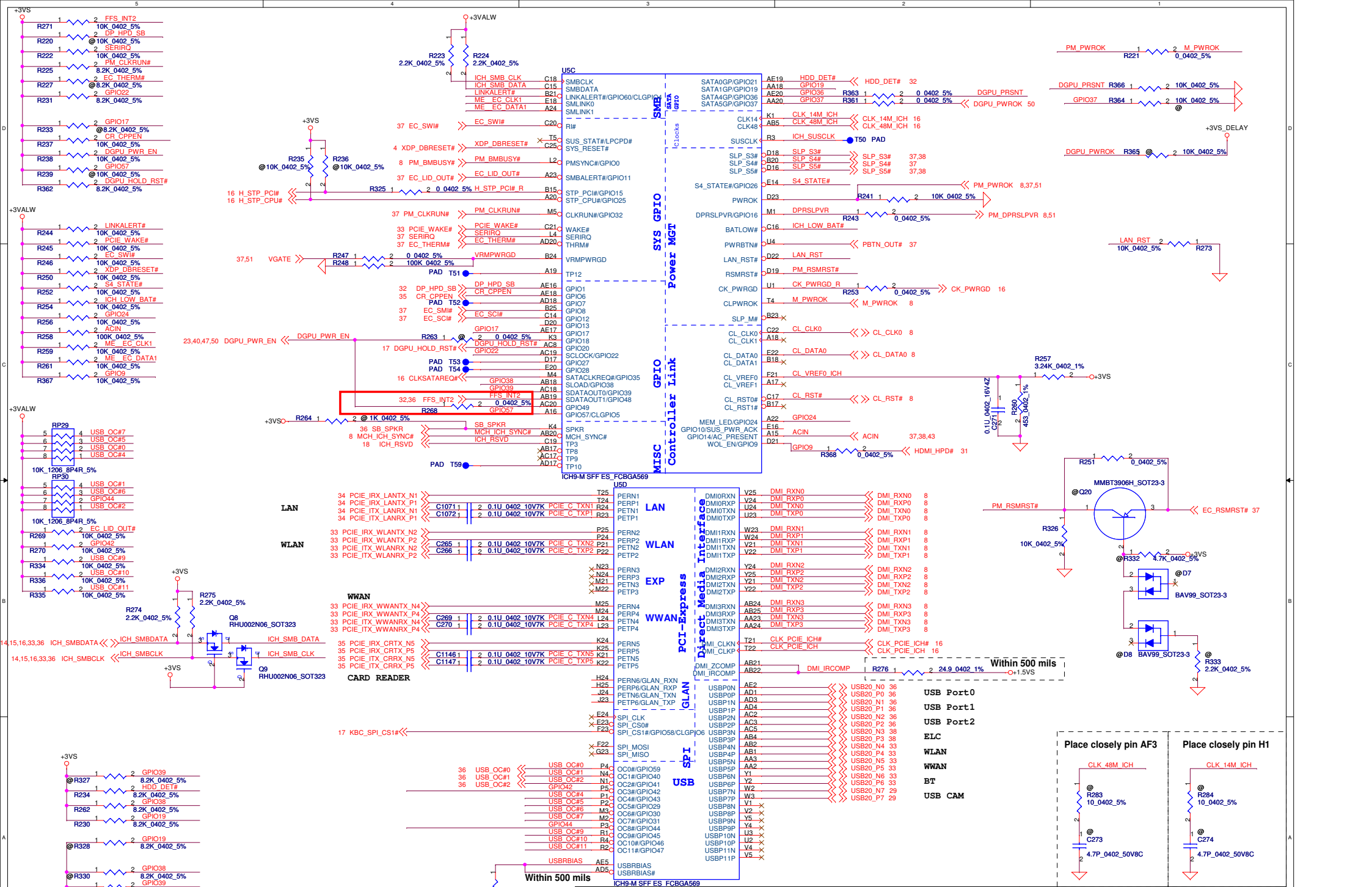
# RTC Reset SW



ICH_RSVD	HDA_SDOOUT_CODEC	Description
0	0	RV
0	1	XOR
1	0	Normal (D)
1	1	PCIE Bit1



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Size	Document Number	Rev	1.0
Custom	LA-5811P	Date:	Tuesday, December 29, 2009
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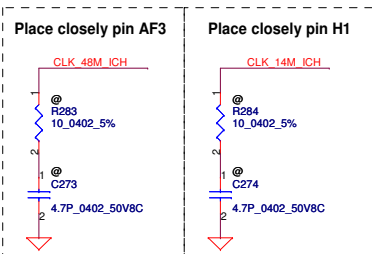
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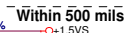
**ICH9(3/4) DMI,USB,GPIO,PCIE**

Size	Document Number	Rev
Custor	LA-5811P	1.0

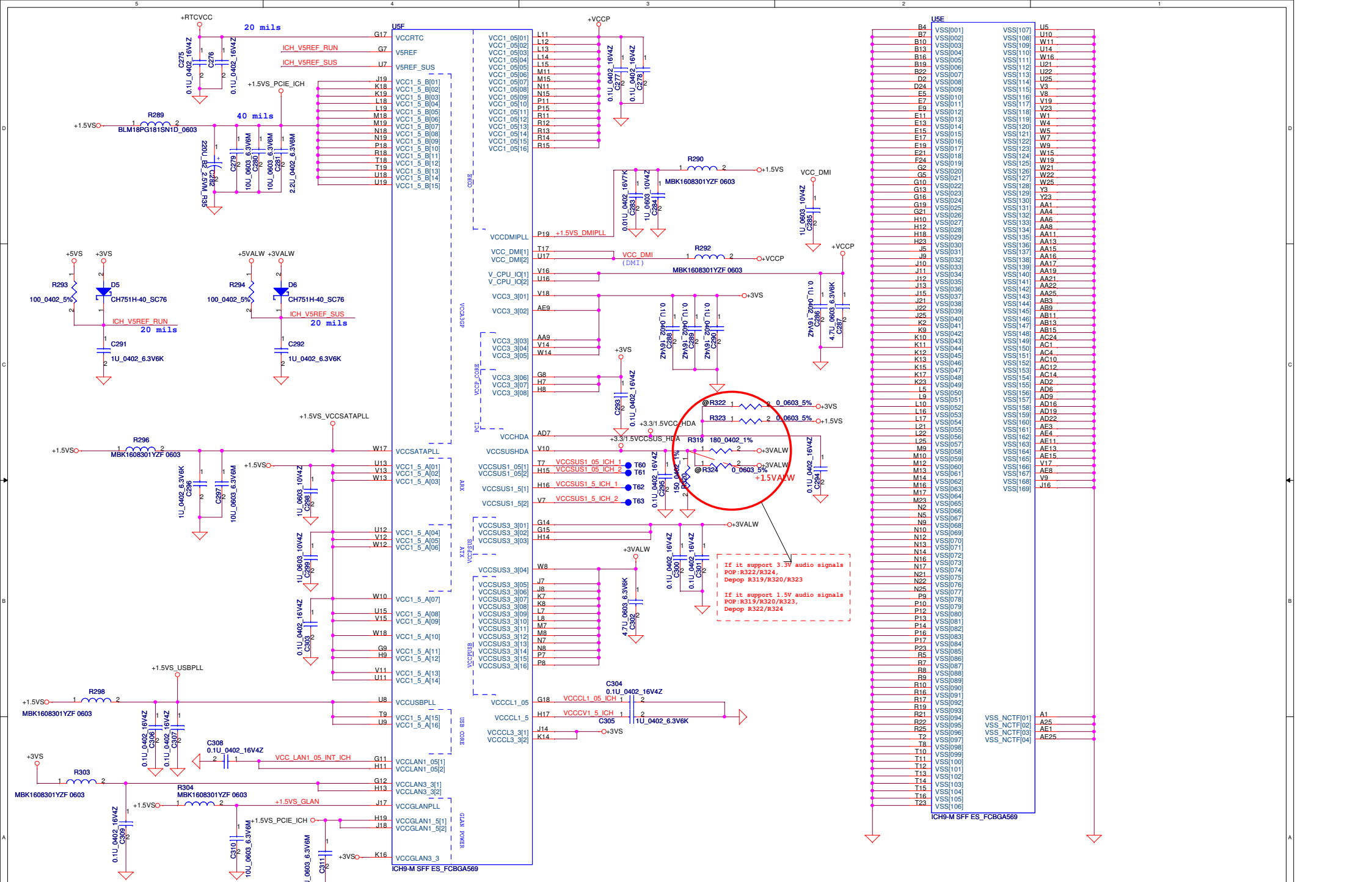
Date: Tuesday, December 29, 2009 Sheet 19 of 58



Within 500 mils



+1.5VS



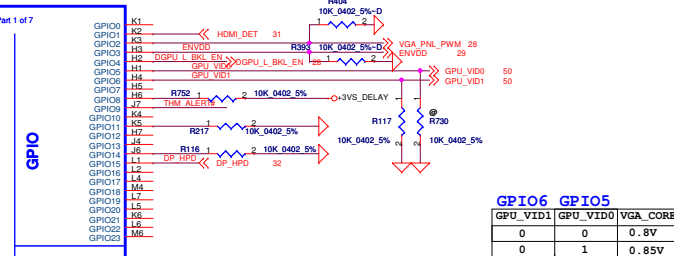
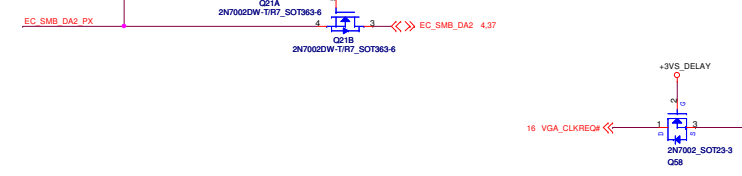
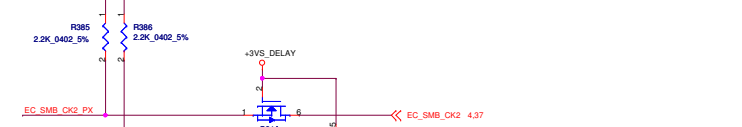
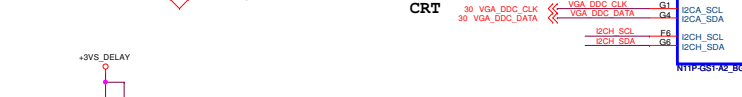
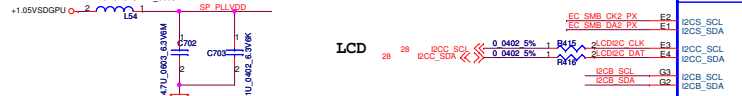
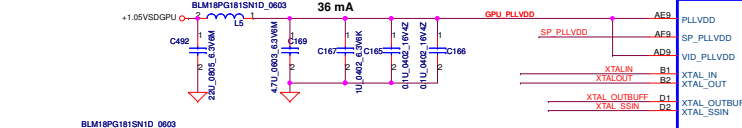
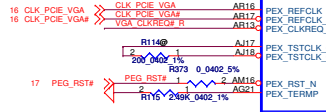
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<b>ICH9(4/4) POWER&amp;GND</b>			
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- 10 PCIE\_MTX\_C\_GRX\_N0-[15] >> PCIE\_MTX\_C\_GRX\_N0-[15]
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- 10 PCIE\_GTX\_C\_MRX\_N0-[15] >> PCIE\_GTX\_C\_MRX\_N0-[15]
- 10 PCIE\_GTX\_C\_MRX\_P0-[15] >> PCIE\_GTX\_C\_MRX\_P0-[15]

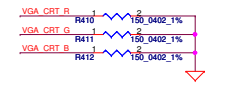
PCIE GTX C MRX P0	C1148	1	2	0.1U 0402 16V7K	PCIE GTX MRX P0	AM17	PEX TX0
PCIE GTX C MRX N0	C1149	1	2	0.1U 0402 16V7K	PCIE GTX MRX N0	AM17	PEX TX0_N
PCIE GTX C MRX P1	C1150	1	2	0.1U 0402 16V7K	PCIE GTX MRX P1	AM18	PEX TX0_N
PCIE GTX C MRX N1	C1151	1	2	0.1U 0402 16V7K	PCIE GTX MRX N1	AM19	PEX TX1_N
PCIE GTX C MRX P2	C1152	1	2	0.1U 0402 16V7K	PCIE GTX MRX P2	AM19	PEX TX2
PCIE GTX C MRX N2	C1153	1	2	0.1U 0402 16V7K	PCIE GTX MRX N2	AK19	PEX TX2_N
PCIE GTX C MRX P3	C1154	1	2	0.1U 0402 16V7K	PCIE GTX MRX P3	AM20	PEX TX3_N
PCIE GTX C MRX N3	C1155	1	2	0.1U 0402 16V7K	PCIE GTX MRX N3	AM20	PEX TX3
PCIE GTX C MRX P4	C1156	1	2	0.1U 0402 16V7K	PCIE GTX MRX P4	AM21	PEX TX4_N
PCIE GTX C MRX N4	C1157	1	2	0.1U 0402 16V7K	PCIE GTX MRX N4	AM22	PEX TX4
PCIE GTX C MRX P5	C1158	1	2	0.1U 0402 16V7K	PCIE GTX MRX P5	AM22	PEX TX5
PCIE GTX C MRX N5	C1159	1	2	0.1U 0402 16V7K	PCIE GTX MRX N5	AM22	PEX TX5_N
PCIE GTX C MRX P6	C1160	1	2	0.1U 0402 16V7K	PCIE GTX MRX P6	AM23	PEX TX6
PCIE GTX C MRX N6	C1161	1	2	0.1U 0402 16V7K	PCIE GTX MRX N6	AM23	PEX TX6_N
PCIE GTX C MRX P7	C1162	1	2	0.1U 0402 16V7K	PCIE GTX MRX P7	AM24	PEX TX7_N
PCIE GTX C MRX N7	C1163	1	2	0.1U 0402 16V7K	PCIE GTX MRX N7	AM25	PEX TX7
PCIE GTX C MRX P8	C1164	1	2	0.1U 0402 16V7K	PCIE GTX MRX P8	AM25	PEX TX8
PCIE GTX C MRX N8	C1165	1	2	0.1U 0402 16V7K	PCIE GTX MRX N8	AK25	PEX TX8_N
PCIE GTX C MRX P9	C1166	1	2	0.1U 0402 16V7K	PCIE GTX MRX P9	AM26	PEX TX9
PCIE GTX C MRX N9	C1167	1	2	0.1U 0402 16V7K	PCIE GTX MRX N9	AM26	PEX TX9_N
PCIE GTX C MRX P10	C1168	1	2	0.1U 0402 16V7K	PCIE GTX MRX P10	AM27	PEX TX10
PCIE GTX C MRX N10	C1169	1	2	0.1U 0402 16V7K	PCIE GTX MRX N10	AM27	PEX TX10_N
PCIE GTX C MRX P11	C1170	1	2	0.1U 0402 16V7K	PCIE GTX MRX P11	AM28	PEX TX11
PCIE GTX C MRX N11	C1171	1	2	0.1U 0402 16V7K	PCIE GTX MRX N11	AK28	PEX TX11_N
PCIE GTX C MRX P12	C1172	1	2	0.1U 0402 16V7K	PCIE GTX MRX P12	AK29	PEX TX12
PCIE GTX C MRX N12	C1173	1	2	0.1U 0402 16V7K	PCIE GTX MRX N12	AM29	PEX TX12_N
PCIE GTX C MRX P13	C1174	1	2	0.1U 0402 16V7K	PCIE GTX MRX P13	AM29	PEX TX13
PCIE GTX C MRX N13	C1175	1	2	0.1U 0402 16V7K	PCIE GTX MRX N13	AM30	PEX TX13_N
PCIE GTX C MRX P14	C1176	1	2	0.1U 0402 16V7K	PCIE GTX MRX P14	AM31	PEX TX14
PCIE GTX C MRX N14	C1177	1	2	0.1U 0402 16V7K	PCIE GTX MRX N14	AM32	PEX TX14_N
PCIE GTX C MRX P15	C1178	1	2	0.1U 0402 16V7K	PCIE GTX MRX P15	AK32	PEX TX15
PCIE GTX C MRX N15	C1179	1	2	0.1U 0402 16V7K	PCIE GTX MRX N15	AK32	PEX TX15_N



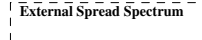
**GPIO6 GPIO5**

GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.8V
0	1	0.85V
1	1	0.95V

**N11P-GS1**

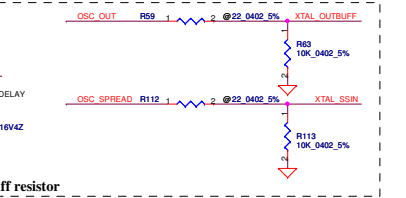
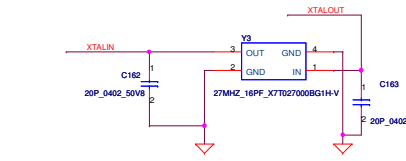


MIOB_D1	Y1	NC
MIOB_D2	Y2	NC
MIOB_D3	AB3	NC
MIOB_D4	AB1	NC
MIOB_D5	AC4	NC
MIOB_D6	AC1	NC
MIOB_D7	AC2	NC
MIOB_D8	AC3	NC
MIOB_D9	AE3	NC
MIOB_D10	AE2	NC
MIOB_D11	UB	NC
MIOB_D12	VB	NC
MIOB_D13	VB	NC
MIOB_D14	VB	NC
MIOB_HSYNC	W1	NC
MIOB_VSYNC	Y2	NC
MIOB_RST_N	AE1	NC
MIOB_TEMP	AE1	NC
MIOB_CLKIN	AE1	NC
MIOB_CLKOUT	AE1	NC
MIOB_CLKOUT_N	AE1	NC
MIOB_CLKIN_N	AE1	NC
MIOB_CAL_PD_VDD	AA2	NC
MIOB_CAL_PU_GND	AA2	NC
DACA_RED	AM15	NC
DACA_GREEN	AM14	NC
DACA_BLUE	AL14	NC
DACA_HSYNC	AM13	NC
DACA_VSYNC	AL13	NC
DACA_VDD	AK12	NC
DACA_VREF	AK12	NC
DACA_RSET	AK12	NC
DACB_RED	AK4	NC
DACB_GREEN	A4	NC
DACB_BLUE	AM1	NC
DACB_HSYNC	AM1	NC
DACB_VSYNC	AM2	NC
DACB_VDD	AG7	NC
DACB_VREF	AG7	NC
DACB_RSET	AH7	NC



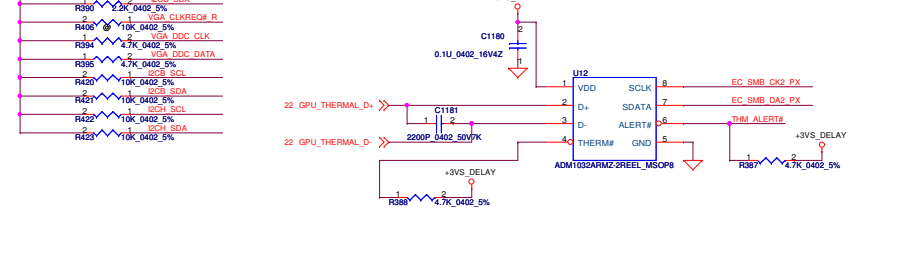
If External Spread Spectrum not stuff then stuff resistor

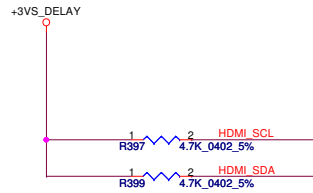
GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	H	N/A
GPIO1	IN	H	HDMI Hot-plug
GPIO2	OUT	H	VGA_PNL_PWM
GPIO3	OUT	H	ENVDD
GPIO4	OUT	H	VGA_BKL_EN
GPIO5	OUT	N/A	NVDD VID0
GPIO6	OUT	N/A	NVDD VID1
GPIO7	IN	L	N/A
GPIO8	IN	L	N/A
GPIO9	IN	L	THM_ALERT#
GPIO10	OUT	N/A	N/A
GPIO11	OUT	N/A	N/A
GPIO12	IN	N/A	N/A
GPIO13	OUT	N/A	N/A
GPIO14	OUT	N/A	N/A
GPIO15	IN	H	DP Hot-plug



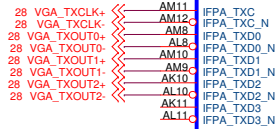
VGA CRT\_VSYNC and VGA CRT\_HSYNC pull up to HDMI & DISPLAY PORT AUDIO function

**VGA Thermal Sensor ADM1032ARMZ**

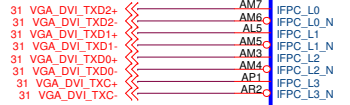




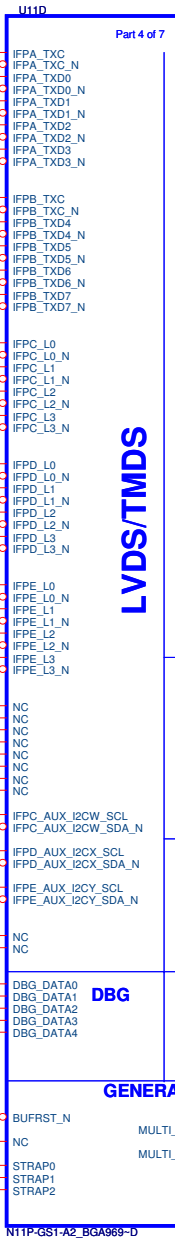
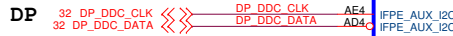
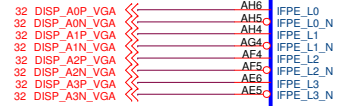
**LVDS**



**HDMI**



**DP**



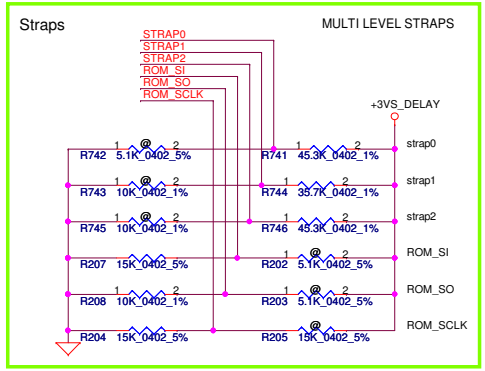
**NC**

**LVDS/TMDS**

**TEST**

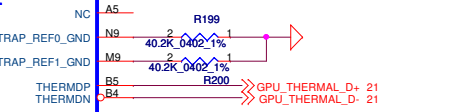
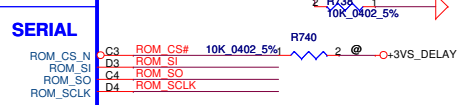
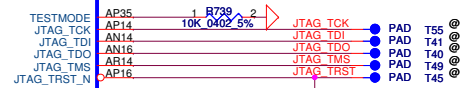
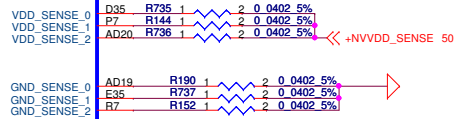
**SERIAL**

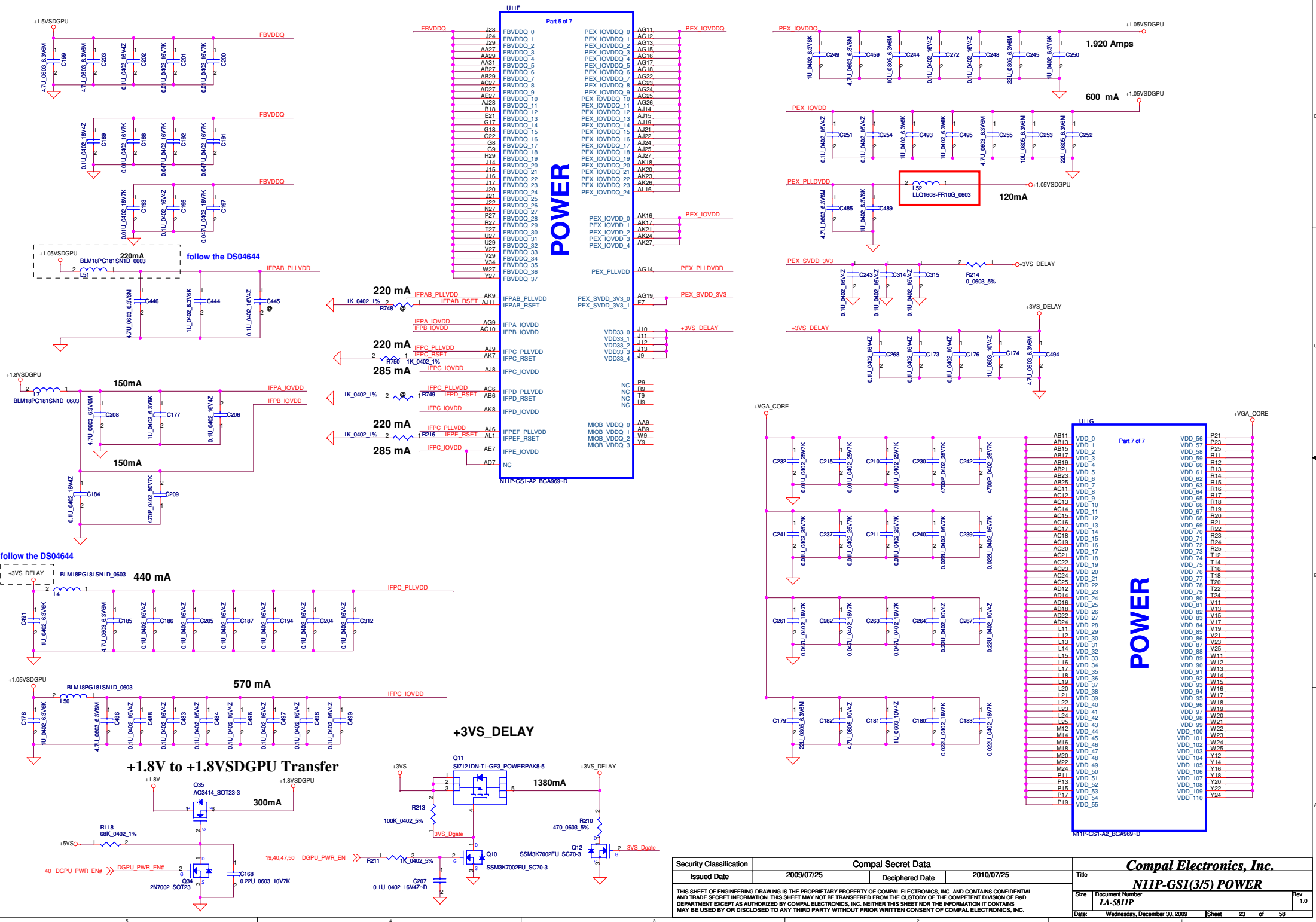
**GENERAL**



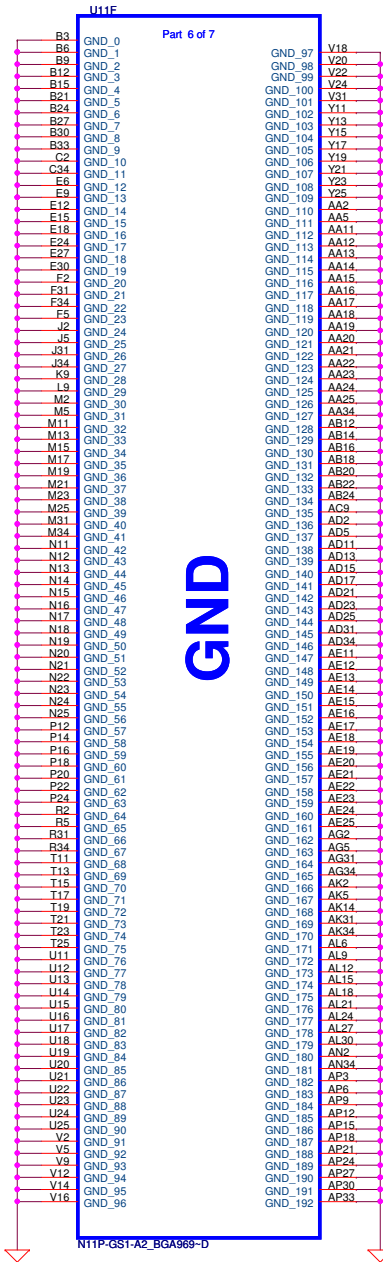
	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung	H 45K	H 35K	H 30K	L 20K	L 10K	L 15K
64MX16 Hynix	H 45K	H 35K	H 30K	L 15K	L 10K	L 15K

SSI --> Hynix  
 PT --> Hynix  
 ST --> Hynix(main),Samsung(second)  
 Hynix:SA0000032400  
 Samsung:SA0000035700



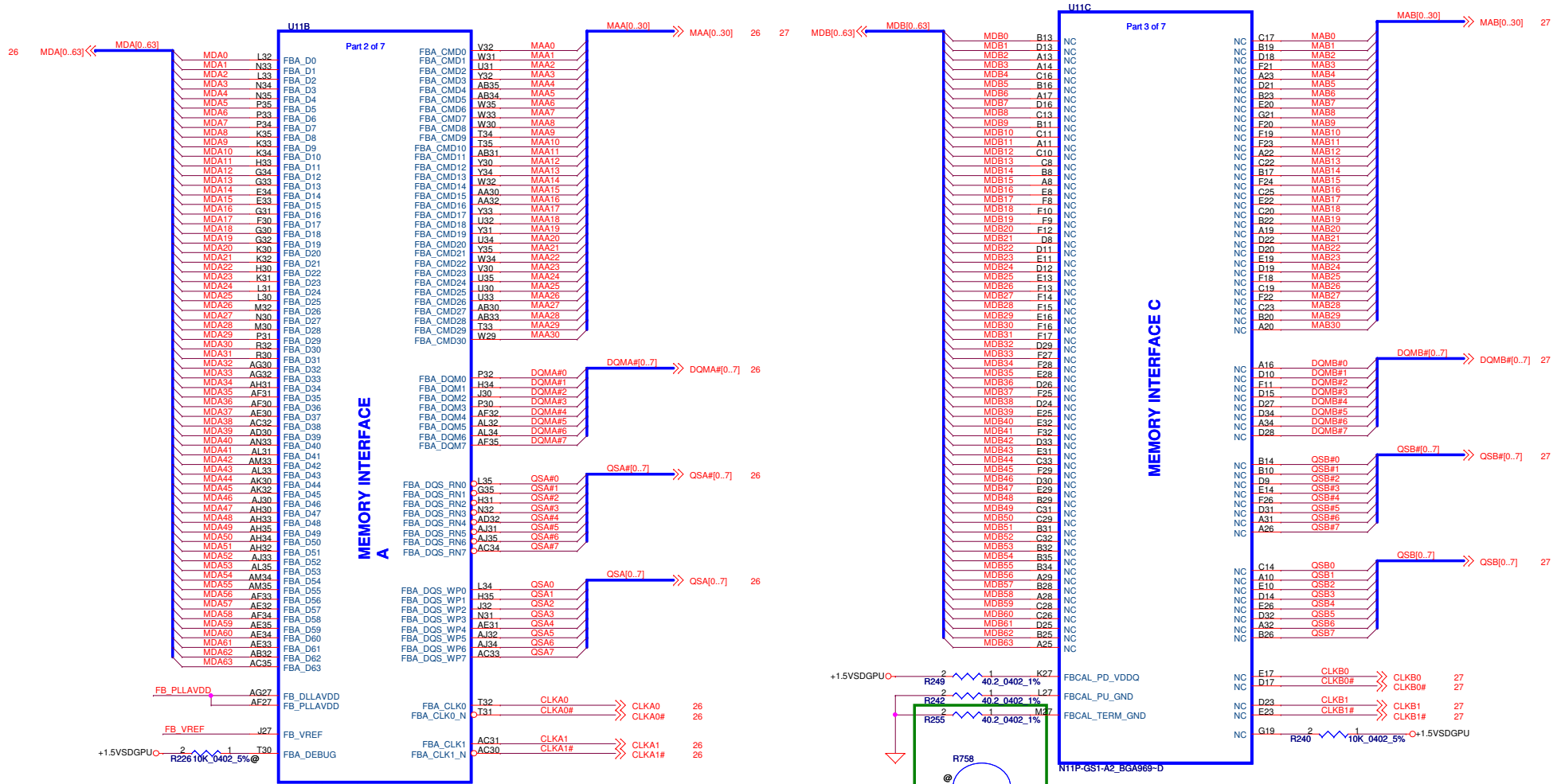


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<b>Compal Electronics, Inc.</b> <b>N11P-GS1(3/5) POWER</b>			
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				Date:	Tuesday, December 29, 2009	Sheet





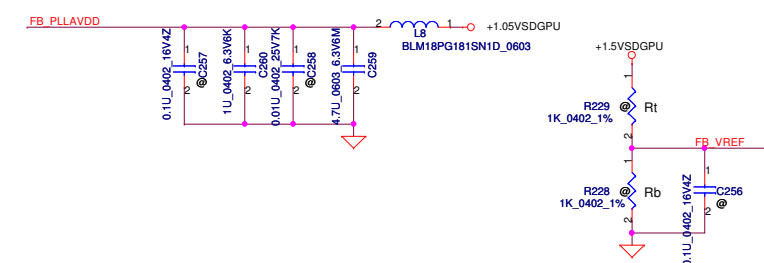
**MEMORY INTERFACE A**

**MEMORY INTERFACE C**

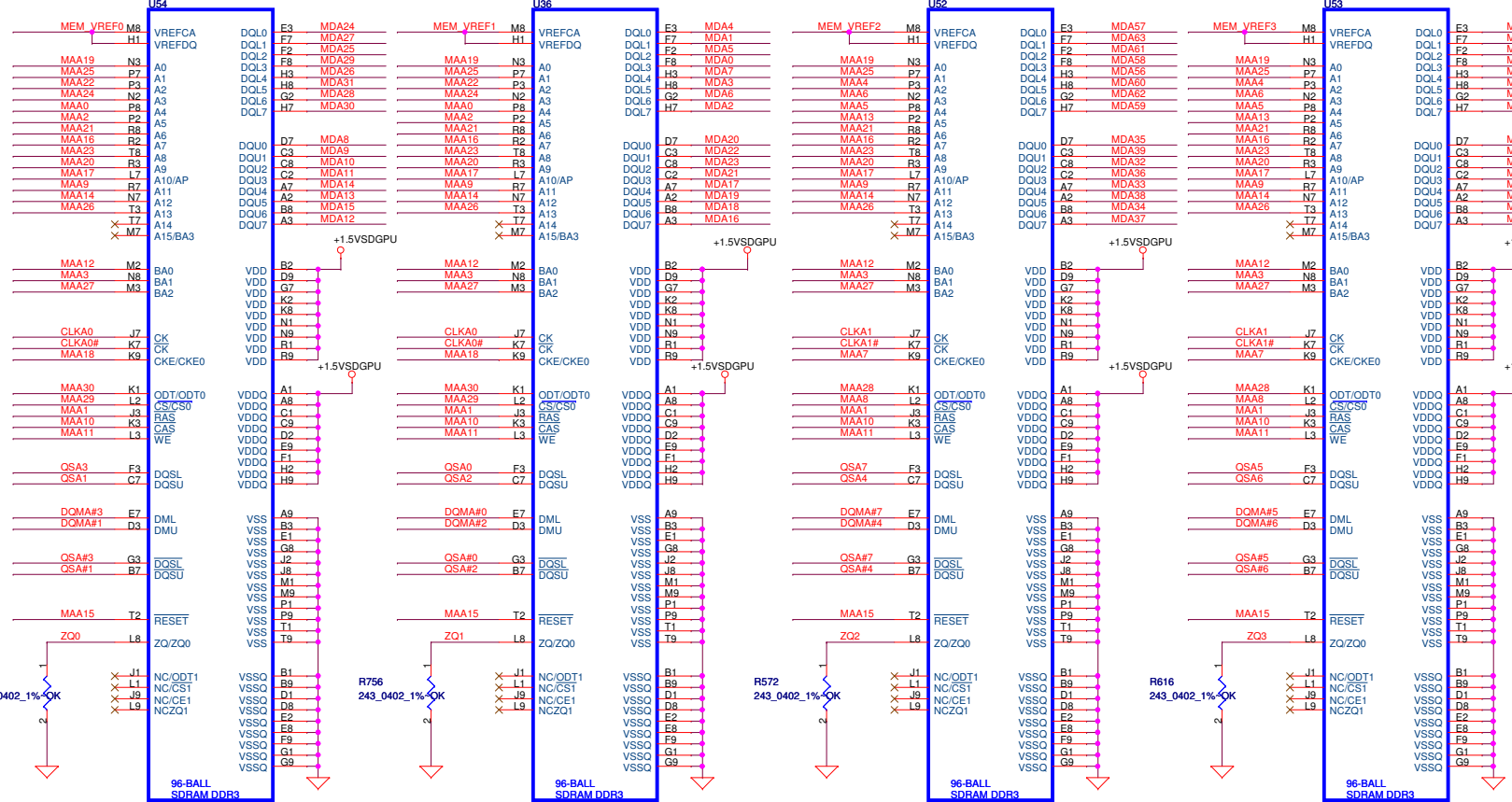
Place Components Close to BGA

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR3 (11P)	+1.5VS	40.2 ohm	40.2 ohm	40.2 ohm

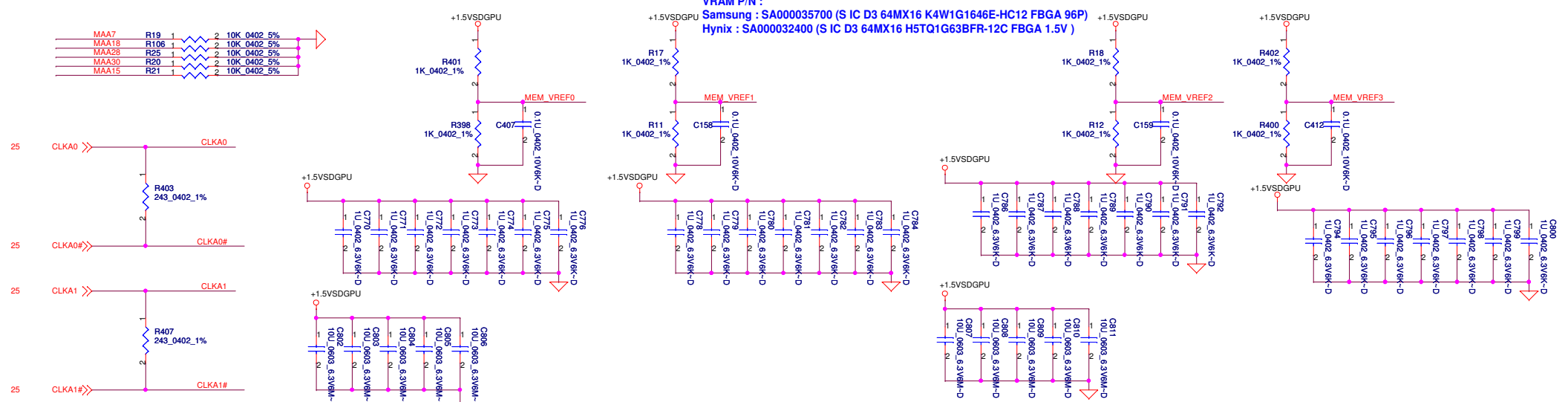
Must be used 1% resistor for driver calibration



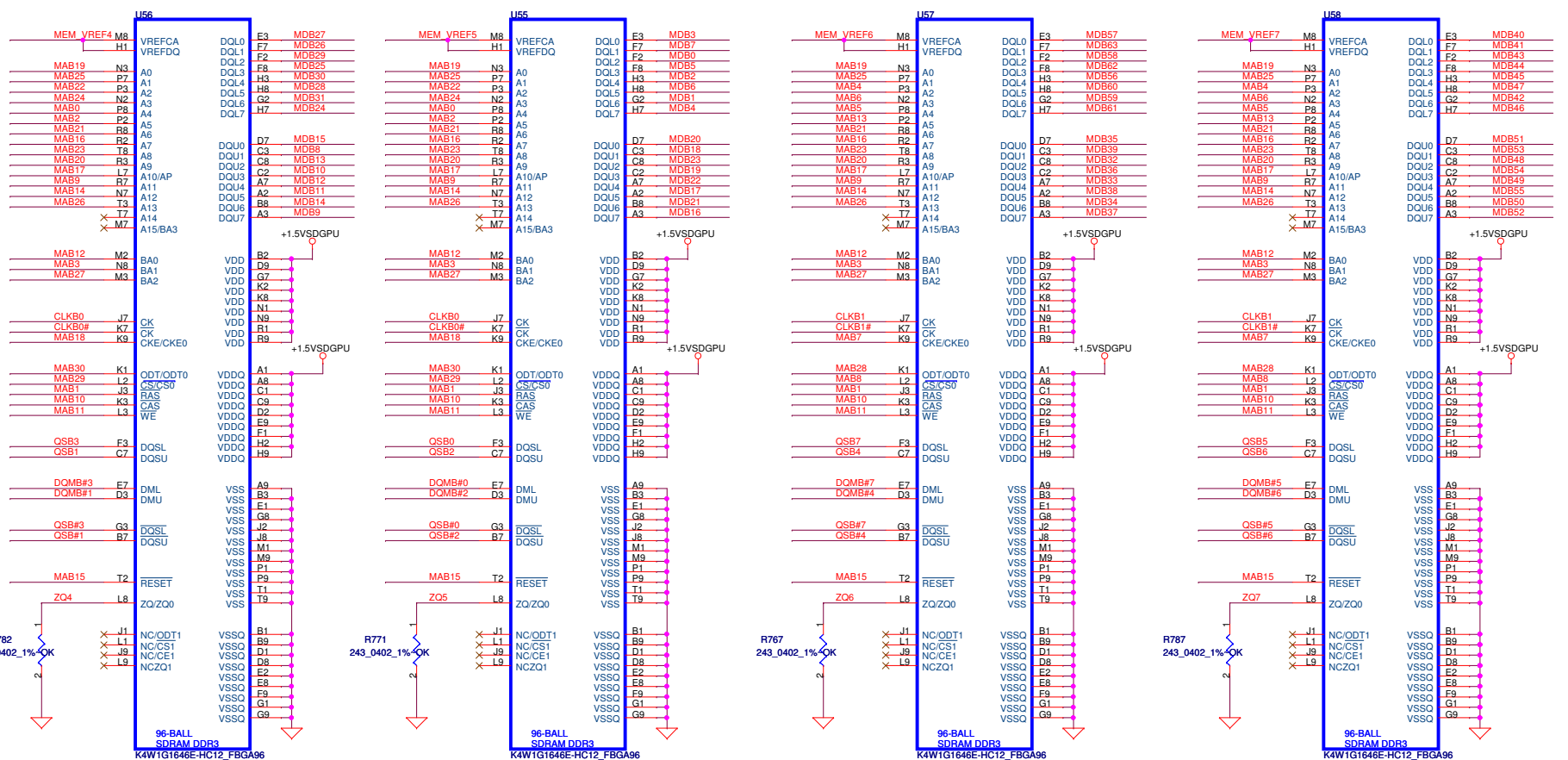
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Issued Date	2009/07/25	Deciphered Date	2010/07/25	<b>Compal Electronics, Inc.</b>
				<b>N11P-GS1(S/5) MEMORY</b>
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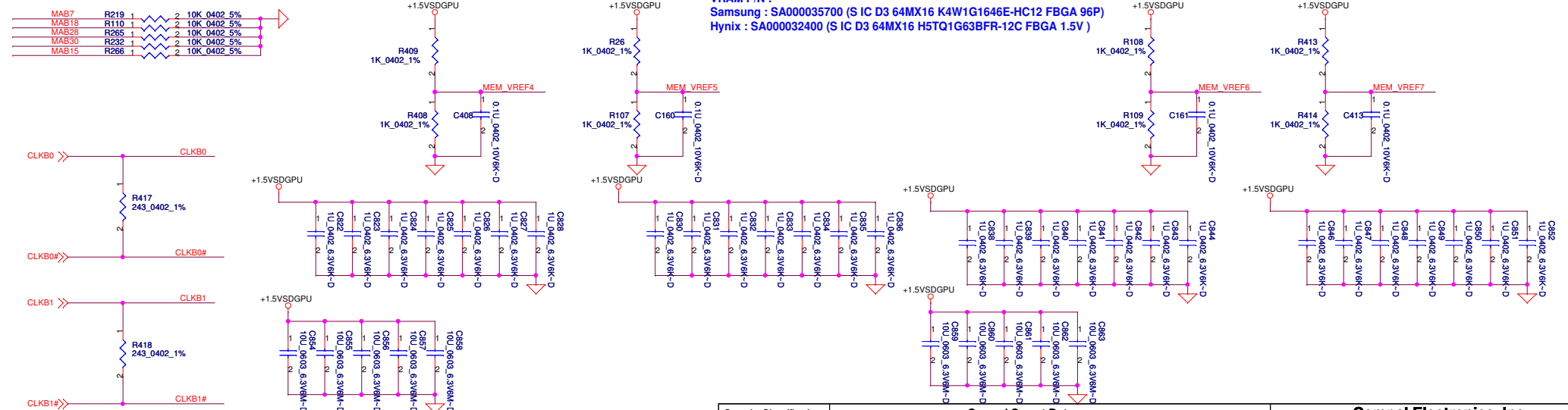
VRAM P/N :  
 Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)  
 Hynix : SA000032400 (S IC D3 64MX16 H5T1G163BFR-12C FBGA 1.5V)



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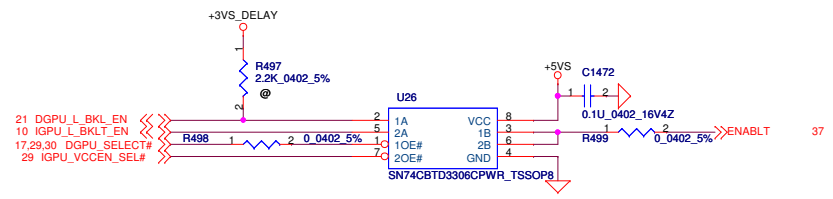
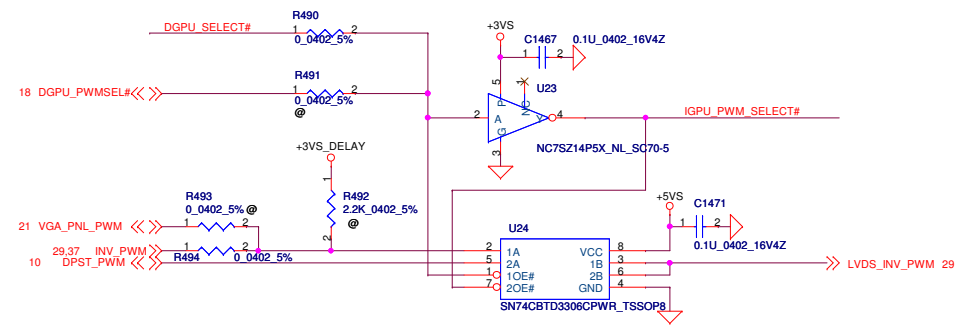
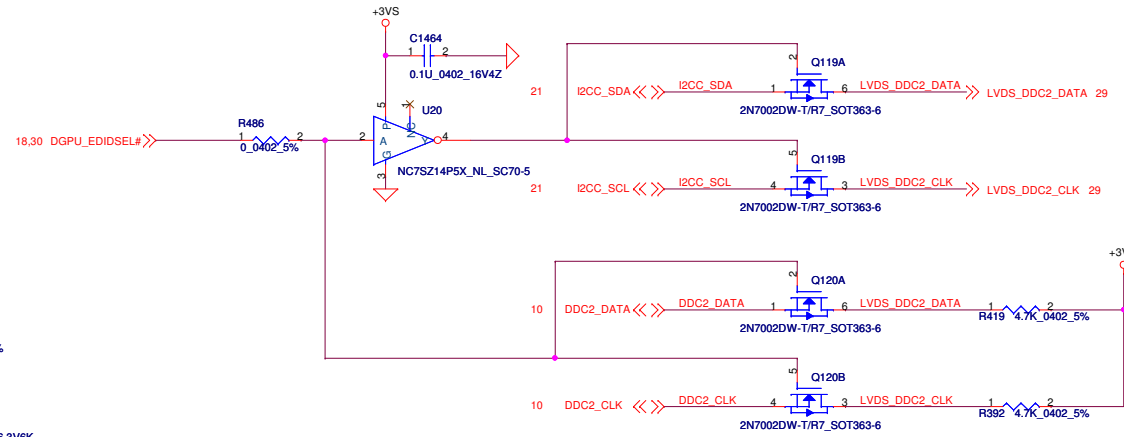
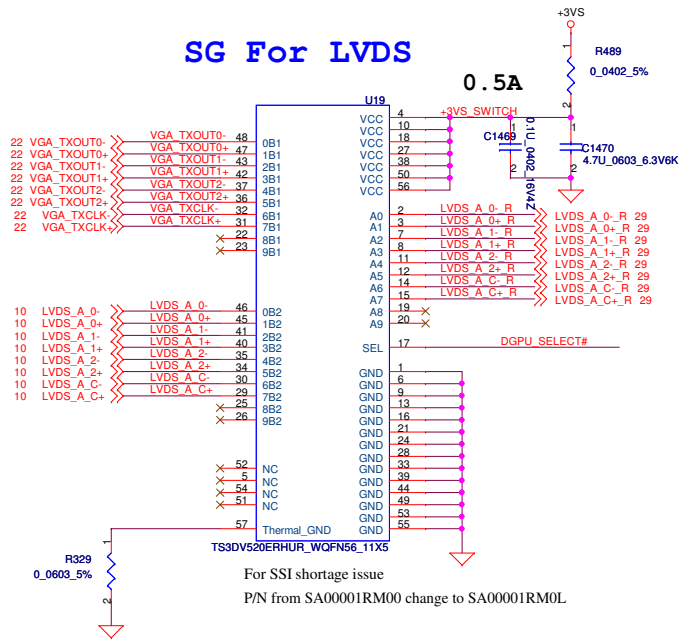
VRAM P/N :  
 Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)  
 Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)



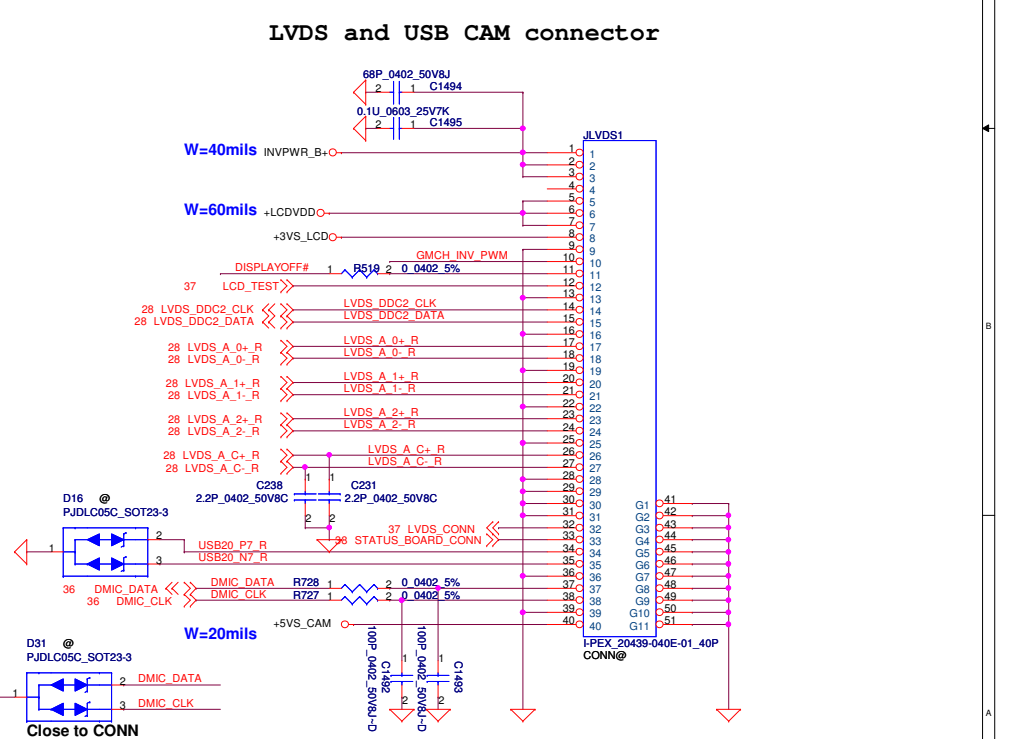
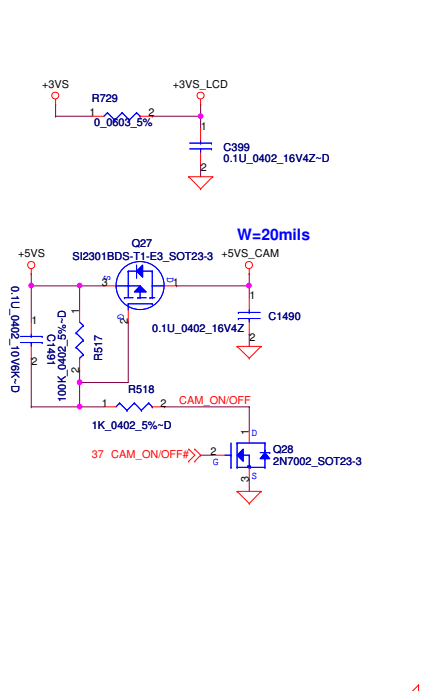
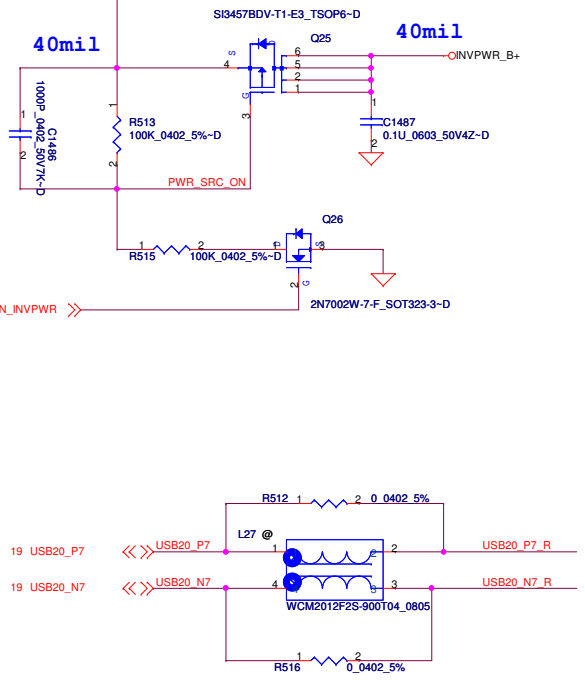
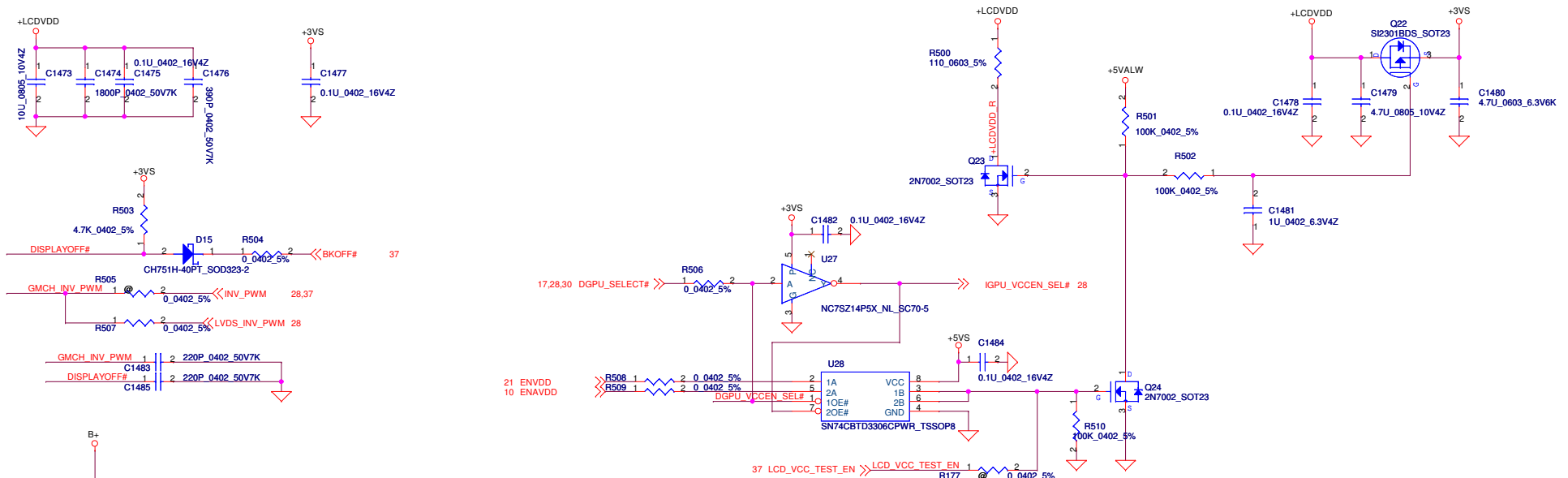
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VRAM DDR3 / Channel B					
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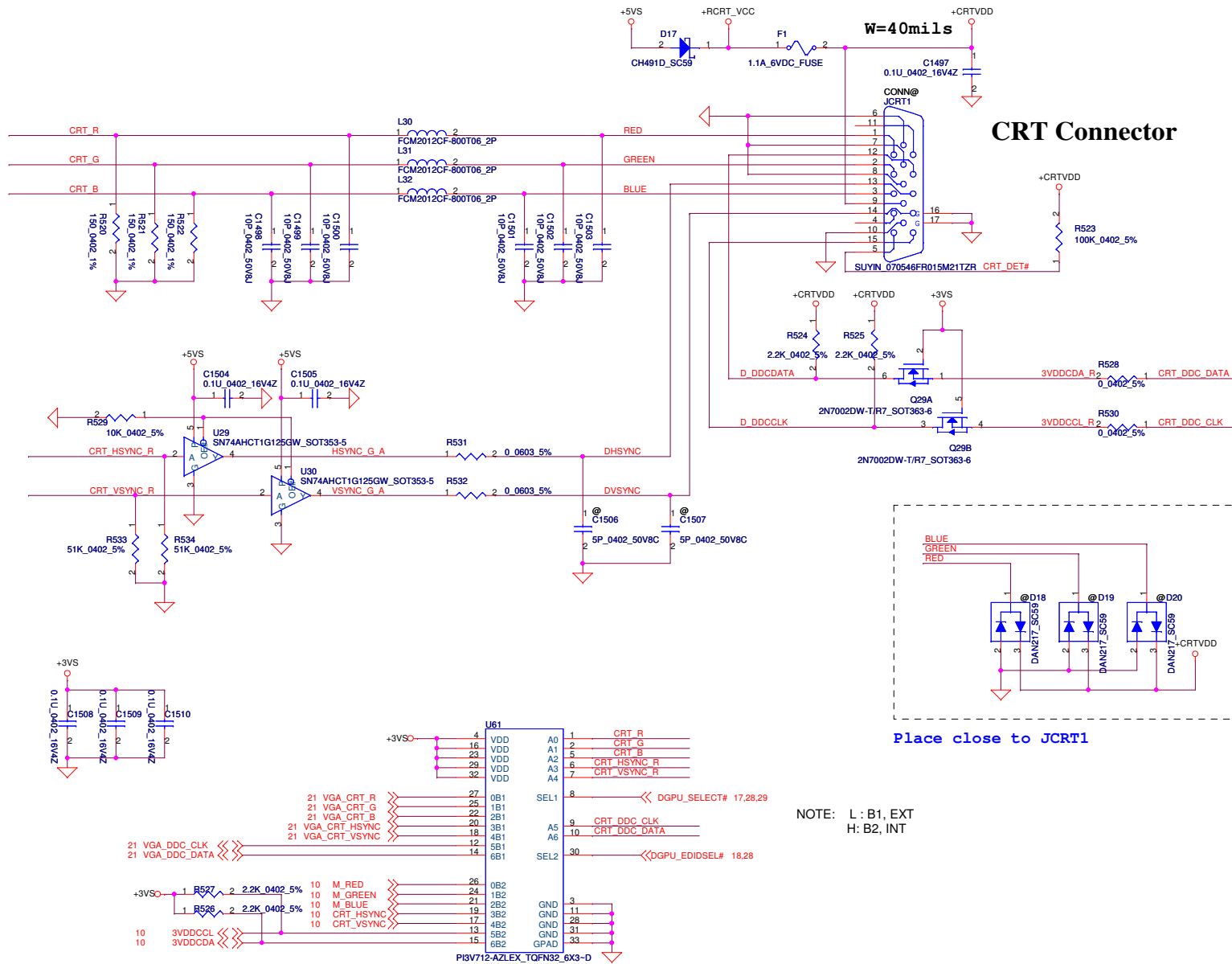
# SG For LVDS



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				LVDS Switch	
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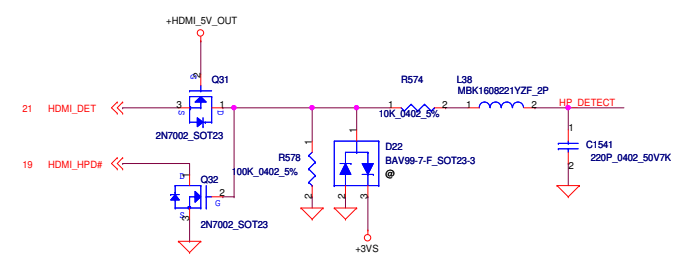
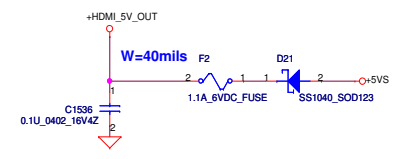
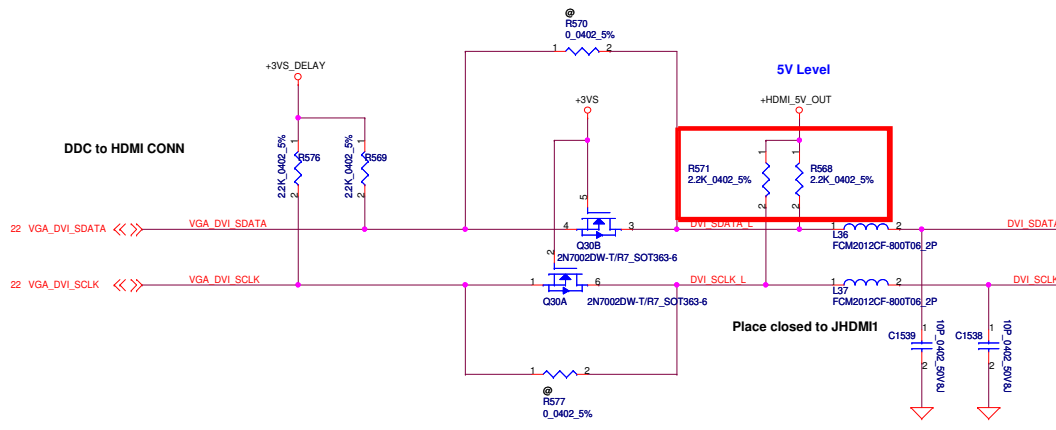


### CRT Connector

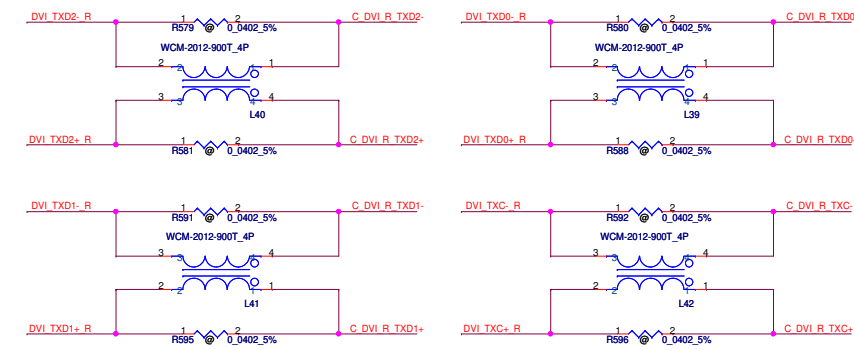
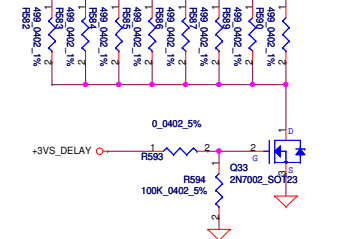
Place close to JCRT1

NOTE: L : B1, EXT  
H: B2, INT

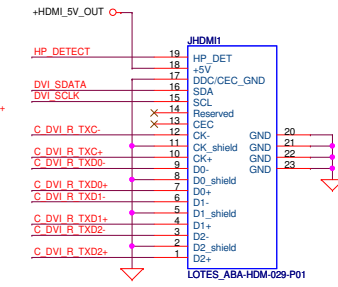
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				Rev	1.0



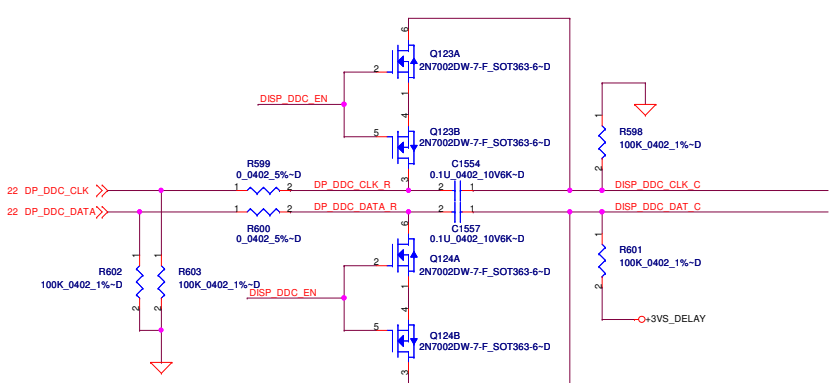
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22	VGA_DVI_TXD2+	VGA DVI TXD2+	C1543	2	1	0.1U 0402 16V7K	DVI TXD2+ R
22	VGA_DVI_TXD1-	VGA DVI TXD1-	C1544	2	1	0.1U 0402 16V7K	DVI TXD1- R
22	VGA_DVI_TXD1+	VGA DVI TXD1+	C1545	2	1	0.1U 0402 16V7K	DVI TXD1+ R
22	VGA_DVI_TXD0-	VGA DVI TXD0-	C1546	2	1	0.1U 0402 16V7K	DVI TXD0- R
22	VGA_DVI_TXD0+	VGA DVI TXD0+	C1547	2	1	0.1U 0402 16V7K	DVI TXD0+ R
22	VGA_DVI_TXC-	VGA DVI TXC-	C1548	2	1	0.1U 0402 16V7K	DVI TXC- R
22	VGA_DVI_TXC+	VGA DVI TXC+	C1549	2	1	0.1U 0402 16V7K	DVI TXC+ R



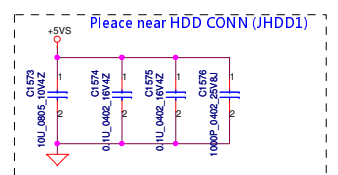
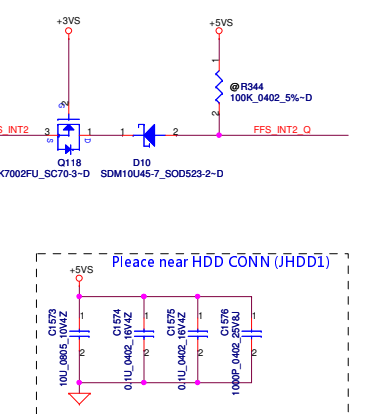
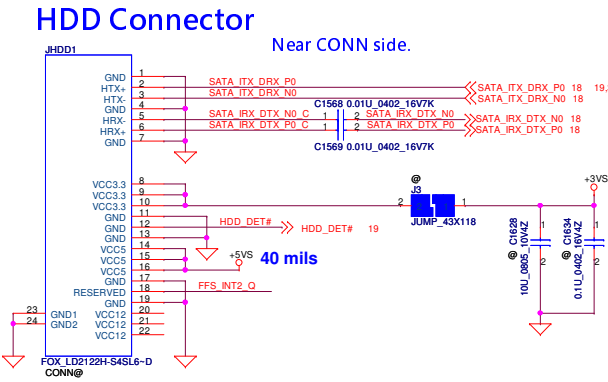
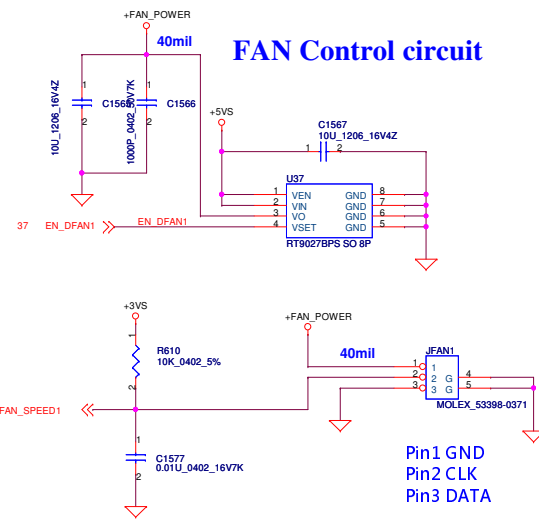
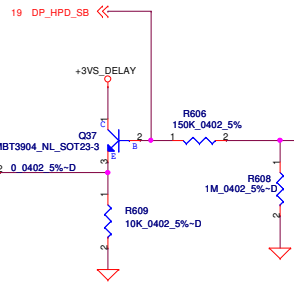
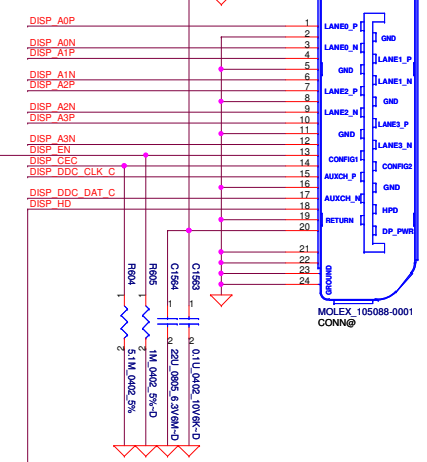
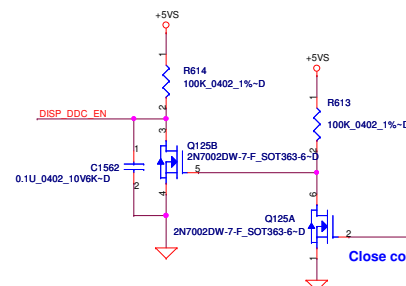
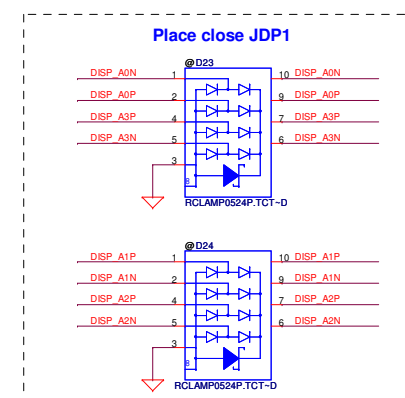
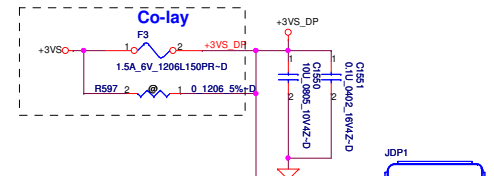
### HDMI Connector



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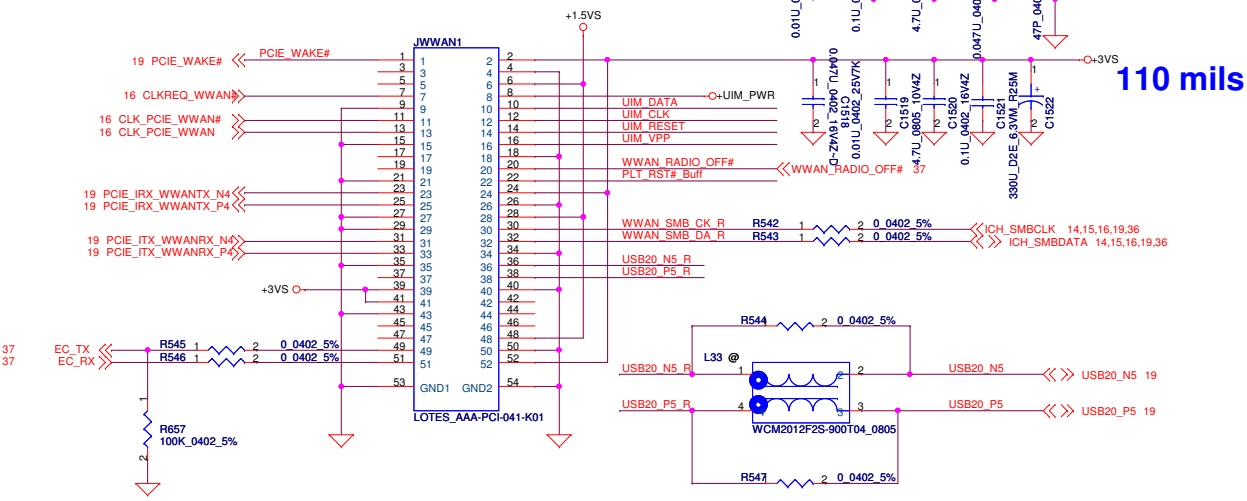
- 22 DISP\_A0N\_VGA >> C1552.2 | 0.1U 0402 10V6K-D | DISP\_A0N
- 22 DISP\_A0P\_VGA >> C1553.2 | 0.1U 0402 10V6K-D | DISP\_A0P
- 22 DISP\_A1N\_VGA >> C1555.2 | 0.1U 0402 10V6K-D | DISP\_A1N
- 22 DISP\_A1P\_VGA >> C1556.2 | 0.1U 0402 10V6K-D | DISP\_A1P
- 22 DISP\_A2N\_VGA >> C1558.2 | 0.1U 0402 10V6K-D | DISP\_A2N
- 22 DISP\_A2P\_VGA >> C1559.2 | 0.1U 0402 10V6K-D | DISP\_A2P
- 22 DISP\_A3N\_VGA >> C1560.2 | 0.1U 0402 10V6K-D | DISP\_A3N
- 22 DISP\_A3P\_VGA >> C1561.2 | 0.1U 0402 10V6K-D | DISP\_A3P



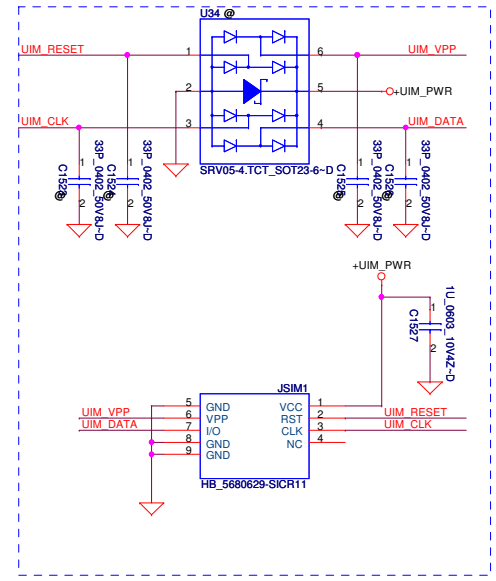
Security Classification	Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2009/07/25	Deciphered Date	2010/07/25	Title	
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# WWAN PCIE MiniCard

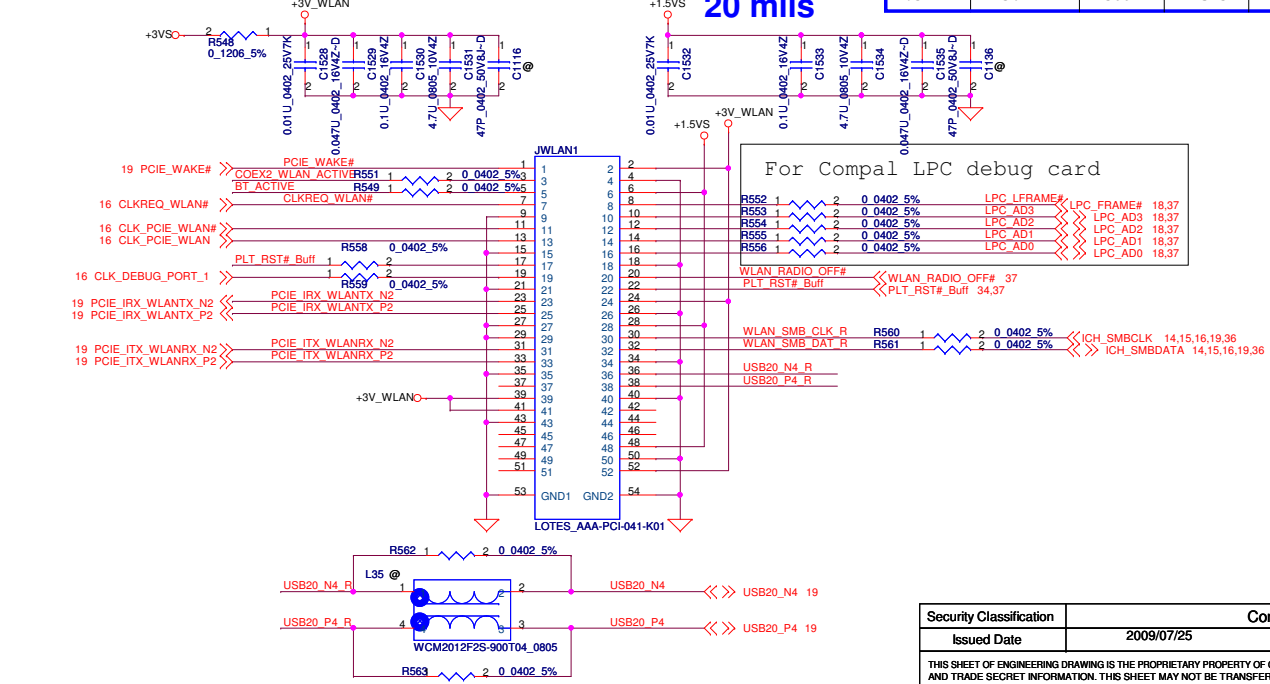


# SIM Card



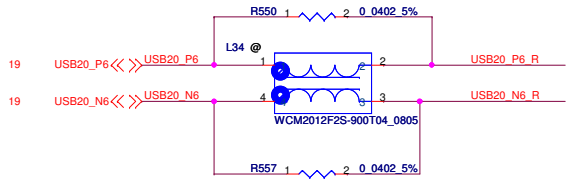
PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+/-9%	1000	750	
+3.3Vaux	+/-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+/-5%	500	375	NA

# 40 mils WLAN/WIMAX PCIE Mini Card

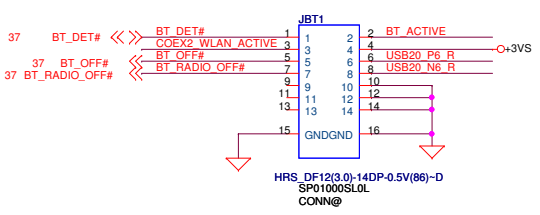


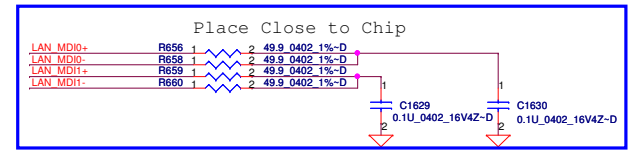
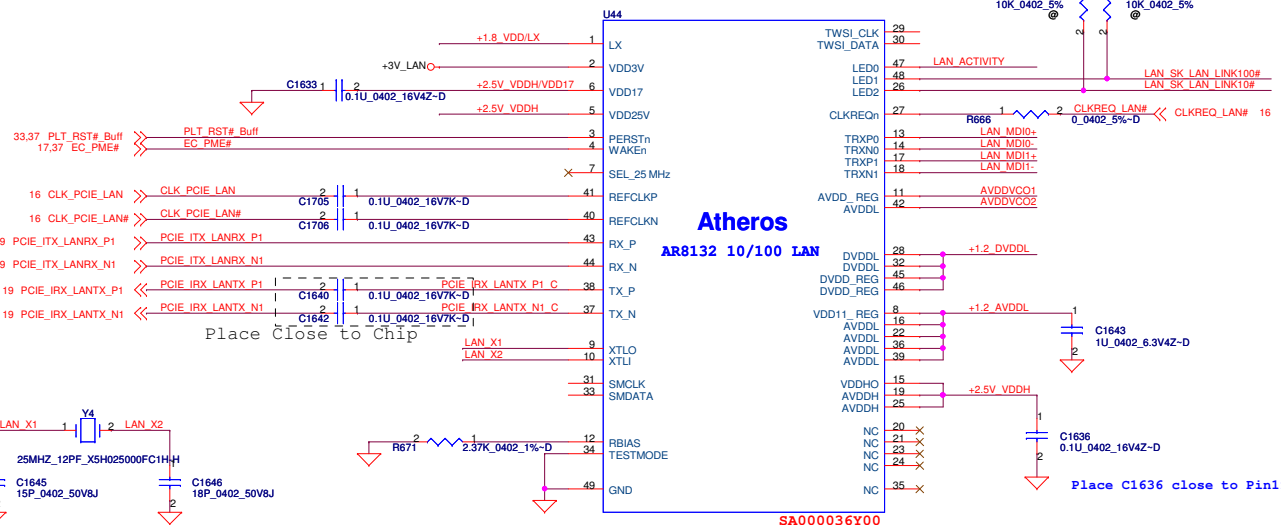
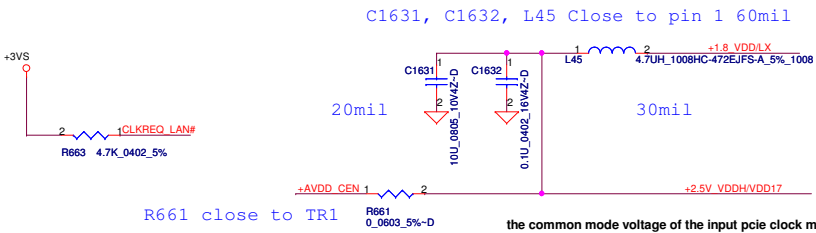
For Compal LPC debug card

R552 1	2	0.0402 5%	LPC_LFRFRAME#	LPC_FRAME# 18,37
R553 1	2	0.0402 5%	LPC_AD3	LPC_AD3 18,37
R554 1	2	0.0402 5%	LPC_AD2	LPC_AD2 18,37
R555 1	2	0.0402 5%	LPC_AD1	LPC_AD1 18,37
R556 1	2	0.0402 5%	LPC_AD0	LPC_AD0 18,37

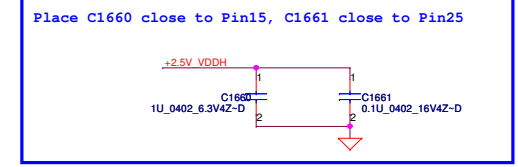
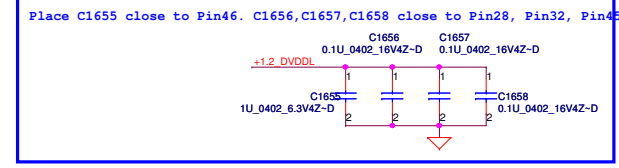
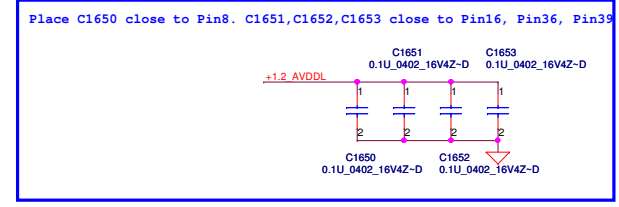
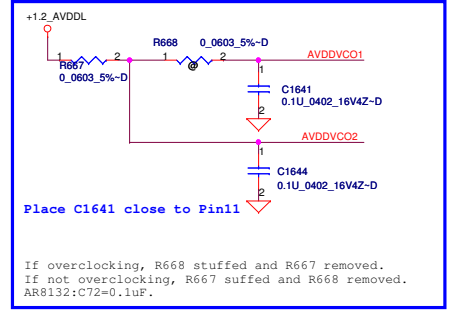
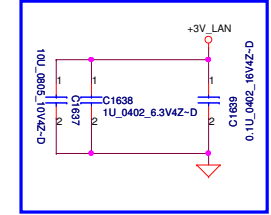


# Bluetooth

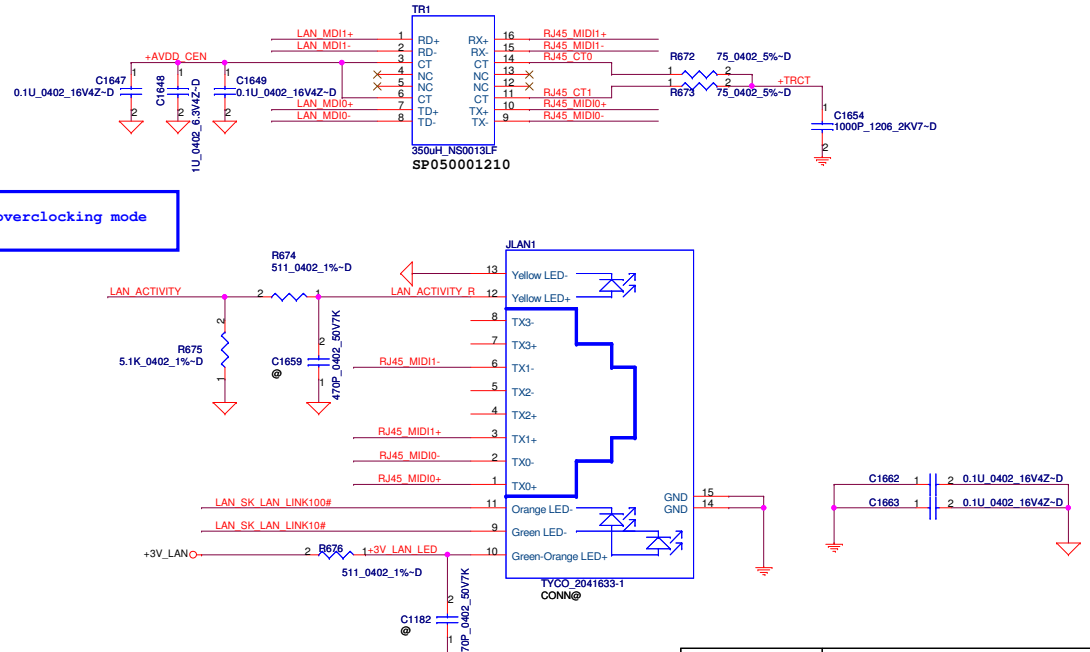




Layout Notice : Place as close chip as possible.

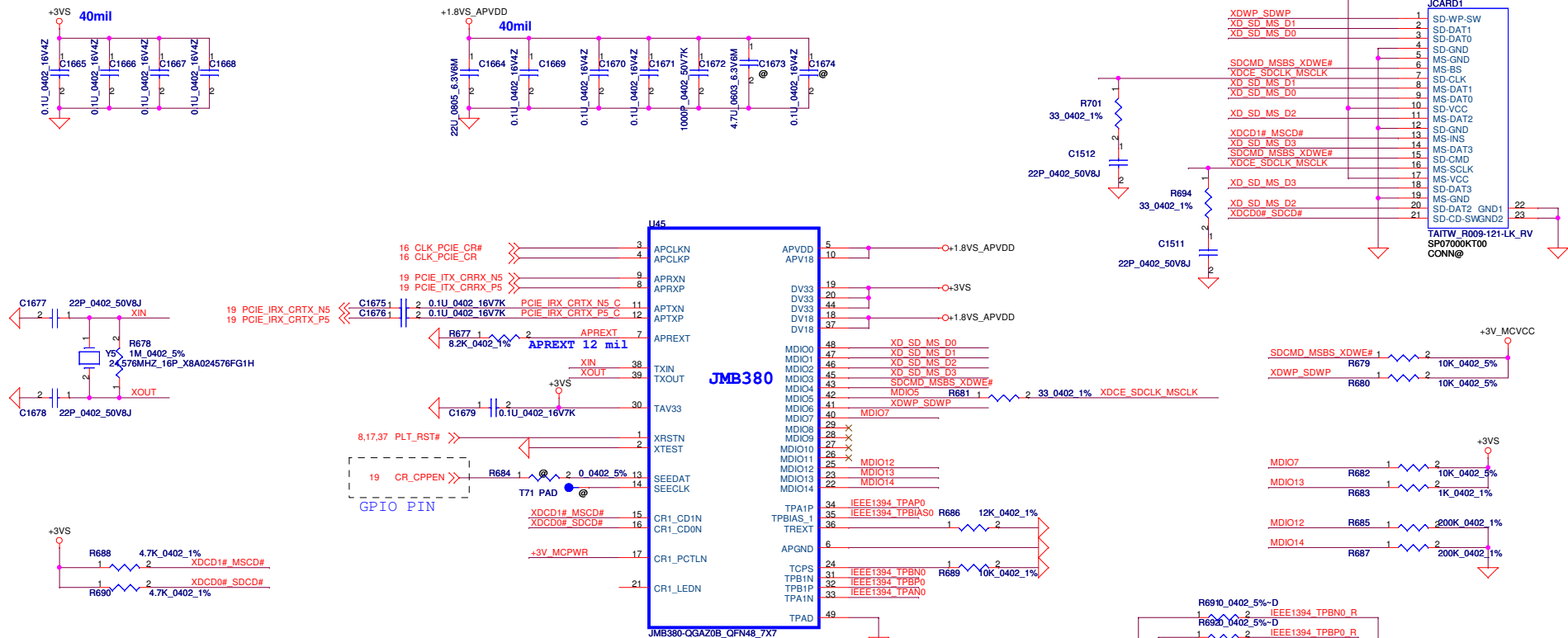


Pull down circuit:  
more power saving in no-overclocking mode  
vendor suggestion

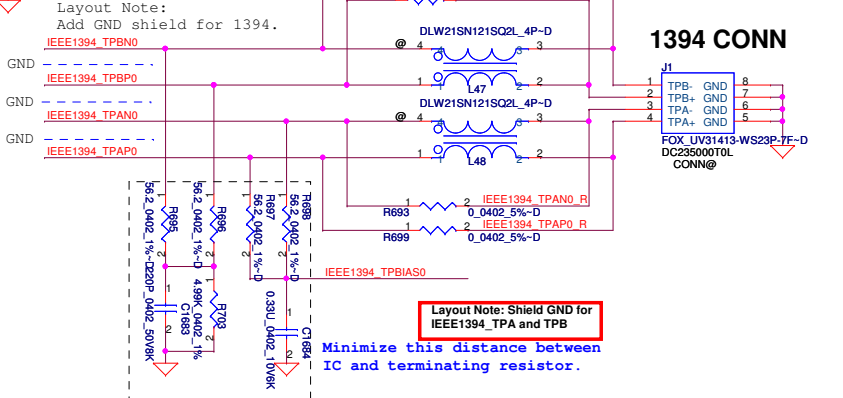
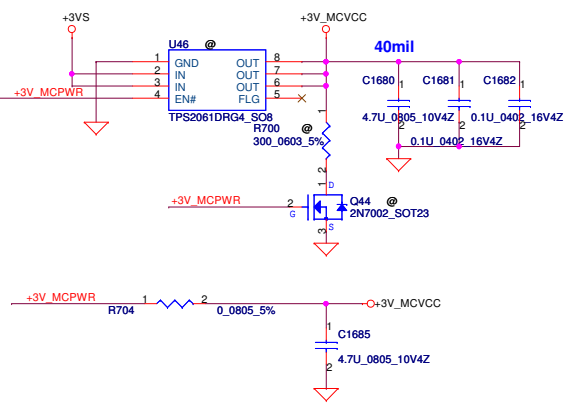


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### 3 in 1 Card Reader CONN



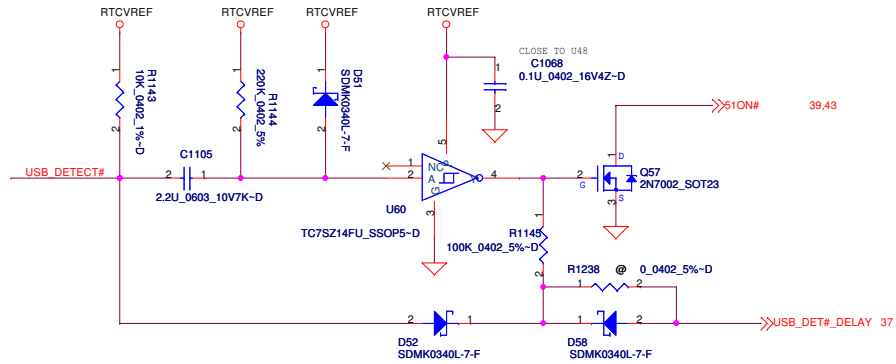
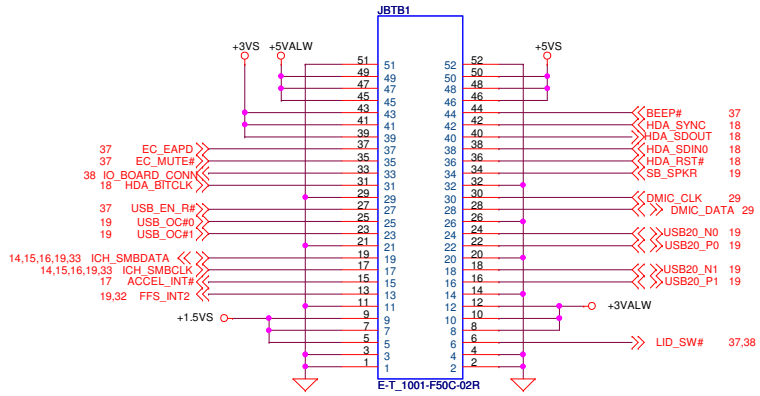
### Memory Card Power Switch



DELL CONFIDENTIAL/PROPRIETARY

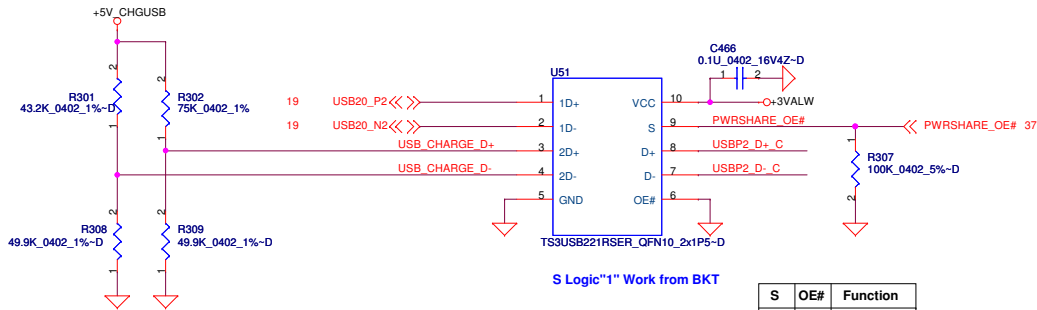
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Issued Date	2009/07/25	Deciphered Date	2010/07/25	Compal Electronics, Inc.	
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Size	Document Number	Date		Rev	
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			35	58	

# IO Board CONN

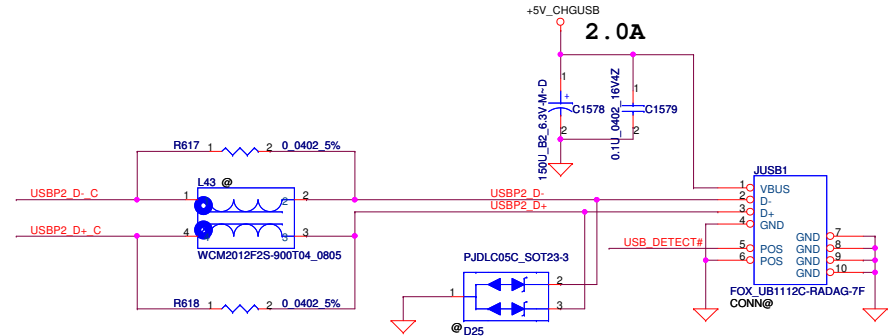


## Power share

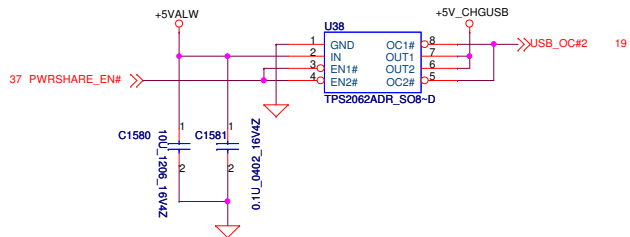
fix +3VALW leakage on Batt mode



S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D



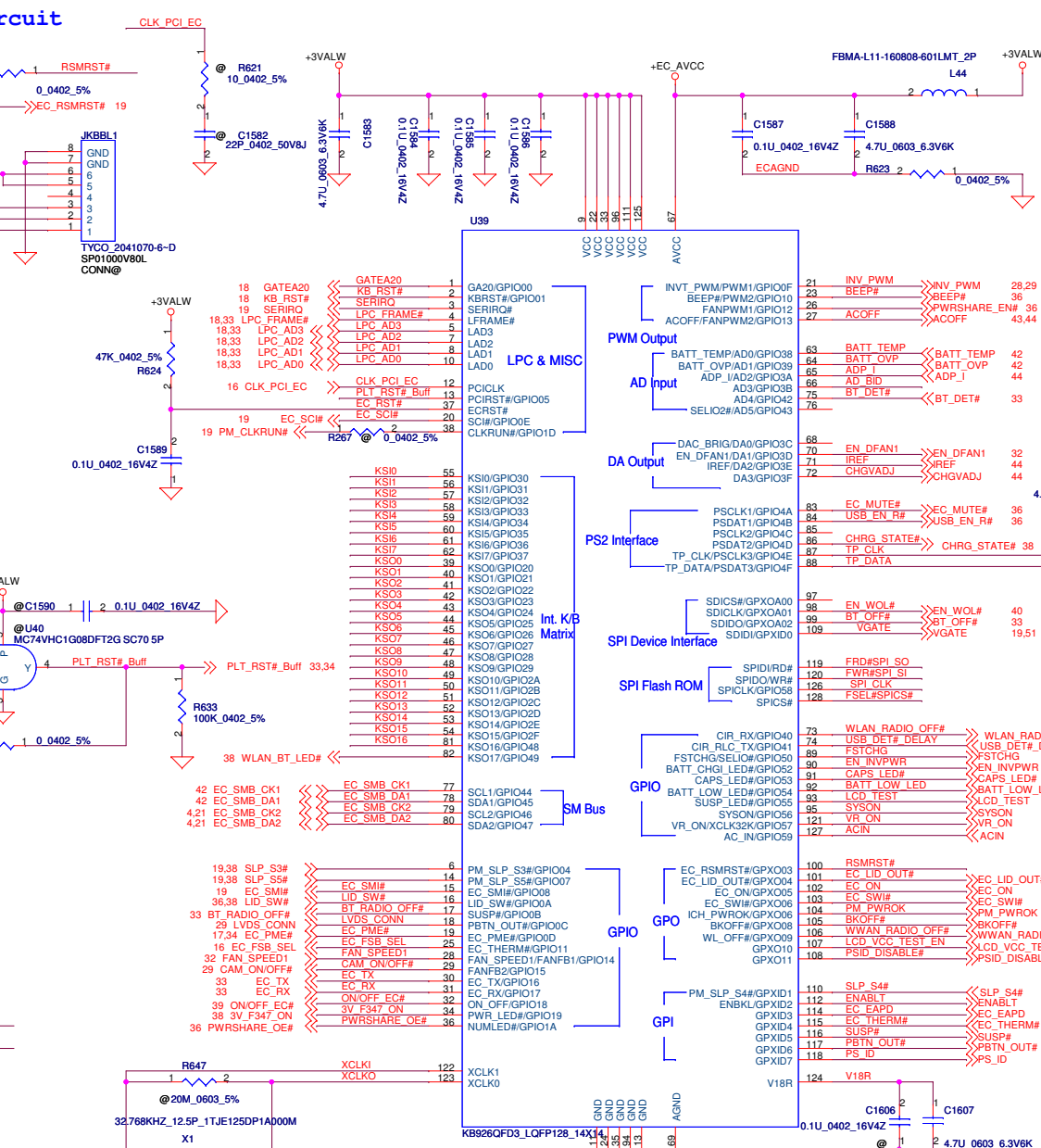
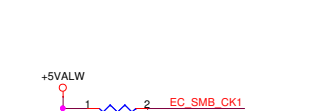
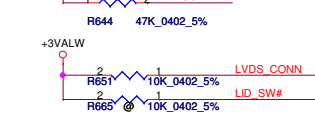
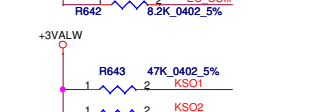
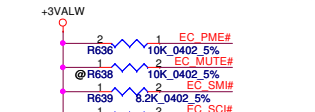
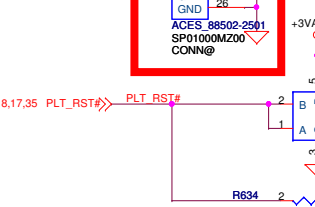
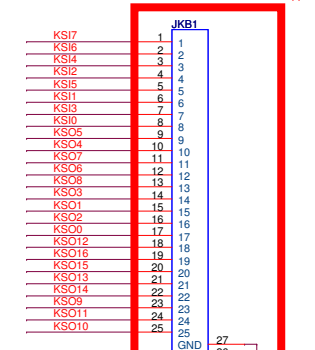
## 2.0A



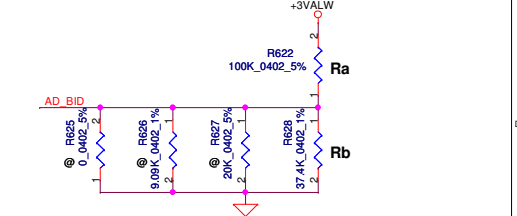
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# RSMRST circuit

## KEYBOARD CONN.



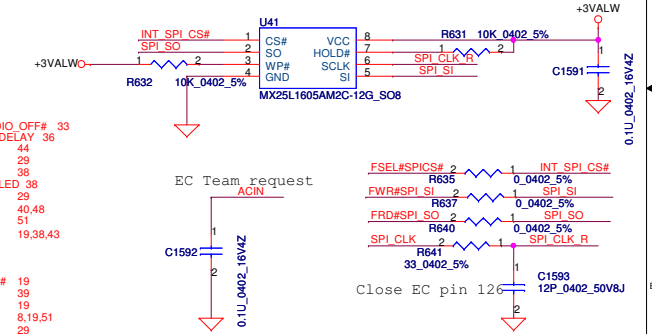
## Board ID



### BOARD ID Table

ID	BOARD ID	Ra	Rb	Vab
0	0.1(X00)	NC	0	0V
1	0.2(X01)	100K	9.09K	0.25V
2	0.3(X02)	100K	20K	0.50V
3	1.0(A00)	100K	37.4K	0.82V

## System SPI Flash ROM (16Mb)

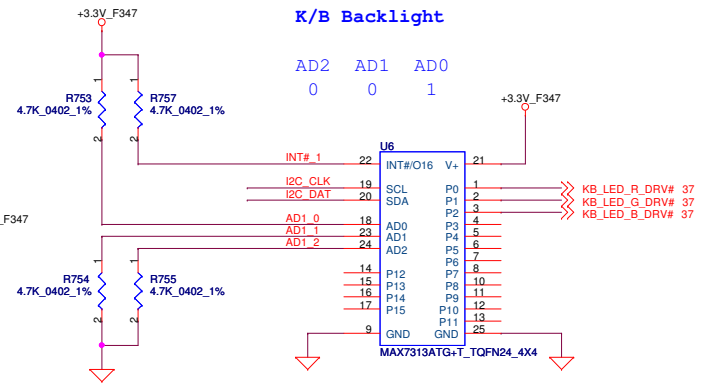
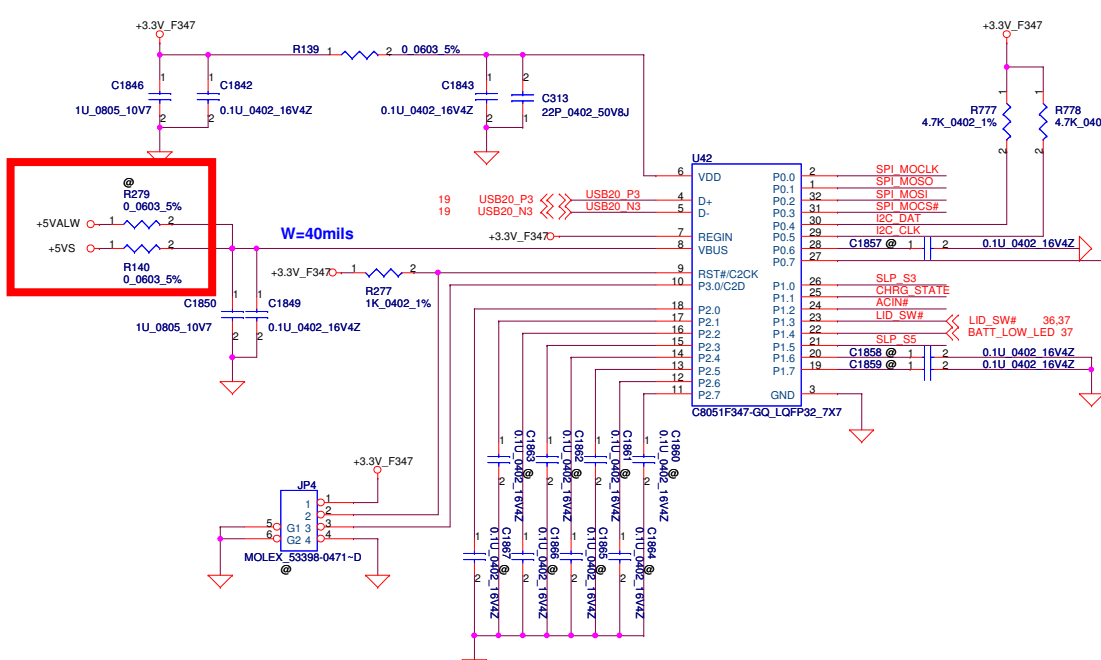


KSO8 @C1594	100P_0402_25V8K	100P_0402_25V8K	C1599	KSI7
KSI3 @C1596	100P_0402_25V8K	100P_0402_25V8K	C1599	KSI6
KSO9 @C1598	100P_0402_25V8K	100P_0402_25V8K	C1599	KSI5
KSI2 @C1600	100P_0402_25V8K	100P_0402_25V8K	C1600	KSO0
KSI1 @C1602	100P_0402_25V8K	100P_0402_25V8K	C1600	KSO1
KSO10 @C1604	100P_0402_25V8K	100P_0402_25V8K	C1600	KSO2
KSO11 @C1608	100P_0402_25V8K	100P_0402_25V8K	C1600	KSI4
KSI0 @C1611	100P_0402_25V8K	100P_0402_25V8K	C1610	KSO3
KSO12 @C1612	100P_0402_25V8K	100P_0402_25V8K	C1610	KSO4
KSO13 @C1614	100P_0402_25V8K	100P_0402_25V8K	C1610	KSO5
KSO14 @C1618	100P_0402_25V8K	100P_0402_25V8K	C1610	KSO6
KSO15 @C1620	100P_0402_25V8K	100P_0402_25V8K	C1620	KSO7
KSO16 @C1622	100P_0402_25V8K	100P_0402_25V8K	C1620	

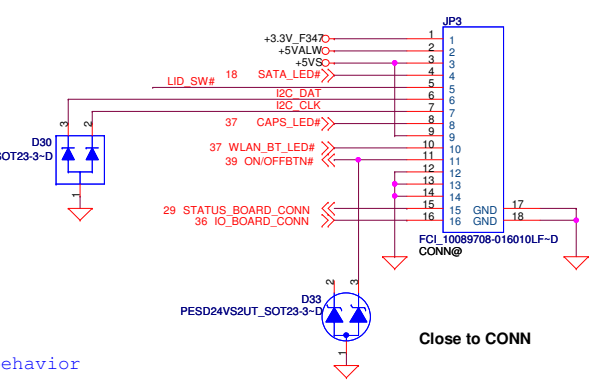
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Issued Date	2009/07/25	Deciphered Date
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Title		
<b>Compal Electronics, Inc.</b>		
<b>EC/KB CONN</b>		
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**Status Board CONN**



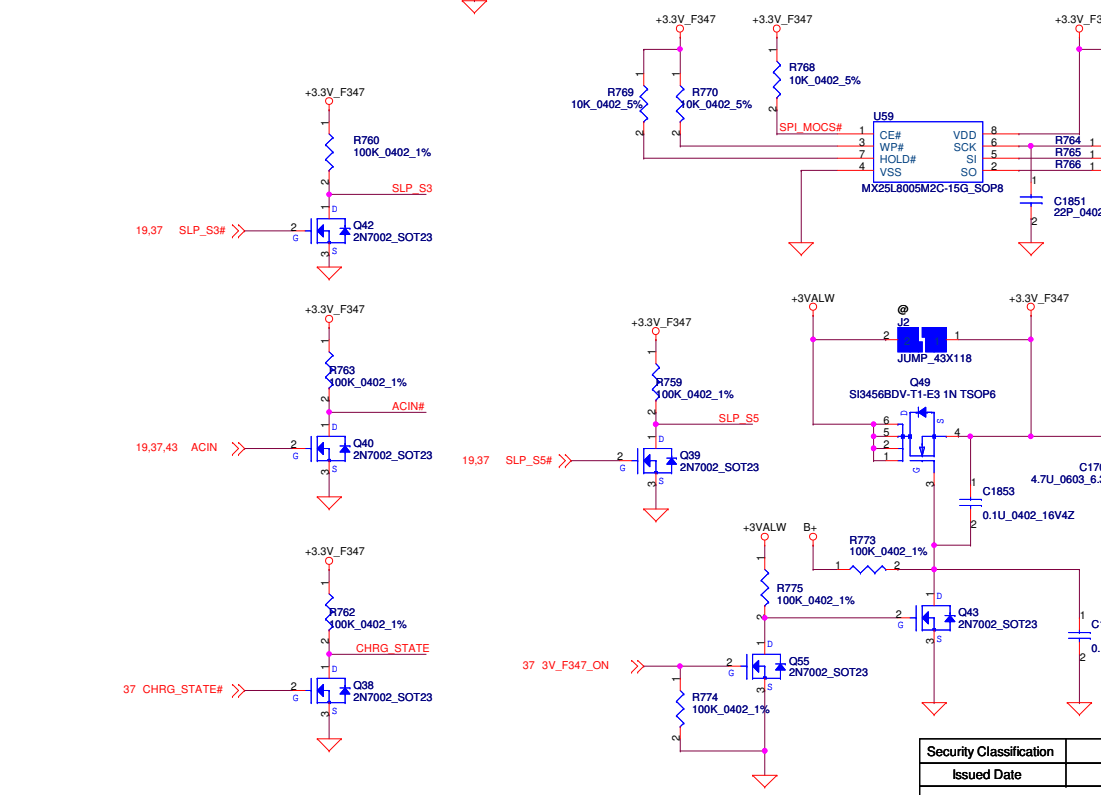
+3.3V\_F347 behavior

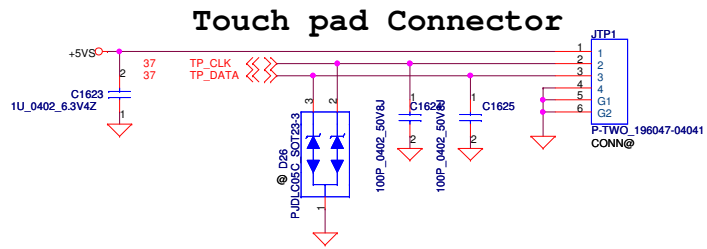
	STATE			
	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BAT only	ON	ON	OFF	OFF

DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b

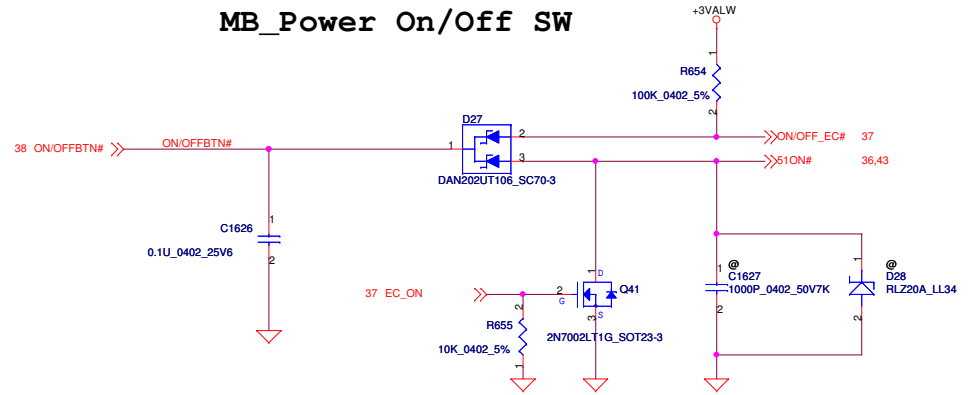
AC mode battery full in S5:turn off ELC controller

Reference	AD2	AD1	AD0	MAX7313
DB	0	1	0	L/R Headlight , Logo
DB	0	1	1	CAP , Wireless Power Button , Eyes/Rim
U6	0	0	1	K/B Backlight

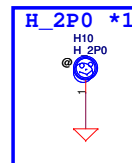
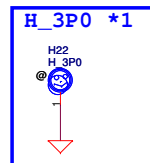
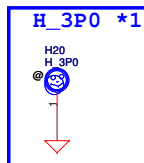
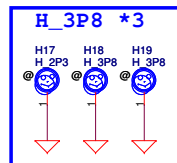
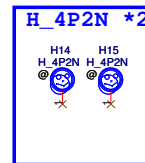
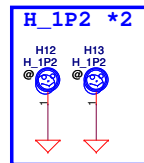
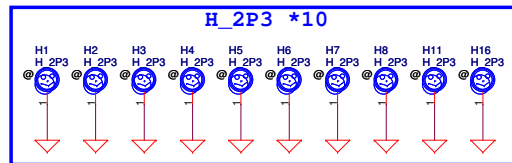
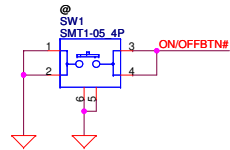




### MB\_Power On/Off SW

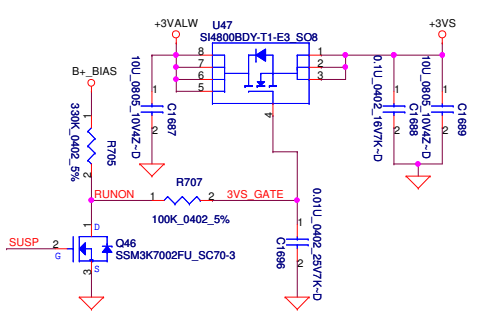


### For Debug Only

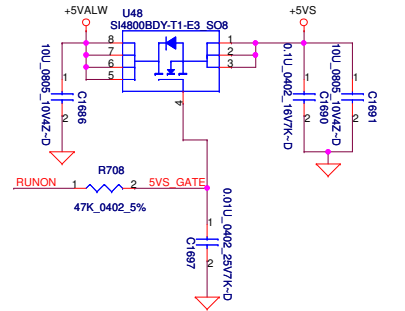


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				Custom	LA-5811P	1.0
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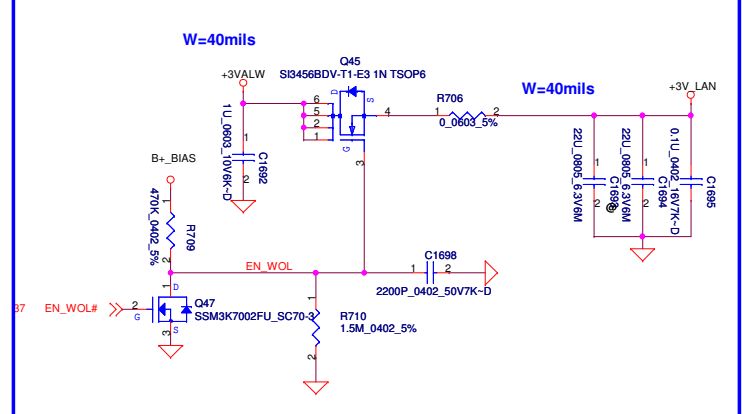
### +3VALW to +3VS Transfer



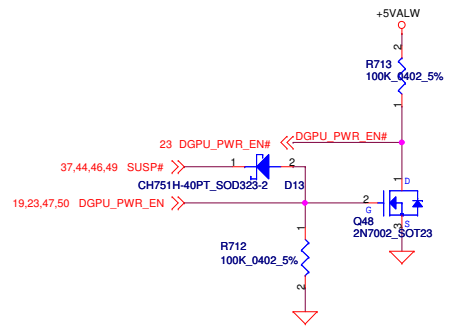
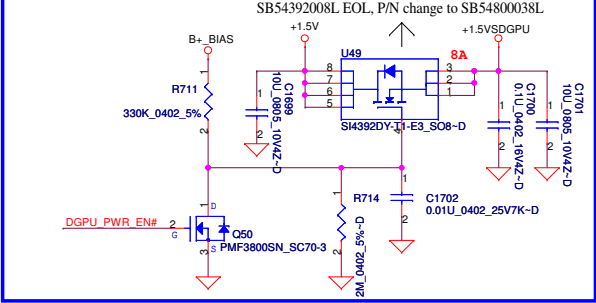
### +5VALW to +5VS Transfer



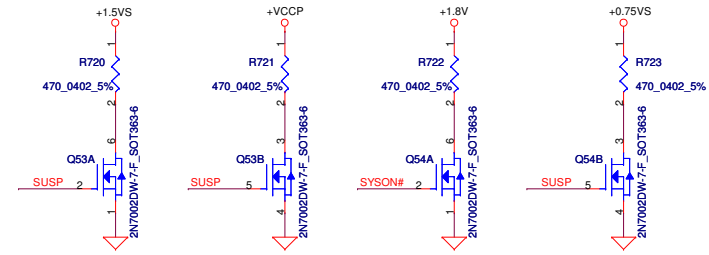
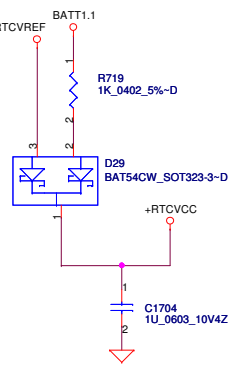
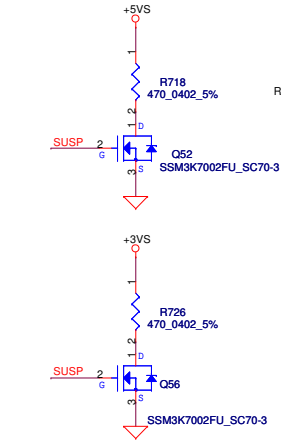
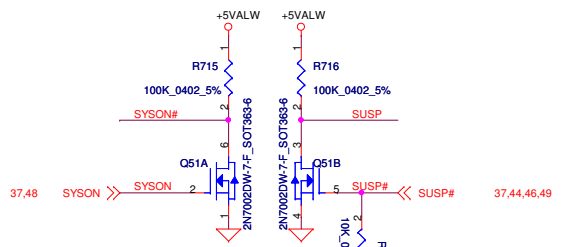
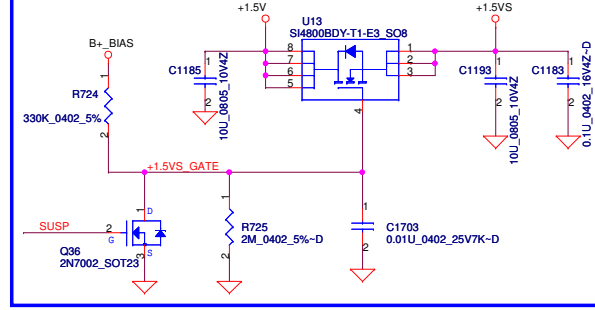
### +3VALW to +3LAN Transfer



### +1.5V to +1.5VSDGPU Transfer



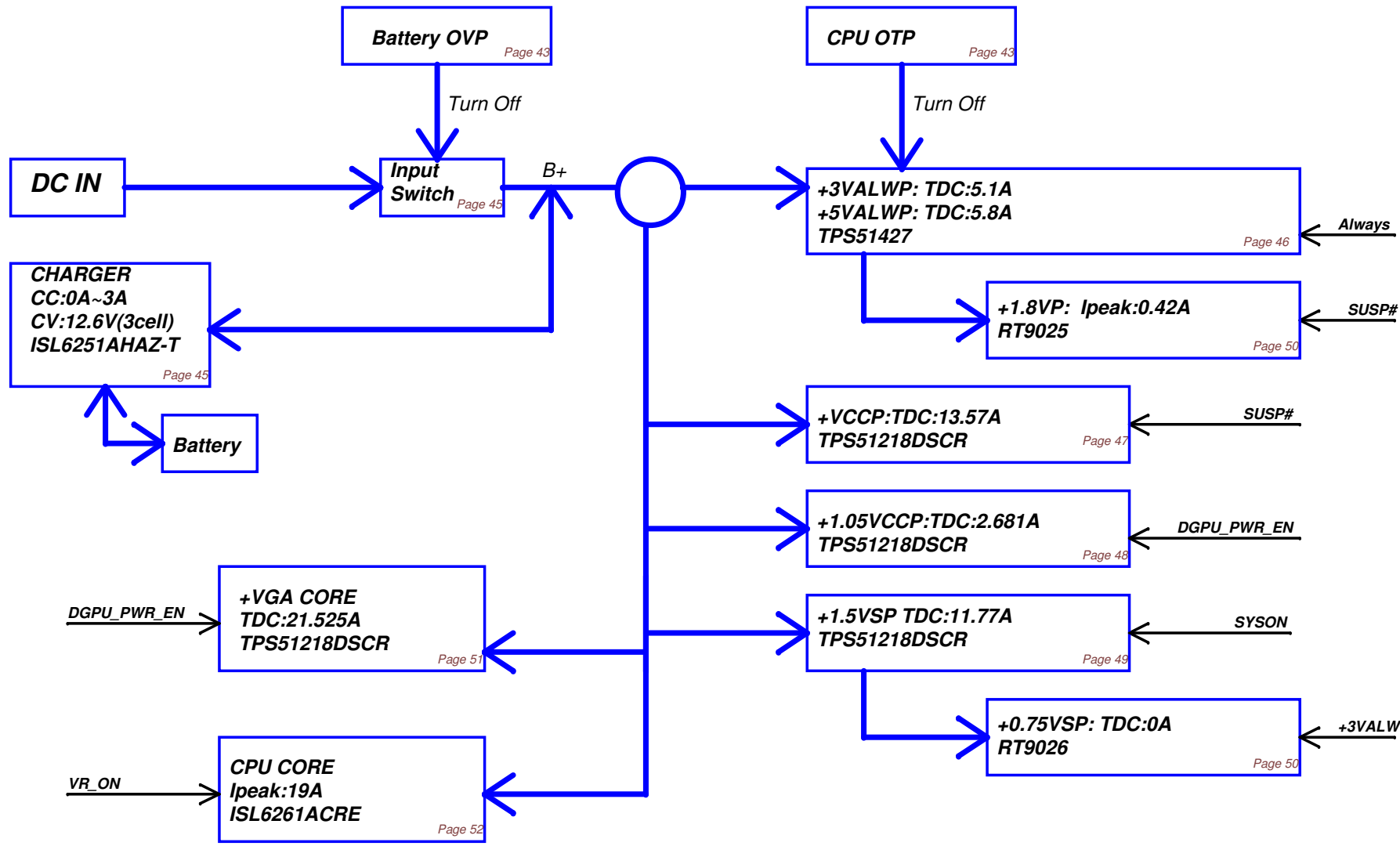
### +1.5V to +1.5VS Transfer



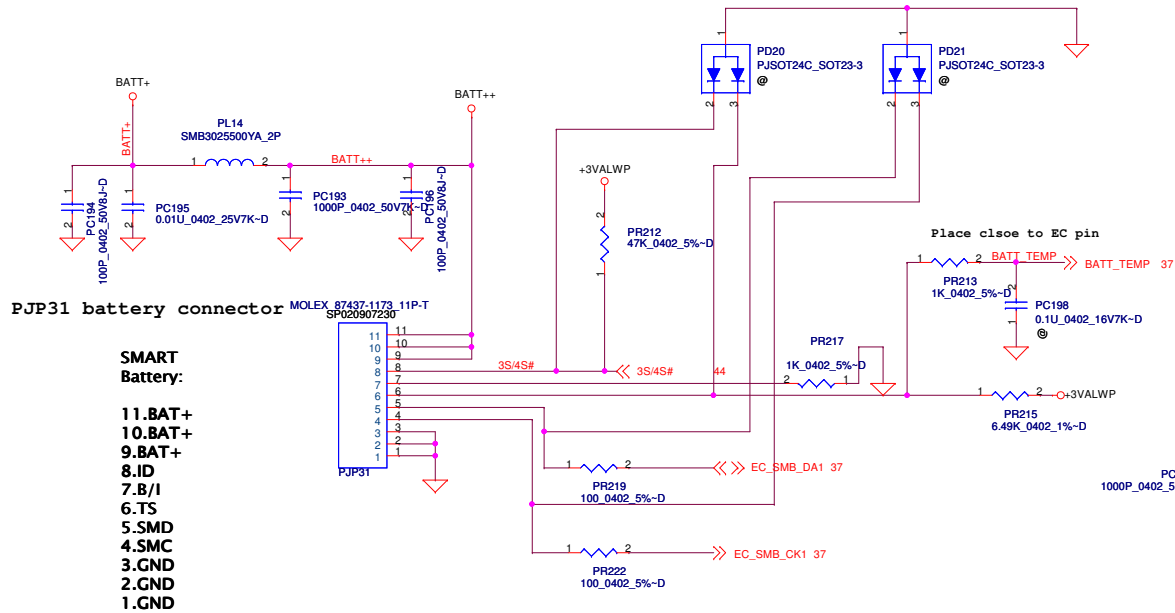
Security Classification	Compal Secret Data			Title	
Issued Date	2009/07/25	Deciphered Date	2010/07/25	DC/DC INTERFACE	
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				Custom	1.0
				Date:	Tuesday, December 29, 2009   Sheet 40 of 58



# Power block

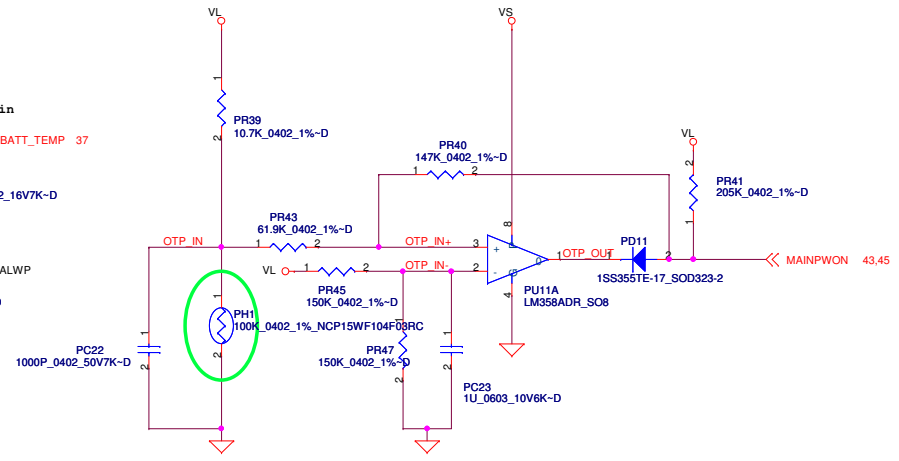


Title		
POWER BLOCK DIAGRAM		
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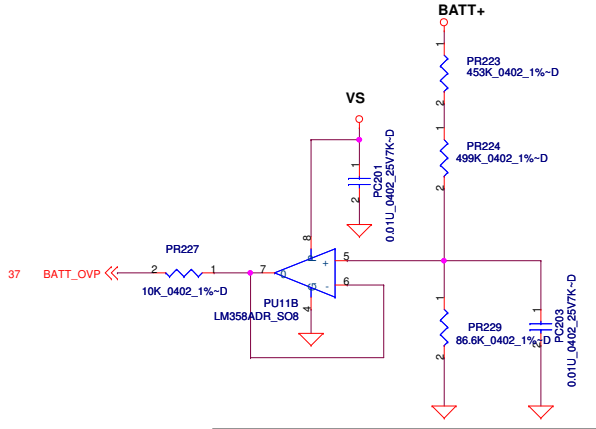
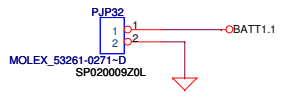
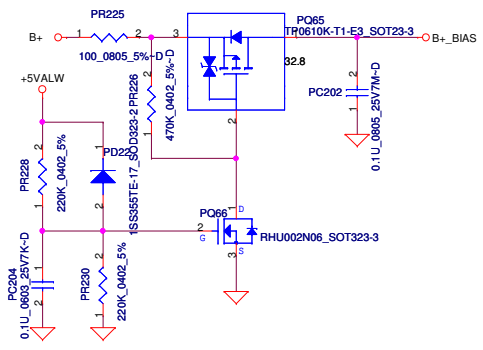


CPU OTP

**PH1 under CPU botten side :**  
 CPU thermal protection at 90 +/-3 degree C  
 Recovery at 50 +/-3 degree C

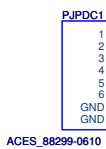


COIN RTC Battery

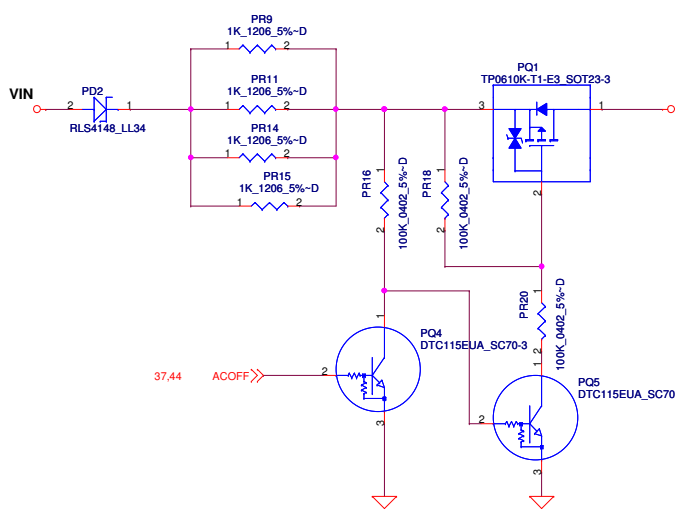
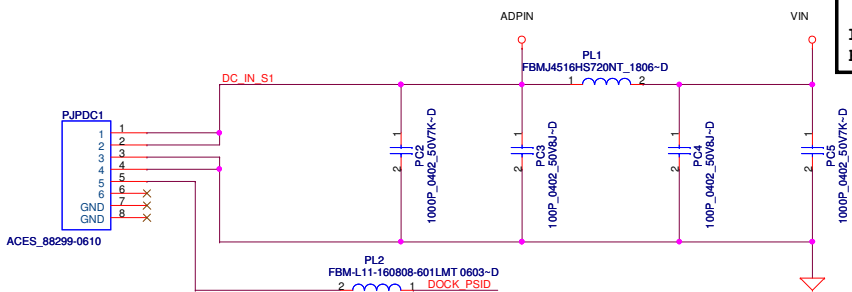


**LI-3S : 13.5V----BATT-OVP=1.126V**  
**LI-4S : 18V----BATT-OVP=1.5V**  
**BATT-OVP=0.08338\*BATT+**

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Issued Date		Deciphered Date		Title	BATTERY CONN/OTP	
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				Date:	Tuesday, December 29, 2009	Sheet 42 of 58

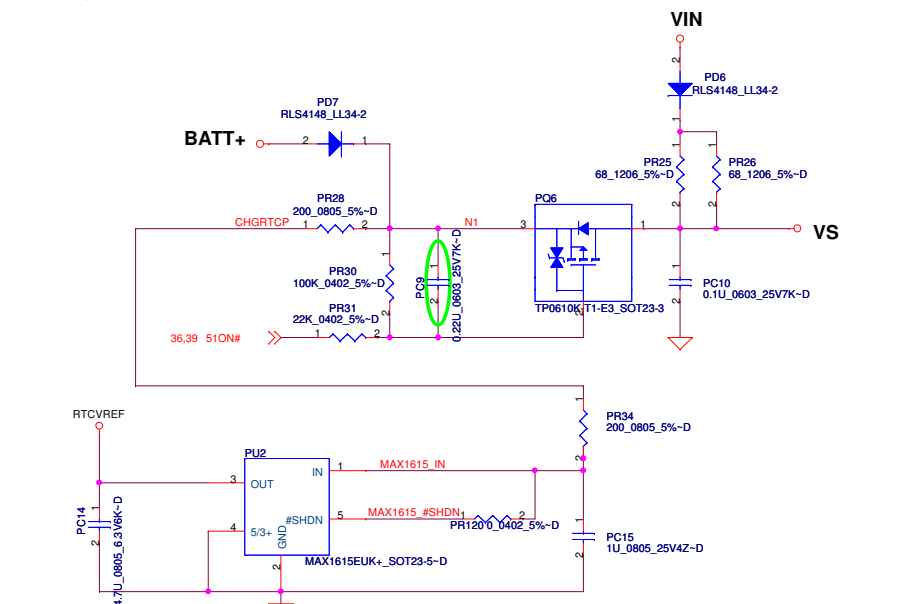
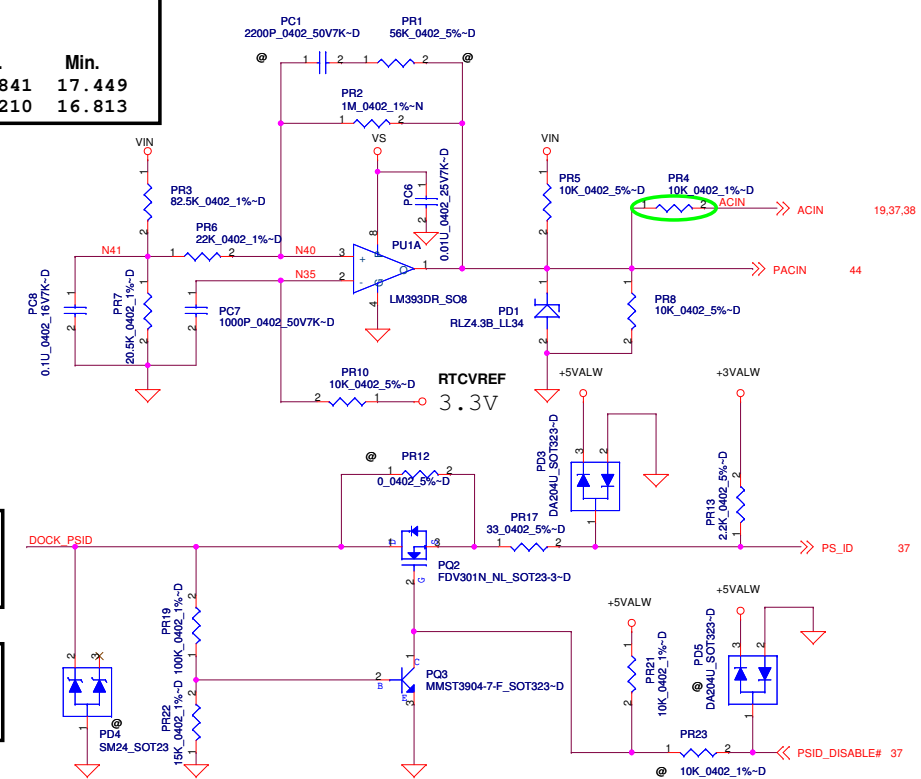
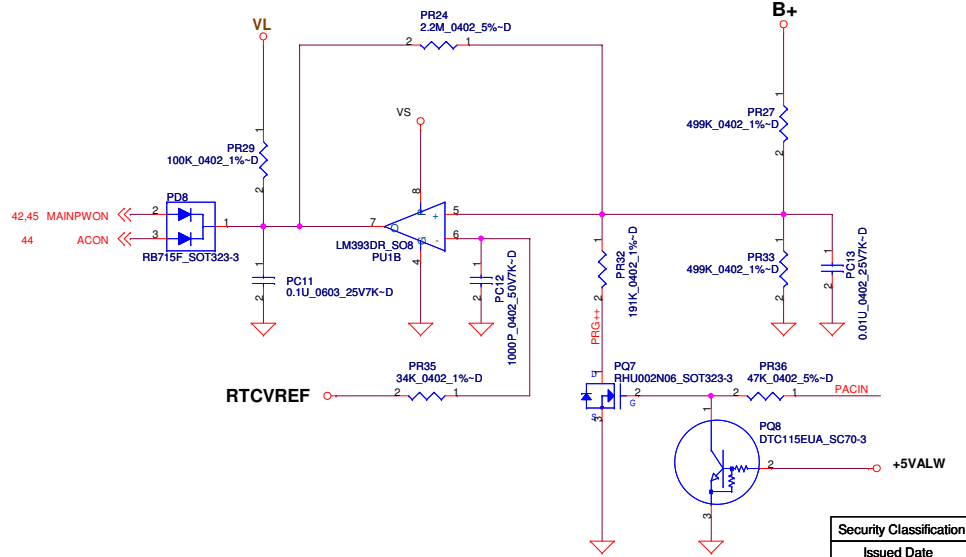


Vin Detector			
	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813



ACIN Precharge detector			
	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

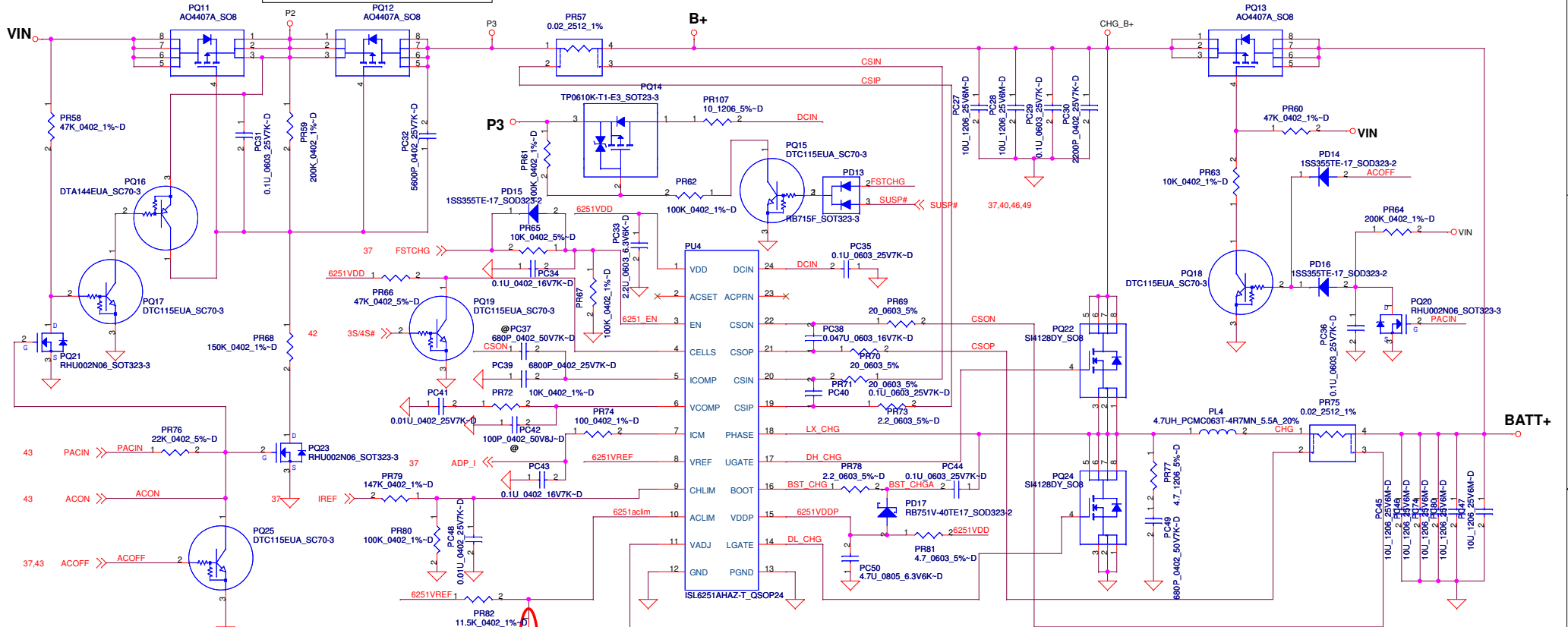
BATT ONLY Precharge detector			
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V



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Iada=0~3.333A (65W)

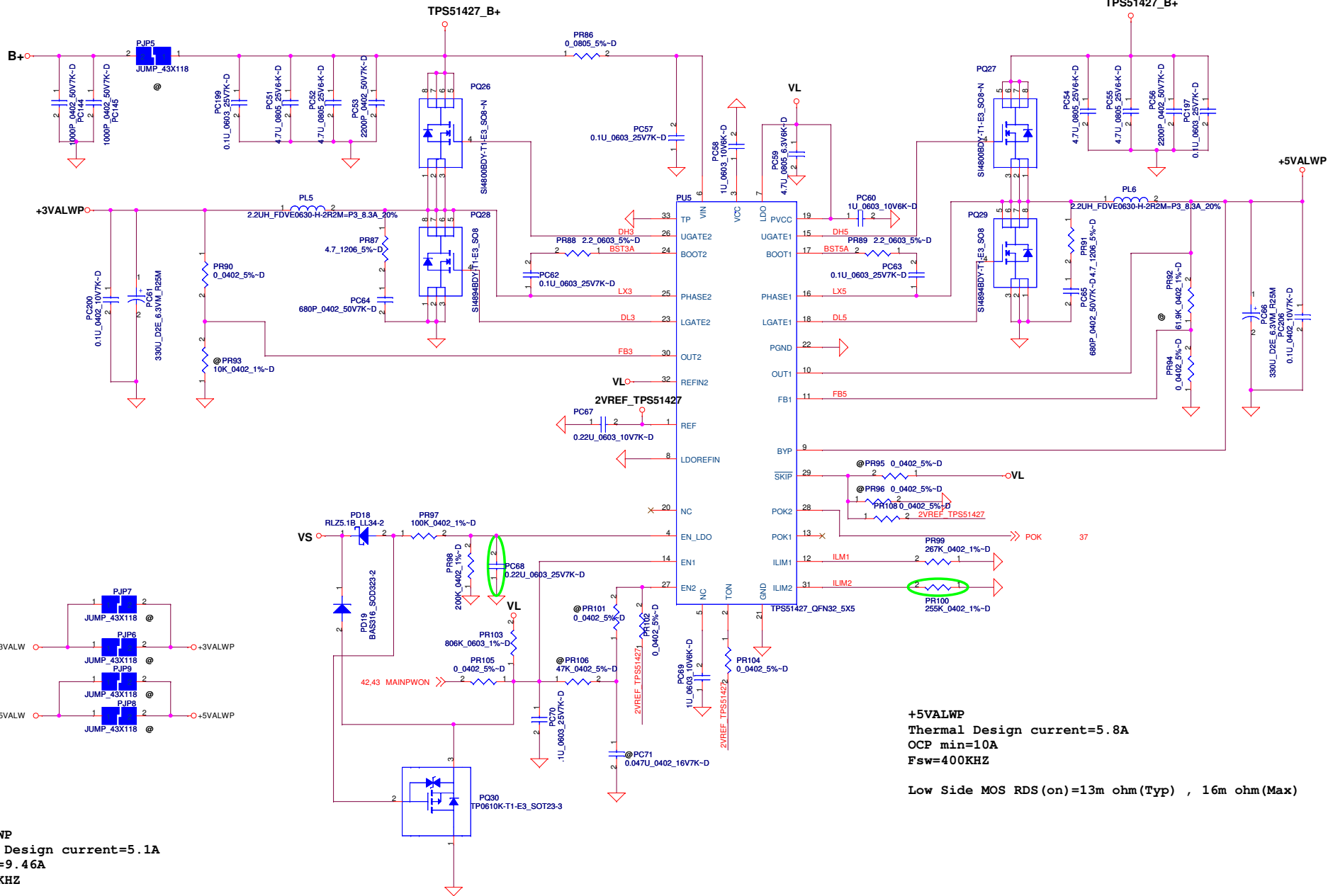
$$ADP\_I = 19.5 * I_{adapter} * R_{sense}$$



CP mode  
 $I_{input} = (1/0.02) * ((0.05 * V_{acLim}) / 2.39 + 0.05)$   
 $V_{acLim} = 2.87 * ((11.5K / 152K) / ((2.87K / 152K) + (11.5K / 152K)))$

CC=3.3A  
 IREF=1\*Icharge  
 IREF=0.25V~3.3V

CHGVADJ	CV mode
0V	3.99V per cell
1.93V	4.2V per cell
3.3V	4.35V per cell



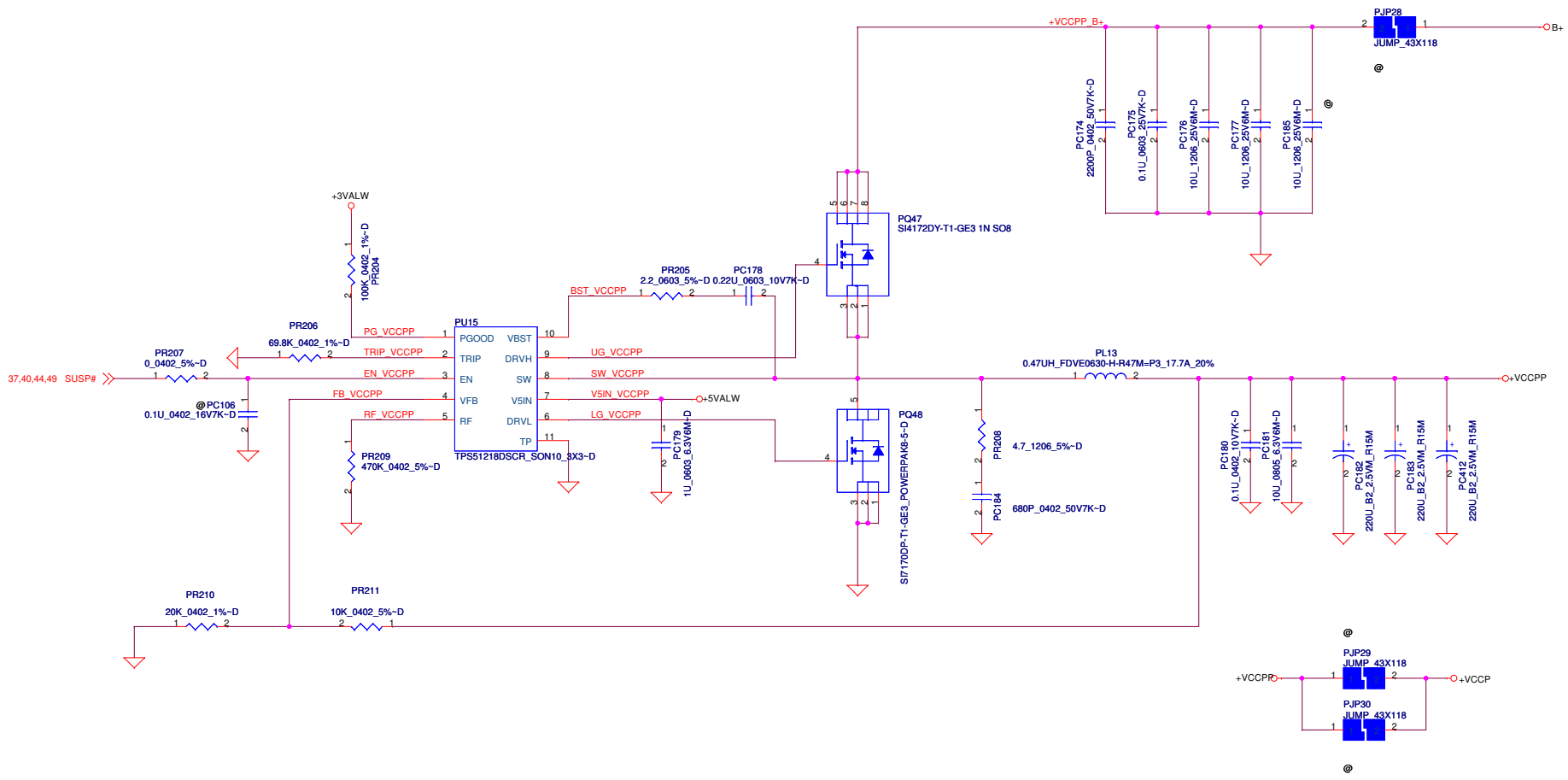
**+3.3VALWP**  
 Thermal Design current=5.1A  
 OCP min=9.46A  
 Fsw=300KHZ

Low Side MOS RDS (on)=13m ohm(Typ) , 16m ohm(Max)

**+5VALWP**  
 Thermal Design current=5.8A  
 OCP min=10A  
 Fsw=400KHZ

Low Side MOS RDS (on)=13m ohm(Typ) , 16m ohm(Max)

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Size	Document Number	Rev		Date: Tuesday, December 29, 2009		
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**+VCCPP**  
 Thermal Design current=13.57A  
 OCPmin=25.2A  
 Fsw=290KHZ

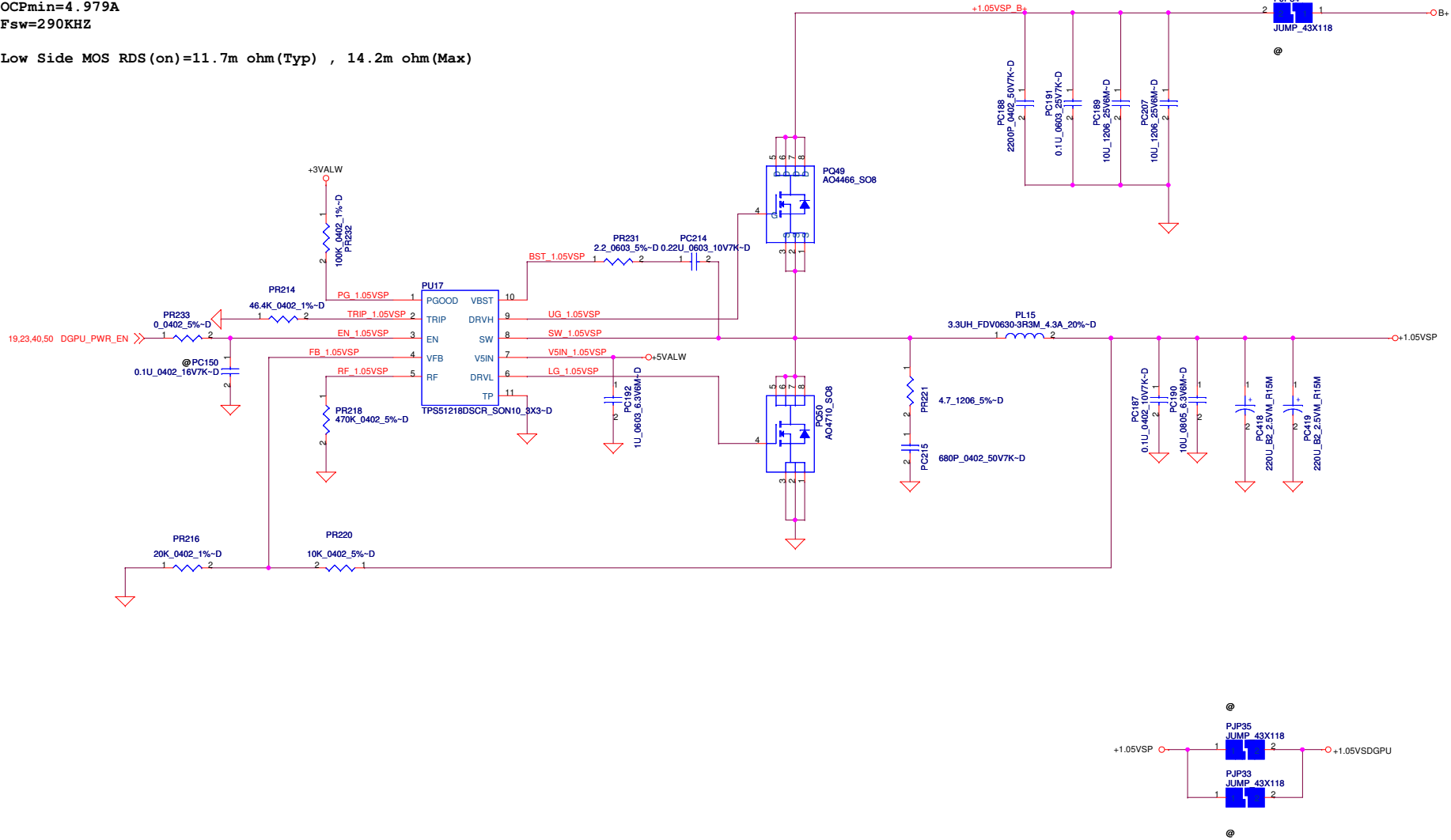
Low Side MOS RDS (on)=3.6m ohm(Typ) , 4.5m ohm(Max)

+VCCPP

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				Custom		
				Date:	Tuesday, December 29, 2009	Sheet 46 of 58

+1.05VSP  
 Thermal Design current=2.681A  
 OCPmin=4.979A  
 Fsw=290KHZ

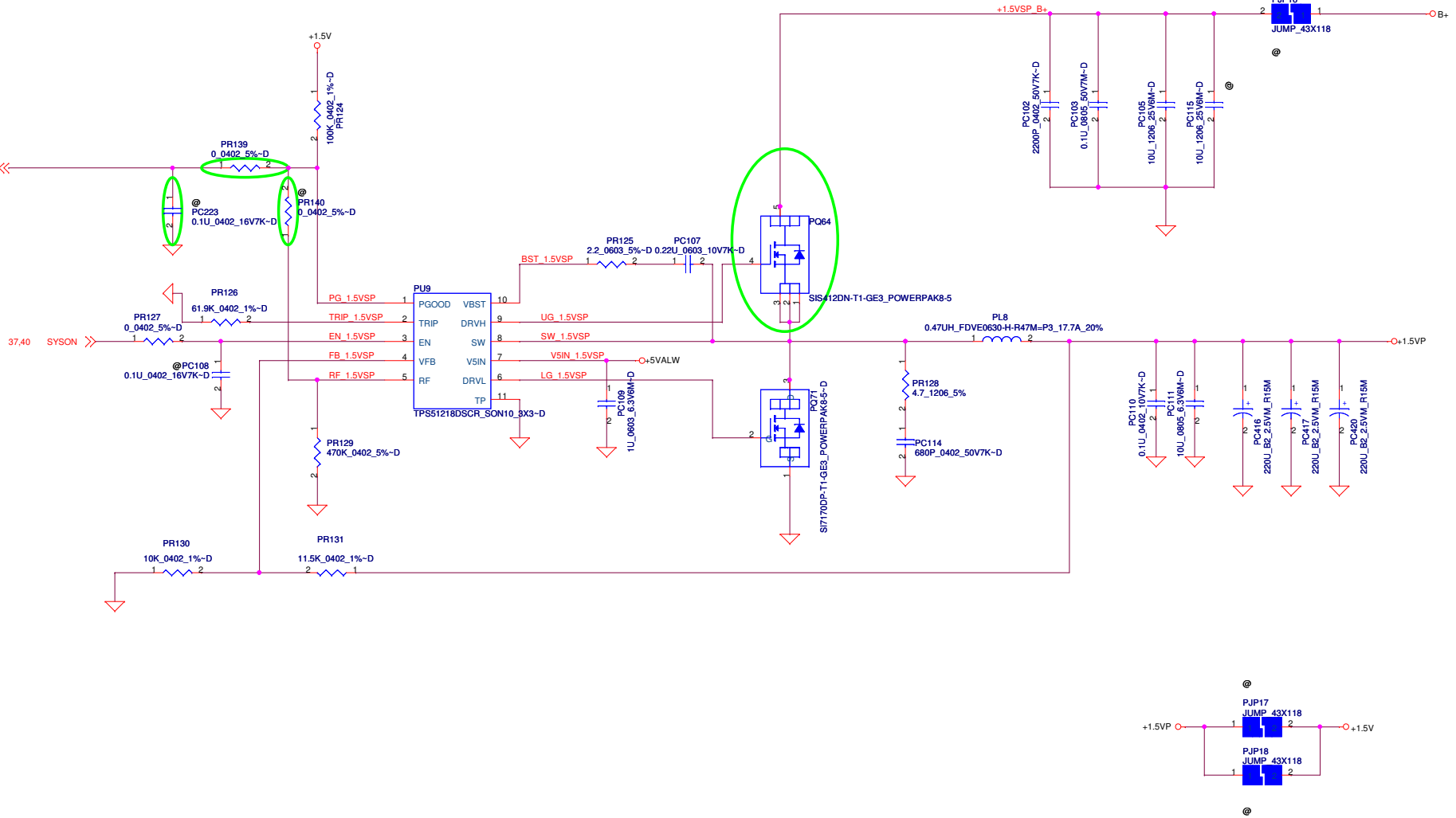
Low Side MOS RDS(on)=11.7m ohm(Typ) , 14.2m ohm(Max)



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				Custom	1.05VSP	
				Date:	Tuesday, December 29, 2009	Sheet 47 of 58

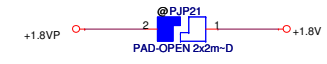
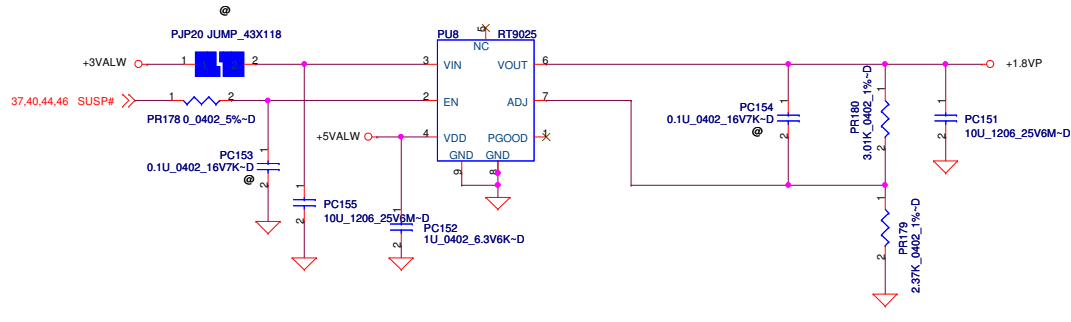
+1.5VSP  
 Thermal Design current=11.77A  
 OCPmin=21.85A  
 Fsw=290KHZ

Low Side MOS RDS(on)=3.6m ohm(Typ) , 4.5m ohm(Max)

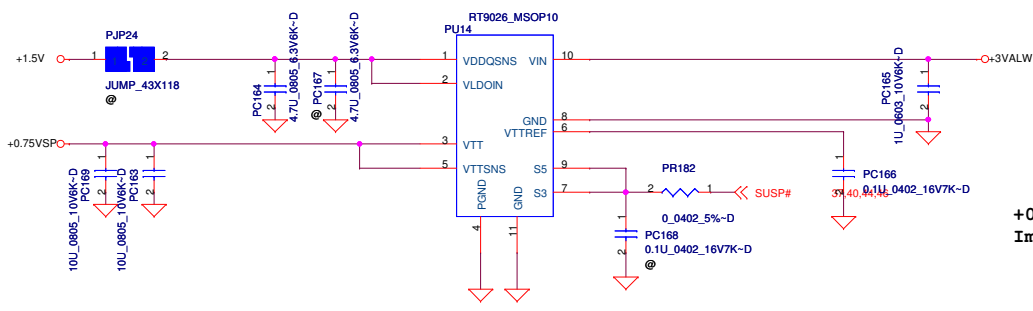


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Issued Date		Deciphered Date		Title <b>+1.5VSP</b>		
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**+1.8VSP**  
**Imax=0.42A**



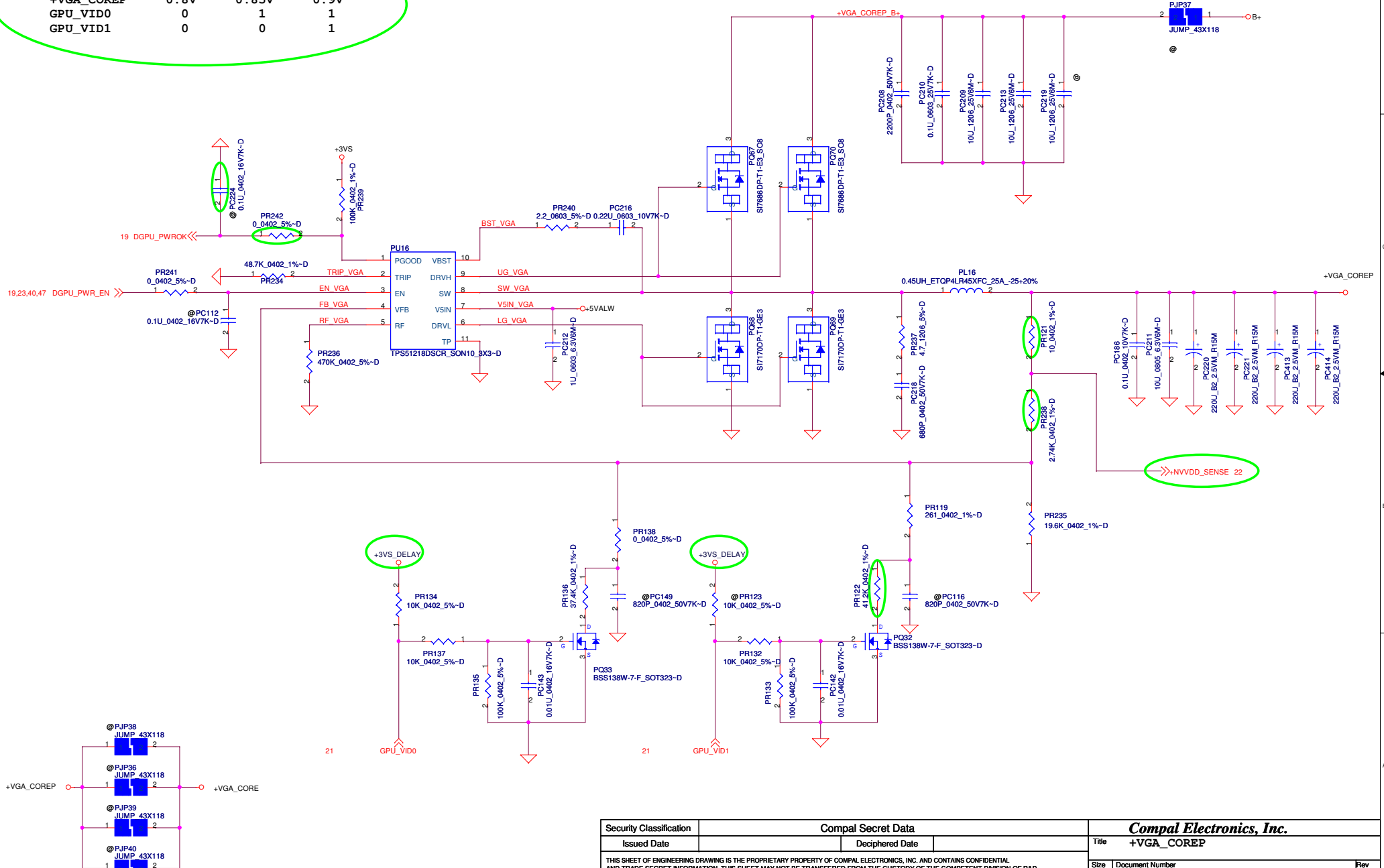
**+0.75VSP**  
**Imax=0A**

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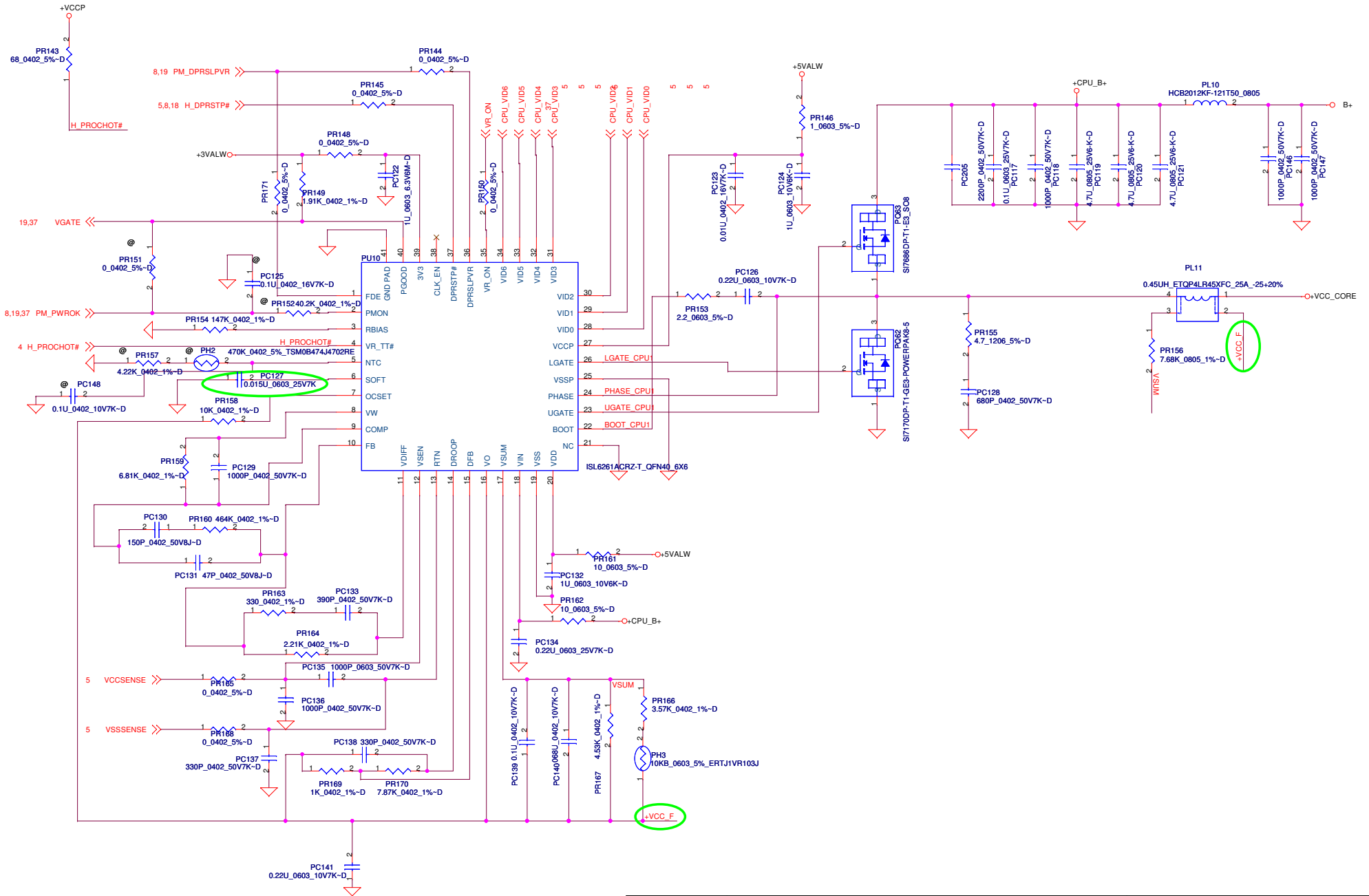
+VGA\_COREP  
 ThermalDesigncurrent=21.525A  
 OCPmin=36.9A  
 Fsw=290KHZ  
 Low Side MOS RDS(on)=1.8m ohm(Typ) , 2.25m ohm(Max)

+VGA\_COREP (N10P\_GS1) PR122=41.2K ohm

+VGA_COREP	0.8V	0.85V	0.9V
GPU_VID0	0	1	1
GPU_VID1	0	0	1



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Issued Date	Deciphered Date	+VGA_COREP		Size
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Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>CPU_CORE</b>		
Issued Date		Deciphered Date				
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				Custom		
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	50	VGA_COREP	8/17	Antony	Change output voltage	Change PR119 from SD0280008L(0 ohm) to SD03426108L(261 ohm)	X00
2	50	VGA_COREP	8/17	Antony	Change output voltage	Change PR122 from SD03424928L(24.9K ohm) to SD03419128L(19.1K ohm)	X00
3	50	VGA_COREP	8/17	Antony	Change output voltage	Change PR136 from SD03437428L(37.4K ohm) to SD03440228L(40.2K ohm)	X00
4	50	VGA_COREP	8/17	Antony	Change output voltage	Change PR238 from SD00000AP8L(2.67K ohm) to SD03427418L(2.74K ohm)	X00
5	50	VGA_COREP	8/17	Antony	Output voltage setting 0.85V (NVIDIA request)	non-populate PR123(reserve space)	X00
6	44	CHARGER	9/10	Antony	CP point 90% setting	Change PR83 from 2.87K ohm to 2.74K ohm	X01
7	44	CHARGER	9/10	Antony	Charger voltage setting	Change PR85 from 200K ohm to 43.2K ohm	X01
8	48	+1.5VSP	9/16	Antony	EE required that SM_PWROK should change to +1.5V	Change net name PR124.1 from +3VALW to +1.5V	X01
9	50	VGA_COREP	9/16	Antony	Change VID time sequence	Change net name PR134.2 and PR123.2 from +3VS to +3VS_DELAY	X01
10	50	VGA_COREP	9/16	Antony	NVIDIA command	interchange with PR121 and PR238	X01
11	50	VGA_COREP	9/16	Antony	NVIDIA command	Delete PR139, +NVVDD_SENCE connect to PR121.2	X01
12	50	VGA_COREP	9/16	Antony	NVIDIA command	Change PR121 from 0 ohm to 10 ohm	X01
13	50	VGA_COREP	9/24	Antony	NVIDIA command	Change PR121 from 19.1K ohm to 41.2K ohm	X01
14	45	3VALWP/5VALWP	9/24	Antony	follow PSL component	Change PD19 from CH355PT to BAS316	X01
15	51	CPU_CORE	9/24	Antony	follow PSL component	Change PC127 to PSL component	X01

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<b>Compal Electronics, Inc.</b>			
<b>Title</b>			
<b>PWR-PIR1</b>			
<b>Size</b>	<b>Document Number</b>		<b>Rev</b>
			<b>1.0</b>
<b>Date:</b> Tuesday, December 29, 2009		<b>Sheet</b> 52	<b>of</b> 58

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
16	46	+VCCPP	9/24	Antony	Change PN to 0 end	Change PQ48 from SB00000FO0L to SB00000FO00	X01
17	48	+1.5VP	9/24	Antony	Change PN to 0 end	Change PQ48 from SB00000FO0L to SB00000FO00	X01
18	50	VGA_COREP	10/1	Antony	EE required that PU16.1 pull high should change to +3VS	Change net name PR239.1 from +3VALW to +3VS	X01
19	48	+1.5VP	10/5	Antony	EMC request	Reserve PC223 space	X01
20	44	CHARGER	10/5	Antony	Quality enhancement	Reserve PQ22 from A04466 to SI4128DY	X01
21	44	CHARGER	10/5	Antony	Quality enhancement	Reserve PQ24 from A04466 to SI4128DY	X01
22	42	BATTERY CONN/OTP	11/13	Antony	OTP meet setting	Change PH1 100K ohm thermistor	X02
23	43	DCIN/DETECTOR	11/13	Antony	Change component size	Change PC9 to size 0603	X03
24	45	+5VALWP/+3VALWP	11/13	Antony	Change component size	Change PC68 to size 0603	X03
25	45	+5VALWP/+3VALWP	11/13	Antony	The quality improvement suggests by PCP	Change PR100 to 255K ohm	X03
26	48	+1.5VSP	11/13	Antony	Reserve 0 ohm space	Add PR139 0 ohm resistor	X03
27	48	+1.5VSP	11/13	Antony	Change component size	Change PQ64 to SIS412DN	X03
28	50	VGA_COREP	11/13	Antony	Reserve RC space	Add PR242 0 ohm resistor and reserve PC223 space	X03
29	45	+5VALWP/+3VALWP	12/21	Antony	Solve S3/S5 acoustic noise issue	PR96 de-populate	X03
30	45	+5VALWP/+3VALWP	12/21	Antony	Solve S3/S5 acoustic noise issue	Add PR108 0 ohm	X03
31	48	+1.5VSP	12/23	Antony	Reserve CCM mode resistor	Reserve PR140 space	X04

Compal Electronics, Inc.

Title		
PWR-PIR2		
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		1.0
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Item	Date	Fixed Issue	Rev.	PG#	Modify List
01	2009/09/07	Enable N11P-GS1 +VGA_COREP when boot system	0.2	19	Mount R238 10K ohm pull high
02	2009/09/07	U3 pin SM_PWROK schematics error for DDR3	0.2	08	U3 pin SM_PWROK connect to +1.5V
03	2009/09/07	LVDS EDID can't switch select for panel	0.2	28	Modify U20,Q119,Q120 schematics and +LCDVDD change to +3VS
04	2009/09/07	GMCH L_BKLT_CTRL isn't inverted before MUXed	0.2	28	Remove U25 for net DPST_PWM
05	2009/09/07	Switch IC U4 pin1 can not enable	0.2	28	Remove R491 0 ohm and add mount R490 0 ohm
06	2009/09/07	Change HDMI connector	0.2	31	Change connector JHDMI1
07	2009/09/07	Change Display port connector	0.2	32	Change connector JDP1
08	2009/09/10	Change D-SUB connector	0.2	30	Change connector JCRT1
09	2009/09/10	Change SIM,WWAN,WLAN,FAN connector	0.2	33	Change connector JSIM1,JWWAN1,JWLAN1,JFAN1
10	2009/09/10	Change BTB connector	0.2	36	Change connector JBTB1
11	2009/09/10	Q26 footprint error	0.2	29	Change Q26 footprint
12	2009/09/10	Audio board move IHDA signal 33ohm to MB	0.2	18	Add R8,R46,R119,R120 33ohm
13	2009/09/16	LID switch move to audio board	0.2	36	Delete U2,C2,C3,R5
14	2009/09/16	Audio board ALC665 pin9 need +1.5VS	0.2	36	Change JBTB1 pin5,pin7,pin9 to +1.5VS
15	2009/09/17	Add +3VALW for ELC function LED power	0.2	36	Change JBTB1 pin8,pin10,pin12 to +3VALW
16	2009/09/17	LID SW move from MB to audio board	0.2	36	Change JBTB1 pin6 to LID_SW#
17	2009/09/17	Modify ELC schematics fllow DELL design	0.2	38	Modify ELC schematics
18	2009/09/17	Change D16,D25,D26,D31 to PJDLCO5C for EMI	0.2	29	Change BOM D16,D25,D26,D31 to SCA00001100
19	2009/09/17	DGPU +3VS_DELAY 漏電	0.2	21	Modify Q21 schematics
20	2009/09/18	Change R681 to 33ohm for EMI request	0.2	35	Change BOM R681 from 22ohm to 33ohm
21	2009/09/18	BOM mount L39,L40,L41,L42 for EMI request	0.2	31	Change BOM R579,R580,R581,R588,R591,R592,R595,R596 to @
22	2009/09/22	JP3 pin6,pin7(I2C) add PJDLCO5C for EMI	0.2	38	Add D30 to JP3 pin6 and pin7
23	2009/09/22	Add 0.1uF to SM_PWROK for EMI request	0.2	08	Add C190 0.1uF
24	2009/09/22	Modify JLAN1 GND for vender request for EMI	0.2	34	Add C1162,C1163 0.1uF
25	2009/09/22	For JMicro vender request	0.2	35	C1685 4.7uF near +3V_MCVCC
26	2009/09/22	DGPU +3VS_DELAY 漏電	0.2	21	Add Q58 and R389 to net VGA_CLKREQ#_R

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27	2009/09/23	Modify screw H12,H13,H17 for ME request	0.2	39	Modify screw H12,H13,H17
28	2009/09/23	Add +5VS for LED board power budget	0.2	39	Change JP3 pin9 from GND to +5VS
29	2009/09/23	Add 1000pF for EMI request	0.2	14	Add C115 1000pF
30	2009/09/23	Add 1000pF for EMI request	0.2	15	Add C196 1000pF
31	2009/09/24	Add 0.1uF on PCIE CLK for vender request	0.2	34	Add C1705,C1706 0.1uF
32	2009/09/24	Add 33ohm and 22pF for EMI request	0.2	35	Add 33ohm and 22pF to JCARD1 pin7,pin16
33	2009/09/24	Change crystal X1 cap. to 27pF	0.2	37	Change BOM C1616,C1617 from 15pF to 27pF(SE071270J8L)
34	2009/09/28	Modify USB powershre schematics	0.2	36	Move L43,R617,R618 near JUSB1
35	2009/09/28	Use the USB detect method for powershare	0.2	36	BOM need mount U60,D52,D58
36	2009/09/28	For CLKRUN# issue	0.2	37	Add U39 pin38 net PM_CLKRUN#
37	2009/09/28	Net SM_PWROK add 0.1uF near PU9 for EMC	0.2	48	Net SM_PWROK add C198 0.1uF
38	2009/09/28	Net SM_PWROK add 0.1uF near U3B for EMC	0.2	08	Net SM_PWROK add C190 0.1uF
39	2009/09/29	For RF request add 47pF for WLAN,WWAN +1.5VS	0.2	33	Add C1136,C1184 47pF to +1.5VS
40	2009/09/29	Intel request delete R27,R28,R29 for layout	0.2	05	Delete R27,R28,R29
41	2009/09/29	Add JLVDS1 connector detect pin	0.2	29	Add JLVDS1 pin32 LVDS_CONN,pin33 STATUS_BOARD_CONN
42	2009/09/30	Add JBTB1 connector detect pin	0.2	36	Add JBTB1 ppin33 IO_BOARD_CONN
43	2009/09/30	Add JP3 connector detect pin	0.2	38	Add JP3 pin15 STATUS_BOARD_CONN,pin16 IO_BOARD_CONN
44	2009/09/30	EC add JLVDS1,JBTB1,JP3 connector detect pin	0.2	37	Add LVDS_CONN to U39 pin18
45	2009/10/01	Add display port AUX schematics	0.2	32	Add Q123,Q124,Q125,R602,R603,R613,R614
46	2009/10/01	Add a FET for CPU overclocking	0.2	06	U39 pin25 add a net EC_FSB_SEL
47	2009/10/05	Add I2CB,I2CH pull high for NVIDIA request	0.2	15	Add R420,R421,R422,R423 pull high to +3VS_DELAY
48	2009/10/06	For Intel request change C1702 BOM	0.2	40	Change C1702 from 0.01uF to 0.1uF
49	2009/10/06	Change BOM error	0.2	23	Change C191,C192,C197,C261,C262,C263 from SE00000JM00 to SE00000MM1M
50	2009/10/08	Change Q35 Id to 300mA	0.2	23	Change Q35 from SB000008J00 to SB000003P10
51	2009/11/05	Change USB D+ and D-	0.3	36	Swap L43 USB signal USBP2_D-_C and USBP2_D+_C
52	2009/11/05	Change location R263 to C271	0.3	19	Change location R263 to C271 for layout.

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Item	Date	Fixed Issue	Rev.	PG#	Modify List
53	2009/11/05	Add 100K pull low for EC debug request	0.3	33	Add JWWAN1 pin49 R657 100K pull low to GND for net EC_TX
54	2009/11/05	Change BIOS ROM part to another PN	0.3	37	Change U41 BOM from SA00001ITOL to SA00002TOOL
55	2009/11/09	Change C189,C195,C202 BOM	0.3	23	Change C189,C195,C202 PN from SE00000IS0A to SE076104K80
56	2009/11/09	Change C1105 BOM	0.3	36	Change C1105 PN from SE000000GK0 to SE000000GC0L
57	2009/11/09	Change C191,C192,C197,C261,C262,C263 BOM	0.3	23	Change C191,C192,C197,C261,C262,C263 PN from SE00000MM1M to SE076473K8L
58	2009/11/10	Add 10K pull high for LAN LED leakage	0.3	34	Add R662,R664 10K pull high to +3V_LAN
59	2009/11/10	Reserved 10K pull high for LID_SW#	0.3	37	Add R665 10K pull high to +3VALW
60	2009/11/10	Modify board ID	0.3	37	Mount R622 100K,R627 20K
61	2009/11/10	Modify U4 pin13,pin14	0.3	16	change R142,R352 to 22ohm,1%
62	2009/11/11	Reserved GPIO49 for DGPU_PWR_EN	0.3	19	Add R263,R268 0 ohm to net DGPU_PWR_EN
63	2009/11/11	For ESD request change D30 PN	0.3	38	Change D30 PN from SCA00001100 to SCA00000200
64	2009/11/12	Change R500 to 110ohm for LCD panel EA	0.3	29	Change R500 from 300ohm to 110ohm
65	2009/11/16	Modify JTP1 footprint for layout	0.3	39	Modify JTP1 footprint
66	2009/11/17	Add a 0603 size 0ohm for LVDS SW thermal	0.3	28	U19 pin 57 add a R329 0ohm to GND
67	2009/11/17	Reserved a jump for HDD 3.3V	0.3	32	Add a J3 to +3VS and C1628,C1634
68	2009/11/17	Change U42 pin8 from +5VS to +5VALW	0.3	38	Change U42 pin8 to +5VALW
69	2009/11/18	Reserved 0.1uF,22P for U42 pin6	0.3	38	Add R139,C1843,C313 to U42 pin6
70	2009/11/20	Net VGA_CLKREQ#_R 重複 pull H to +3VS_DELAY	0.3	21	BOM delete R406 10K ohm
71	2009/11/20	Change Q35 to AO3414 for +1.8VSDGPU 300mA	0.3	23	Change BOM Q35 from SB000003P10 to SB000007600
72	2009/11/20	Change Q11 to SI7121DN for +3VS_DELAY 1380mA	0.3	23	Change Q11 from SB923010020 to SB00000KI00
73	2009/11/20	U42 reserved 0.1uF for RF request.	0.3	38	Add C1857,C1858,C1859,C1860,C1861,C1862,C1863,C1864,C1865,C1866,C1867 0.1uF
74	2009/11/20	Change BOM error.	0.3	40	Change C1702 from 0.1uF to 0.01uF
75	2009/12/16	Modify board ID	1.0	37	Mount R628 37.4K and delete R627 20K
76	2009/12/16	Change DGPU_PWR_EN from GPIO18 to GPIO49	1.0	19	BOM mount R268 0 ohm and delete R263 0 ohm
77	2009/12/16	For DGPU thermal error modify power sequence	1.0	23	BOM mount R210,C207 and change R118 to 68K,C168 to 0.22uF
78	2009/12/16	For nVIDIA request change R571,R568 value	1.0	31	Change BOM R571,R568 from 10K(SD028100280) to 2.2K(SD028220180) or 4.7K

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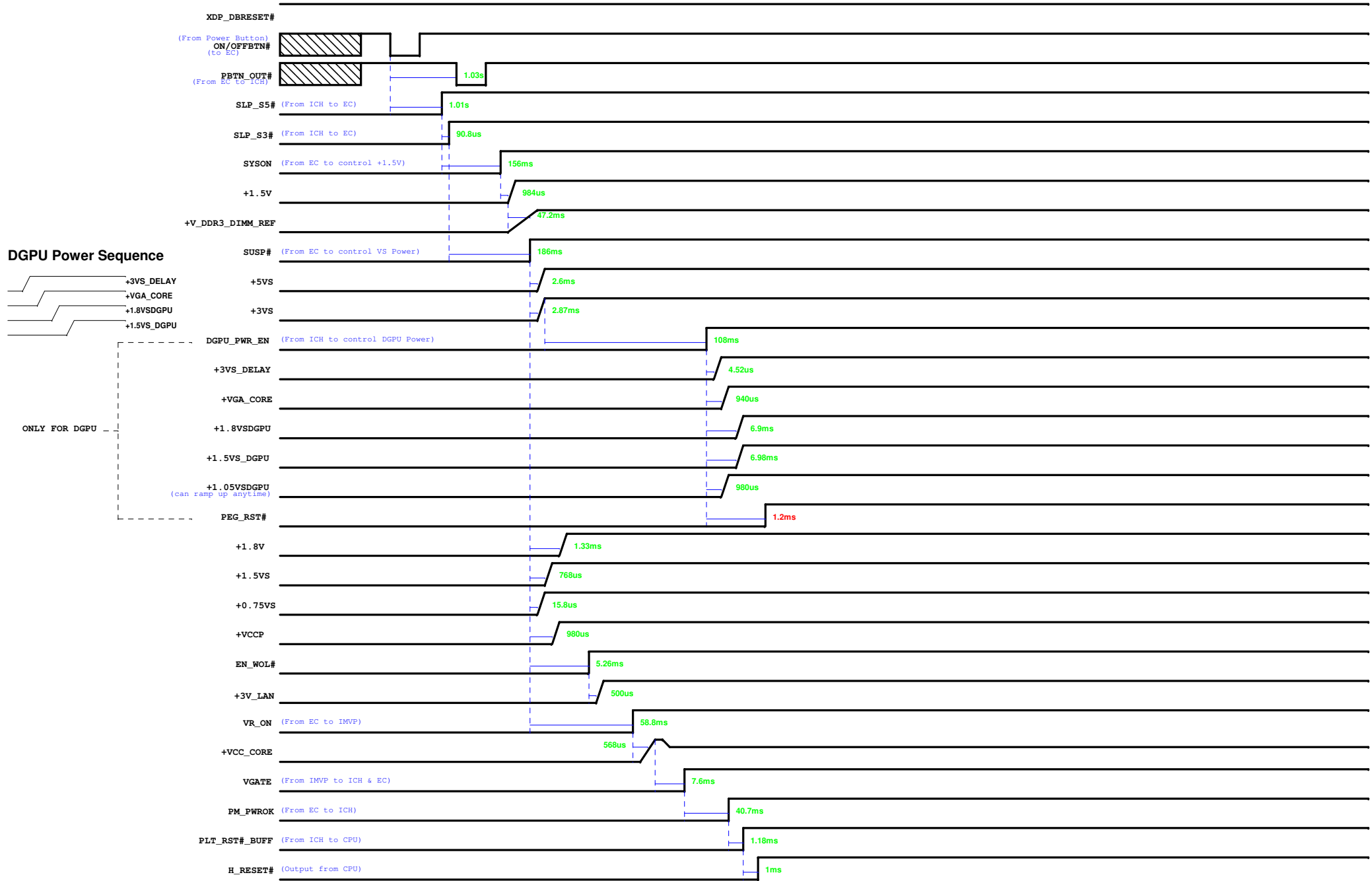
Item	Date	Fixed Issue	Rev.	PG#	Modify List
103	2009/12/28	Change BOM for DELL 禁用料	1.0	23	Change C1664,C1694,C179,C245,C252,C492,C1564,C1693 from SC1H751H01L to SC1SS355010
104	2009/12/28	Change BOM for DELL 禁用料	1.0	11	Change C90 from SE000005T80 to SE000005T8L
105	2009/12/28	Change BOM for DELL 禁用料	1.0	11	Change C93 from SE000008L80 to SE000008L0L
106	2009/12/28	Change BOM for DELL 禁用料	1.0	11	Change C1117,C1142,C86 from SE049225Z80 to SE049225Z8L
107	2009/12/28	Change BOM for DELL 禁用料	1.0	34	Change C1654 from SE067102K80 to SE067102K8L
108	2009/12/28	Change BOM for DELL 禁用料	1.0	20	Change C286,C288,C289,C290,C293,C304 from SE070104Z80 to SE070104Z8L
109	2009/12/28	Change BOM for DELL 禁用料	1.0	08	Change C1514,C1519,C1528,C1532,C210,C211,C215,C232,C237 ,C241,C72,C74 from SE075103K80 to SE068103K8L
110	2009/12/28	Change BOM for DELL 禁用料	1.0	40	Change C1696,C1697 from SE075103ZN0 to SE068103K8L
111	2009/12/28	Change BOM for DELL 禁用料	1.0	07	Change C56,C57,C58 from SGA20221D40 to SGA20221E8L
112	2009/12/28	Change BOM for RF team request	1.0	29	Change C231,C238 from SE07150AC00 to SE07122AC8L

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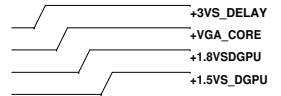
Item	Date	Fixed Issue	Rev.	PG#	Modify List
79	2009/12/16	Change L52 part number	1.0	23	Change BOM L52 from SHI00006N0L to SHI00005V0L
80	2009/12/17	Change Q11 Compal PN	1.0	23	Change Q11 from SB00000KI00 to SB00000MK00
81	2009/12/18	Change L39,L40,L41,L42 PN for EMI	1.0	31	Change L39,L40,L41,L42 from SM070000K00 to SM070000I00
82	2009/12/20	Change C1616,C1617 to 18PF	1.0	37	Change C1616,C1617 from SE071270J8L to SE071180J80
83	2009/12/20	Change BOM for cost	1.0	11	Change C5,C84,C146 from SGA19331D10 to SGA00002680
84	2009/12/20	Change BOM for cost	1.0	12	Change C153 from SE124474KT0 to SE124474K80
85	2009/12/20	Change BOM for cost	1.0	12	Change C153 from SE000000GK0 to SE000003H00
86	2009/12/21	Change BOM for DELL 禁用料	1.0	23	Change C179,C245,C252,C492,C1664,C1693,C1694 from SE000000I10 to SE00000110L
87	2009/12/21	Change BOM for DELL 禁用料	1.0	11	Change C93 from SE000008L80 to SE000008L0L
88	2009/12/22	Change BOM for DELL 禁用料	1.0	23	Change C72,C74,C210,C211,C215,C232,C237,C241,C258,C1514,C1519,C1528,C1532 from SE075103K80 to SE068103K8L
89	2009/12/22	Change BOM for DELL 禁用料	1.0	40	Change C1696,C1697 from SE075103ZN0 to SE068103K8L
90	2009/12/22	Change BOM for DELL 禁用料	1.0	07	Change C56,C57,C58 from SGA20221D40 to SGA20221E8L
91	2009/12/22	Change LVDS switch IC	1.0	28	Change U19 from SA00001RM0L to SA000030900
92	2009/12/22	Modify BOM for cost	1.0	32	BOM @ C1628,C1634
93	2009/12/22	Modify JKB1 footprint for 2nd source DFX	1.0	37	Modify JKB1 LTCX0020V0L footprint to TYCO_2-2041084-5_25P-T
94	2009/12/23	Change BOM for DELL 禁用料	1.0	17	Change U10 from SA007080B9L to SA007080B90
95	2009/12/23	Change BOM for DELL 禁用料	1.0	29	Change Q23,Q34,Q36,Q59 from SB000008J00 to SB570020110
96	2009/12/23	Change BOM for DELL 禁用料	1.0	23	Change Q10,Q12,Q46,Q47,Q52,Q56 from SB000009610 to SB00000960L
97	2009/12/28	Change BOM for DELL 禁用料	1.0	28	Change Q119,Q120,Q21,Q29,Q30 from SB00000AR00 to SB57002528L
98	2009/12/28	Change BOM for DELL 禁用料	1.0	19	Change Q8,Q9 from SB502060000 to SB50206008L
99	2009/12/28	Change BOM for DELL 禁用料	1.0	29	Change Q28,Q58 from SB570020020 to SB57002008L
100	2009/12/28	Change BOM for DELL 禁用料	1.0	29	Change Q26 from SB570020400 to SB57002041L
101	2009/12/28	Change BOM for DELL 禁用料	1.0	40	Change Q51,Q53,Q54 from SB570025280 to SB57002528L
102	2009/12/28	Change BOM for DELL 禁用料	1.0	11	Change D1,D13,D15,D5,D6 from SC1H751H01L to SC1SS355010

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# NAP00 Power On Sequence



## DGPU Power Sequence



ONLY FOR DGPU

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