

MODEL NAME : *PAP00*

PCB NO : *LA-6961P (DA*****)*

BOM P/N : *TBD*

Dell/Compal Confidential

Schematic Document

Phantom (Huron River)

Sandy Bridge (BGA1023) + Cougar Point (SFF)

DISCRETE VGA N12P-GS (optimus)

2010-11-29

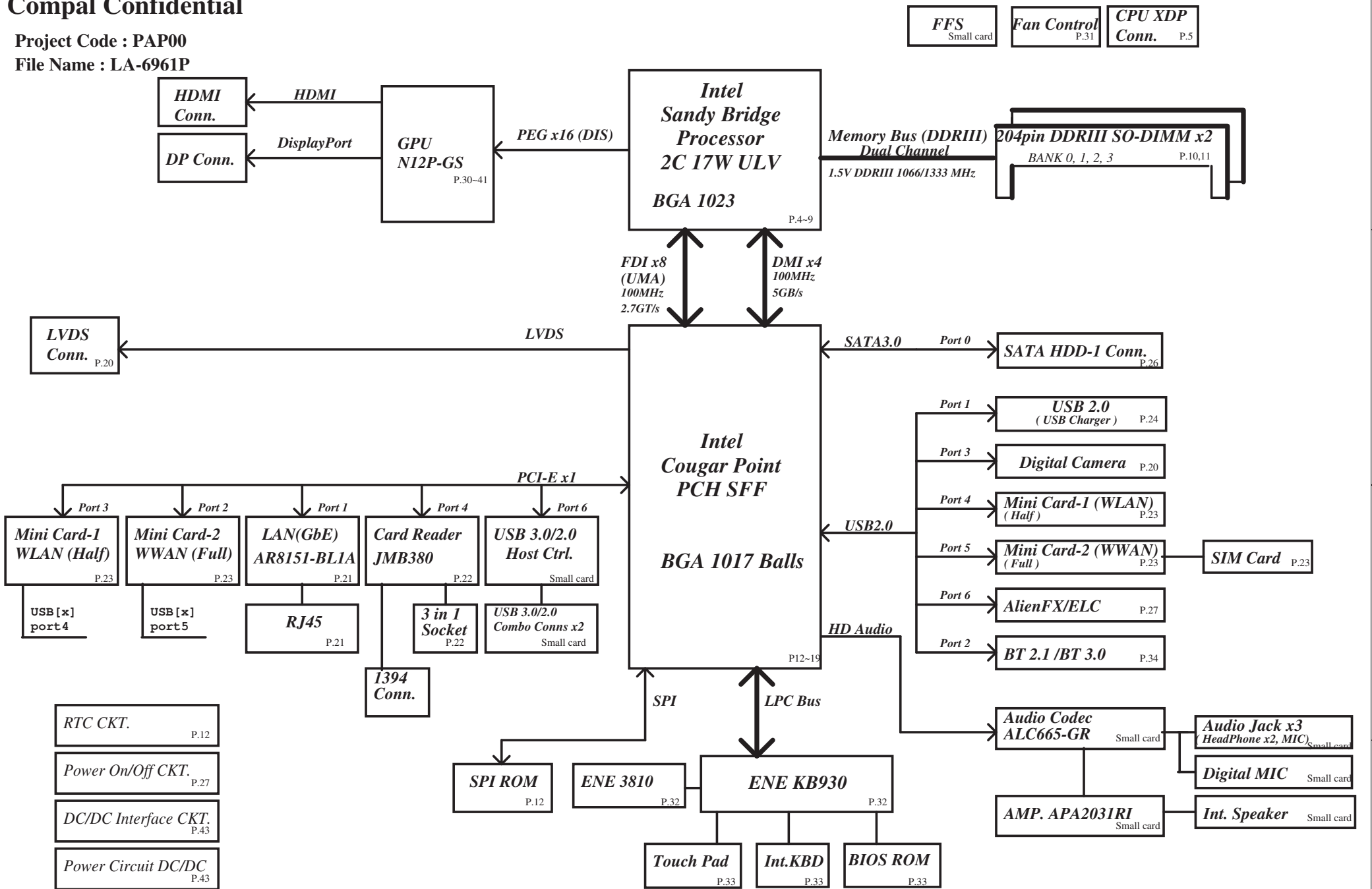
Rev: 0.4

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Project Code : PAP00

File Name : LA-6961P



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Issued Date	2010/06/10	Deciphered Date	2011/07/06	Title	PCH (6/8) PWR	
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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

PCH	USB PORT#	DESTINATION
	0	None
	1	JUSB1 (Ext Left Side)
	2	Bluetooth
	3	CAMERA
	4	JMINI1 (WLAN)
	5	JMINI2 (WWAN)
	6	ELC
	7	None
	8	None
	9	None
	10	None
	11	None
	12	None
13	None	

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Thermal Sensor 1	FFS	VGA Thermal Sensor	SMSC
EC_SMB_CK1 EC_SMB_DA1	KB930			V					
EC_SMB_CK2 EC_SMB_DA2	KB930								
PCH_SML0CLK PCH_SML0DATA	PCH								
PCH_SML1CLK PCH_SML1DATA	PCH	V	V			V		V	V
MEM_SMBCLK MEM_SMBDATA	PCH				V		V		

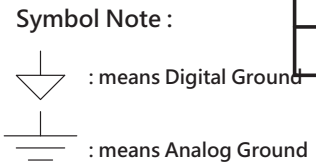


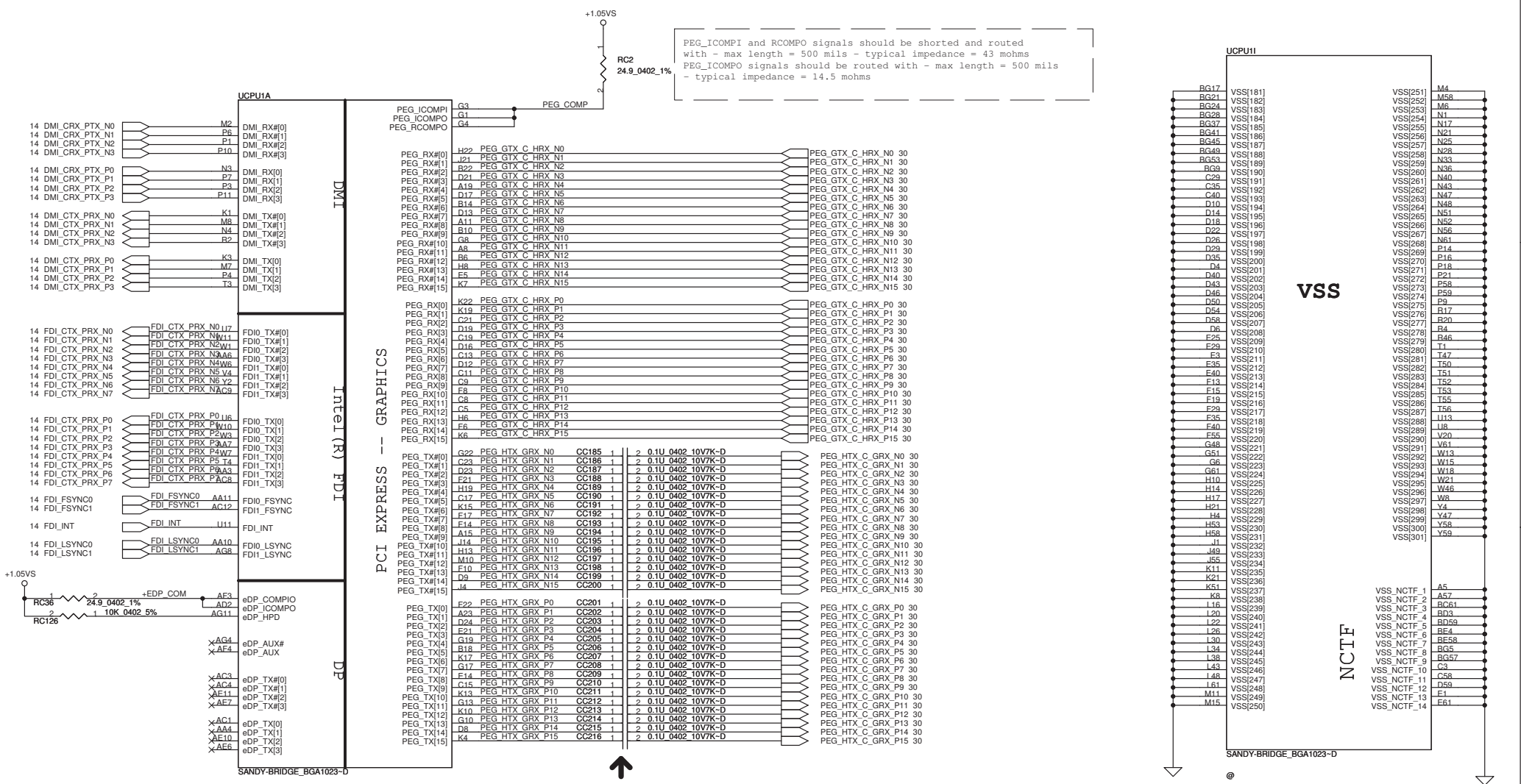
CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	MINI CARD-2 WWAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	USB 3.0		
	CLKOUT_PEG_B	None		

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	None
SATA3	None
SATA4	None
SATA5	None

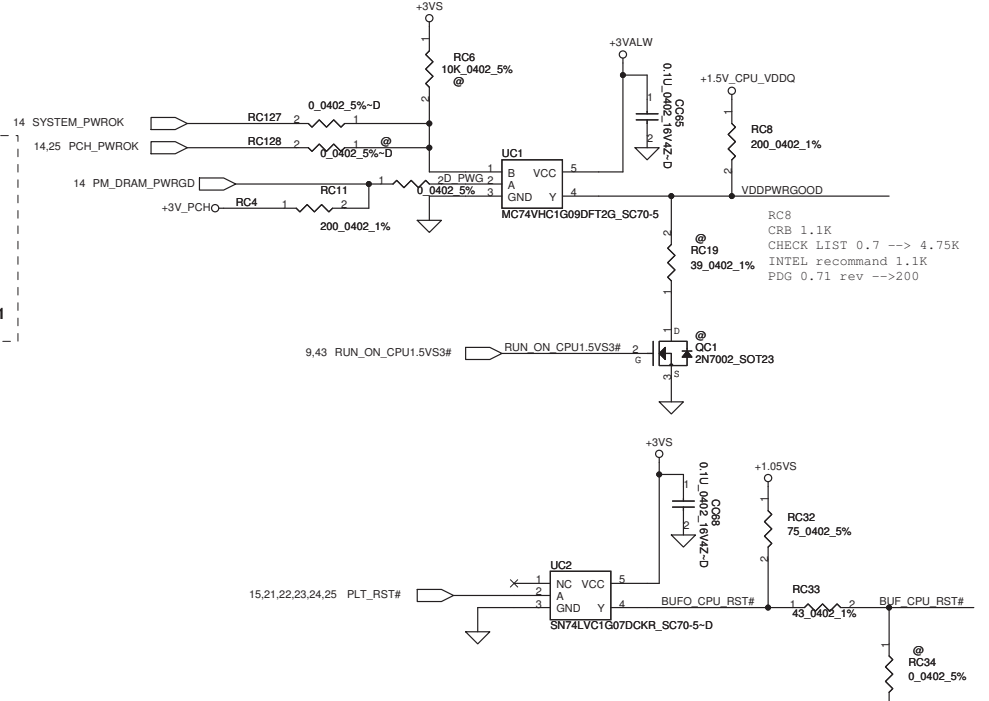
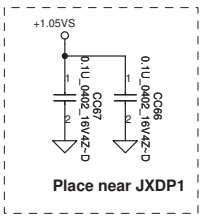
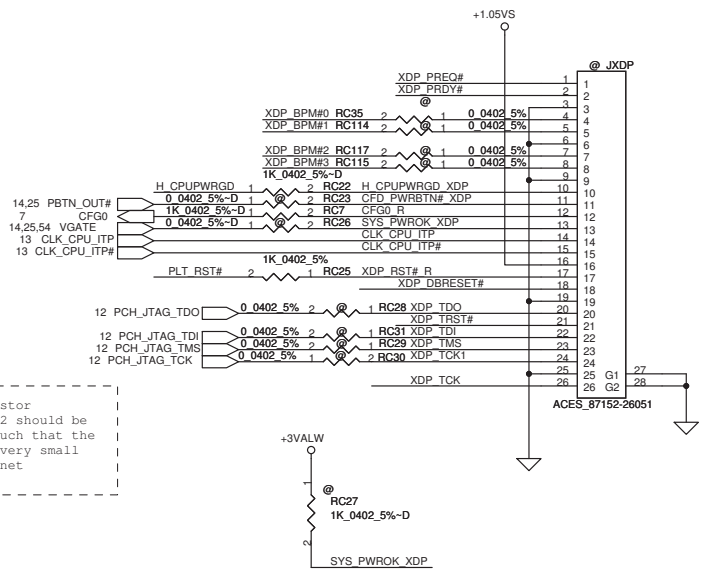
PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER and 1394
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None



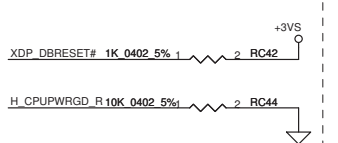
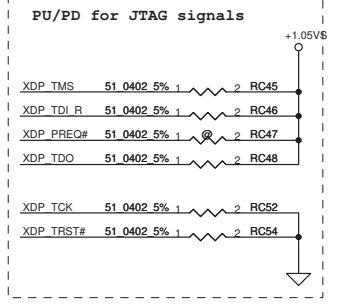
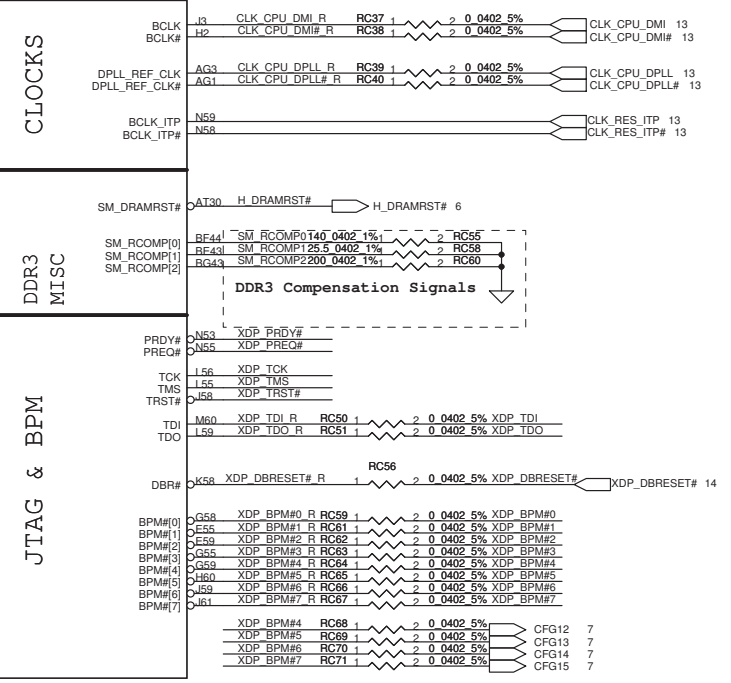
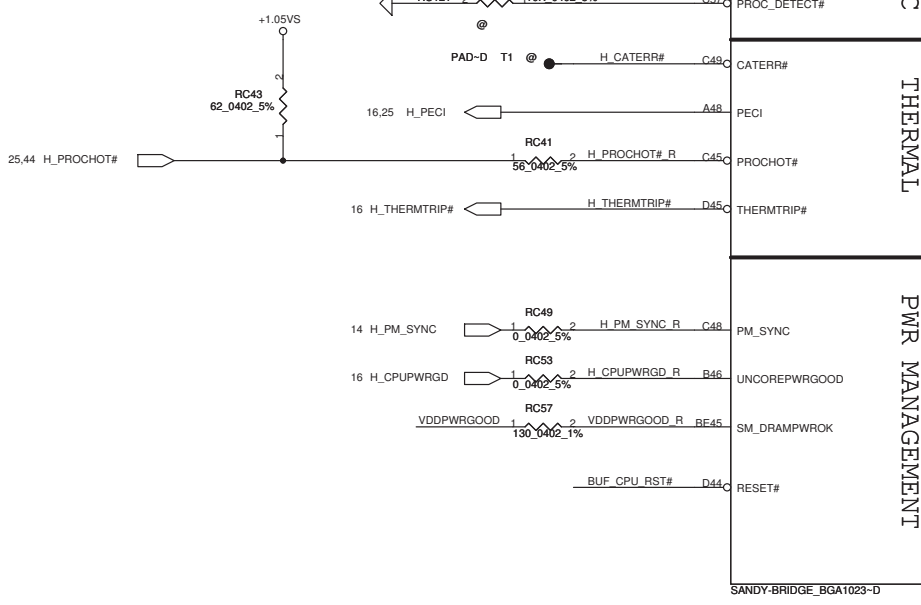


Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

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Issued Date	2010/07/06	PROCESSOR(I/6) DMI,FDI,PEG	
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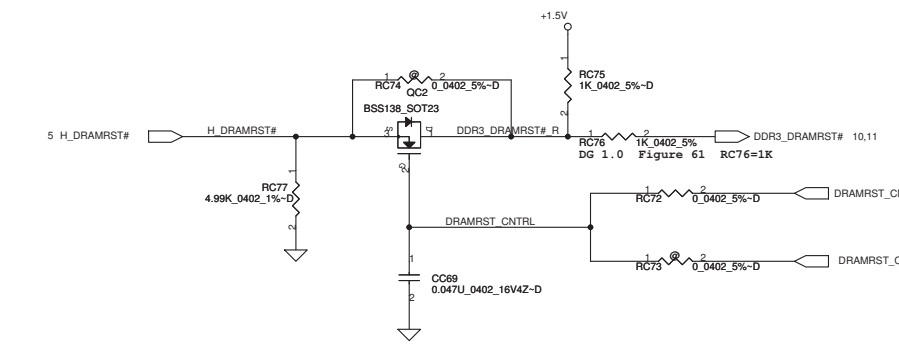
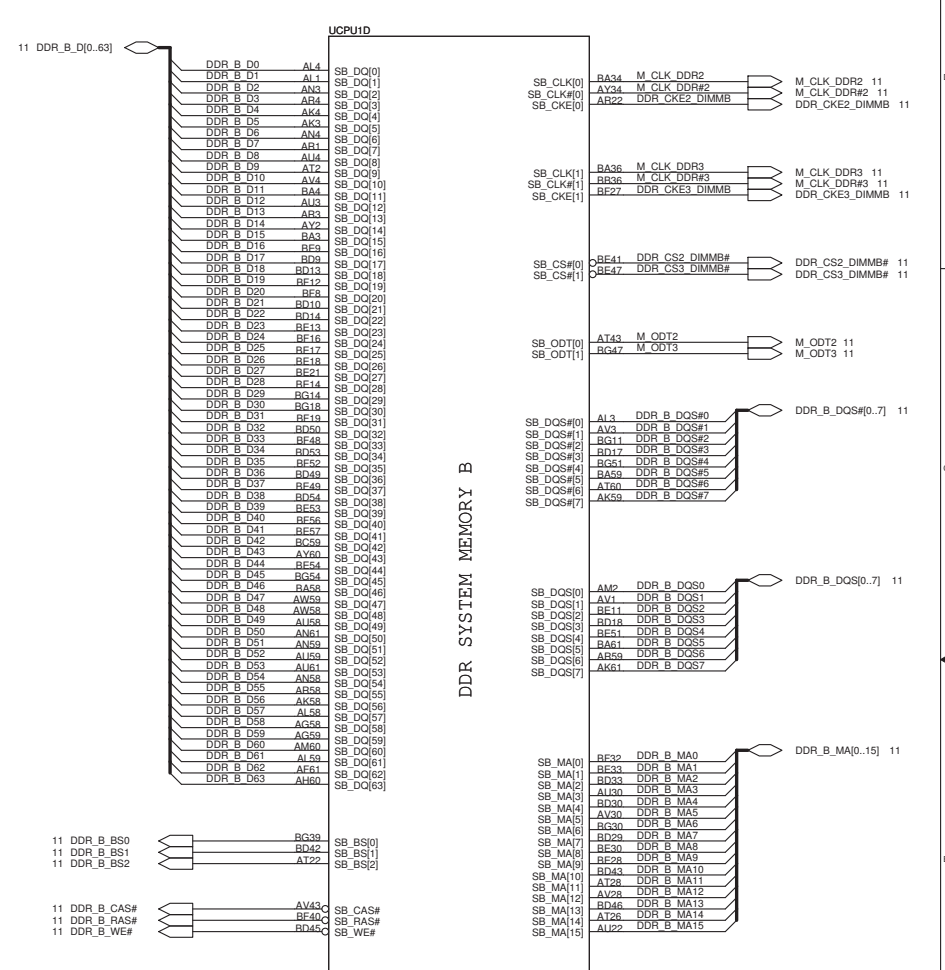
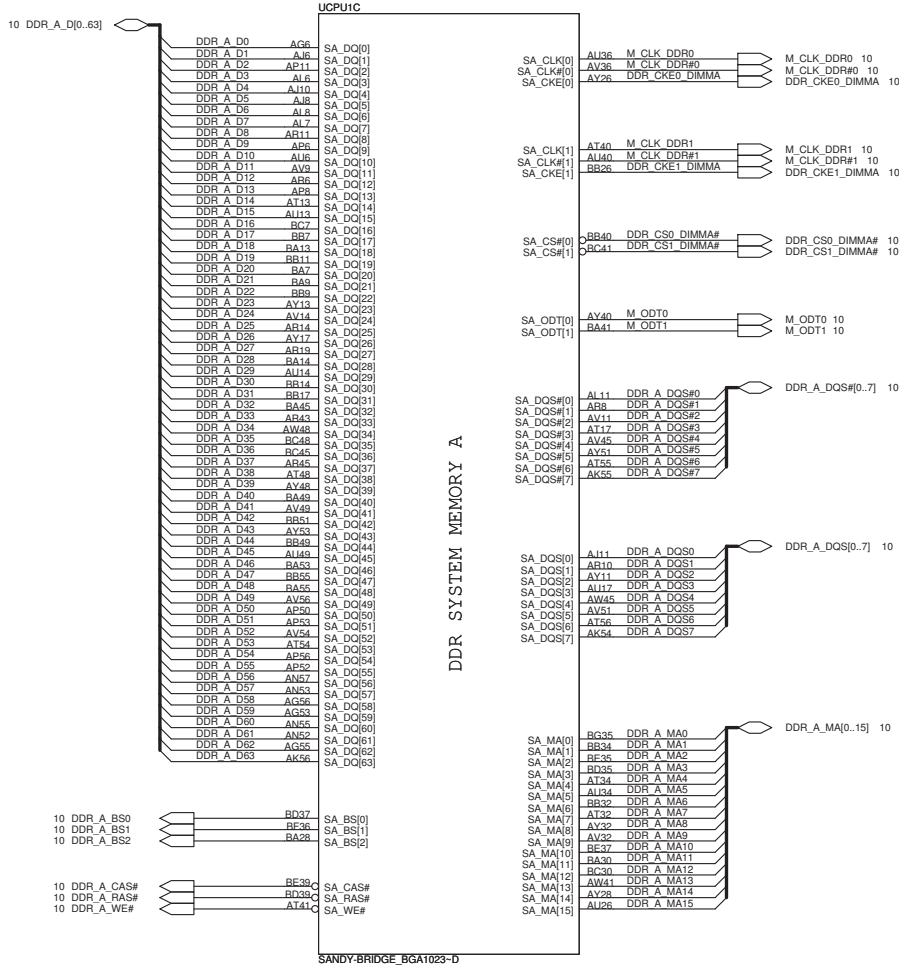
PROC_DETECT (Processor Detect): pulled to ground on the processor package. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present



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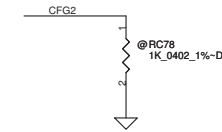
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PROCESSOR(2/6) PM,XDP,CLK		
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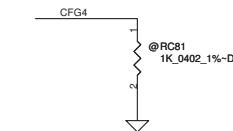


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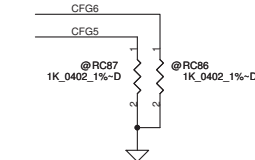
CFG Straps for Processor



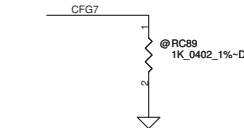
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	<ul style="list-style-type: none"> *1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



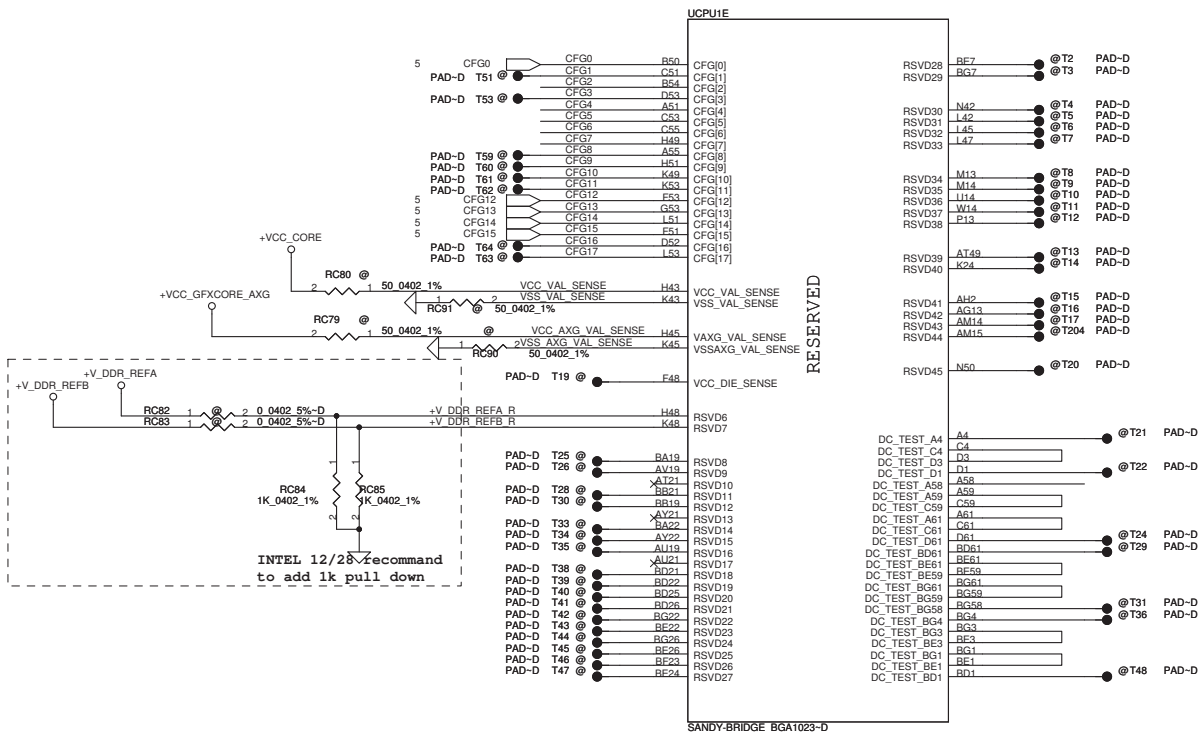
Display Port Presence Strap	
CFG4	<ul style="list-style-type: none"> *1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

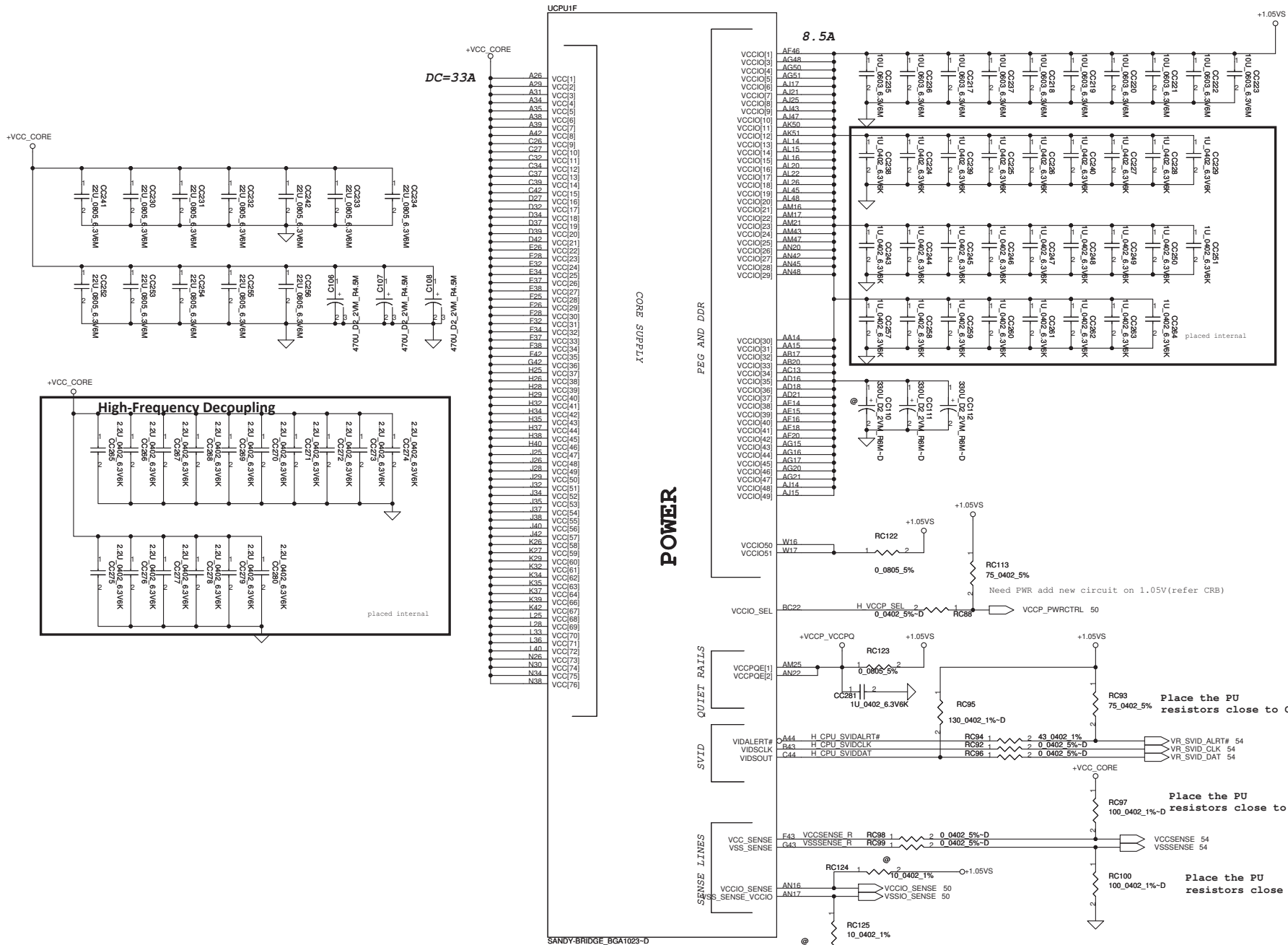


PCIe Port Bifurcation Straps	
CFG[6:5]	<ul style="list-style-type: none"> *11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



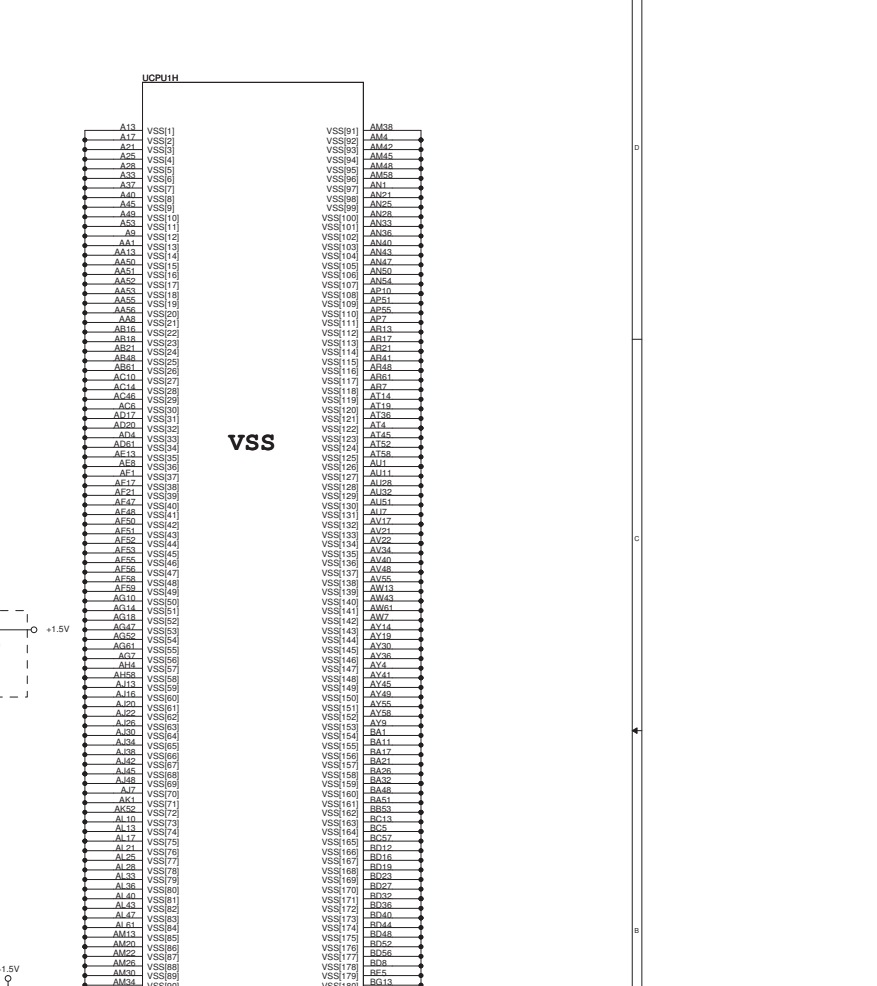
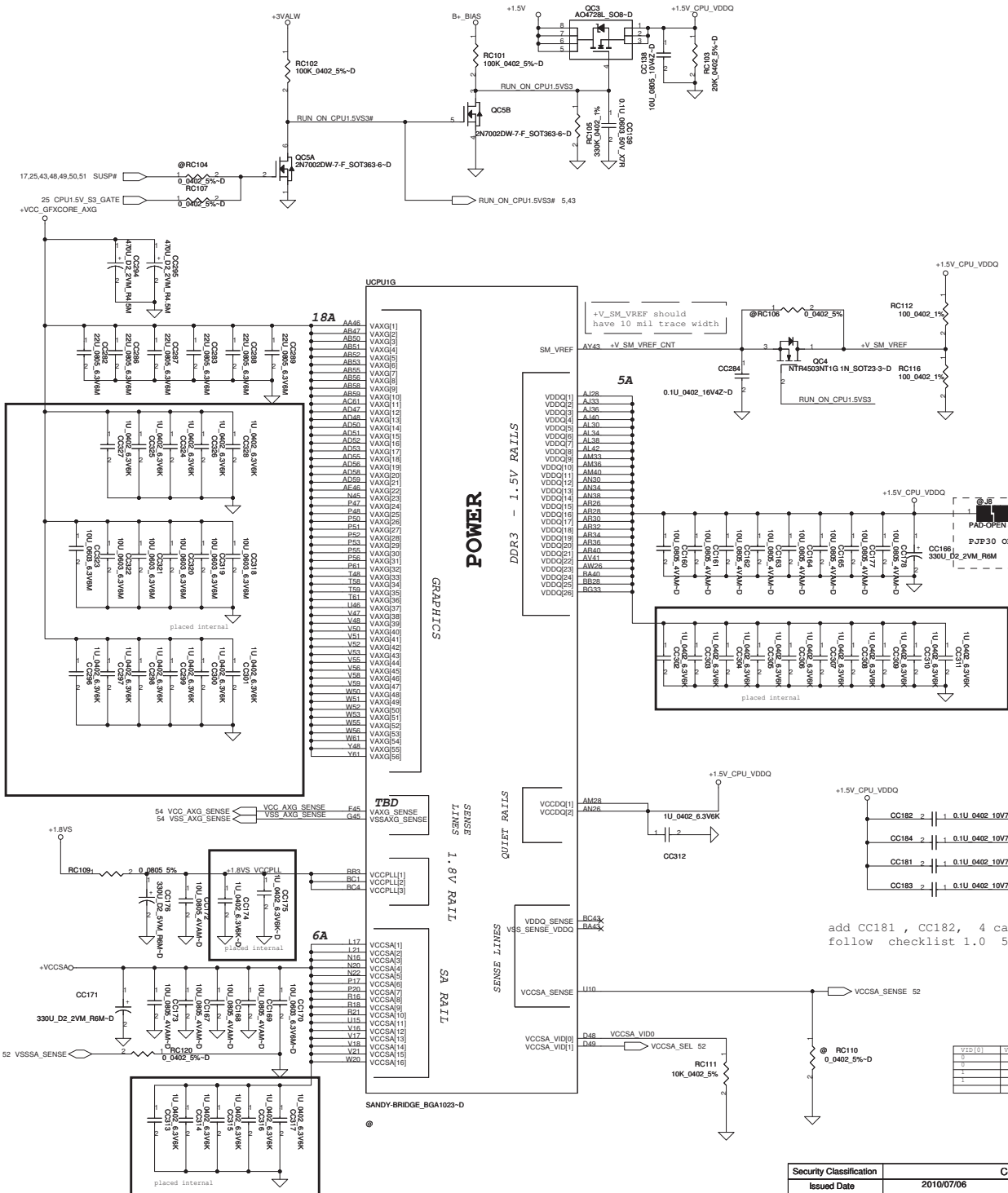
PEG DEFER TRAINING	
CFG7	<ul style="list-style-type: none"> *1: (Default) PEG Train immediately following xRESET# de assertion 0: PEG Wait for BIOS for training





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+1.5V_CPU_VDDQ Source



POWER

GRAPHICS

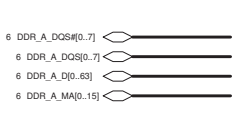
SENSE

1.0V RAIL

SA RAIL

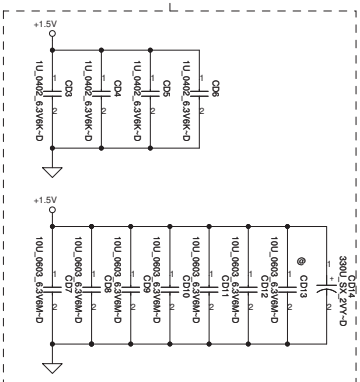
add CC181 , CC182, 4 caps are all pop.
follow checklist 1.0 5/24

V2D[0]	V2D[1]		2011	2012
1	1	0.30 V	Yes	Yes
1	1	0.30 V	Yes	Yes
1	1	0.72 V	No	Yes
1	1	0.675 V	No	Yes

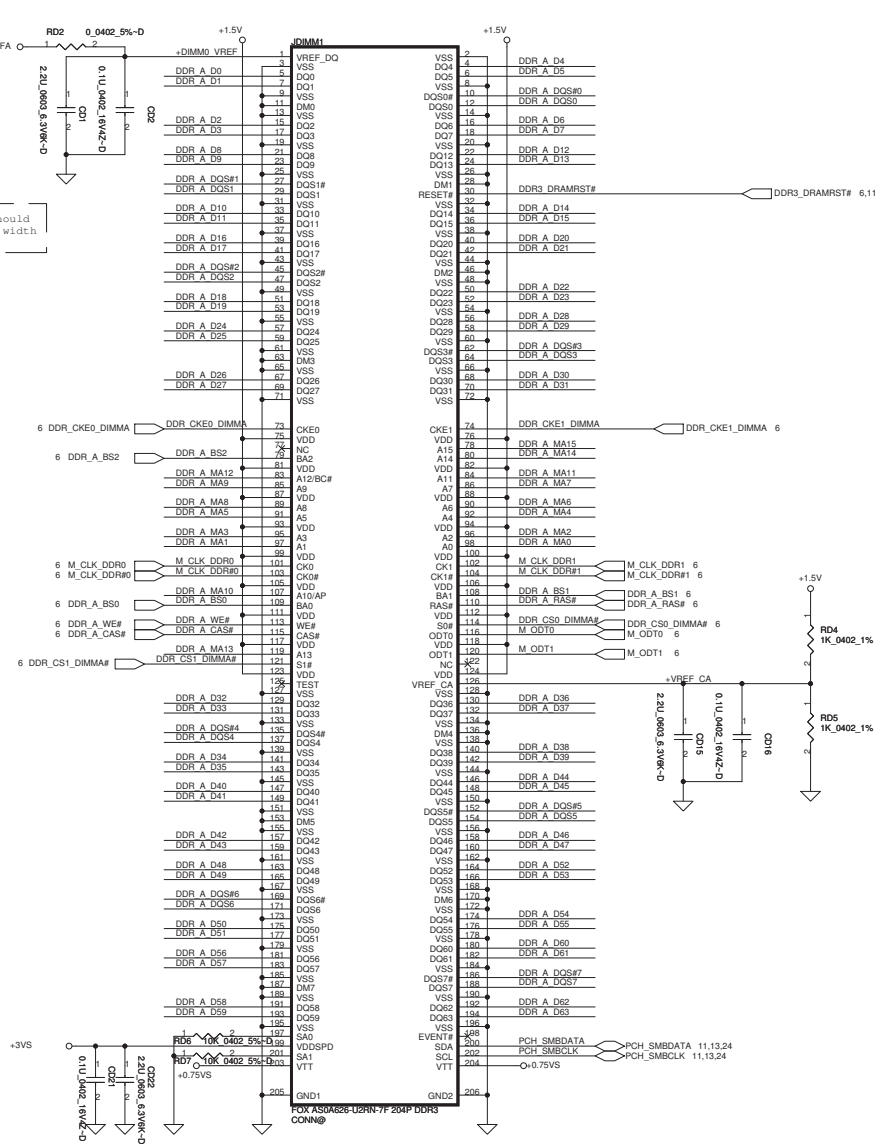
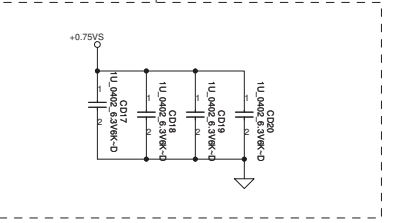


Layout Note:
Place near JDIMM1

All VREF traces should
have 10 mil trace width



Layout Note:
Place near JDIMM1.203,204



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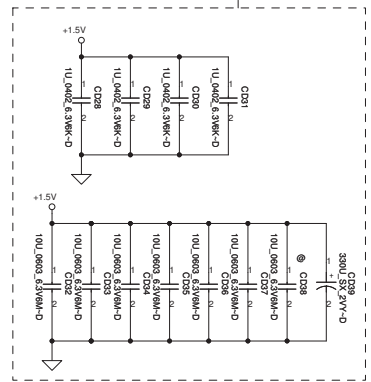
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DDRIII DIMMA			
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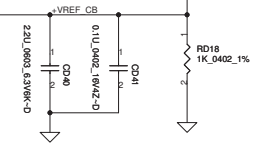
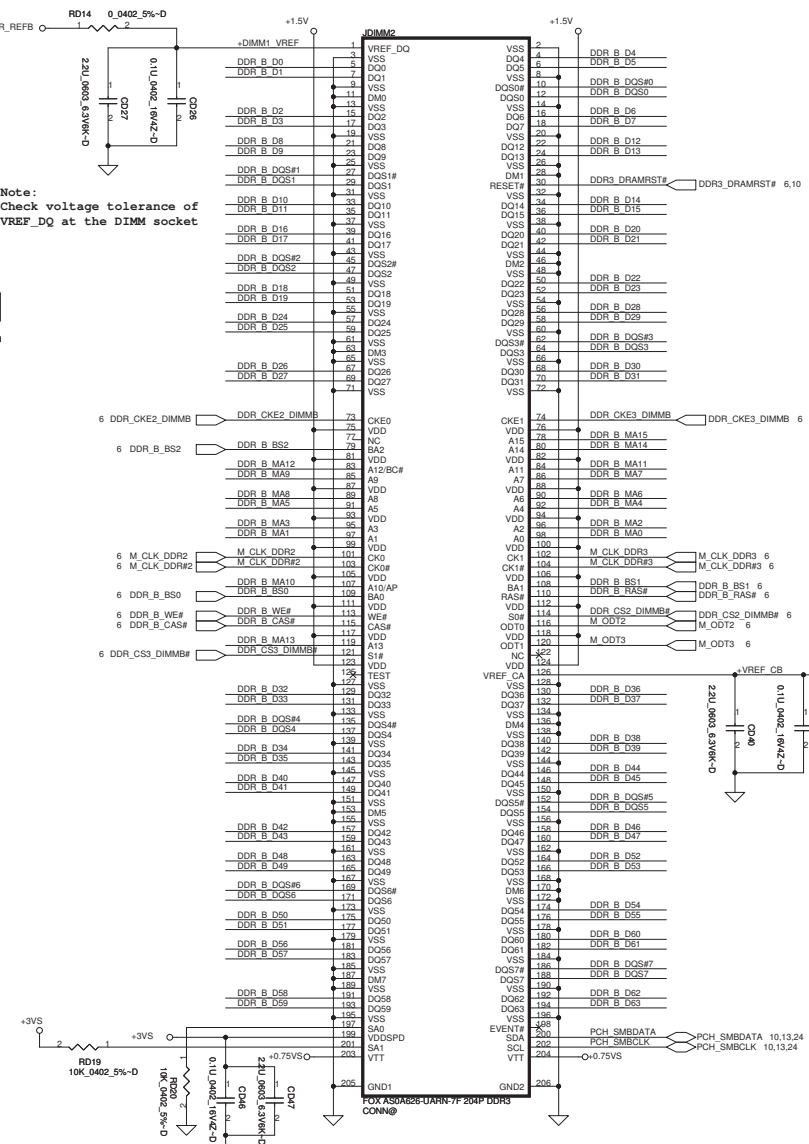
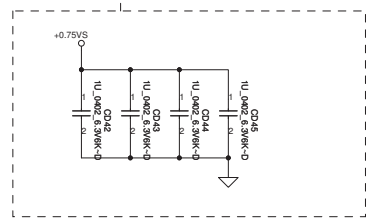
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

Layout Note:
Place near JDIMMB

All VREF traces should
have 10 mil trace width



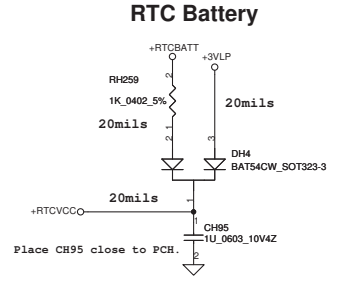
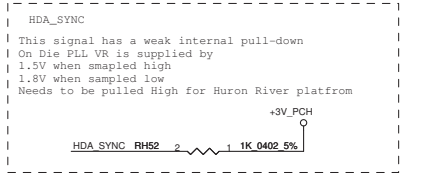
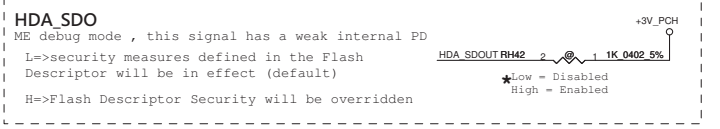
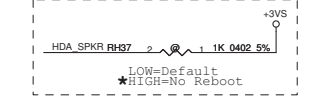
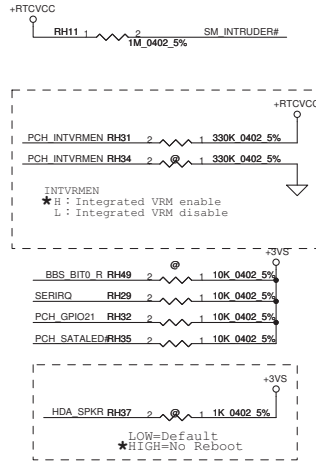
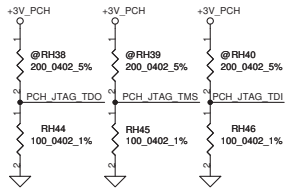
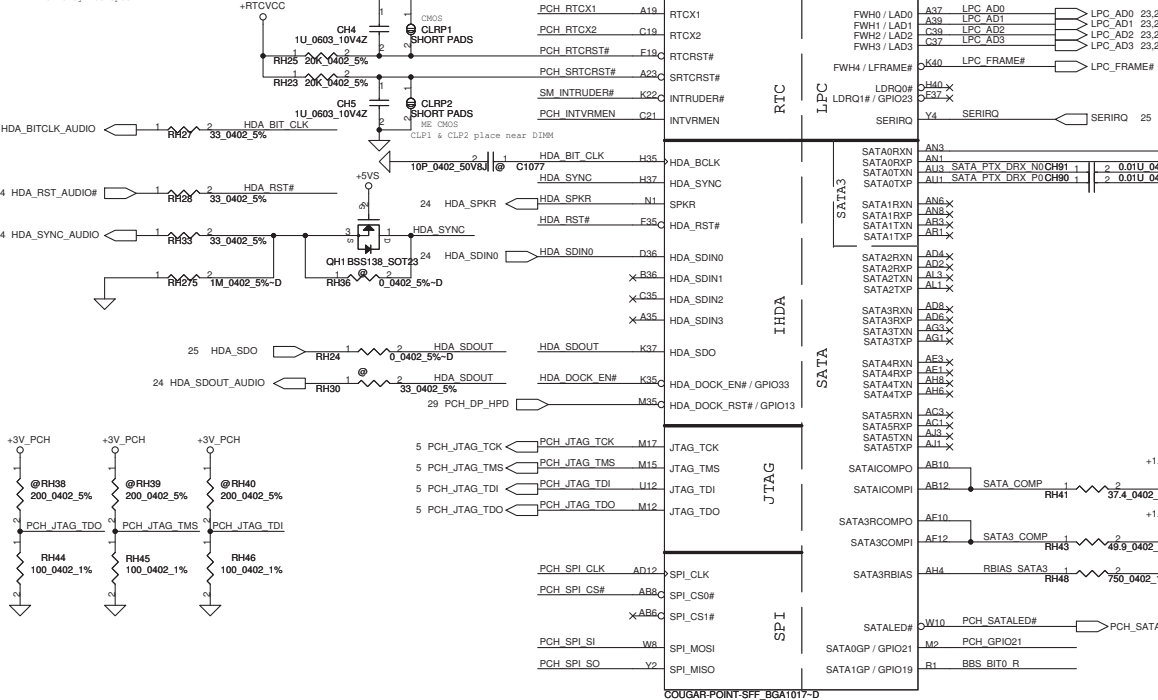
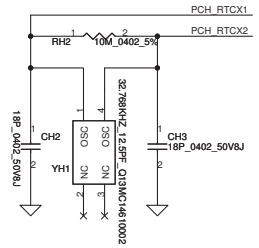
Layout Note:
Place near JDIMMB.203,204



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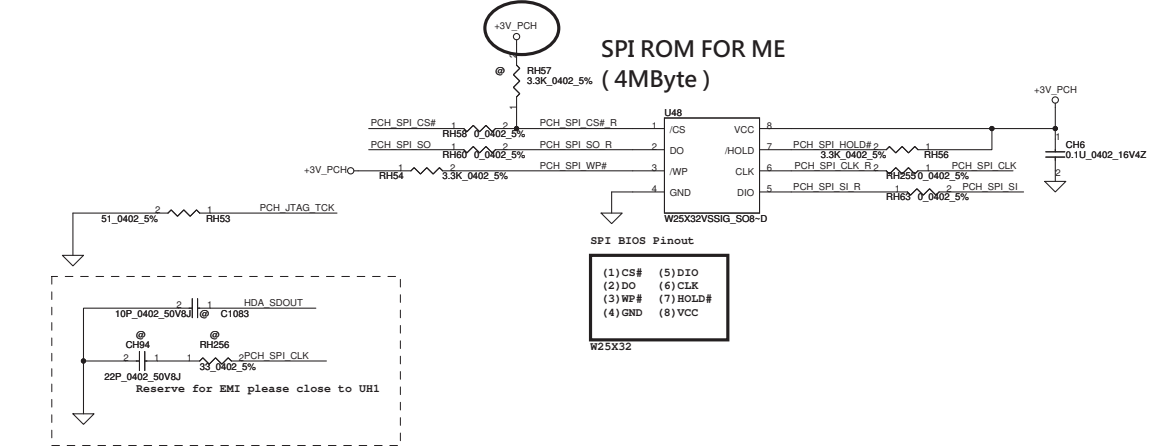
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DDRIII DIMMB



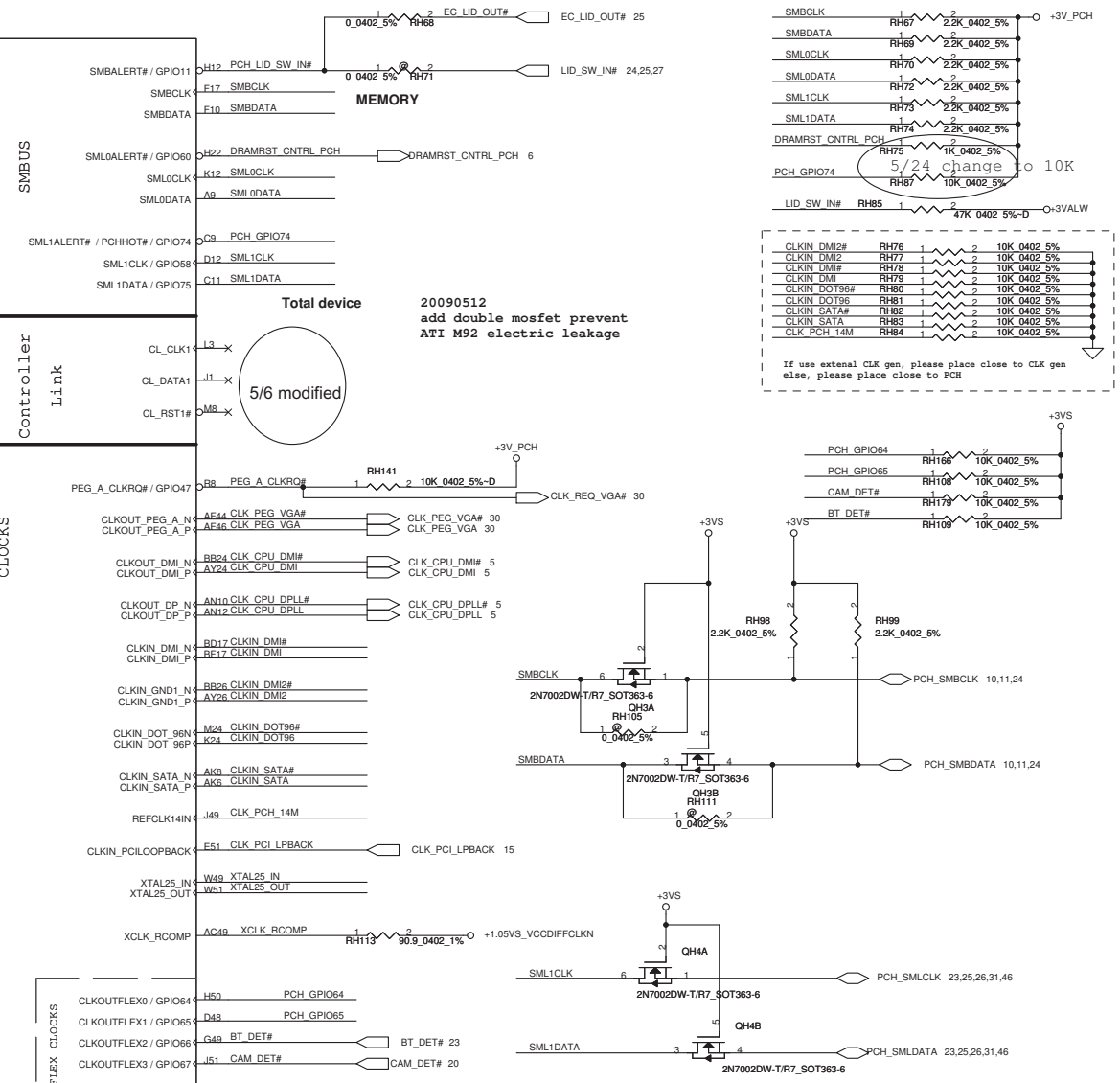
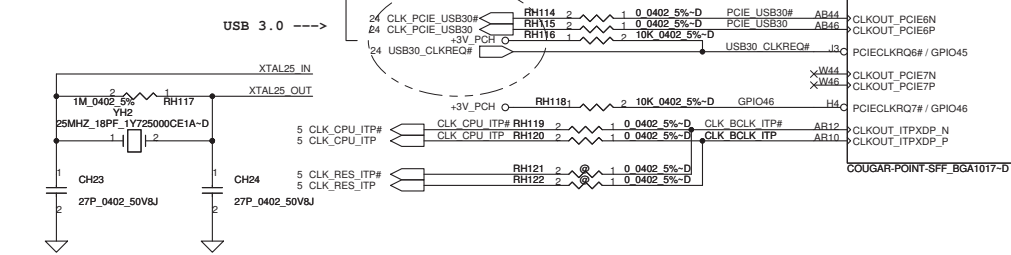
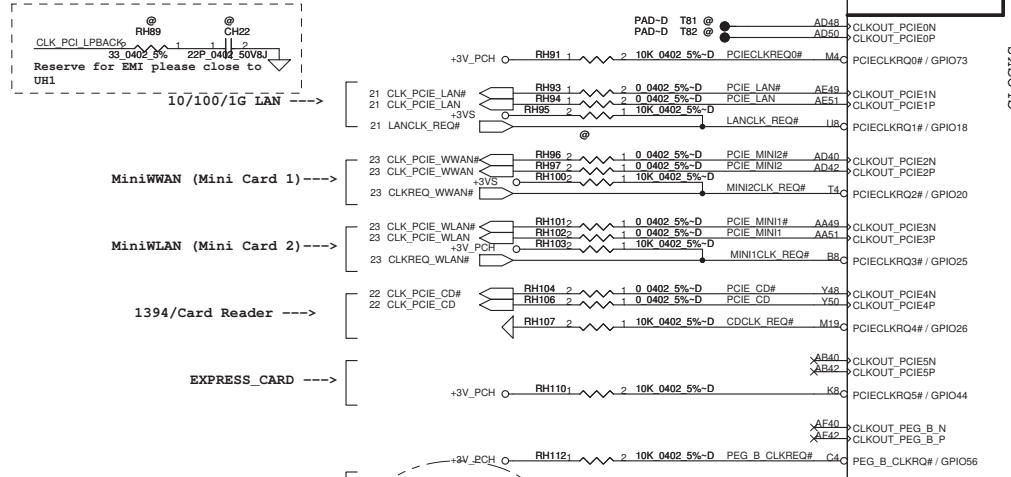
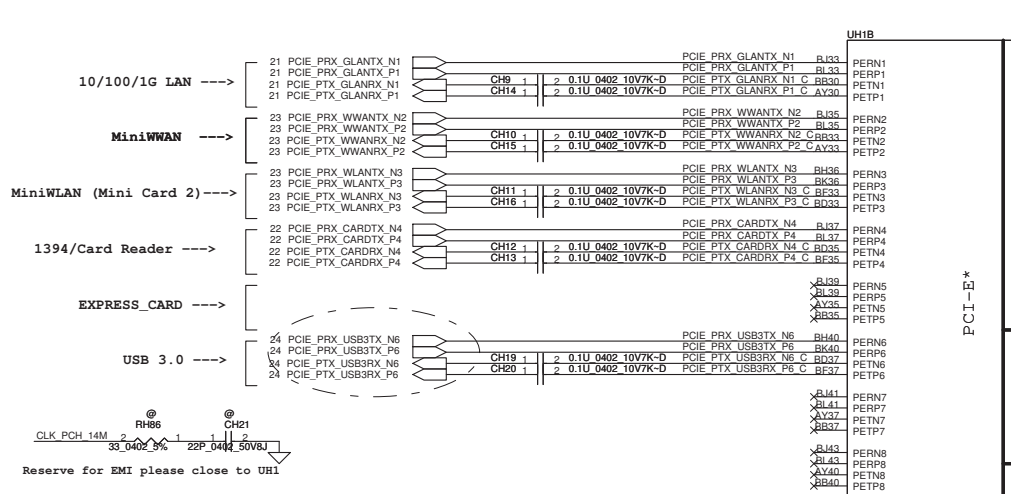
SPI ROM FOR ME (4MByte)

SPI ROM FOR ME (4MByte)

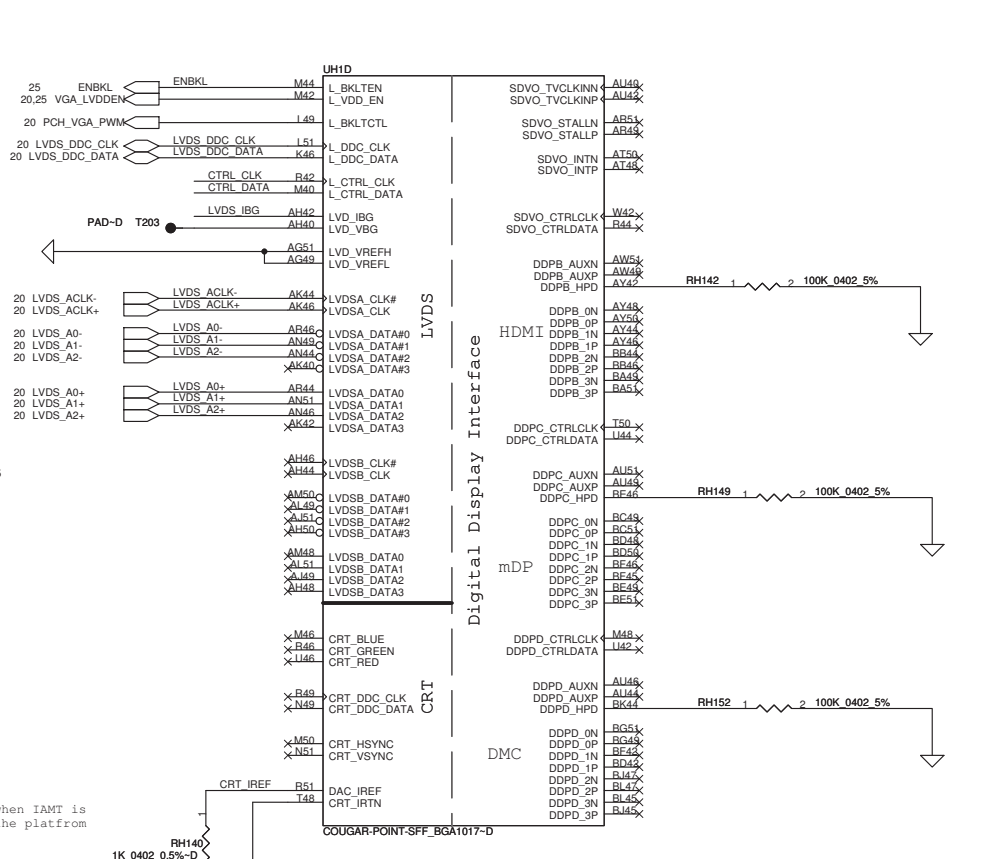
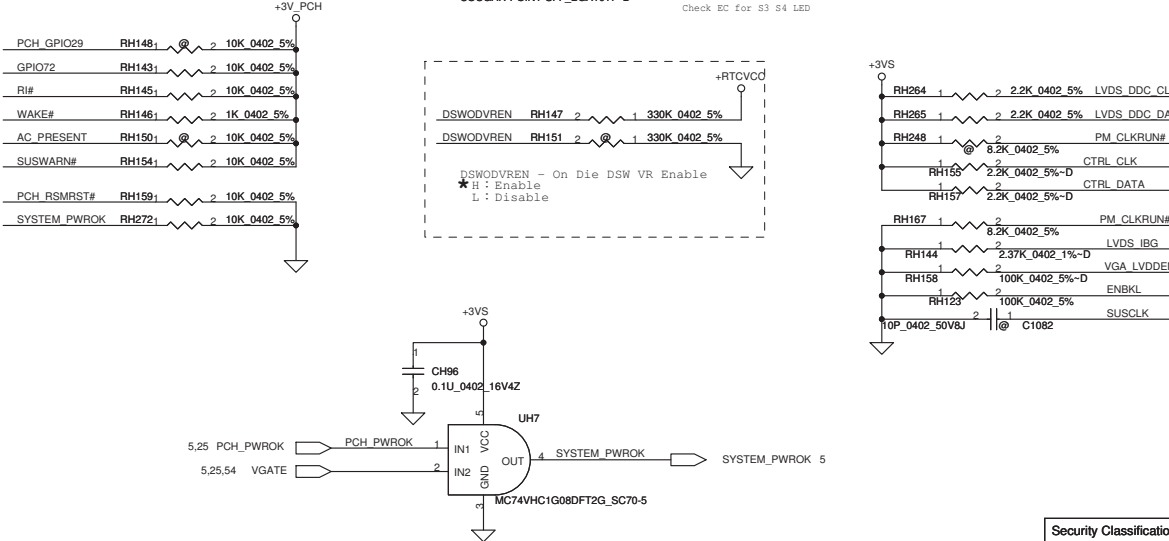
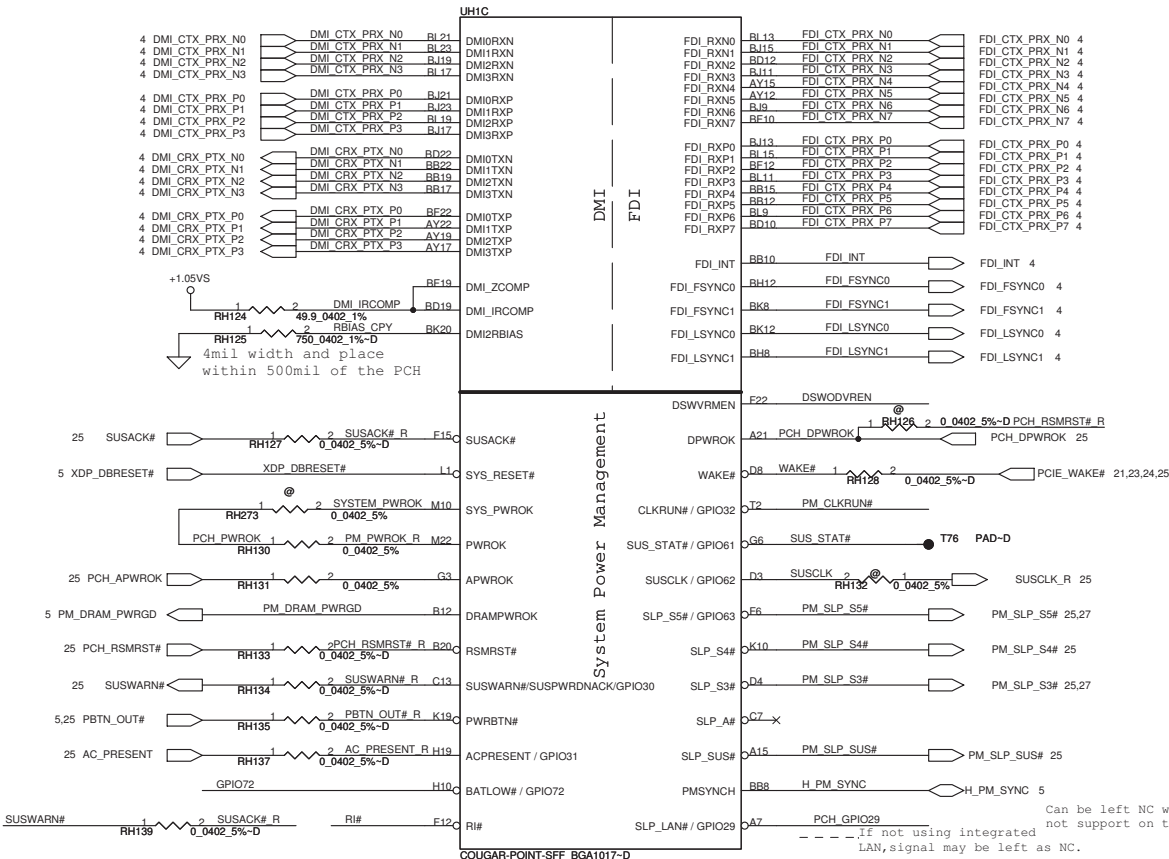


- SPI BIOS Pinout
- | | |
|---------|-----------|
| (1) CS# | (5) DIO |
| (2) DO | (6) CLK |
| (3) WP# | (7) HOLD# |
| (4) GND | (8) VCC |

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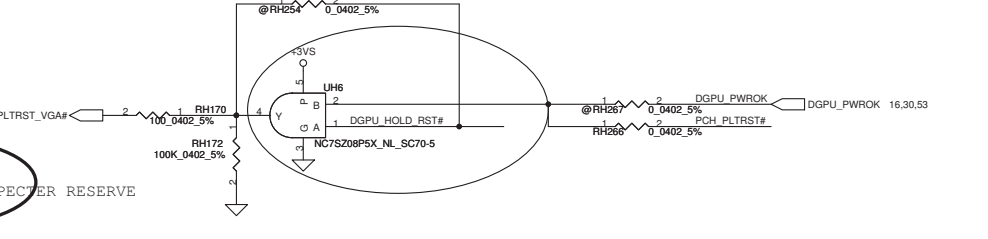
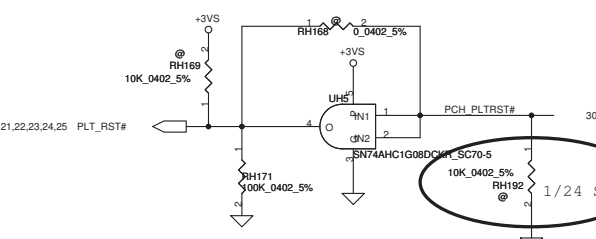
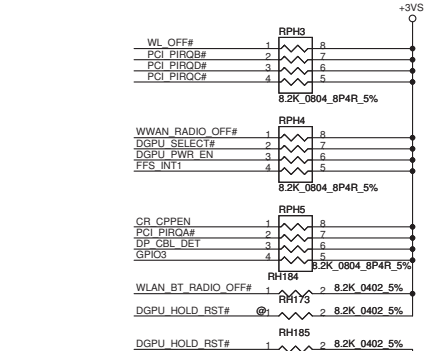
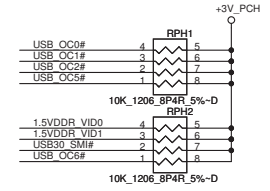
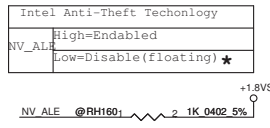
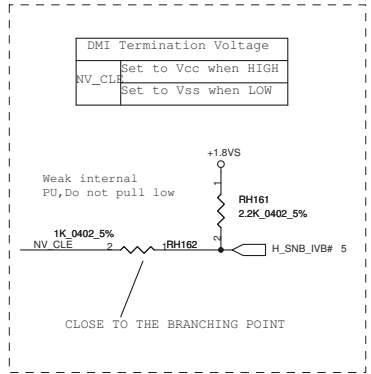
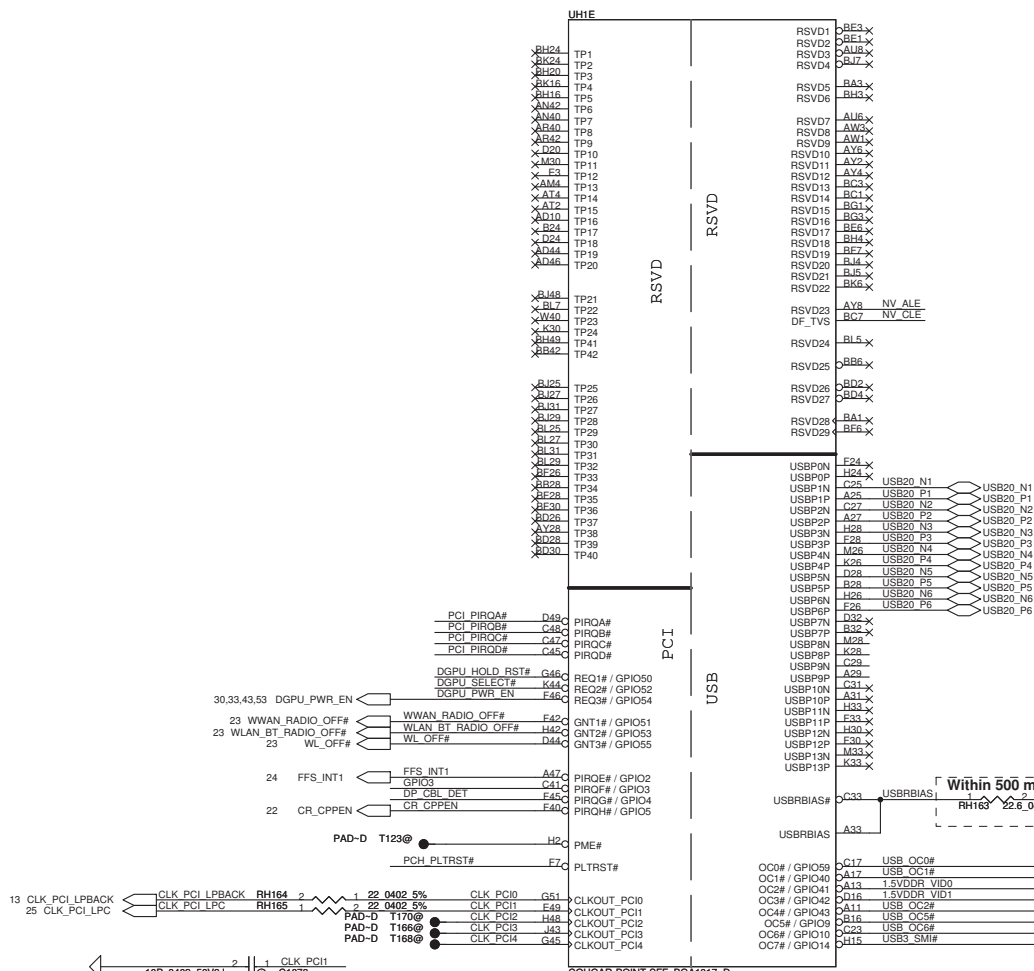


Security Classification	Compal Secret Data		Title PCH (2/8) PCIE, SMBUS, CLK
Issued Date	2010/07/06	Deciphered Date	
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Size	Document Number	Sheet	Rev
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Date:	Monday, January 24, 2011		

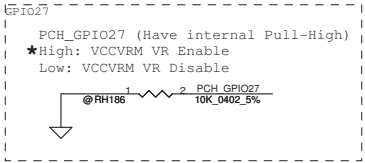
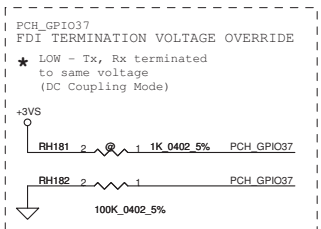
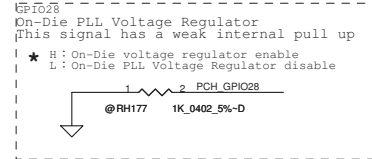


Security Classification				Compal Secret Data		Title	
Issued Date	2010/07/06	Deciphered Date	2011/07/06	Compal Electronics, Inc.			
				PCH (3/8) DMI, FDI, PM, GFX, DP			
				LA-6961P			
				Monday, January 24, 2011 Sheet 14 of 54			

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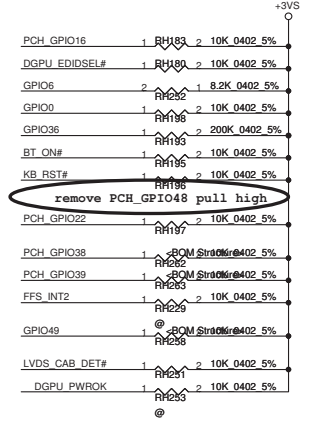
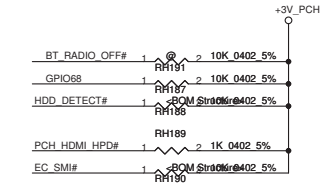
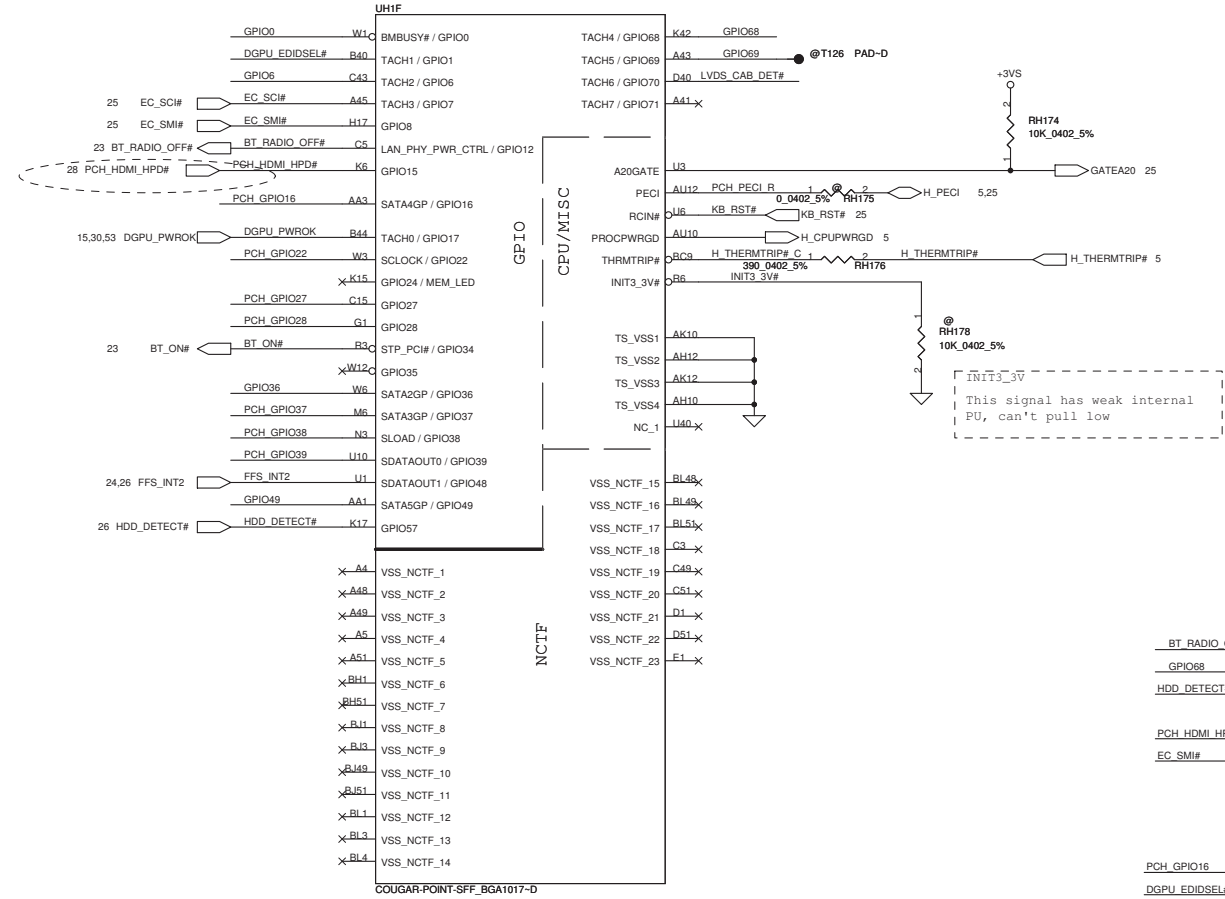


Security Classification	Compal Secret Data		Title PCH (4/8) PCI, USB, NVRAM
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Date: Tuesday, January 25, 2011			Sheet 15 of 54



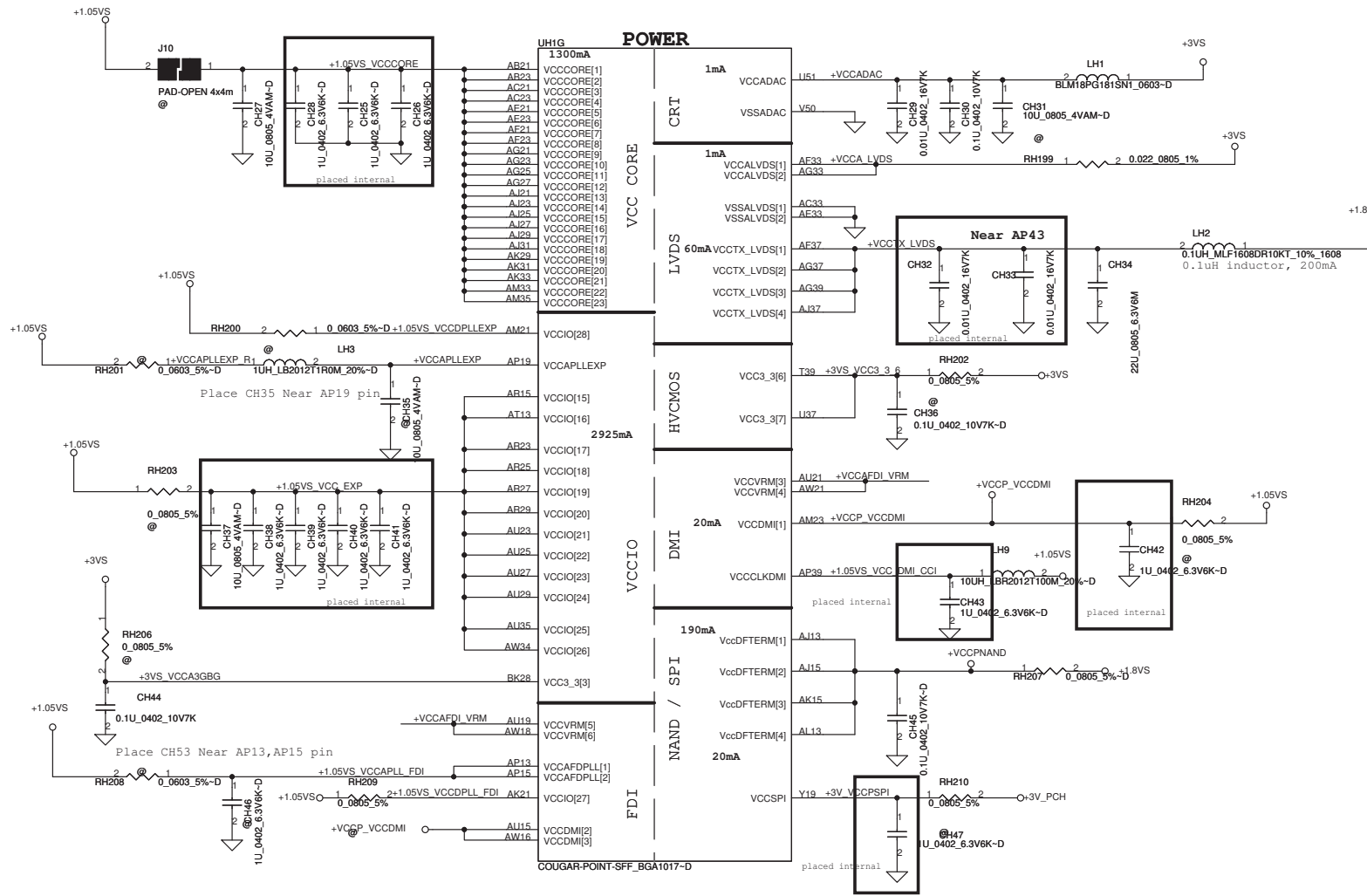
PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16

Please refer to Huron River Debug Board DG 0.5



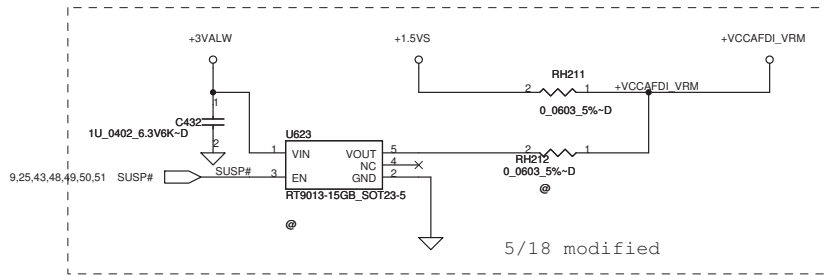
add RH185, RH229, RH251
5/25

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PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

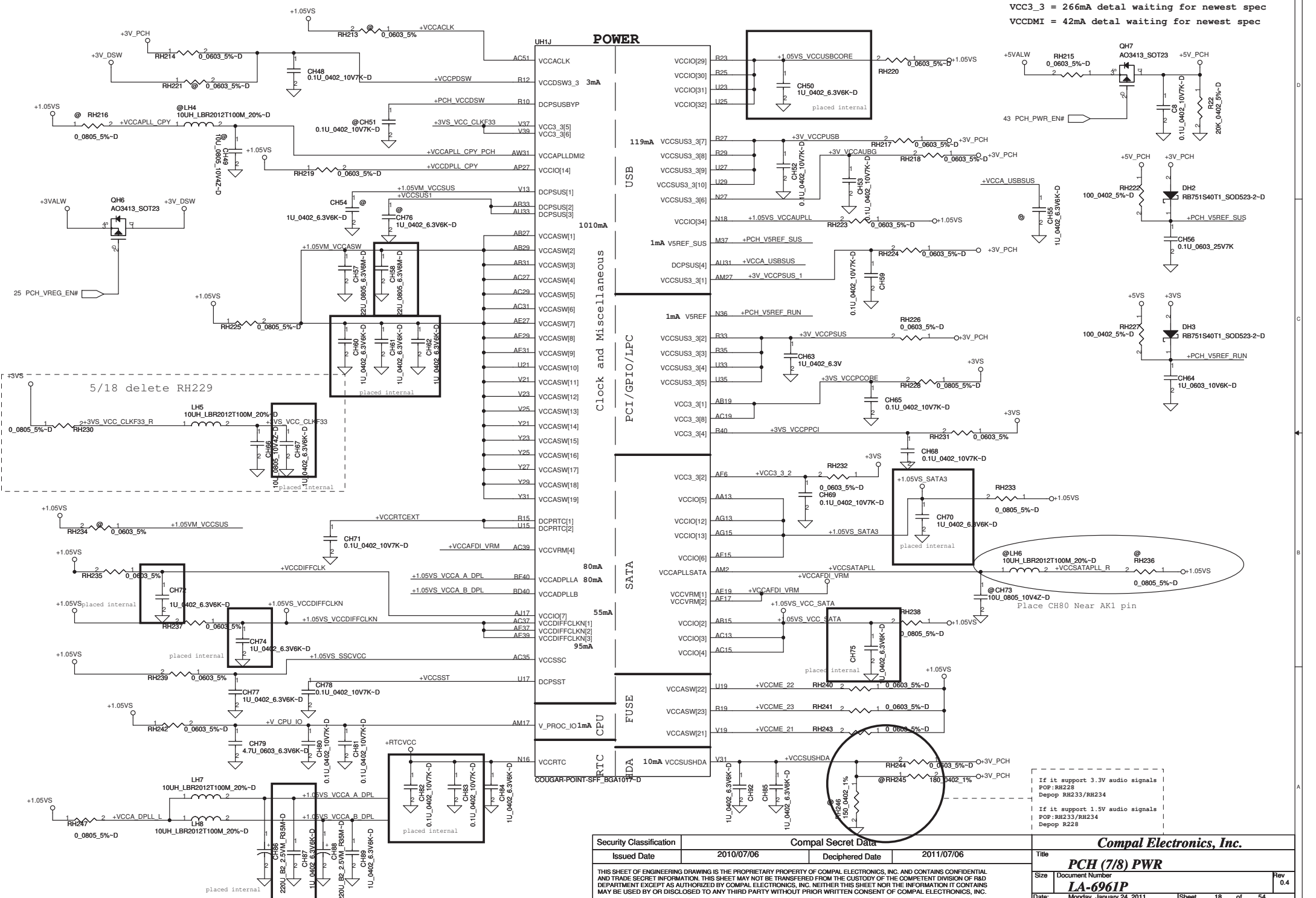
VCCVRM = 160mA detail waiting for newest spec



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Compal Electronics, Inc.		
Title	PCH (6/8) PWR	
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VCC3_3 = 266mA detail waiting for newest spec
 VCCDMI = 42mA detail waiting for newest spec



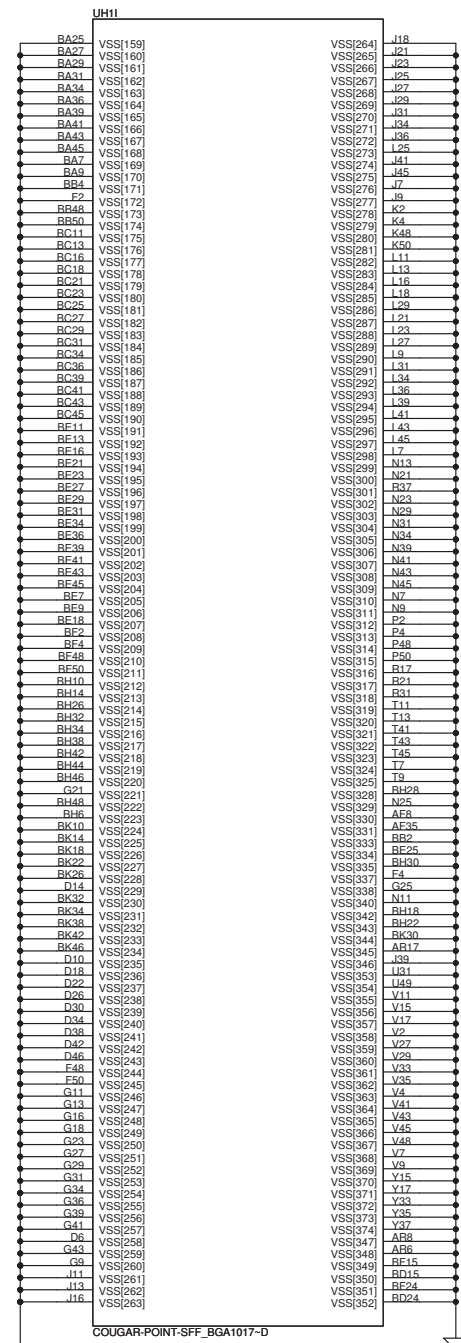
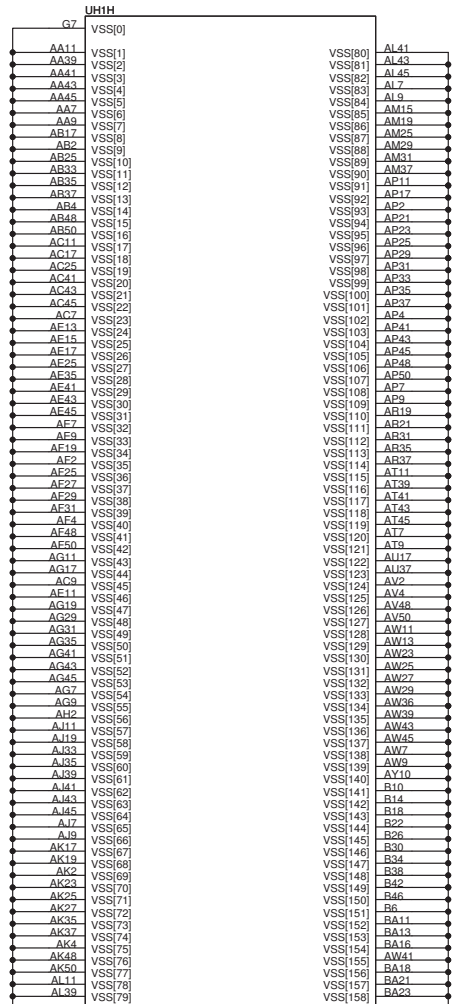
Security Classification	Compal Secret Data	
Issued Date	2010/07/06	Deciphered Date
		2011/07/06

Compal Electronics, Inc.		
Title		
PCH (7/8) PWR		
Size	Document Number	Rev
	LA-6961P	0.4
Date:	Monday, January 24, 2011	Sheet 18 of 54

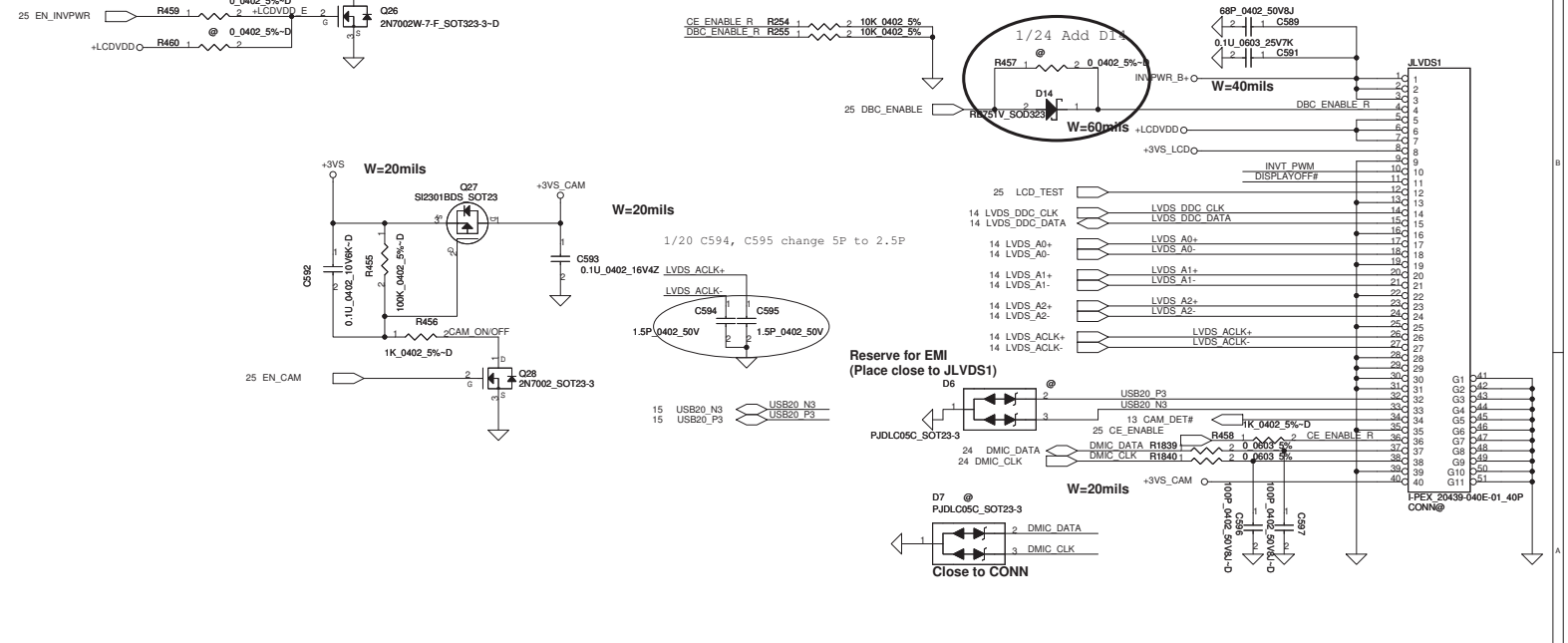
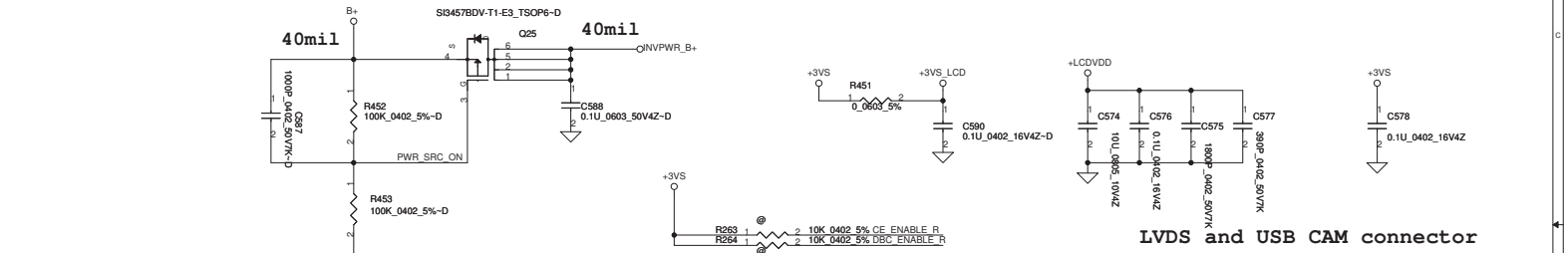
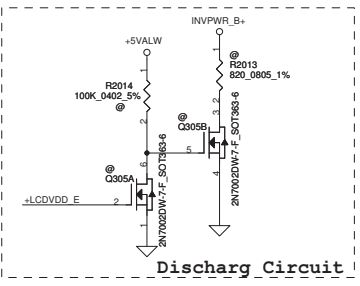
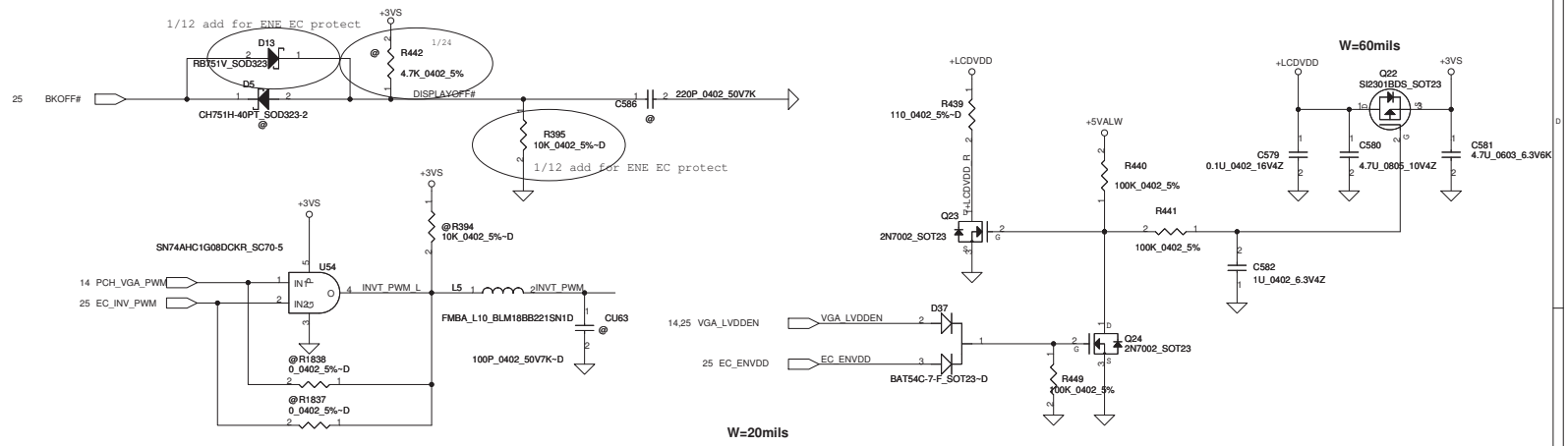
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If it support 3.3V audio signals
 POP: RH228
 Depop: RH233/RH234

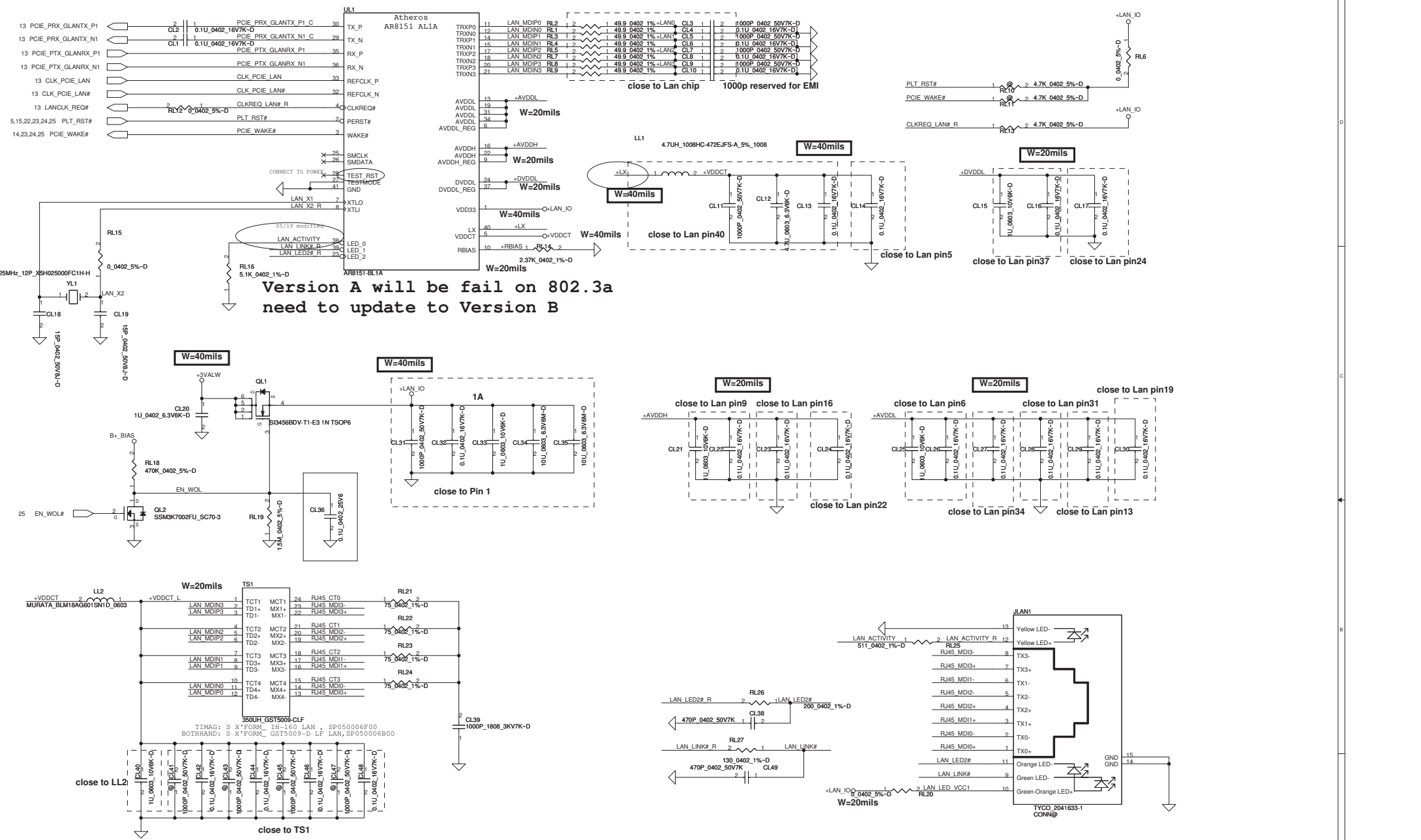
If it support 1.5V audio signals
 POP: RH233/RH234
 Depop: R228



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Date: Monday, January 24, 2011			Sheet: 19	of 54

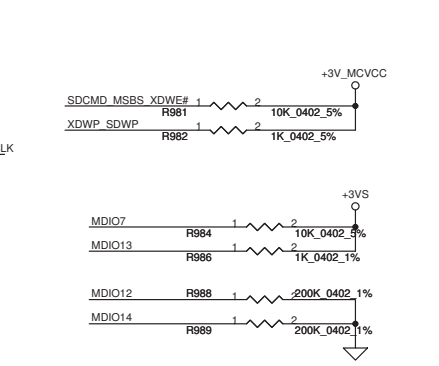
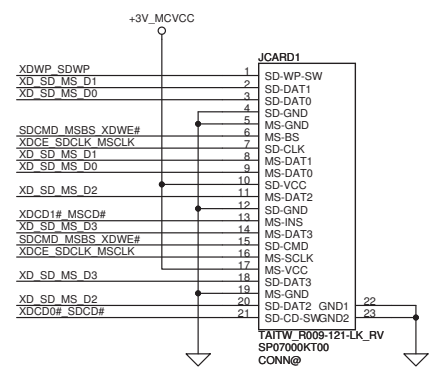


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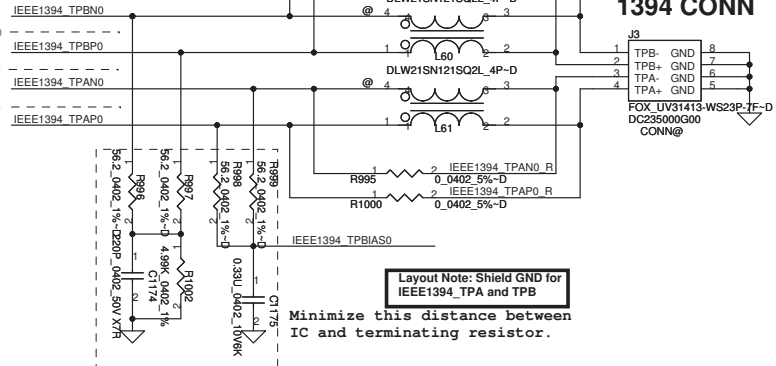


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Date:	Tuesday, January 25, 2011	Sheet	21 of 54

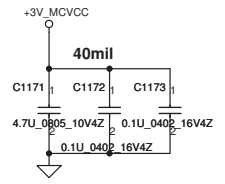
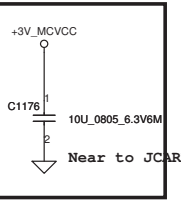
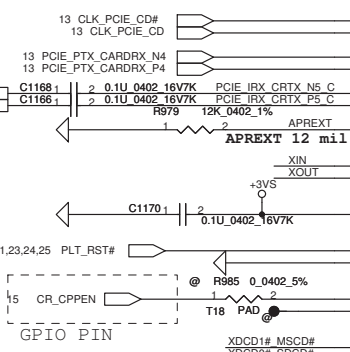
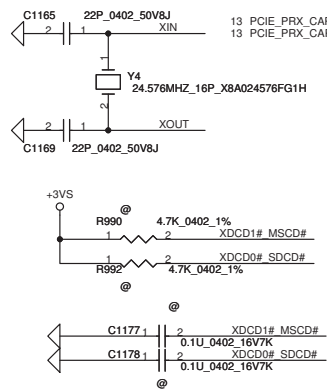
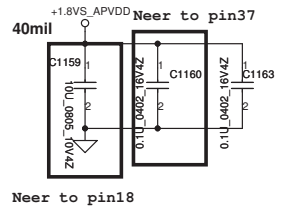
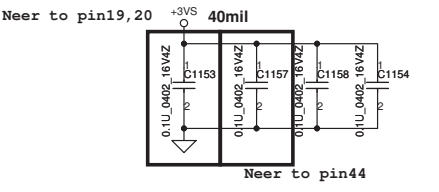
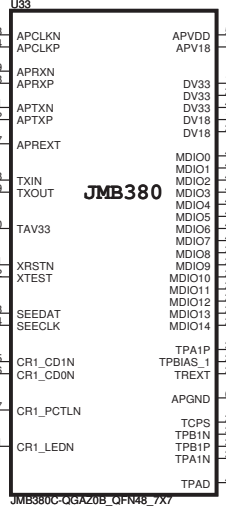
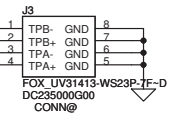
3 in 1 Card Reader CONN



Layout Note:
Add GND shield for 1394.



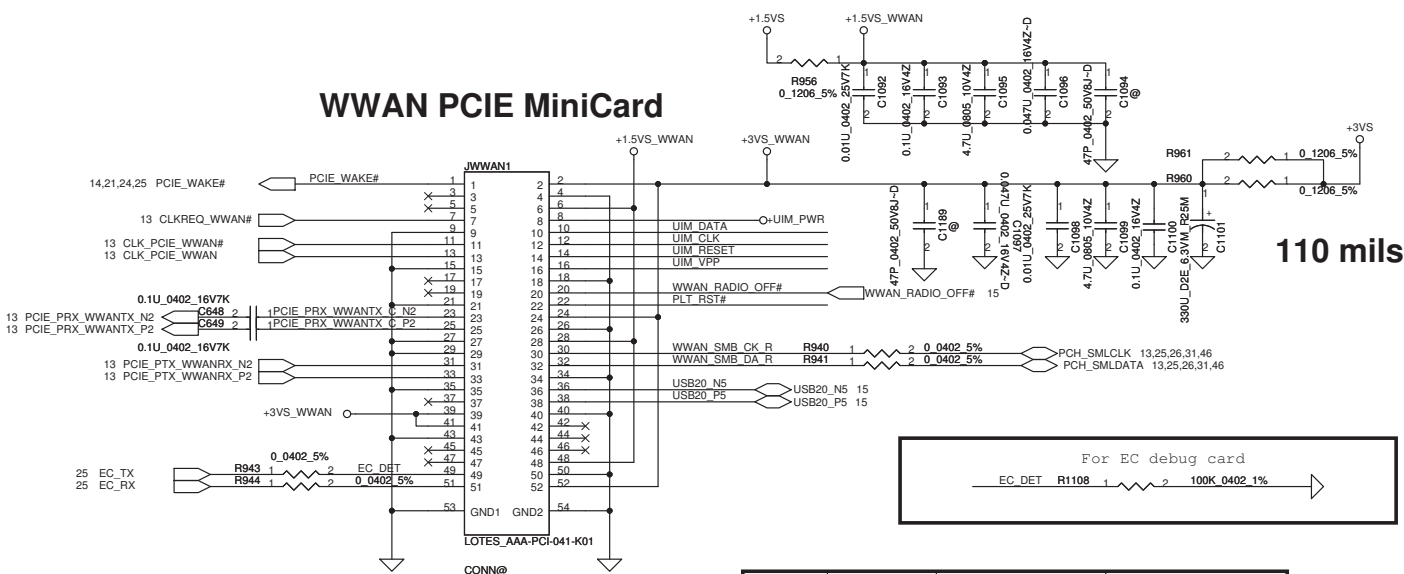
1394 CONN



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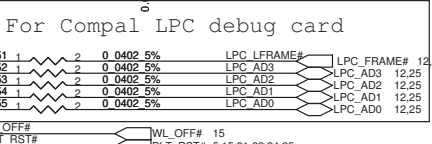
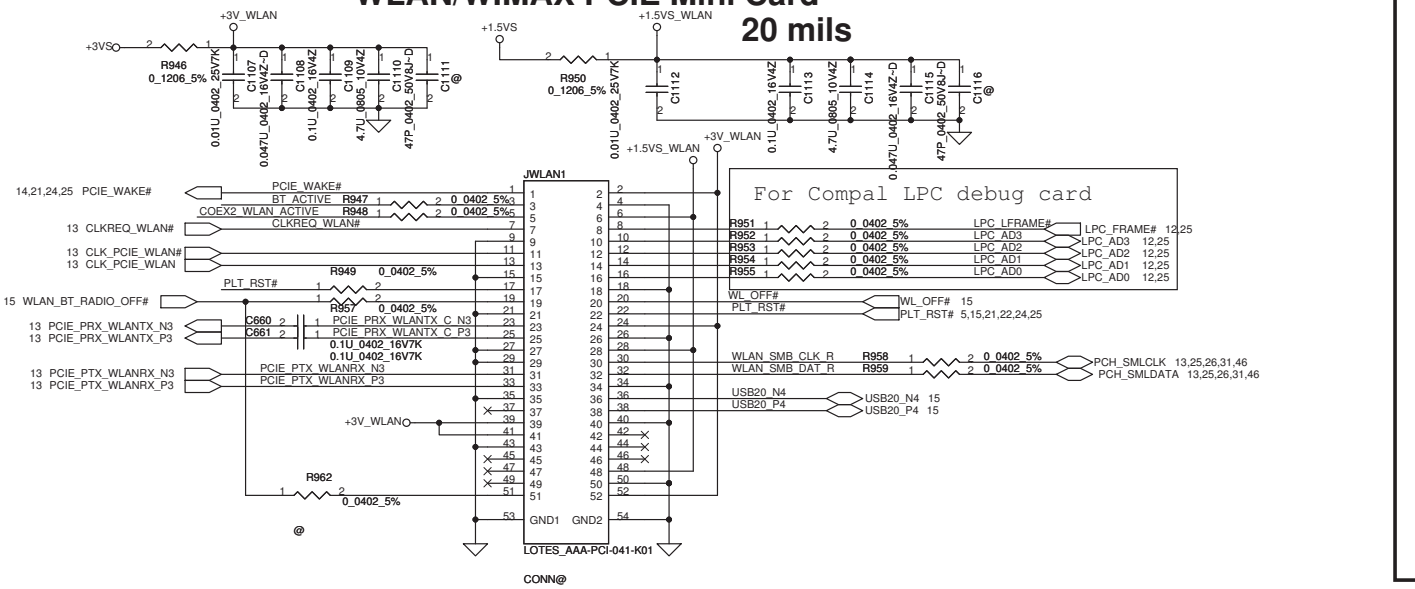
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WWAN PCIE MiniCard

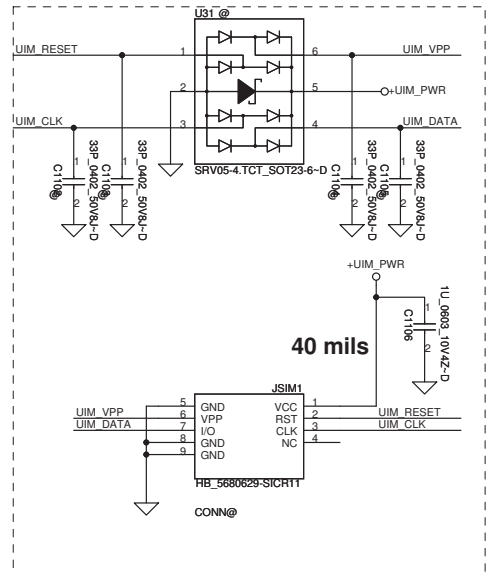


PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+/-9%	1000	750	
+3.3Vaux	+/-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+/-5%	500	375	NA

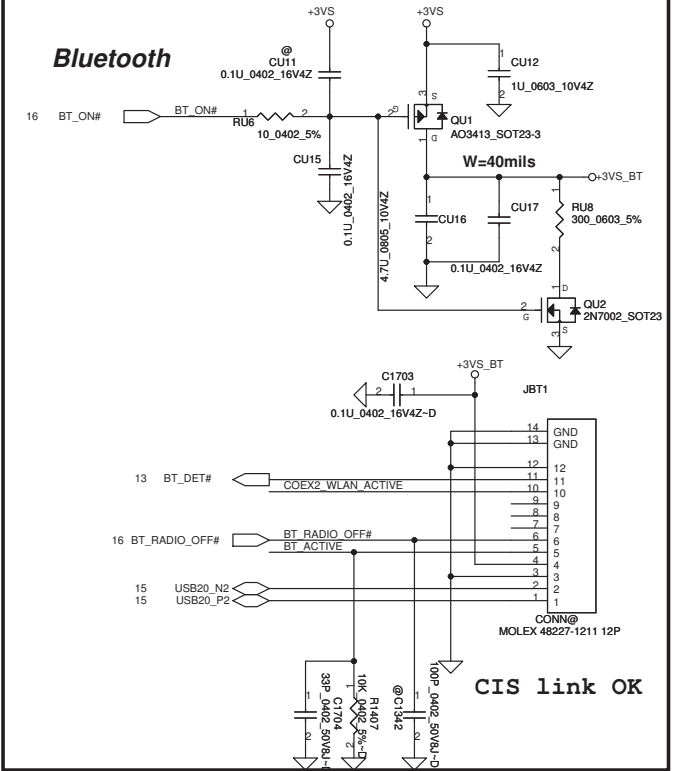
40 mils WLAN/WIMAX PCIE Mini Card



SIM Card



Bluetooth



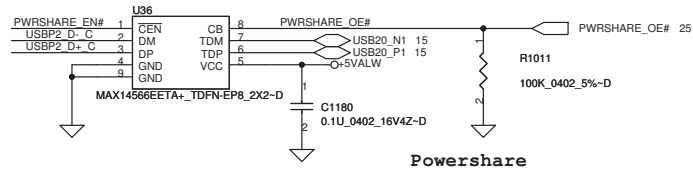
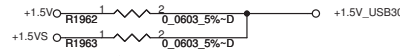
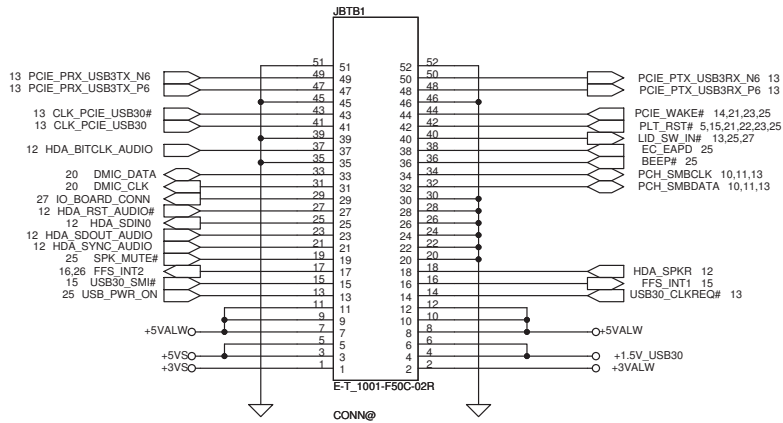
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Size	Document Number	Rev	
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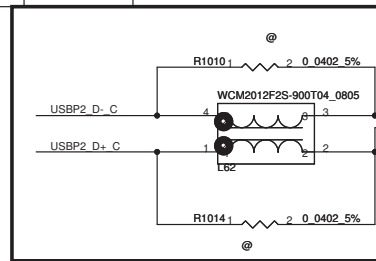
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IO Board CONN

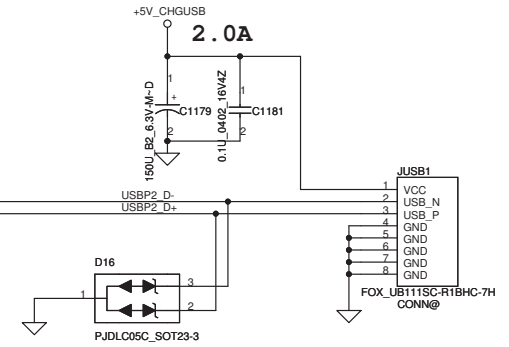
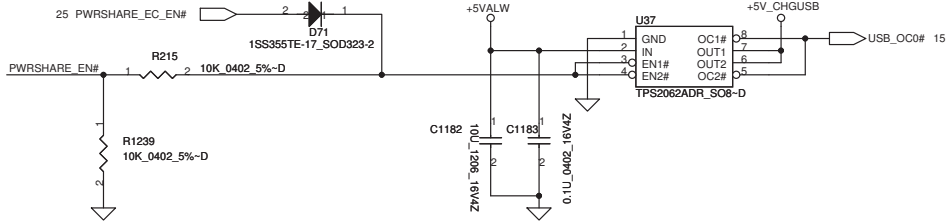


Powershare

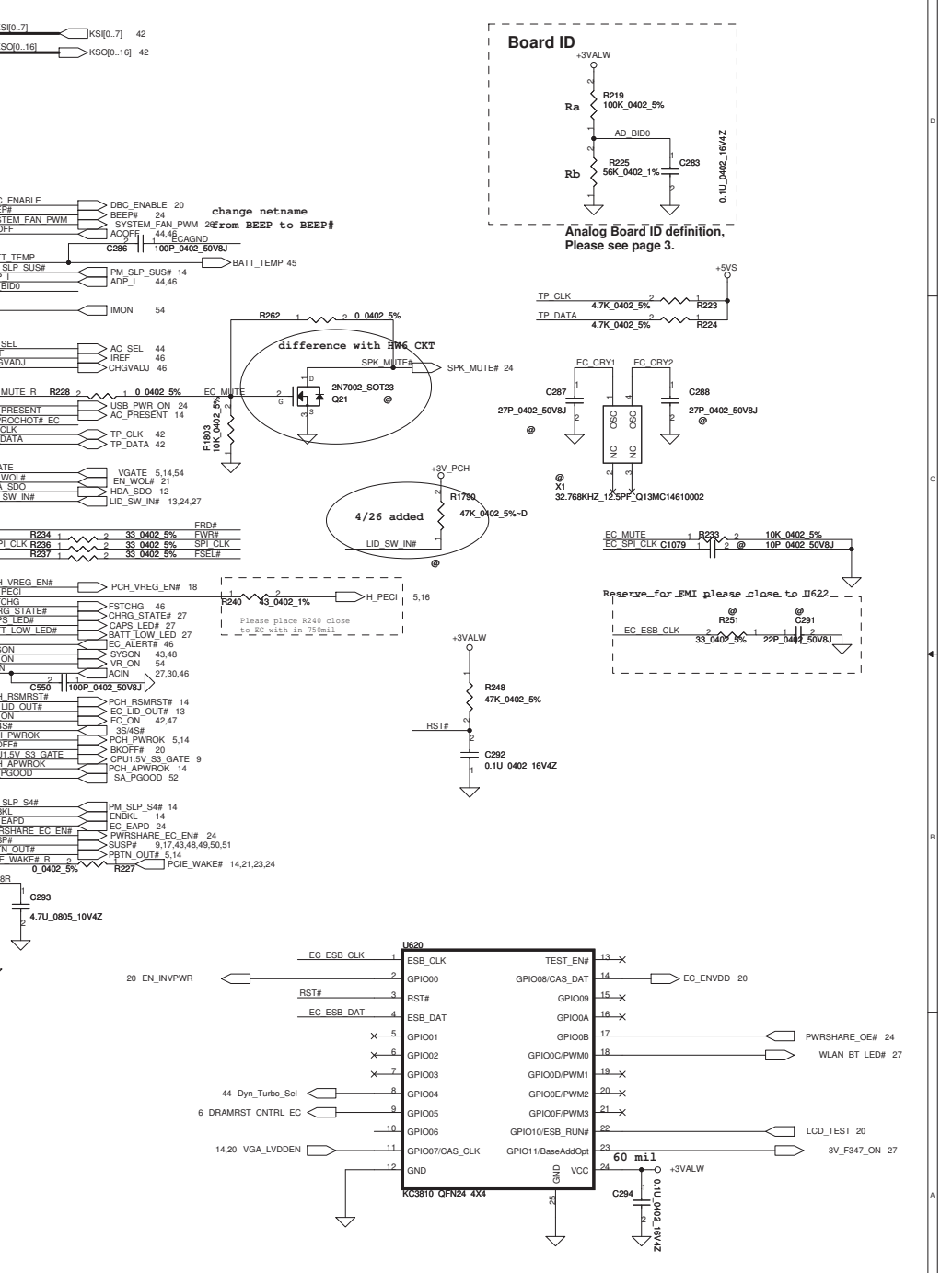
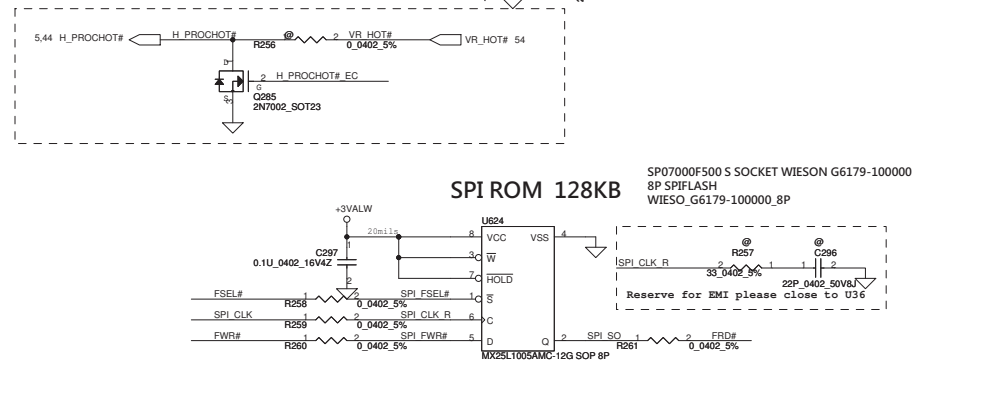
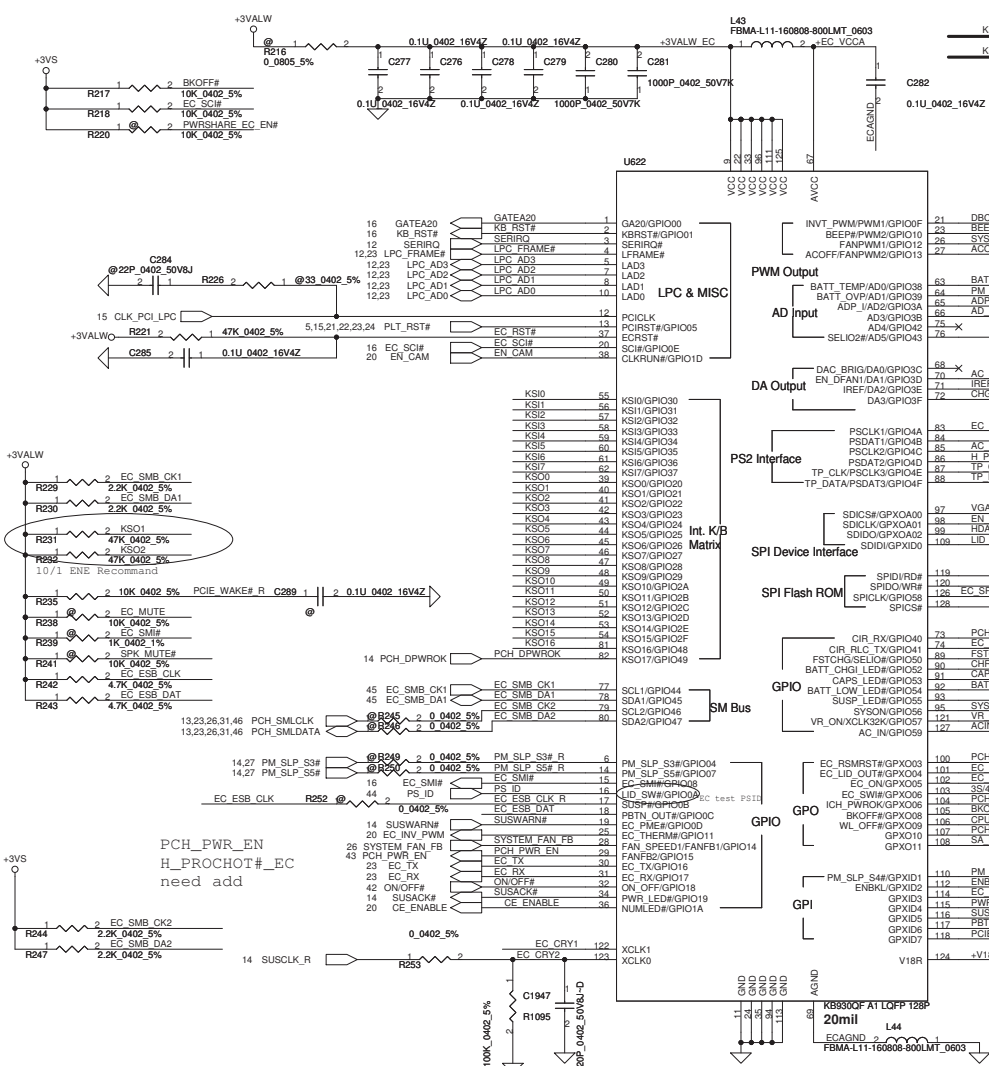
OE#	Function
L	Dect charger
H	D=1D



2.0A

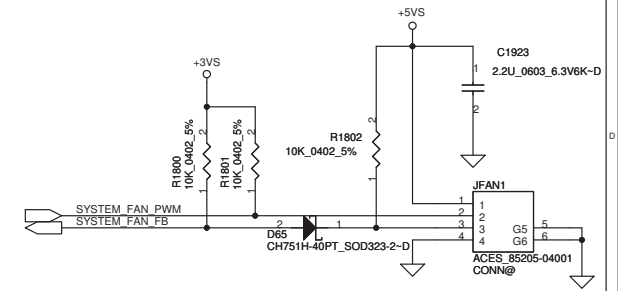
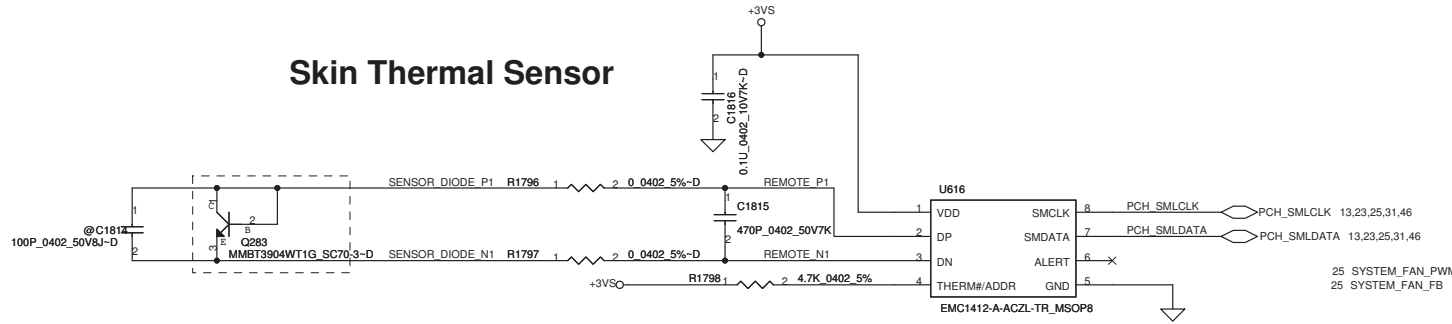


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				USB/LID SW/IO CONN	
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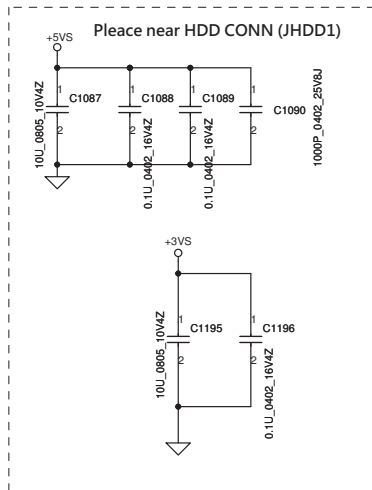
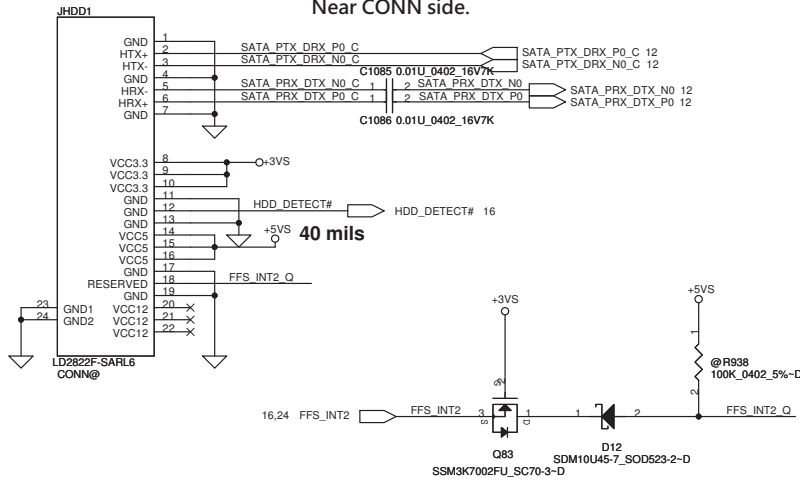
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Skin Thermal Sensor



HDD Connector

Near CONN side.

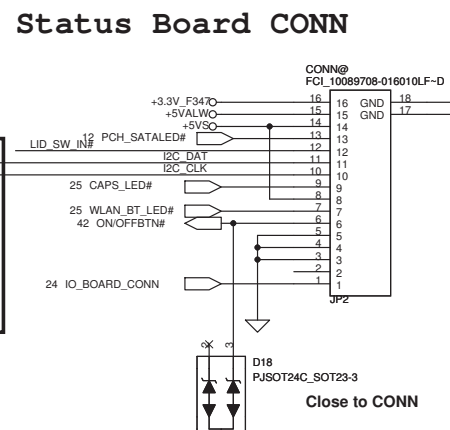
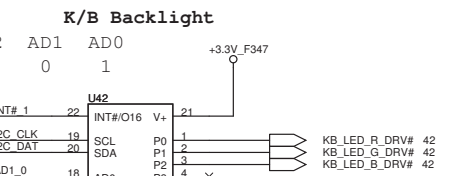
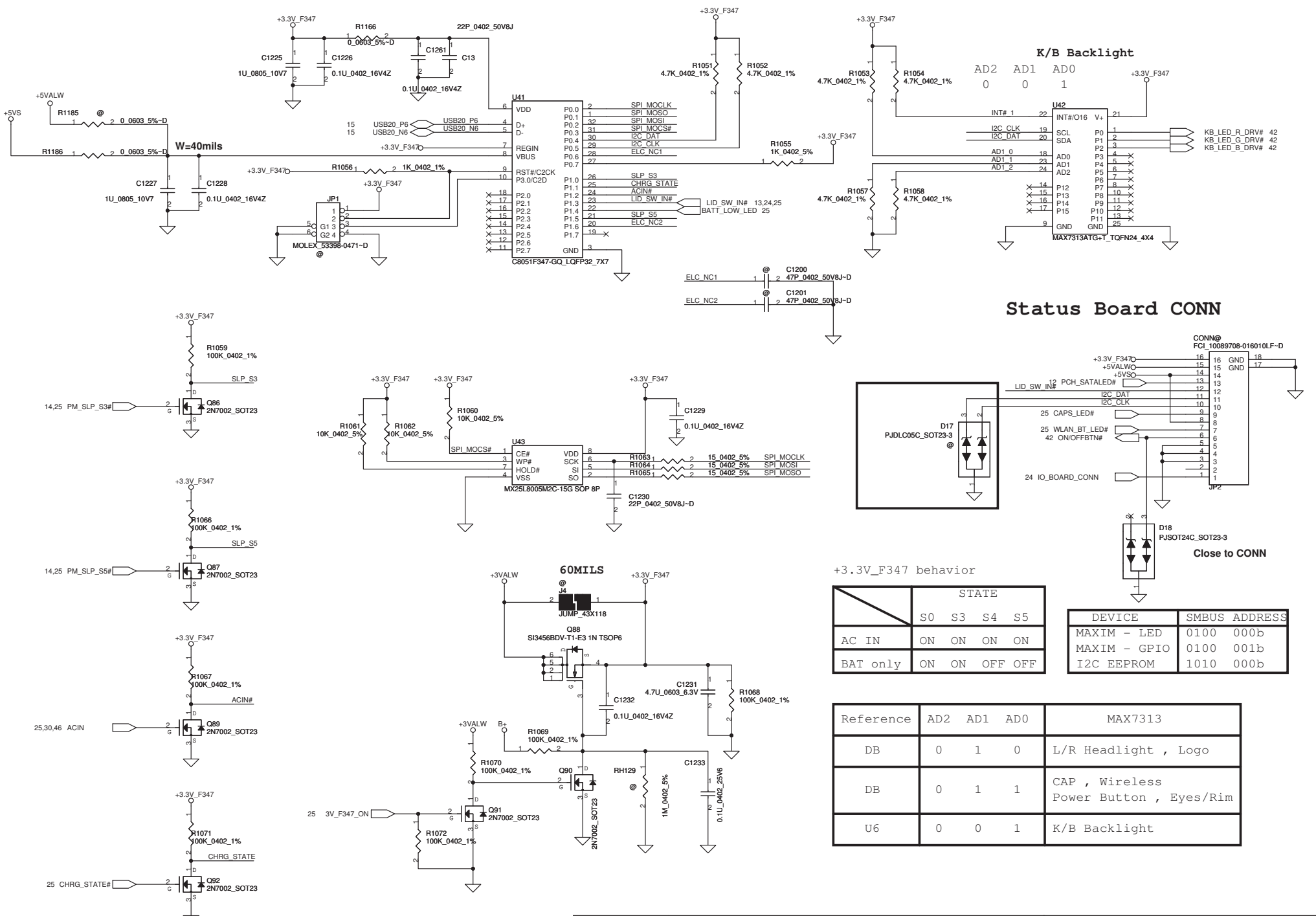


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Compal Electronics, Inc.

Title		
FAN & Thermal Sensor		
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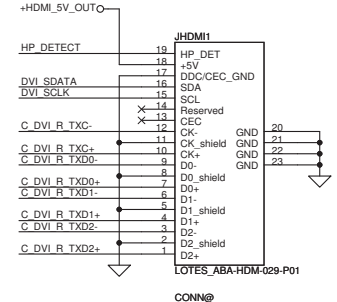
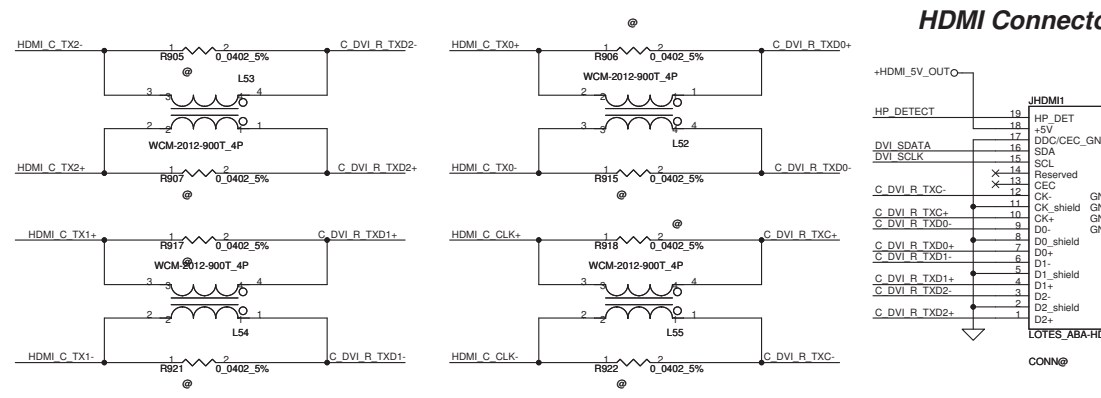
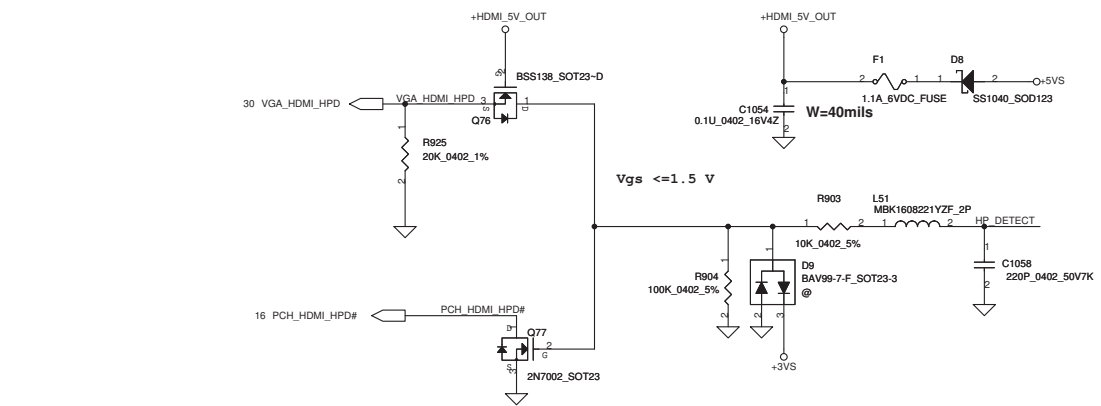
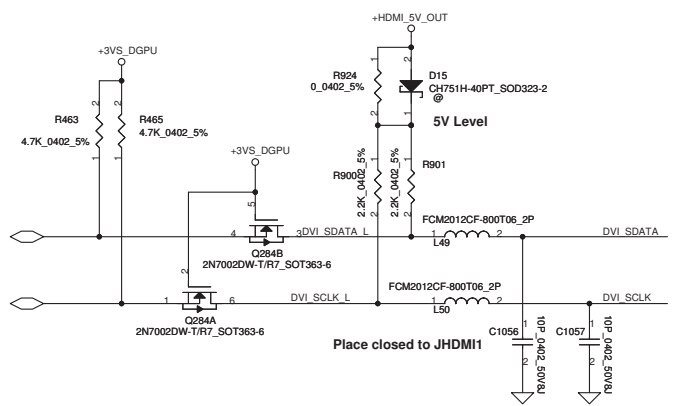
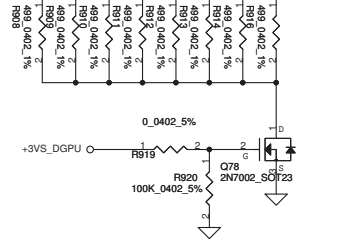
+3.3V_F347 behavior

	STATE			
	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BAT only	ON	ON	OFF	OFF

DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b

Reference	AD2	AD1	AD0	MAX7313
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DB	0	1	1	CAP , Wireless Power Button , Eyes/Rim
U6	0	0	1	K/B Backlight

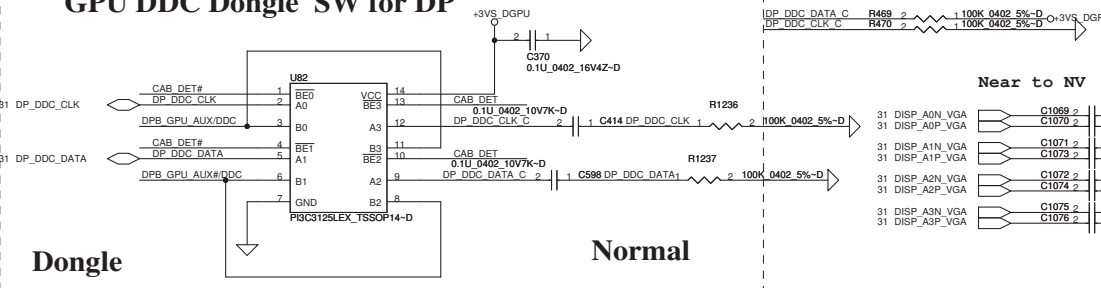
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31	VGA_HDMI_TX2+	VGA_HDMI_TX2+	C1060	2	1	0.1U_0402_16V7K	HDMI C_TX2+
31	VGA_HDMI_TX1-	VGA_HDMI_TX1-	C1061	2	1	0.1U_0402_16V7K	HDMI C_TX1-
31	VGA_HDMI_TX1+	VGA_HDMI_TX1+	C1062	2	1	0.1U_0402_16V7K	HDMI C_TX1+
31	VGA_HDMI_TX0-	VGA_HDMI_TX0-	C1063	2	1	0.1U_0402_16V7K	HDMI C_TX0-
31	VGA_HDMI_TX0+	VGA_HDMI_TX0+	C1064	2	1	0.1U_0402_16V7K	HDMI C_TX0+
31	VGA_HDMI_CLK-	VGA_HDMI_CLK-	C1065	2	1	0.1U_0402_16V7K	HDMI C_CLK-
31	VGA_HDMI_CLK+	VGA_HDMI_CLK+	C1066	2	1	0.1U_0402_16V7K	HDMI C_CLK+



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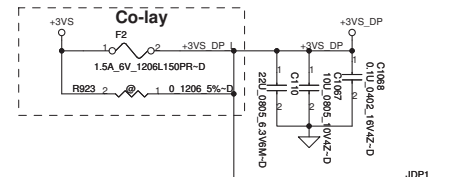
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.
Issued Date	2009/07/25	Deciphered Date	2011/07/06	HDMI
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				Document Number LA-6961P
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GPU DDC Dongle SW for DP



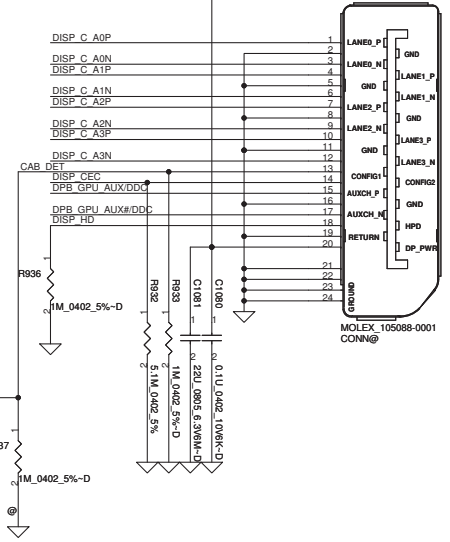
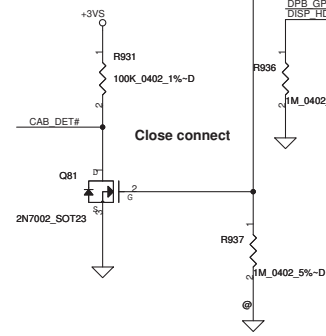
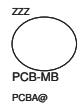
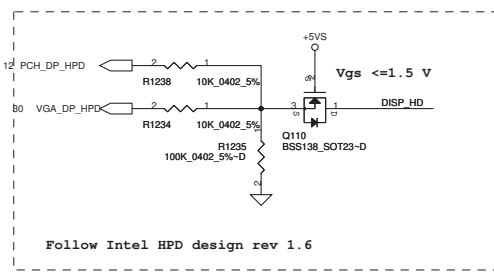
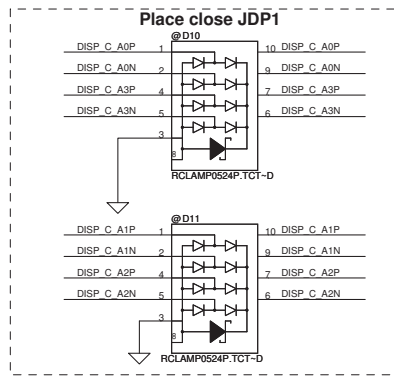
Dongle

Normal



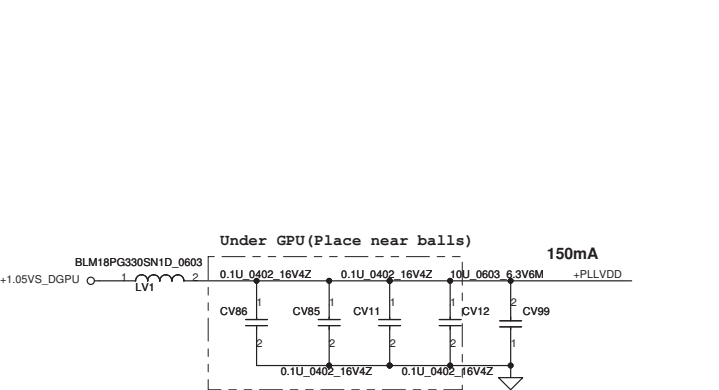
Near to NV

31 DISP_A0N_VGA	C1069	2	1	0.1U 0402 10V6K-D	DISP_C_A0N
31 DISP_A0P_VGA	C1070	2	1	0.1U 0402 10V6K-D	DISP_C_A0P
31 DISP_A1N_VGA	C1071	2	1	0.1U 0402 10V6K-D	DISP_C_A1N
31 DISP_A1P_VGA	C1073	2	1	0.1U 0402 10V6K-D	DISP_C_A1P
31 DISP_A2N_VGA	C1072	2	1	0.1U 0402 10V6K-D	DISP_C_A2N
31 DISP_A2P_VGA	C1074	2	1	0.1U 0402 10V6K-D	DISP_C_A2P
31 DISP_A3N_VGA	C1075	2	1	0.1U 0402 10V6K-D	DISP_C_A3N
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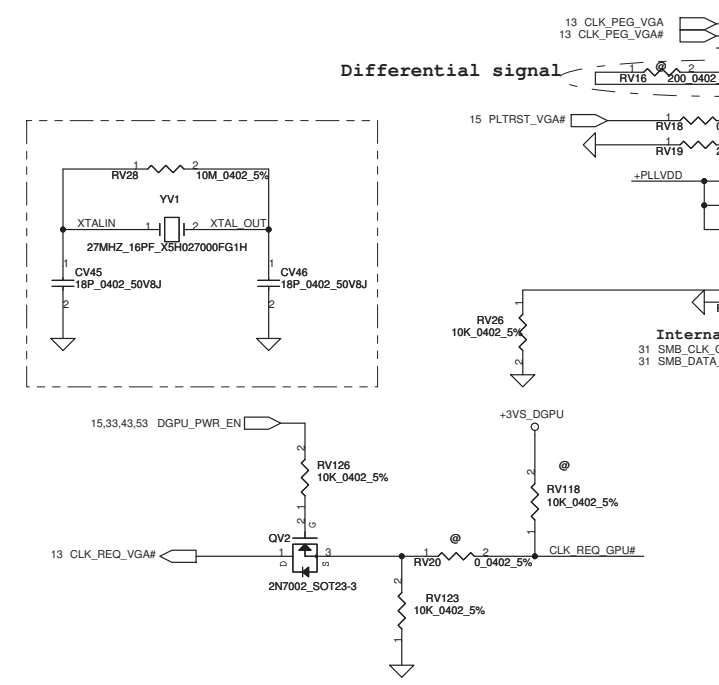


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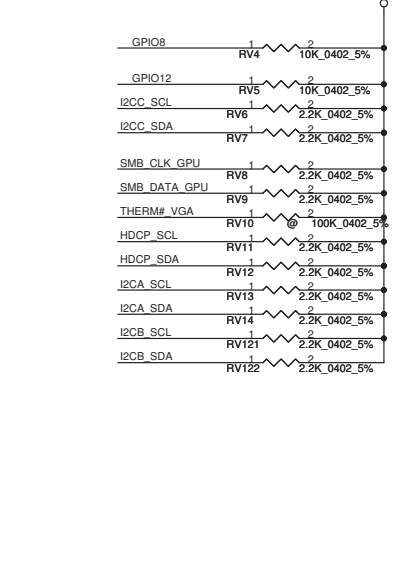
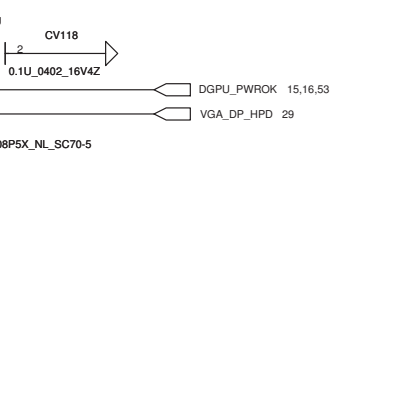
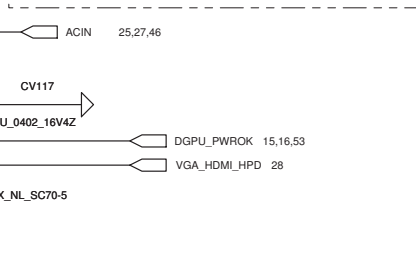
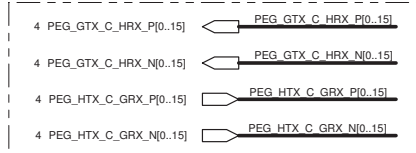
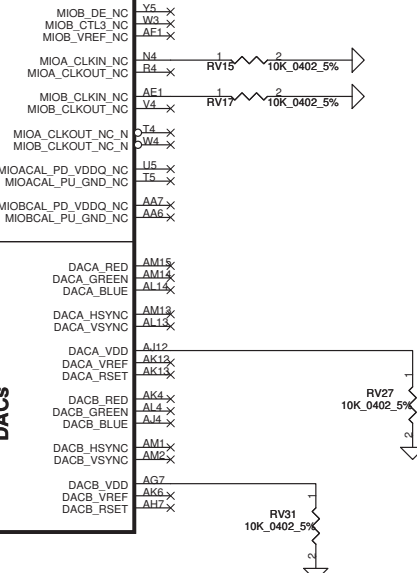
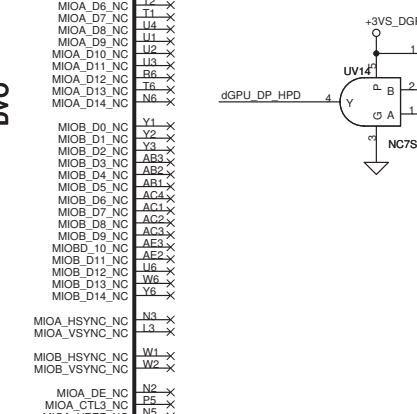
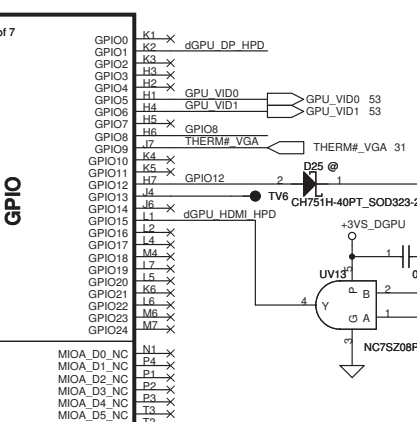
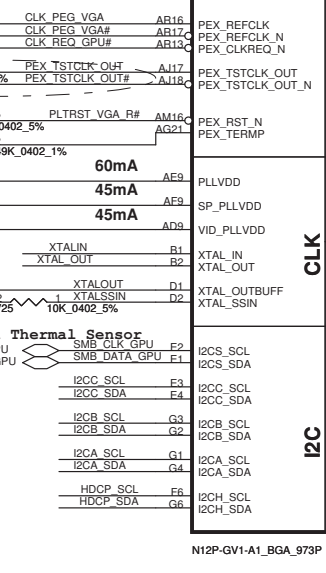


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PEG GTX C HRX P1	CV15	1	2	0.1U 0402 10V7K-D	PEG GTX CRX P1	AM18
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PEG HTX C GRX N14	AN31
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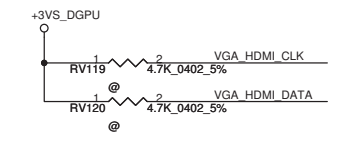
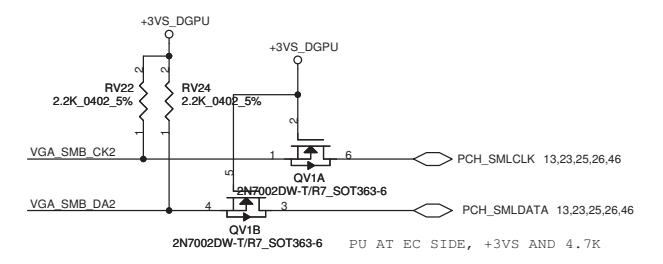
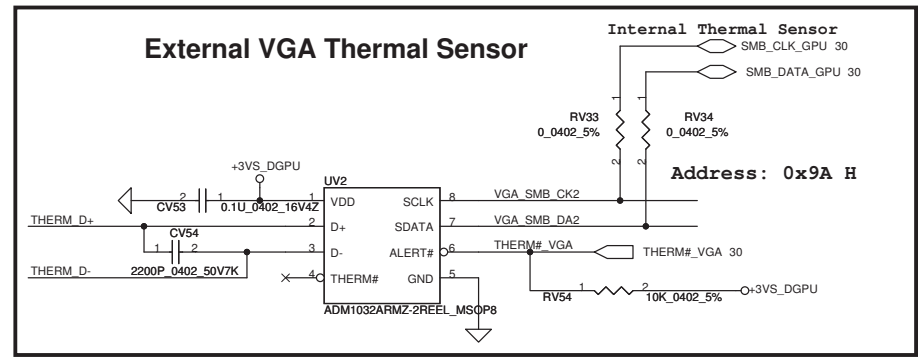
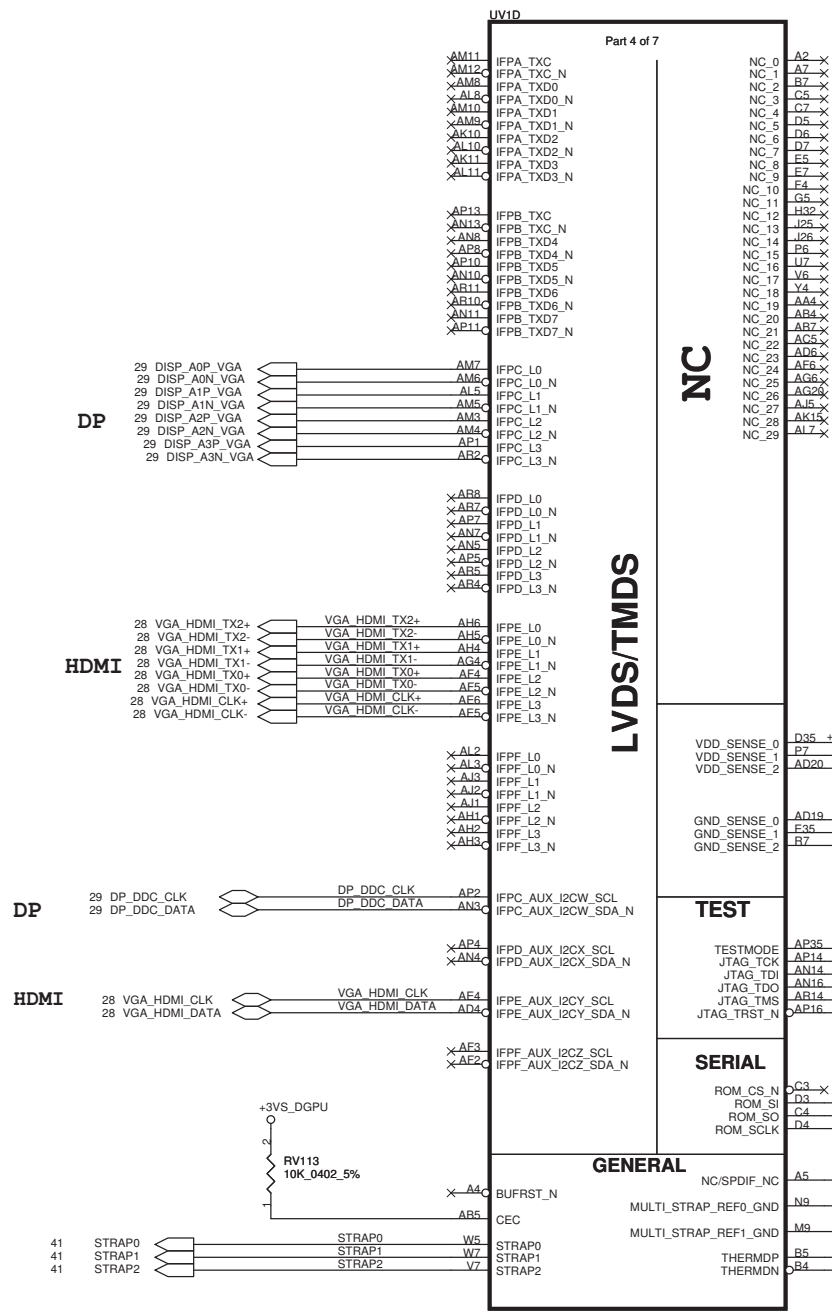
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VGA(1/12)-PCIE/DAC/GPIO

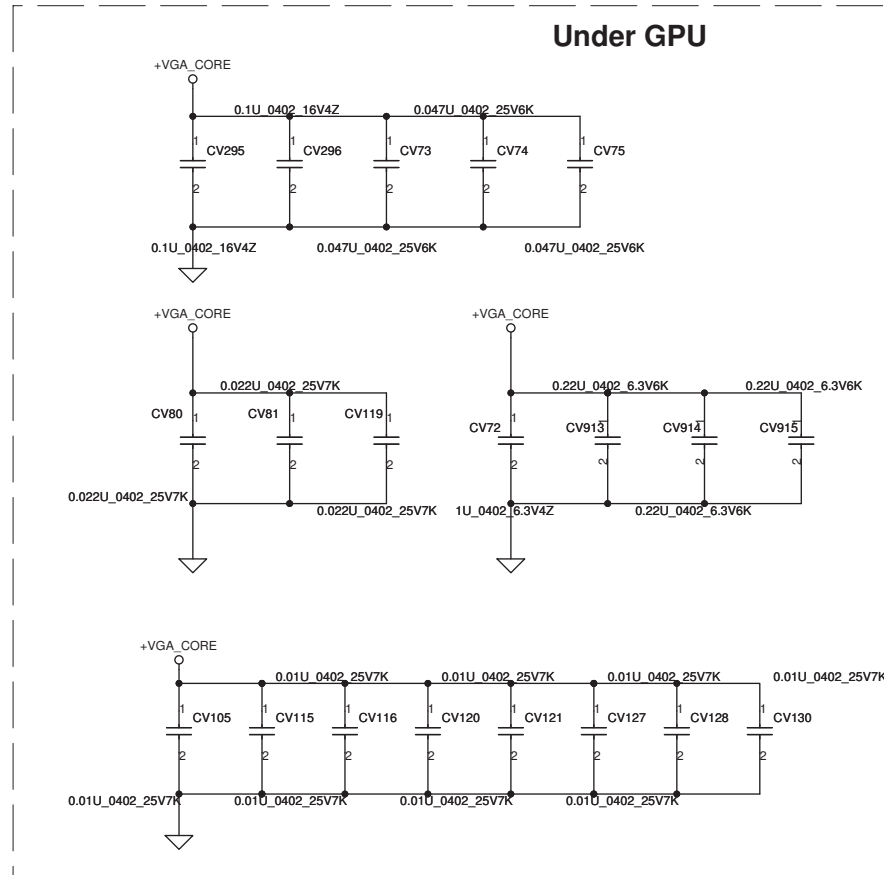
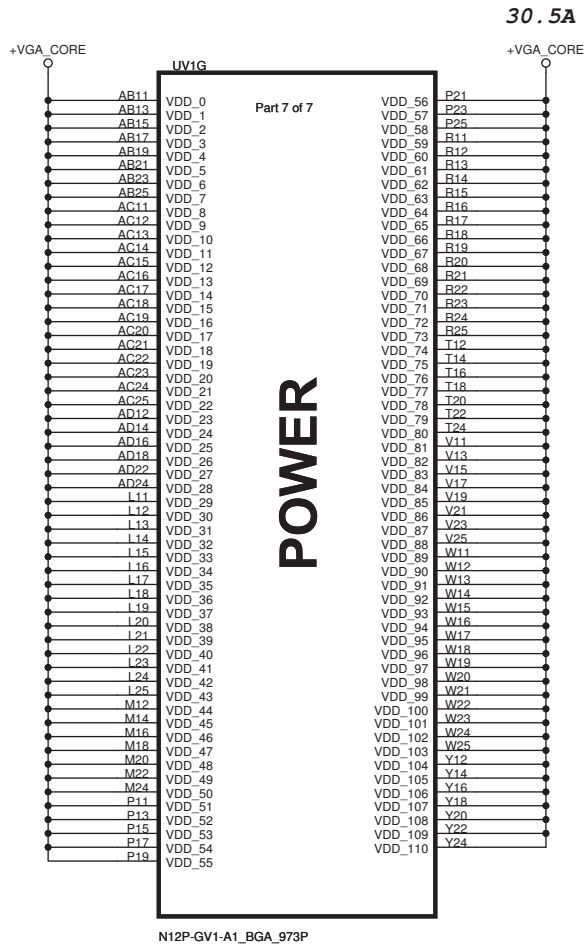
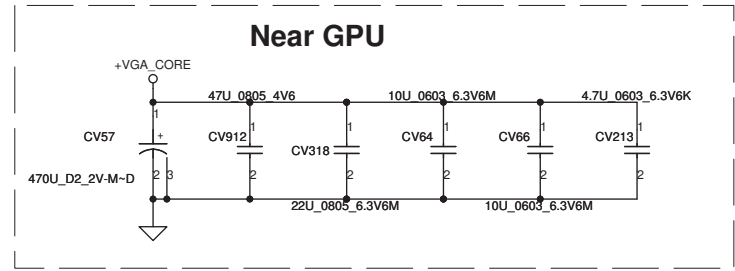
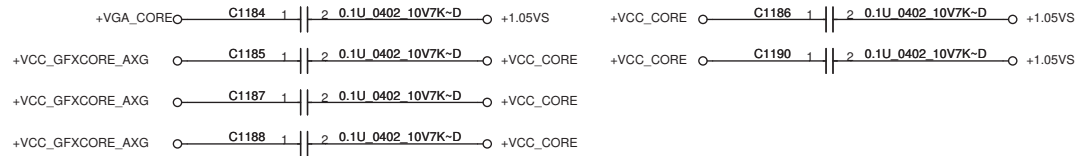
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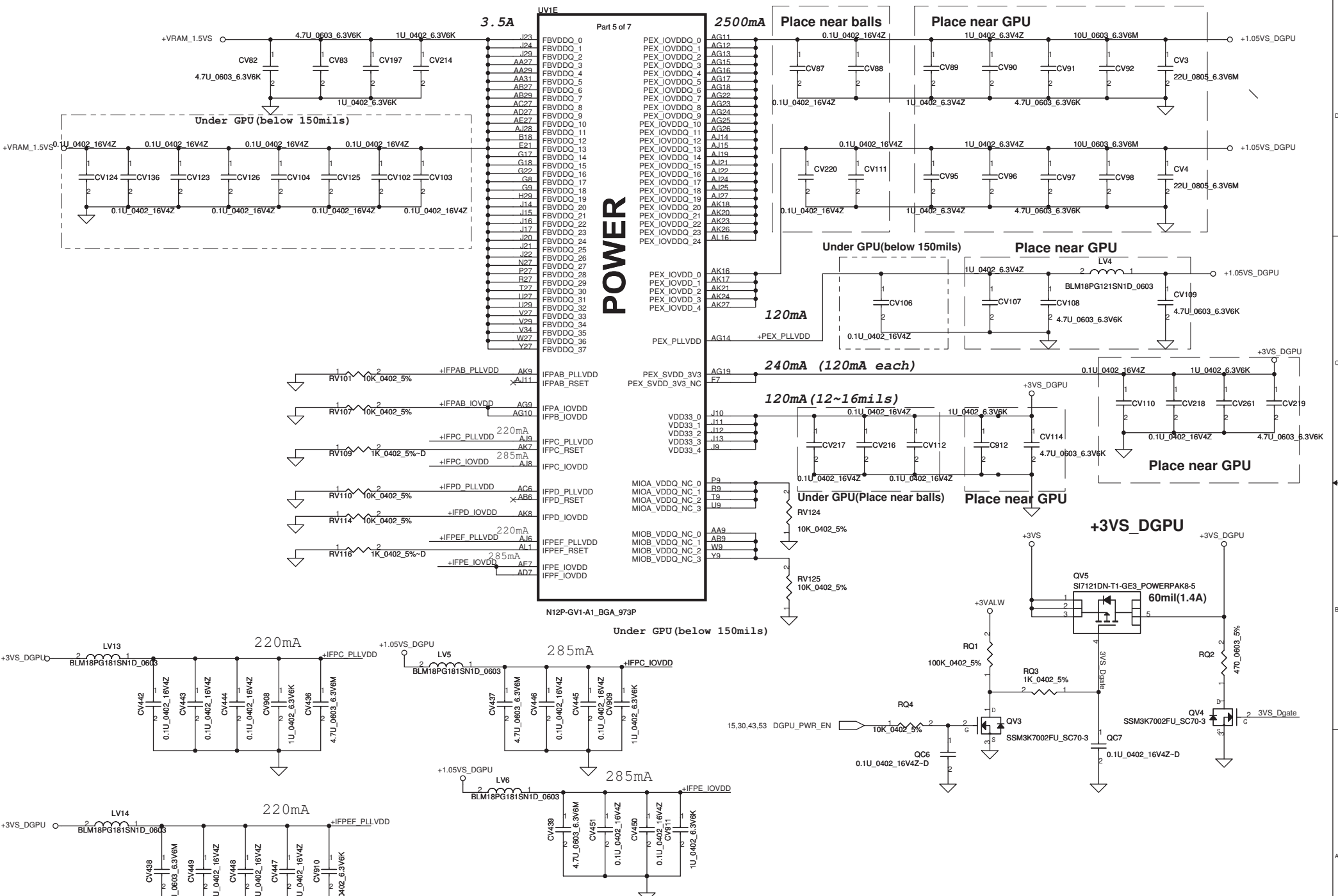


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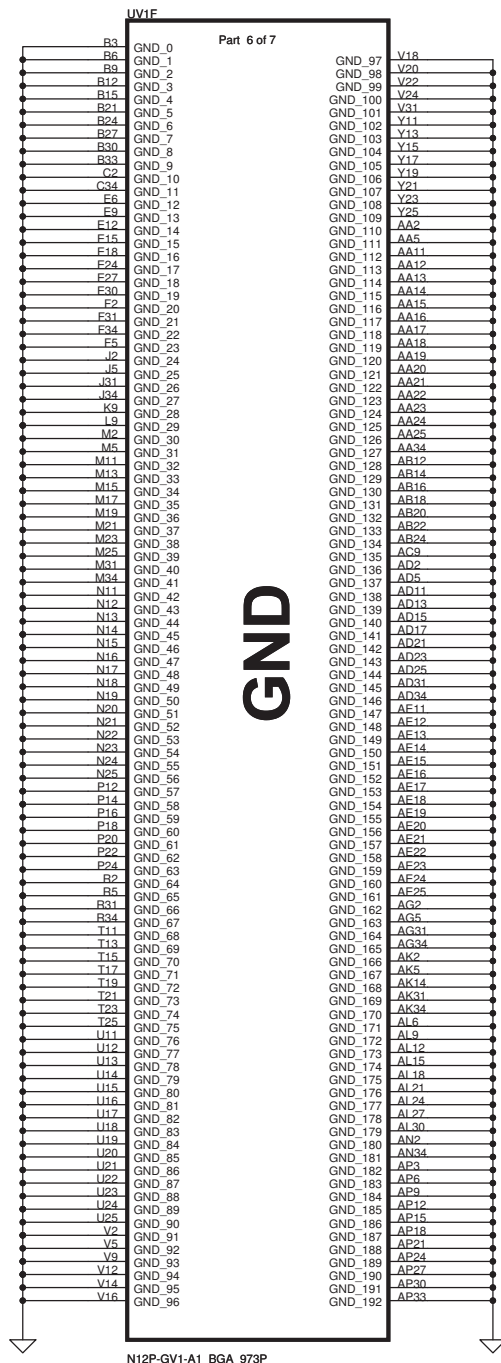
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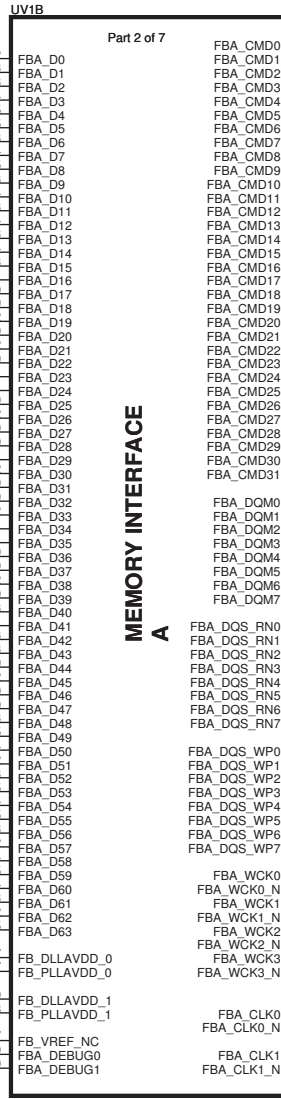


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Title VGA(5/12)-GND			
Size	Document Number	Rev	
	LA-6961P	0.4	
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Mode E - Mirror Mode Mapping

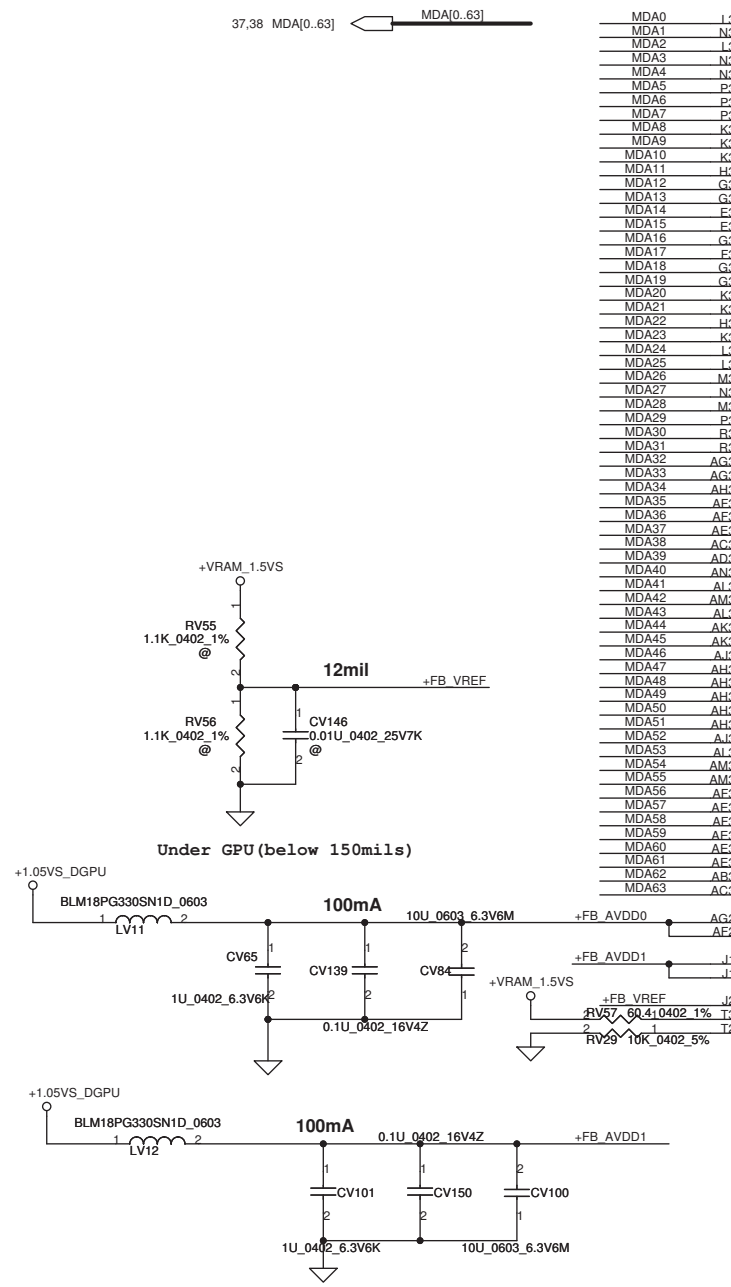
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CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



MEMORY INTERFACE A

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Compal Electronics, Inc.		
Title VGA(6/12)-MEM Interface A		
Size	Document Number LA-6961P	Rev 0.4
Date:	Monday, January 24, 2011	Sheet 35 of 54



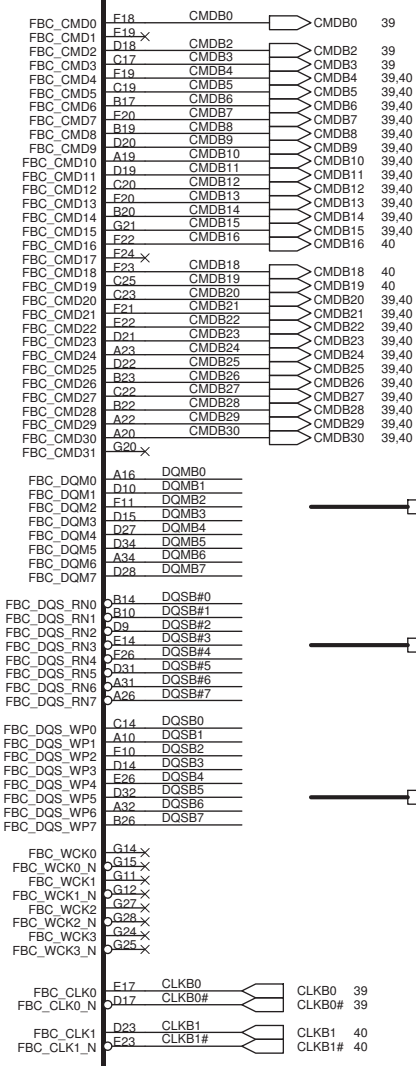
N12P-GV1-A1_BGA_973P

39.40 MDB[0..63] ← MDB[0..63]

- UVIC
- MDB0 B13 FBC_D0
 - MDB1 D13 FBC_D1
 - MDB2 A14 FBC_D2
 - MDB3 C16 FBC_D3
 - MDB4 C16 FBC_D4
 - MDB5 B16 FBC_D5
 - MDB6 A17 FBC_D6
 - MDB7 D16 FBC_D7
 - MDB8 C13 FBC_D8
 - MDB9 B11 FBC_D9
 - MDB10 A11 FBC_D10
 - MDB11 C11 FBC_D11
 - MDB12 C10 FBC_D12
 - MDB13 C8 FBC_D13
 - MDB14 B8 FBC_D14
 - MDB15 A8 FBC_D15
 - MDB16 F8 FBC_D16
 - MDB17 F8 FBC_D17
 - MDB18 F10 FBC_D18
 - MDB19 E9 FBC_D19
 - MDB20 F12 FBC_D20
 - MDB21 D8 FBC_D21
 - MDB22 D11 FBC_D22
 - MDB23 F11 FBC_D23
 - MDB24 D12 FBC_D24
 - MDB25 E13 FBC_D25
 - MDB26 F13 FBC_D26
 - MDB27 F14 FBC_D27
 - MDB28 F15 FBC_D28
 - MDB29 F16 FBC_D29
 - MDB30 F16 FBC_D30
 - MDB31 F17 FBC_D31
 - MDB32 D29 FBC_D32
 - MDB33 F27 FBC_D33
 - MDB34 F28 FBC_D34
 - MDB35 F28 FBC_D35
 - MDB36 D26 FBC_D36
 - MDB37 F25 FBC_D37
 - MDB38 D24 FBC_D38
 - MDB39 F25 FBC_D39
 - MDB40 F32 FBC_D40
 - MDB41 F32 FBC_D41
 - MDB42 D33 FBC_D42
 - MDB43 F31 FBC_D43
 - MDB44 C33 FBC_D44
 - MDB45 F29 FBC_D45
 - MDB46 D30 FBC_D46
 - MDB47 F29 FBC_D47
 - MDB48 B29 FBC_D48
 - MDB49 C31 FBC_D49
 - MDB50 C29 FBC_D50
 - MDB51 B31 FBC_D51
 - MDB52 C32 FBC_D52
 - MDB53 B32 FBC_D53
 - MDB54 B35 FBC_D54
 - MDB55 B34 FBC_D55
 - MDB56 A29 FBC_D56
 - MDB57 F28 FBC_D57
 - MDB58 A28 FBC_D58
 - MDB59 C28 FBC_D59
 - MDB60 C26 FBC_D60
 - MDB61 D25 FBC_D61
 - MDB62 B25 FBC_D62
 - MDB63 A25 FBC_D63

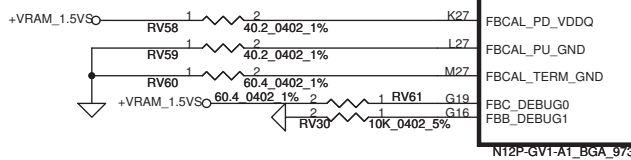
Part 3 of 7

MEMORY INTERFACE C



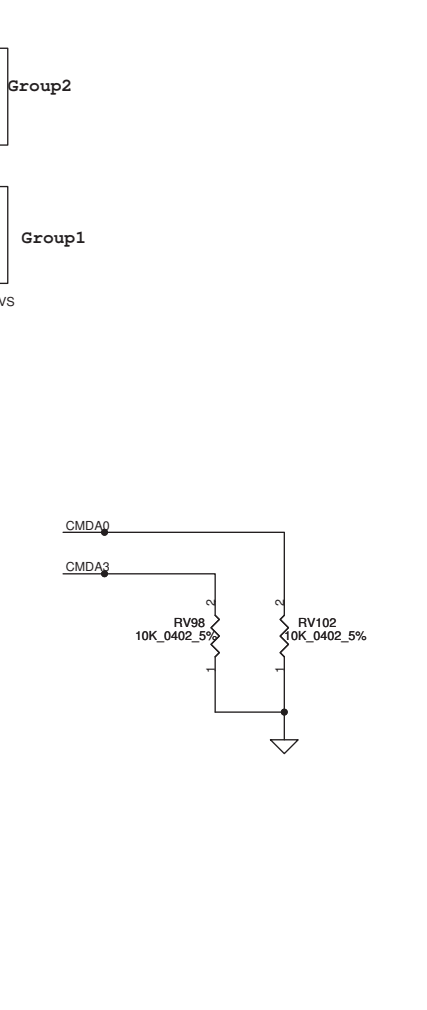
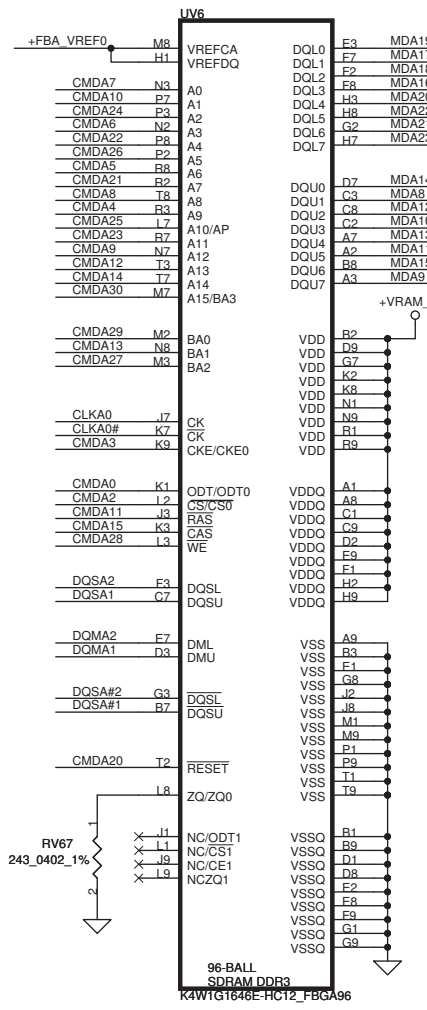
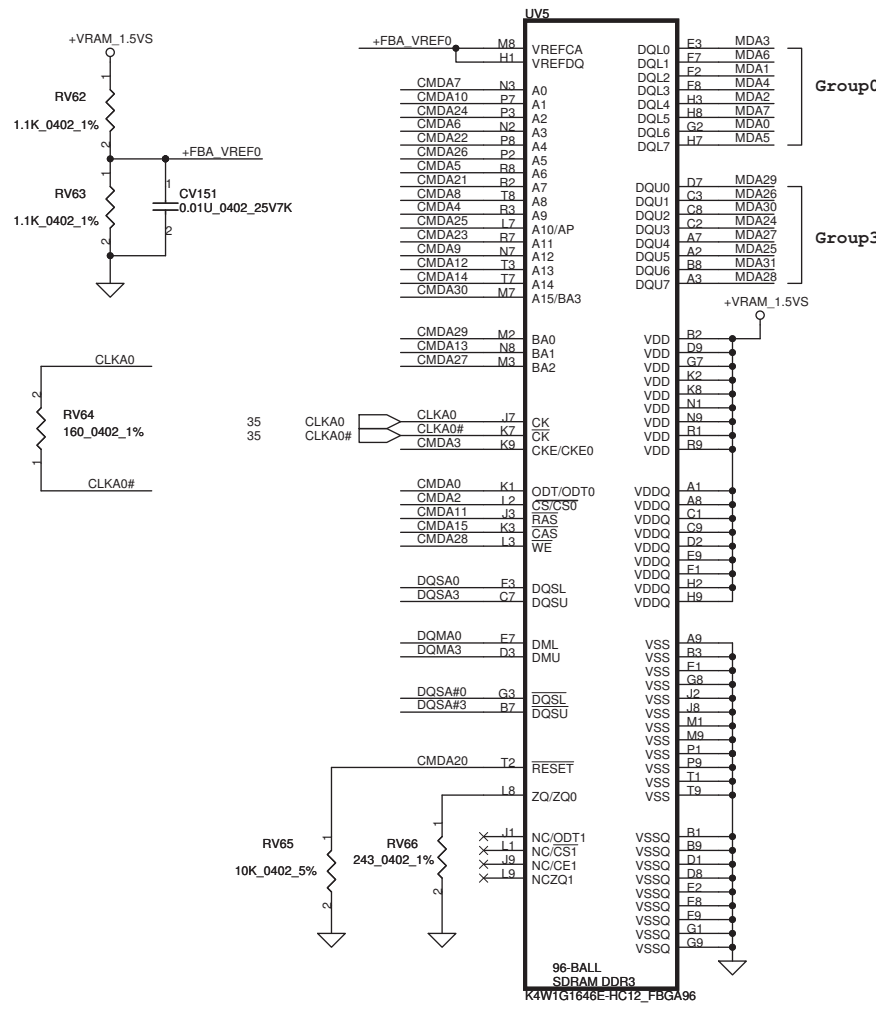
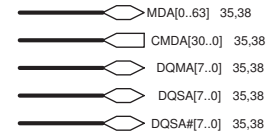
Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



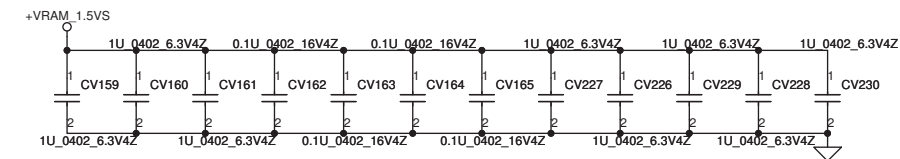
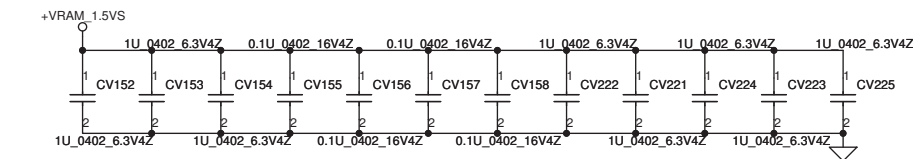
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Rev 0.4				

Memory Partition A - Lower 32 bits



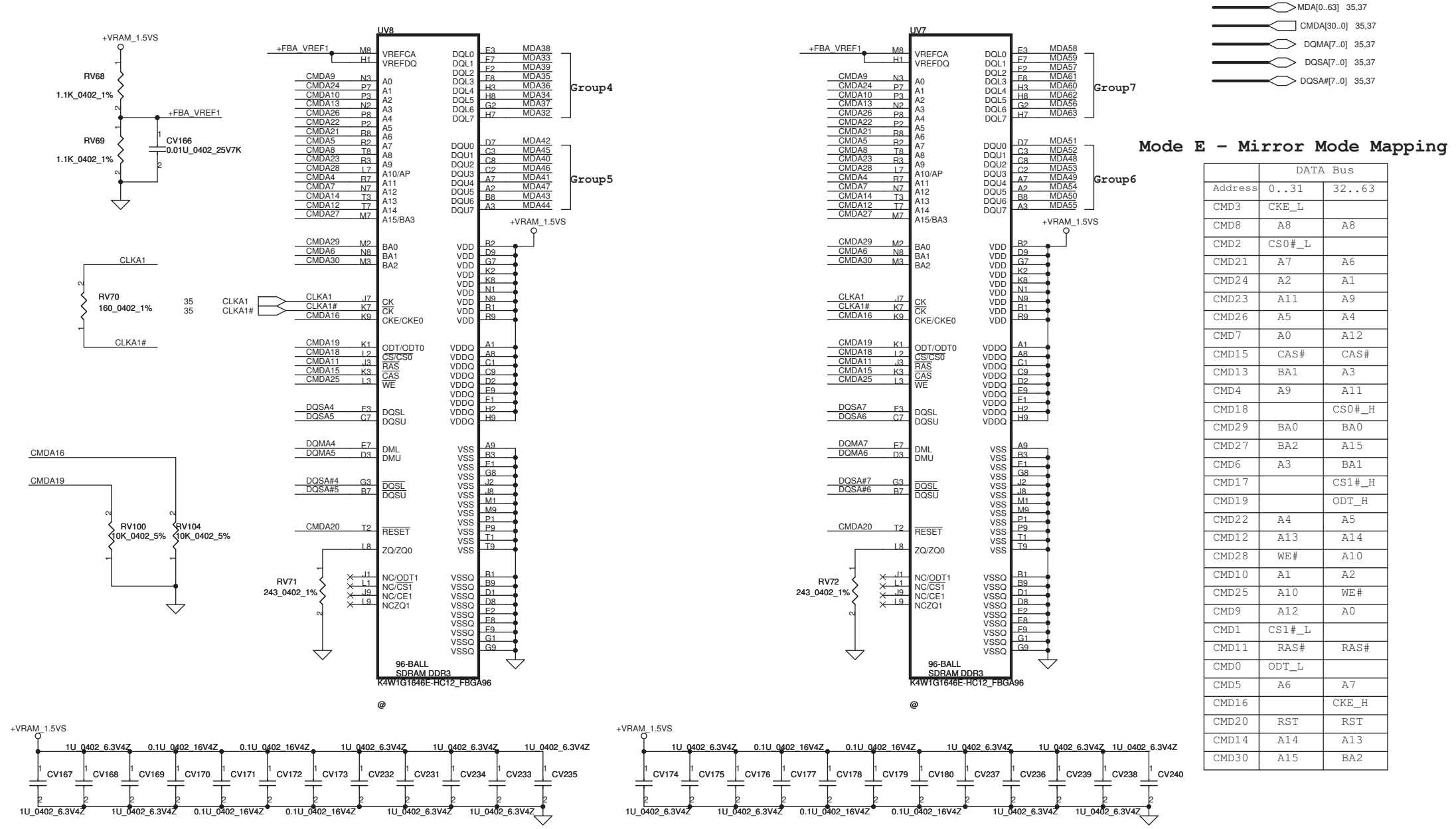
Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



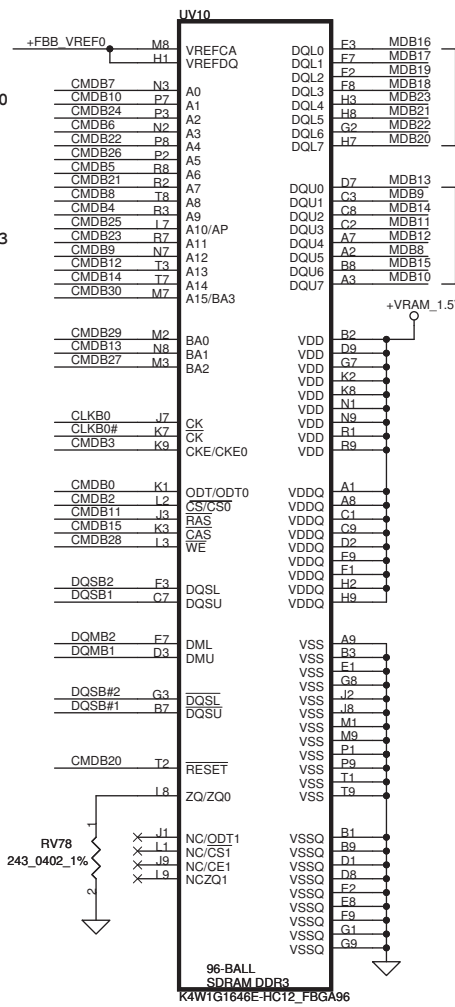
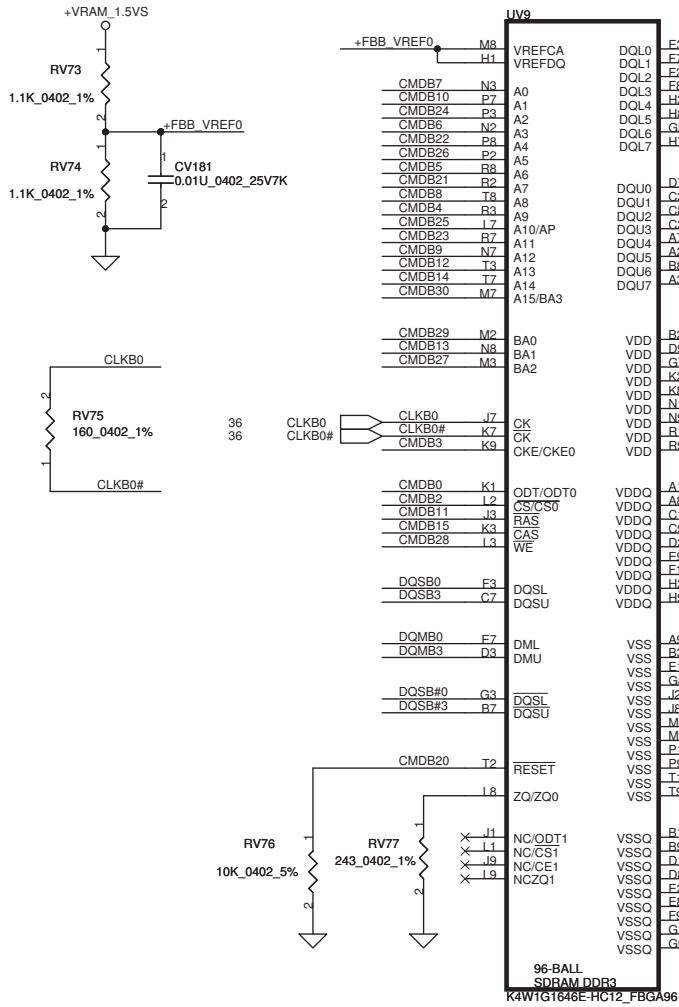
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Memory Partition A - Upper 32 bits



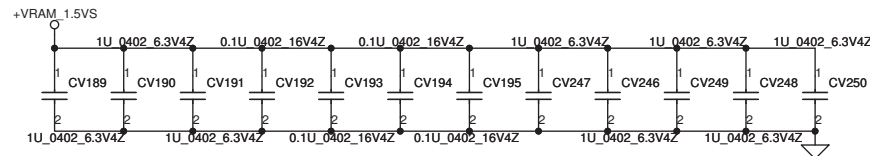
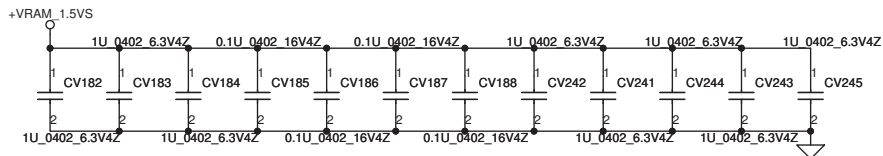
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Issued Date	2010/05/27	Deciphered Date	2011/07/06		
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Memory Partition C - Lower 32 bits



Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



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			Date:	Monday, January 24, 2011
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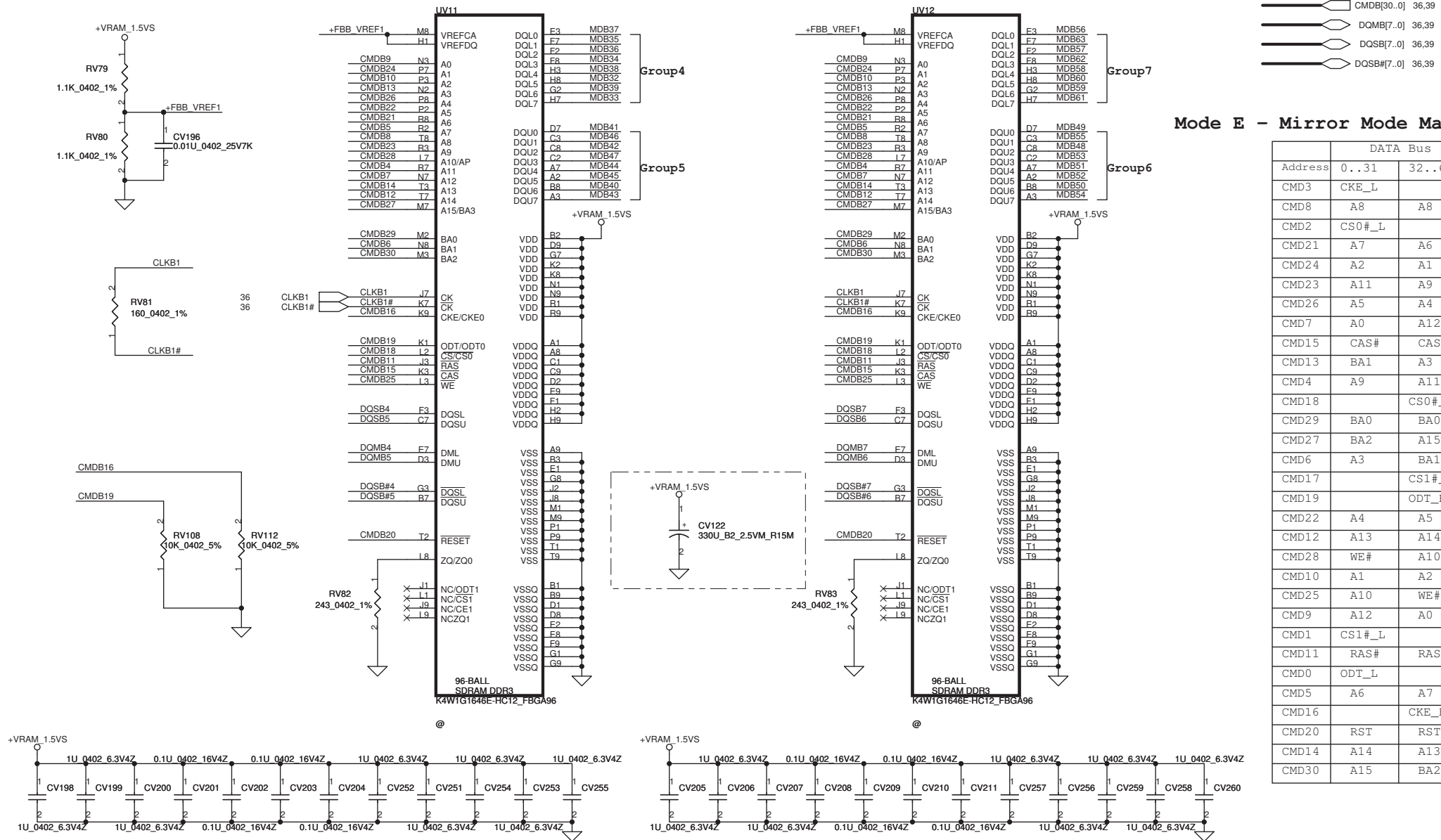
Compal Electronics, Inc.

VGA(10/12)-VRAM C Lower

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Memory Partition C - Upper 32 bits



Mode E - Mirror Mode Mapping

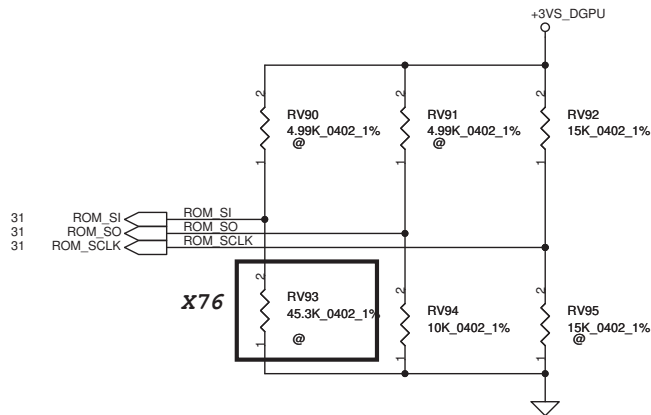
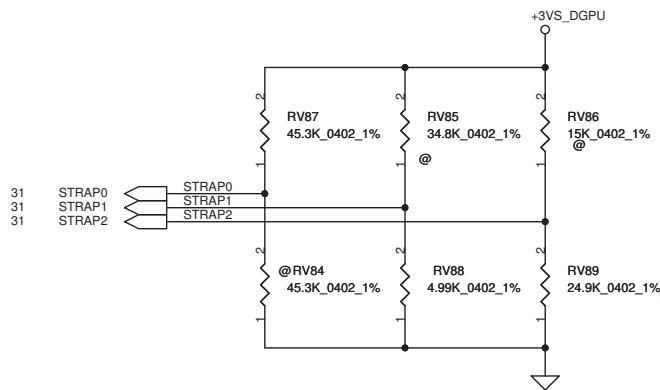
Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD4	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification		Compal Secret Data		Title VGA(11/12)-VRAM C Upper	
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Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SCLK	STRAP2
N12M-GE	0x0A7A	Pull up 15K	Pull up 15K
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GE	0x0DF5	Pull up 15K	Pull down 30K



N12P-GS-A1 :
 ROM_SO : PL-10K
 ROM_CLK : PH-15K
 ROM_SI : PL45.3K (Samsung 2GB)
 Strap 2 : PL-5K
 Strap 1 : PH-35K
 Strap 0 : PH-45K

Hynix (900MHZ) 64MX16 H5TQ1G63DFR-11C SA000041S20	1GB	0010	PD 15K (SD034150280)
Hynix (900MHZ) 128MX16 H5TQ2G63BFR-11C SA00003Y000	2GB	0110	PD 34.8k(SD034348280)
Samsung (900MHZ) 64MX16 K4W1G1646E-HC11 SA000041T00	1GB	0011	PD 20K (SD034200280)
Samsung (900MHZ) 128M16 K4W2G1646C-HC11 SA000047Q00	2GB	0111	PD 45.3K(SD034453280)

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User [3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

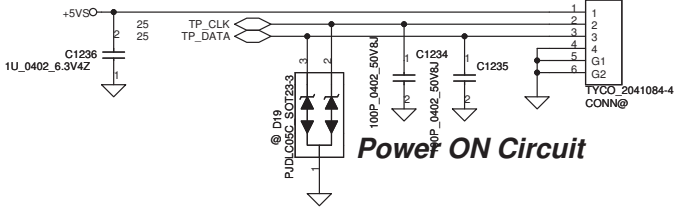
SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

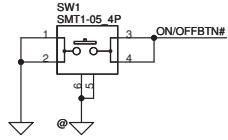
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Size Custom	Document Number	Date	Monday, January 24, 2011	Rev 0.4
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Touch pad Connector

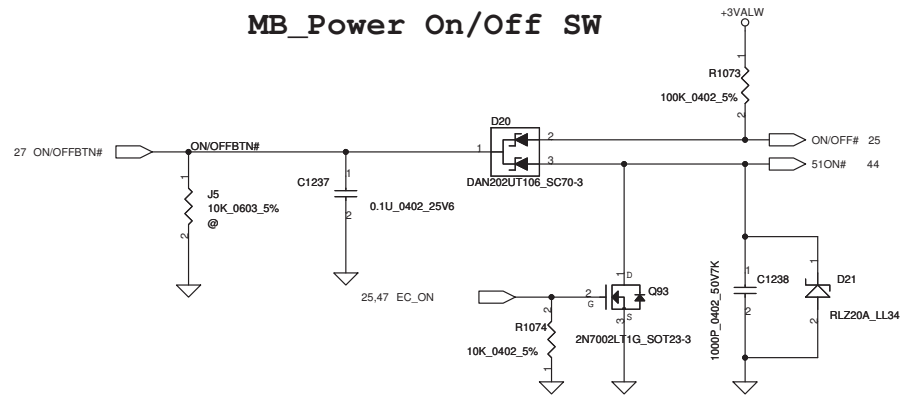


Power ON Circuit

For Debug Only

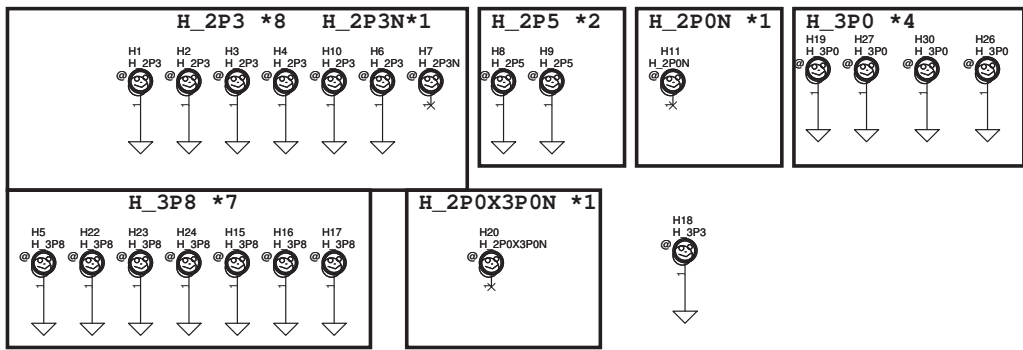
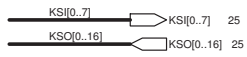
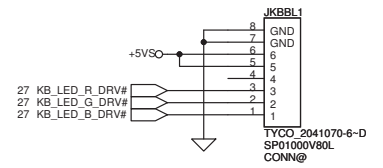


MB_Power On/Off SW



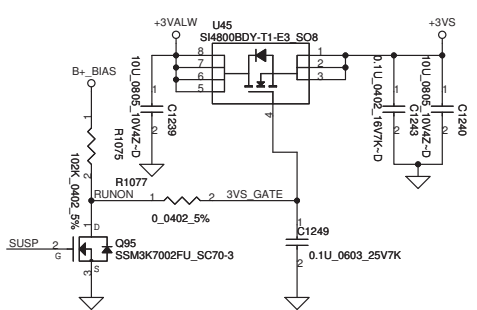
KSO8 @C736	100P_0402_25V8K	100P_0402_25V8K	C737@	KSI7
KSI3 @C738	100P_0402_25V8K	100P_0402_25V8K	C739@	KSI6
KSO9 @C740	100P_0402_25V8K	100P_0402_25V8K	C741@	KSI5
KSI2 @C742	100P_0402_25V8K	100P_0402_25V8K	C743@	KSO0
KSI1 @C744	100P_0402_25V8K	100P_0402_25V8K	C745@	KSO1
KSO10 @C746	100P_0402_25V8K	100P_0402_25V8K	C747@	KSO2
KSO11 @C750	100P_0402_25V8K	100P_0402_25V8K	C751@	KSI4
KSI0 @C752	100P_0402_25V8K	100P_0402_25V8K	C753@	KSO3
KSO12 @C754	100P_0402_25V8K	100P_0402_25V8K	C755@	KSO4
KSO13 @C756	100P_0402_25V8K	100P_0402_25V8K	C757@	KSO5
KSO14 @C760	100P_0402_25V8K	100P_0402_25V8K	C761@	KSO6
KSO15 @C762	100P_0402_25V8K	100P_0402_25V8K	C763@	KSO7
KSO16 @C764	100P_0402_25V8K			

KSI7	1
KSI6	2
KSI4	3
KSI2	4
KSI5	5
KSI1	6
KSI3	7
KSI0	8
KSO5	9
KSO4	10
KSO7	11
KSO6	12
KSO8	13
KSO3	14
KSO1	15
KSO2	16
KSO0	17
KSO12	18
KSO13	19
KSO15	20
KSO13	21
KSO14	22
KSO9	23
KSO11	24
KSO10	25

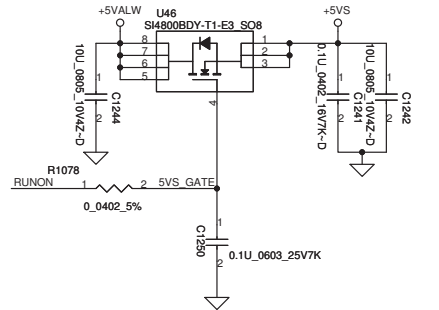


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				Date:	Monday, January 24, 2011
				Sheet	42 of 54

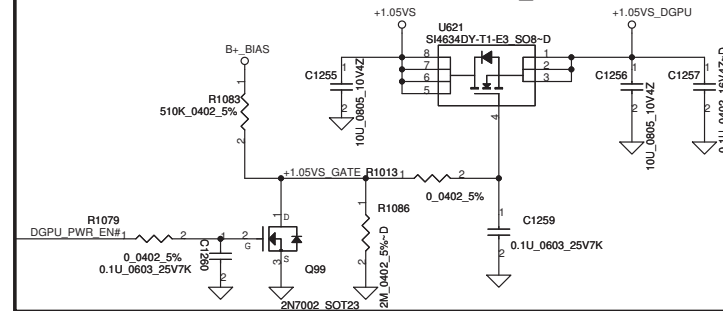
+3VALW to +3VS Transfer



+5VALW to +5VS Transfer

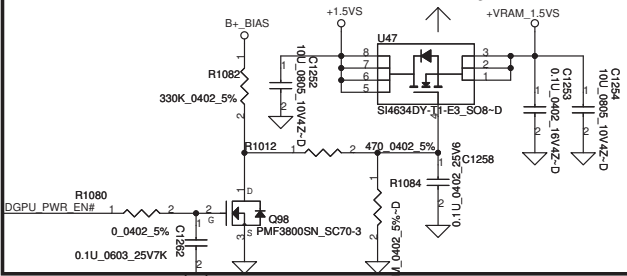


+1.05V to +1.05VS_DGPU Transfer

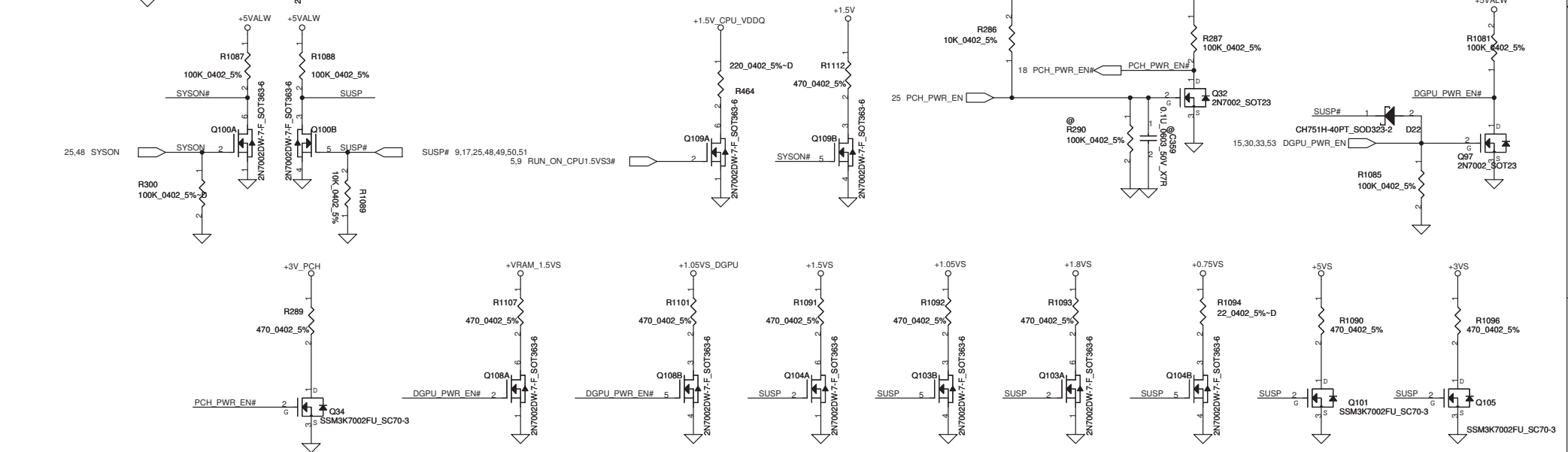
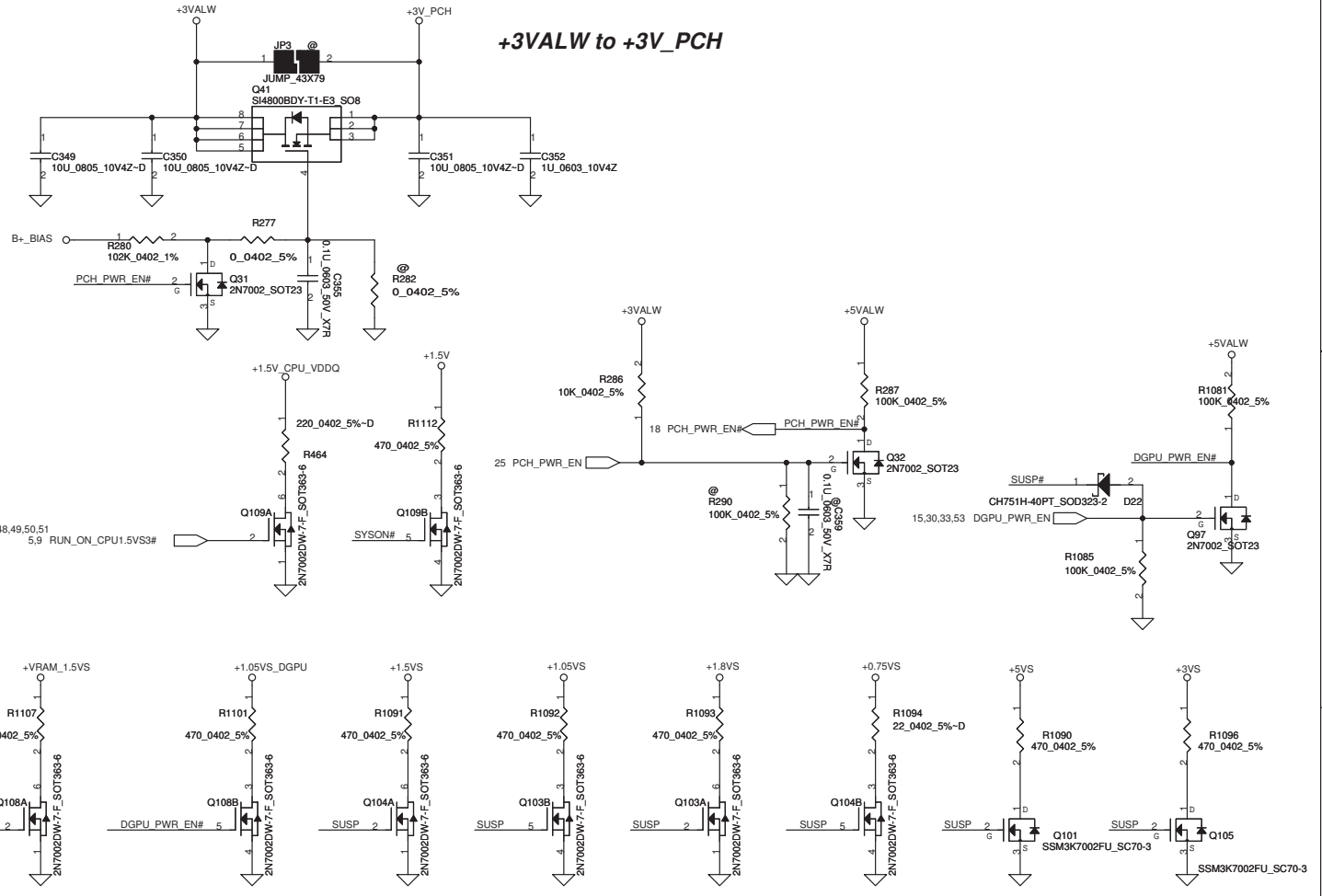


+1.5VS to +1.5VSDGPU Transfer

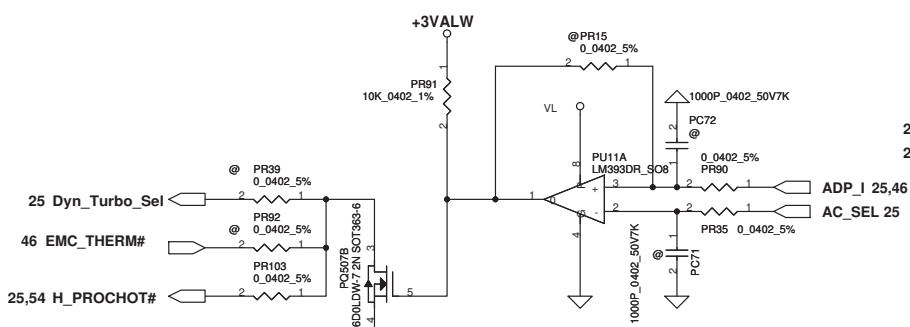
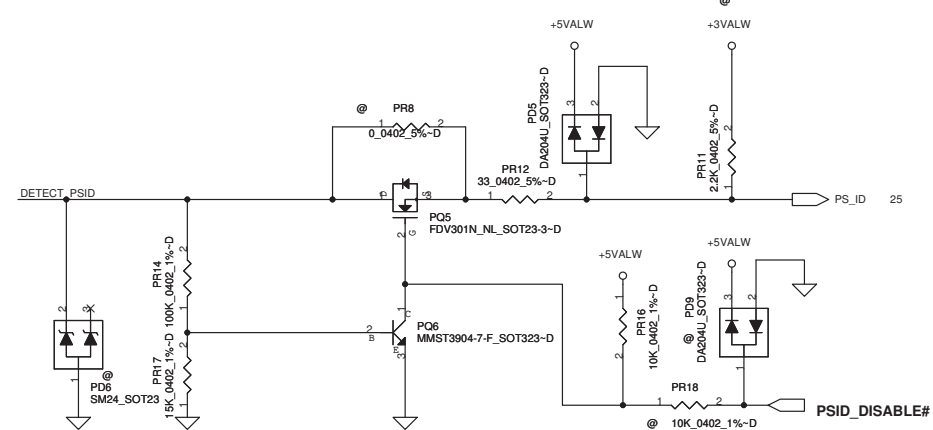
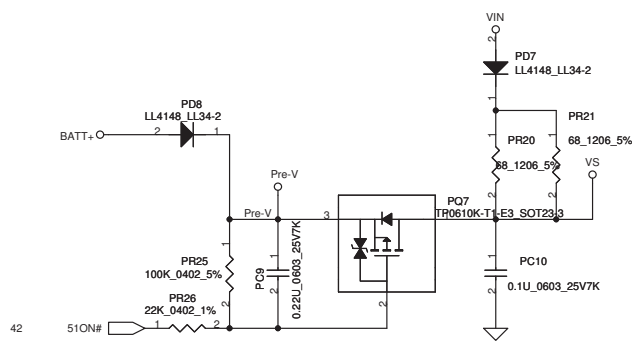
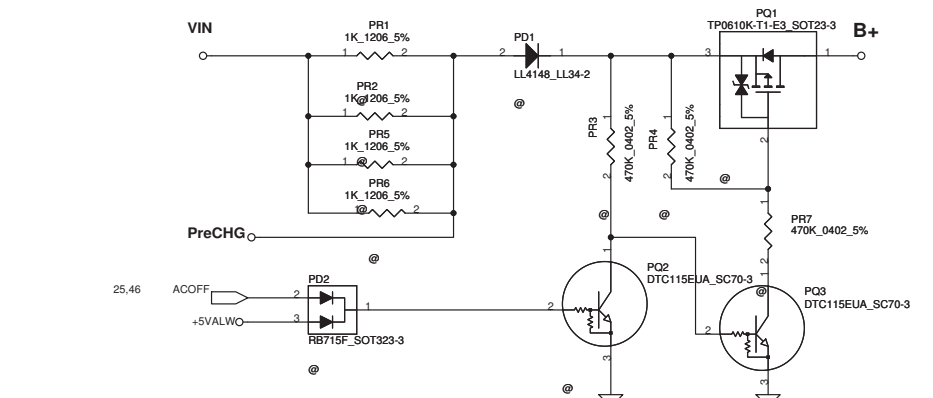
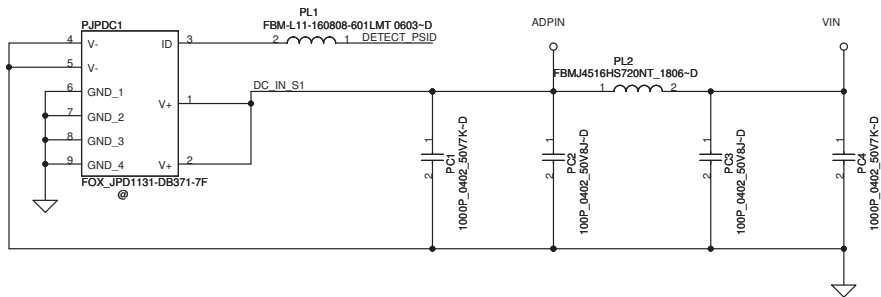
SB54392008L EOL, P/N change to SB54800038L



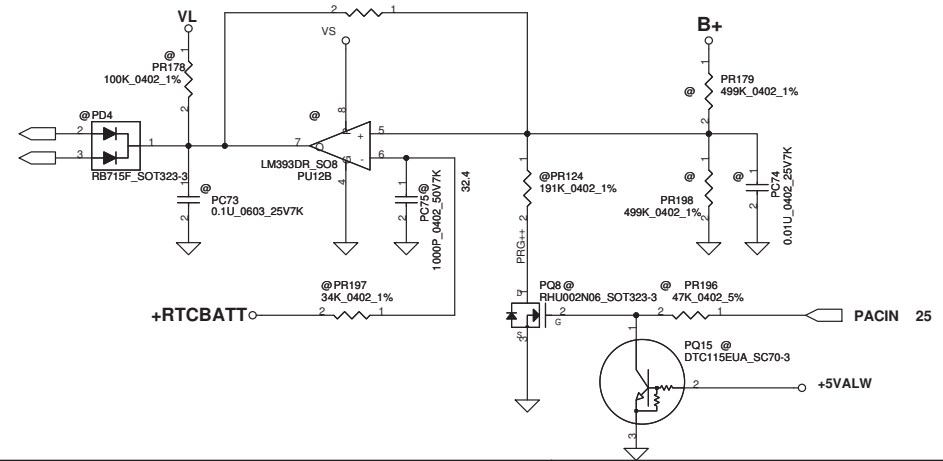
+3VALW to +3V_PCH Transfer



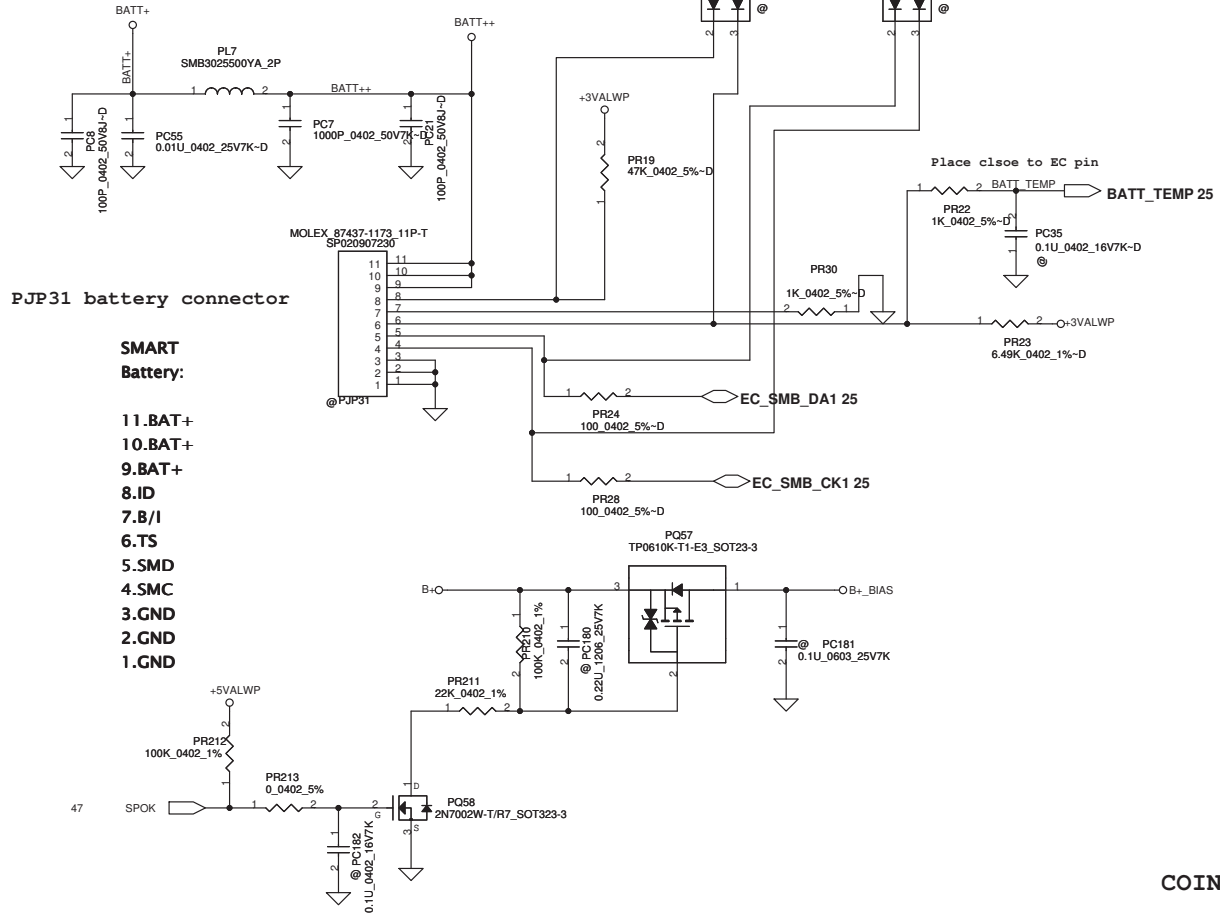
Security Classification		Compal Secret Data		Title	
Issued Date	2009/07/25	Deciphered Date	2011/07/06	DC/DC INTERFACE	
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25,54 MAINPWN
25,54 ACON



Security Classification		Compal Secret Data		Title	
Issued Date	2009/12/01	Deciphered Date	2010/05/28	PWR-DCIN / Vin Detector	
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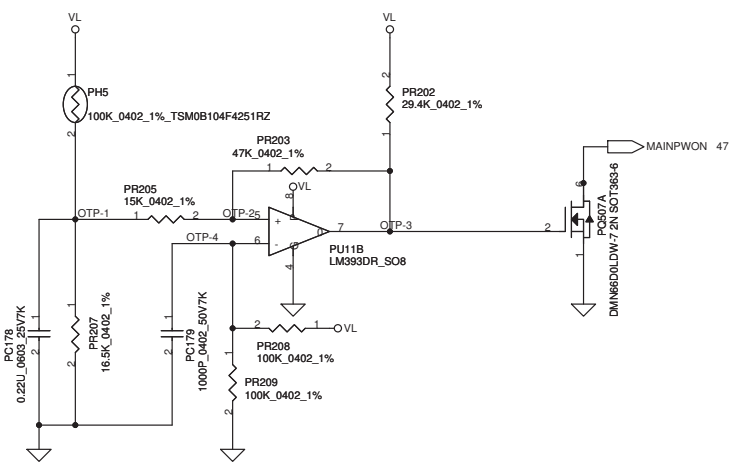
PJP31 battery connector

SMART Battery:

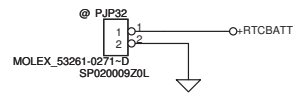
- 11.BAT+
- 10.BAT+
- 9.BAT+
- 8.ID
- 7.B/I
- 6.TS
- 5.SMD
- 4.SMC
- 3.GND
- 2.GND
- 1.GND

Battery Connect/OTP

PH3 under CPU bottom side :
 CPU thermal protection at 90 degree C
 Recovery at 50 degree C



COIN RTC Battery

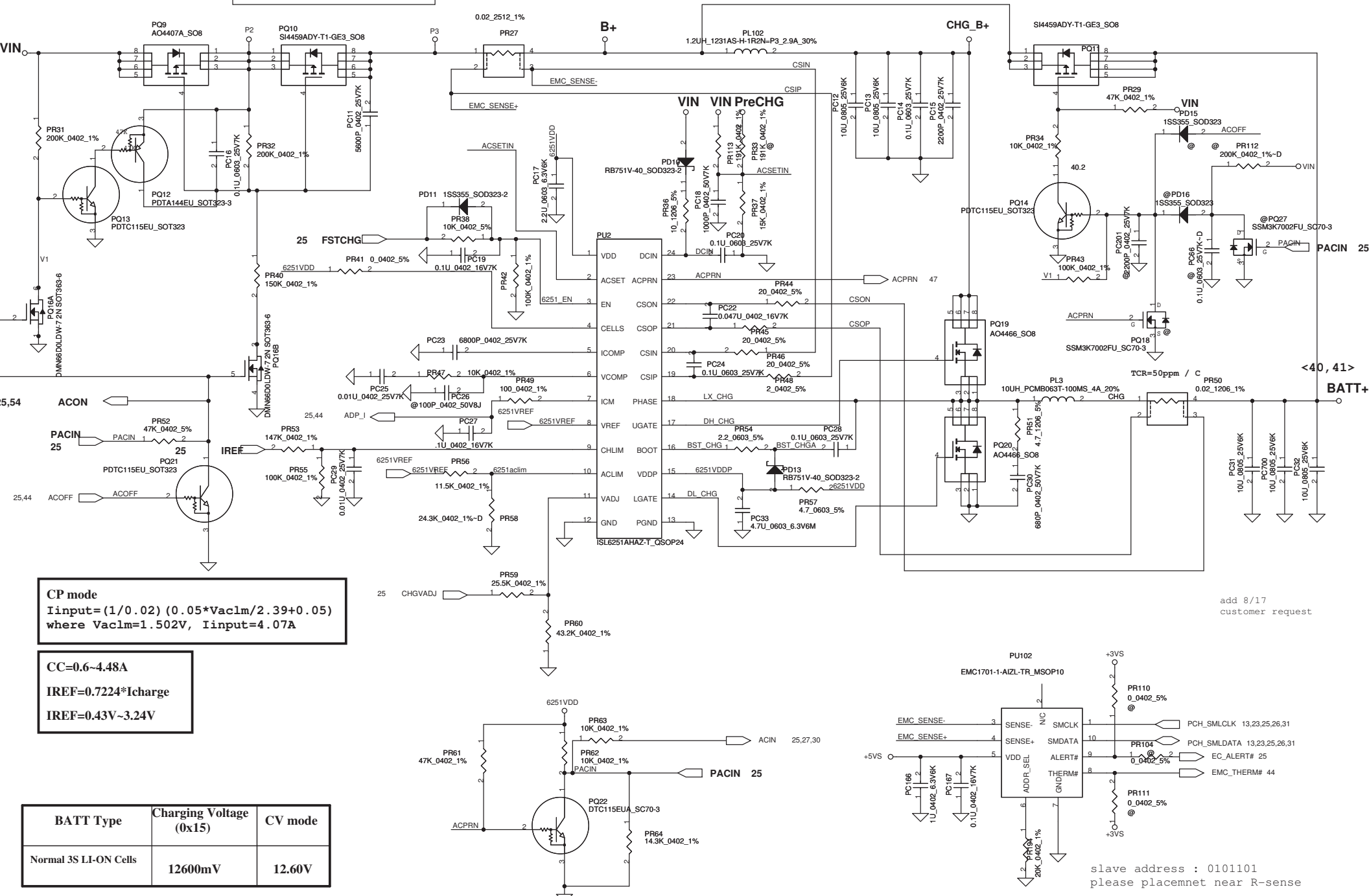


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$I_{ada} = 0 \sim 4.74A$ ($90W/19V = 4.736A$)

$ADP_I = 19.9 * I_{adapter} * R_{sense}$

$CP = 85% * I_{ada}$; $CP = 4.07A$

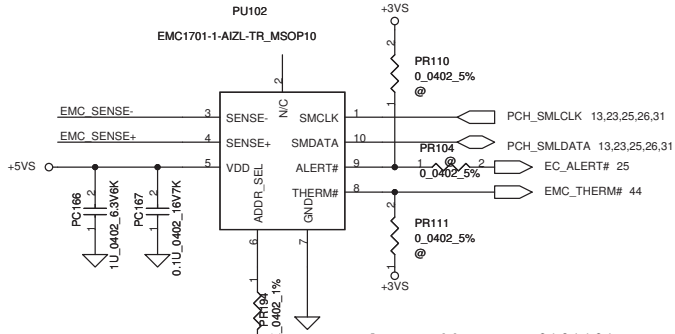


CP mode
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
 where $V_{ac1m} = 1.502V$, $I_{input} = 4.07A$

CC=0.6-4.48A
 $I_{REF} = 0.7224 * I_{charge}$
 $I_{REF} = 0.43V \sim 3.24V$

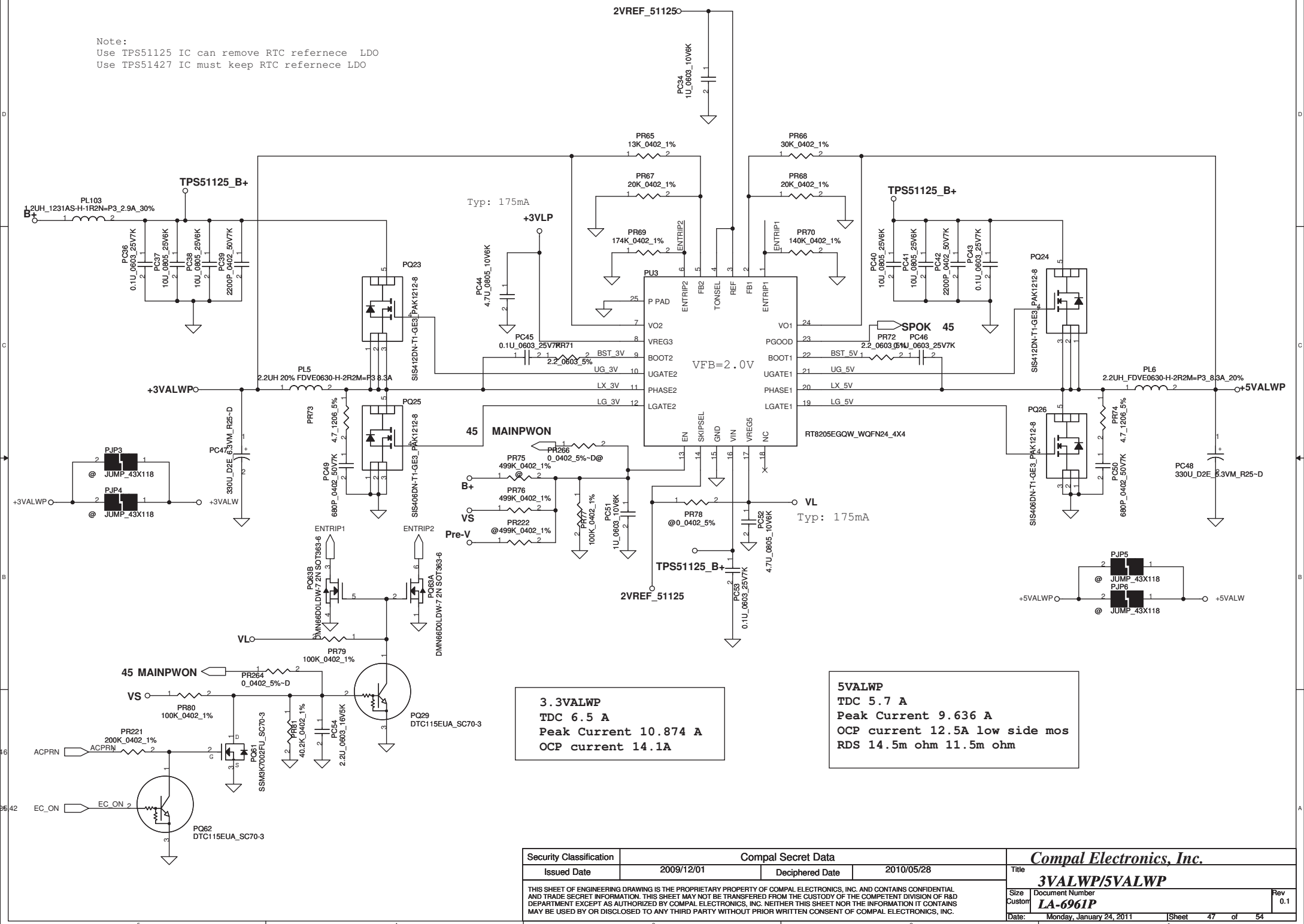
BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

add 8/17 customer request



slave address : 0101101
 please placemnet near R-sense

Note:
 Use TPS51125 IC can remove RTC refernece LDO
 Use TPS51427 IC must keep RTC refernece LDO



3.3VALWP
 TDC 6.5 A
 Peak Current 10.874 A
 OCP current 14.1A

5VALWP
 TDC 5.7 A
 Peak Current 9.636 A
 OCP current 12.5A low side mos
 RDS 14.5m ohm 11.5m ohm

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/05/28

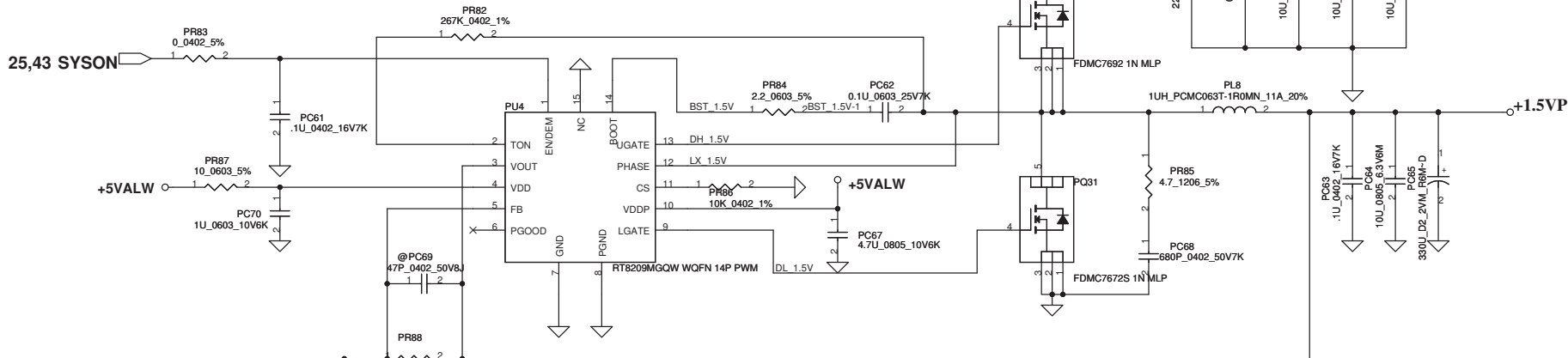
Compal Electronics, Inc.		
3VALWP/5VALWP		
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25,43 SYSON

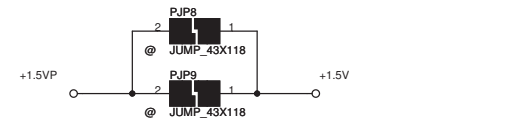
+5VALW

+1.5VP



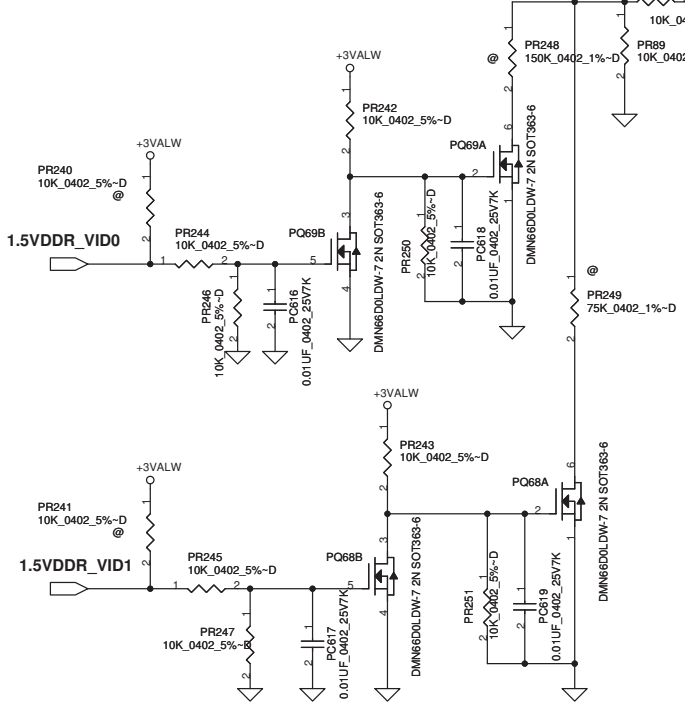
DDR GPIO Output Voltage Selection		
bit2 = 1.5DDR_VID0	bit1 = 1.5DDR_VID1	DDR Vout
0	0	1.65V
0	1	1.6V
1	0	1.55V
1	1	1.5V (Default)

1.5VP
TDC 8.9A
Peak Current 12.72 A
OCp current 16.5A
low side mos RDS 4.5ohm 3.6ohm

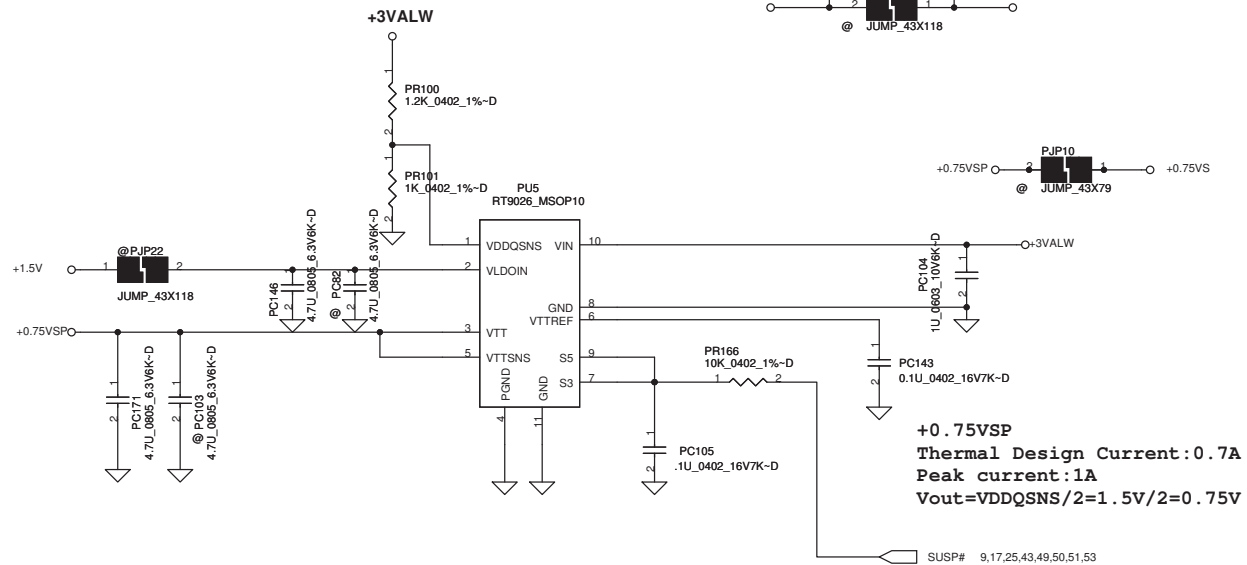


1.5VDDR_VID0

1.5VDDR_VID1

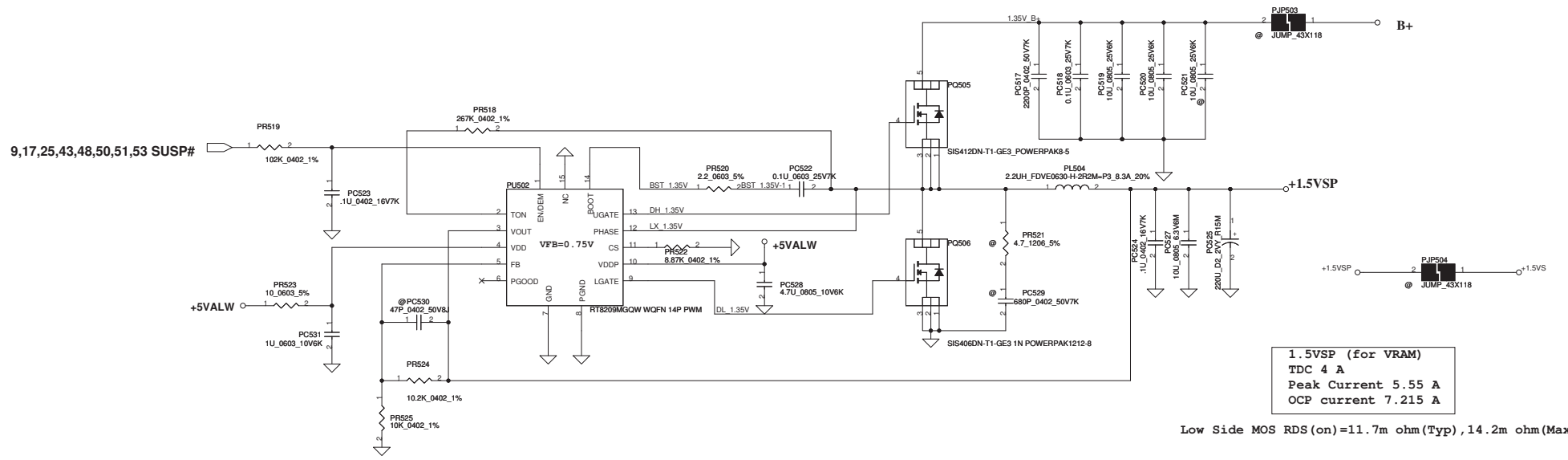


+3VALW



+0.75VSP
Thermal Design Current: 0.7A
Peak current: 1A
Vout=VDDQSNS/2=1.5V/2=0.75V

Security Classification	Compal Secret Data		Title PWR-+1.5VP/+0.75VSP
Issued Date	2009/12/01	Deciphered Date	
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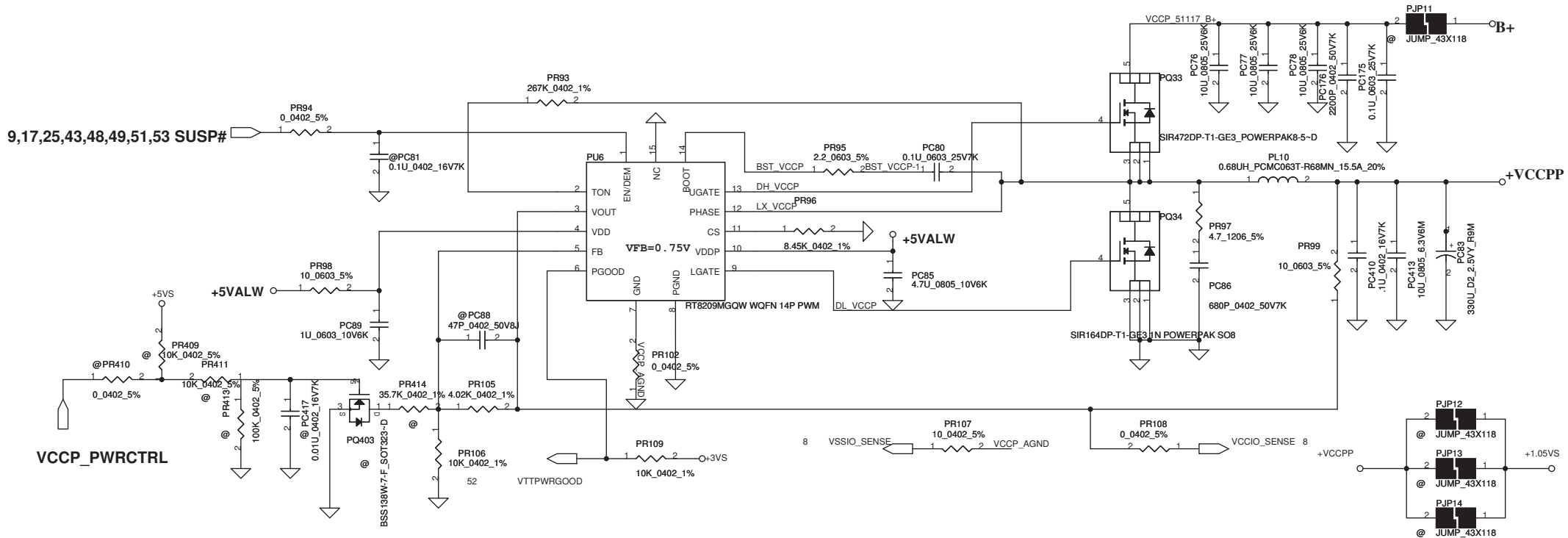


1.5VSP (for VRAM)
 TDC 4 A
 Peak Current 5.55 A
 OCP current 7.215 A

Low Side MOS RDS(on)=11.7m ohm(Typ) , 14.2m ohm(Max)

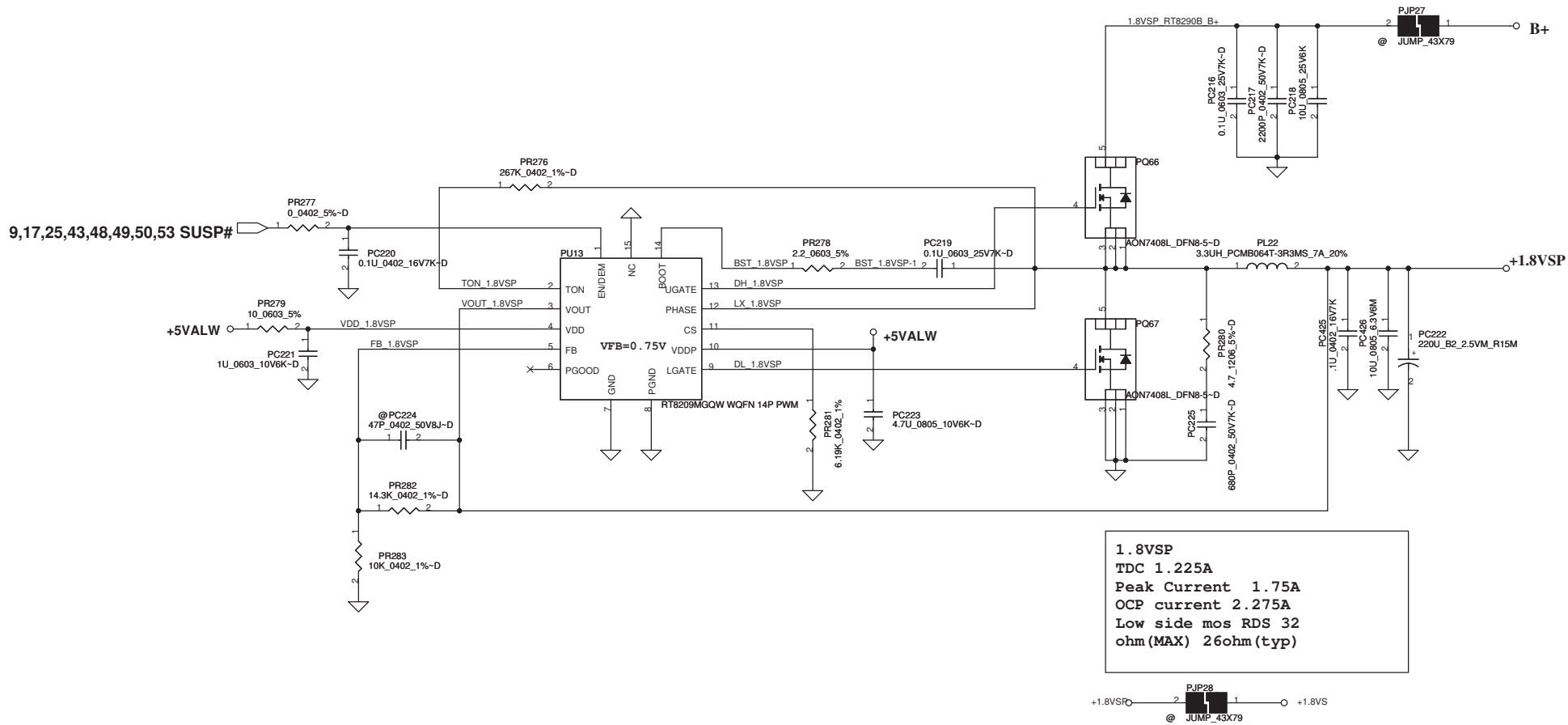
9,17,25,43,48,50,51,53 SUSP#

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Issued Date	2010/08/03	Deciphered Date	2011/08/03	Title
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VCCP
 TDC 11.5 A
 Peak Current 16.458 A
 OCP 21.4 currentA
 low side mos RDS 4.5 ohm(MAX)
 3.6ohm(MAX)

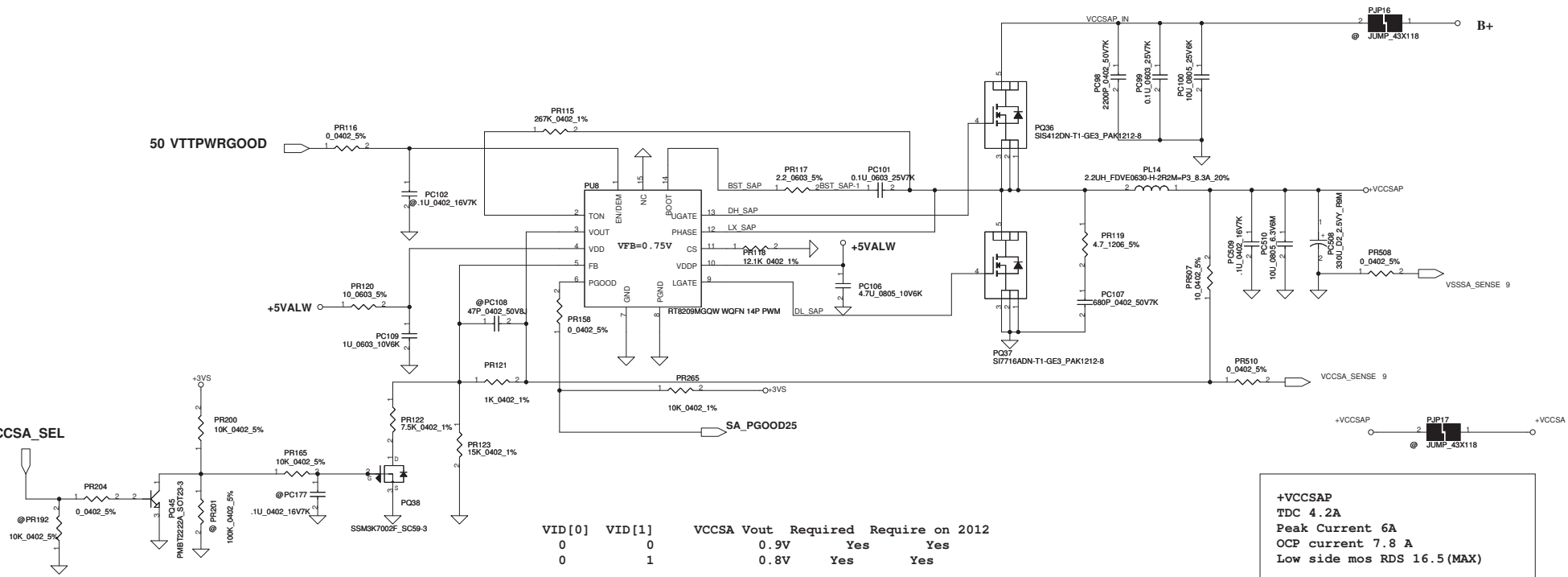
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/12/01	Deciphered Date	2010/05/28	Title	PWR+1.05VSP/+VCCPP
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Security Classification		Compal Secret Data		Title	
Issued Date	2009/12/01	Deciphered Date	2010/05/28	Size	PWR-+1.8VSP
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9 VCCSA_SEL

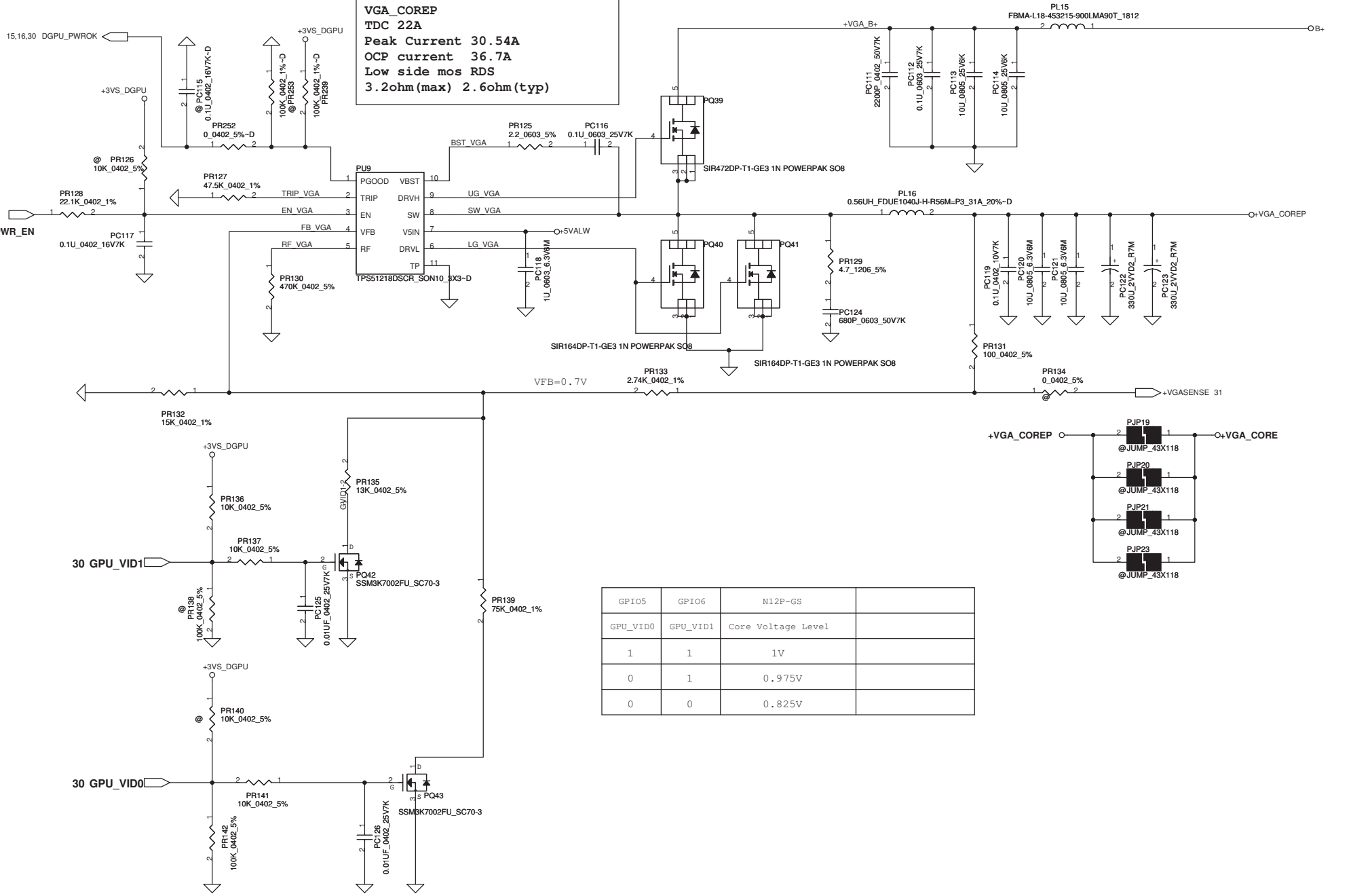
50 VTPWRGOOD



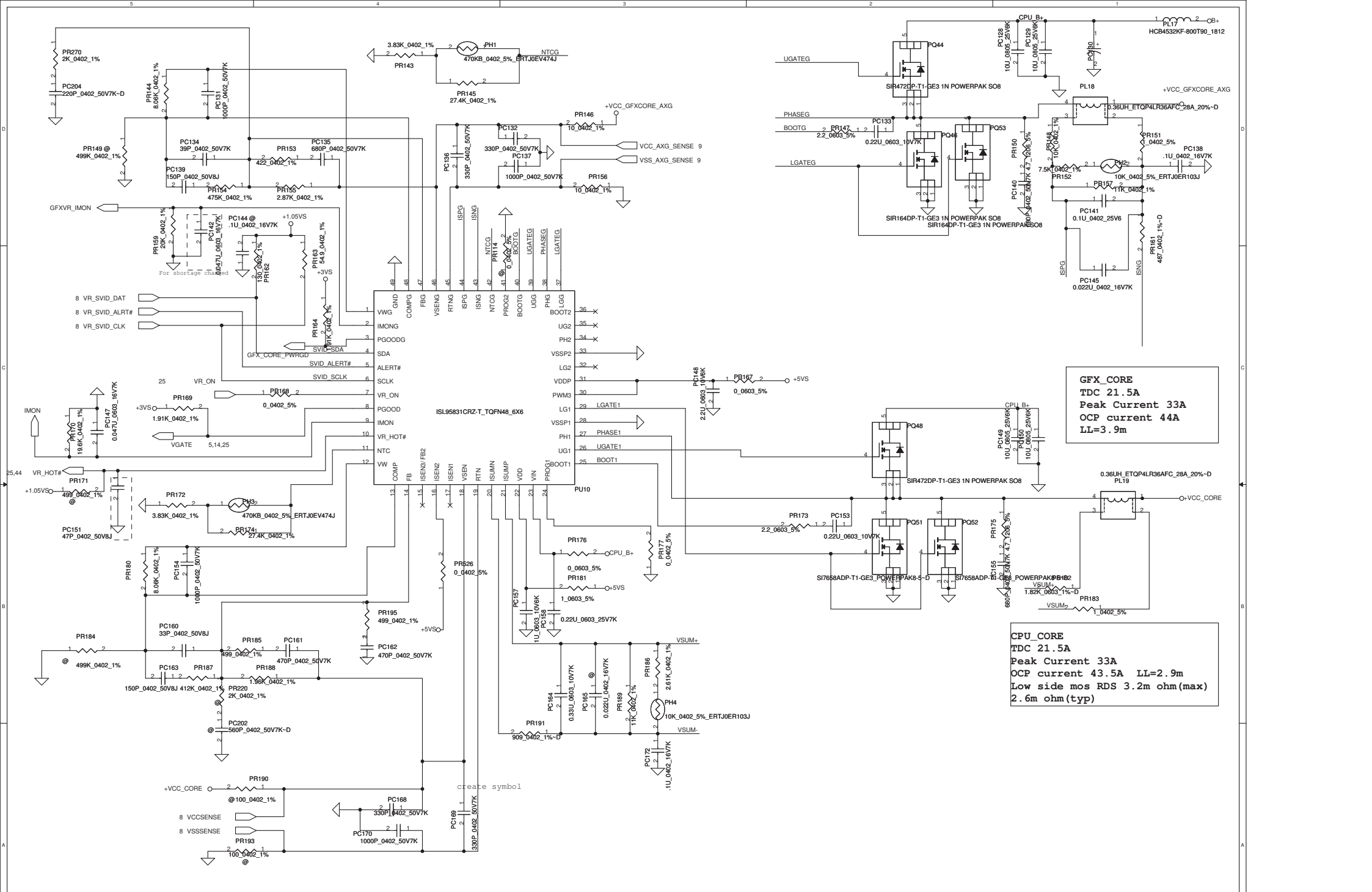
VID[0]	VID[1]	VCCSA Vout	Required	Require on 2012
0	0	0.9V	Yes	Yes
0	1	0.8V	Yes	Yes

+VCCSAP
 TDC 4.2A
 Peak Current 6A
 OCP current 7.8 A
 Low side mos RDS 16.5 (MAX)

VGA_COREP
TDC 22A
Peak Current 30.54A
OCp current 36.7A
Low side mos RDS
3.2ohm(max) 2.6ohm(typ)



GPIO5	GPIO6	N12P-GS	
GPU_VID0	GPU_VID1	Core Voltage Level	
1	1	1V	
0	1	0.975V	
0	0	0.825V	



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Issued Date	2010/01/25	Deciphered Date	2010/05/28	Title
				PWR +CPU CORE+VGFX CORE
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				Document Number LA-6761P
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Item	Reason for change	PG#	Modify List	Date	Phase
1	SYSON signal Pull low	43	Add R300	2010/10/15	PT
2	Q21 Reverse	25	Change Q21 DS pin	2010/10/15	PT
3	Fan voltage need to stable	26	Add C1923	2010/10/15	PT
4	Timing change	5	Add RC127,RC128,and Change BOM RC6 resrve	2010/10/15	PT
5	Leakge +3vs	13	Change BOM RH95 to resrve	2010/10/15	PT
6	EA crystal fail	25	Change BOM of C287,C288	2010/10/15	PT
7	EA crystal fail	13	Change BOM of CH23,CH24	2010/10/15	PT
8	EA crystal fail	21	Change BOM of C118,C119	2010/10/15	PT
9	High pot	21	Change CL39 to SB120102R1L	2010/10/15	PT
10	DFX request	42	Change JKB1 symbol	2010/10/15	PT
11	ME request	23	Change JBT1 symbol	2010/10/15	PT
12	PCH change version	12	Change BOM UH1 SA00004IV0L	2010/10/15	PT
13	Control LAN LED limiting light	21	Add series connection RL26,RL25,Change BOM RL20 to 0ohm	2010/10/17	PT
14	HuronRiver DC updated for HAD_SYNC pull-down 1M ohm	12	Add RH275 resistor connect to HDA_SYNC_R & GND	2010/10/17	PT
15	Control the LCD sequence for AUC requirement	20	Add R2005,R2006 to reserve EN_INVFWR & +LCDVDD solution	2010/10/17	PT
16	Control the LCD sequence for AUC requirement	20	Add R2013,R2014,Q305 to reserve INVPWR_B+ Discharg Circuit	2010/10/20	PT
17	USB3.0 controller change to UPD720200AF1DAPA	24	Add R1962,R1963 to UPD720200AF1DAPA solution	2010/10/20	PT
18	NV request	28	Change R463,R465 pin2 net to +3VS_DGPI	2010/10/22	PT
19	NV request	33	Change BOM of RV109,RV116 to 1kohm	2010/10/22	PT
20	The double pull low	29	Change BOM R937 to resrve	2010/10/22	PT
21	Modify screw H18 for ME request	39	Change H18 symbol	2010/10/22	PT
22	The EC request	25	Change R1095 to EC_CRY2 net,	2010/10/22	PT
23	The EC request	25	Change BOM R253 to 0ohm,R1095 to 100kohm,C287,C288, X1 resrve	2010/10/24	PT
24	The EC request	25	Change BOM R225 to 8.2kohm	2010/10/24	PT
25	The EC request	25	Change R222 to DVI	2010/10/26	PT
26	Intel request	12-19	Change BOM UH1 SA00004IV1L	2010/12/1	ST
27	Changed from +3vs to +valw to fix issue can't wake from S3 by port of USB3.0	24	Change BOM Del R1963 ,Add R1962	2010/12/1	ST
28	NV request	41	Change BOM RV88 to 4.99K ohm	2010/12/1	ST
29	Maximum derateing changed from 12V to 20V	9	Change BOM QC4 to SB00000HK0L	2010/12/1	ST
30	Maximum derateing changed from 2V to 2.5V	9	Change BOM CC176 to SGA00005H0L	2010/12/1	ST
31	EMI request	20	Add L5 to SM01000DH0L	2010/12/6	ST
32	EMI request	20	Change BOM CU63 to 100PF	2010/12/6	ST
33	EMI request	20	Change BOM C1167 to 22PF	2010/12/6	ST
34	GLAN orange LED too dark	21	Change BOM RL26 to 200ohm	2010/12/6	ST
35	The EC request	25	Add C1947 to SB071200J6L	2010/12/8	ST
36	The safety request	12	Change DH4 pin1,2,3	2010/12/8	ST
37	The USB3_SMI# signal change to GPFI04	15	Change UH1 pin C23 and H15	2010/12/8	ST
38	The DP Power Dongle	29	Add C110	2010/12/8	ST
39	The ME request	8	Change BOM C110 to C112	2010/12/9	ST
40	For ENE EC protect	20	1712 add D13, R395		
41					
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				Date:	Monday, January 24, 2011	Sheet 55 of 55