

Compal confidential

Schematics Document

Mobile Baniyas uFCBGA/uFCPGA with Intel ODEM_MCH+ICH4-M core logic

2003-07-09

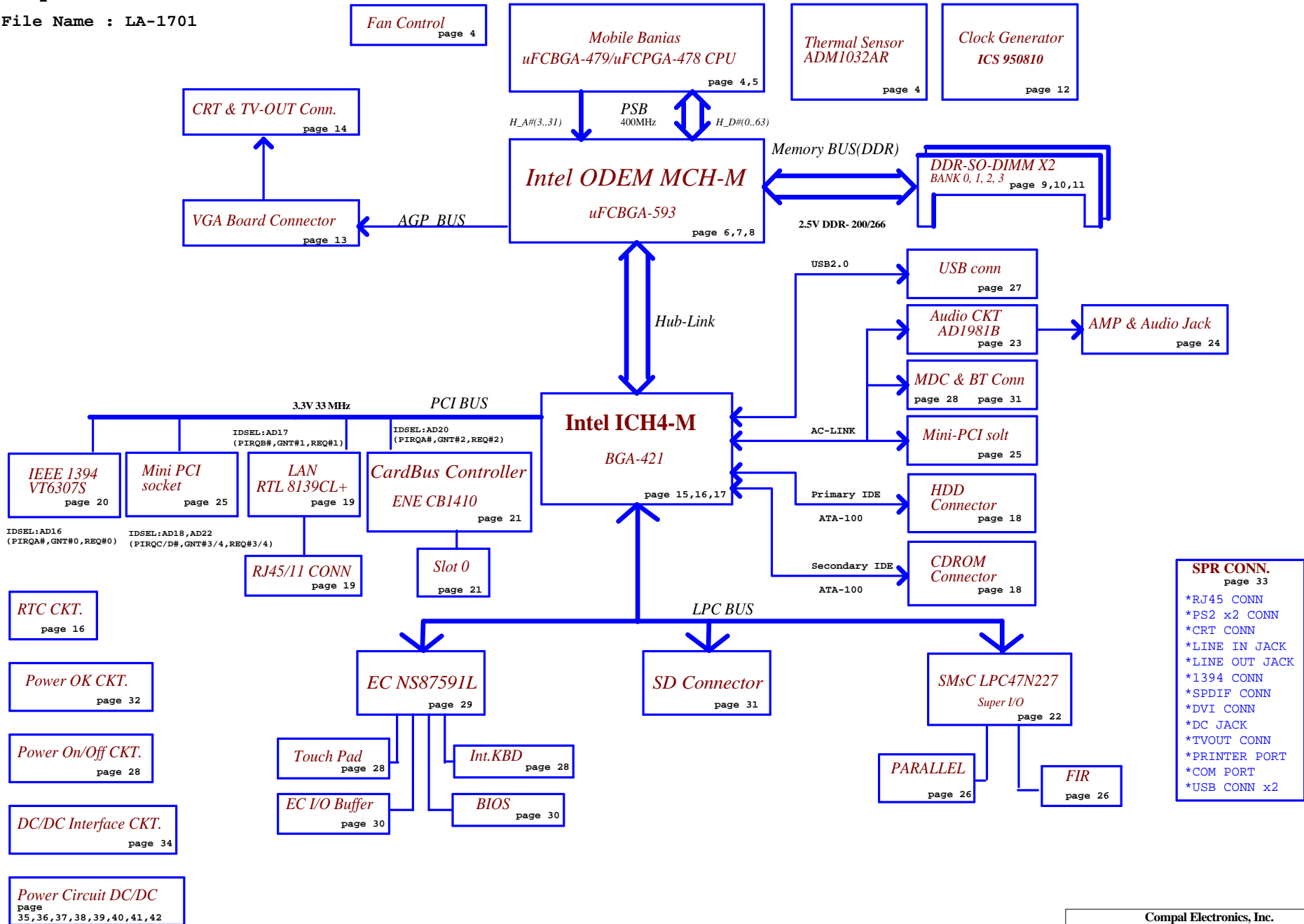
REV: 2.0

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File Name : LA-1701



- SPR CONN.**
page 33
- *RJ45 CONN
 - *PS2 x2 CONN
 - *CRT CONN
 - *LINE IN JACK
 - *LINE OUT JACK
 - *1394 CONN
 - *SPDIF CONN
 - *DVI CONN
 - *DC JACK
 - *TVOUT CONN
 - *PRINTER PORT
 - *COM PORT
 - *USB CONN x2

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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V rail for Processor I/O	ON	OFF	OFF
+1.25VS	1.25V switched power rail for DDR Vtt	ON	OFF	OFF
+1.2VS	1.2V switched power rail for MCH core power	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail for AGP interface	ON	OFF	OFF
+1.8VS	1.8V switched power rail for CPU PLL & Hub-Link	ON	OFF	OFF
+2.5V	2.5V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12V	12V power rail	ON	ON	OFF
+12VS	12Vswitched power rail on power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Symbol note:

- ↓ :means digital ground.
- ↓ :means analog ground.
- @ :means reserved.

Internal PCI Devices

DEVICE	PCI Device ID
HUB	D30
USB	D29
AC97 MODEM	D31
AC97	D31
ATA 100	D31
ETHERNET	D8 (AD24)
LPC I/F	D31
SMBUS	D31

External PCI Devices

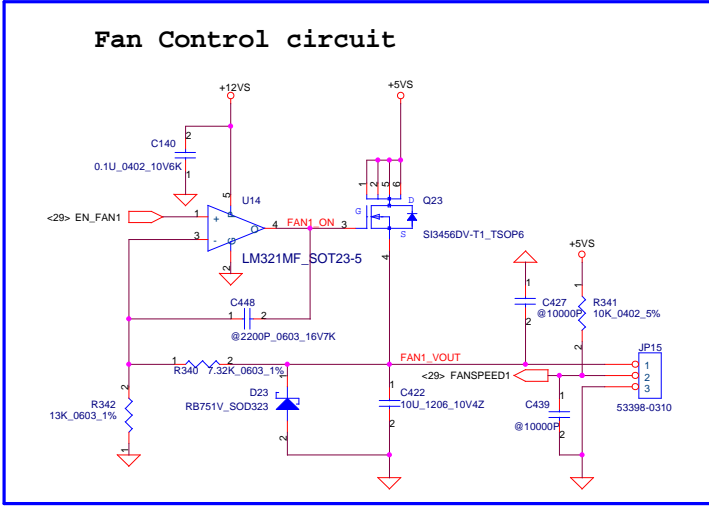
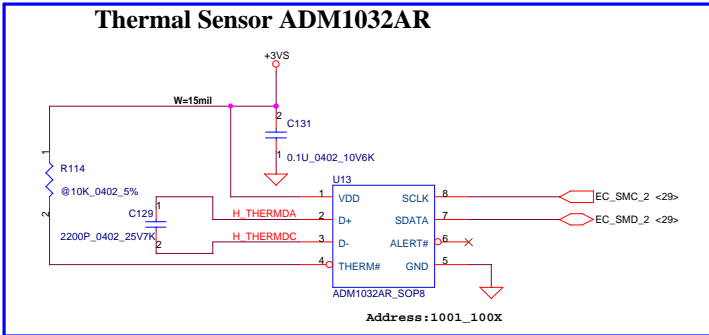
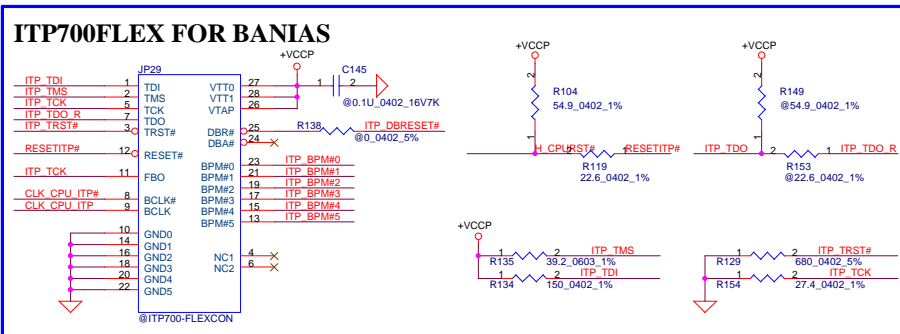
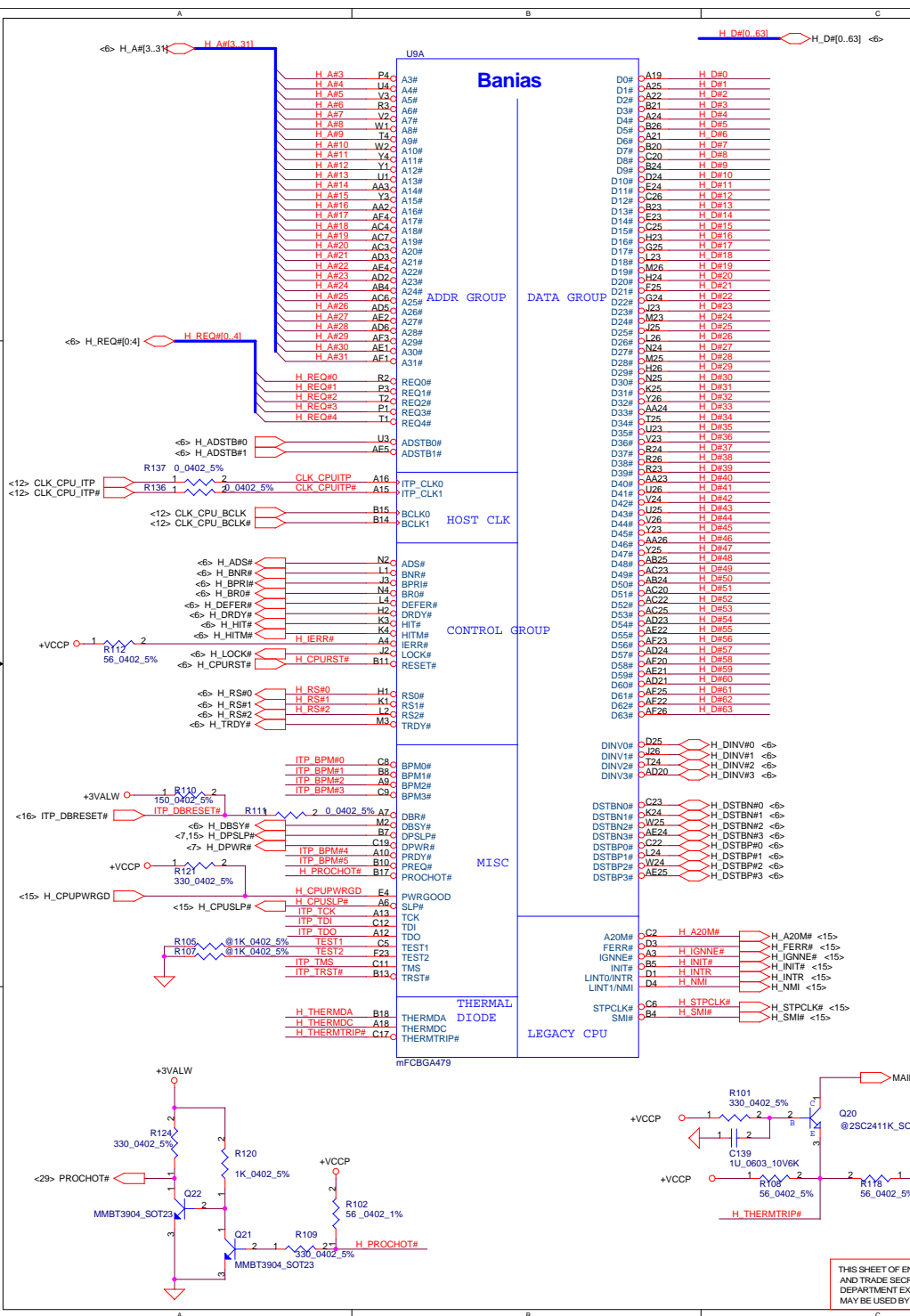
DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
1394	D0	AD16	0	A
LAN	D1	AD17	1	B
CARD BUS	D4	AD20	2	C
Wireless LAN	D2	AD18	3	D
Mini-PCI	D6	AD22	4	D
AGP BUS	N/A	AGP_DEVSEL#	N/A	A

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 X
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 X

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Notes List			
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Resistor placed within 0.5" of CPU pin. Trace should be at least 25 miles away from any other toggling signal.

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 miles away from any other toggling signal.

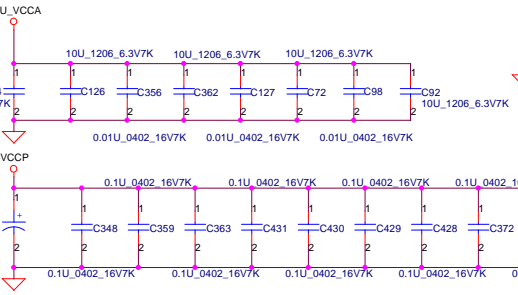
Banias

Banias

POWER, GROUND, RESERVED SIGNALS AND NC

POWER, GROUND

Vcc-core Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	4X220uF	12m ohm/4	3.5nH/4
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35



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Title: INTEL CPU BANIAS (2 of 2)

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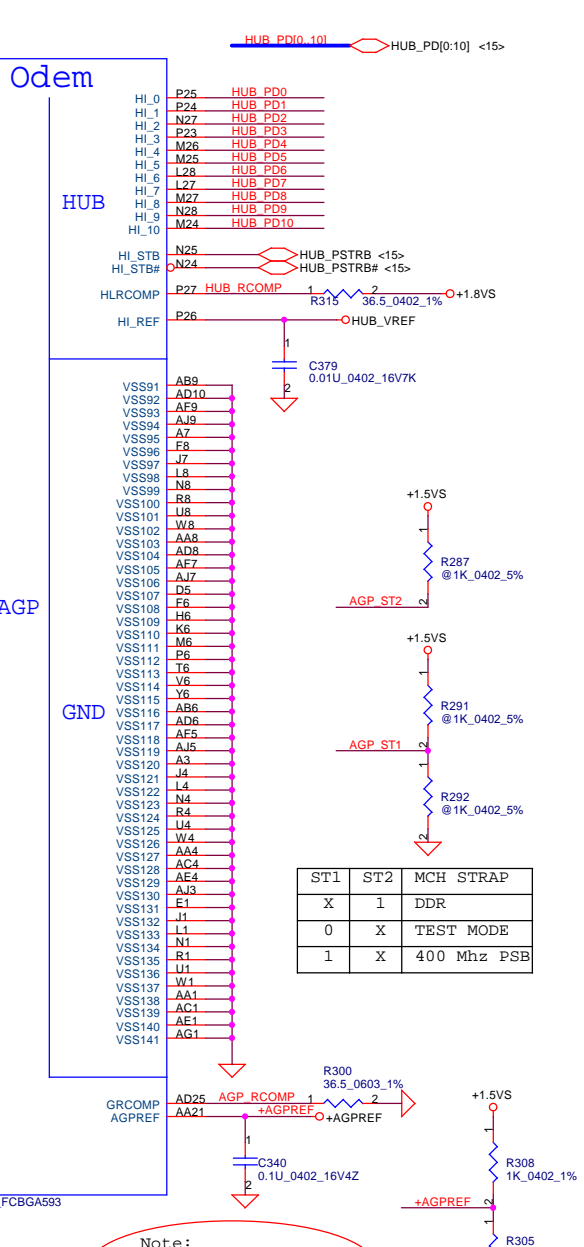
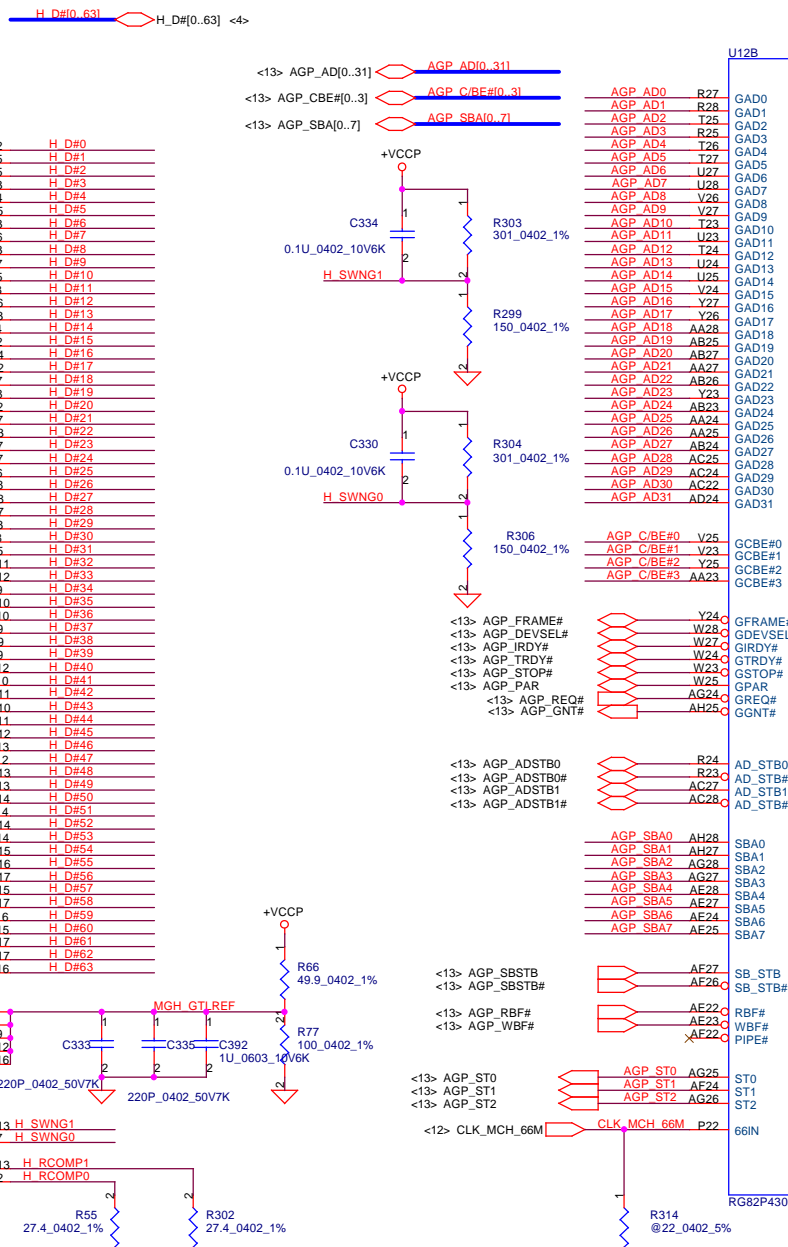
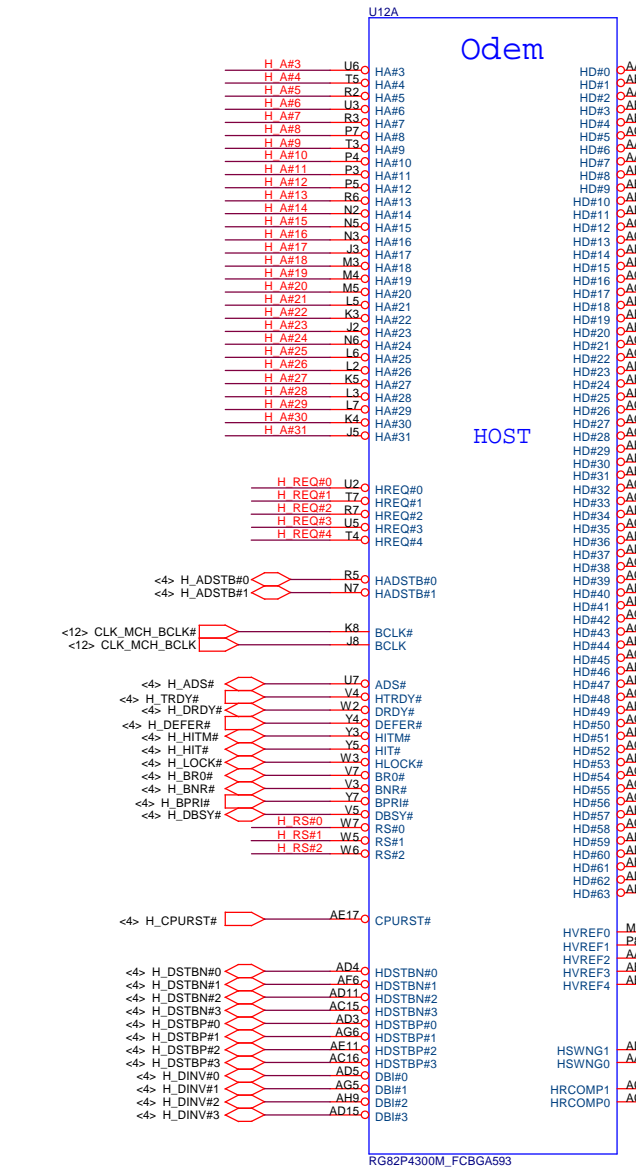
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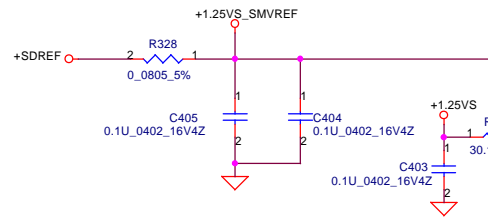
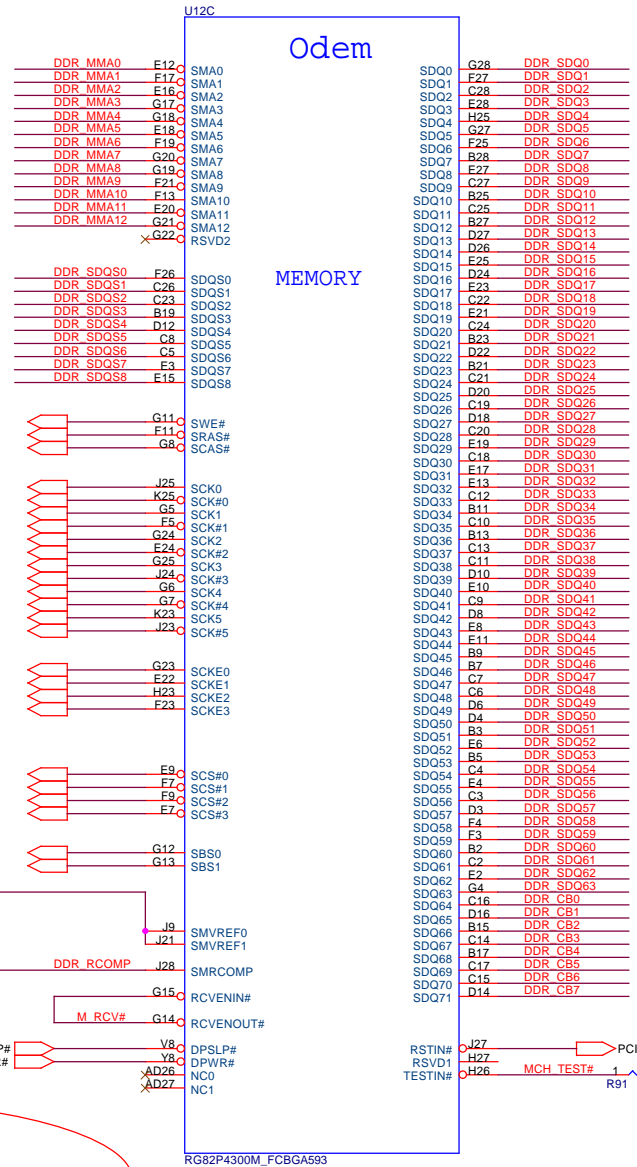
<4> H_RS#[0..2] H_RS#[0..2]
 <4> H_A#[3..31] H_A#[3..31]
 <4> H_REQ#[0..4] H_REQ#[0..4]



ST1	ST2	MCH STRAP
X	1	DDR
0	X	TEST MODE
1	X	400 Mhz PSB

Note: Placement R308,R305 close to MCH

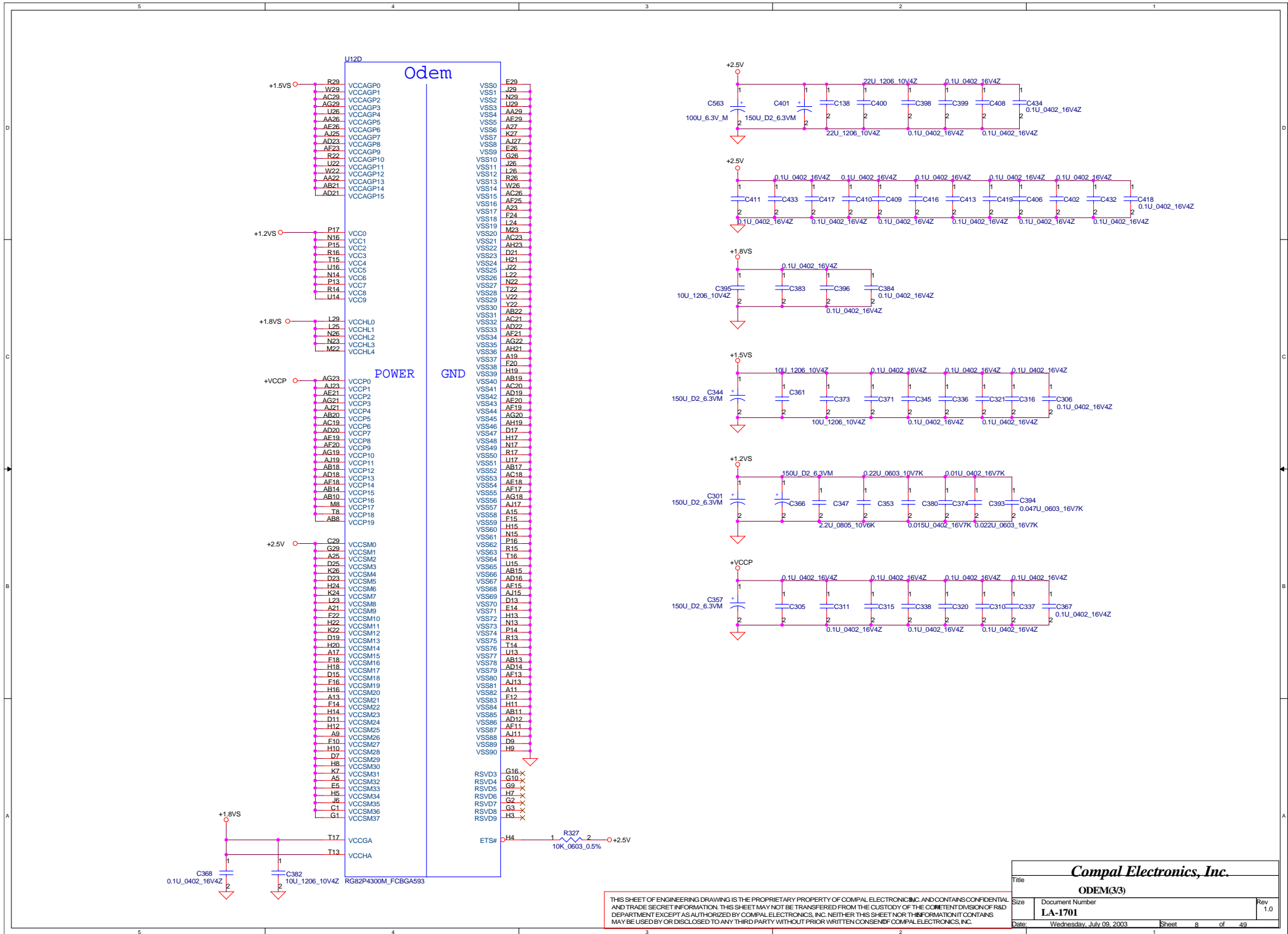
<9,10> DDR_MMA[0..12]  DDR_MMA[0..12]
 <9> DDR_SDQ[0..63]  DDR_SDQ[0..63]
 <9> DDR_SDQS[0..8]  DDR_SDQS[0..8]
 <9> DDR_CB[0..7]  DDR_CB[0..7]



NOTE: 1.M_RCV# max 2Via
 2.G15 to Via max=40mils
 3.G14 to Via max=40mils
 4.Via to Via must = 100mils +-5mils

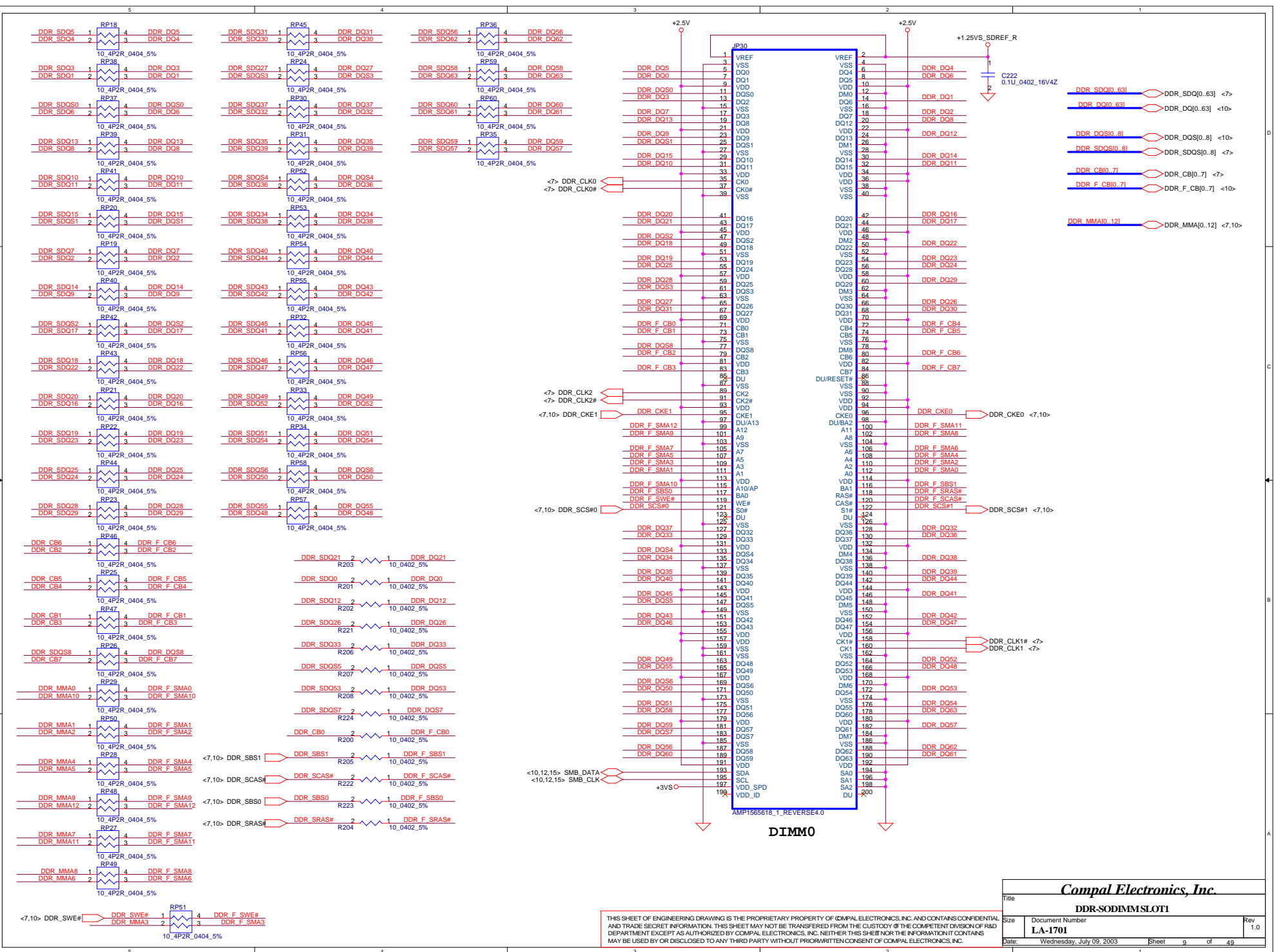
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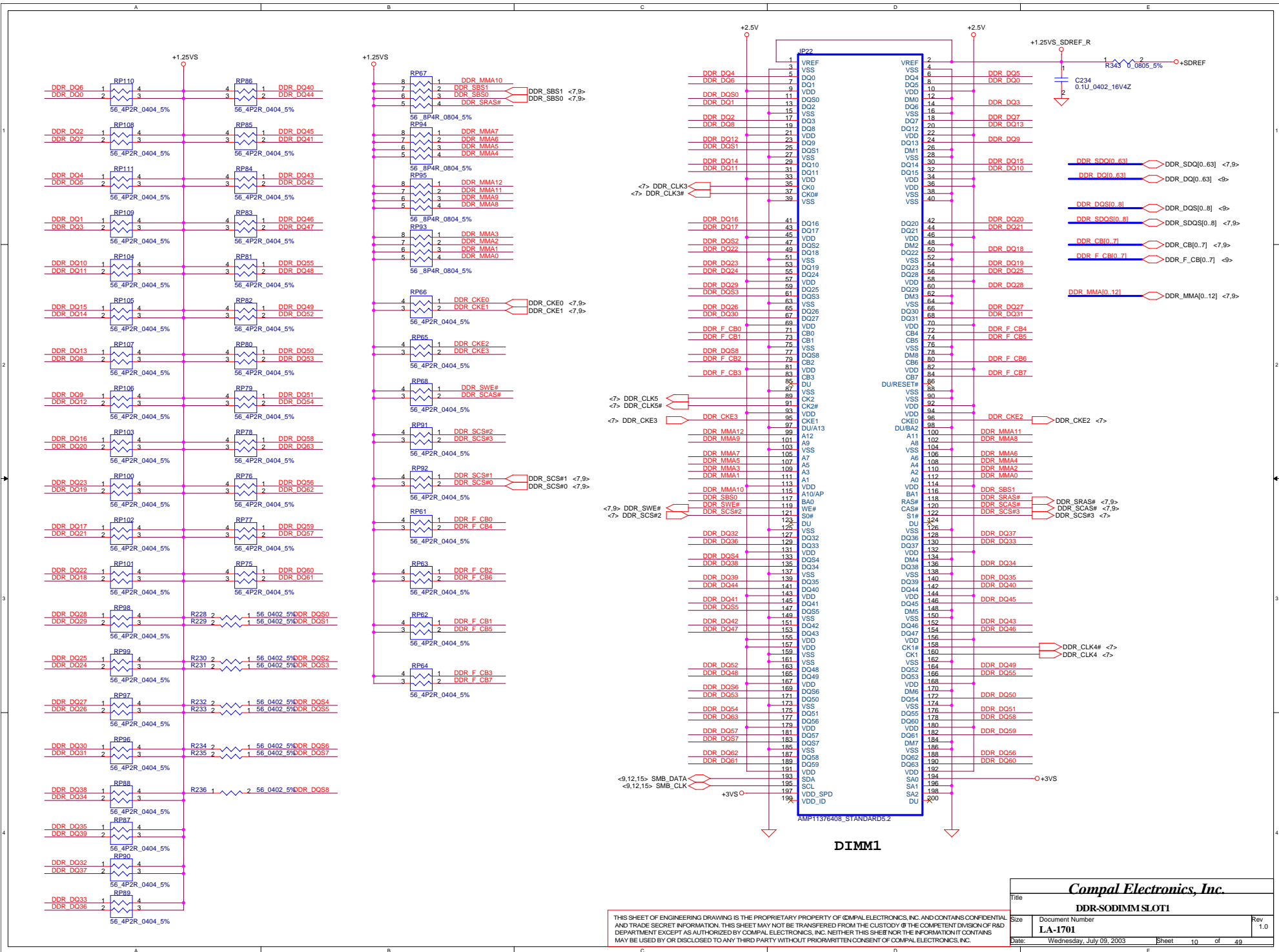
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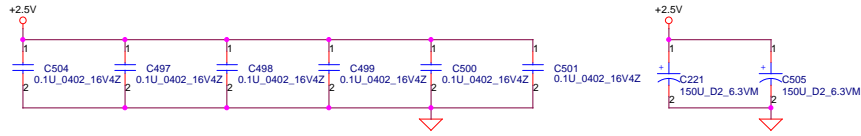
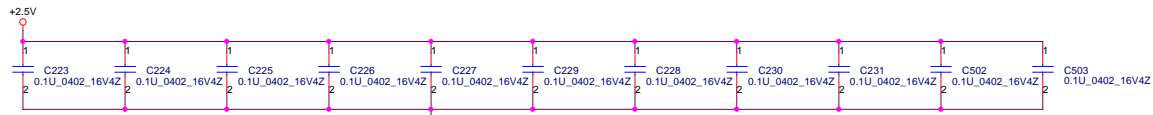
DDR-SODIMMSLOT1		
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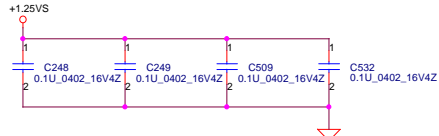
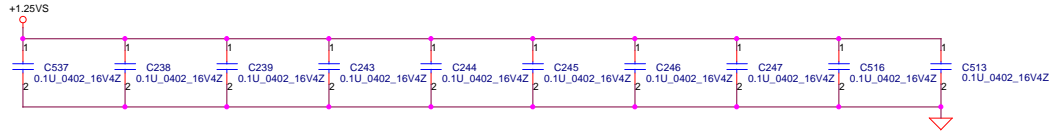
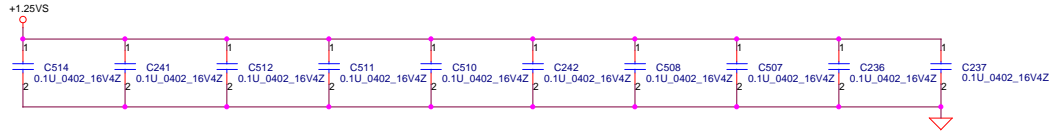
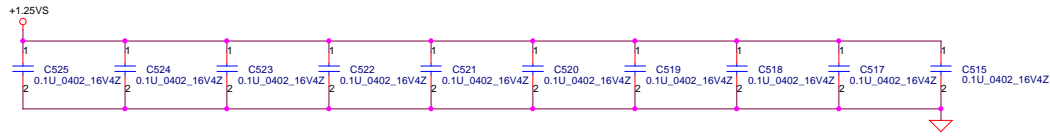
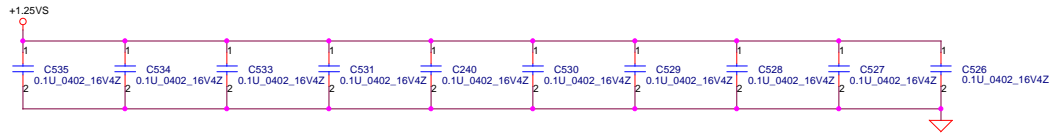
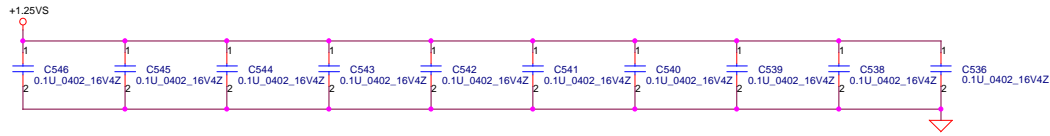


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Layout note :
Distribute as close as possible to DDR-SODIMM.



Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25V

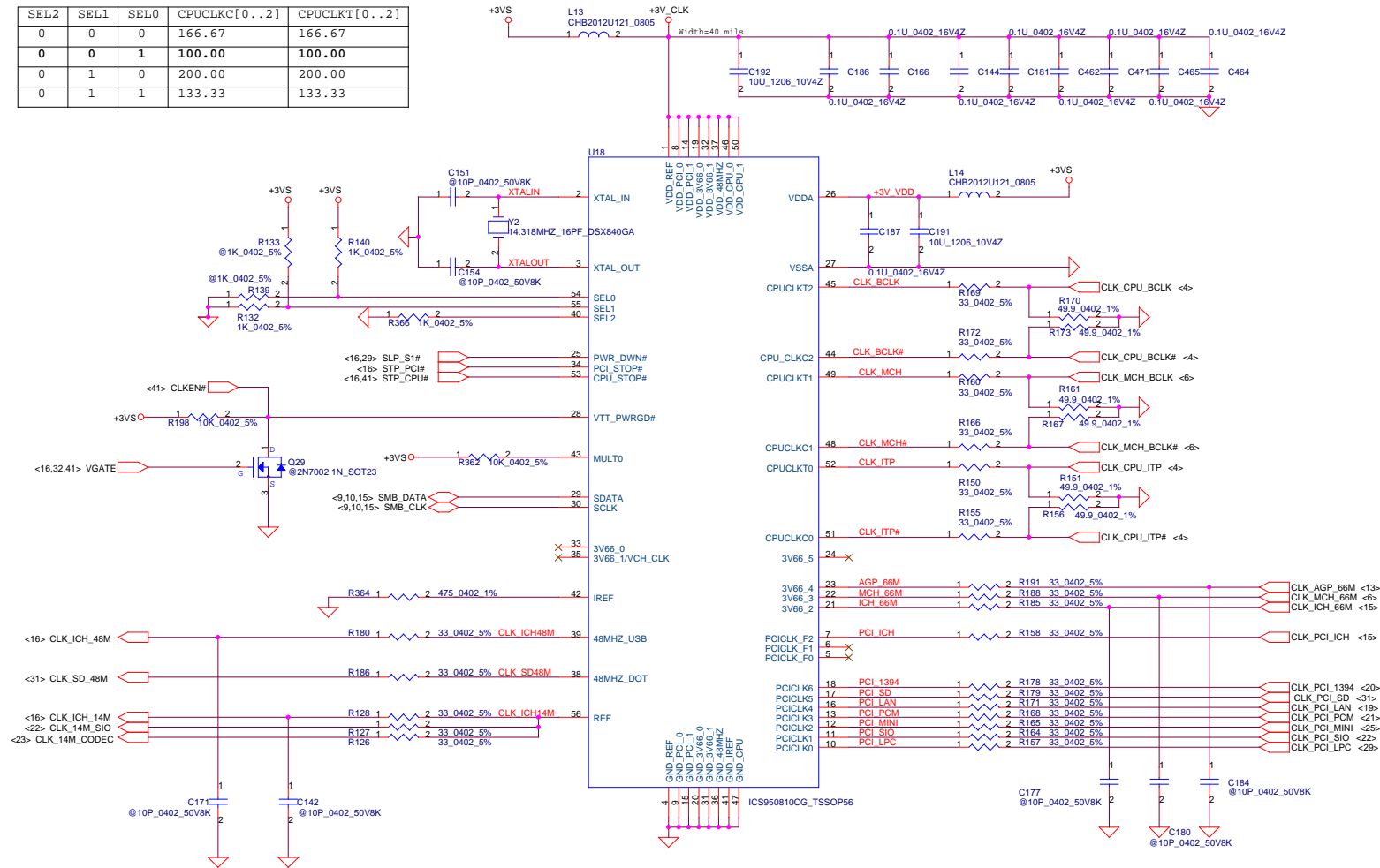


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Title DDR SODIMM Decoupling		
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Clock Generator

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33

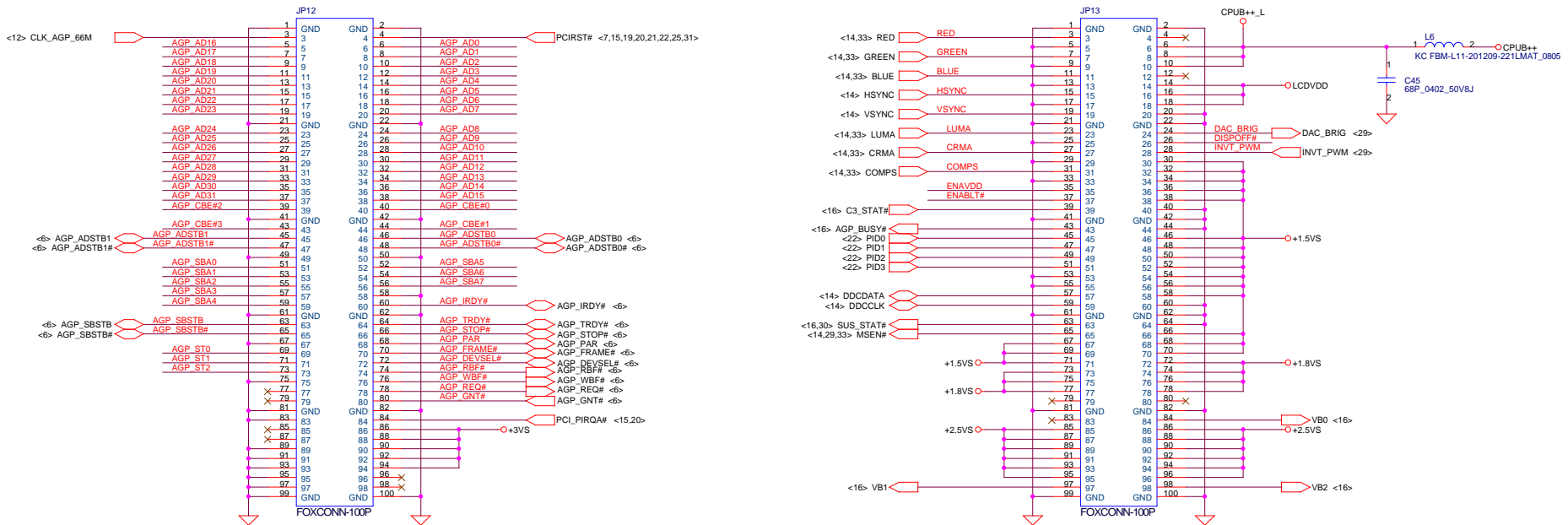


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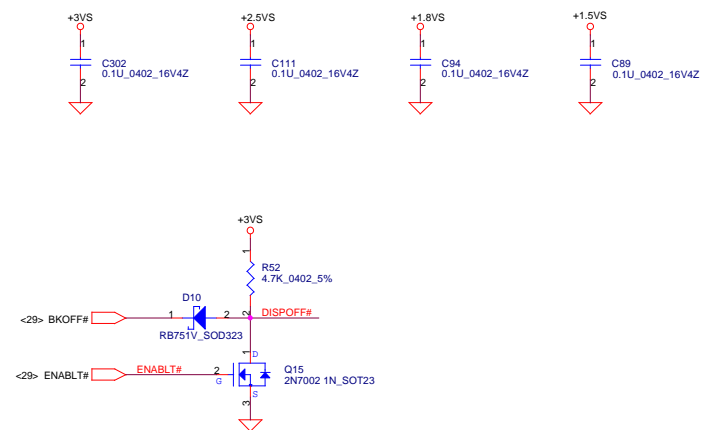
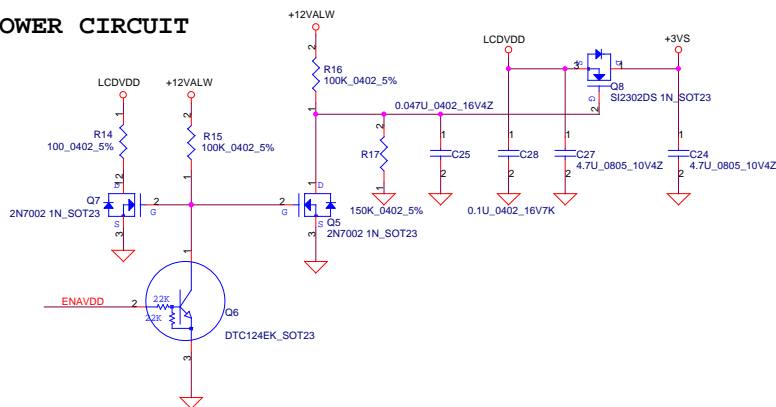
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Clock Generator		
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AGP CONN

<6> AGP_SBA[0..7] <AGP_SBA[0..7]>
 <6> AGP_CBE#[0..3] <AGP_CBE#[0..3]>
 <6> AGP_AD[0..31] <AGP_AD[0..31]>
 <6> AGP_ST[0..2] <AGP_ST[0..2]>



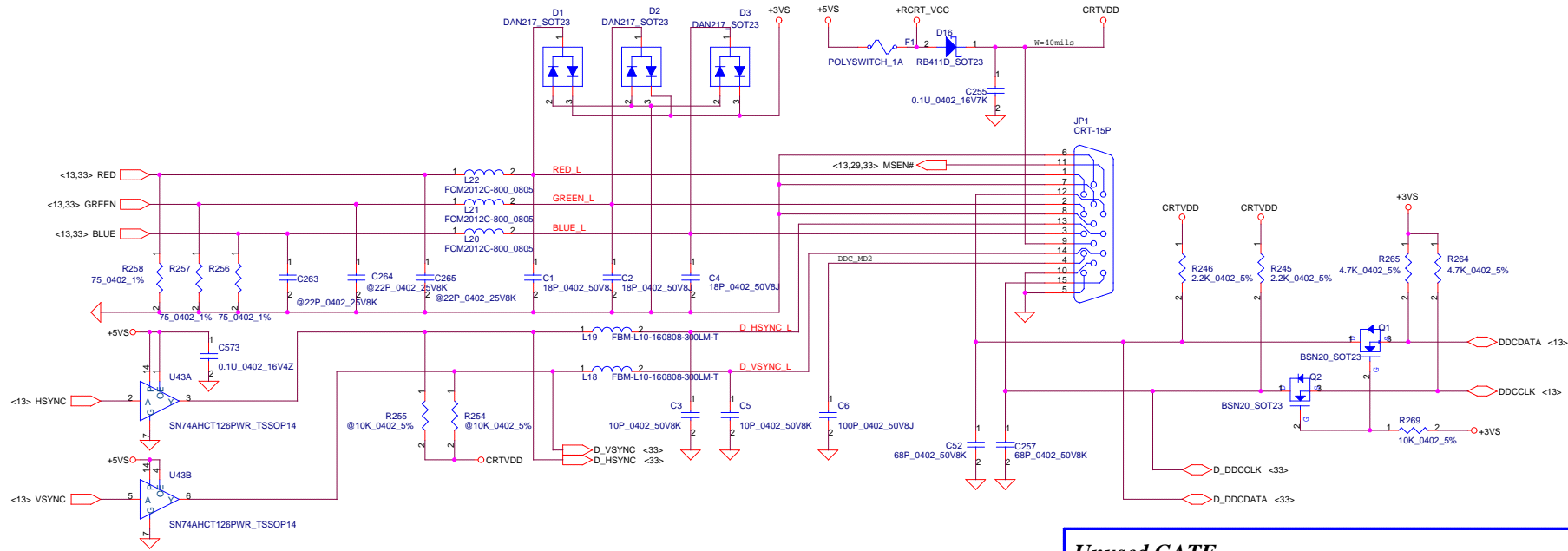
LCD POWER CIRCUIT



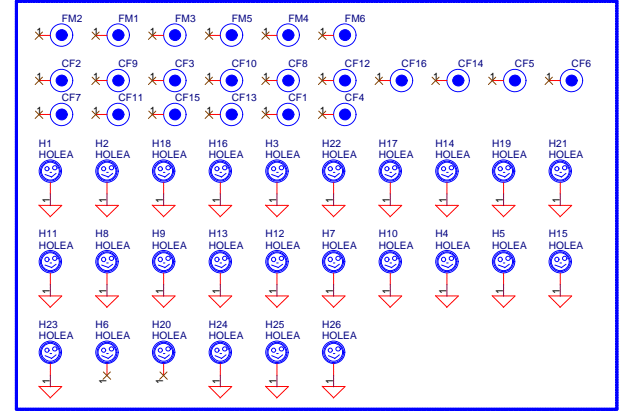
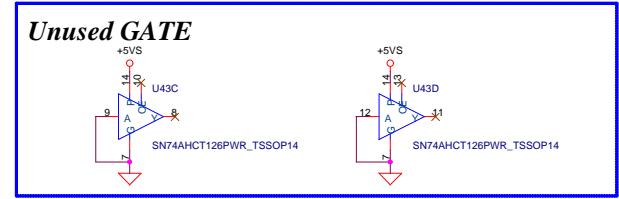
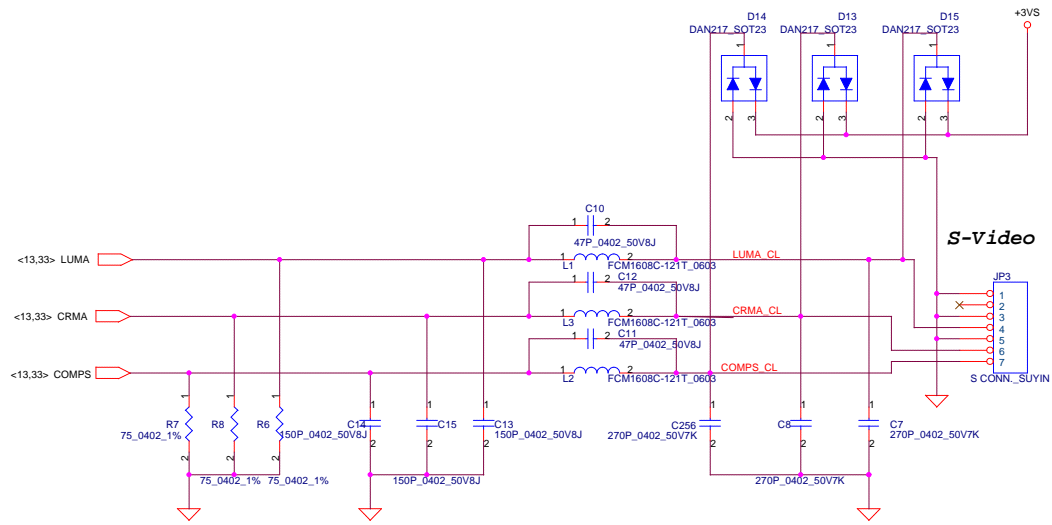
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CRT Connector

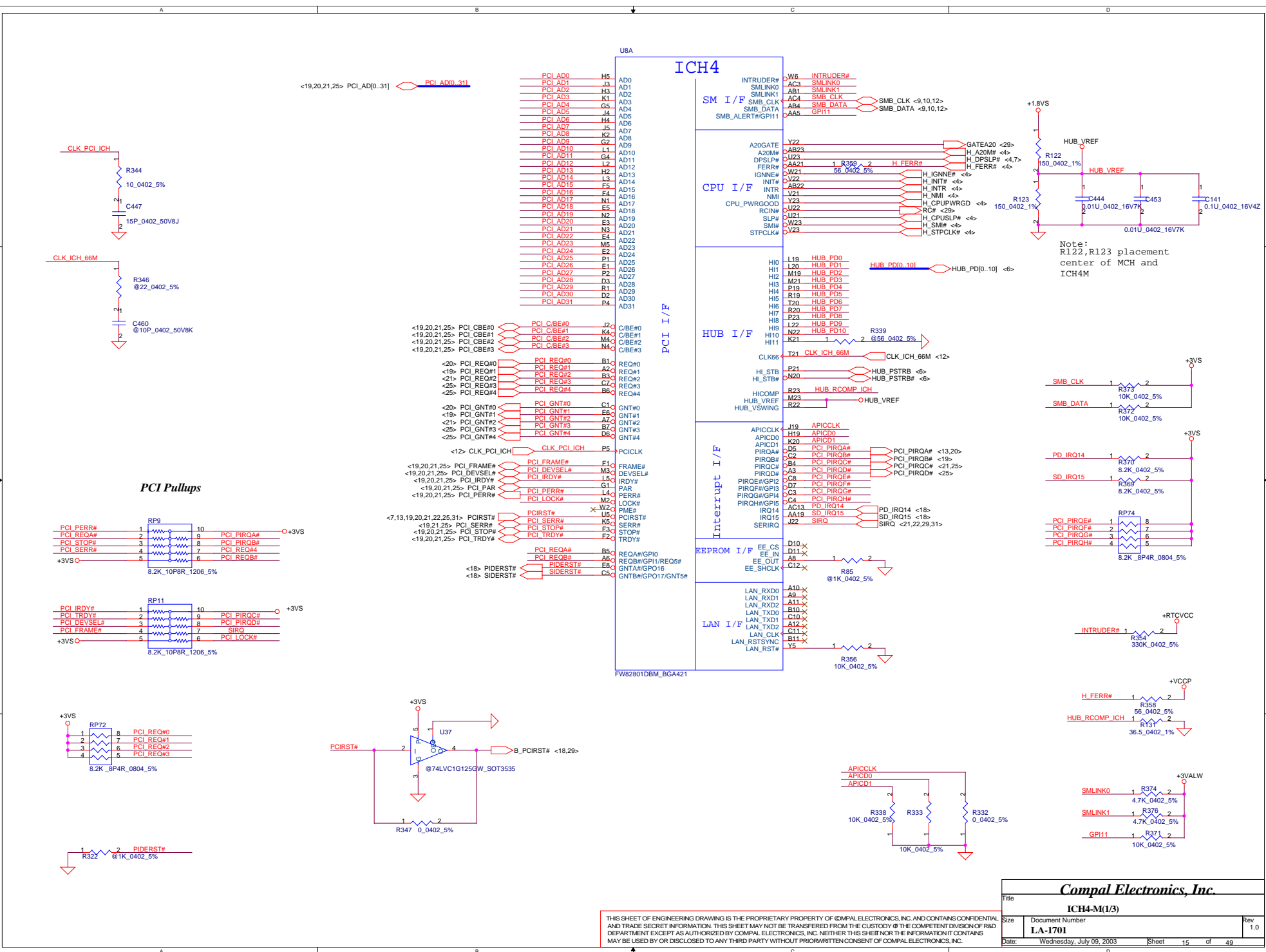


TV-Out Connector



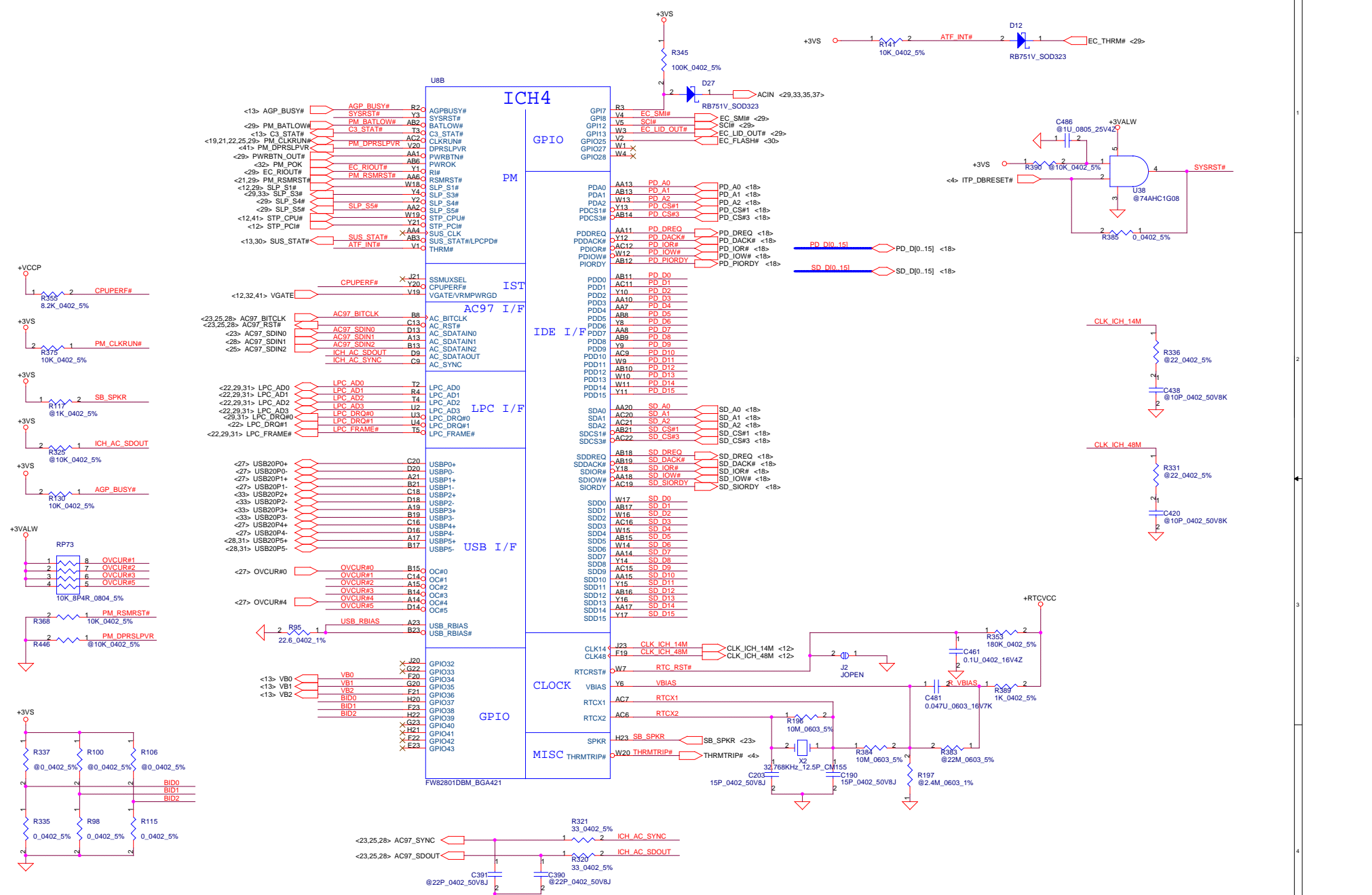
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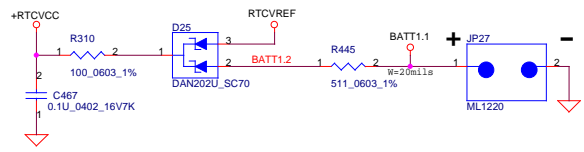
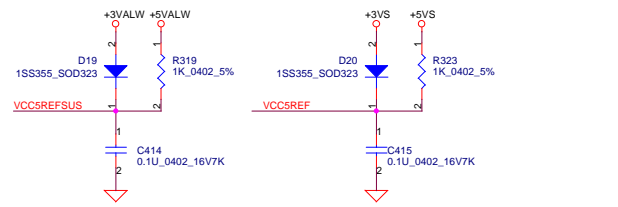
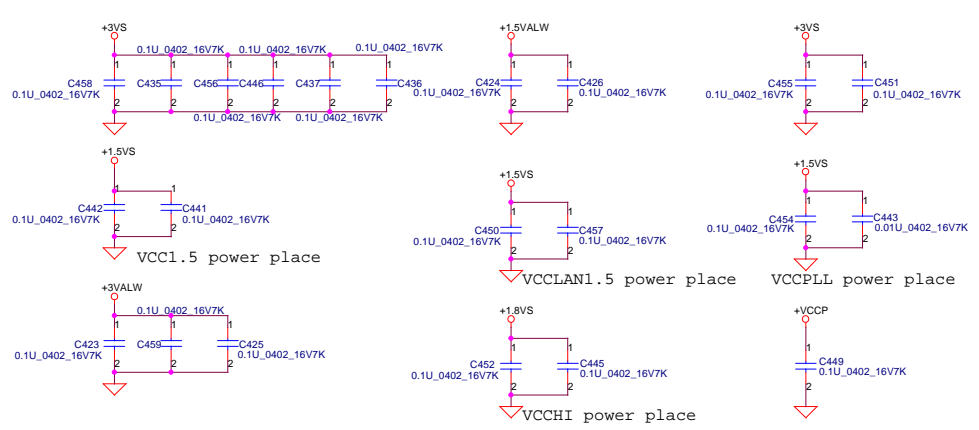
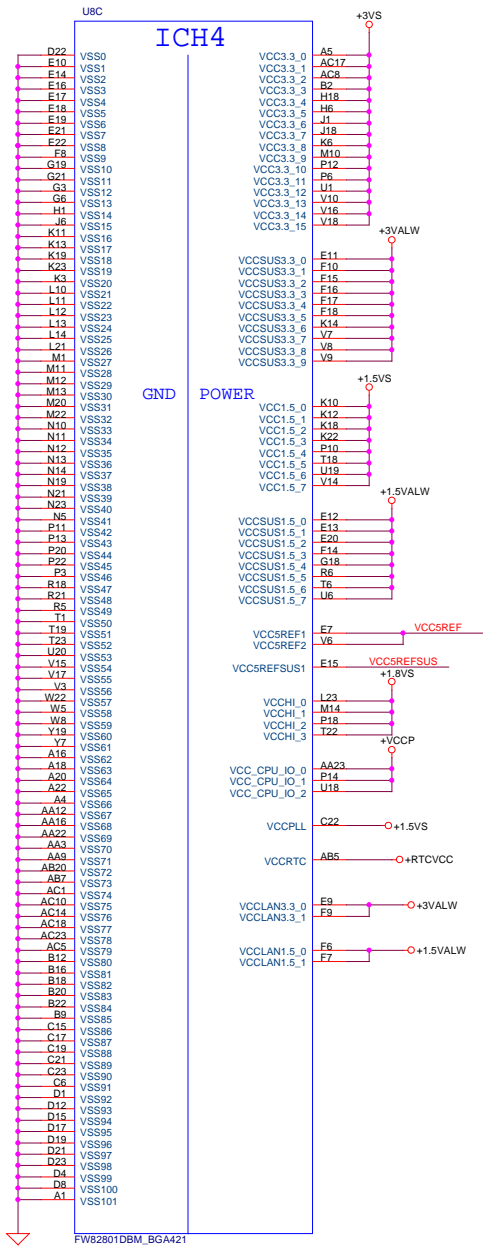
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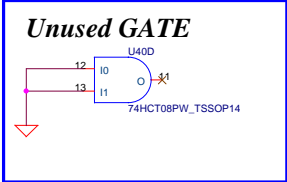
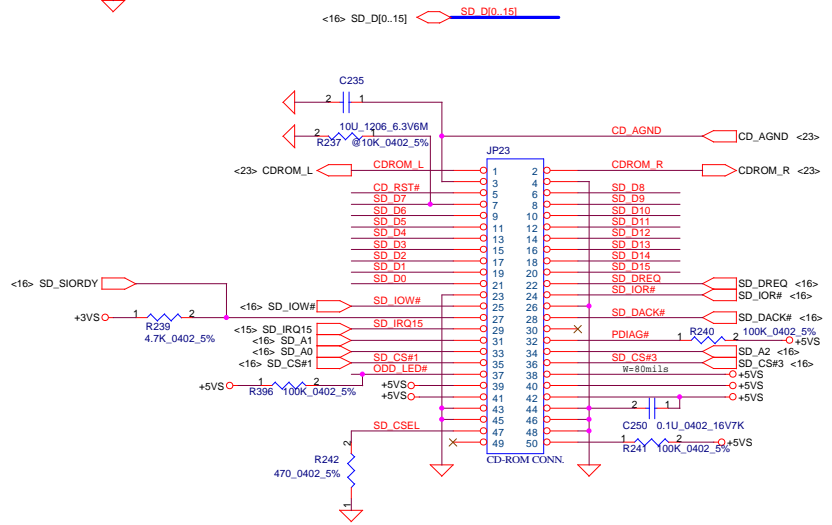
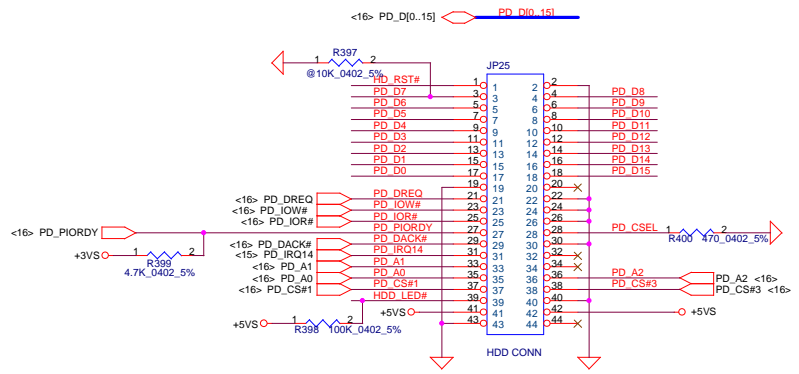
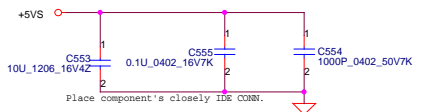
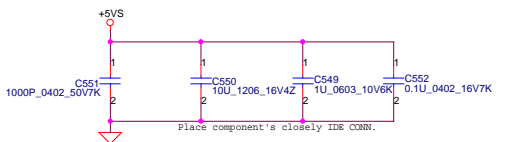
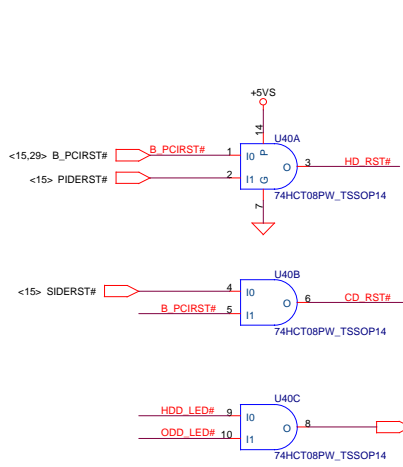
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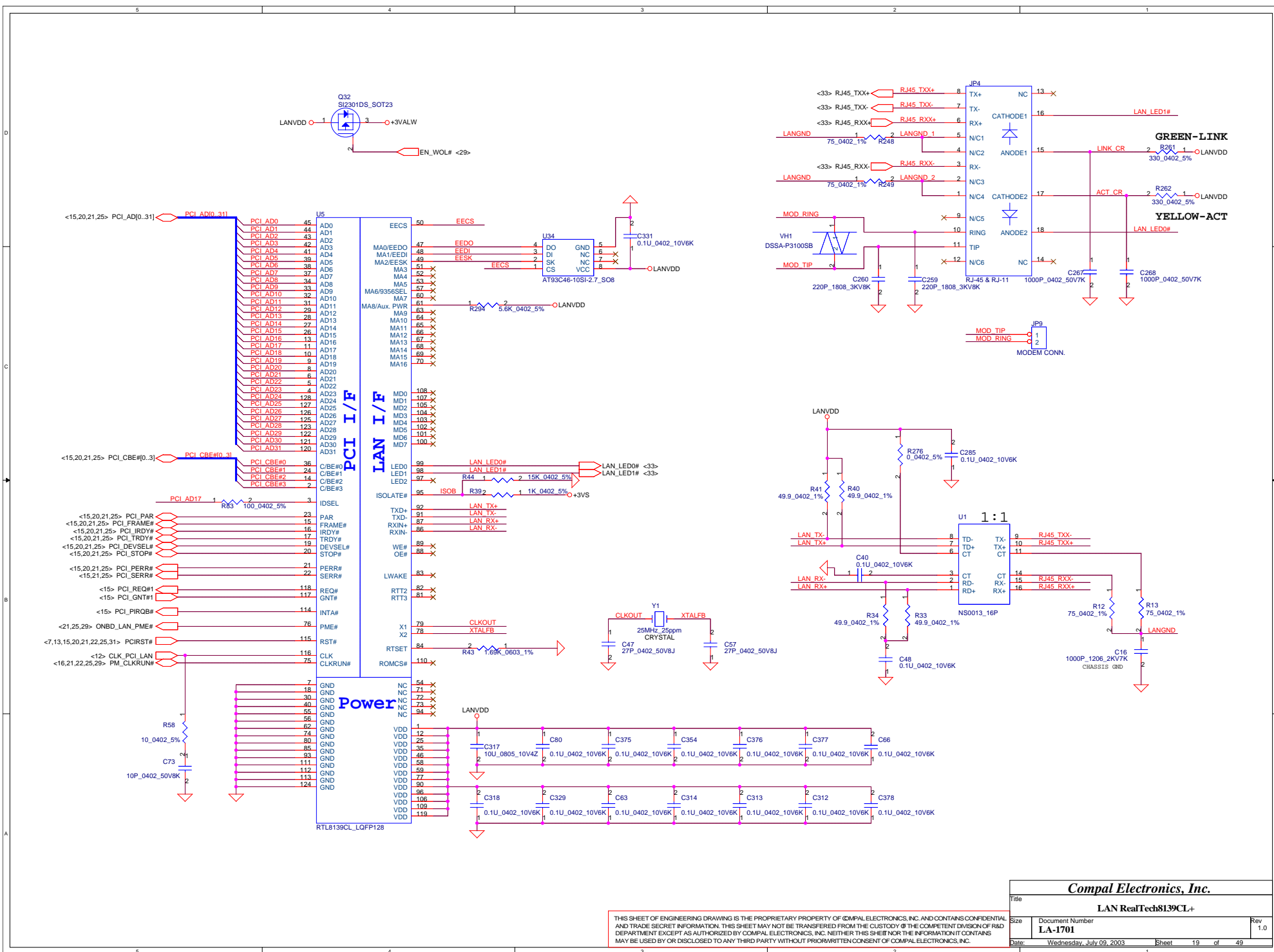
Compal Electronics, Inc.		
Title ICH4-M(3/3)		
Size	Document Number	Rev
LA-1701		1.0
Date:	Wednesday, July 09, 2003	Sheet 17 of 49

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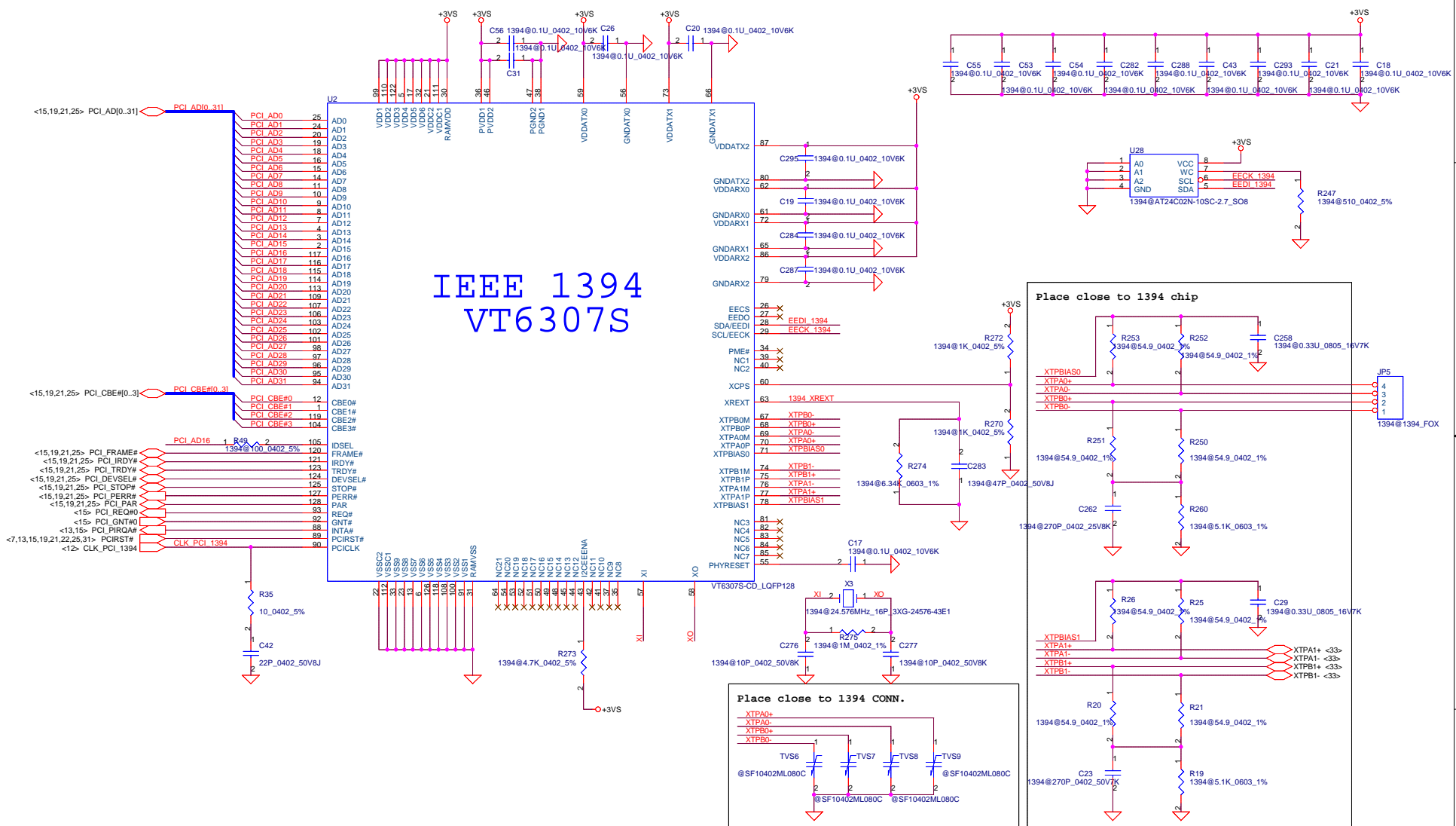
Compal Electronics, Inc.		
Title HDD & CDROM Connector		
Size	Document Number LA-1701	Rev 1.0
Date	Wednesday, July 09, 2003	Sheet 18 of 49



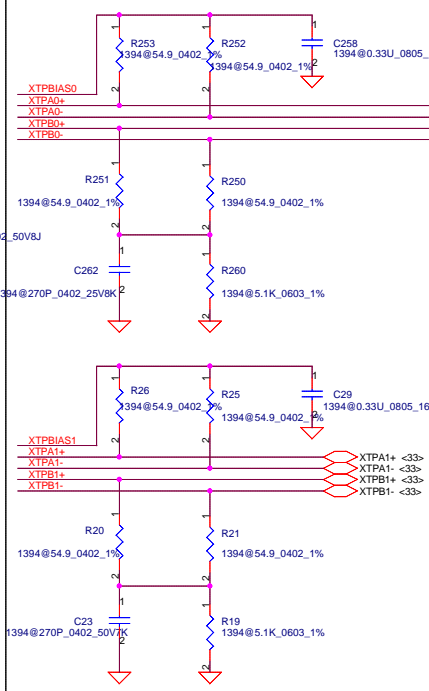
Compal Electronics, Inc.		
Title LAN RealTech8139CL+		
Size	Document Number	Rev
	LA-1701	1.0
Date:	Wednesday, July 09, 2003	Sheet 19 of 49

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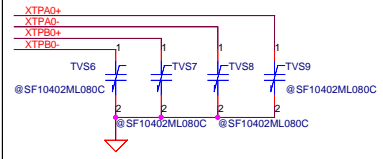
IEEE 1394 VT6307S

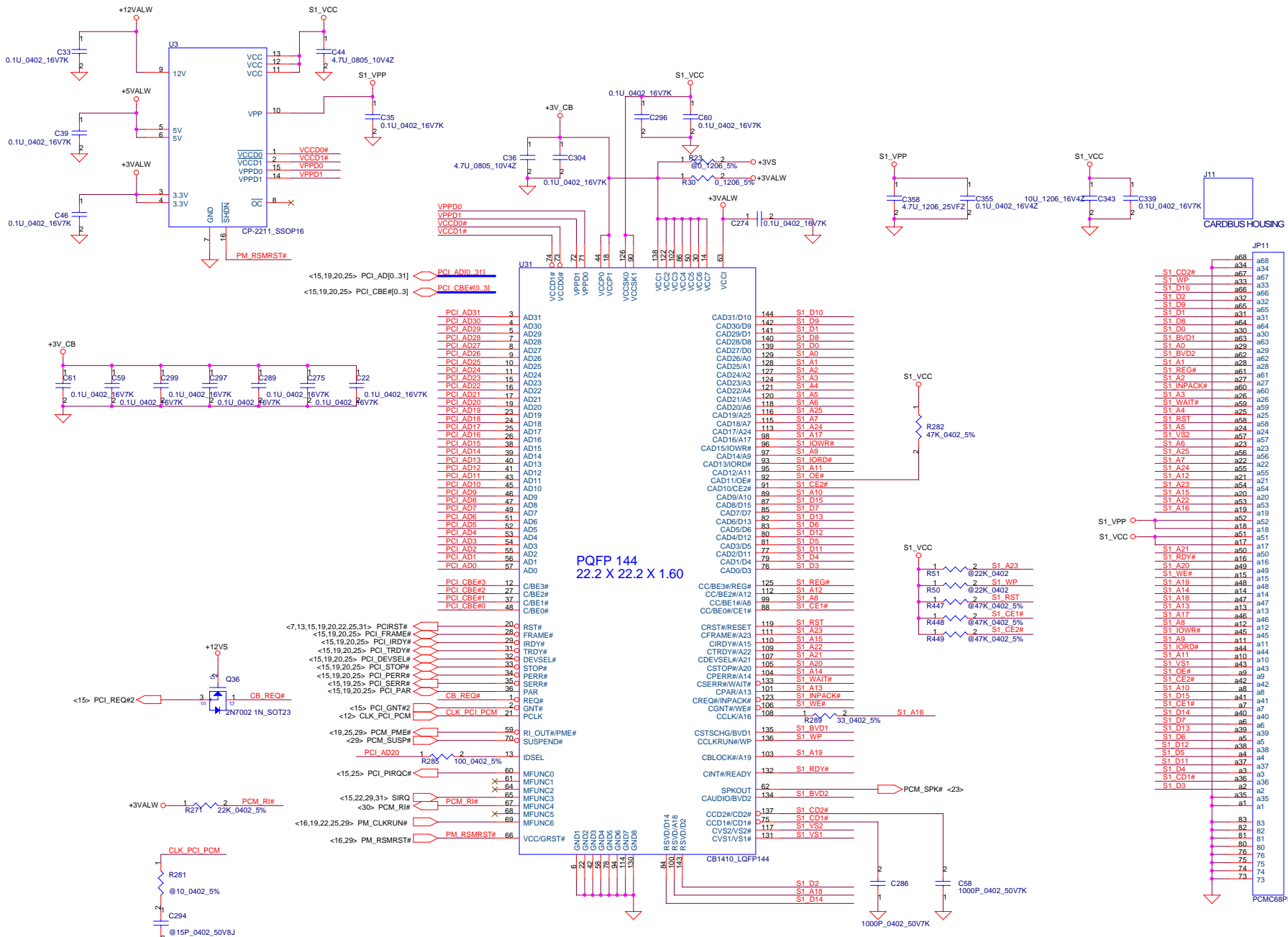


Place close to 1394 chip



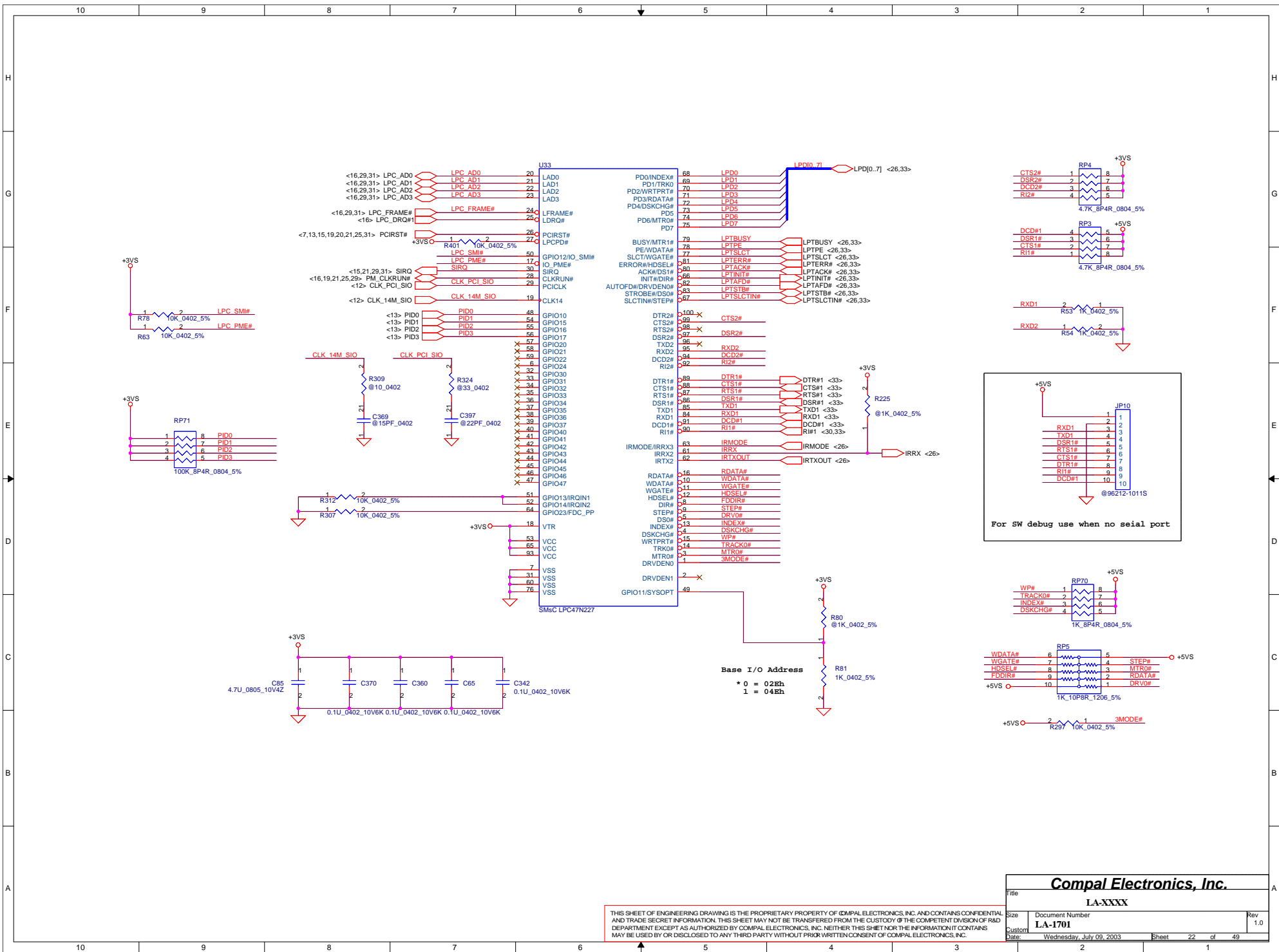
Place close to 1394 CONN.



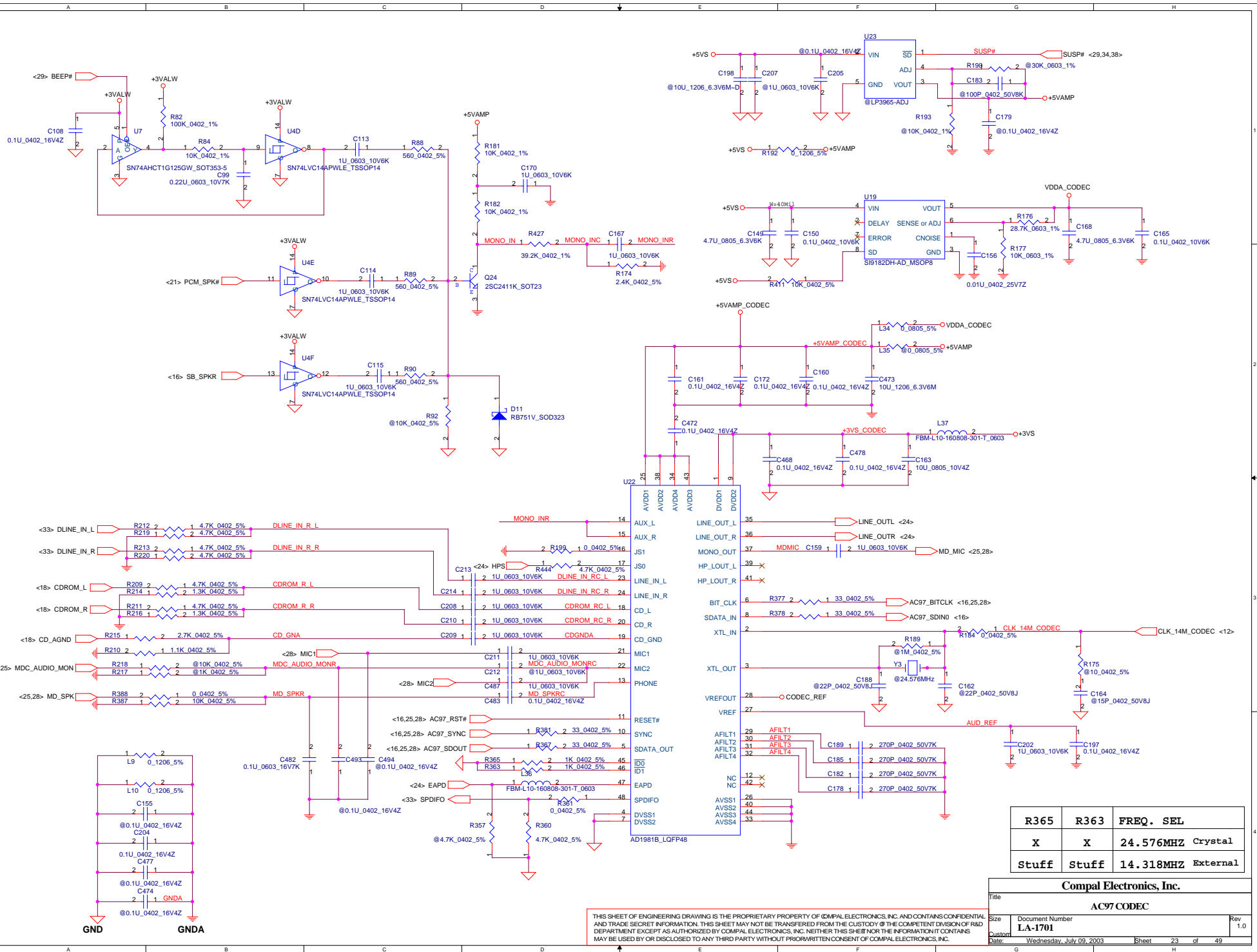


Compal Electronics, Inc.		
CardBus Controller CB1410 & Socket		
Title	Document Number	Rev
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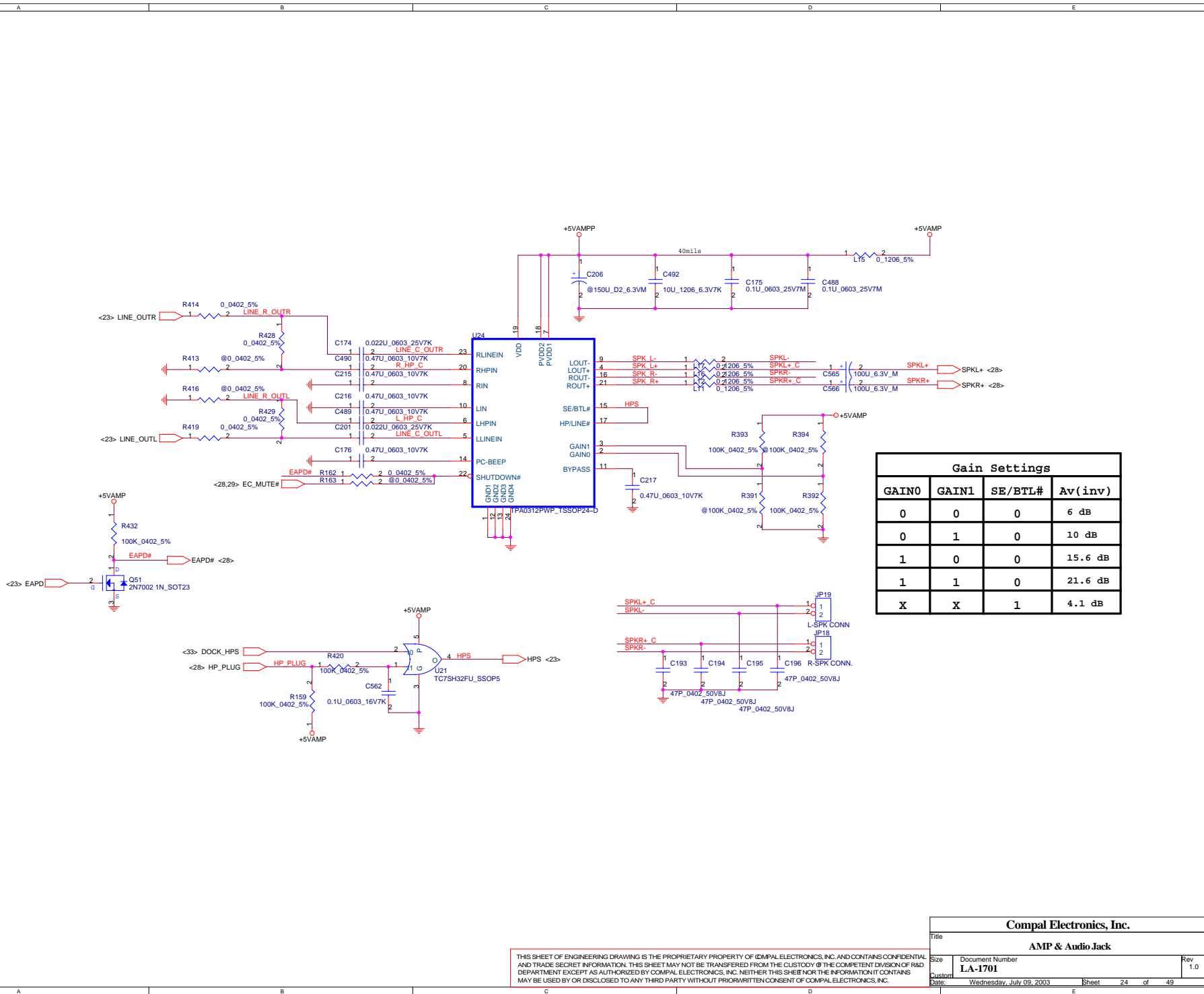
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R365	R363	FREQ. SEL
X	X	24.576MHZ Crystal
Stuff	Stuff	14.318MHZ External

Compal Electronics, Inc.		
AC97 CODEC		
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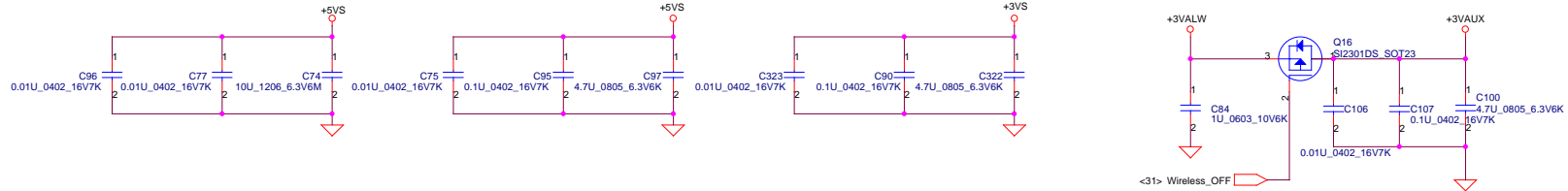
Gain Settings			
GAIN0	GAIN1	SE/BTL#	Av(inv)
0	0	0	6 dB
0	1	0	10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

Compal Electronics, Inc.

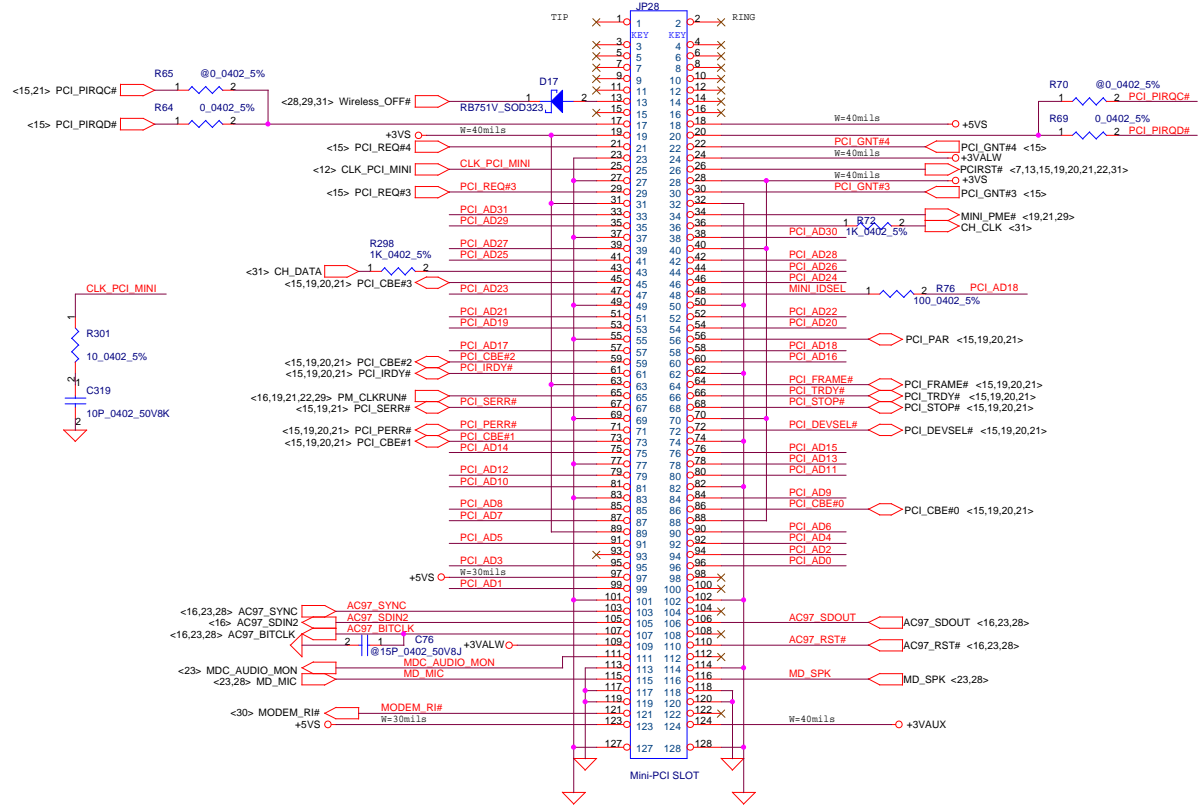
AMP & Audio Jack

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	LA-1701		1.0
Customer	Date	Sheet	of
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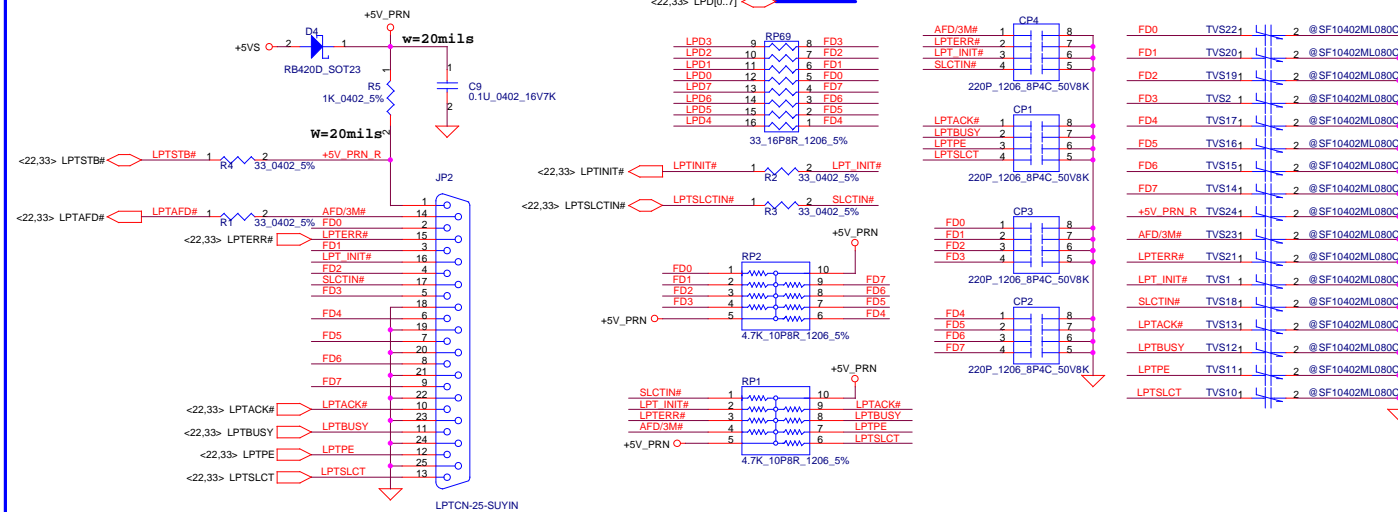
PCI_AD[0..31] PCI_AD[0..31] <15,19,20,21>



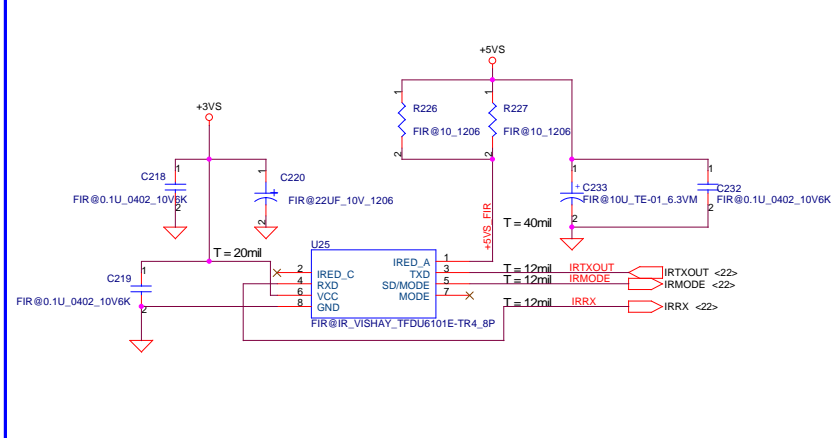
Title		
Compal Electronics, Inc.		
Mini PCI Slot		
Size	Document Number	Rev
	LA-1701	1.0
Date:	Wednesday, July 09, 2003	Sheet 25 of 49

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Parallel Port



FIR Module



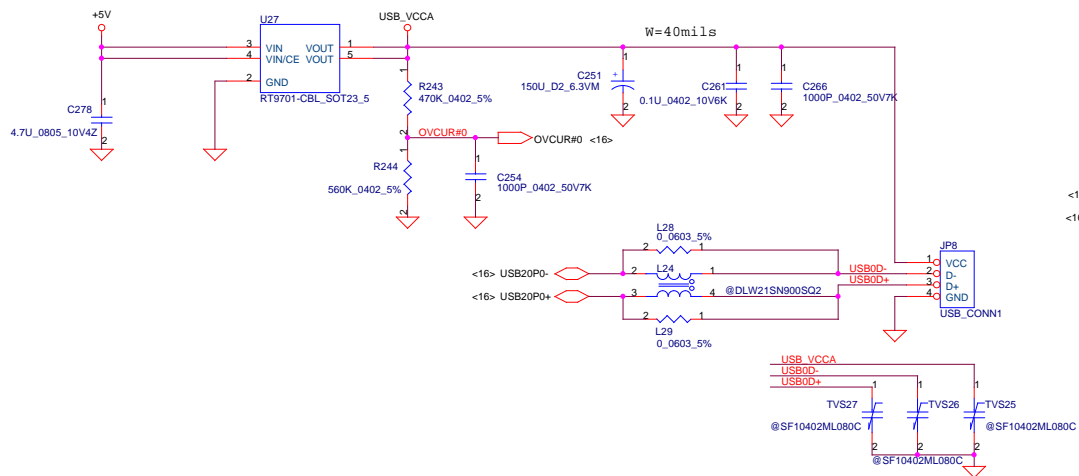
Compal Electronics, Inc.

LPT Port & FIR

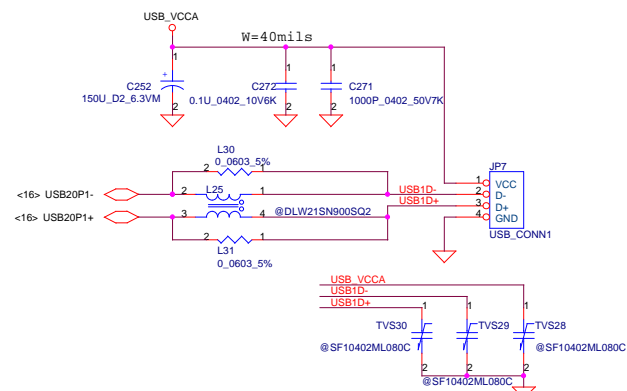
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Title	LPT Port & FIR	
Size	Document Number	Rev
	LA-1701	1.0
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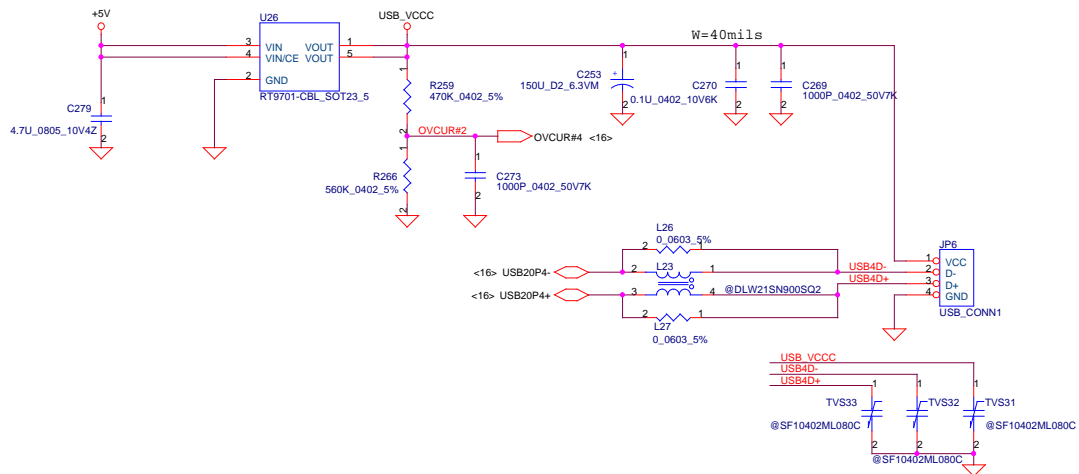
USB CONNECTOR 1



USB CONNECTOR 2



USB CONNECTOR 3

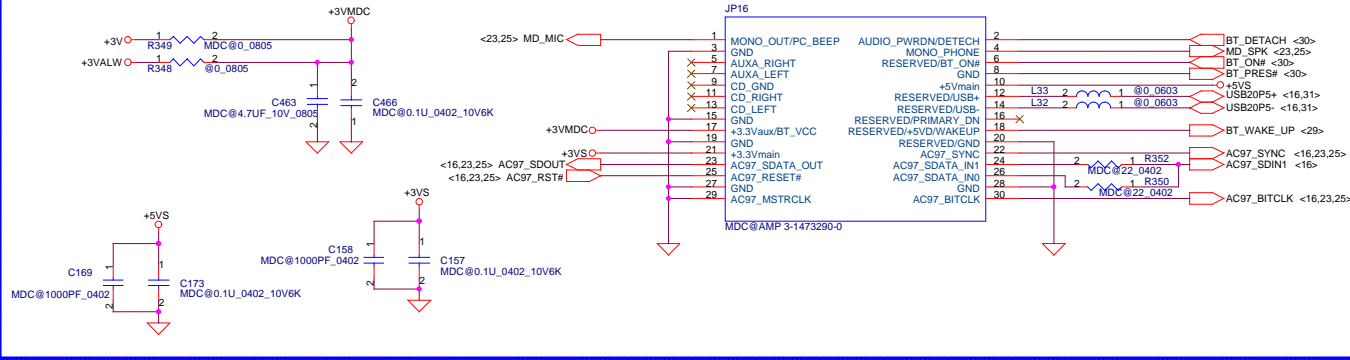


Compal Electronics, Inc.

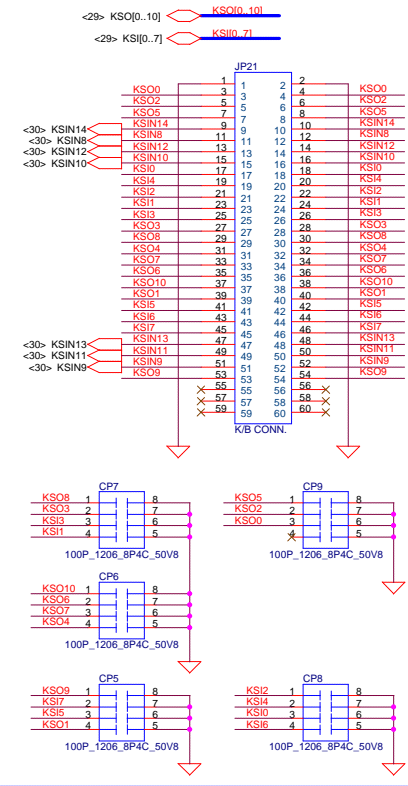
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USB Connector		
Size	Document Number	Rev
Custom	LA-1701	1.0
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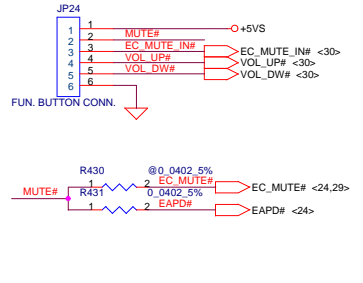
MDC Conn.



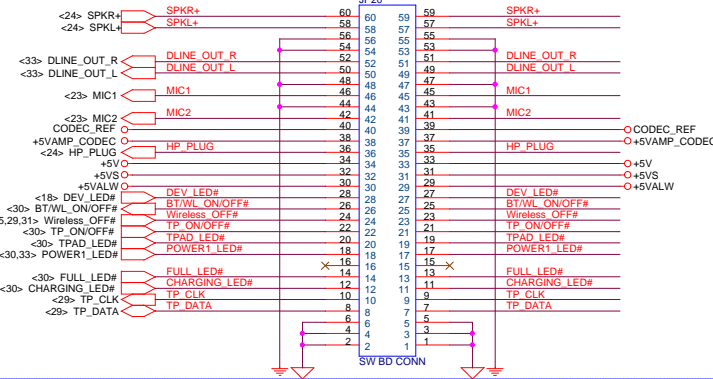
INT_KBD CONN.



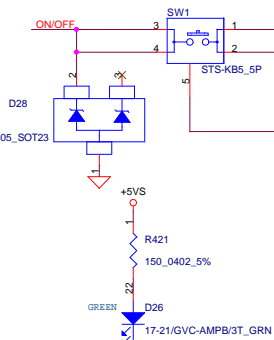
FUN. BUTTON BD.



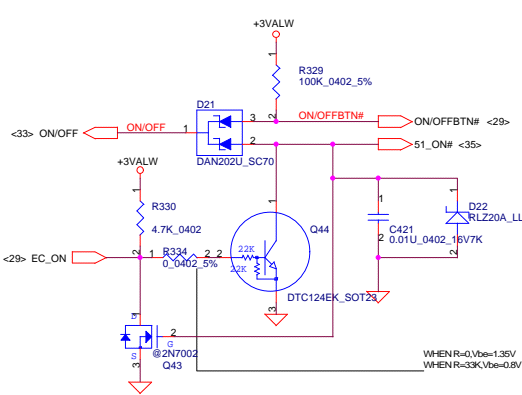
TP & LED BD.



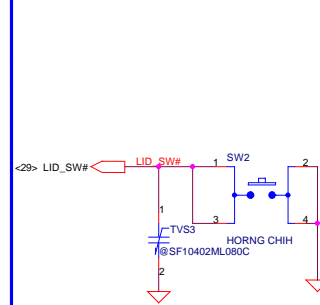
Power button



ON/OFF BUTTON



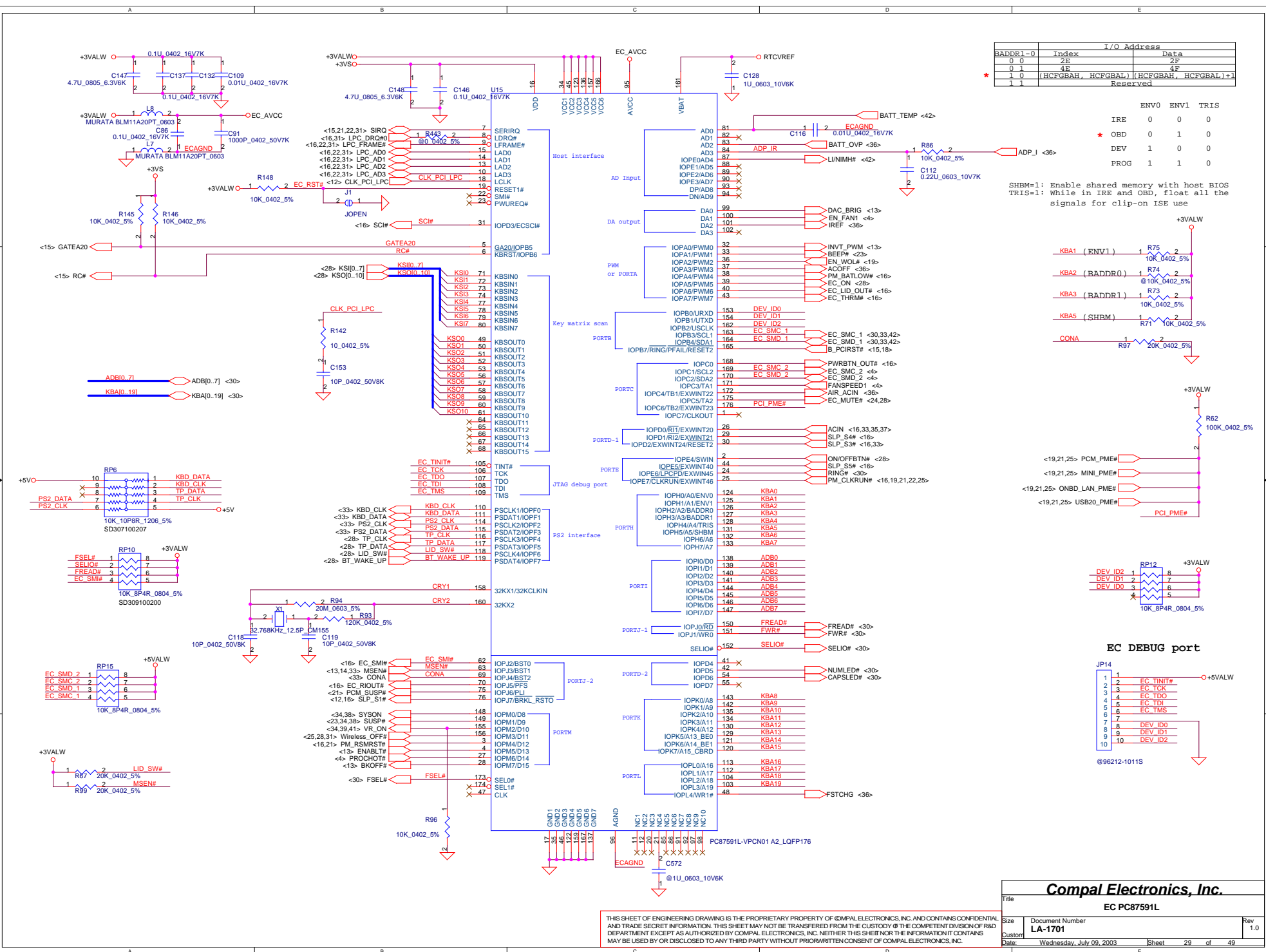
LID SW



Compal Electronics, Inc.

MDC/BT/KBD/ON_OFF/LID		
Title	Document Number	Rev
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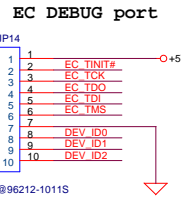
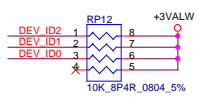
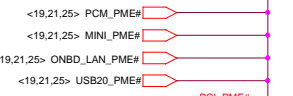
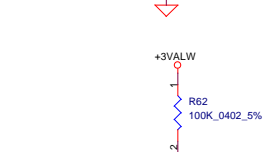
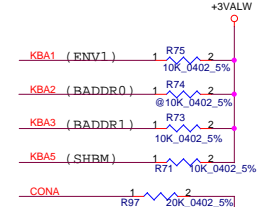
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BADDR_0	Index	I/O Address	Data
0 0	2E		2F
0 1	4F		4F
1 0		{HCFGBAH, HCFGBAL} {HCFGBAH, HCFGBAL}+1	
1 1		Reserved	

ENVO	ENV1	TRIS
IRE	0	0
* OBD	0	1
DEV	1	0
PROG	1	1

SHBM=1: Enable shared memory with host BIOS
 TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use



Compal Electronics, Inc.
 EC PC87591L

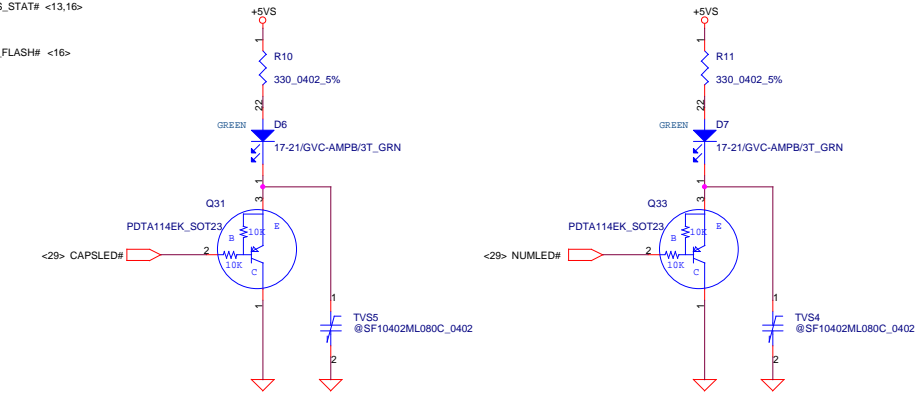
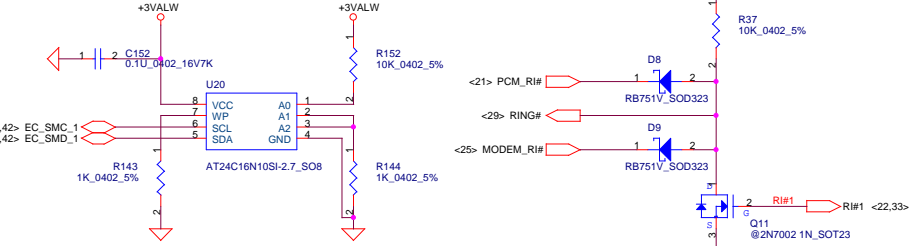
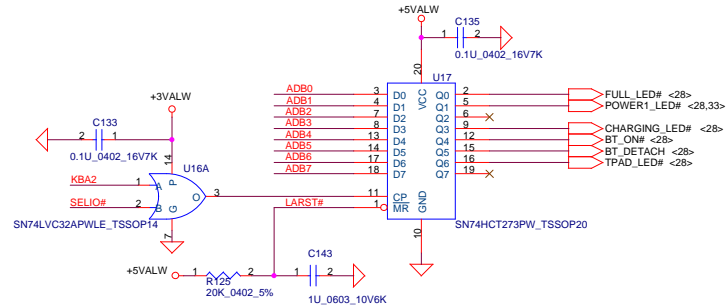
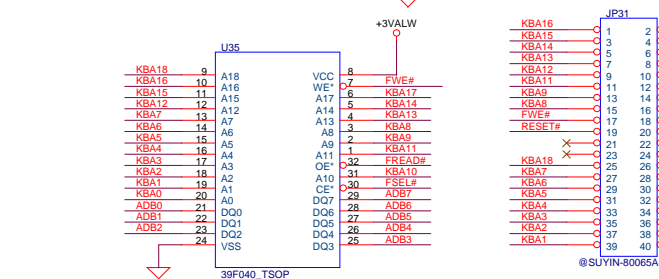
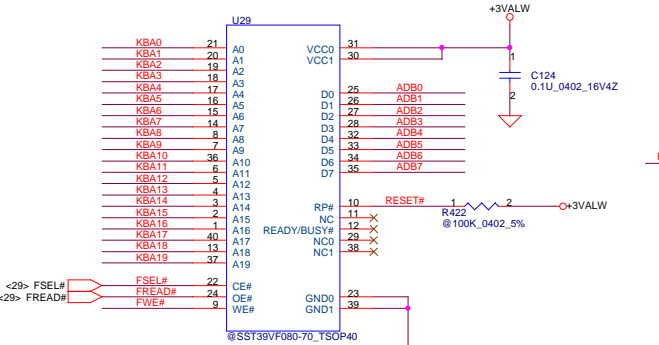
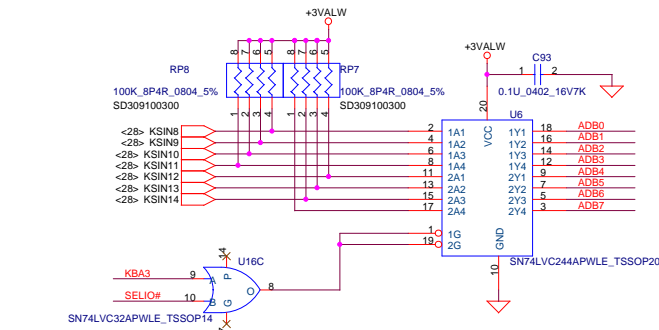
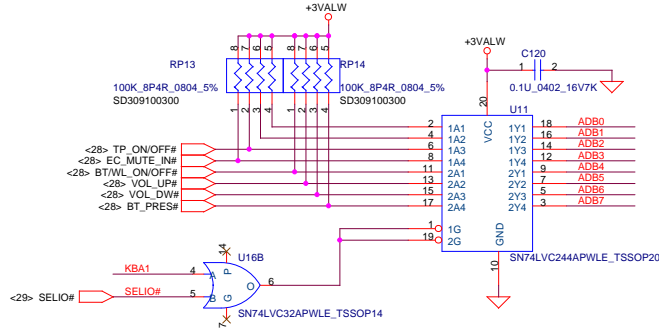
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Size	Document Number	Rev
Custom	LA-1701	1.0
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INPUT

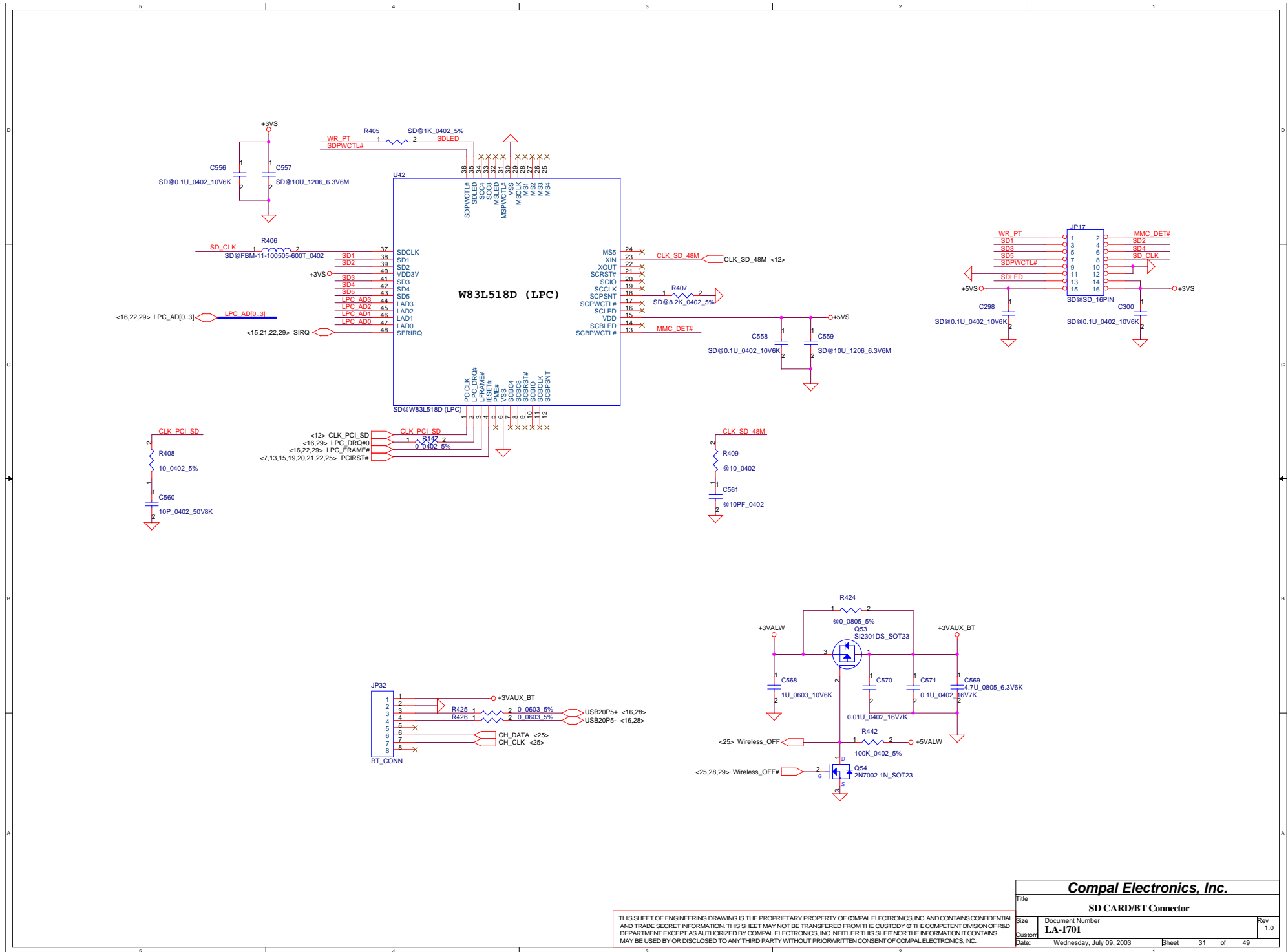
<29> KBA[0..19]
<29> ADB[0..7]

OUTPUT



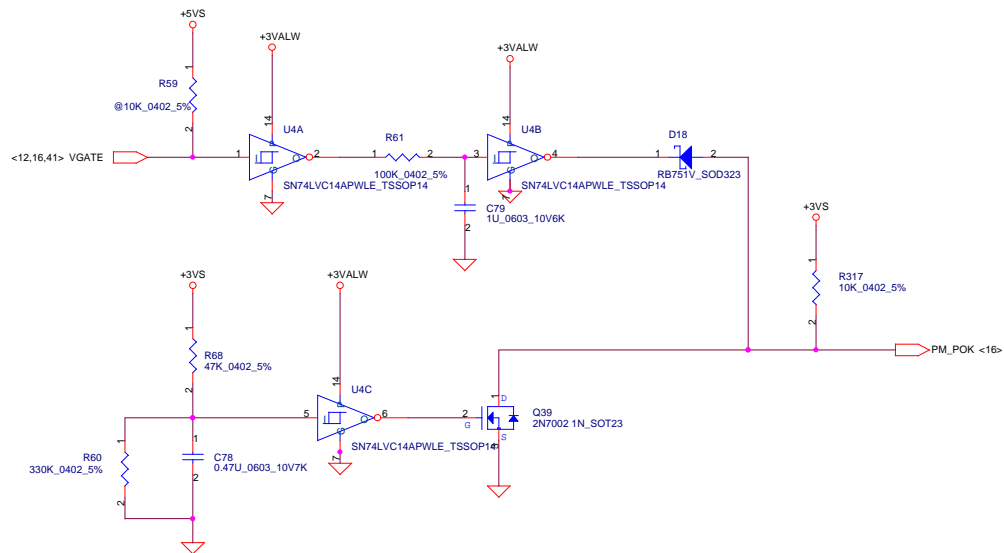
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Table with 4 columns: Title, Size, Date, and Rev. Title: Compal Electronics, Inc. BIOS & EC I/O Port LA-1701. Size: Document Number LA-1701. Date: Wednesday, July 09, 2003. Rev: 1.0. Sheet: 30 of 49.



Title			
SD CARD/BT Connector			
Size	Document Number	Rev	
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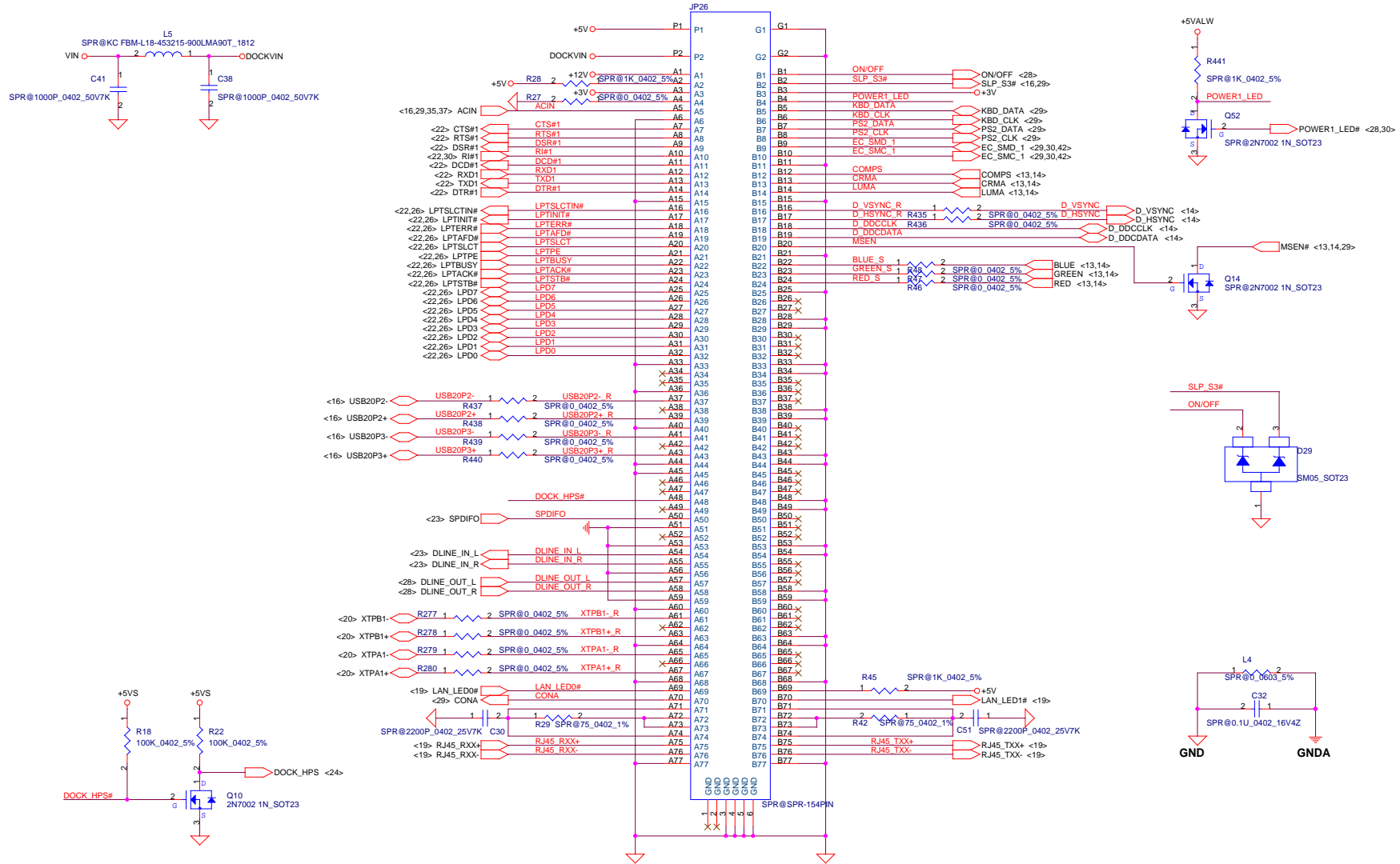
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Compal Electronics, Inc.			
RESET CKT			
Title	Document Number	Rev	
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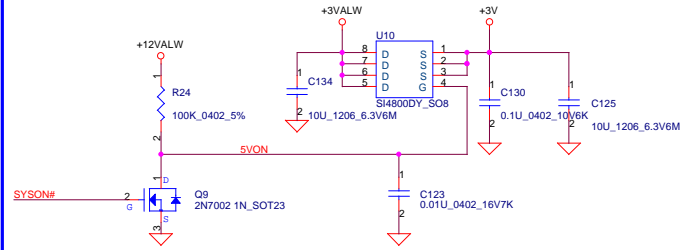
SPR CONN. 154PIN



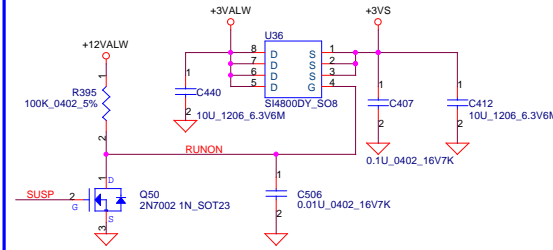
Compal Electronics, Inc.		
Title SPR Connector		
Size	Document Number	Rev
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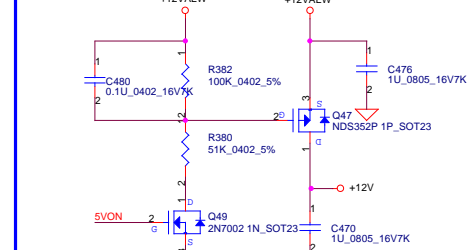
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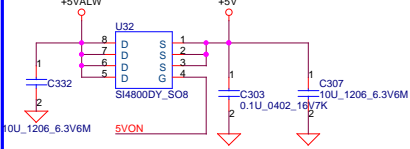
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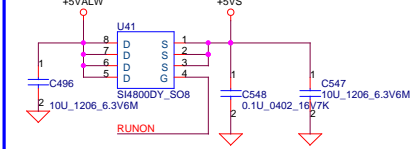
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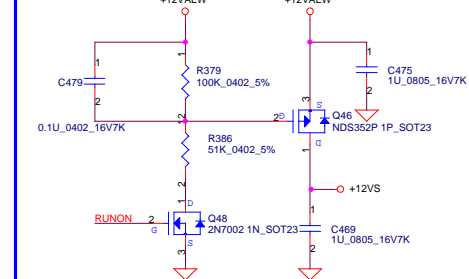
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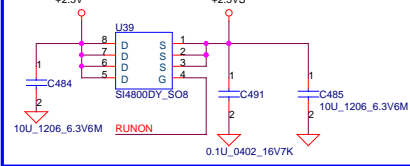
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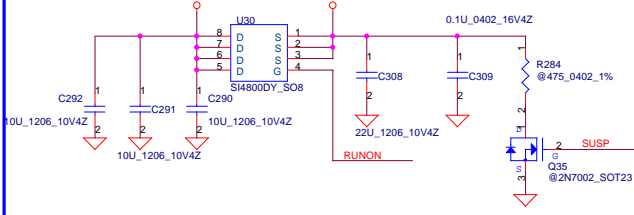
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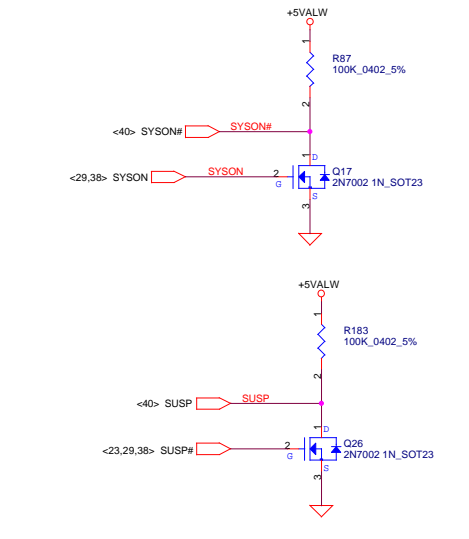
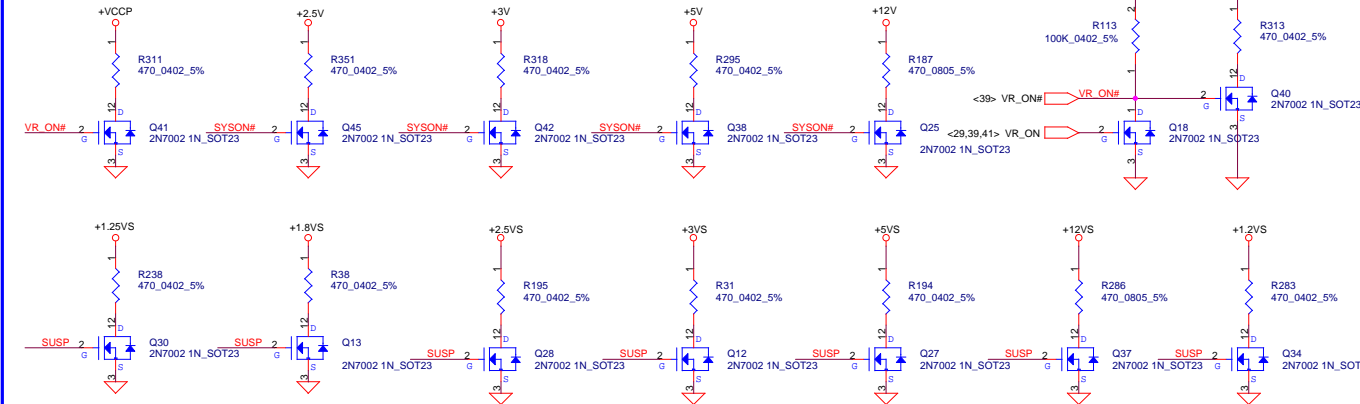
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+1.5VALW to +1.5VS Transfer



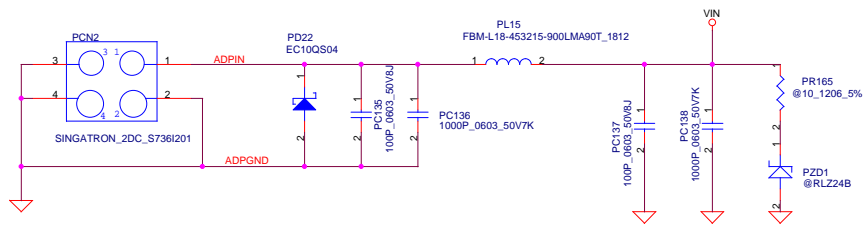
Discharge circuit



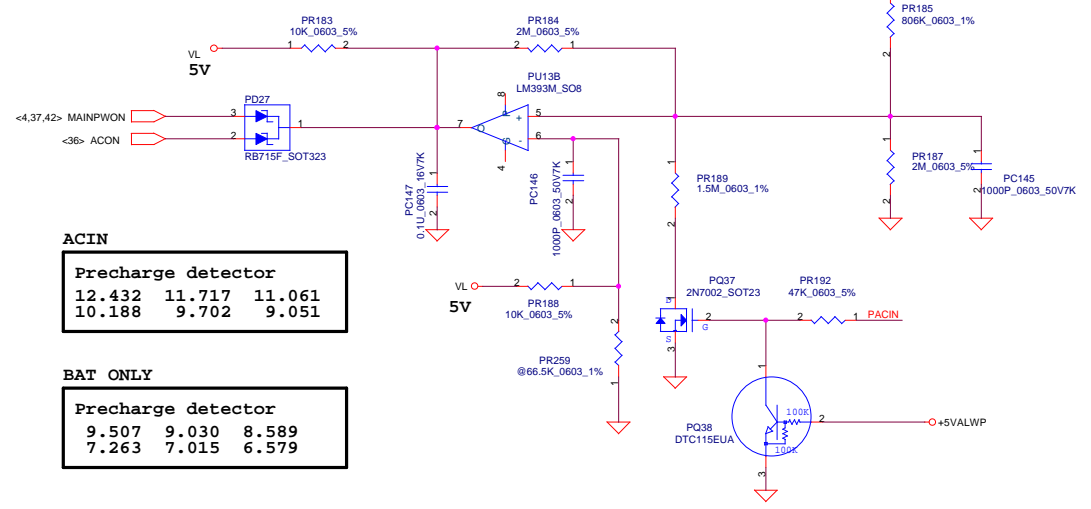
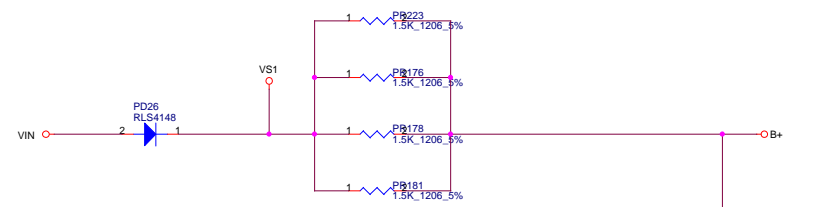
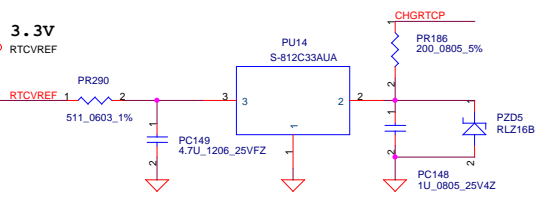
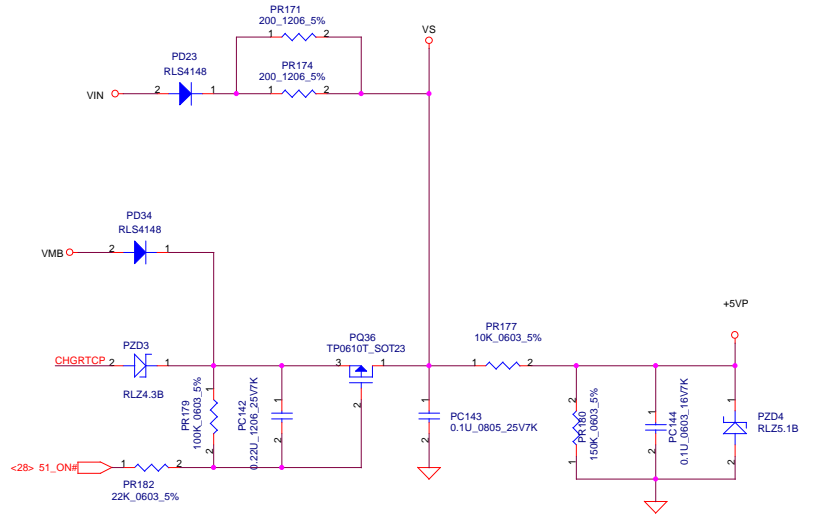
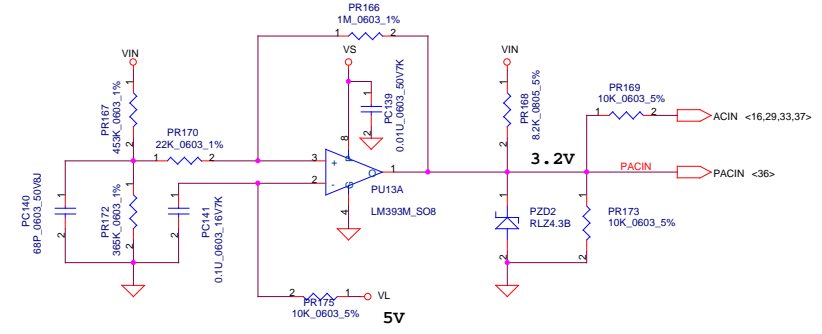
Compal Electronics, Inc.		
Title DC/DC Circuits		
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Detector

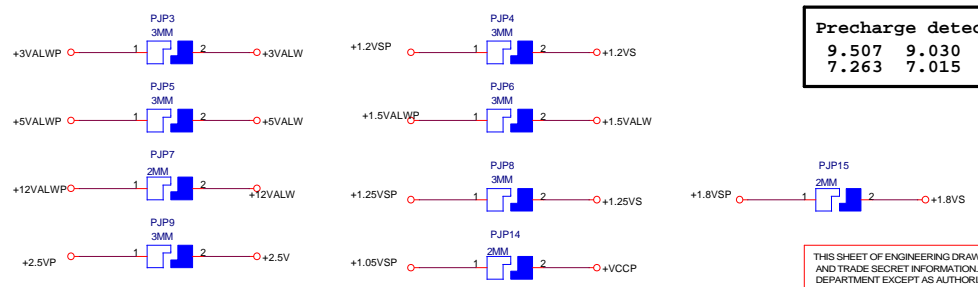


VIN detector		
14.229	13.717	13.217
12.520	12.110	11.566



ACIN		
Precharge detector		
12.432	11.717	11.061
10.188	9.702	9.051

BAT ONLY		
Precharge detector		
9.507	9.030	8.589
7.263	7.015	6.579

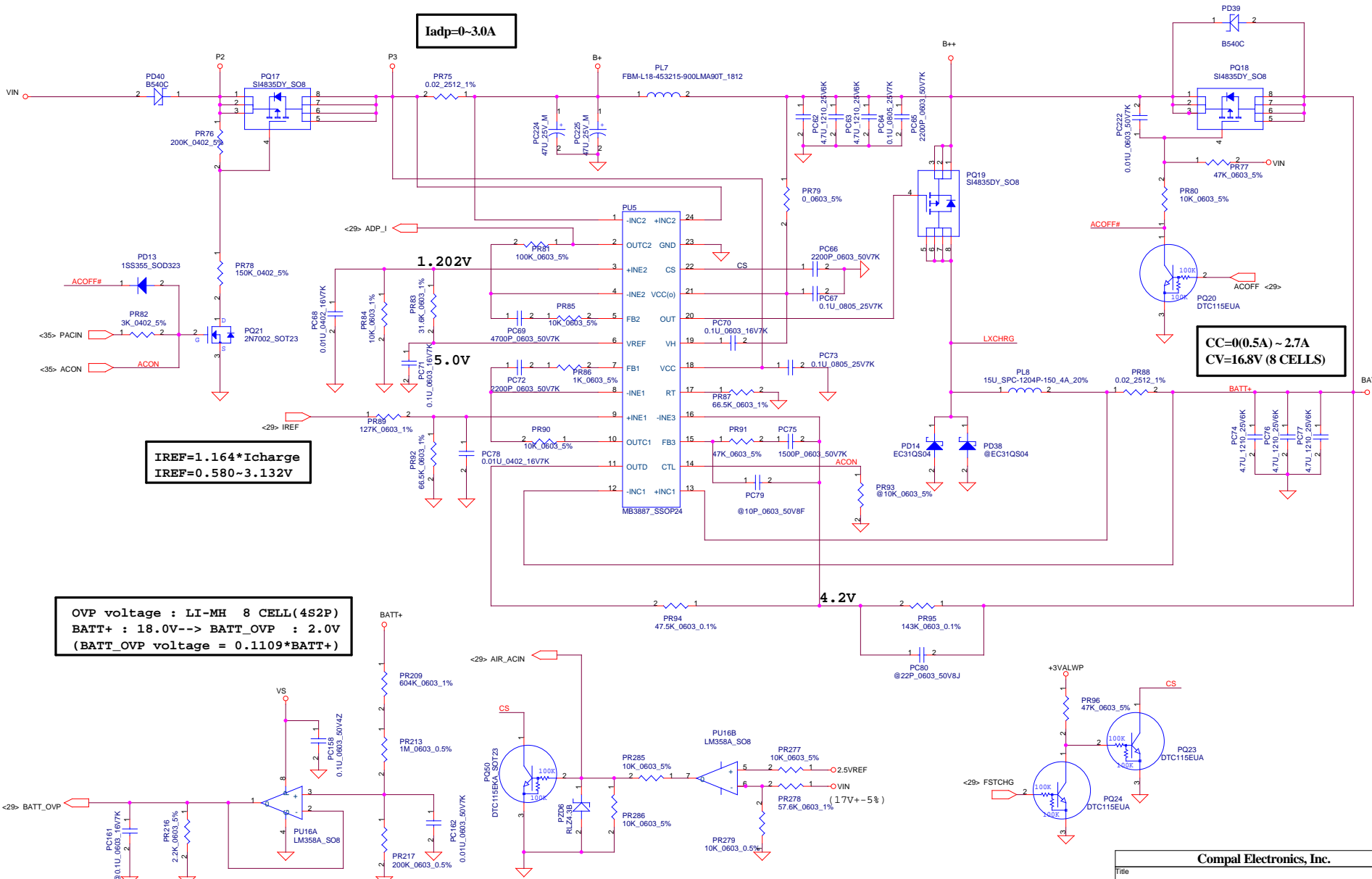


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Charger

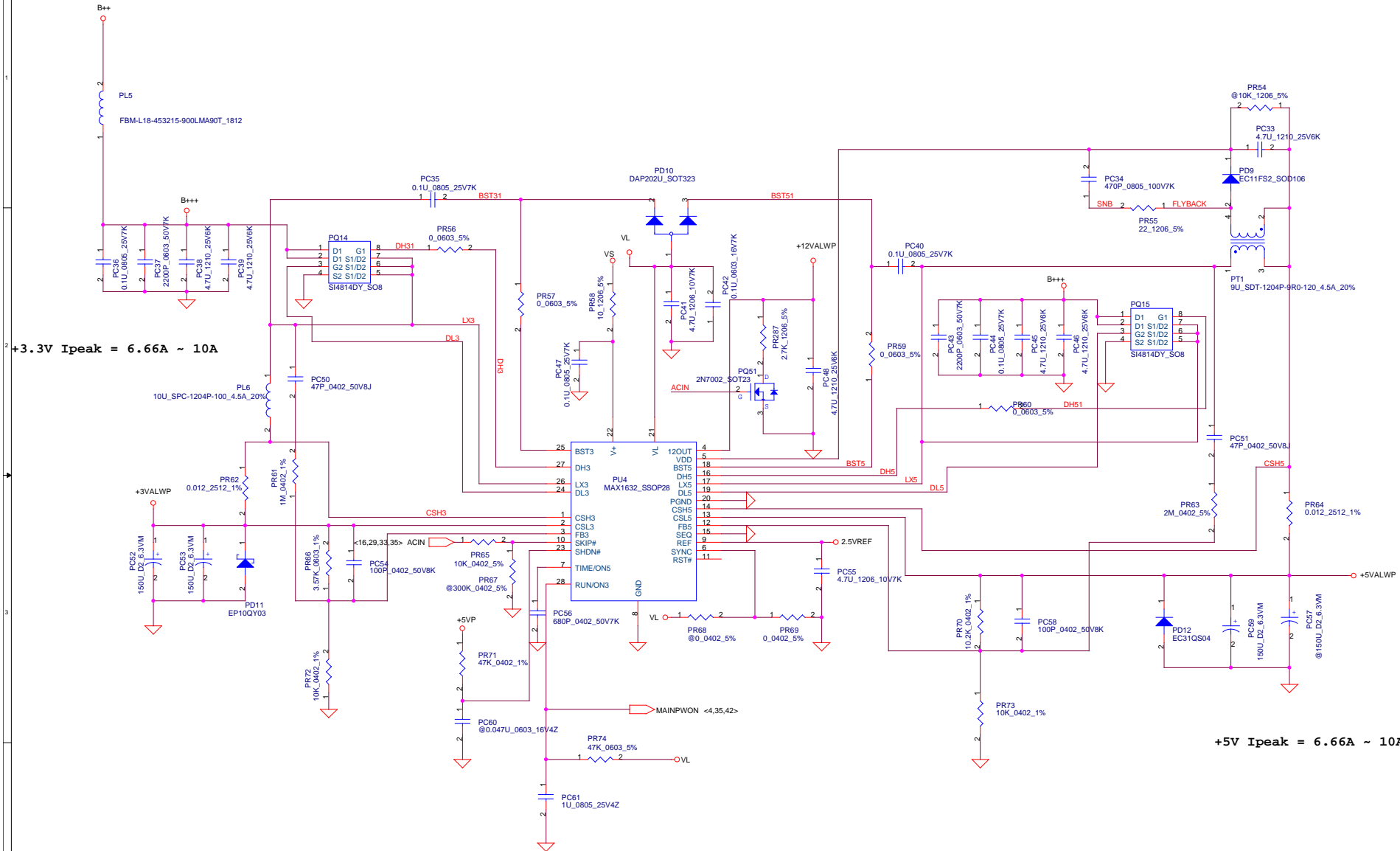
Iadp=0~3.0A



$I_{REF} = 1.164 * I_{charge}$
 $I_{REF} = 0.580 \sim 3.132V$

CC=0(0.5A) ~ 2.7A
 CV=16.8V (8 CELLS)

OVP voltage : LI-MH 8 CELL(4S2P)
 BATT+ : 18.0V--> BATT_OVP : 2.0V
 (BATT_OVP voltage = 0.1109*BATT+)



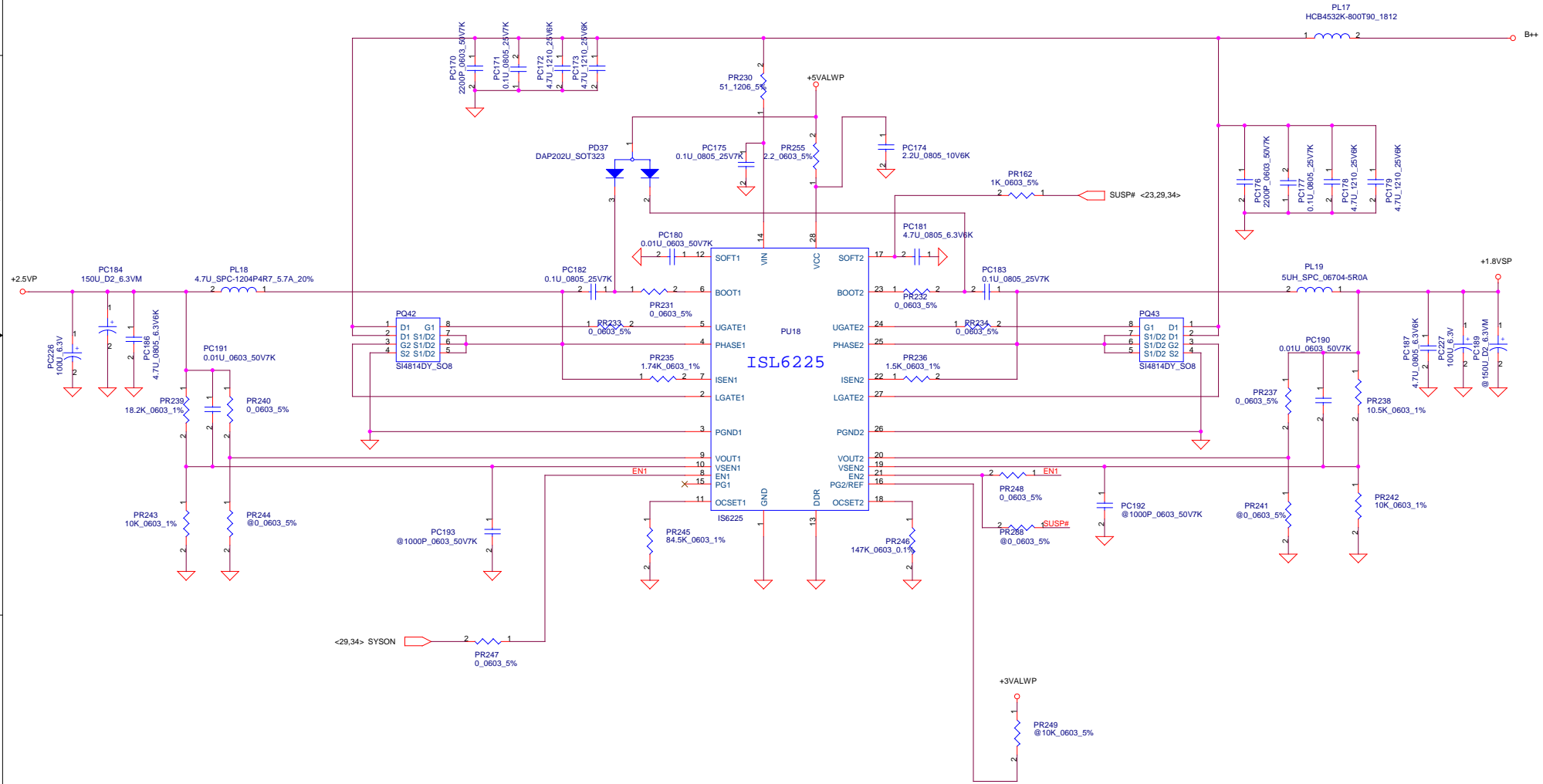
+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

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Title		3.3V / 5V / 12V	
Size	B	Document Number	LA-1701
Rev	0.1	Date	Wednesday, July 09, 2003
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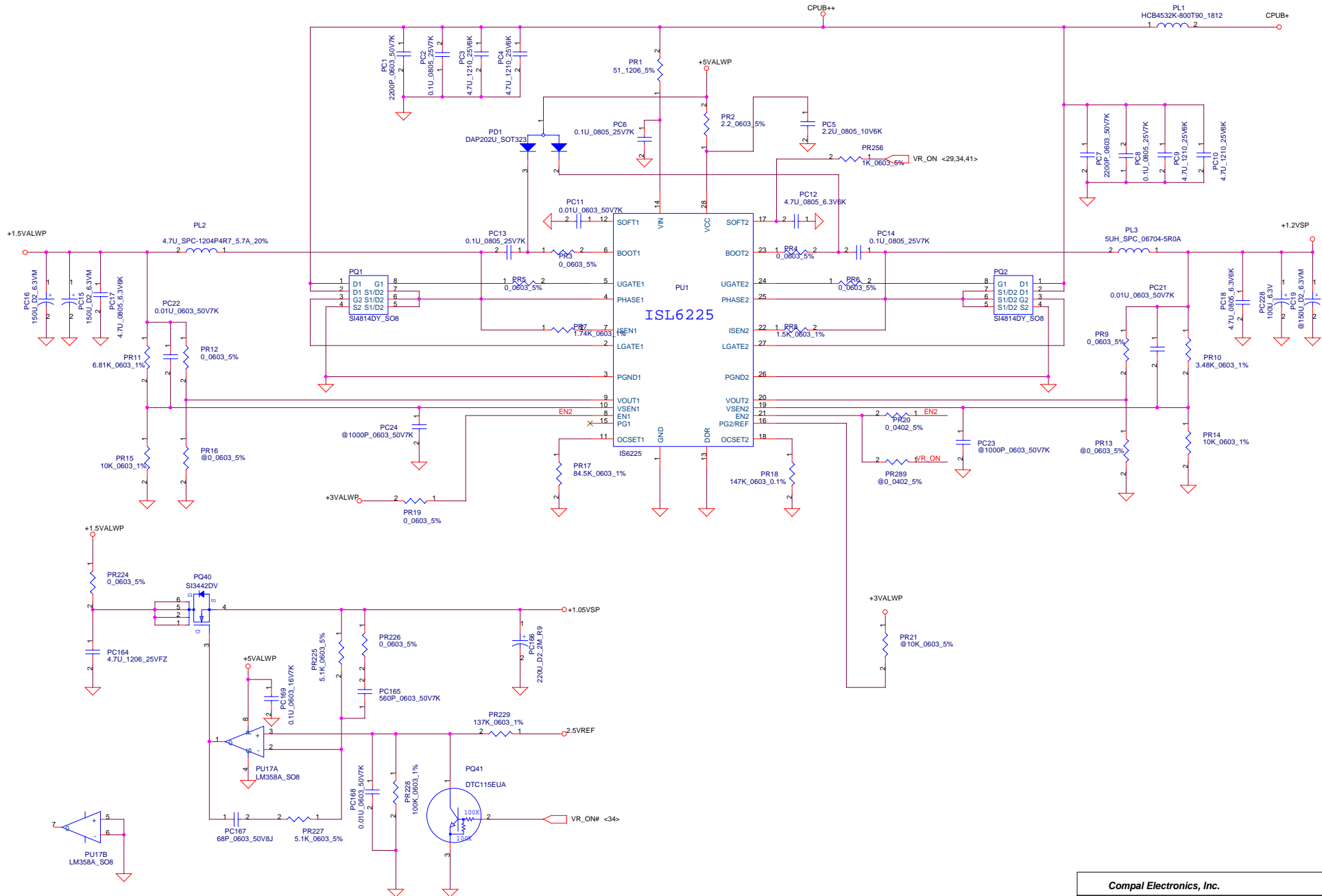
+2.5VP/+1.8VSP



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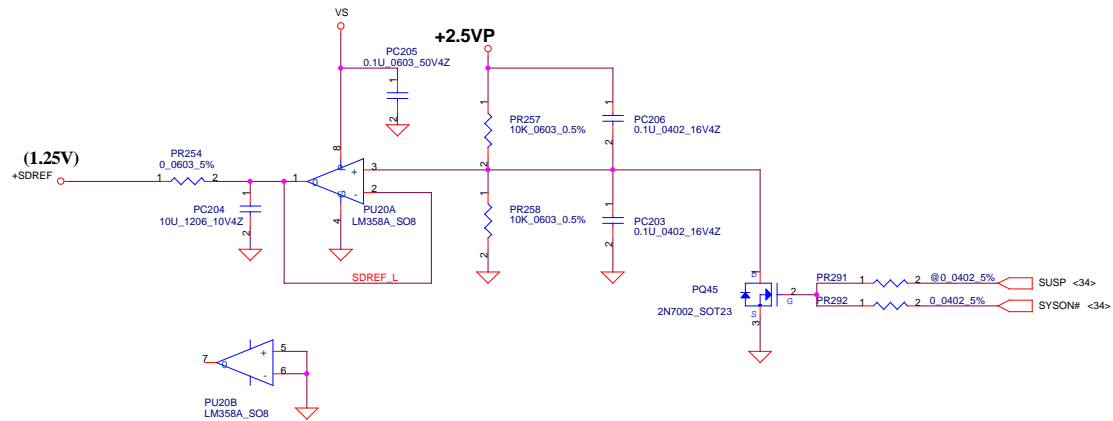
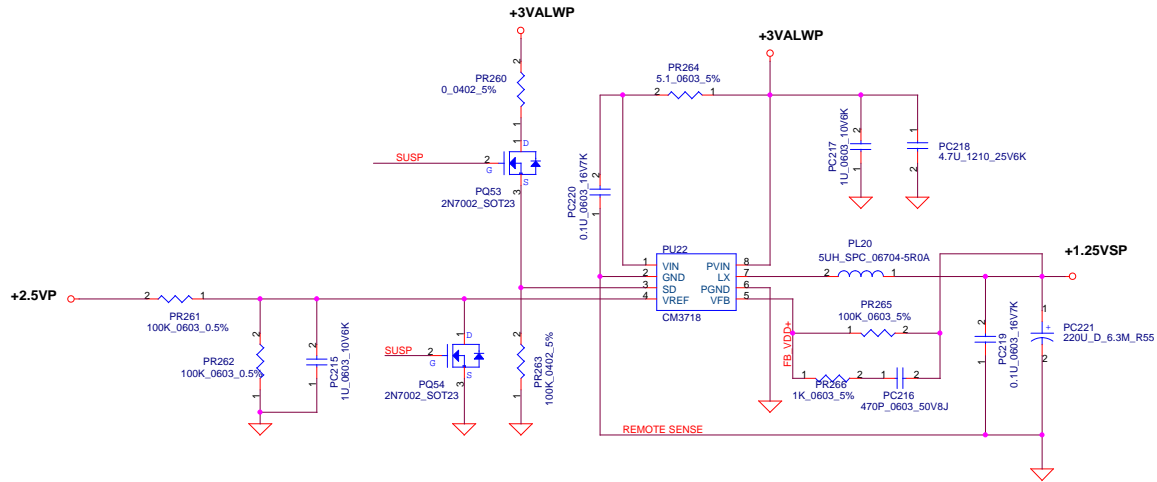
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Title	DDR POWER 2.5V / 1.8V	
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+1.2VSP/+1.5VALWP/1.05VSP



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Title	1.2V / 1.5V / 1.05V	
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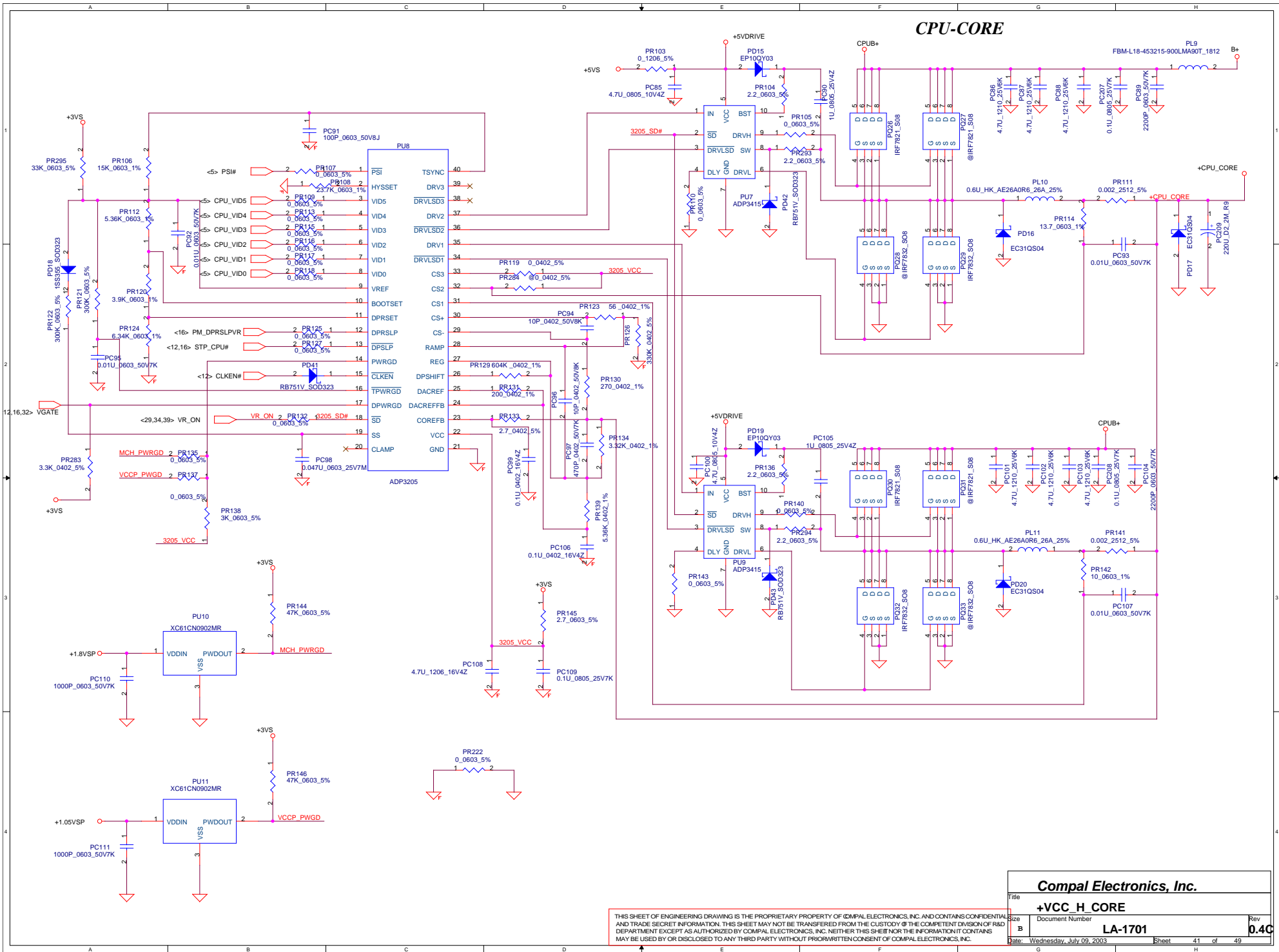
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CPU-CORE



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Title: +VCC_H_CORE

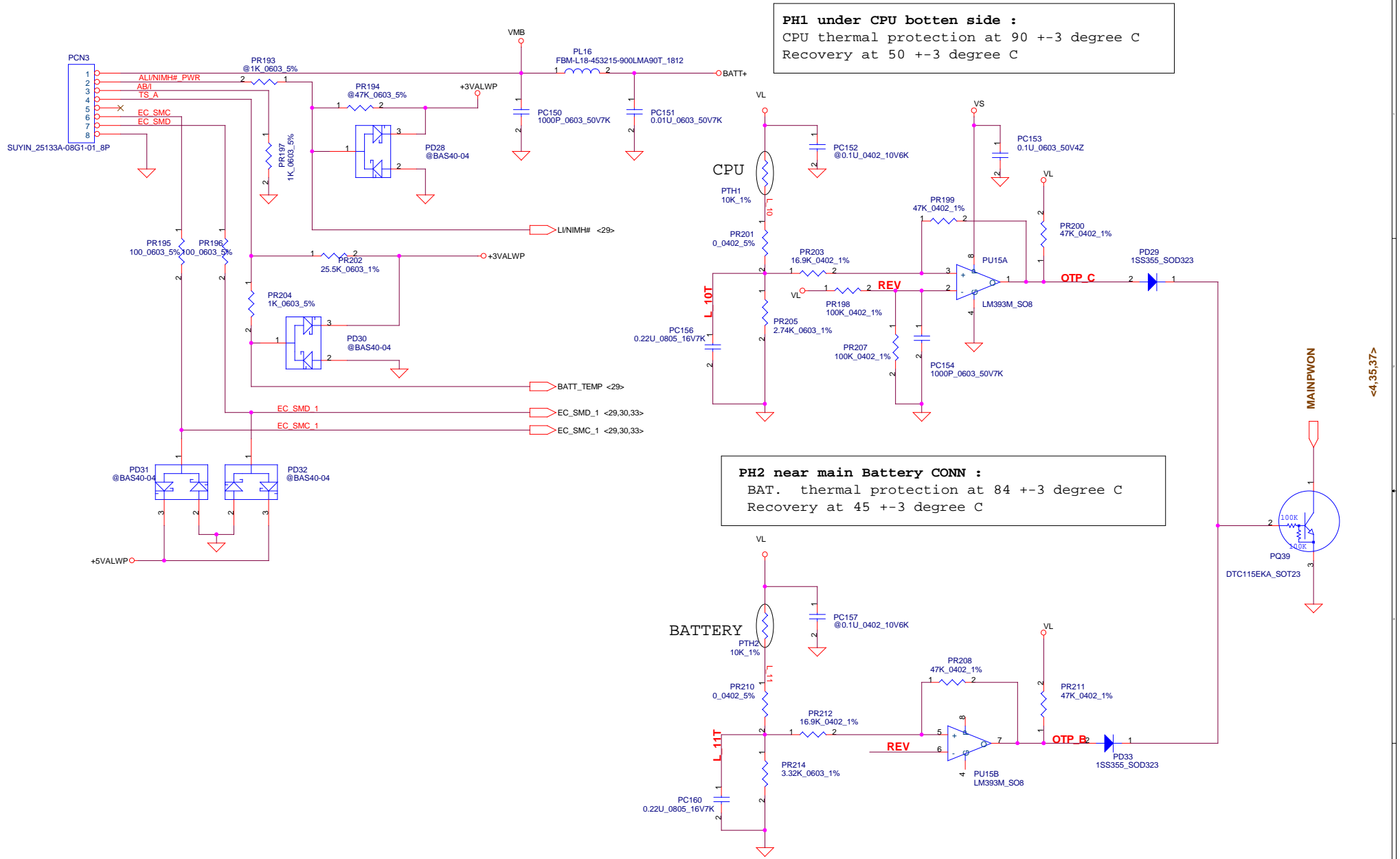
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Title		
BATTERY CONN / OTP/1.8V		
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REV: 0.1A

1. Update PCI resource table. (Page 3)
2. Change U41 power source form +12VS to +5VS for correcting error. (Page 4)
3. Remove DVI signals. (Page 13)
4. Add Video board ID and Mother board ID for HP requirement. (Page 16)
5. Change LAN controller from RTL8100BL to RTL8139CL+ for HP requirement. (Page 19)
6. Change audio CODEC from ALC202A to AD1981B and modify relational components for HP requirement. (Page 23,24)
7. Change USB power protector from Poly switch to RT9701-CBL for meet HP's specification. (Page 27)
8. Add CP9, CP10 (100P_1206_8P4C) for EMI requirement. (Page 28)
9. Add a power button LED (D34) for HP requirement. (Page28)
9. Add a power button LED (D34) for HP requirement. (Page28)

REV: 0.1B

1. U33,U34,U56 combine to U33 (74HCT08 TSSOP14).(Page 18)
2. Add Q81,C892,C891 for +3VAUX turn on/off.(Page 25)
3. Add R91,R1132,C893 for correcting error. (Page 26)
4. U12 pin9,10 contact to GND. (Page 30)
5. Change U47D,U47E,U47F to U14A,U14B,U14C. (Page 32)
6. Add L57,C894,C895,C896,C897 for HPQ request to add SPR GNDA.
7. Add U57 and relation components for AD1981B's AVDD power source. (Page 23)
8. Change U23 and relation components to reserve. (Page 23)
9. Add R1137, 0_1206_5% resistor for optional AMP. power source of +5VS. (Page 24)
10. Add L58~L61 on AMP.(U53) output trace. (Page 24)
11. Delete TVS41~TVS44 and change C863~C866 to 47PF. (Page 24)
12. Modify JP8's pin define for using switched jacks on the headphone audio. (Page 28)
13. Change audio amplifier from TPA0202 to TPA0312. (Page 24)
14. Connecting the pin97 of JP28 and JP29 to GND for HP's requirement. (Page9,10)
15. Install a 0 ohm (R703) between ITP_DBRESET# and SYSRST# then de-populate U51,R704 and C833. (Page 16)
16. Modify USB routing method for HP's requirement. (Page 16)
 - i. USB0 and USB 1 (U45.C20/D20, U45.A21/B21) to the two ganged system USB ports.
 - ii. USB2 and USB3 (U45.C18/D18, U45.A19/B19) to the docking connector.
 - iii. USB4 (U45.C16/D16) to single USB.
 - iv. USB5 (U45.A17/B17) to MDC.
17. Delete net MBAY_DISABLE from JP1 pin A49 for HP's requirement. (Page 29,33)
18. Change powerm source of D10,D11 and D12 from CRTVDD to +3VS for HP's requirement. (Page 14)
19. Add an IO buffer (U56) for supporting EVO600's keyboard. (Page 30)

REV: 0.1C

1. Re-location all parts.

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REV: 0.1D

1. Change U20 to AT24C16N and change power source to +3VALW. (Page 30)
2. Change U49 EC_SMC_1/EC_SMD_1 to EC_SMC_2/EC_SMD_2. (Page 4)
3. Change Battery EC_SMC_2/EC_SMD_2 to EC_SMC_1/EC_SMD_2. (Page 42)
4. Modify SD controller to M/B. (Page 31)

REV: 0.2A (For DB-1 SMT)

1. For solving FAN can't work properly issue. (Page 4)
 - a. Change U14's power plan from +5VS to +12VS.
 - b. Change U14 from LMV321M5X to LM321MF.
2. For solving system boot fail issue. (Page 12)
 - a. Del Q29.
 - b. Add PD41 RV751V.
3. For EMI requirement. (Page 14)
Change L1,L2,L3,L18,L19 from FBM-11-160808-121 to FCM1608C-121T.
4. For solving main battery only, system can't boot on issue. (Page 15,16)
 - a. Change ACIN signal connection from GPI11(U8.AA5) to GPIO27.(U8.W1)
 - b. Pull high GPI11 to +3VALW.
5. Pull high U19.8 to +5VS for solving SUSP# signal don't well issue. (Page 23)
6. Del L10,C155,C204,C477,C474 for HP requirement. (Page 23)
7. Change R363,R365 to 1K_0402_5% for solving CODEC can't be detected issue. (Page 23)
8. Add voltage divider R413,R414,R416,R419 for HP requirement. (Page 24)
9. Change AMP. gain from 6dB to 10dB for HP requirement. (Page 24)
10. Add R420 100K_0402_5% for solving headphone plug fail issue. (Page 24)
11. Change JP20.27 and JP20.28's power plan from +5VS to +5V for supporting touch pad wake up from S3 function. (Page 28)
12. Change U15.161's power plan from +RTCVCC to RTCVREF from increasing RTC battery life. (Page 29)
13. Add U29 for supporting 8Mbits BIOS. (Page 30)
14. Change D6,D7 to HSMB-C172 for HP requirement. (Page 30)
15. For supporting SD active LED function. (Page 31)
 - a. Connection JP17.13 to SDLED.
 - b. Change JP17.15's power plan from +3VS to +5VS.
16. Add JP32 for supporting BT module. (Page 31)

REV: 0.2B (For DB-2 gerber)

Add R427 20K ohm resistor for solving PC-beep is too loud issue. (Page 23)

REV: 0.2C (For DB-2 SMT)

1. Phase-in EMI solution.
 - a. Add R35,R344,R58,R142,R301,R408 10_0402_5%.
 - b. Add C42 22PF_0402_NPO.
 - c. Add C447 15PF_0402_NPO.
 - d. Add C73,C153,C319,C560 10PF_0402_NPO.

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REV: 0.2D

1. To change the mute circuitry for SI build.
 - a. Connect EAPD (pin U22.47) to JP24.2 and reserve a 0_0402_5% (R431) resistor for testing.
 - b. Install R162 (0_0402_5%) and no install R163.
 - c. Add R432 (100K_0402_5%) and Q51 (2N7002) to invert EAPD signal for amplifier and mute LED.

REV: 0.2E

1. For EMI requirement.
 - Add C204 0.1U_0402_16V4Z
2. To exchange TP and PS2 signals for EC requirement.
3. For cost down plan.
 - To exchange the capacitor of C83,C136 from 150U_D2_6.3VM to 100U_6.3V_M.

REV: 0.2F

1. For cost down plan.
 - Move audio line-out BLOCK capacitor from TP to MB. To add C565,C566 100U_6.3V_M.
2. For solving audio noise when IR active. (A2C039)
 - a. Del C206.
 - b. To change C492 from 150U_D2_6.3VM to 10U_1206_6.3V7K.
3. For EMI requirement.
 - Add R435~R440 0_0402_5%.

REV: 0.2G

1. For solving power LED signal wrong on PR/APR side.
 - a. Add R441 1K_0402_5%.
 - b. Q52 2N7002.
2. For solving power button must be pressed twice issue.
 1. Add D27 RB751V.
 2. Add R330 4.7K_0402_5%.
 3. Change R345 from 10K_0402_5% to 100K_0402_5%.
3. Per HPQ requirement to change audio component.
 - To change C174 and C201 to 0.022U_0603_25V7K.

REV: 0.2H (For SI gerber)

1. Per HPQ requirement to change audio component.
 - To change R427 from 20K_0402_5% to 39.2K_0402_1%.

REV: 0.3 (For SI SMT)

1. Per HPQ requirement to change LED color from BLUE to GREEN.
 - a. Change D5,D6,D7,D26 from HSMB-C172_BLUE_0805 to HSMG-C170_GRN_0805.
 - b. Change R9,R10,R11,R421 from 140_0402_1% to 330_0402_5%.
2. To improve RTC crystal accuracy.
 - Change C190,C203 from 12P_0402_50V8J to 15P_0402_50V8J.

REV: 0.3A (For PV Build)

1. Per HPQ requirement to add FET to shut off power to the Bluethumb module.
 - a. Add Q53 SI2301DS.
 - b. Add C568 1U_0603_10V6K.
 - c. Add C570 0.01U_0402_16V7K.
 - d. Add C571 0.1U_0402_16V7K.
 - e. Add C569 4.7U_0805_6.3V6K.
 - f. Add Q54 2N7002.
 - g. Add R442 100K_0402_5%.
 - h. Del R424.
 - i. Change Q16.2 signal source from Wireless_OFF# to Wireless_OFF.
2. For supporting WLAN and BT devices exist in the same system.
 - a. Connect Mini-PCI JP28-36 to Bluethumb JP32-7 using a series resistor of 1K_0402_5% (R72).
 - b. Connect Mini-PCI JP28-43 to Bluethumb JP32-6 using a series resistor of 1K_0402_5% (R298).

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REV: 0.3B

1. Exchange signals NUMLED# and CAPSLED# of Q31 and Q33 for solving BC022.
2. Rotate JP20 180 degree for solving PCP assembly issue.
3. Change JP18 & JP19's pin1 signal from SPKR+ and SKPL+ to SPKR+_C and SPKL+_C for solving audio noise issue.

REV: 0.4 (For PV gerber)

1. Connection LPC_DRQ#0 to U42.2 through R147 0_0402_5% for support SD controller DMA function.
2. For EMI requirement.
 - a. Add L10 0_1206_5% and exchange layout position with C204.
 - b. Add L36 FBM-L10-160808-301-T_0603 on EAPD signal and closed to audio CODEC.
 - c. Add L37 FBM-L10-160808-301-T_0603 on +3VS power line of audio CODEC.
 - d. Change R406 from 10_0402_5% to 33_0402_5%.
3. Per ME team Tony Liu request, change LED type and current limit resistor for increasing luminous intensity.
 - a. Change D5, D6, D7 and D26 from HSMG-C170 to 17-21SYGC/S530-E1/TR8.
 - b. Change R9, R421 from 330_0402_5% to 150_0402_1%.
4. Del C567 layout pad for solving DFX issue.
5. Reserve 1U_0603_10V6K (C572) pad and connection to U15.21 for supporting PC97591L/V in the further.
6. Do not install R72 and R298 (1K_0402_5%) for HP requirement.
7. For solving OTS#95452 which are HSYNC and VSYNC out of specification.
 - a. Add C573 0.1UF_0402_5%.
 - b. Add U43 SN74AHCT126PWR.
 - c. Del Q3, Q4, R263, R268, R267, R255, R254.
 - d. Change C3, C5 from 68P_0402_50V8K to 10P_0402_50V8K.
8. Base on HPQ Robert's command to do some audio's design change.
 - a. Install R433, R434 0_0603_5%
 - b. No install C565, C566 100UF_6.3V_M.
 - c. Correct the left channel input voltage divider, connect R419.1 to LINE_OUTL and R416.1 to analog GND.
 - d. Change C562 from 0.1U_0402_16V4Z to 0.1U_0603_16V7K.
 - e. Change R387 from 4.7K_0402_5% to 10K_0402_5%.
 - f. Change D24 from 1N4148 to R444 4.7K_0402_5%.
 - g. Del R416 0_0402_5%.
 - h. Add R419 0_0402_5%.
9. Change some component's value as HPQ Darrell's request.
 - a. Change C330, C334 from 0.01UF to 0.1UF.
 - b. Change R354 from 100Kohm to 330Kohm.

REV: 0.4A (For PV SMT)

1. Add C482 0.1UF_0402_16V4Z for solving OTS#96542.
2. For solving OTS#95994.
 - a. Change R428, R429 from 0_0402_5% to 4.7K_0402_5%.
 - b. Add R413, R416 4.7K_0402_5%.

REV: 0.4B

1. Add R445 511_0603_1% to limit RTC battery discharge current for meeting OSM 4.3.8 specification.

REV: 0.4C

1. Per HPQ David request to do some audio components change.
 - a. Change R428, R429 from 4.7K_0402_5% to 0_0402_5%.
 - b. No install R413, R416, R433, R434.
 - c. Install C565 and C566 100uF CV-AX.
2. Delete reserved layout pad for solving DFX issue.
Del C83, C136, R433 and R434.
3. No install R59 10K_0402_5% for solving double pull high issue.

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4. Change R406 from 33_0402_5% to FBM-11-100505-600T to solve EMI issue.
5. Del R9 and D5 for ME team request.

REV: 0.4D

1. For solving HSYNC and VSYNC waveform undershoot over specification issue.
Change L18,L19 from FCM1608C-121T to FBM-L10-160808-300LM-T.
2. Per ME (Tony Liu) request, change D6,D7,D26 from 17-21SYGC/S530-E1/TR8 to 17-21/GVC-AMPB/3T for solving lightness not enough issue.
3. Reserve R447,R448,R449 layout pad for support CB1410 B0 version chip in the further.
4. Add D29 SM05 for solving ESD test fail issue.
5. For solving "BoBo" audio noise from HLDS and TEAC ODD.
 - a. Change R214,R216 from 4.7K_0402_5% to 1.3K_0402_5%.
 - b. Change R210 from 2.7K_0402_5% to 1.1K_0402_5%.

REV: 1.0 (MP)

REV: 2.0

1. Install R72 and R298 1K_0402_5% (page 25). This is for better performance when both BT and Wireless cards co-exist in the system.
2. Connection SLP_S3# to D29 (ESD diode) on docking side..

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Version change list (P.I.R. List)

Power section

Item	Reason for change	PG#	Modify List	Date	B.Ver#
1	RTC battery doesn't need to charge	35	PR190 and PR191 change to @200	2002.10.15	
2	change reference voltage, because VL build up fast then RTCVREF	35	PR188 change to 34K, add PR259 (66.5K)	2002.10.15	
3	adapter change from 75W to 65W. So, the power limiter must to reduce with adapter	36	PR83 change to 31.6K, PR84 change to 10K	2002.10.15	
4	the current rating of the new BEAD is 9A, the old one is 8A.	37	PL5 change to FBM-L18-453215-900-LMA90T	2002.10.15	
5	modify circuit for aircraft power	36	add PD38, PD39, PD40, PQ46, PQ47, PQ48, PQ49, PQ50, PQ51, PQ52, PU21, PR267, PR268, PR269, PR270, PR271, PR272, PR273, PR274, PR275, PR276, PR277, PR278, PR279, PR280, PR281, PC210, PC211, PC212, PC213, PC214, PZD8	2002.10.23	
6	modify circuit for DDR, change CM8500 to CM3718	40	delete PD35, PD36, PQ44, PR250, PR251, PR252, PR253, PC194, PC195, PC196, PC197, PC198, PC199, PC200, PC201, PU19 add PR260, PR261, PR262, PR263, PR264, PR265, PR266, PC215, PC216, PC217, PC218, PC219, PC220, PC221, PU22	2002.10.23	
7	change VIN detector voltage and Precharge detector voltage	35	PR167 change to 60.4K, PR166 change to 604K, PR184 change to 604K, PR185 change to 301K, PR187 change to 402K	2002.10.23	
8	modify circuit for aircraft power, when use aircraft power, battery can discharge	36	delete PU21, PQ47, PQ48, PQ49, PQ51, PD40, PZD8, PQ16, PR267-PR276, PR280-PR281, PC210-PC214, PC223, PD38, PD39 add PD40, PD41, PQ50, PZD6, PR285, PR286	2002.12.04	
9	for EMI solution	36	PC62 and PC63 change to 10U_1210_25V	2002.12.04	
10	to solve noise issue	37	add PQ51(2N7002) and PR287 (2.7K_1206_5%) change PC33 to 2.2U_1210_25V	2002.12.04	
11	to prevent leakage current	40	change PR45 from DTC115EUA to 2N7002	2002.12.04	
12	modify circuit form dual phase to single phase at CPU-CORE	41	delete PQ26-PQ29, PU7, PD15, PD16, PC85-PC90, PC93, PL10, PR104, PR105, PR110, PR111 add PC223 change PR129 to 604K_0402_5%, PR134 to 3.32K_0402_1%, PR126 to 120K_0402_5%, PR141 to 0.001_2512_5%, PC107 to 0.01U_0603_25V	2002.12.04	
13	to prevent leakage current	41	change PR128 to PD41 (RB751V)	2002.12.04	
14	change CPU thermal protect to 90 degree C	42	change PR205 form 3.32K_0603_1% to 2.74K_0603_1%	2002.12.18	
15	to reduce tolerance on CPU CORE voltage feedback	41	change PR126 form 120K_0402_5% to 120K_0402_1%	2002.12.18	

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Item	Reason for change	PG#	Modify List	Date	B.Ver#
16	the component is too high (2.5mm), so change to 1206 size(1.6mm)	41	chang PC101,PC102,PC103 to 10U_25V_X5R_1206 (SE142106M00)	2002,12,30	
17	to adjust CPU CORE load line	41	change PR123 to 47_0402_1% (SD034470A00) PC96 to 22P_0402_50V (SE071220J00) PR126 to 240K_0402_5% (SD028240300) PR129 TO 1M_0402_1% (SD034100400) delete PC97	2002,12,30	
18	the component is too high (5.2mm), so change to 1210 size(2.0mm)	36	chang PC74 to 4.7U_25V_X5R_1210 (SE065475K00)	2002,12,30	
19	to reduce inrush current for 1.25V	40	change PR261,PR262 to 100K_0603_0.5% (SD019100309) PR260 to 100K_0603_5% (SD0131003T1) add PQ53,PQ54 2N7002 (SB7700200T5)	2002,12,30	
20	to reduce power consumption and inrush current	35	change PR223,PR176,PR178,PR181 to 1.5K_1206_5% (SD0111501T6)	2002,12,30	
21		35	delete PR165 and PZD1	2002,12,30	
22	to speed up response time	39	change PC165 to 560P_0603_50V_X7R (SE025561K00)	2002,12,30	
23	to solve noise issue	36	add PC224,PC225 47U_25V_EC (SF04704M000)	2003,01,05	
24		40	change PC218 to 4.7U_1210_25V (SE065475K00) from 100U_6.3V (SG017101310)	2003,01,05	
25	to solve noise issue (A2C021)	41	add PQ26,PQ29,PU7,PD15,PD16,PC85-PC90,PC93,PC97 PL10,PR104,PR105,PR110,PR111,PR114,PC230,PC231 delete PC223 change PR129 to 604K_0402_5%, PR134 to 3.32K_0402_1%, PR126 to 330K_0402_5%, PR123 to 56_0402_1%, PC96 to 10P_0402_50V	2003,01,23	
26	to reduce negative voltage at High-side GATE for ADP3415 (A2C014,A2C098)	41	add PD42,PD43 change PR105 and PR140 to 2.2_0603_5%	2003,01,23	
27	to limit RTC battery discharge current for meeting OSM 4.3.8 specification.	35	change PR290 from 200_0805_5% to 511_0603_1%	2003,05,02	
28	adjust ripple voltage and ripple current when charger battery	36	delete PC79 and PC80 change PR91 from 330K_0603_5% to 47K_0603_5%	2003,05,02	
29	to solve noise issue (OTS:97258)	37	change PC33 from 2.2U_1206 to 4.7U_1210	2003,05,02	
30	Modify battery connector layout footprint for support has lock pin type battery connector.	42		2003,05,02	
31	Modify DC-IN jack library for solving AC jack plug-in loose issue.	35		2003,05,02	

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