

Compal confidential

Schematics Document

Mobile Merom uFCPGA with Intel
Crestline_PM+ICH8-M core logic

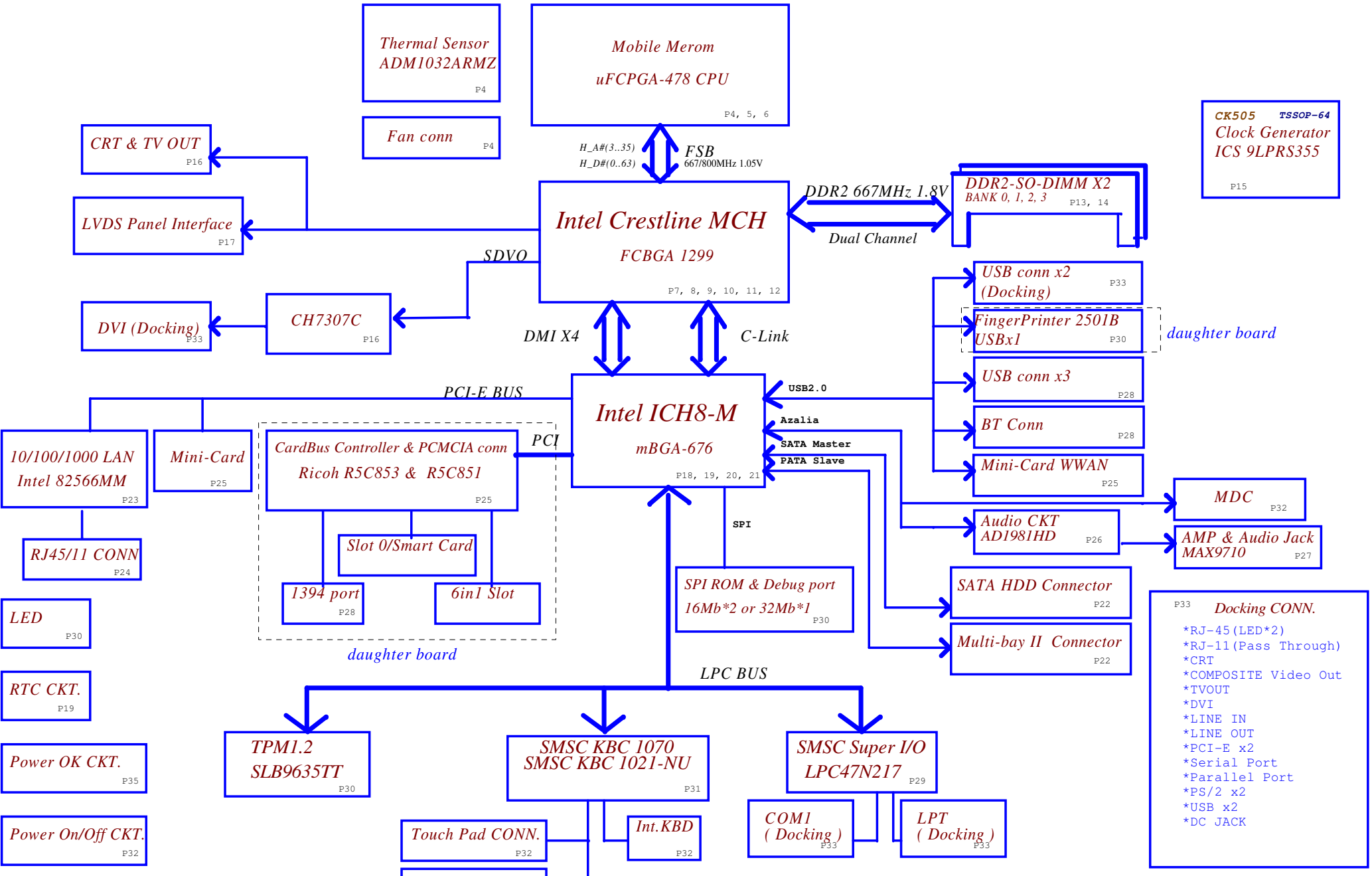
IBT00 LA-3261P UMA

2007-03-28 REV:1A (MV2)



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Chimay UMA



- P33 **Docking CONN.**
- *RJ-45 (LED*2)
 - *RJ-11 (Pass Through)
 - *CRT
 - *COMPOSITE Video Out
 - *TVOUT
 - *DVI
 - *LINE IN
 - *LINE OUT
 - *PCI-E x2
 - *Serial Port
 - *Parallel Port
 - *PS/2 x2
 - *USB x2
 - *DC JACK

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				Block Diagram	

Voltage Rails O MEANS ON X MEANS OFF

power plane / State	+B LDO3 LDO5	+5VALW +3VALW	+1.8V +5V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.25VS +VGA_CORE +CPU_CORE +VCCP	+3VM +1.05VM +1.25VM	CLOCK
S0	O	O	O	O	O	O
S3/M1	O	O	O	X	O	O
S3	O	O	O	X	O	O
S5 S4/AC	O	O	X	X	O	O
S5 S4/ Battery only	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS & 1394	AD22	2	C,D,E,G

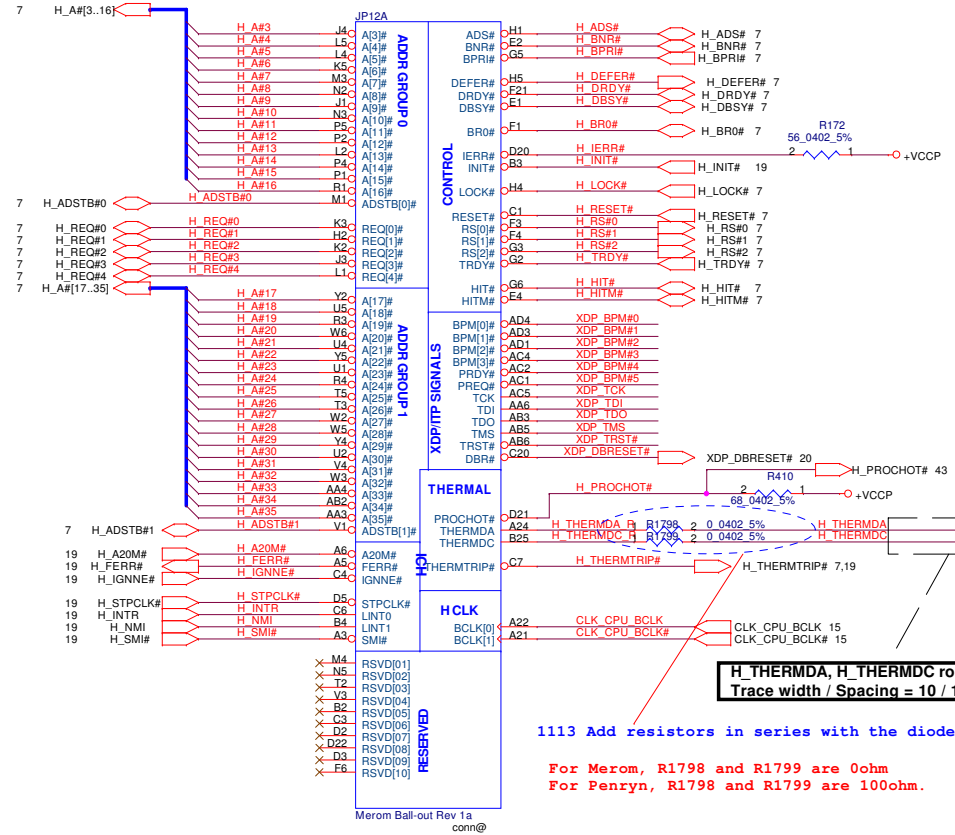
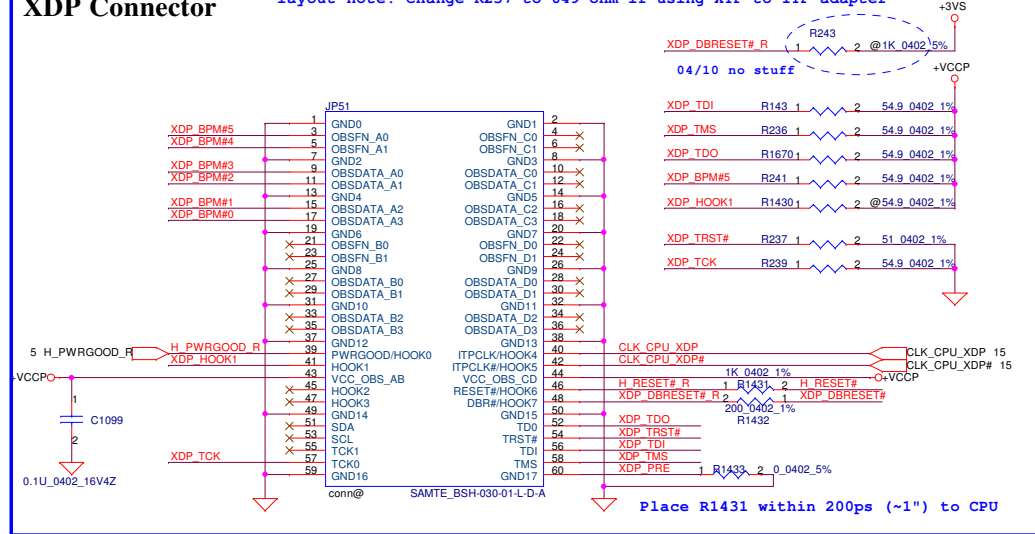
DMA Channel	Device
DMA0	MODEM / LAN
DMA1	ECP
DMA2	FLOPPY DISK
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

USB PORT#	Destination
0	Walk-up0 (Right side)
1	Fingerprint
2	Reserve
3	WWAN
4	Walk-up1 (Left Side)
5	Walk-up2 (Left Side)
6	Bluetooth
7	Reserve
8	Docking
9	Docking

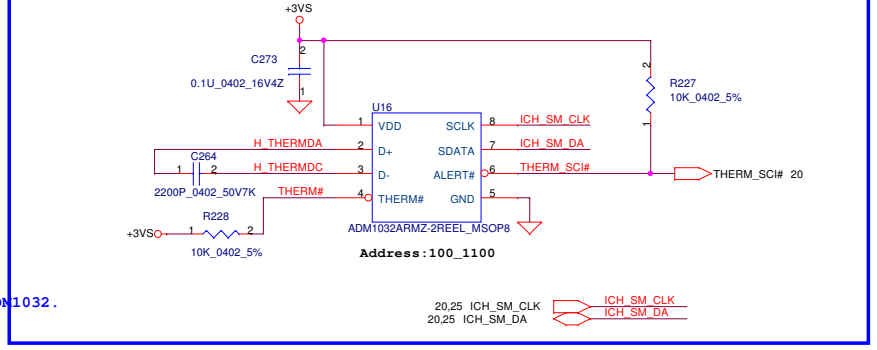
IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2), LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	Floppy
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A, Memem, LAN
11	Mass storage control/ PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface, HDD
15	Secondary IDE innterface, CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Driver for High Definition Audio Intel 82801H (ICH8 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH8 Family) PCI Express Root Port - 27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH8 Family) USB Universal Host Controll
18	Intel 82801H (ICH8 Family) USB Universal Host Controll Ricoh R5C853 Cardbus Control Ricoh R5C853 Integrates FlashMedia Control Ricoh R5C853 Gemcore based SmartCard Control
19	Intel 82801H (ICH8 Family) PCI Express Root Port - 27D6 Intel 82801H (ICH8 Family) USB Universal Host Controll
20	Intel 82801H (ICH8 Family) USB Universal Host Controll Intel 82801H (ICH8 Family) USB2 Enhanced Host Controll
21	Intel 82801H (ICH8 Family) USB Universal Host Controll
22	SDA Standard Compliant SD Host Controller
23	HP Mobile Data Protection Sensor

XDP Connector

layout note: Change R237 to 649 ohm if using XTP to ITP adapter



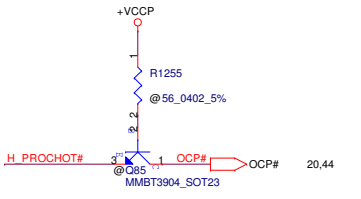
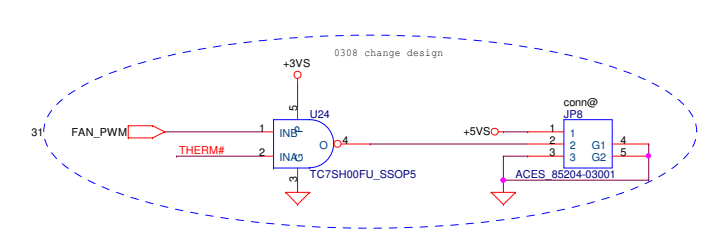
Thermal Sensor ADM1032ARMZ



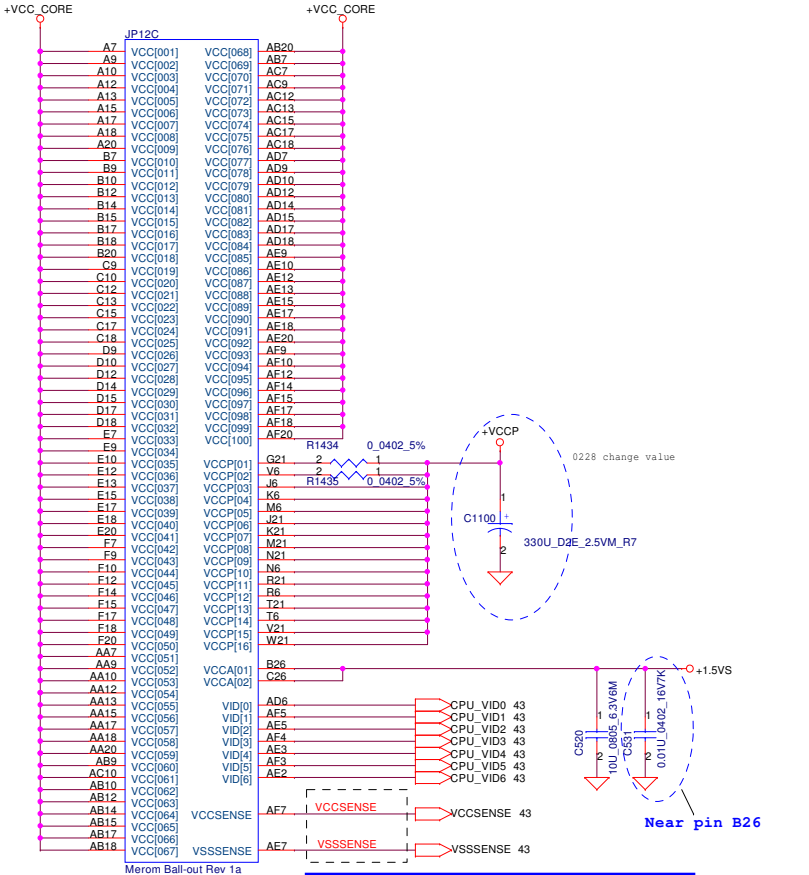
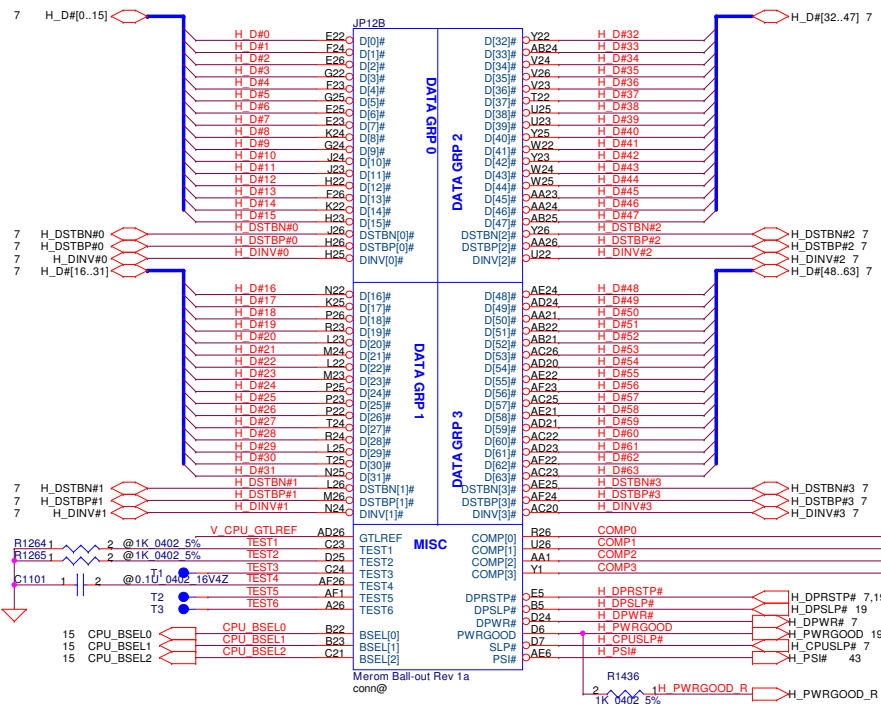
1113 Add resistors in series with the diode signals going to ADM1032.

For Merom, R1798 and R1799 are 0ohm
For Penryn, R1798 and R1799 are 100ohm.

PWM Fan Control circuit



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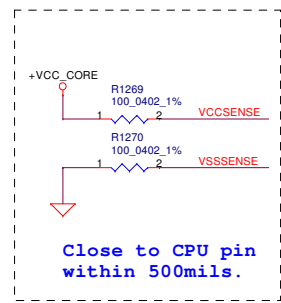
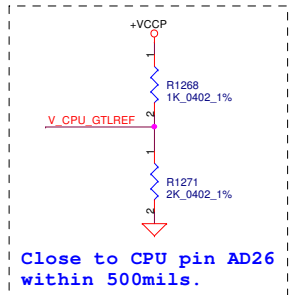


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

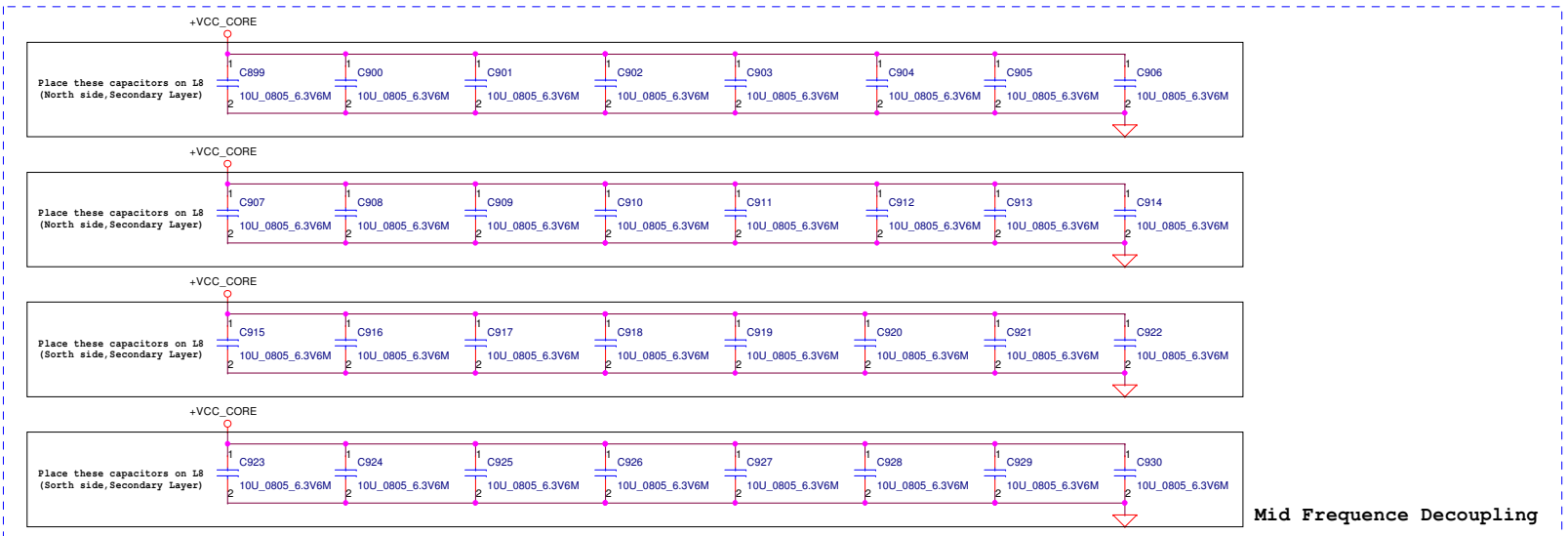
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.

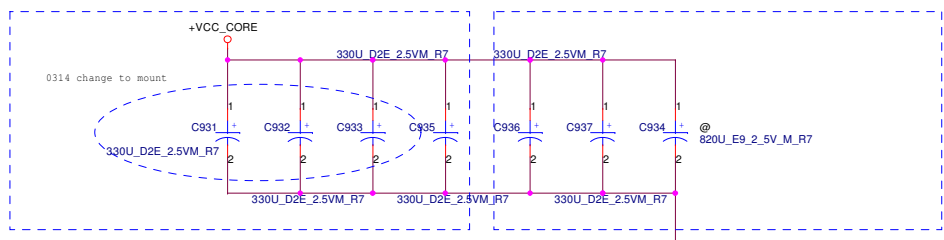


JP12D		
A4	VSS[001]	P6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R2
A16	VSS[005]	R5
A19	VSS[006]	R22
A23	VSS[007]	R25
AF2	VSS[008]	T1
B6	VSS[009]	T23
B8	VSS[010]	T26
B11	VSS[011]	U3
B12	VSS[012]	U6
B16	VSS[013]	U21
B19	VSS[014]	U24
B21	VSS[015]	U2
B24	VSS[016]	V5
C5	VSS[017]	V22
C8	VSS[018]	V25
C11	VSS[019]	W1
C14	VSS[020]	W4
C16	VSS[021]	W23
C2	VSS[022]	W26
C22	VSS[023]	Y3
C25	VSS[024]	Y6
D1	VSS[025]	Y21
D4	VSS[026]	Y24
D8	VSS[027]	AA2
D11	VSS[028]	AA5
D13	VSS[029]	AA8
D16	VSS[030]	AA11
D19	VSS[031]	AA14
D23	VSS[032]	AA16
D26	VSS[033]	AA19
E3	VSS[034]	AA22
E6	VSS[035]	AA25
E8	VSS[036]	AB1
E11	VSS[037]	AB4
E14	VSS[038]	AB8
E16	VSS[039]	AB11
E19	VSS[040]	AB13
E21	VSS[041]	AB16
E24	VSS[042]	AB19
F5	VSS[043]	AB23
F8	VSS[044]	AB26
F11	VSS[045]	AC3
F13	VSS[046]	AC6
F16	VSS[047]	AC8
F19	VSS[048]	AC11
F2	VSS[049]	AC14
F22	VSS[050]	AC16
F25	VSS[051]	AC19
G4	VSS[052]	AC21
G1	VSS[053]	AC24
G23	VSS[054]	AD2
G26	VSS[055]	AD5
H3	VSS[056]	AD8
H6	VSS[057]	AD11
H21	VSS[058]	AD13
H24	VSS[059]	AD16
J2	VSS[060]	AD19
J5	VSS[061]	AD22
J22	VSS[062]	AD25
J25	VSS[063]	AE1
K1	VSS[064]	AE4
K4	VSS[065]	AE8
K23	VSS[066]	AE11
K26	VSS[067]	AE14
L3	VSS[068]	AE16
L6	VSS[069]	AE19
L21	VSS[070]	AE23
L24	VSS[071]	AE26
M2	VSS[072]	A2
M5	VSS[073]	AF6
M22	VSS[074]	AF8
M25	VSS[075]	AF11
N1	VSS[076]	AF13
N4	VSS[077]	AF16
N23	VSS[078]	AF19
N26	VSS[079]	AF21
P3	VSS[080]	A25
	VSS[081]	AF25

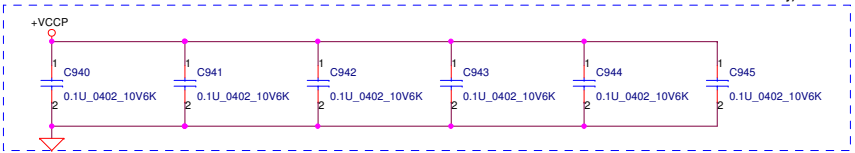
Merom Ball-out Rev 1a
conn@



Near CPU CORE regulator
ESR <= 1.5m ohm
Capacitor > 1980uF

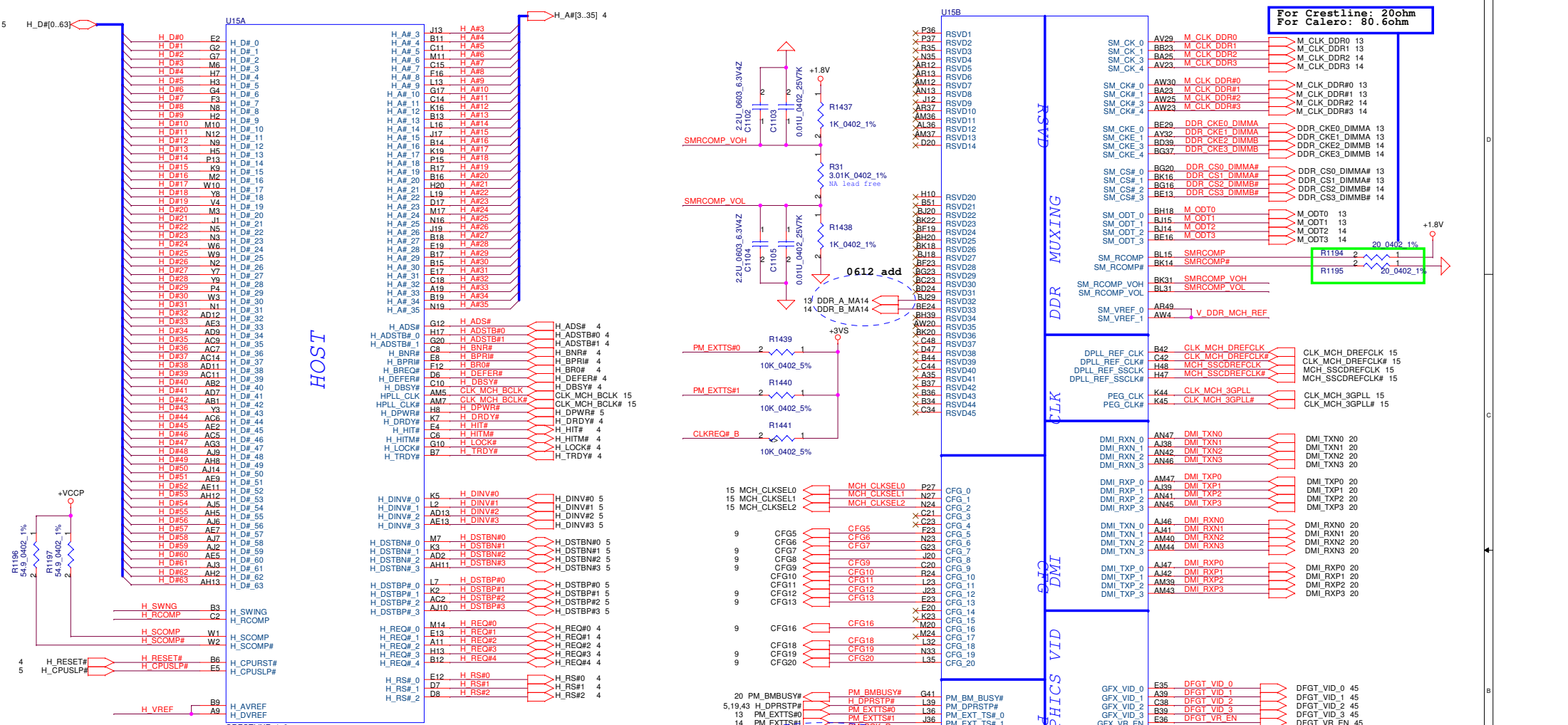


Place these inside
socket cavity on L8
(North side
Secondary)



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Merom(3/3)-GND&Bypass			
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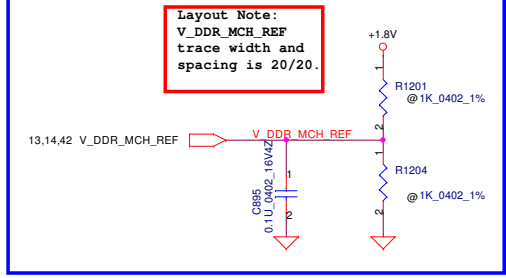
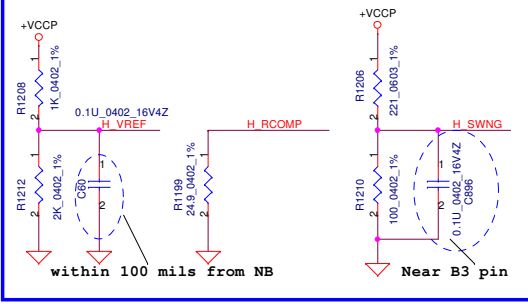
For Crestline: 20ohm
For Calero: 80.6ohm

layout note:

Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

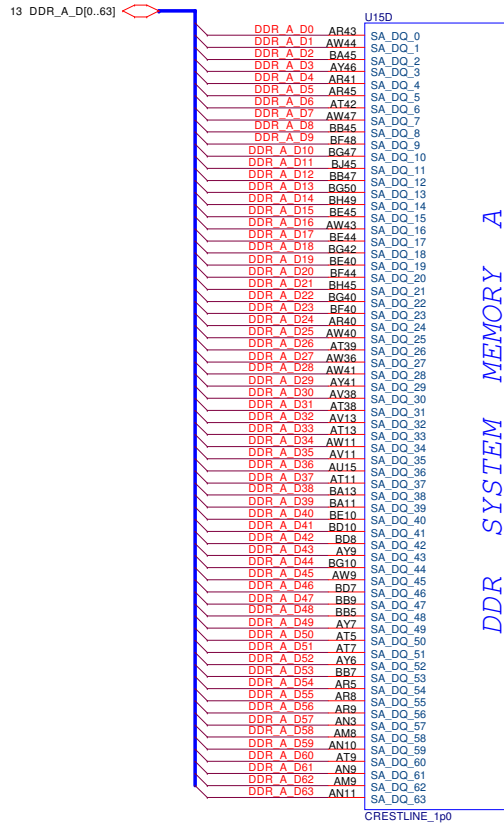
Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

Layout Note:
V_DDR_MCH_REF
trace width and
spacing is 20/20.

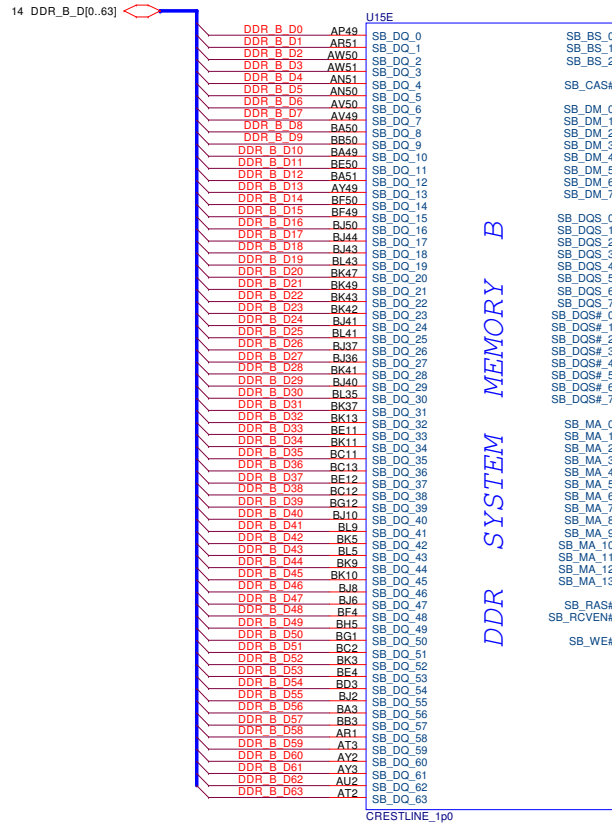
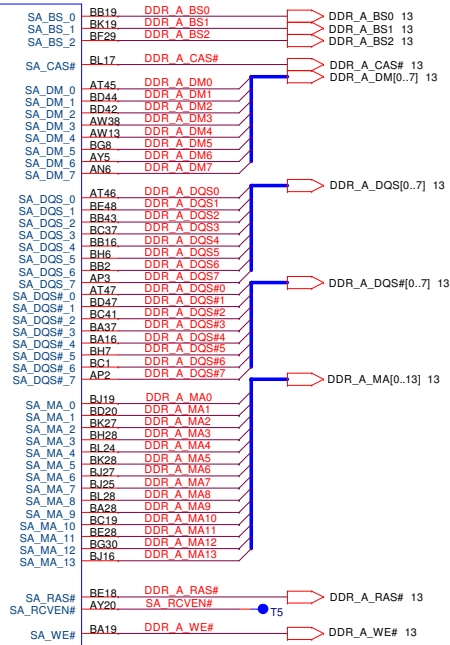


0830 Add pull-up and pull-down resistor.

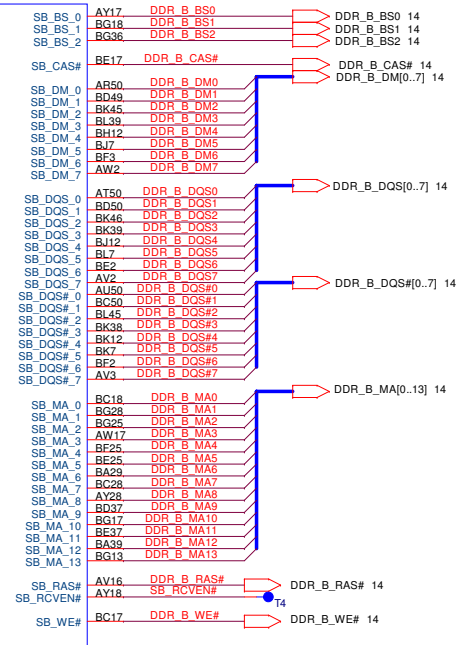
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CRESTLINE_1p0



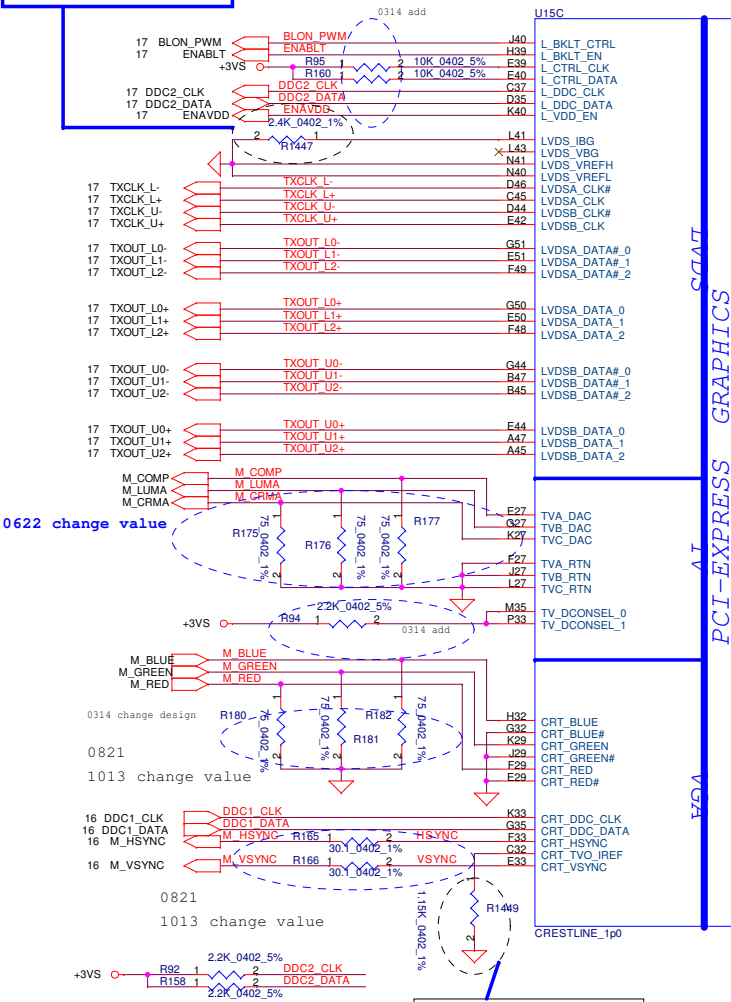
CRESTLINE_1p0



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CRESTLINE((2/6)-DDR2 A/B CH		
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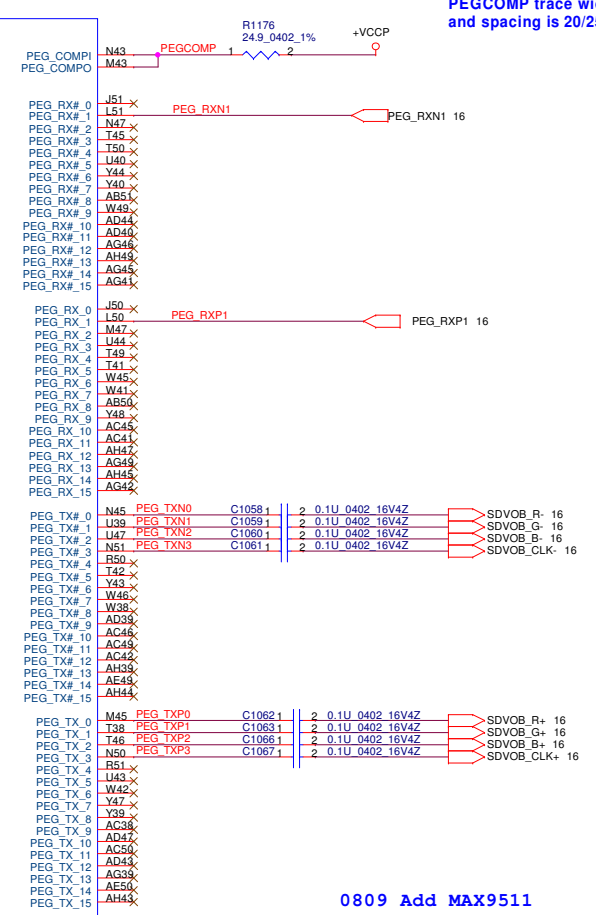
For Crestline: 2.4kOhm
For Calero: 1.5kOhm



0622 change value
0314 change design
0821
1013 change value
0821
1013 change value

For Crestline: 1.3kOhm
For Calero: 255ohm

PEGCOMP trace width and spacing is 20/25 mils.

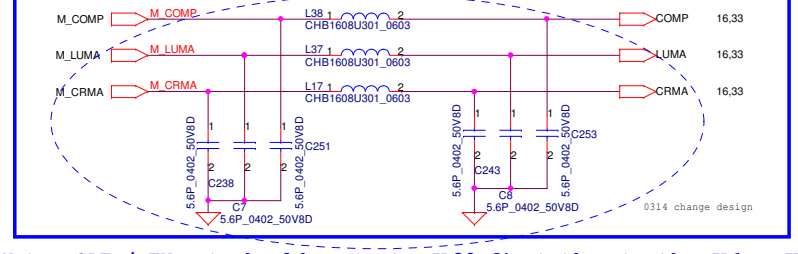


0809 Add MAX9511
1013 Remove MAX9511

Strap Pin Table

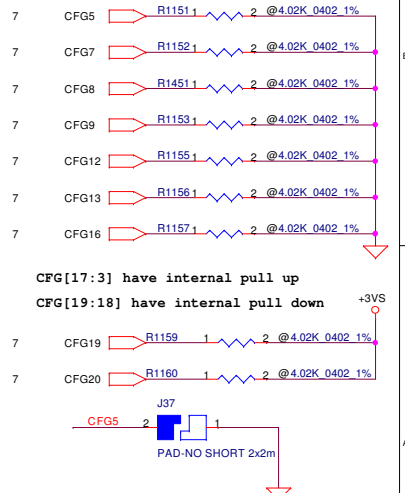
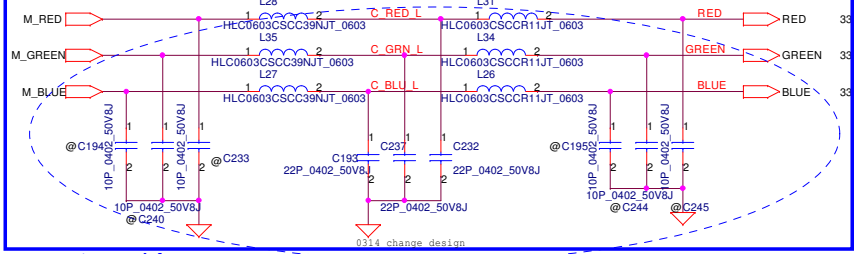
CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

TV-Out Termination/EMI Filter Place close to U15



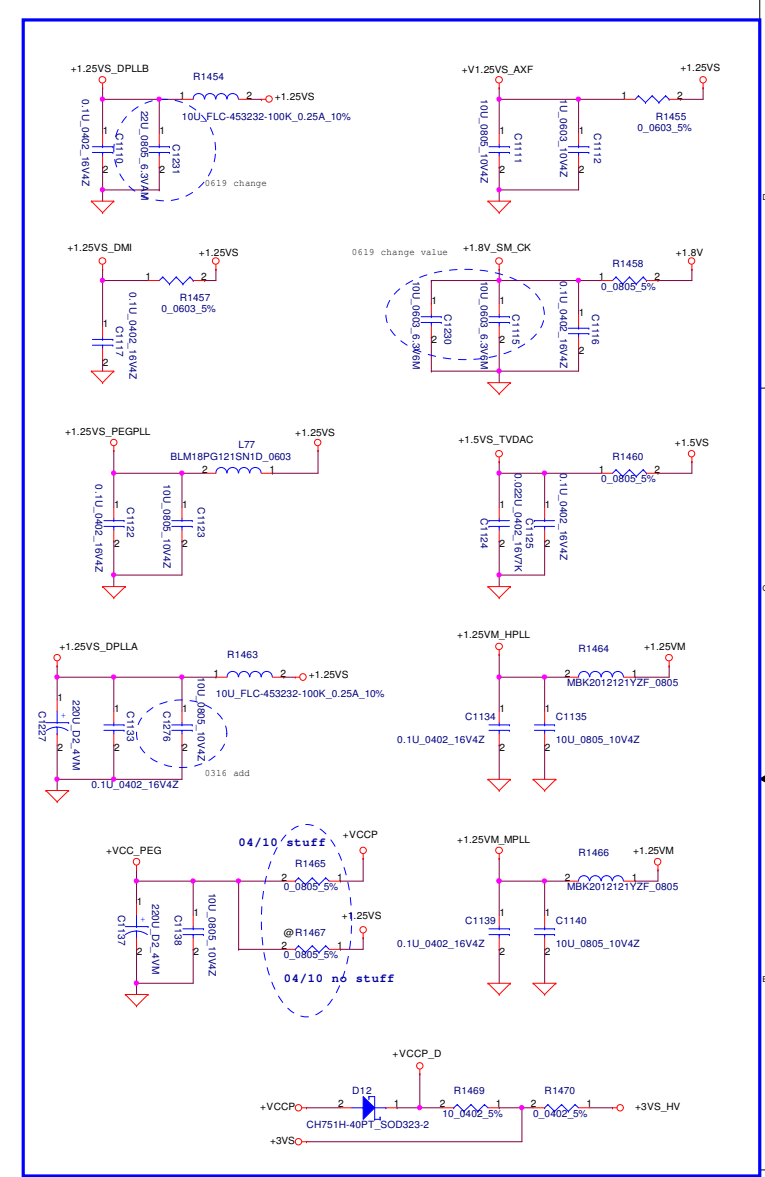
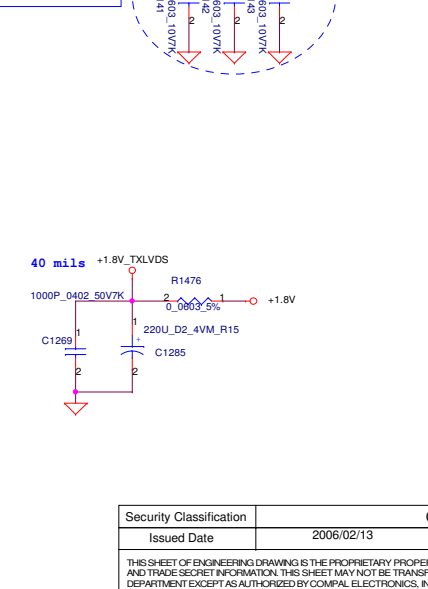
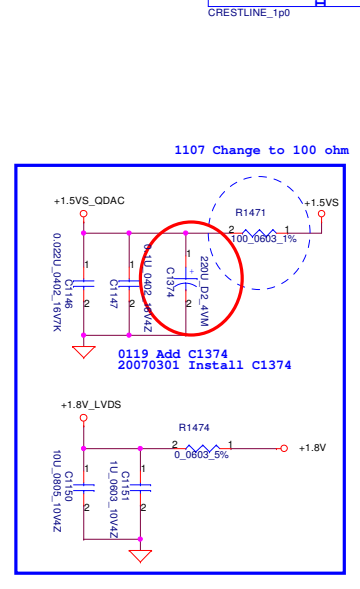
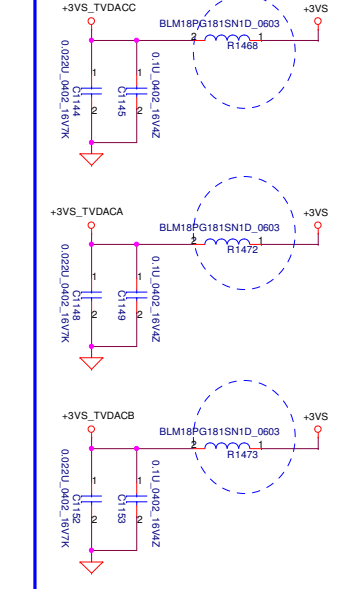
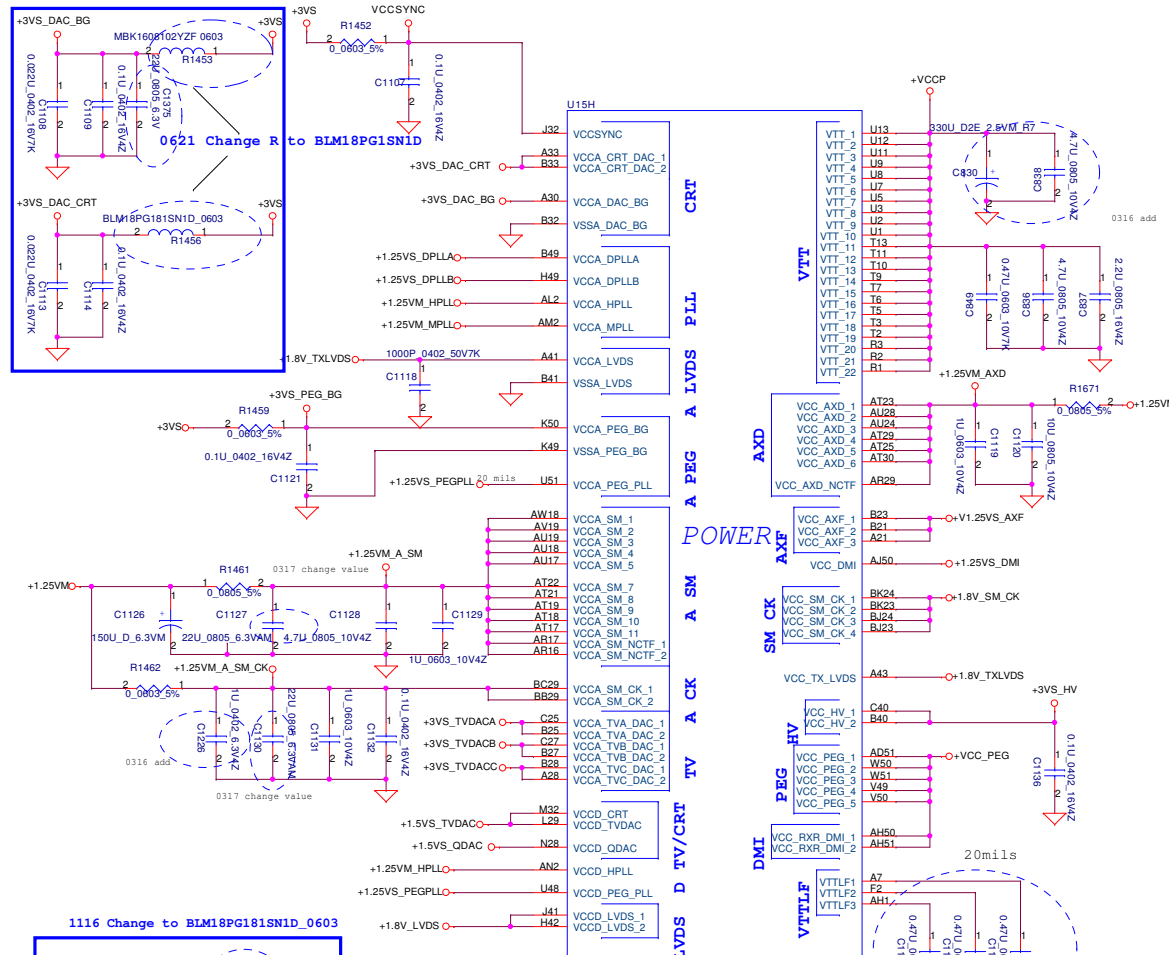
Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.

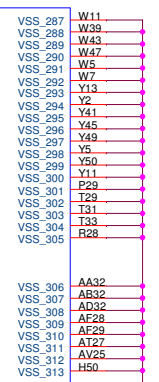
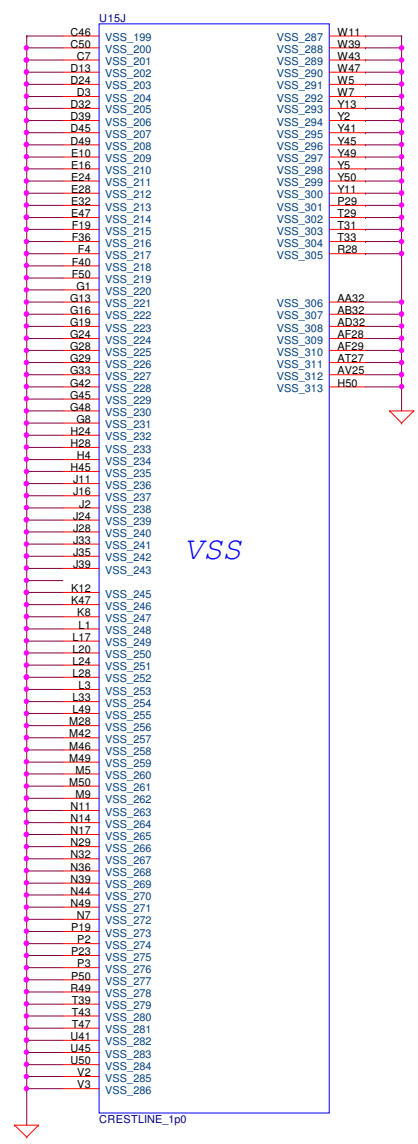
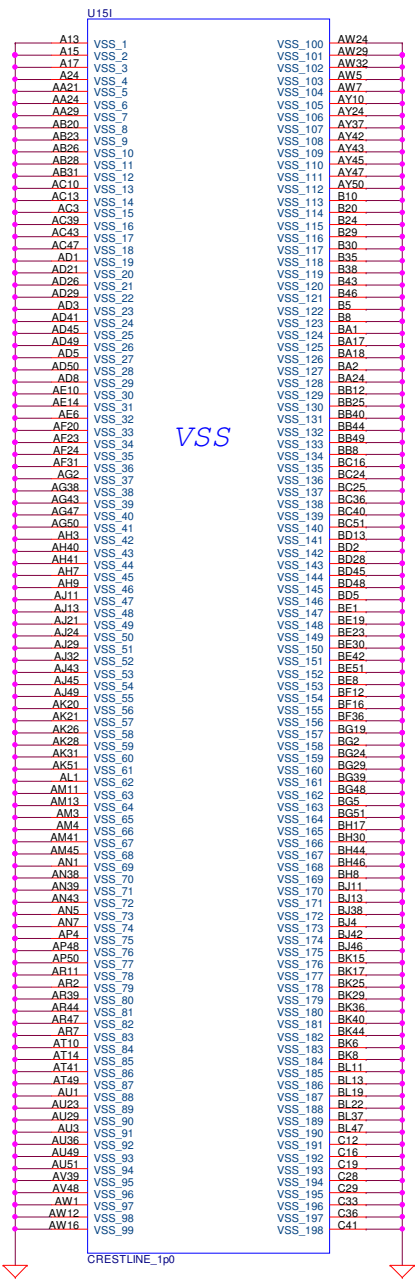
CRT Termination/EMI Filter Place Closed to U15



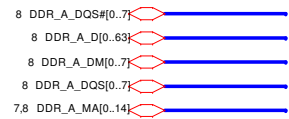
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CRESTLINE((3/6)-VGALVDS/TV		
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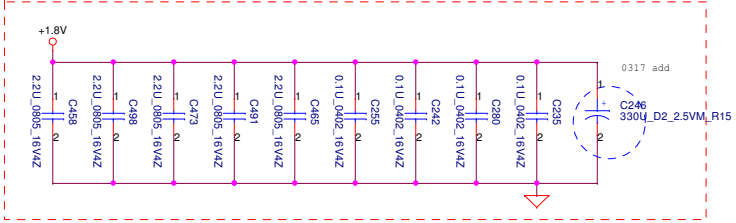




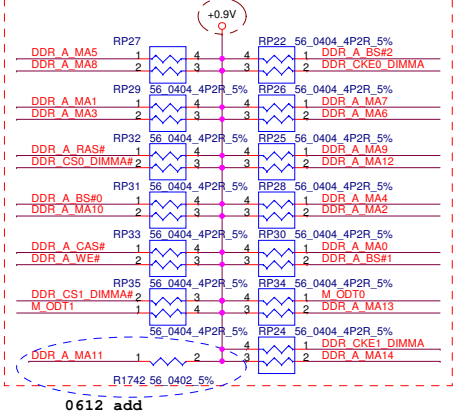
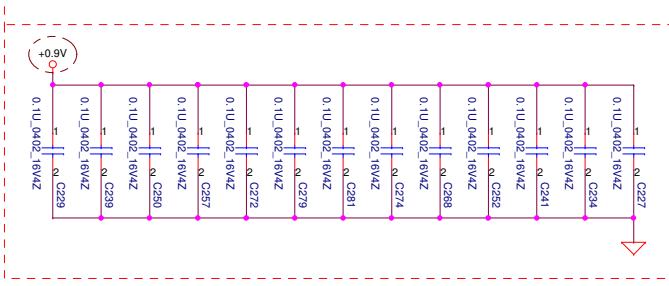
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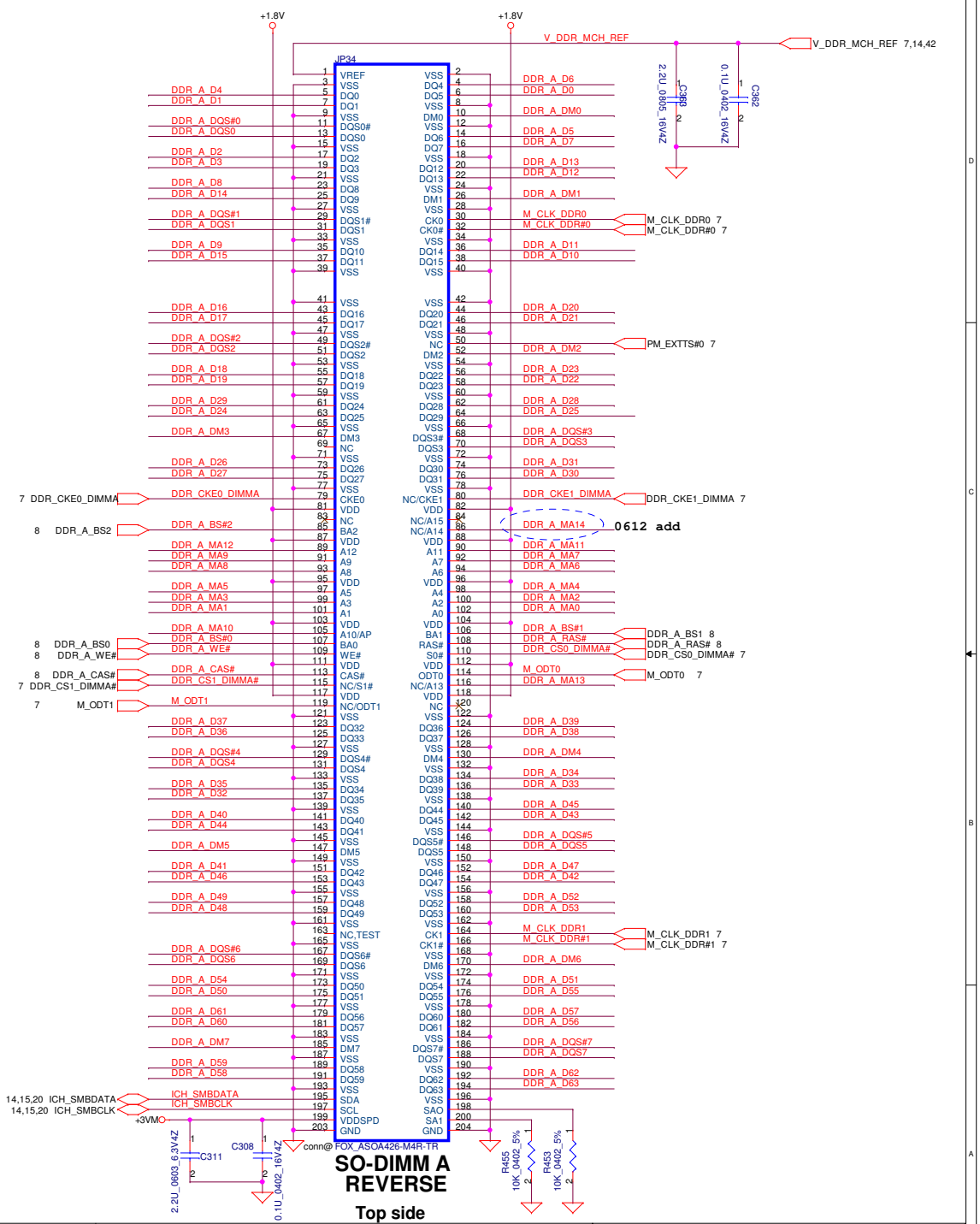
Layout Note:
Place near JP34



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



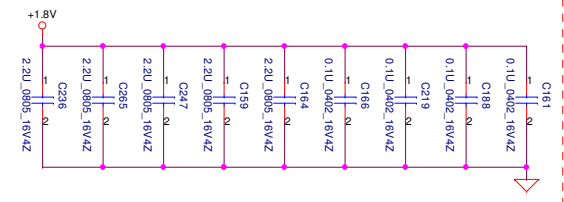
Layout Note:
Place these resistor closely JP34, all trace length Max=1.5"



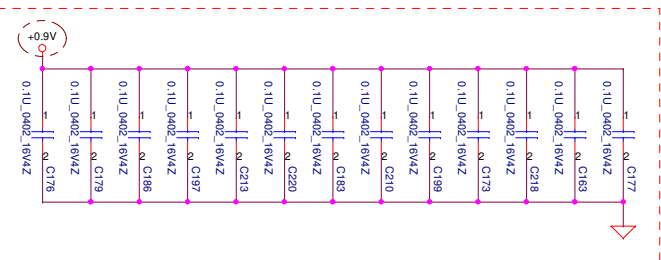
Security Classification		Compal Secret Data		Title	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Compal Electronics, Inc.	
				DDR II-SODIMM SLOT I	
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Size	Document Number	Date		Rev	
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- 8 DDR_B_DQS#(0..7)
- 8 DDR_B_D[0..63]
- 8 DDR_B_DM(0..7)
- 8 DDR_B_DOS(0..7)
- 7,8 DDR_B_MA(0..14)

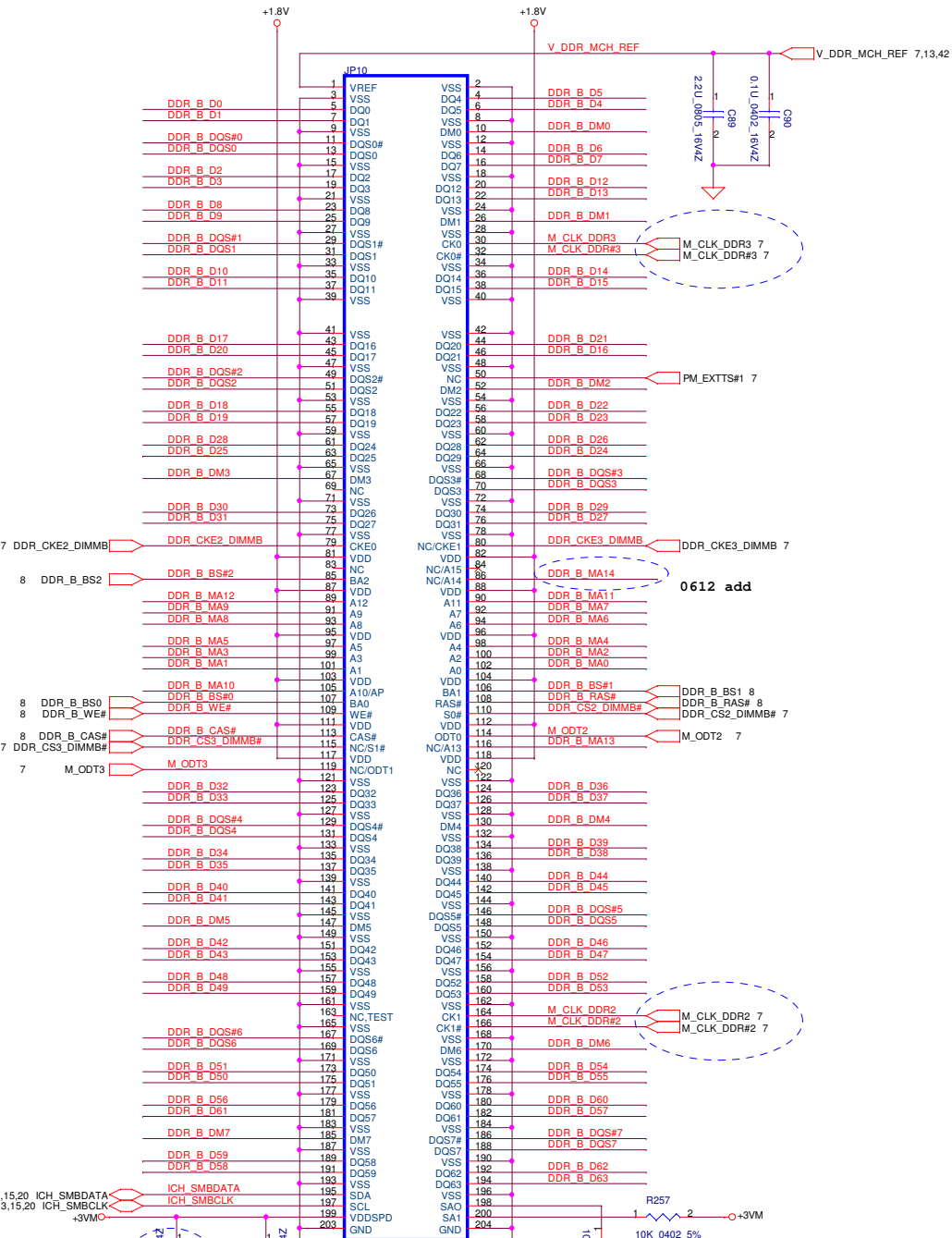
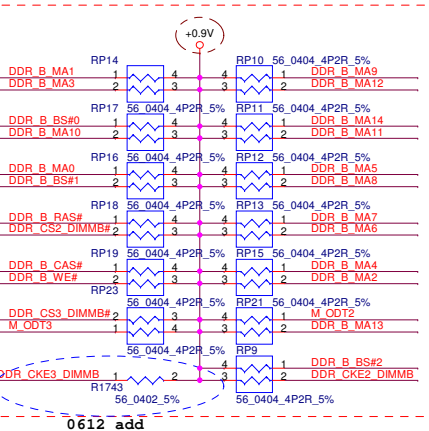
Layout Note:
Place near JP10



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



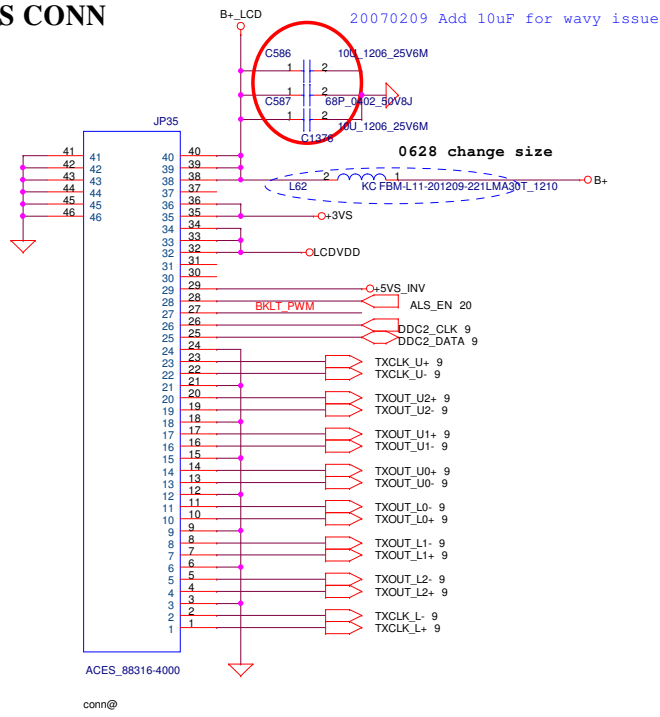
Layout Note:
Place these resistor closely JP10, all trace length Max=1.5"



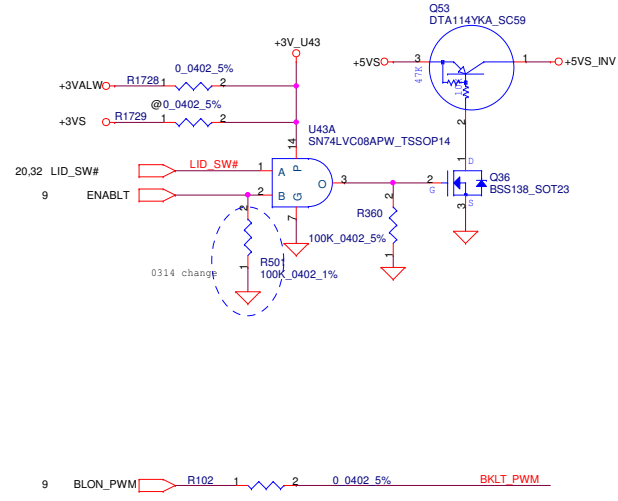
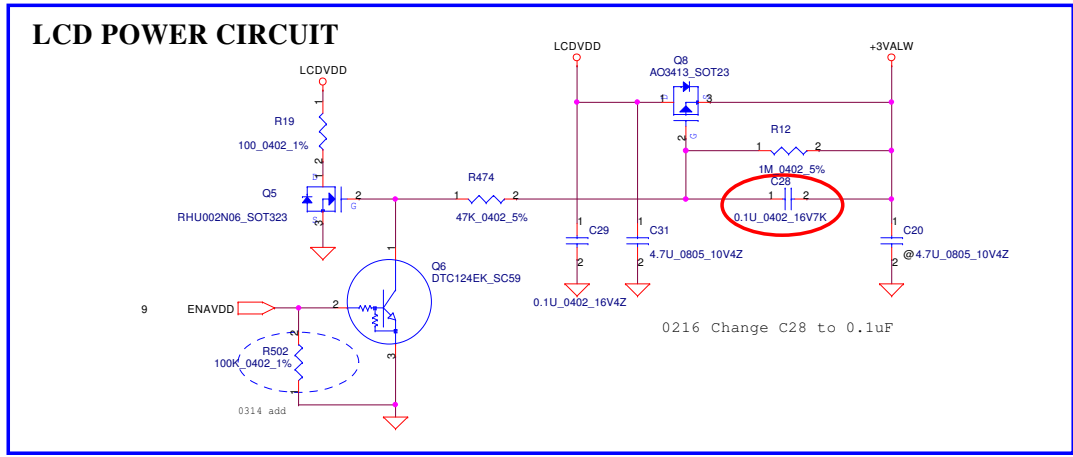
Security Classification		Compal Secret Data	
Issued Date	2006/02/13	Deciphered Date	2006/03/10
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Title			
Compal Electronics, Inc.			
DDRII-SODIMM SLOT2			
Size	Document Number	Rev	
	LA-3261P UMA	0.4	
Date:	Tuesday, March 27, 2007	Sheet	14 of 55

LVDS CONN

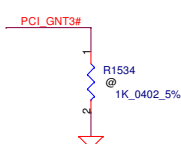
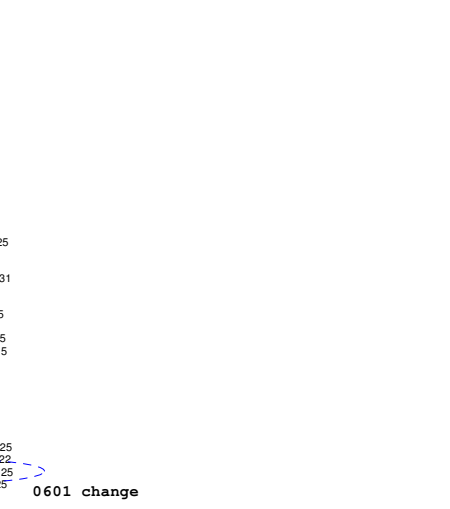
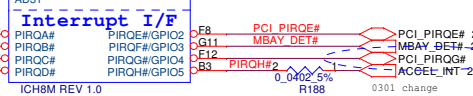
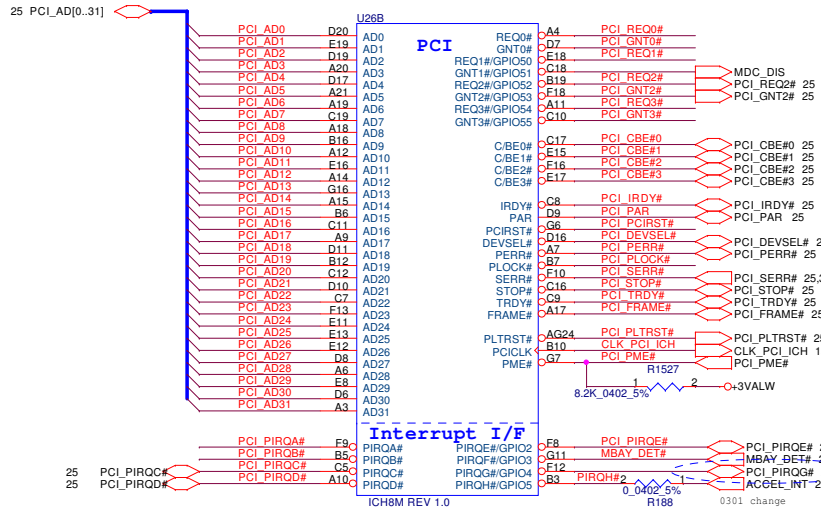
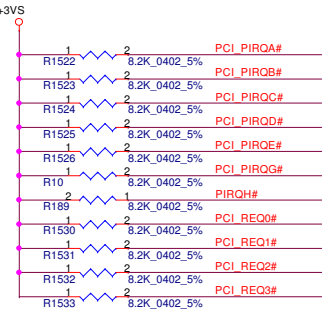
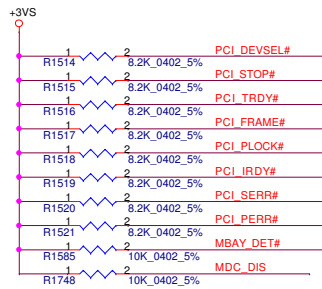


LCD POWER CIRCUIT



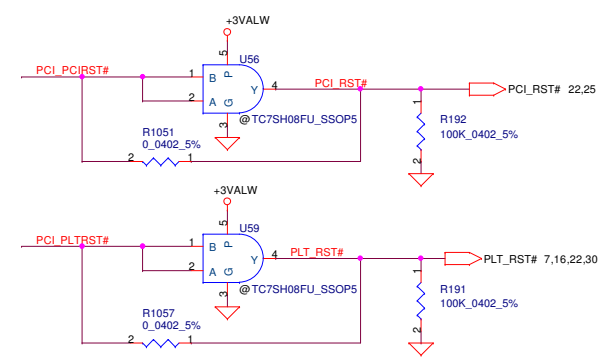
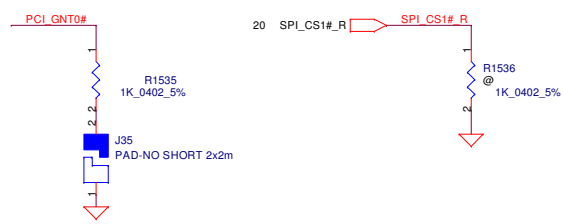
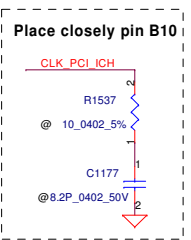
Support 3V inverter

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Issued Date	2006/02/13	Deciphered Date	2006/07/26			
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				Date:	Tuesday, March 27, 2007	Sheet 17 of 55

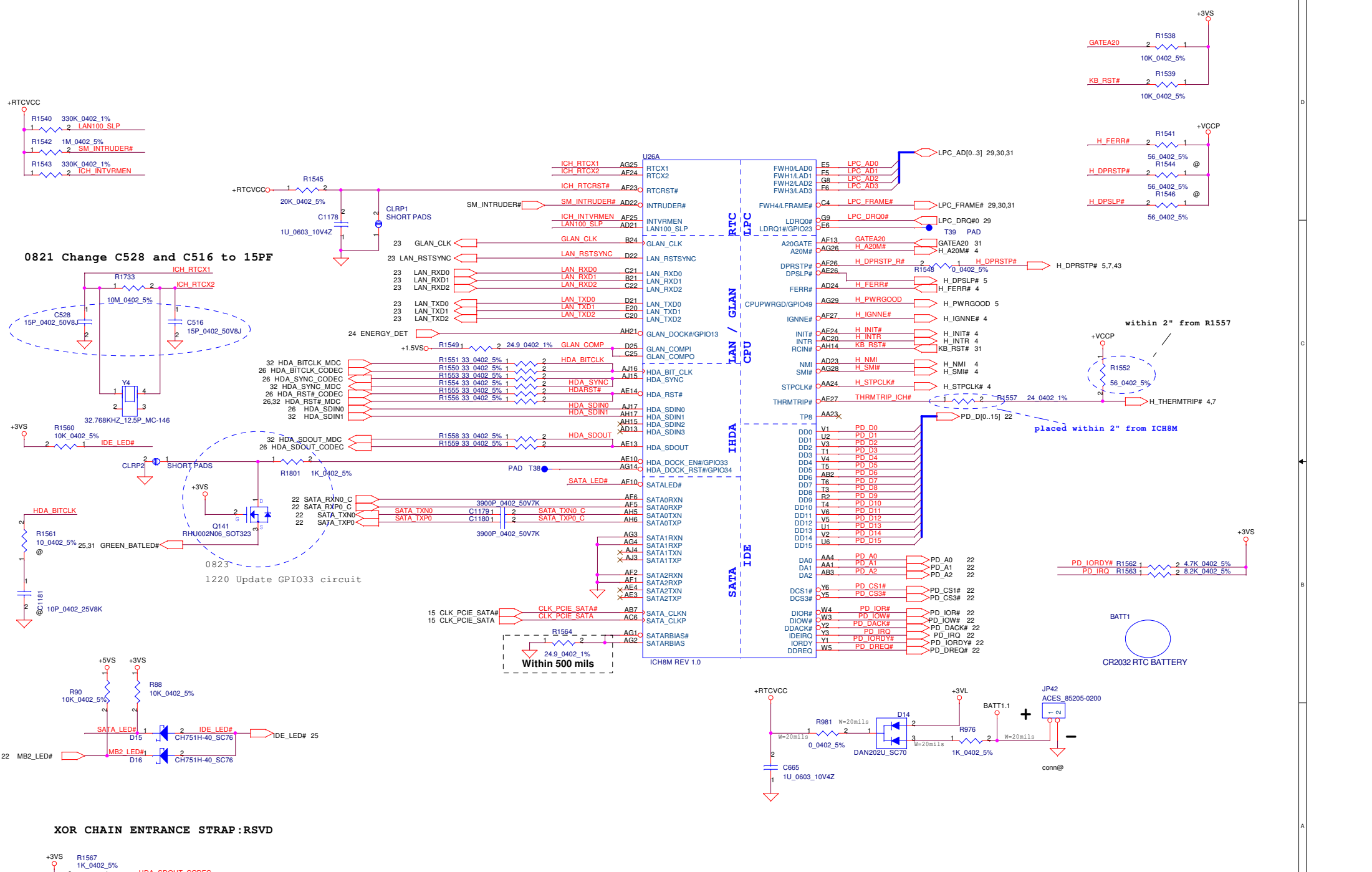


A16 swap override Strap	
Low= A16 swap override Enable	High= Default *

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC

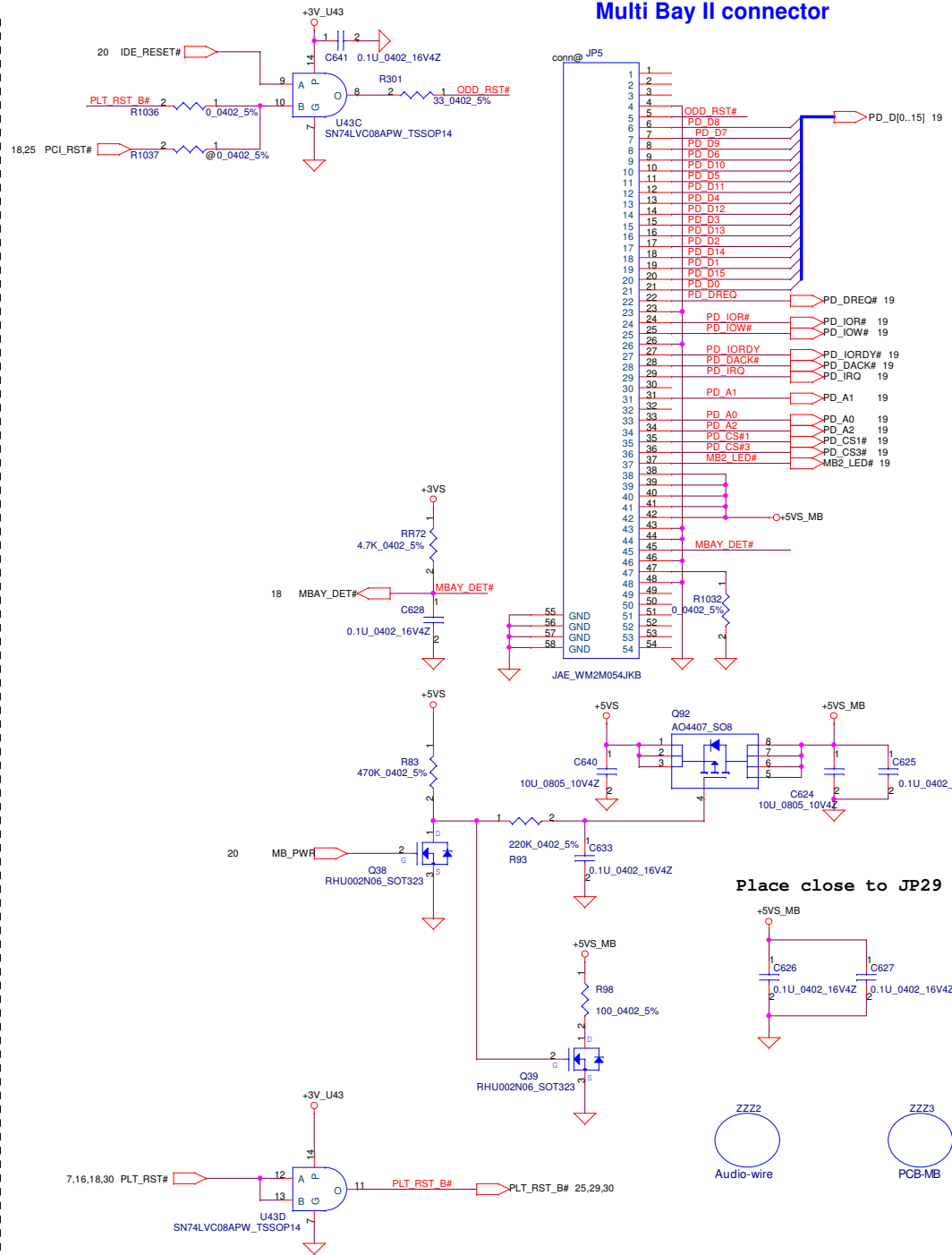
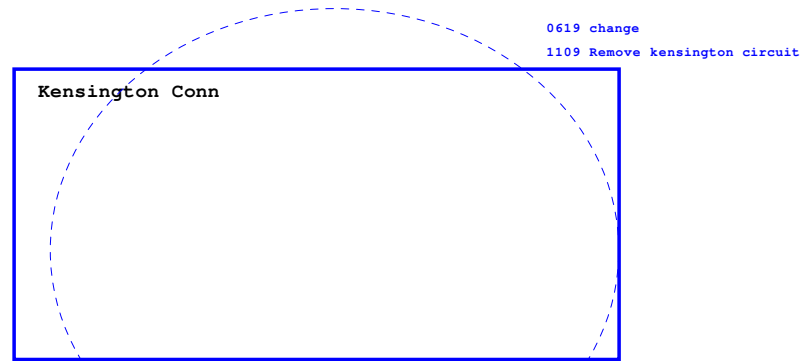
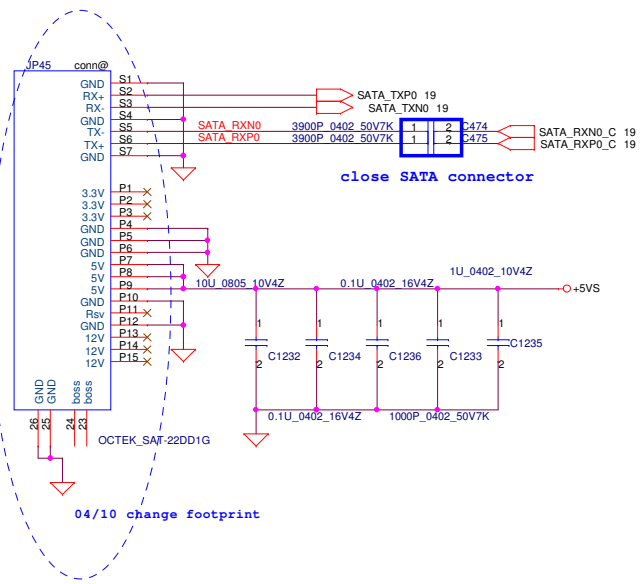


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Issued Date	2006/02/13	Deciphered Date	2006/03/10
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Title			
Compal Electronics, Inc.			
ICH8(2/4) LAN, HD, IDE, LPC			
Size	Document Number	Rev	
Custom	LA-3261P_UMA	0.4	
Date:	Tuesday, March 27, 2007	Sheet	19 of 55



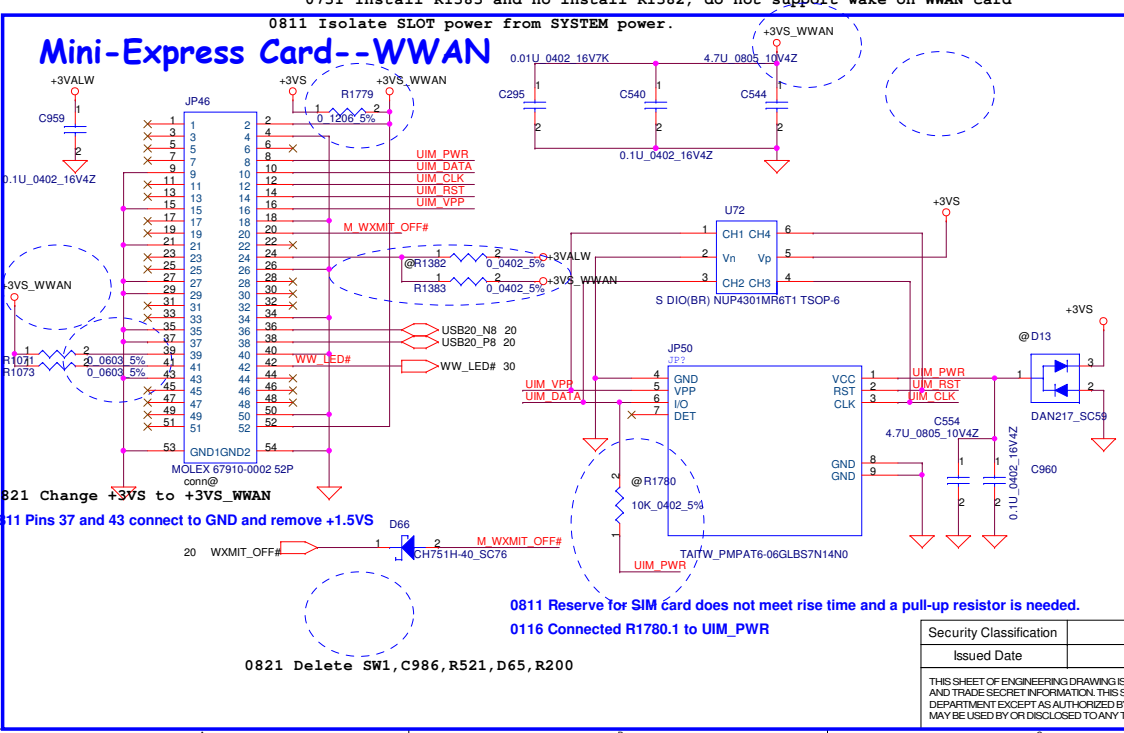
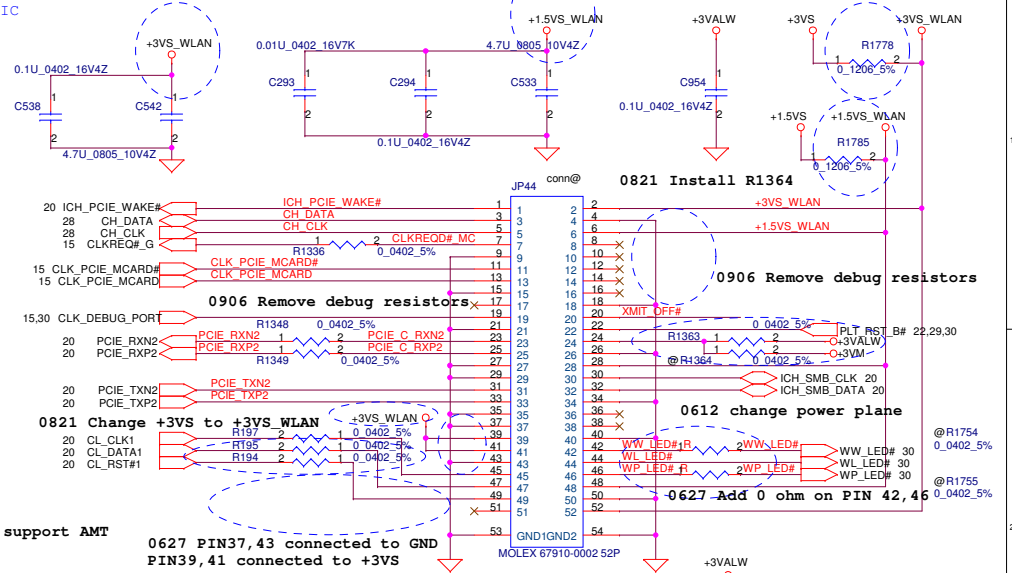
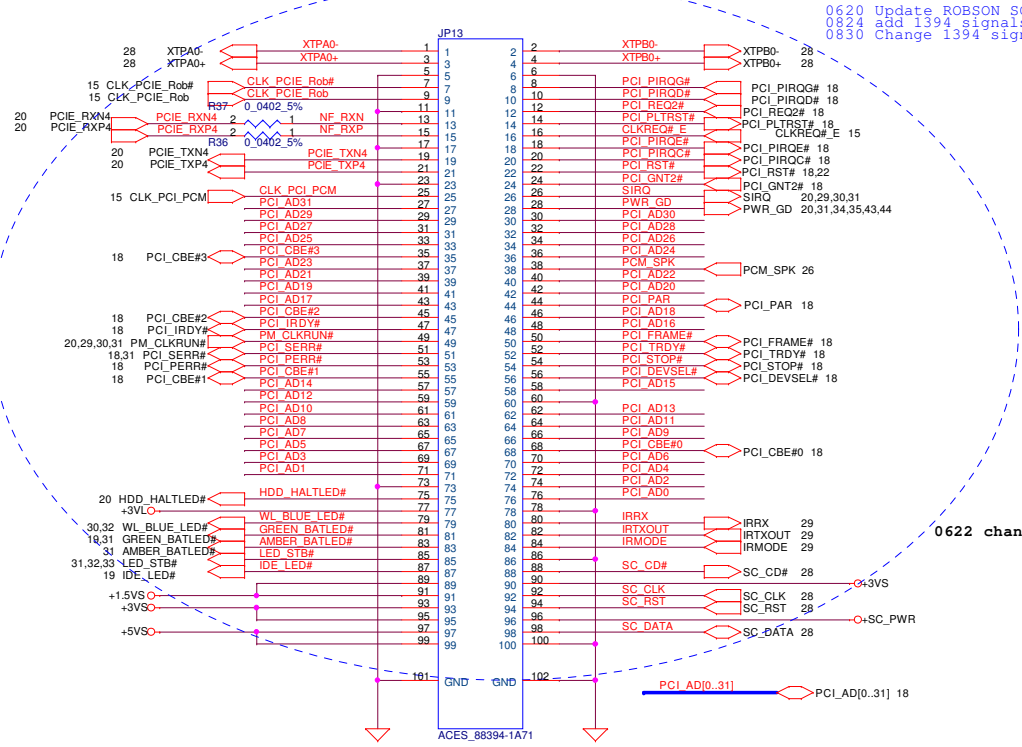
Security Classification	Compal Secret Data		Title	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	HDD & CDROM
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				Document Number LA-3261P UMA
				Rev 0.4
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B/B connector with PCI / LED / FIR / SC interface

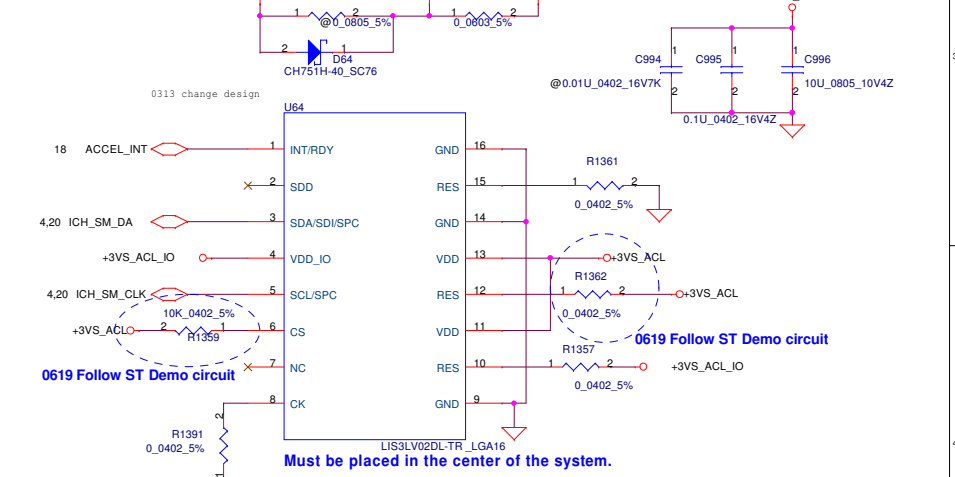
Mini-Express Card---WLAN

0824 Add +1.5VS_WLAN
0811 Isolate SLOT power from SYSTEM power.

0620 Update ROBSON SCHEMATIC
0824 add 1394 signals
0830 Change 1394 signals



ACCELEROMETER

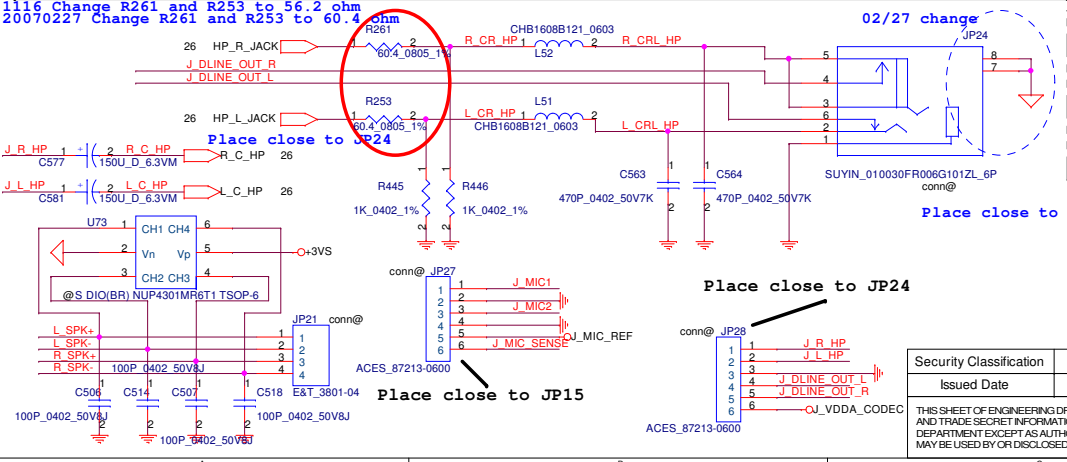
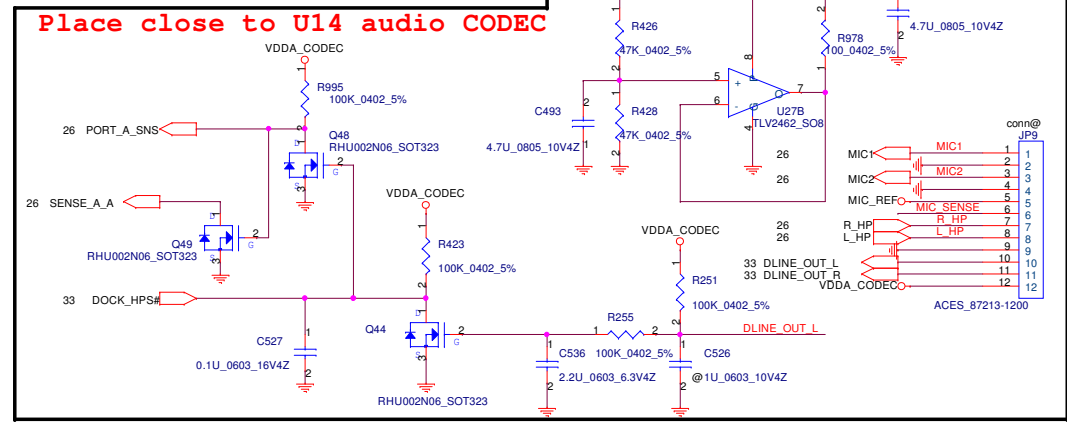
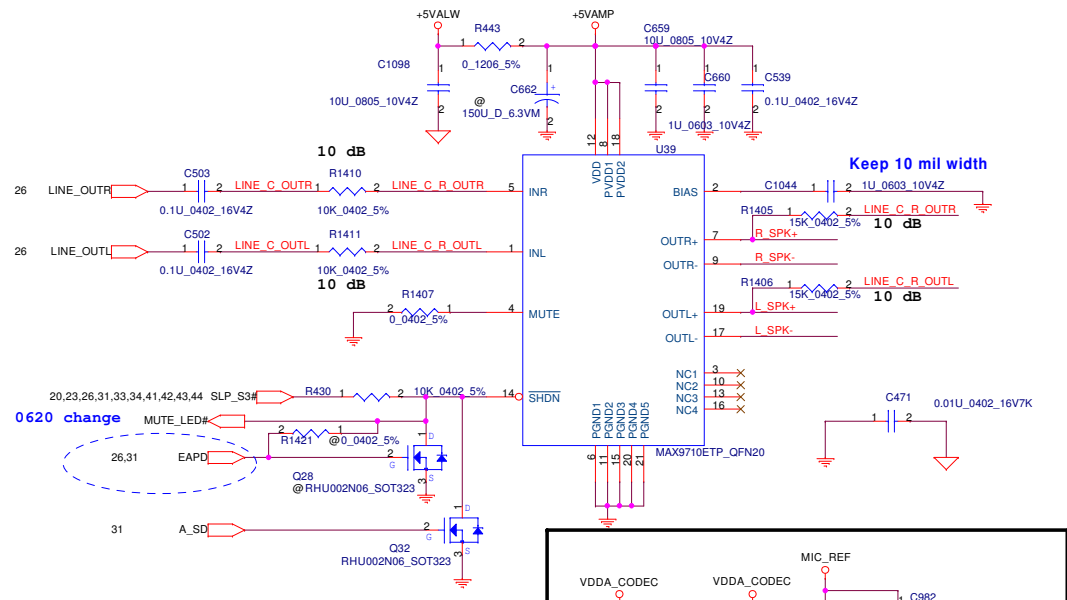


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		2006/07/26

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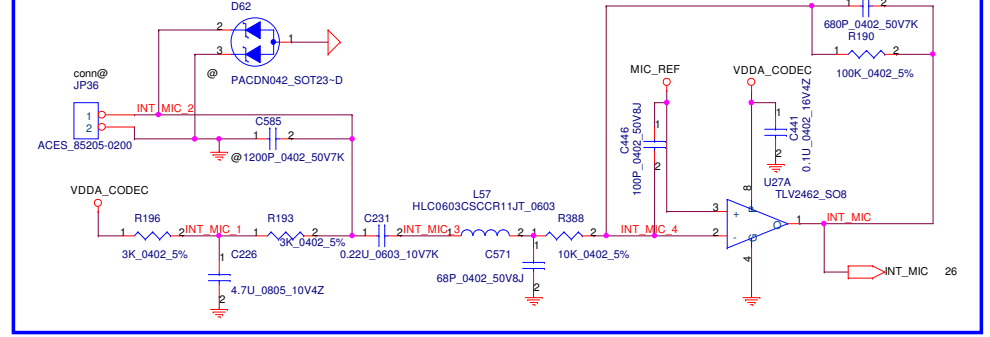
Compal Electronics, Inc.		
Title		
Mini-Card/Mini-PCI/Accelerometer		
Size	Document Number	Rev
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AMP. FOR INTERNAL SPEAKER



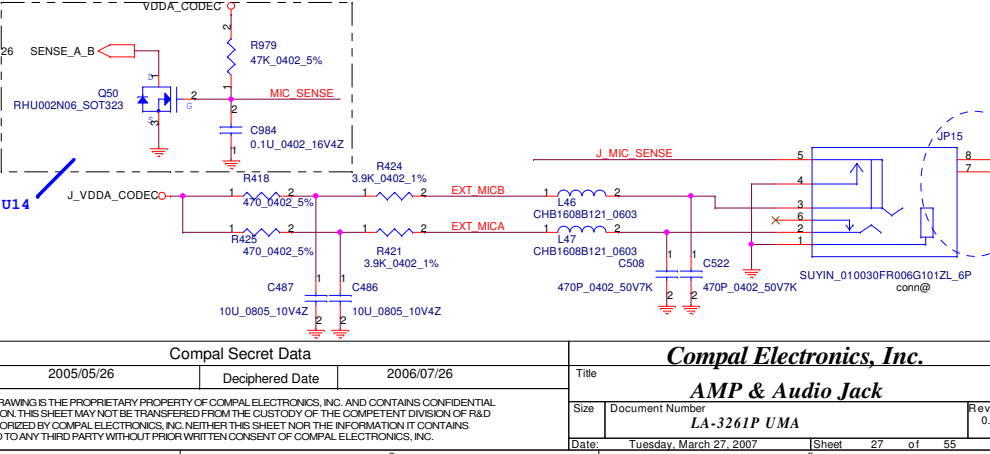
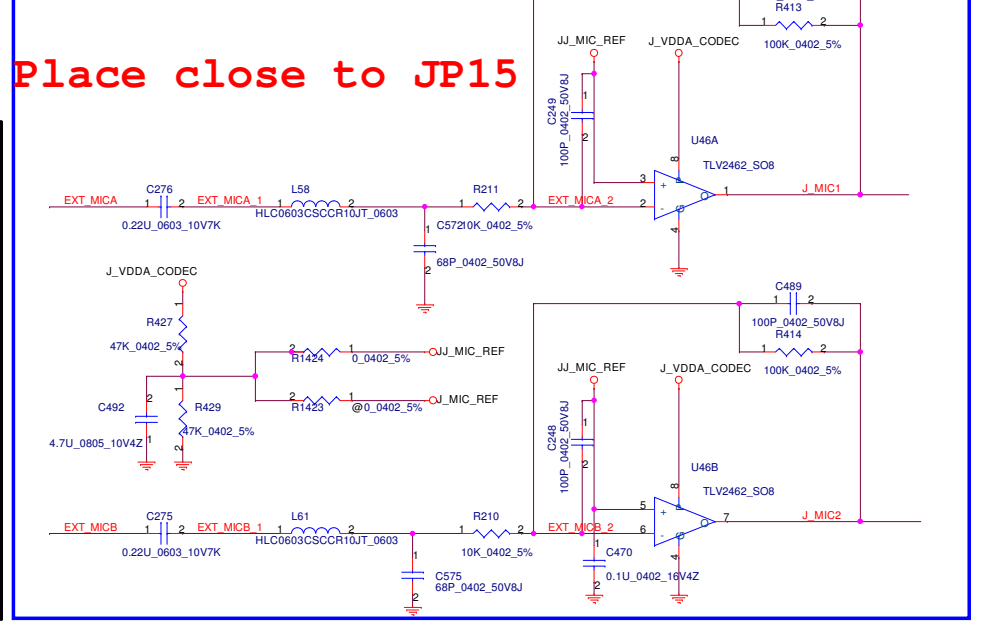
AMP. FOR INTERNAL MICROPHONE

Place close to U14 audio CODEC



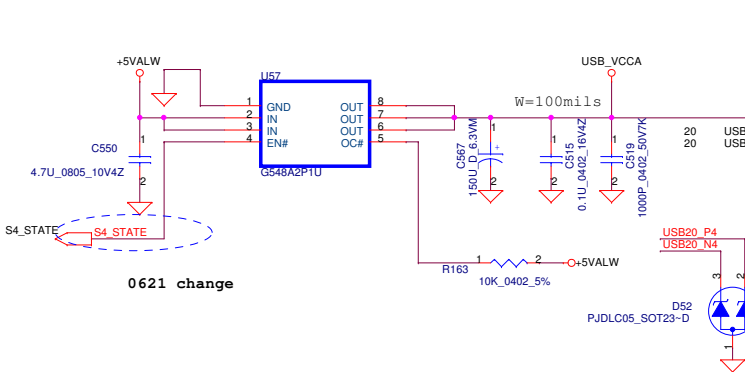
AMP. FOR EXTERNAL MICROPHONE

Place close to JP15

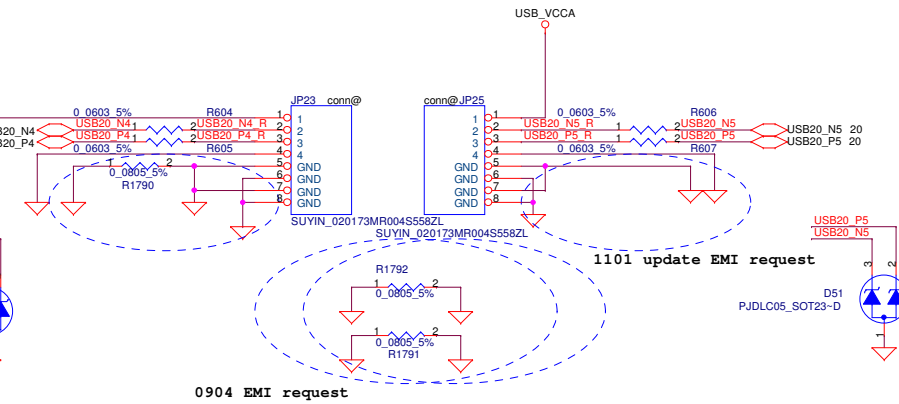


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Size	Document Number	Rev		
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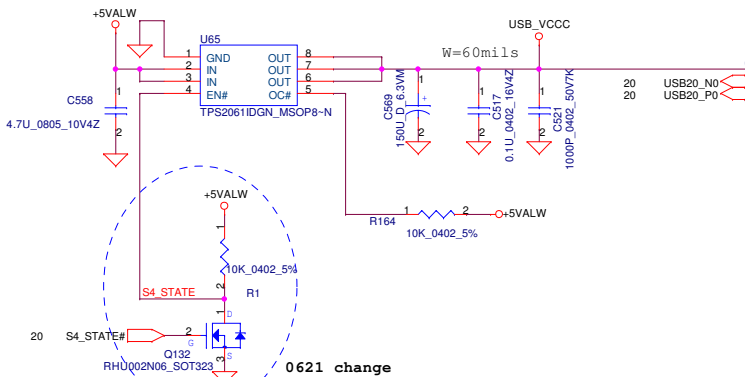
Left side USB CONNECTOR 0



Left side USB CONNECTOR 1

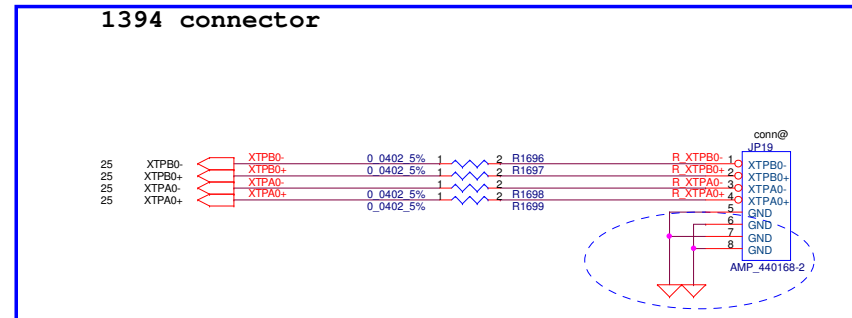


Right side USB CONNECTOR 0

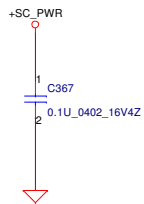
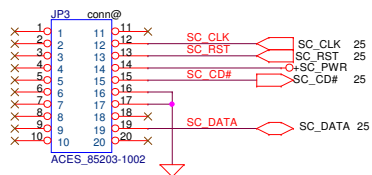


0904 EMI request

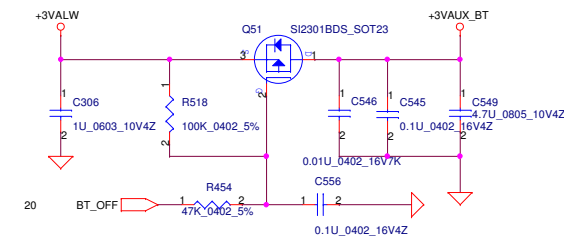
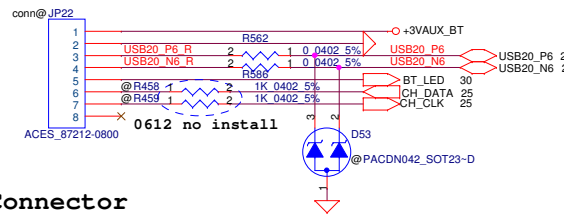
1394 connector



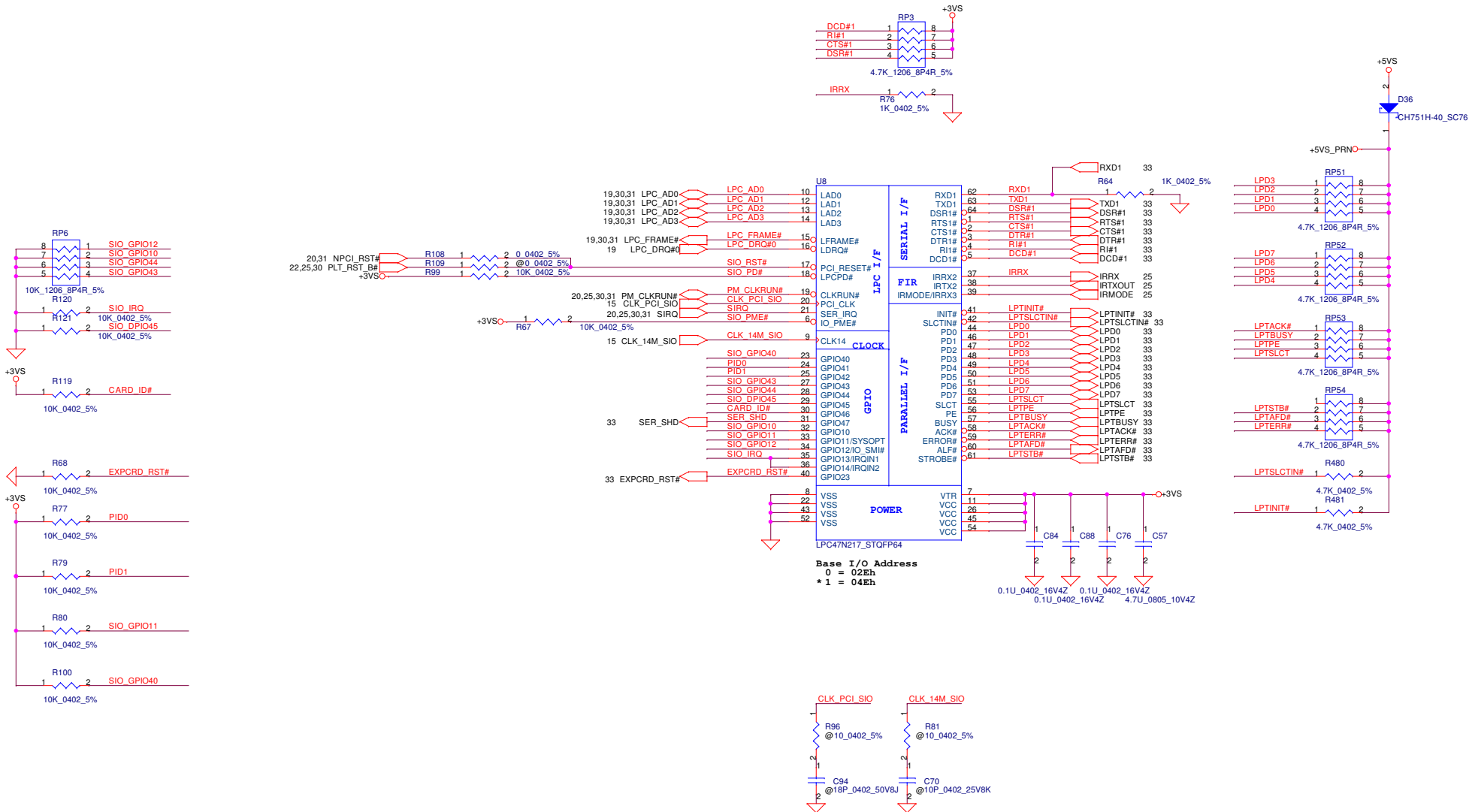
SMART Card connector



BT Connector



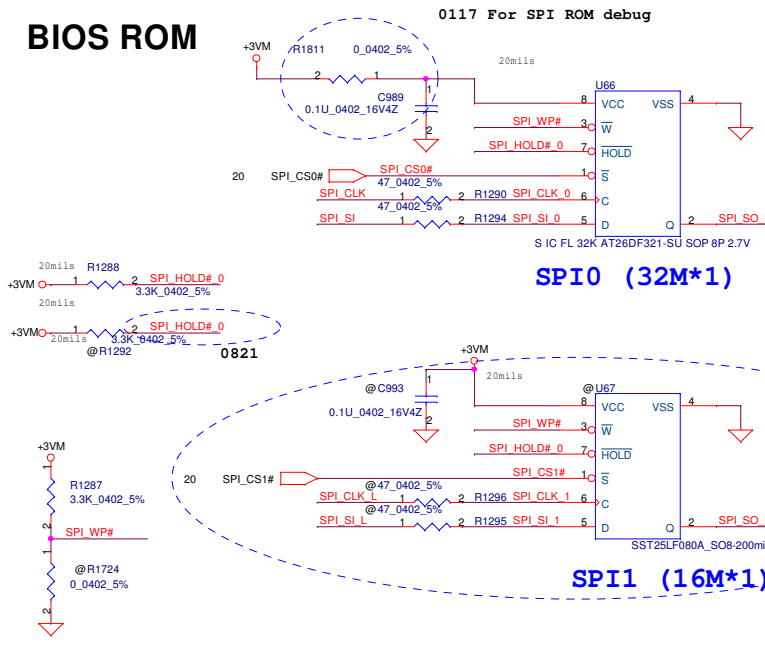
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Issued Date	2006/02/13	Deciphered Date	2006/07/26	USB & BT Connector	
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Compal Electronics, Inc.		
SUPER I/O LPC47N217		
Size	Document Number	Rev
	LA-3261P UMA	0.4
Date:	Tuesday, March 27, 2007	Sheet 29 of 55

BIOS ROM

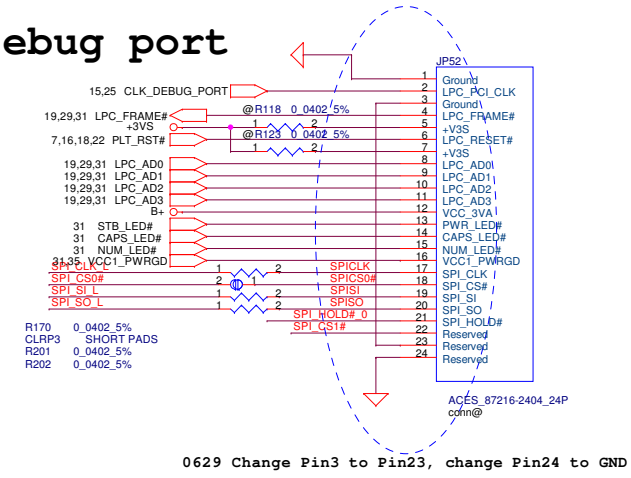


SPI0 (32M*1)

SPI1 (16M*1)

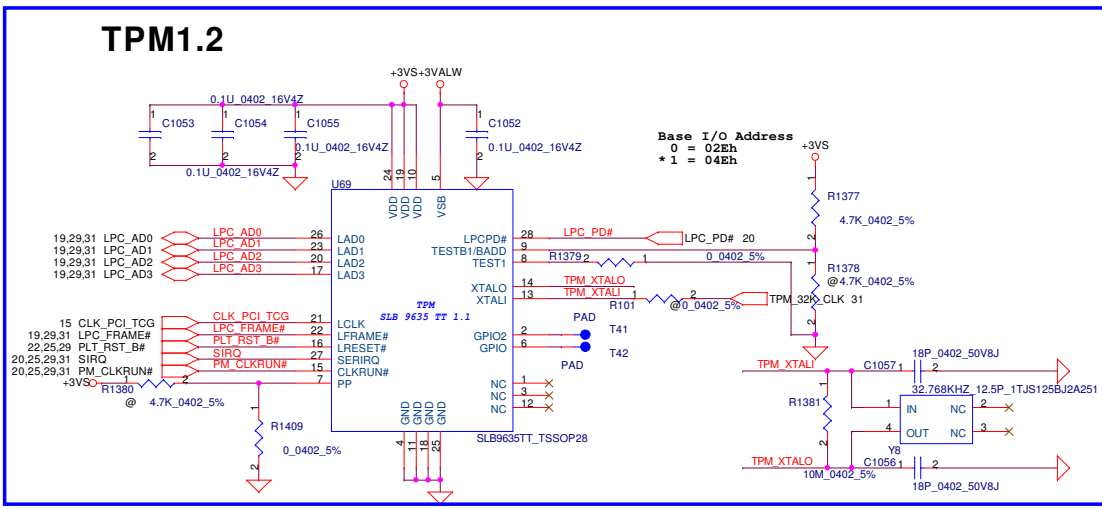
- 0821 SPI1 no install
- 0906 SPI1 install
- 1116 SPI1 no install

Debug port



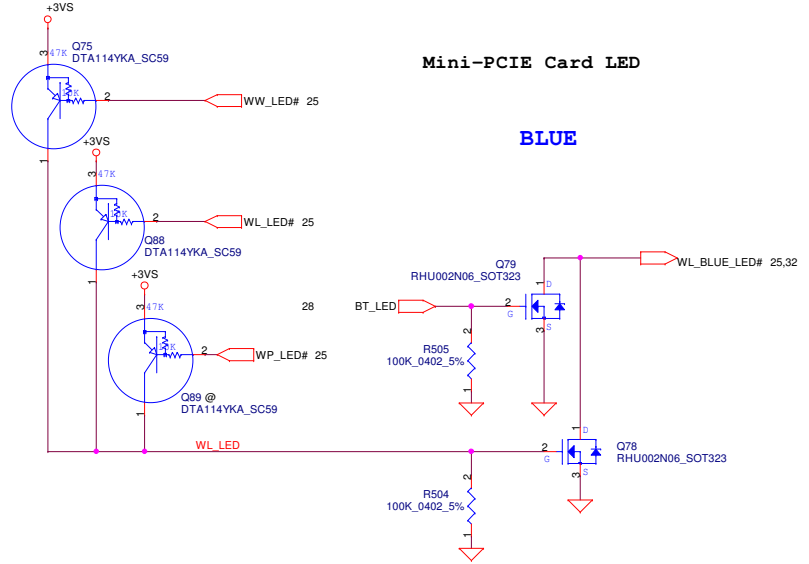
0629 Change Pin3 to Pin23, change Pin24 to GND

TPM1.2



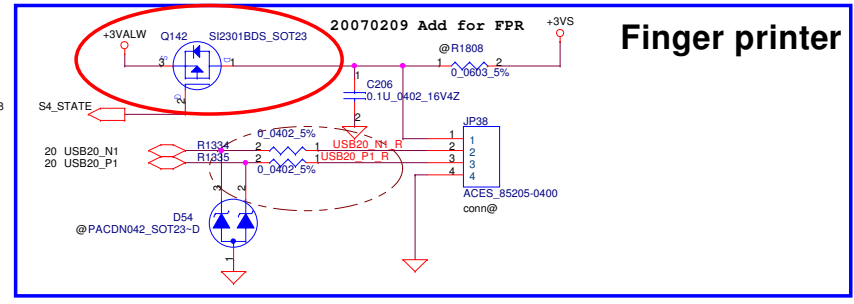
Base I/O Address
0 = 02Eh
* 1 = 04Eh

Mini-PCIE Card LED

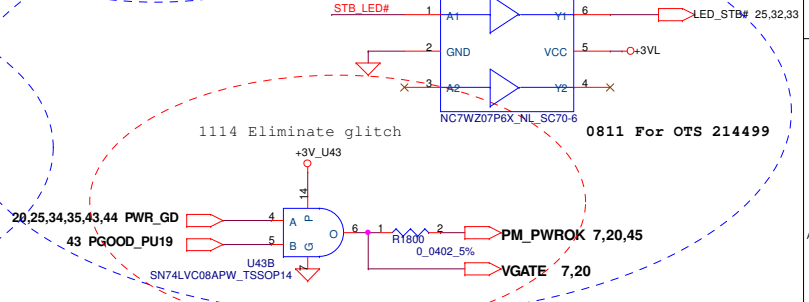
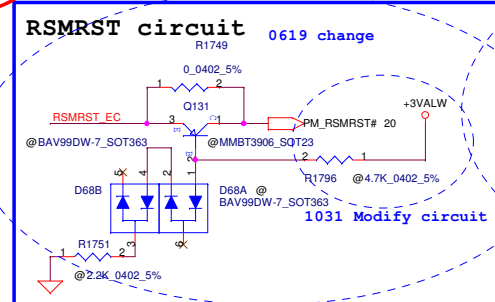
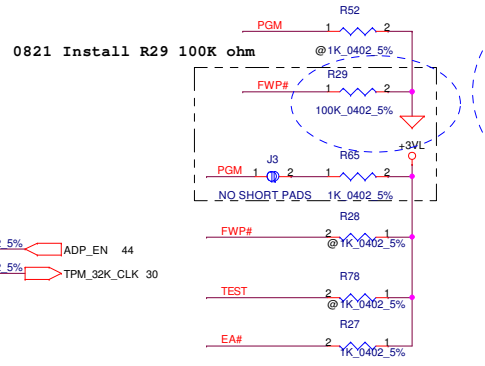
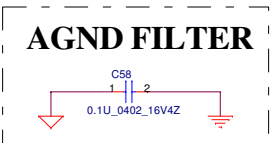
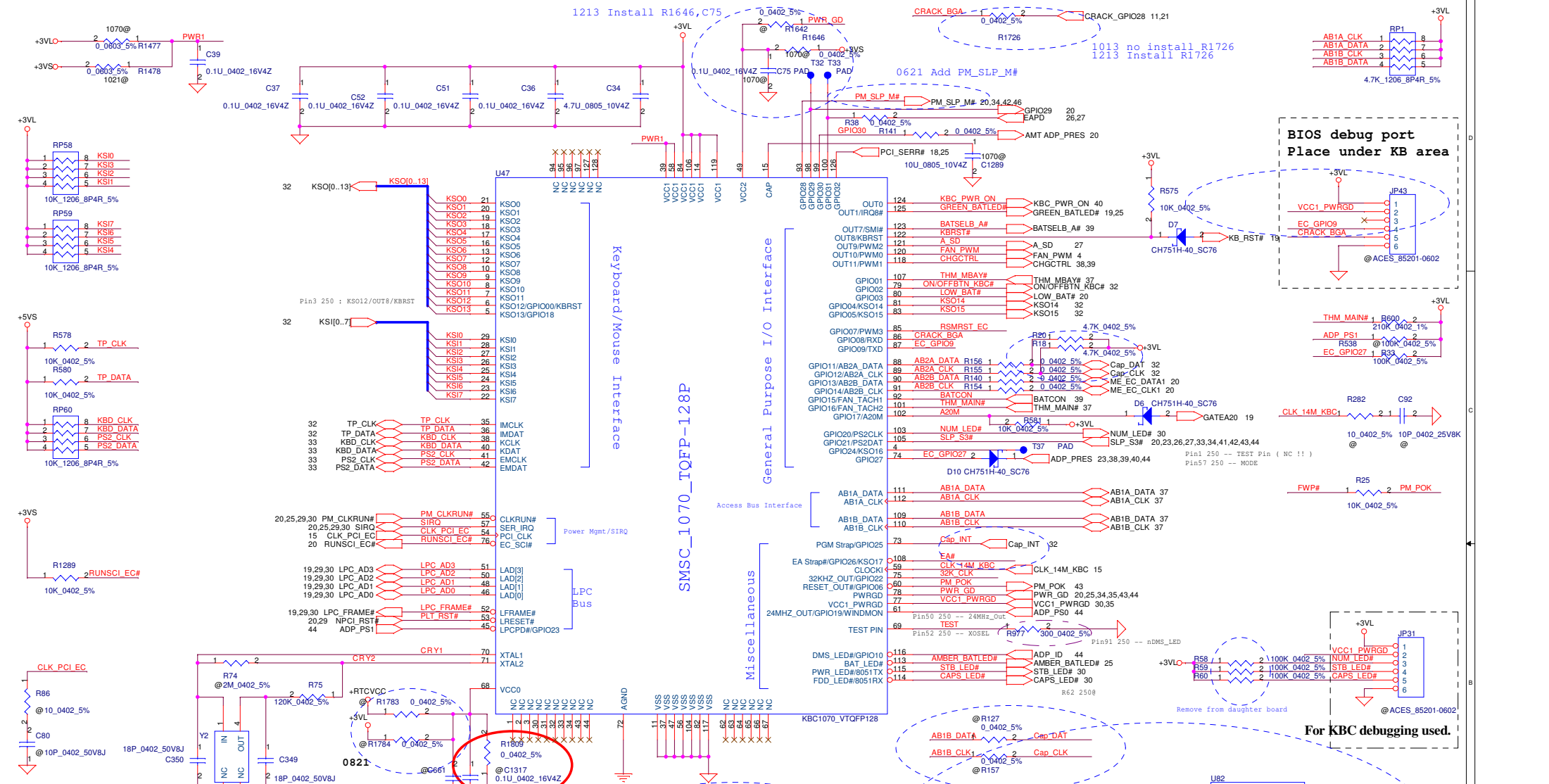


BLUE

Finger printer

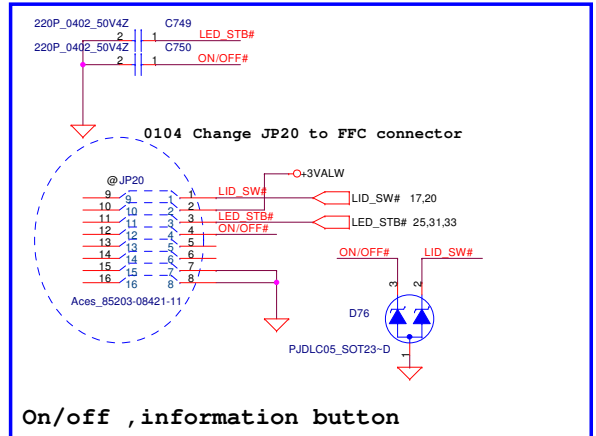
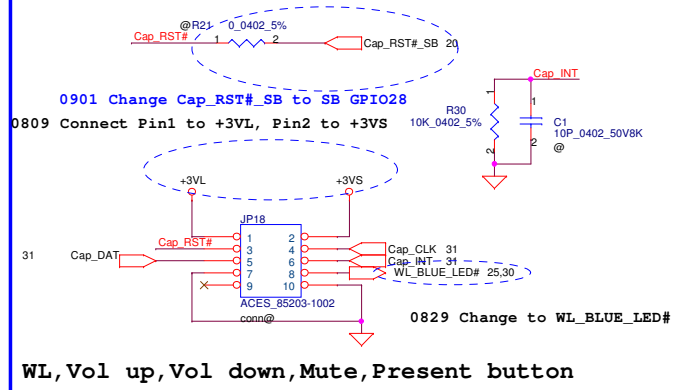


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Issued Date	2006/02/13	Deciphered Date	2006/07/26		
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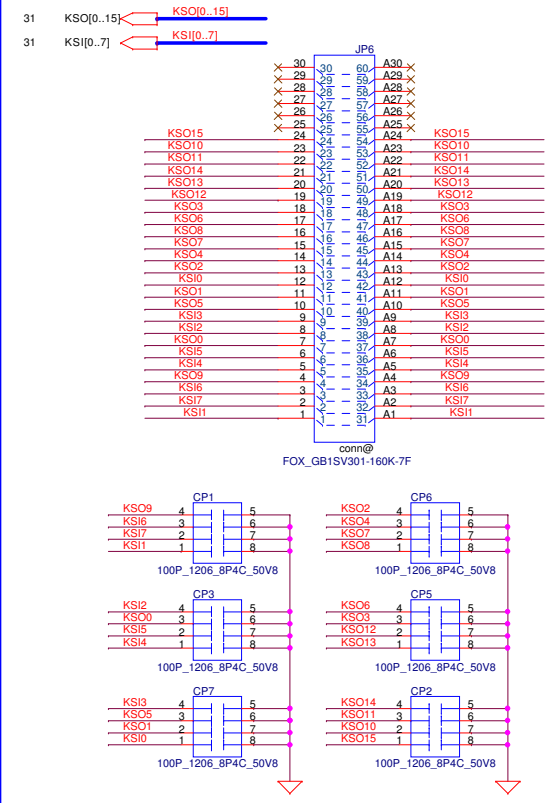


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Size	Document Number	Date: Tuesday, March 27, 2007		Sheet	Rev
	LA-326IP UMA			31	0.4

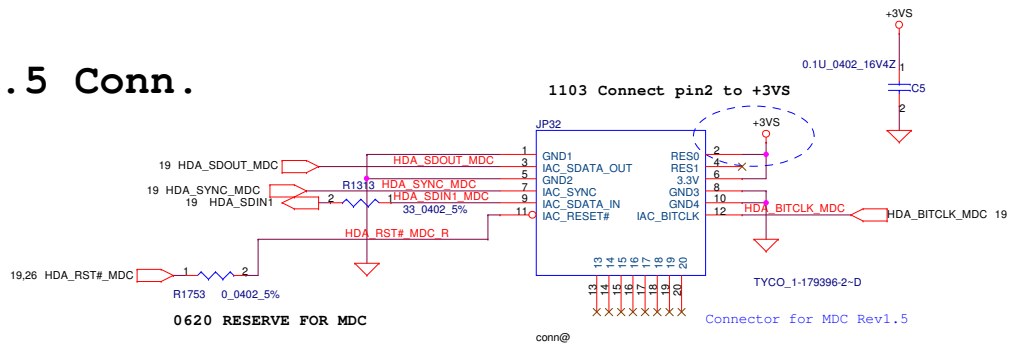
SWITCH BOARD. 0622 change



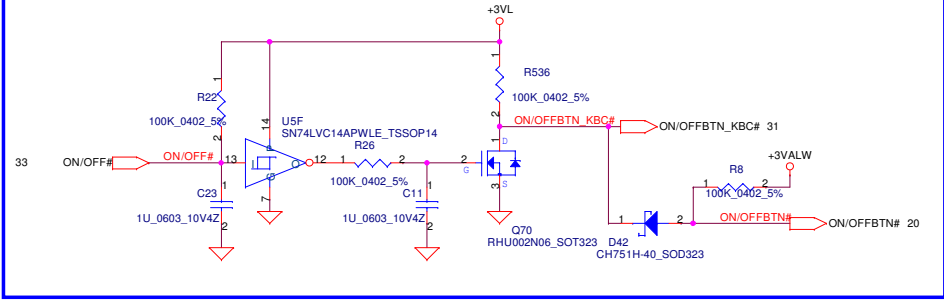
INT_KBD CONN.



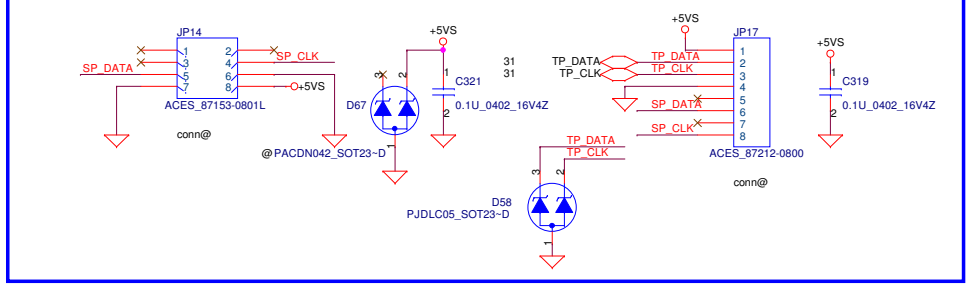
MDC 1.5 Conn.



Power button



TrackPoint CONN.

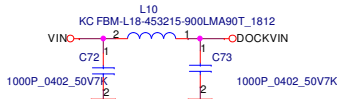
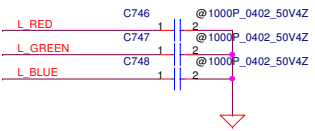


T/P BOARD.

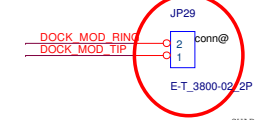
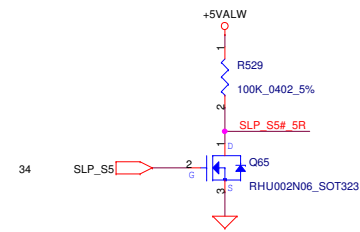
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Issued Date	2006/02/13	Deciphered Date	2006/07/26	Title
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			Rev	0.4
			Sheet	32 of 55

DOCK CONN. 184PIN

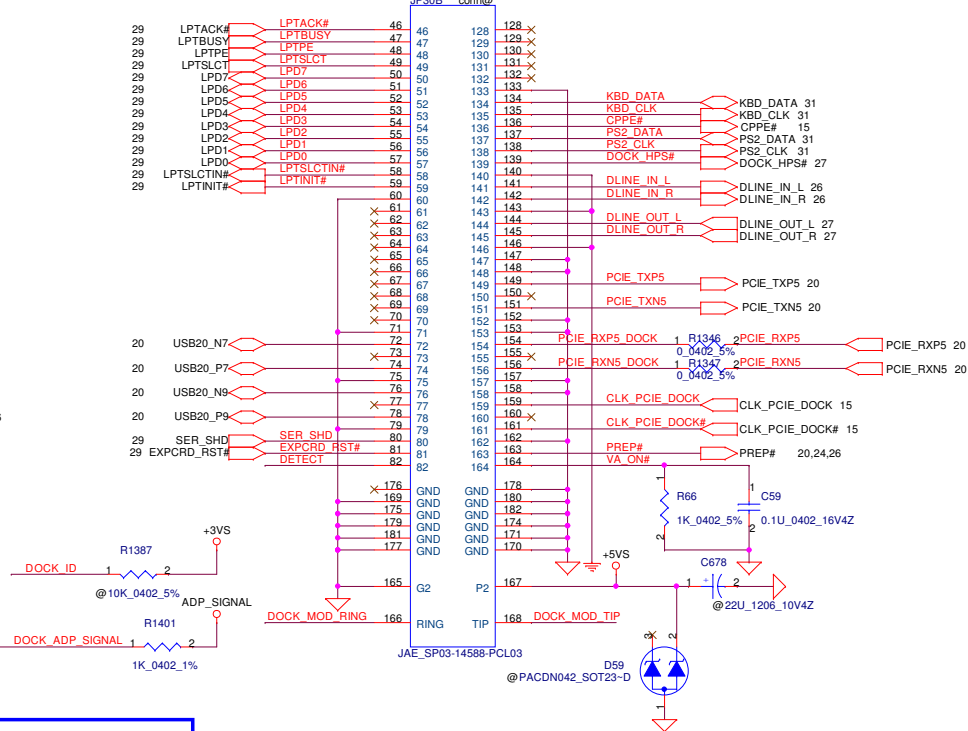
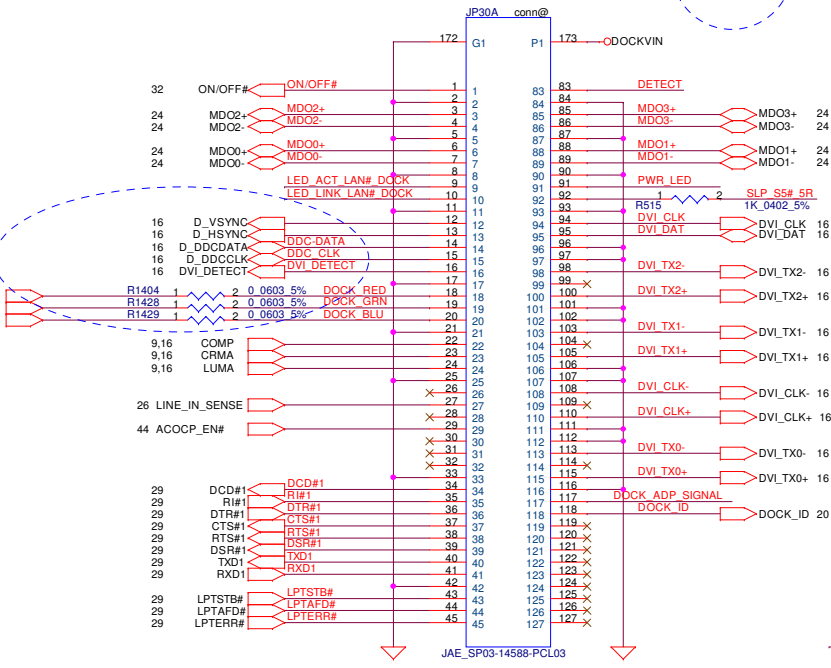
20070226 Change RJ11 connector



Closed to dock JP30

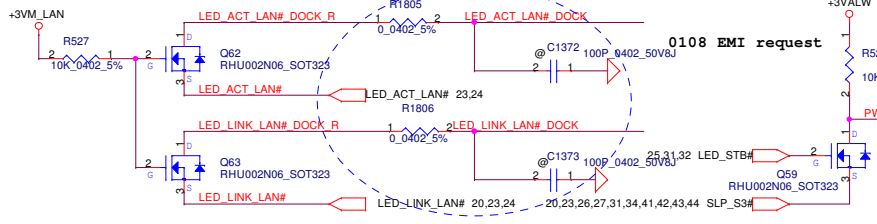
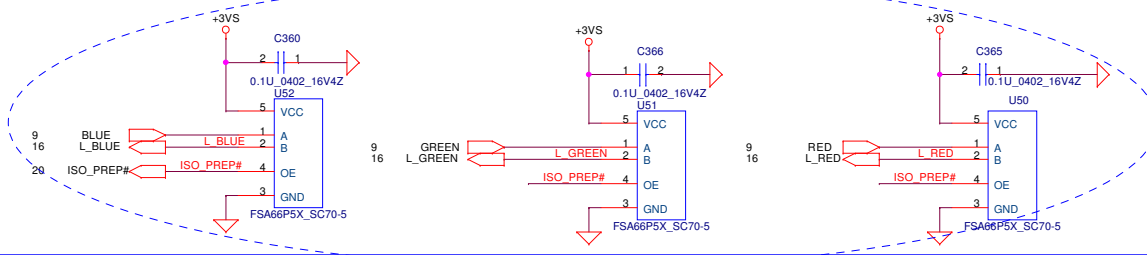


0314 change
1013 change



1013 Add CRT circuit

Closed to JP30

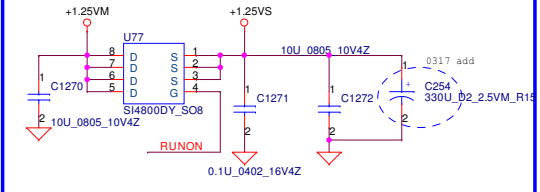


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Issued Date	2006/02/13	Deciphered Date
		2006/07/26

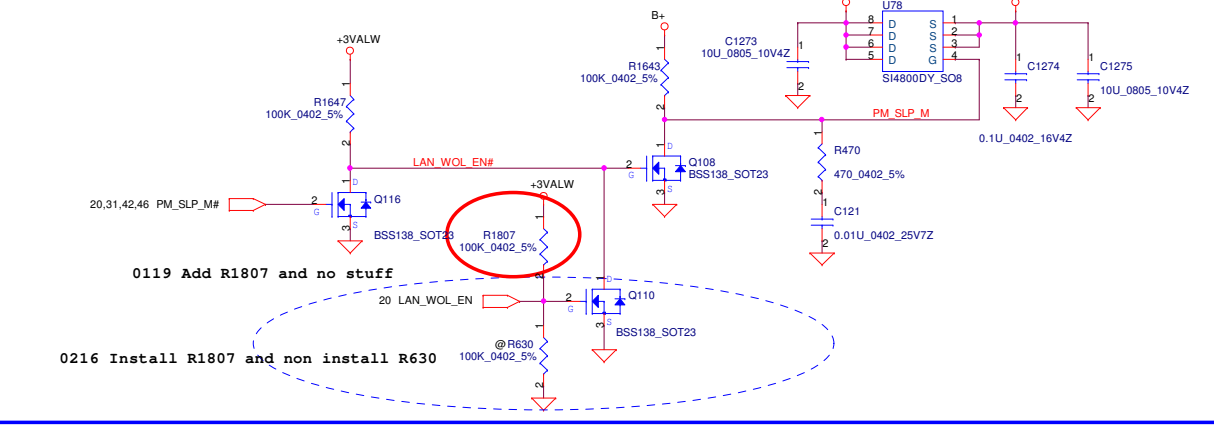
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			Docking CONN.	
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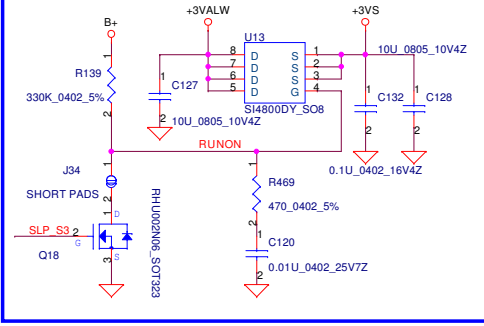
+1.25VM to +1.25VS Transfer



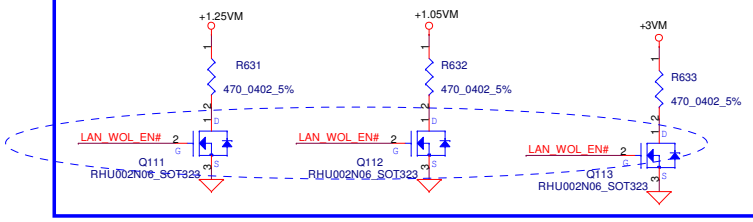
+3VALW to +3VM Transfer



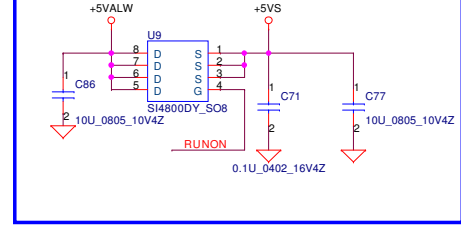
+3VALW to +3VS Transfer



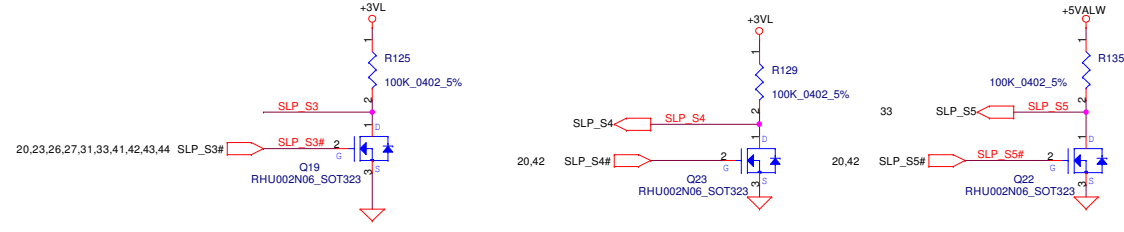
Discharge circuit-2 for V-M



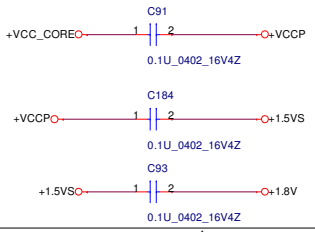
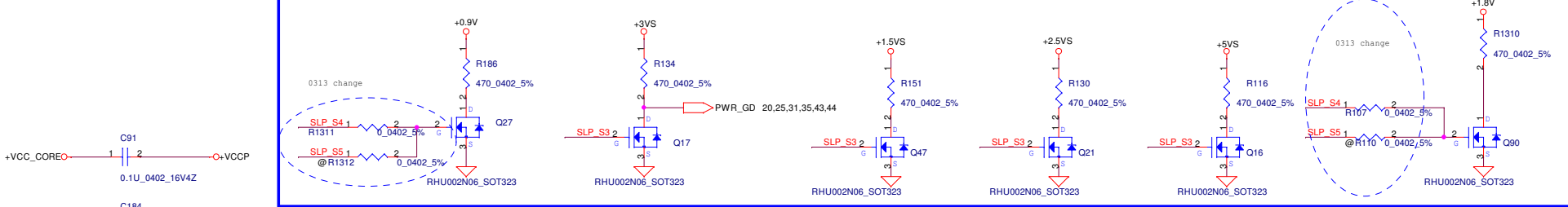
+5VALW to +5VS Transfer



0718 Change net from PM_SLP_M# to LAN_WOL_EN#

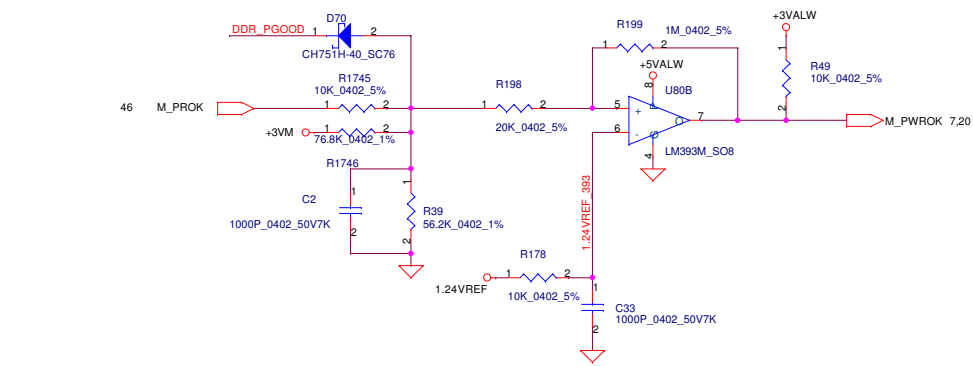
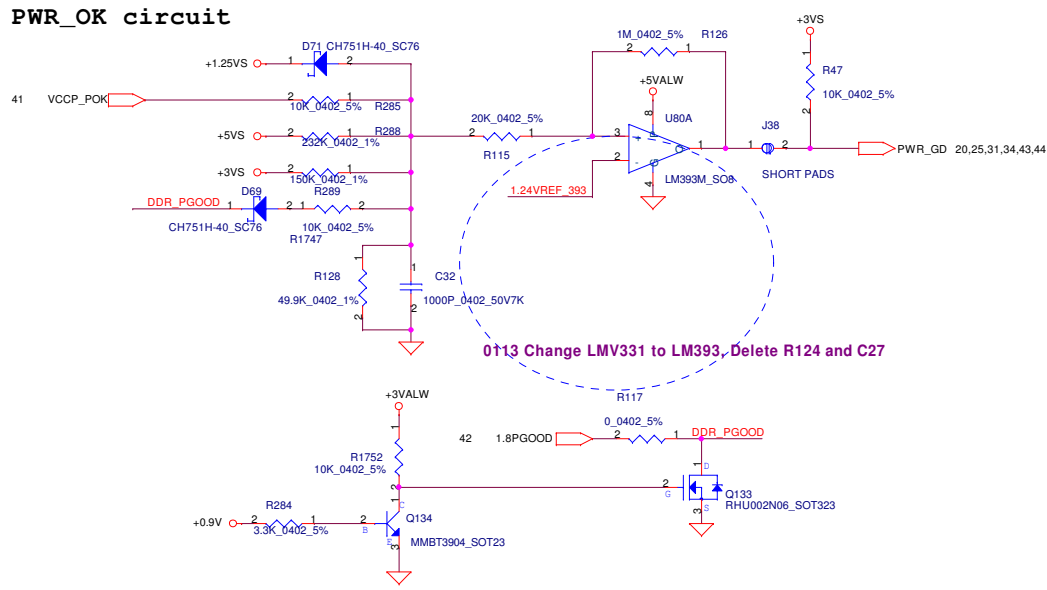


Discharge circuit-1

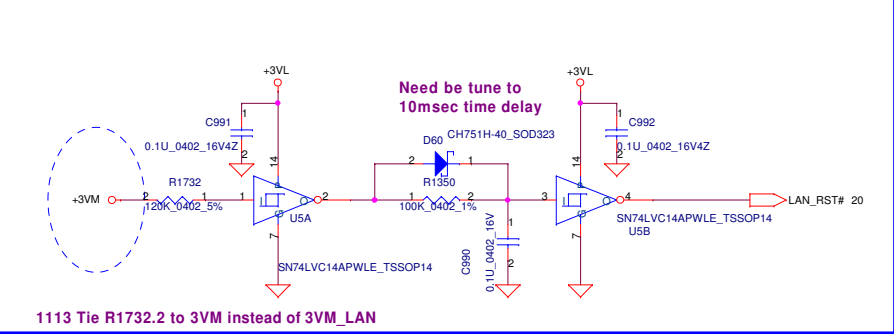


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Issued Date	2006/02/13	Deciphered Date	2006/07/26	DC/DC Circuits	
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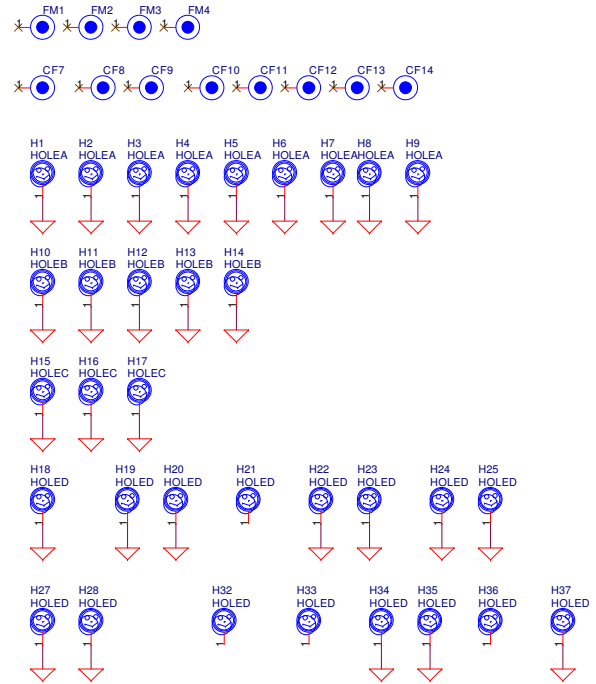
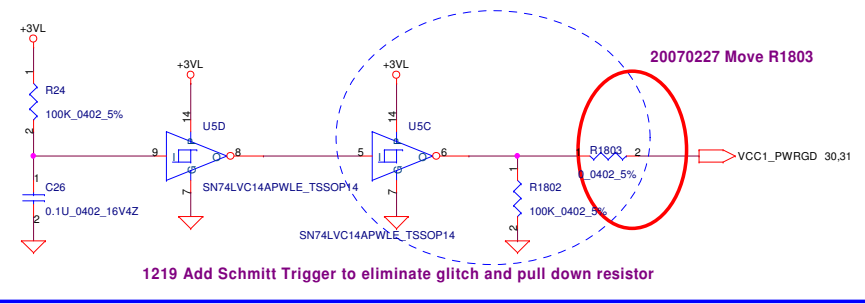
PWR_OK circuit



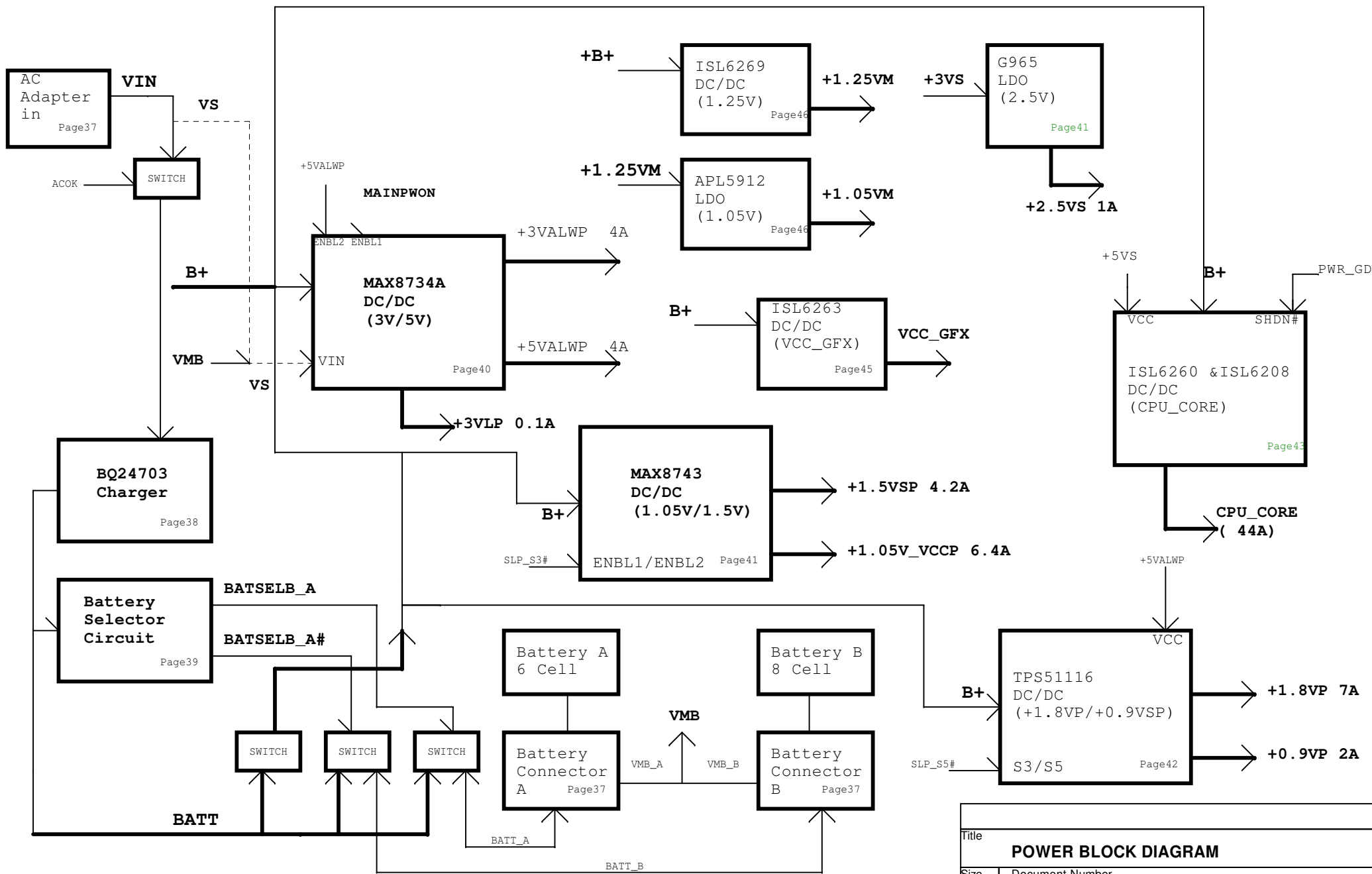
LAN_RST circuit



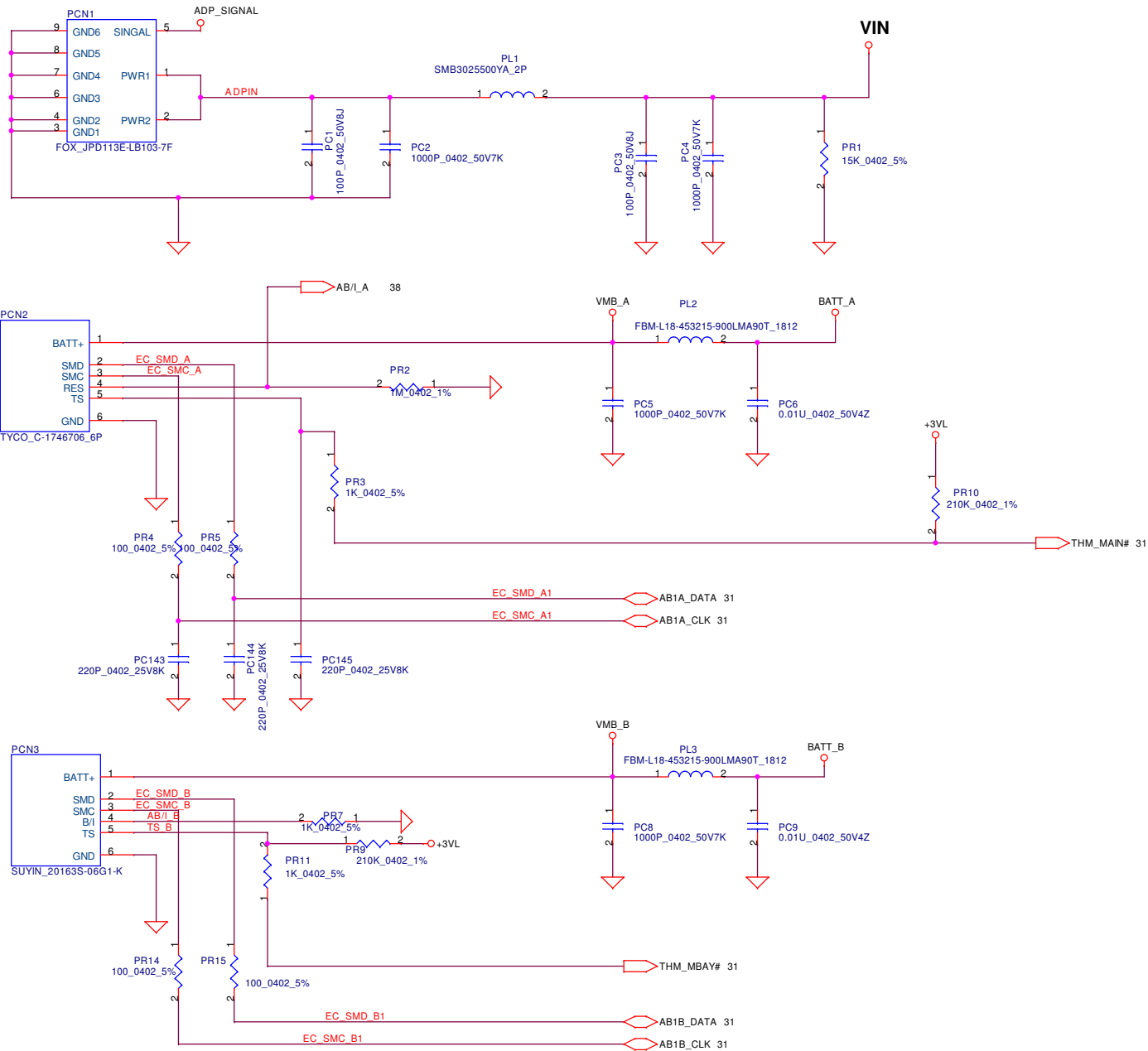
KBC PWR_OK circuit



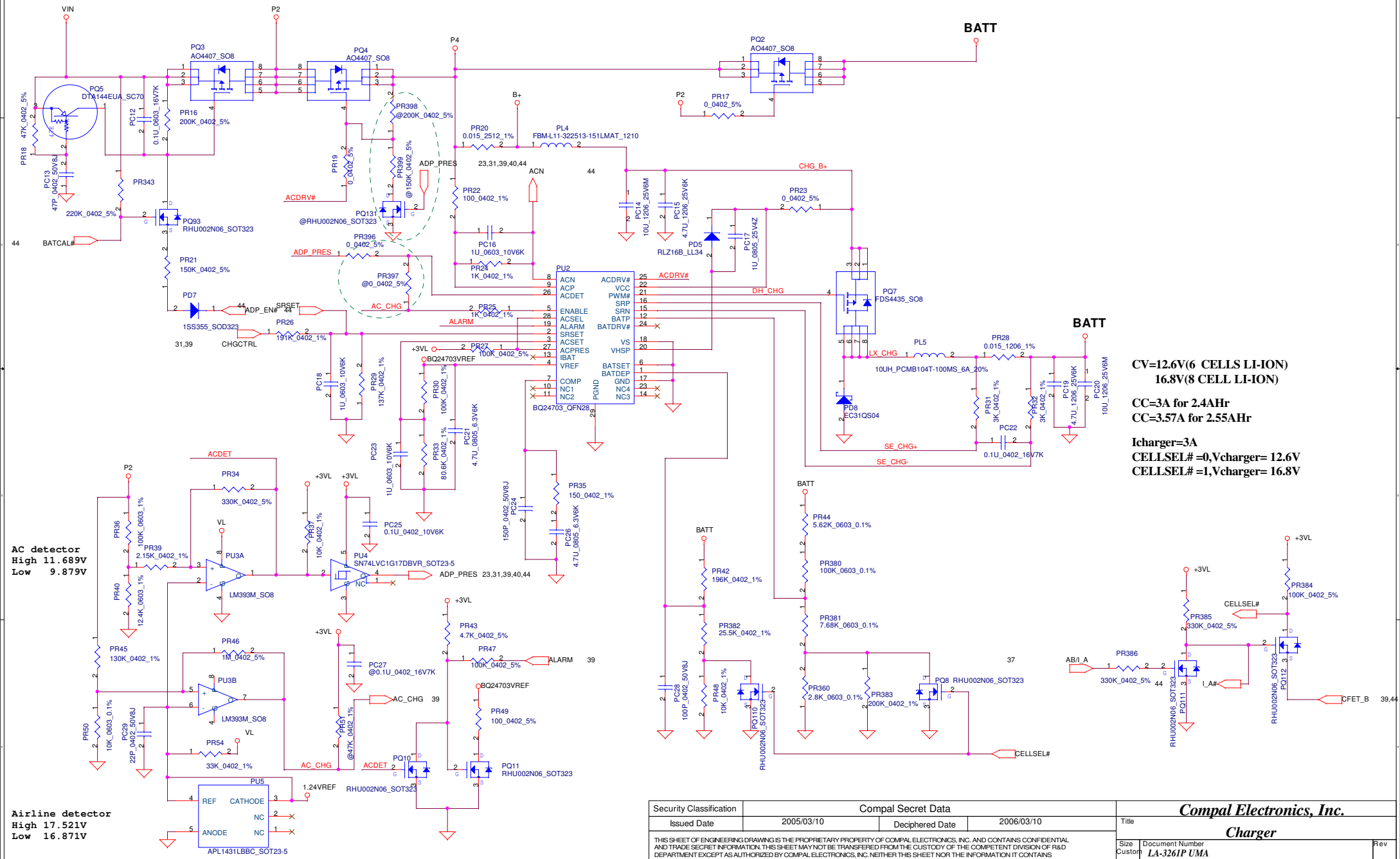
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Issued Date	2005/05/26	Deciphered Date	2006/07/26	Compal Electronics, Inc.
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Title		
POWER BLOCK DIAGRAM		
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Issued Date	2005/03/10	Deciphered Date	2006/03/10		
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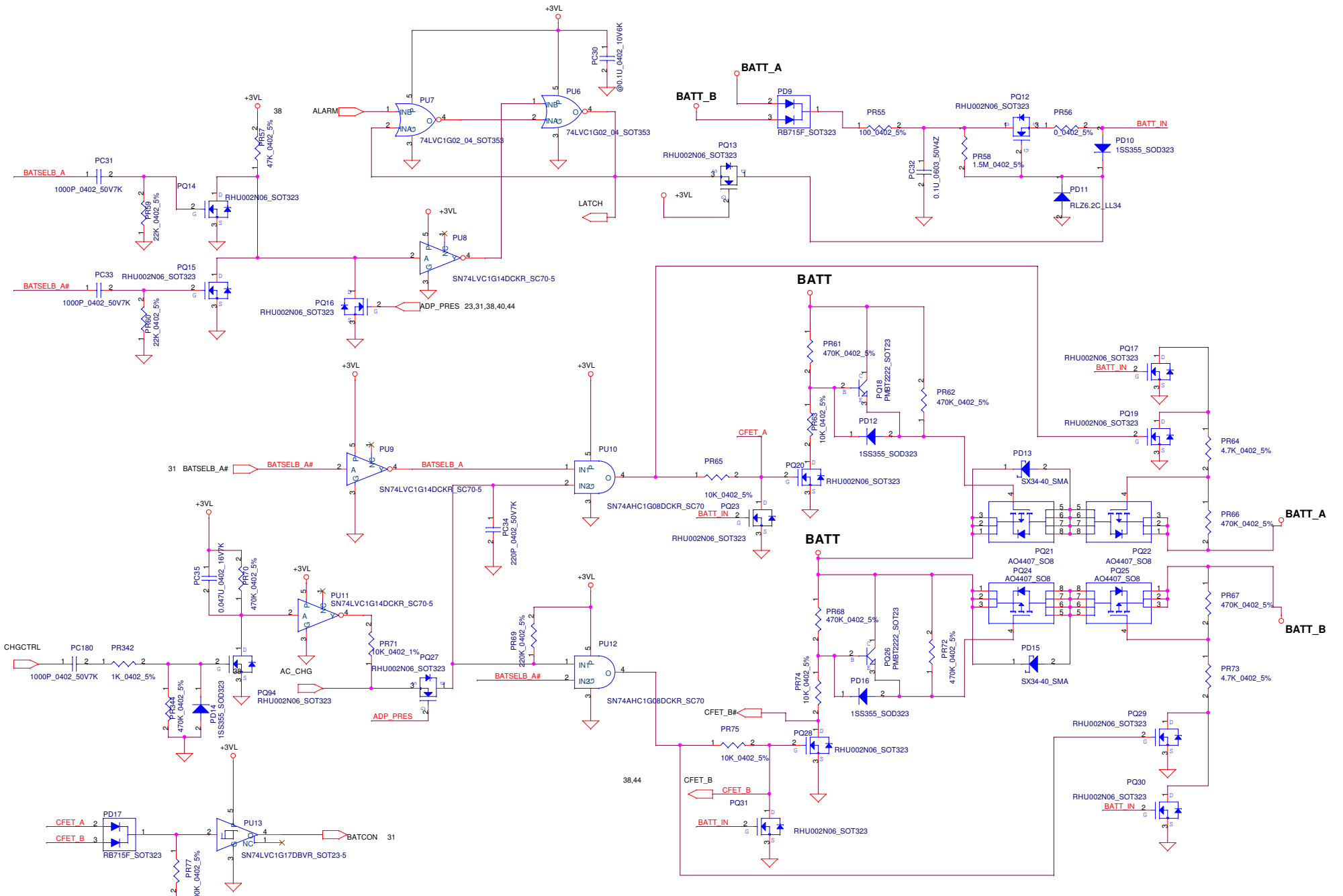
CV=12.6V(6 CELLS LI-ION)
16.8V(8 CELL LI-ION)
CC=3A for 2.4Hr
CC=3.57A for 2.55Ahr
Icharger=3A
CELLSEL#=0,Vcharger=12.6V
CELLSEL#=1,Vcharger=16.8V

AC detector
High 11.689V
Low 9.879V

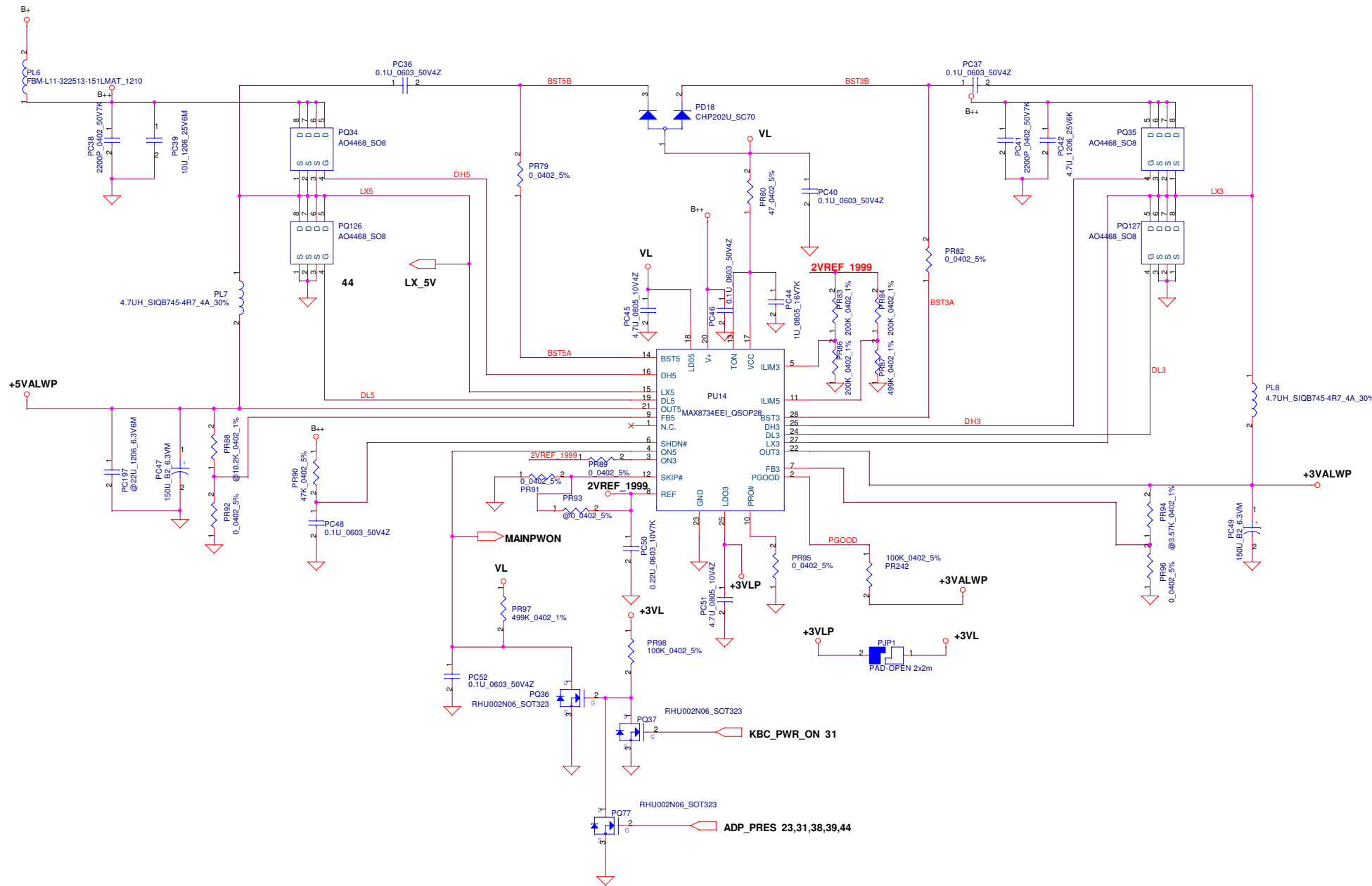
Airline detector
High 17.521V
Low 16.871V

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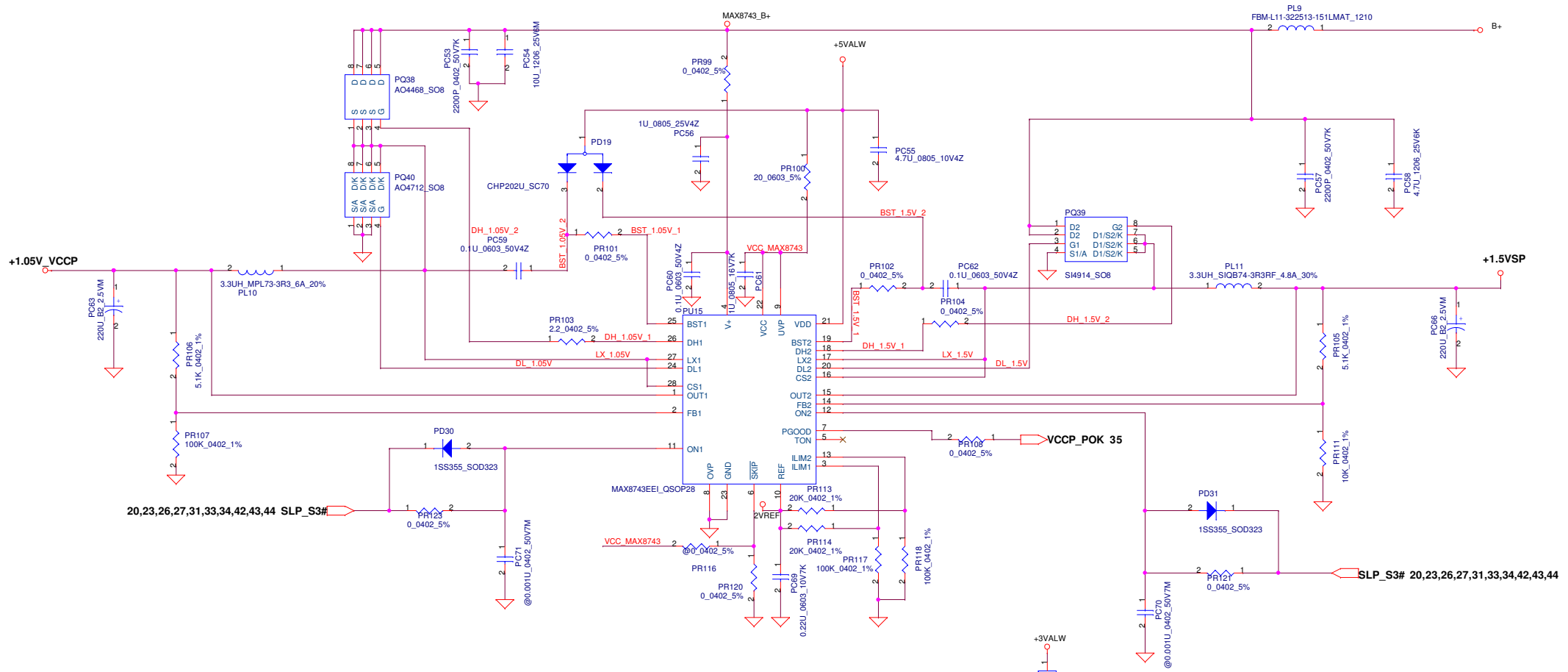
Compal Electronics, Inc.		
Charger		
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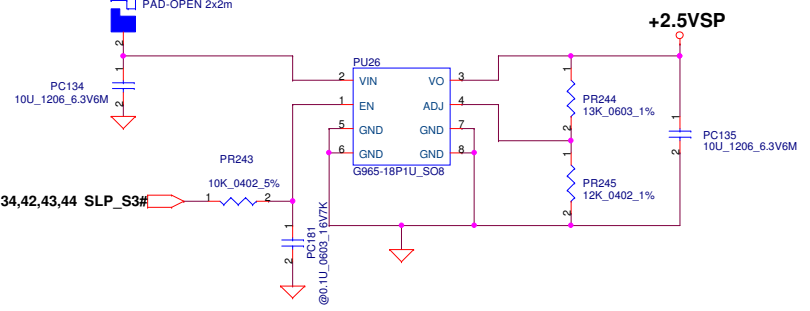
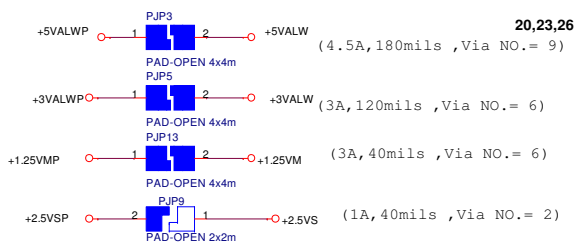
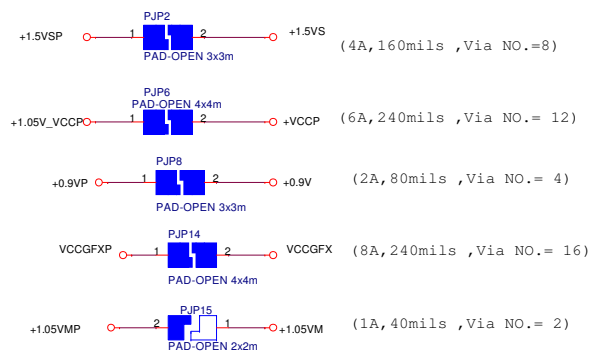
Security Classification	Compal Secret Data		Title	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Compal Electronics, Inc.
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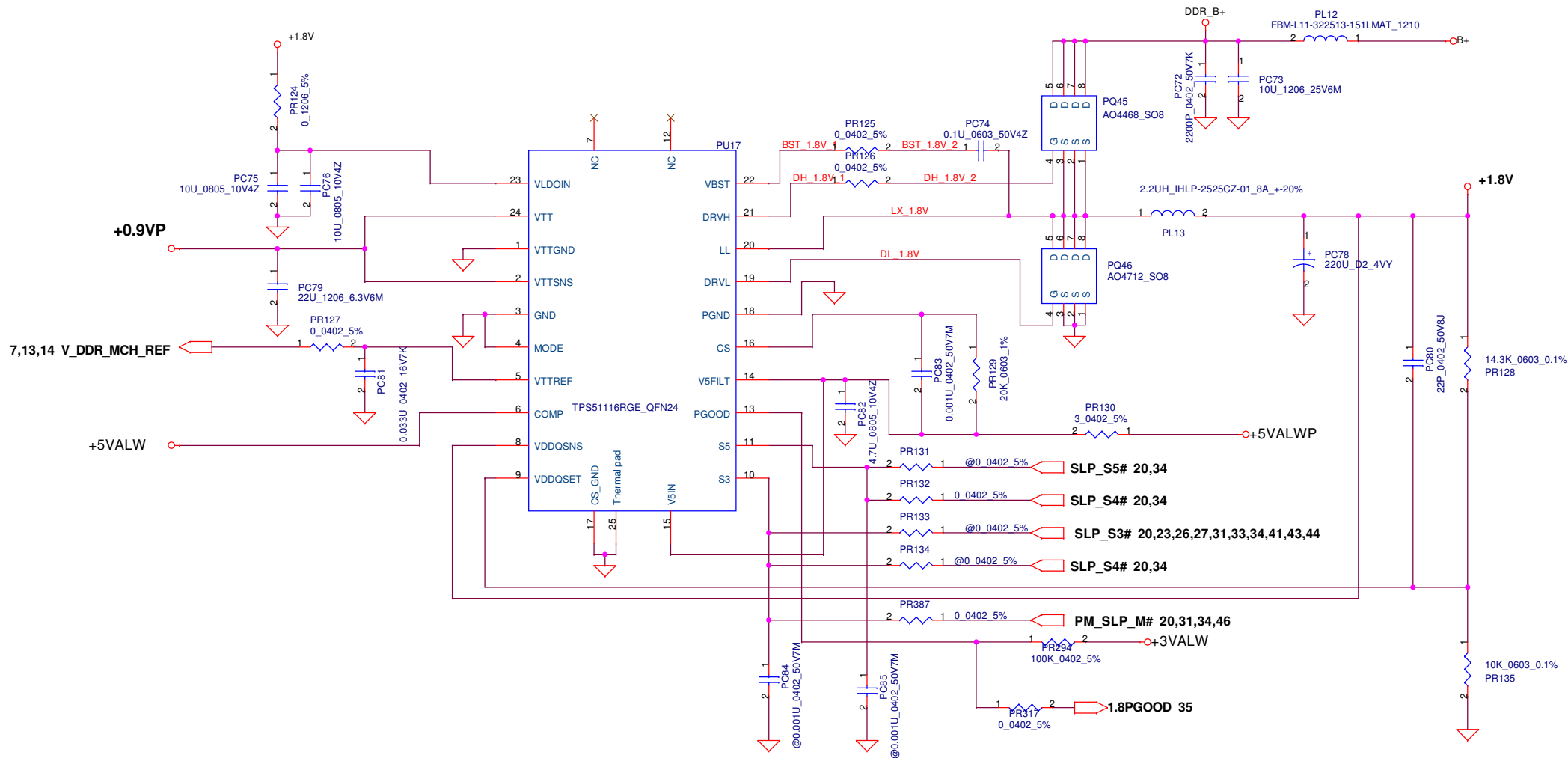
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1.5VSP/+1.05V_VCCP/+2.5V

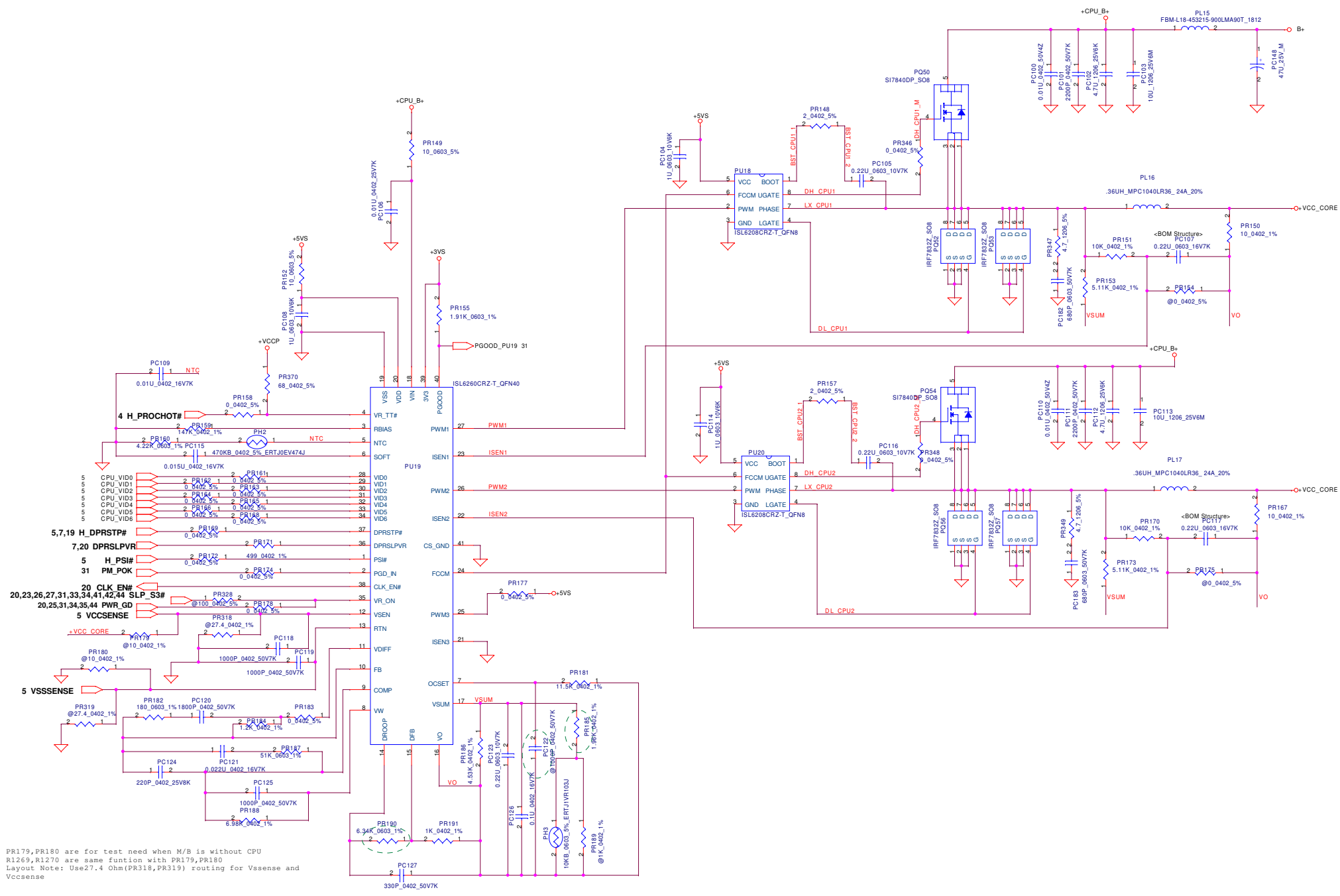


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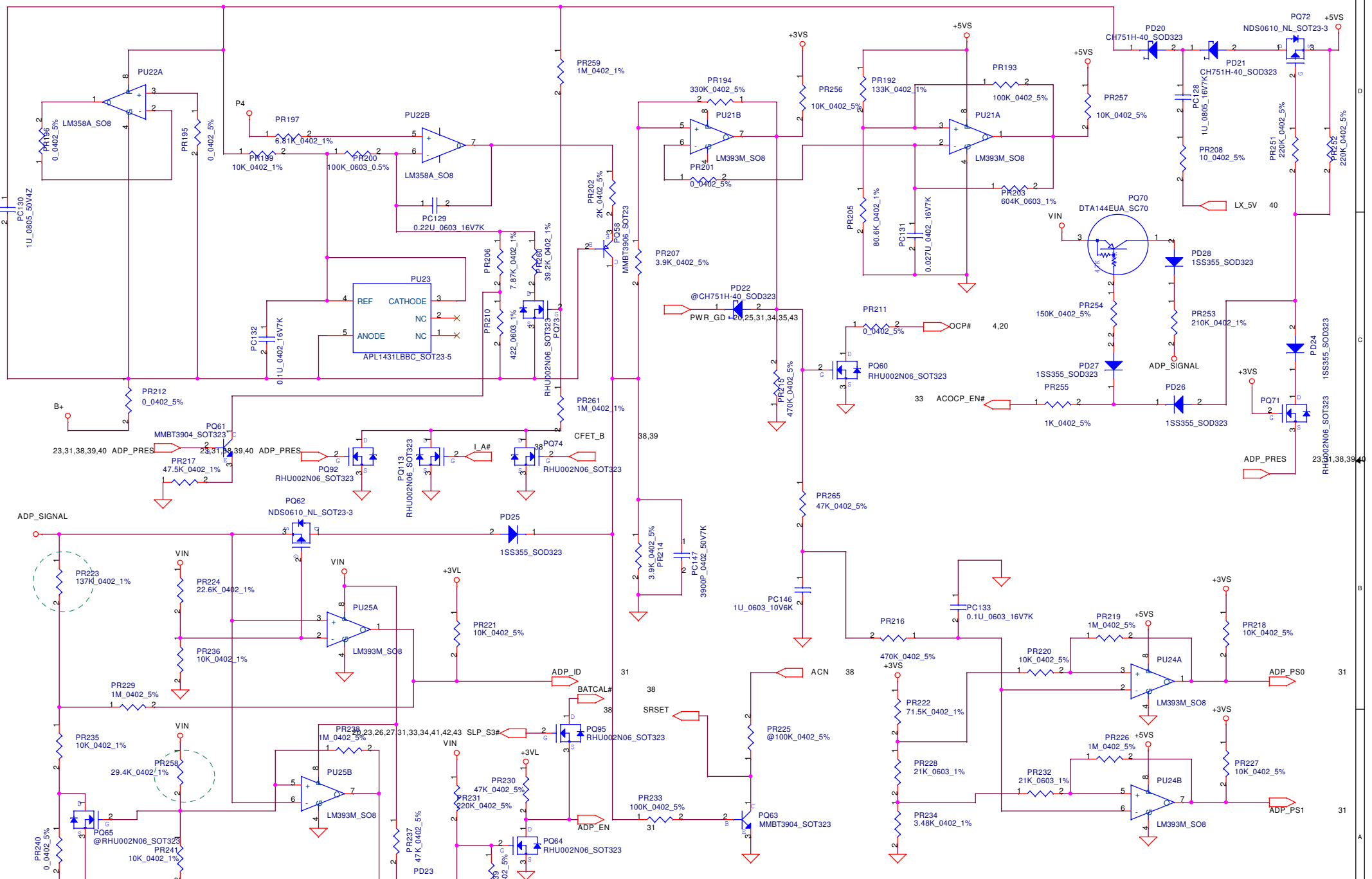
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Issued Date	2005/03/10	Deciphered Date	2006/03/10			Title	
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PR179, PR180 are for test need when M/B is without CPU
 R1269, R1270 are same function with PR179, PR180
 Layout Note: Use 27.4 Ohm (PR318, PR319) routing for Vssense and Vccsense

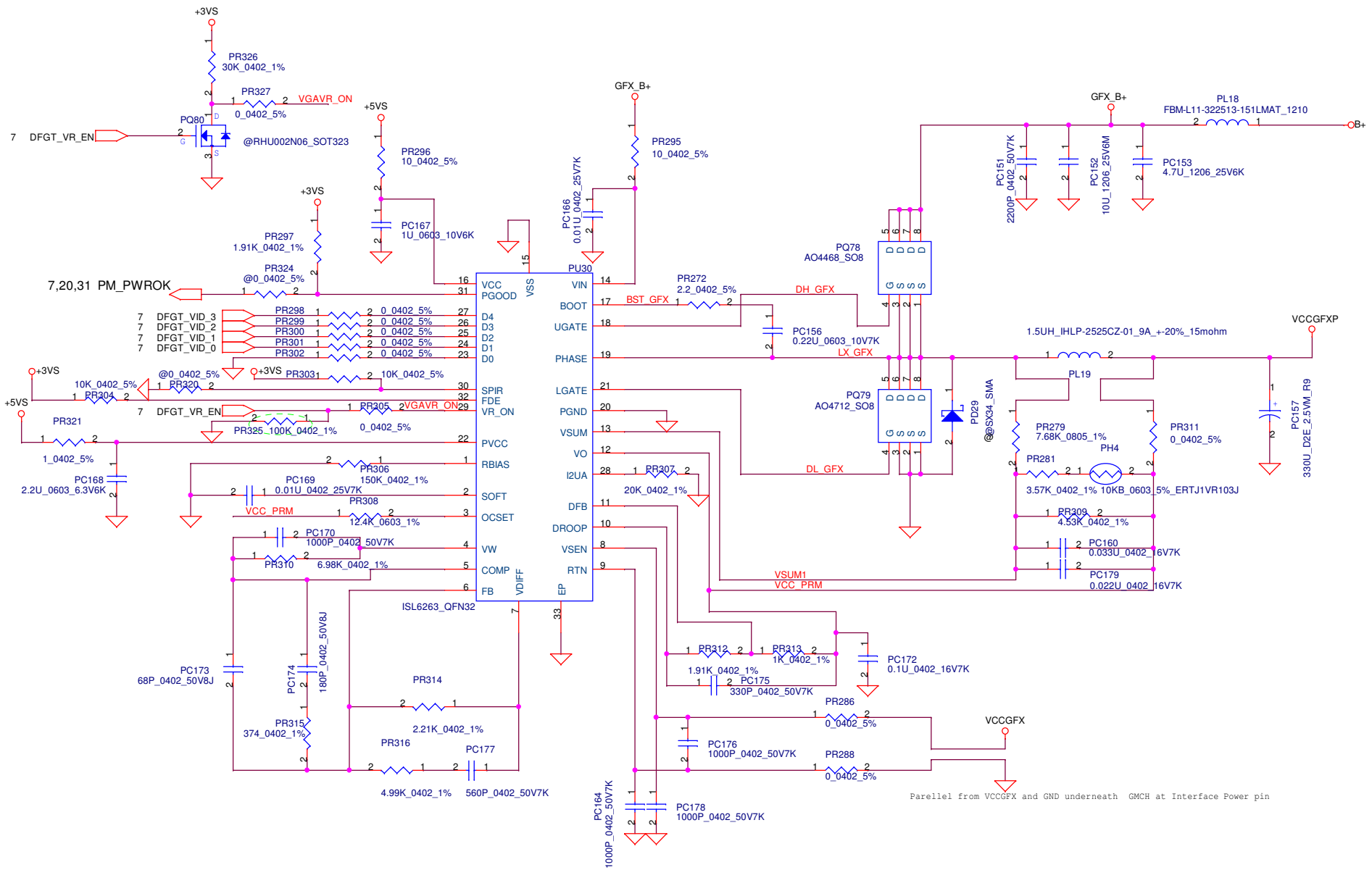
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title
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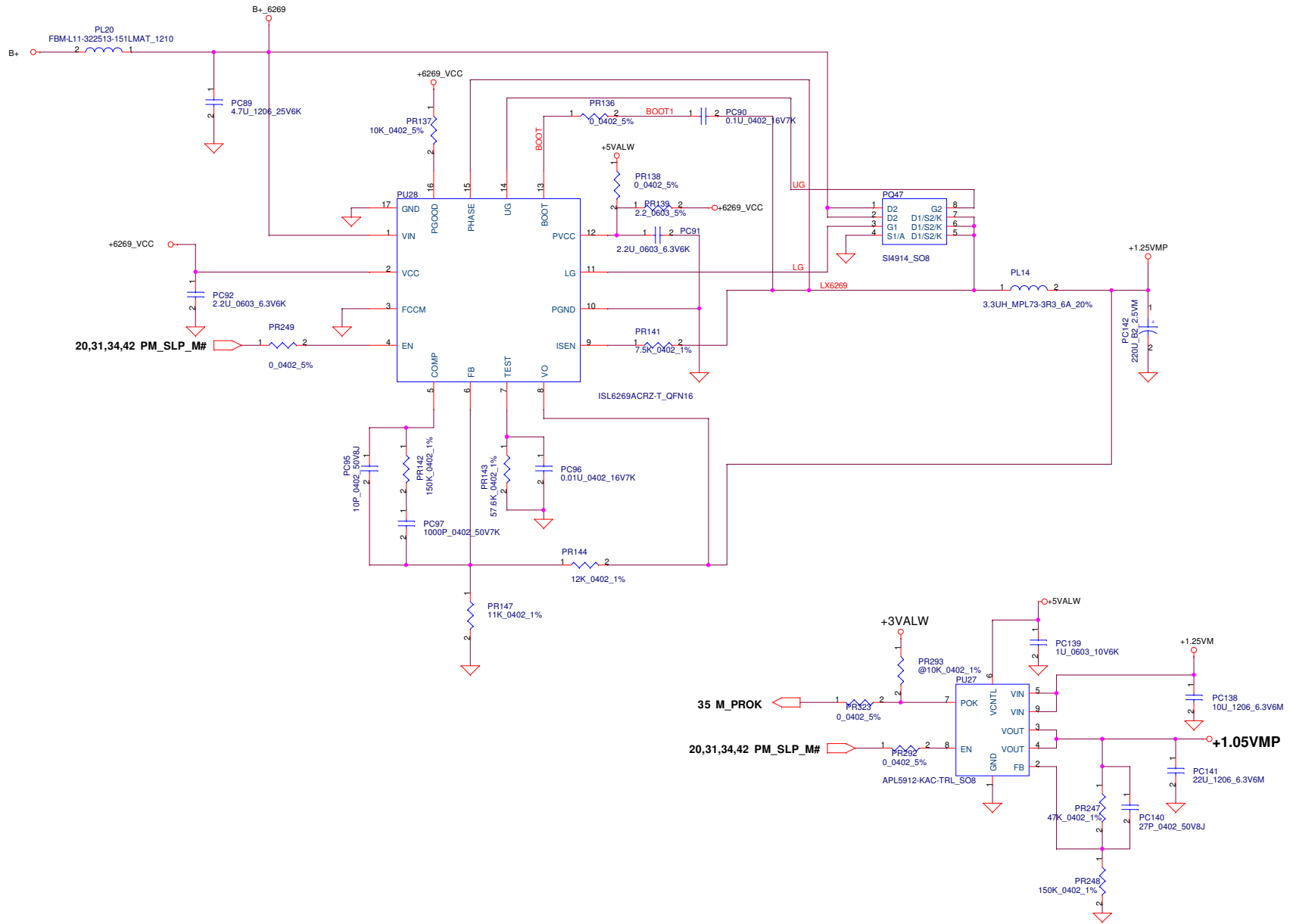
2005.8.20

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ADP_OCP		
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Size	Document Number	Date		Sheet	Rev
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Version Change List (P. I. R, List) for Power Circuit (1)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	Page42	1.8V/0.9V	3/9/2006	HP RL	Power Sequence	No install PR131 and install PR132 Change SLP_S5# at PR134.1 to SLP_S4# No install PR133 and install PR134 Add a 0 ohm resistor PR317 (no stuff) on M_PWROK	DB
2	Page45	VCCGFX	3/9/2006	Compal	MAX8776 VID table can't meet Intel VID SPEC	Change VCCGFX IC solution from MAX8776 to ISL6263	DB
3	Page43	CPU_CORE	3/10/2006	HP RL		Add 27.4 ohm pull-down (no stuff) on VCCSENSE & VSSSENSE near VR	DB
4	Page46	1.25VM/1.05VM	3/9/2006	HP RL	M_PWROK	Add a 0 ohm resistor PR323 (install) on M_PWROK change PR293 pin1 to +3VL	DB
5	Page46	1.25VM/1.05VM	4/10/2006	Compal	Correct 1.25VM voltage setting	Change PR144 to 12K and PR147 to 11K.	DB1-A
6	Page45	VCCGFX	4/10/2006	Compal	Power Sequence	Add a 0ohm PR324 (no stuff) on PM_PWROK	DB1-A
7	Page45	VCCGFX	4/24/2006	Compal	In S3 state, DFGT_VR_EN will no be actively driven, it is better to have a pull down resistor on DFGT_VR_EN.	Add a 30Kohm PR325	DB1-A
8	Page42	1.8V/0.9V	5/15/2006	HP MJ	Power Sequence	Change 1.5S to 1.8V in page 42 at pin 23 (VLDOIN)	DB1-B
9	Page46	1.25VM/1.05VM	5/15/2006	HP MJ	Power Good	Add PU34	DB2
10	Page38	Charge	5/15/2006	compal	For reducing charge temperture.	Change PL5 from 8.2uh MPL73-8R2 to 10UH_PCMB104T-100 Change PR28 from 0.015_2512 to 0.015_1206	DB2
11	Page43	CPU_CORE	6/5/2006	HP MJ	Power Sequence	investigate that SLP_S3# connect VR_ON and PM_POK connect PGD_IN	DB2
12	Page41	VCCP&1.5VS	6/5/2006	compal	Swap +1.05V_VCCP and +1.5VS location for improving power plane.	Change PR107 from 100k to 10K,PR111 from 10K to 100K.	DB2
13	Page37,38,44		6/22/2006	HP MJ	Chimay support for new battery cell chemistries	P38 : Remove PR52, PR38, PR41, PR53, P09 P39 :remove PR262, PR263, PR264, PR76, PQ75, PQ76, PQ32 P37: Add P081~P091 PR329~PR341,PD32~PD36 P38 :Add PD37 P44 :Add PQ92,PD38,PD39	DB2
14	Page41	2.5VALW/1.5VS /1.05VCCP	8/17/2006	HP MJ	For sequence fine tune	Add PC181 but not be installed	SI
15	Page43	CPU_CORE	8/17/2006	HP RL	Add 68ohm pull up to +VCCP at PU19.4 per Intel DG1.0 sec. 4.4.1.3 Figure 50	Add PR345 as 68ohm between +VCCP and PU19.4	SI
16	Page44	ADP_OCP	11/08/2006	HP RL	Identify 65W adapter as full adapter	Change PR223 from 180K to 182K, PR258 from 29.4K to 22.6K	SI2
17	Page43	CPU_CORE	11/08/2006	compal	For EMI concern, add snabber	Add PR349 and PR347 as 4.7ohm, Add PC183 and PC182 as 680pF Change boost resistor (PR148 and PR157)from 0 to 2 ohm	SI2
18	Page38	Charge	11/08/2006	compal	Base on "Energy STAR" spec, reduce S5 and S3 power consumption (AC mode)	Uninstall PQ11	SI2
19	Page42	1.8V/0.9V	11/13/2006	HP	Add PM_SLP_M# sequence	Add PR387	SI2

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Issued Date	2005/03/01	Deciphered Date	2006/03/01	PWR PIR Sheet (1)	
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Version Change List (P. I. R. List) for Power Circuit (2)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
20	Page43	CPU_CORE	2/28/2007	Compal	Fine tune CPU CORE solution	No install PC122 Change PR185 from 3K to 1.96K Change PR190 from 6.19K to 6.34K	MV
21	Page44	ADP_OCP	2/28/2007	HP	System identity	Change PR223 from 182K to 137K Change PR258 from 22.6K to 29.4K	MV
22	Page38	Charger	3/1/2007	Compal	Reserve circuit for testing Energy STAR	Reserve PR397, PR398, PR399 and PQ131 Add PR396 as 0 ohm.	MV

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For DBI-B

<2006.03.29>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Reserve resistors on Debug ports	30	Add R170, R201, R202 and CLR3 jopen	0.2
2	SATA footprint is wrong	SATA connector's PCB footprint is wrong	22	change to OCTEK_SAT-22DD1G_22P	0.2

<2006.04.10>

1		follow Intel suggestion for XDP_DBRESET#	4, 20	R243 no install and R1589 install (XDP_DBRESET#)	0.2
2		Change component' s footprint for supply and layout easy	07	R1443 change from 0603 size to 0402	0.2
3		+VCC_PEG should be 1.05V instead of 1.25V for Creatline	10	R1465 install and R1467 no install	0.2
4		Monitor NB cracked pins	11	Add Q118, Q119, Q120, Q121, Q122, Q123, R1700, R1701, R1702 R1703, R1704, R1705, R1706, R1707, R1708, R1709, R1710, R1711	0.2
5		Monitor SB cracked pins	21	Add Q124, Q125, Q126, Q127, R1716, R1712, R1713, R1717 R1718, R1714, R1719, R1715	0.2
6	SPI BIOS can not flash.	For SPI BIOS flash issue	23	Delete Q102, R178 and Q115 Q102 pin1 short to pin3-->+3VM connect to +3VM_LAN PLT_RST# connect to PM_LAN_EN	0.2

<2006.04.21>

1		For LAN link status	18	change PCI_PIRQG to LED_LINK_LAN# and add R1727 0 ohm	0.2
2		For LAN active status	23	Add LED_ACT_LAN# this net	0.2
3		For ADP_PRES new design	20	add D68 and disconnect LED_LINK_LAN#	0.2
4		For LAN net name	19	change net name from LAN_RST to LAN_RSTSYNC change net name from LANLINK_STATUS# to LED_LINK_LAN#	0.2
5		For Compal Fan design	4	change Fan connector pin 1 and pin4	0.2

<2006.04.24>

1		For NIC RST	20 35	change net name from PM_LAN_EN to LAN_RST# Add a Resistor R1722(0 ohm), R1732, R1731(no install) change net name from PGD_IN to LAN_RST# Install C991, C990, C992, D60, R1350 Adjust C990 and R1350 value to 0.1uF and 100K ohm.	0.2
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For DBI-C

<2006.05.15>

1	System can not power on	For RTC CLK	19	add R1733	0.3
2	LAN can not work	For LAN function	23	modify LAN relative schematics	0.3
3		For PWR OK	35	Change R124 pin2's voltage from 0.9v to 1.24VREF Change R1732 pin2's voltage from 3VM to 3VM_LAN	0.3

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For DB2
<2006.05.29>

<2006.06.12>

<2006.06.14>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Add new feature (Kill switch)	22	Add R1736, jp53, R1737 and Q129	0.4
2		modify CRACK_GPIO28 circuits	11 21	delete R1700, R1707, R1705-->NB delete R1712, R1713, R1714-->SB	0.4
3		Change pull up for CK505 strapping	15	on R1108, R1690, R1245 from +3.3VM_CK505 to +3VS	0.4
4		for LAN IVRI thermal protect and limit current.	23	add R1	0.4
5		Add resisters for GPI pins floating	20	addR3, R6, R9, R11, R15	0.4
6		Change KBC RST pin	31	change from PLT_RST# to NCPI_RST#	0.4
7		Change to USB port assignments	28	Move Dock1 from USB8 to USB7 and move WWAN from USB3 to USB8	0.4
1		New PCIE assignments	20	Updated Changes: PCie - port1 = Free PCie - port2 = WLAN PCie - port3 = Free PCie - port4 = Robson PCie - port5 = Docking PCie - port6 = Intel LOM is fixed at this location	
2		Change SW design to Capsense SW.	32	Change SW Connector JP18 type and relative circuits	
3		Add new feature (Robson)	15	Add R5, R13 on SRC6 and R14, R17 on CLKREQ_E#	
4		Change GPIO pins	18 20	change GPIO4(SB) from LED_LINK_LAN# to PCI_PIRQG# change GPIO1(SB) from CB_PE# to LANLINK_STATUS#(i)	
5		Change HP debug port power source	30	Add R1740, R1741 and connect to +3vs	
6		Change KBC 1070 GPIO pins	31	CRACK_GPIO28 from GPIO28(KBC) to GPIO8(KBC) add R155, R156, R18, R20 and their signals connect to JP18 Add Cap_INT on GPIO25(KBC)	
7		change WALN power source	25	change from +3valw to +3vM	
8		Change U75 power source for LAN function	23	U75 should be powered by V3.3M instead of 1.8VM	
9		Change USB power switch control pin	28	From S5 to S4_STATE# to control USB power	
10		For support 2GB DIMMs	7 13, 14	BJ29 pin and BE24 pin (NB)connect to DDR DIMMA, B(A14 pin)	
11		For Crestline sightings requires	7	add a 0ohm R1759 on pin N20(NB).	
1		Modify PWROK circuits for All power source check	35	Change R1732 pin2's voltage from 3VM to 3VM_LAN	

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For DB2

<2006.06.19>

<2006.06.20>

<2006.06.21>

<2006.06.22>

<2006.06.23>

<2006.07.18>

<2006.07.31>

<2006.08.09>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Add Intel RSMRST circuit	31	Add R1749, R1750, R1751 and Q131, D68	0.4
2		Change resister value meet G-vendor suggestion	25	change R1359, R1362 VALUE	0.4
3		Kill switch design change	22	change R1736 pin2 contact to +RTCVCC	0.4
1		Change PWR_OK circuit	35	delete R157 and PGD_IN net	0.4
2		Reserve resister on HDA_RST#_MDC	32	Reserve R1753 0 ohm	0.4
3		delete two components on Debug part 21	30	delete R1740, R1741	0.4
4		Control Audio volume when boot	28	add EAPD link to KBC GPIO31	0.4
5		Add new feature -->Robson	25	Add and change JP13 pin assignment for Robson	
6		Fix LAN power circuit to IVRD	23	Delete R1 (0.68ohm), R1624, and install R1734	
7		improve LAN Power ripple	23	Add C1364, C1363 on +3V_LAN and +1.8VM_LAN	
8		improve DVI issue	16	Add SDVO_CLK/Data net name to NB SDVO_CLK/ Data pins	
1		Change USB control signal	28	Change control signal name to S4_STATE and add Q132	
2		Isolate power noise for NB	10	change R1453, R1456 from Resister to bead	
1		Hold RESET to modem	32	Install R1753	
2		Enable WLAN for AMT	25	Install R194, R195 and R197	
3		Improve TV-out signals and fix TV garbage issue	10	change R175, R176, R177 from150 ohm to 75 ohm	
4		follow Intel Demo circuit for XDP	28	Change pull up R1589 value for XDP_DBRESET# from 10K to 1K	
1		Chnage Fan Connector pins' count	4	Chnage JP8 from 4pins to 3 pins.	
2		delete MDC disable reserve part	32	delete U43B	
3		Implement STB_LED# driver	31	add U43B	
4		Modify power OK circuit	35	add Q134, Q133, R39, C2 Delete R286, R127, C30, R117, R35, R34, R118, U79	
5		For Non-link part (INV_PWM from KBC to LCD)	17	delete R131	
6		Delete Repeated function circuit	11	Delete D21,R520	
1		For C-status	20	Install R179	0.5
2		For discharge issue	34	Change discharge circuit net from PM_SLP_M# to LAN_WOL_EN#	0.5
3		HP request	31	Install R155,R156 and un-install R127,R157	0.5
1		Do not support wake on WWAN card	25	Install R1383 and no install R1382	0.5
1		Add anti-pop circuit	26	Add anti-pop circuit	0.5
2		Eliminate glitch	20	Add R1767, no install R434, C1365, R1757	0.5

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Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
3		HP request	32	Connect JP18 pin1 to +3VL, pin2 to +3VS	0.5
4		EMI request	24	Add D72 and D73 for EMI request	0.5
5		Add MAX9511	9, 16, 33	Add MAX9511	0.5
<2006.08.11> 1		For OTS 214499	31	Add U82	0.5
2		HP request	25	No install R1418, R1358, R1359, R1360	0.5
3		HP request	25	JP44 PIN37, 43 connected to GND JP44 PIN39, 41 connected to +3VS	0.5
4		HP request	25	Isolate SLOT power from SYSTEM power.	0.5
5		HP request	25	Remove 1.5V from WWAN slot	0.5
6		HP request	25	Install schottkey diode D74	0.5
7		SIM I/O pull-up footprint is requested.	25	Add R1780 and no install	0.5
<2006.08.21> 1		HP request	25	change +3VS to +3VS_WLAN ,Change +3VS on R1383.2 to +3VS_WWAN Change +3VS on R1071.1 and R1703.1 to +3VS_WWAN	0.5
2		HP request	9	Changes for MAX9511	0.5
3		HP request	25	Remove SW1, C986, R521, D65, R200	0.5
4		HP request	30	Need to connect SPI_HOLD#_0 and SPI_HOLD#_1 together.	0.5
5		HP request	31	Item 191, 192, 193	0.5
6		HP request	25	Install R1363 and NO INSTALL R1364	0.5
<2006.08.23> 1		HP request	19	Move D75 to SB and delete R1782	0.5
2		HP request	25	Add 1394 signals on M/B	0.5
<2006.08.25> 1		HP request	25	Add a 0 ohm 0805 on 1.5VS to WLAN mini card connector	0.5
2			20	Swap GPIO01 and GPIO11 connections.	0.5
<2006.08.29> 1		OTS issue	32	Change JP18 pin8 to WL_BLUE_LED#	0.5
<2006.08.30> 1			16	Change R142, R144 to 3.9K ohm	0.5

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Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
3		Intel update	7	Add R1786,R1787,R1788,R1789	0.5
<2006.09.01> 1		HP request	32	Remove R23 and NPCI_RST# connection Remove PLT_RST# connection to R21.2 and connect GPIO28 from ICH8	0.5
<2006.09.04> 1		EMI request	28	Add R1790,R1791,R1792	0.5
<2006.09.06> 1		HP request	23	Change C1257 and C1359 to 10uF 0805	0.5
2		HP request	25	Remove R1412,1413,1414,1415,1416,1417	0.5
3		HP request	25	Remove R1418,1358,1353,1360	0.5
4		HP request	30	Add 0 ohm for SPI, R1793,1794,1795	0.5
<2006.10.13> 1		HP request (MAX9511 issue)	9,16,33	Remove MAX9511 from CRT circuit	0.6
2			11,21,31	No install BGA crack circuit	0.6
3			32	Change KB connector	0.6
<2006.10.31> 1			31	Change RSMRST circuit, add R1796	0.6
<2006.11.01> 1		Auto power on issue	20	Auto power on issue(add Q140, R1797)	0.6
2		1394 issue	28	Modify EMI request	0.6
<2006.11.03> 1		HP request	32	Connect JP32 pin2 to +3VS	0.6
<2006.11.07> 1		HP request	31	Install R1784, no install R1783	0.6
2		Intel document	10	Change R1471 to 100 ohm	0.6
<2006.11.09> 1		Layout space	22	Remove kensinton circuit	0.6
<2006.11.11> 1		HP request	15	Add CLRP4 and CLRP5 for FSB 667/800 select	0.6
<2006.11.13> 1		HP request	35	Tie R1732.2 to 3VM instead of 3VM_LAN	0.6
2		HP request	24	Change R1639 to 1.4K based on Intel WW44	0.6
3		HP request	4	Add resistors in series with the diode signals going to ADM1032.	0.6
4		HP request	31	Eliminate glitch circuit, install R1483 and no install R1484	0.6

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<2006.11.16> 1		HP request	10	Change R1468, R1472, R1473 to bead	0.6
2		HP request	24	Change R1639 to 1.87K ohm	0.6
3		HP request	27	Change R261 and R253 to 56.2 ohms 1%.	0.6
<2006.11.28> 1		HP request	23	Install Q102,R1730, no install R1612,Q104,Q105.	0.6
2		HP request	7	Install R1739	0.6
<2006.12.19> 1		HP request	35	Add Schmitt Trigger to eliminate glitch	0.7
2		HP request	31	Install R1646,C75	0.7
3		HP request	19	Update GPIO33 circuit	0.7
<2006.12.26> 1		HP request	7	Add C and no install	0.7
2		Chrontel request	16	Add C for DVI I2C	0.7
<2007.01.02> 1		ME request	25	Change JP50 for rewrok	0.7
<2007.01.04> 1		Intel request	23	Add R1804	0.7
2		ME request	32	Change JP20 to FFC connector	0.7
<2007.01.08> 1		EMI request	33	Add R1805,R1806 0 ohm, reserve C1372, C1373	0.7
<2007.01.10> 1		HP request	31	R1783 connected to +3VL	0.7
<2007.01.13> 1		Compal request	35	Change LMV331 to LM393, delete R124 and C27	0.7
<2007.01.15> 1		HP request	26	R370, R369 - change from 4.7k to 6.04k R374, R375 - change from 4.7k to 2.00k	0.7
<2007.01.16> 1		HP request	25	Connected R1780.2 to UIM_PWR	0.7
<2007.01.17> 1		HP request	30	Add pad for BIOS debug	0.7
<2007.01.19> 1		HP request	34	Add R1807 and no stuff	0.7
2		CRT wavy issue	10	Add C1374 for CRT wavy issue	0.7
<2007.02.09> 1		CRT wavy issue	17	Add 10uFX2 for CRT wavy issue (C586, C1376)	0.9

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<2007.02.09> 2		HP request	30	Add Q142 for FPR	0.9
<2007.02.16> 1		+3VM_LAN leakage	20	Add U83 for auto boot and leakage issue	0.9
2		Compal request	15	Delete CLPR4, CLRP5	0.9
3		HP request	34	Install R1807 and non install R630	0.9
4		LVDS sequence issue	17	Change C28 to 0.1uF	0.9
5		HP request	31	Add R1809 to GND	0.9
<2007.02.26> 1		Safety request	33	Change RJ11 connector	0.9
<2007.02.27> 1		HP request	27	Change R261 and R253 to 60.4 ohm	0.9
2		HP request	35	Move R1803	0.9
<2007.02.28> 1		HP request	11,21	Change to +3VL	0.9
<2007.03.01> 1		HP request	10	CRT wavy issue -- add C1374	0.9
2		HP request	15	Add CAP for WWAN issue	0.9

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