

Compal confidential

Schematics Document

Mobile Merom uFCPGA with Satna Rosa Platform

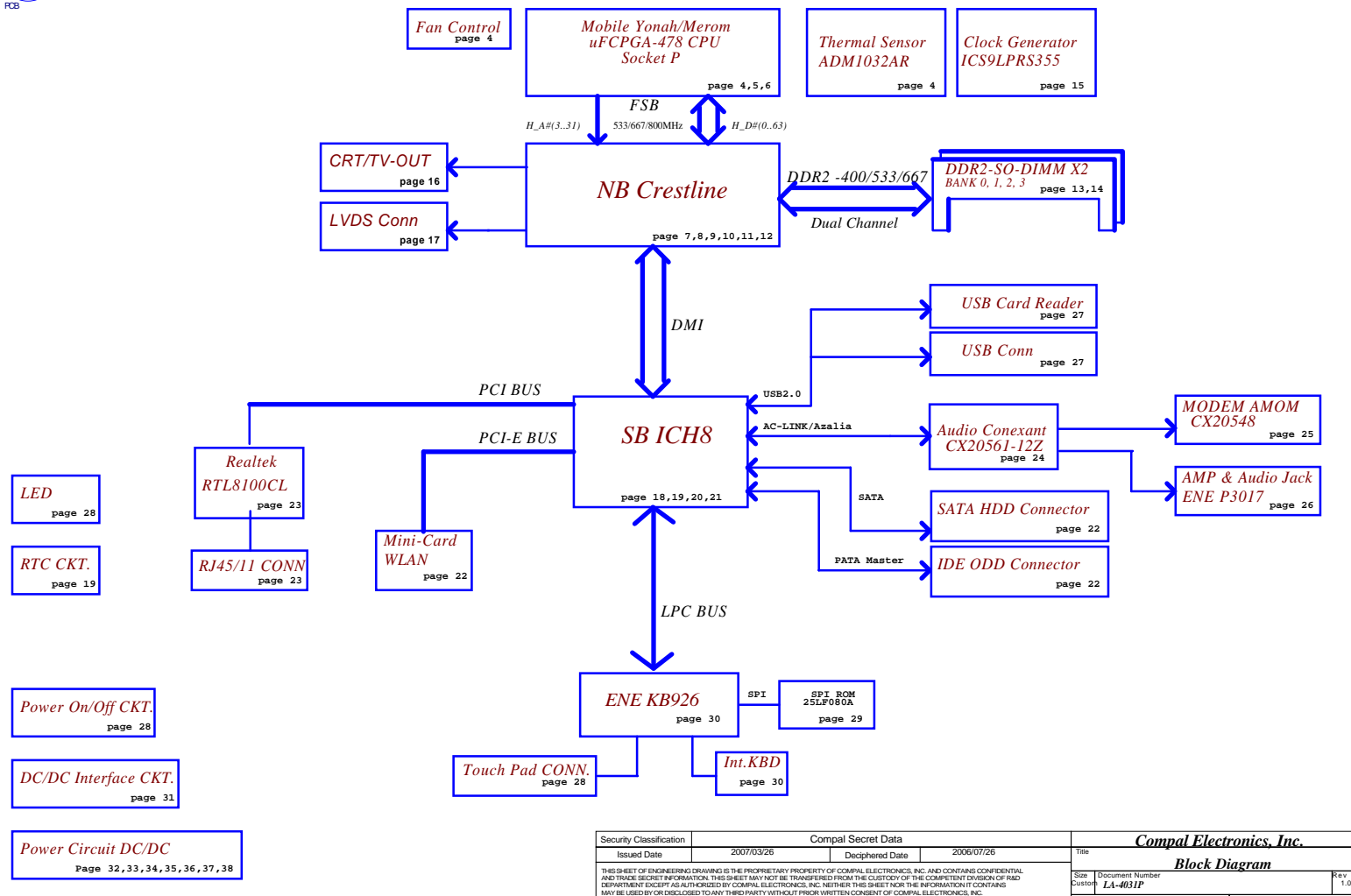
2007-07-30

REV: 0.2

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Spartan 1.1 (Merom +Crestline+ICH8)

ZZZ
PCB



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Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



: means Digital Ground



: means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD17	0	A

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

SMBUS Control Table

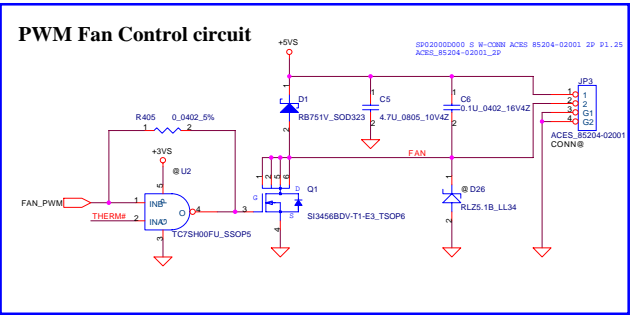
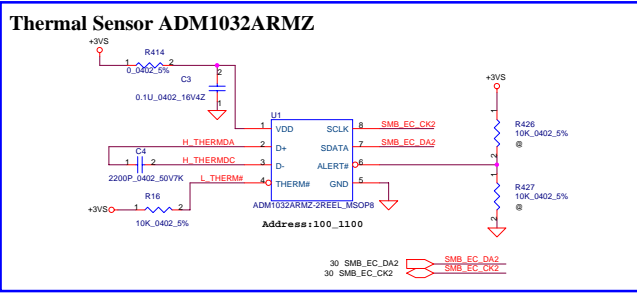
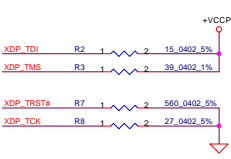
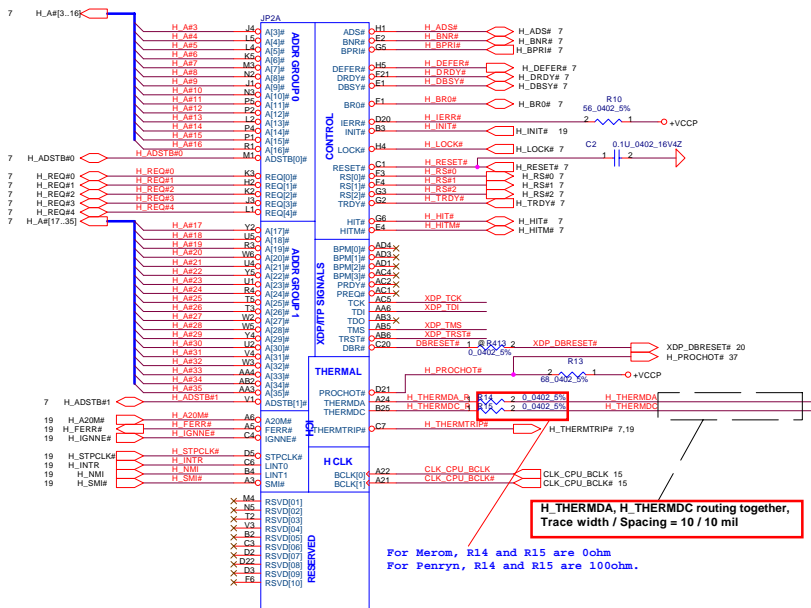
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADM1032	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB925	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CR_DAT1	ICH8	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Crestline	X	X	X	X	X	X	X	V

BOM: 43152432L03(965GM) & 43152432L04(960GML) with card reader

BOM: 43152432L01(965GM) & 43152432L02(960GML) without card reader

Jump-Short: PJP?

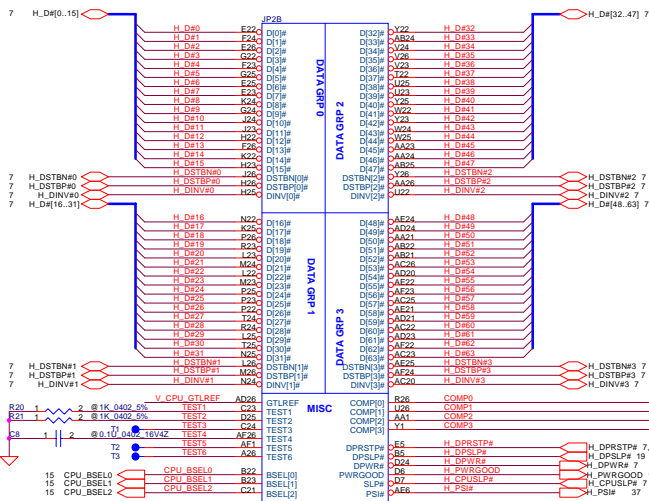
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**H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil**

For Merom, R14 and R15 are 0ohm
For Penryn, R14 and R15 are 100ohm.

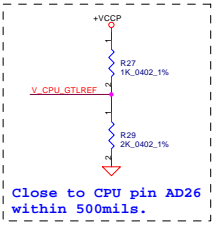
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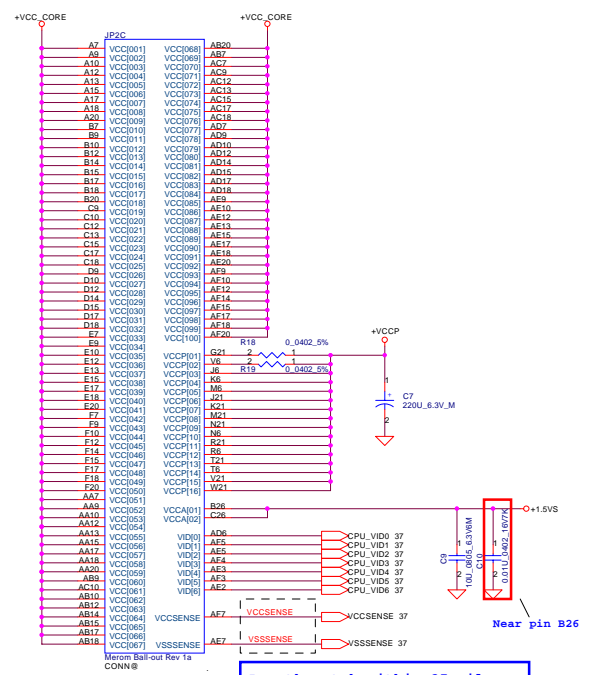
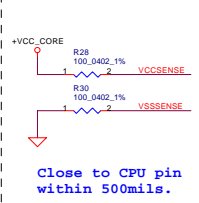
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0, 2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

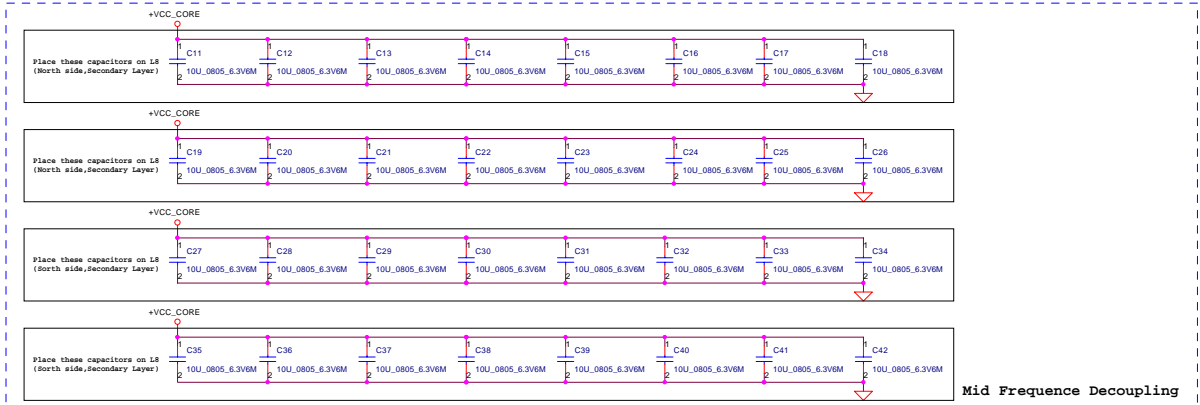


Length match within 25 mils. The trace width/space/other is 20/7/25.



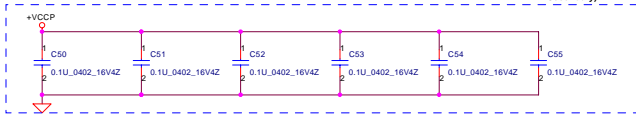
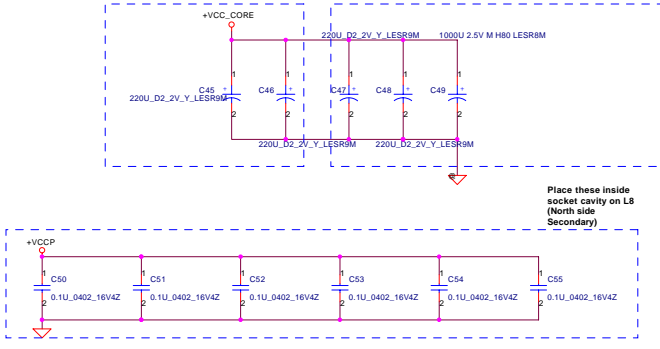
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JP2D			
A4	VSS1001	VSS1080	P6
A5	VSS1002	VSS1083	P21
A6	VSS1003	VSS1084	P22
A14	VSS1004	VSS1085	B2
A16	VSS1005	VSS1086	B22
A19	VSS1006	VSS1087	B22
A22	VSS1007	VSS1088	T1
AF2	VSS1008	VSS1089	T1
BB	VSS1009	VSS1090	T4
BB	VSS1010	VSS1091	T7
B11	VSS1011	VSS1092	T26
B13	VSS1012	VSS1093	T17
B18	VSS1013	VSS1094	U6
B19	VSS1014	VSS1095	U2
B21	VSS1015	VSS1096	U24
C2	VSS1016	VSS1097	U5
C4	VSS1017	VSS1098	U2
C8	VSS1018	VSS1099	U22
C11	VSS1019	VSS1100	U25
C14	VSS1020	VSS1101	W1
C16	VSS1021	VSS1102	W1
C19	VSS1022	VSS1103	W2
C2	VSS1023	VSS1104	W2
C22	VSS1024	VSS1105	X3
C25	VSS1025	VSS1106	X6
D1	VSS1026	VSS1107	X2
D4	VSS1027	VSS1108	Y24
D8	VSS1028	VSS1109	Y2
D11	VSS1029	VSS1110	Y24
D13	VSS1030	VSS1111	Y8
D18	VSS1031	VSS1112	AA1
D19	VSS1032	VSS1113	AA4
D23	VSS1033	VSS1114	AA16
D28	VSS1034	VSS1115	AA19
E3	VSS1035	VSS1116	AA2
E8	VSS1036	VSS1117	AA25
E8	VSS1037	VSS1118	AB1
E11	VSS1038	VSS1119	AB4
E14	VSS1039	VSS1120	AB6
E16	VSS1040	VSS1121	AB11
E19	VSS1041	VSS1122	AB13
E21	VSS1042	VSS1123	AB16
E24	VSS1043	VSS1124	AB19
F4	VSS1044	VSS1125	AB3
F8	VSS1045	VSS1126	AB26
F11	VSS1046	VSS1127	AC6
F18	VSS1047	VSS1128	AC8
F19	VSS1048	VSS1129	AC11
F21	VSS1049	VSS1130	AC14
F2	VSS1050	VSS1131	AC16
F22	VSS1051	VSS1132	AC19
F25	VSS1052	VSS1133	AC21
G4	VSS1053	VSS1134	AC24
G9	VSS1054	VSS1135	AD2
G28	VSS1055	VSS1136	AD5
H8	VSS1056	VSS1137	AD8
H8	VSS1057	VSS1138	AD11
H21	VSS1058	VSS1139	AD13
H24	VSS1059	VSS1140	AD16
J2	VSS1060	VSS1141	AD19
J2	VSS1061	VSS1142	AD22
J22	VSS1062	VSS1143	AD25
K5	VSS1063	VSS1144	AE1
K1	VSS1064	VSS1145	AE4
K1	VSS1065	VSS1146	AE8
K4	VSS1066	VSS1147	AE11
K29	VSS1067	VSS1148	AE14
K28	VSS1068	VSS1149	AE16
L3	VSS1069	VSS1150	AE19
L6	VSS1070	VSS1151	AE23
L21	VSS1071	VSS1152	AE26
M2	VSS1072	VSS1153	AF
M5	VSS1073	VSS1154	AF8
M5	VSS1074	VSS1155	AF9
M22	VSS1075	VSS1156	AF11
M28	VSS1076	VSS1157	AF16
N1	VSS1077	VSS1158	AF19
N4	VSS1078	VSS1159	AF21
N23	VSS1079	VSS1160	AF25
N23	VSS1080	VSS1161	AF26
P1	VSS1081	VSS1162	AF26
P1	VSS1081	VSS1163	AF26

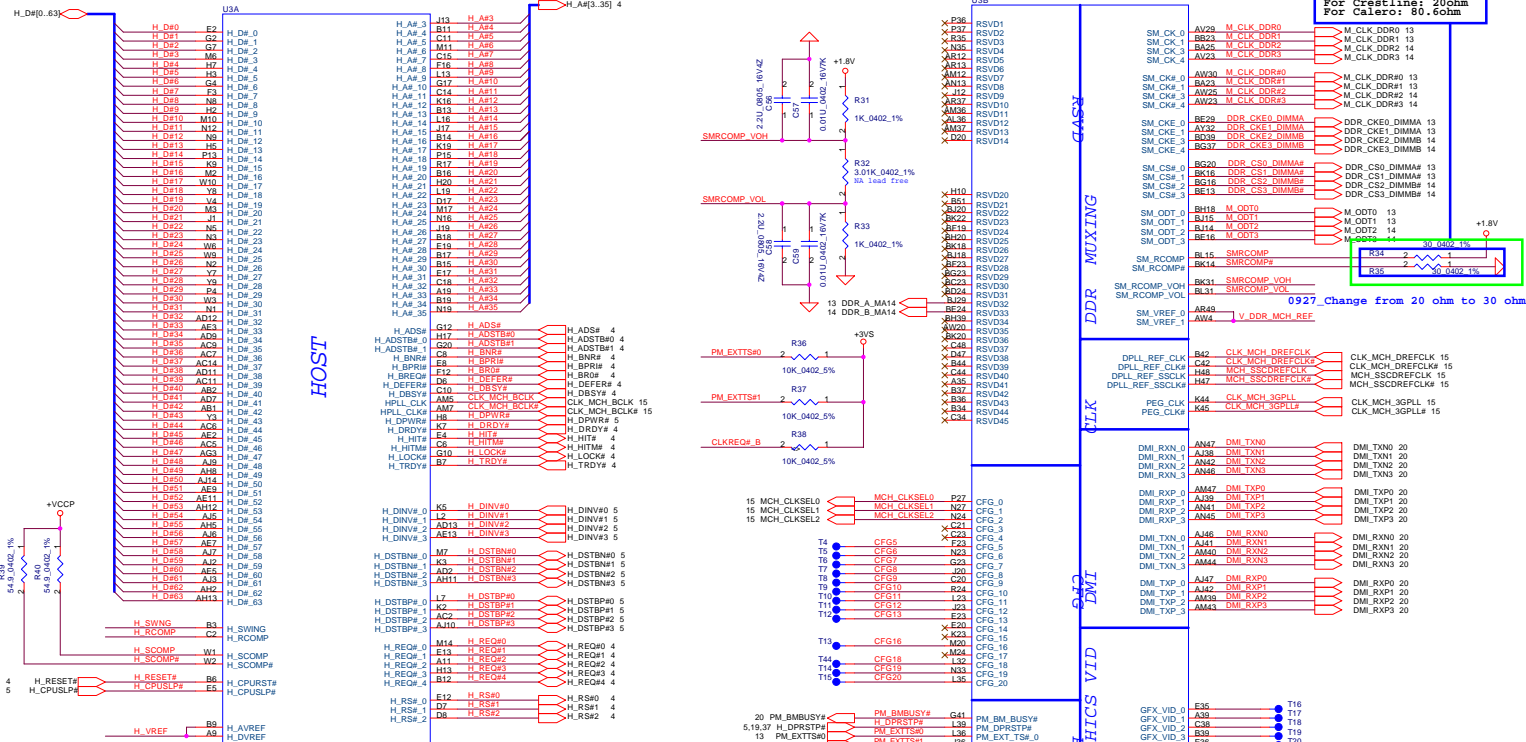


Mid Frequency Decoupling

Near CPU CORE regulator ESR <= 1.5m ohm Capacitor > 1980uF

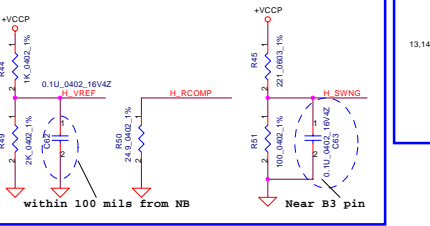


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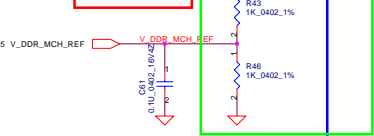


layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCMP / H_VREF / H_SWNG trace width and spacing is 10/20



Layout Note:
V_DDR_MCH_REF trace width and spacing is 20/20.

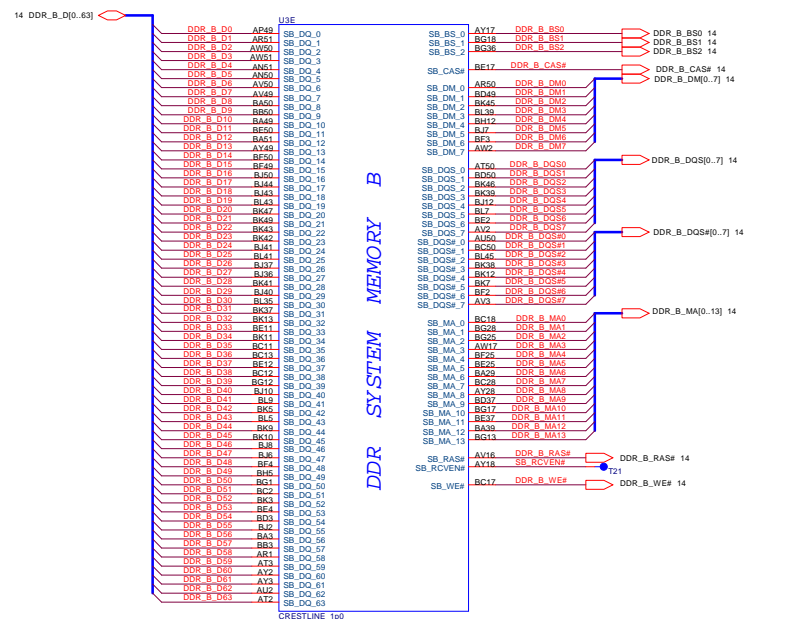
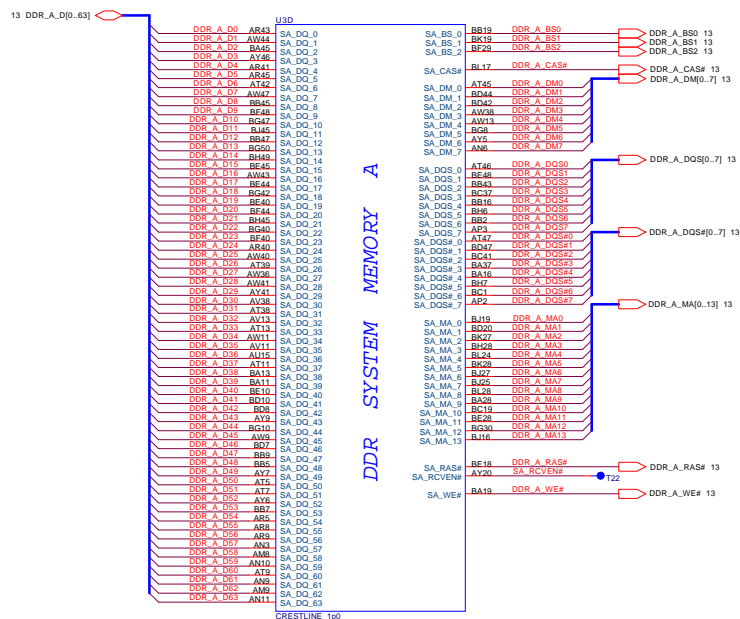


0925_Staff R43 and R46.

For Crestline: 20ohm
For Calero: 80.6ohm

0927_Change from 20 ohm to 30 ohm.

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CRESTLINE_1p0

CRESTLINE_1p0

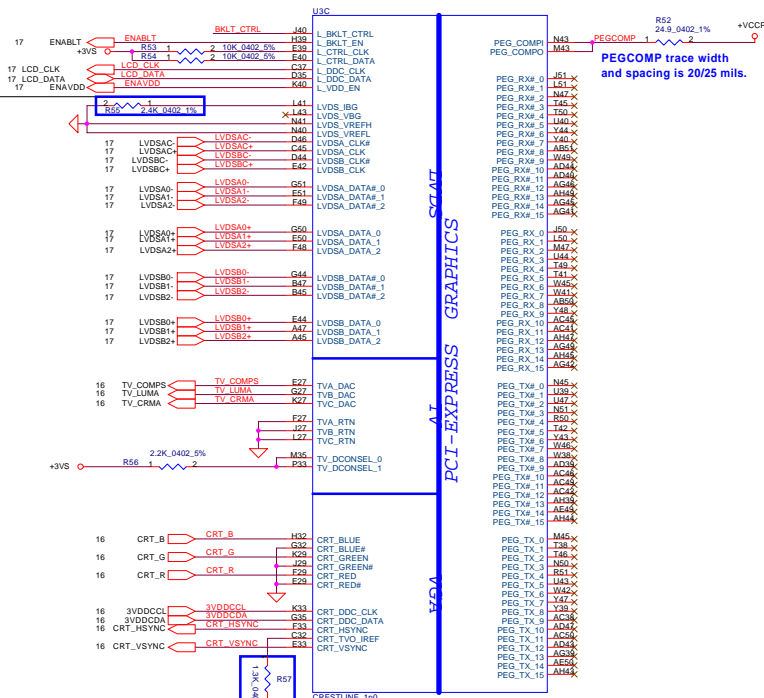
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Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIe)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

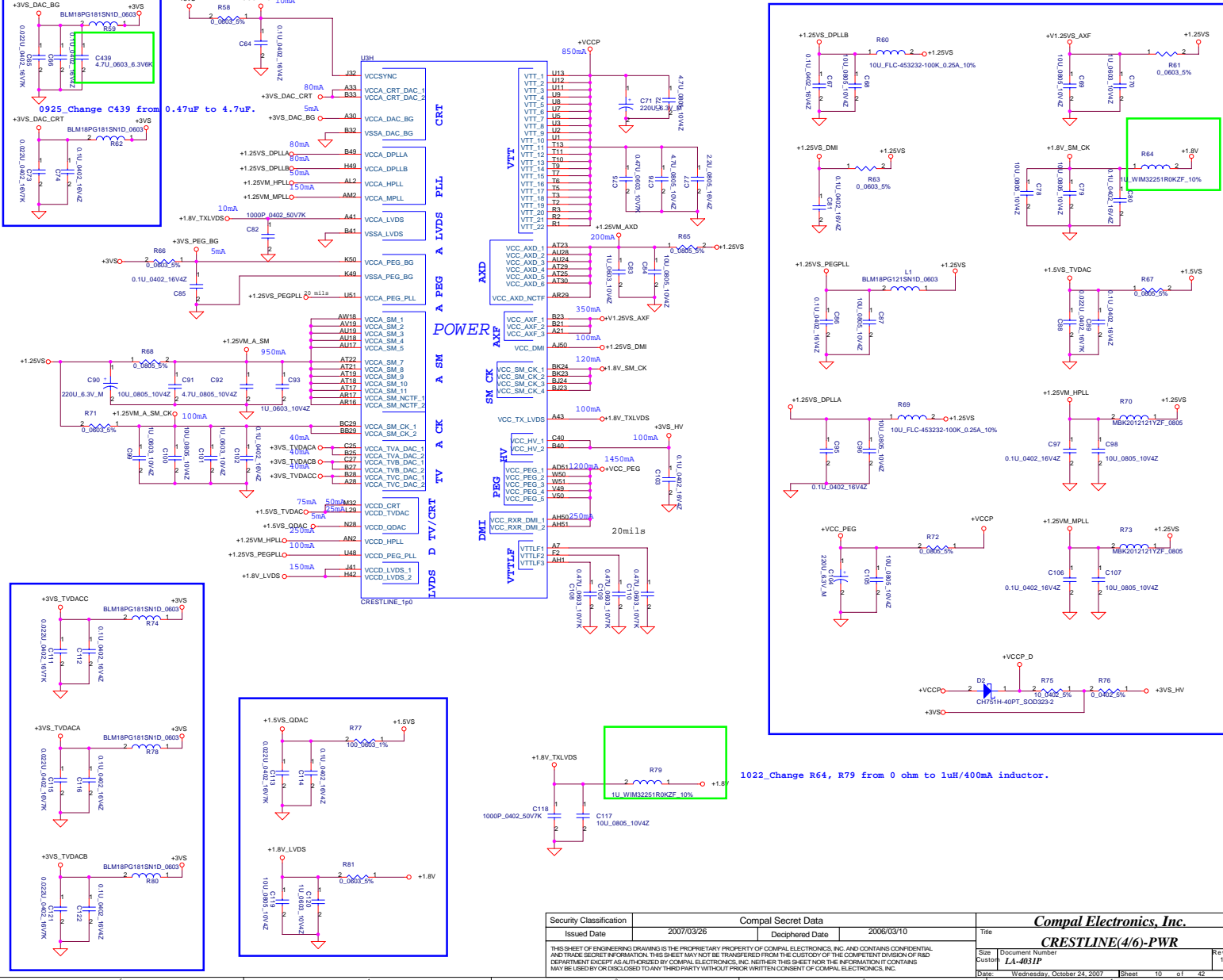
For Crestline: 2.4kohm
For Calero: 1.5kohm



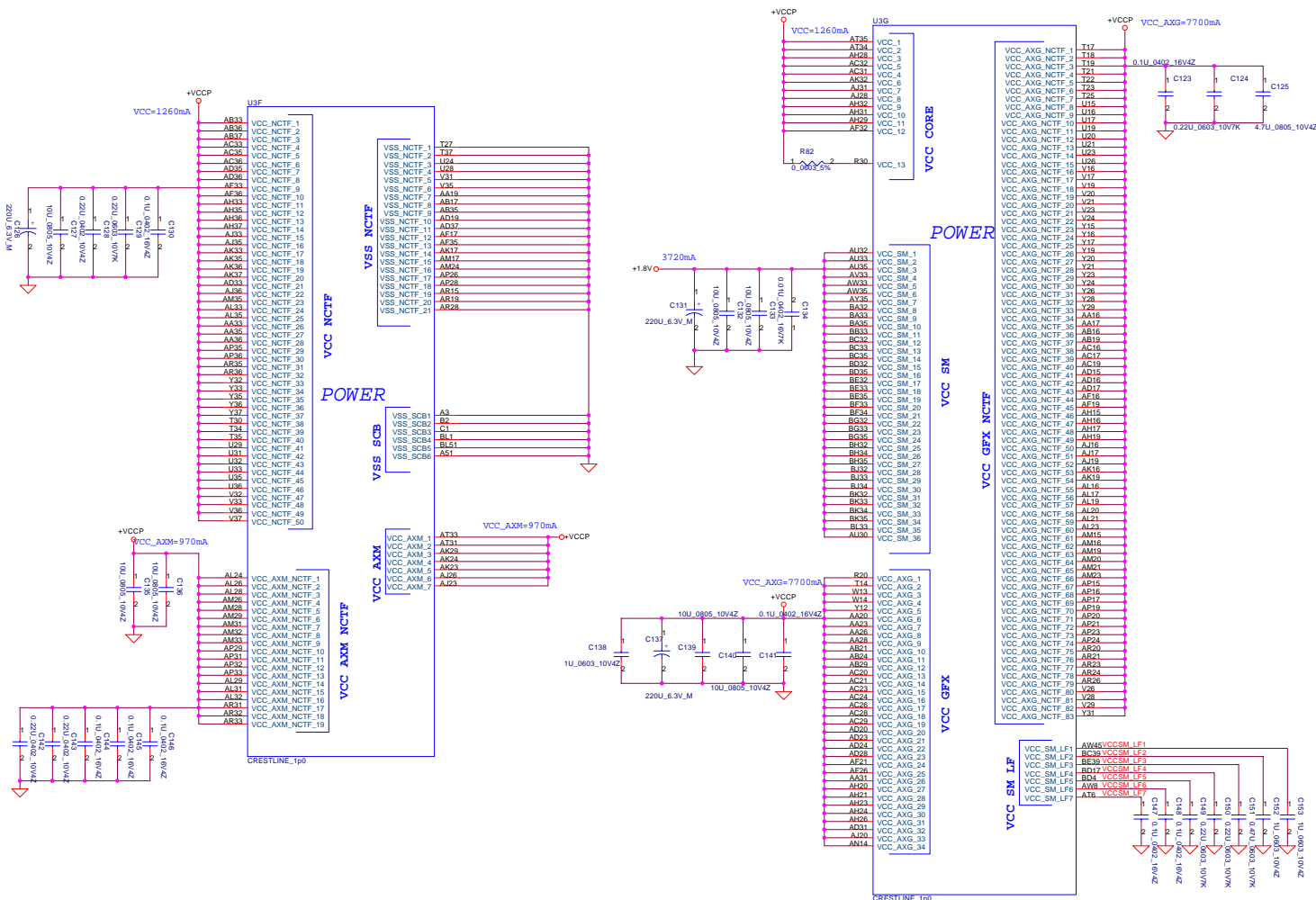
For Crestline: 1.3kohm
For Calero: 255ohm

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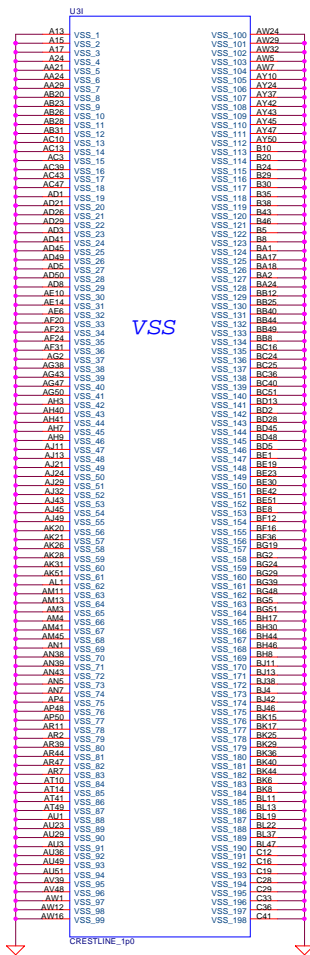
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CRESTLINE(3/6)-VGA/LVDS/TV



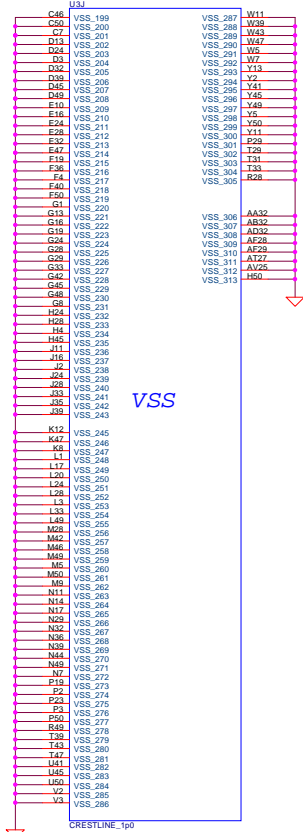
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VSS

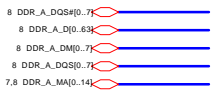


VSS

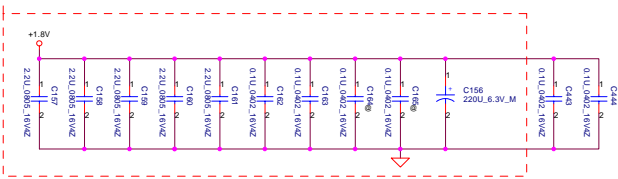
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CRESTLINE((6/6)-PWR/GND

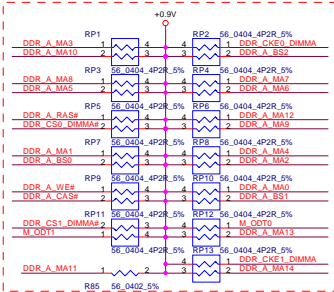
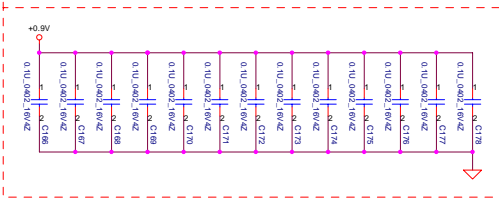
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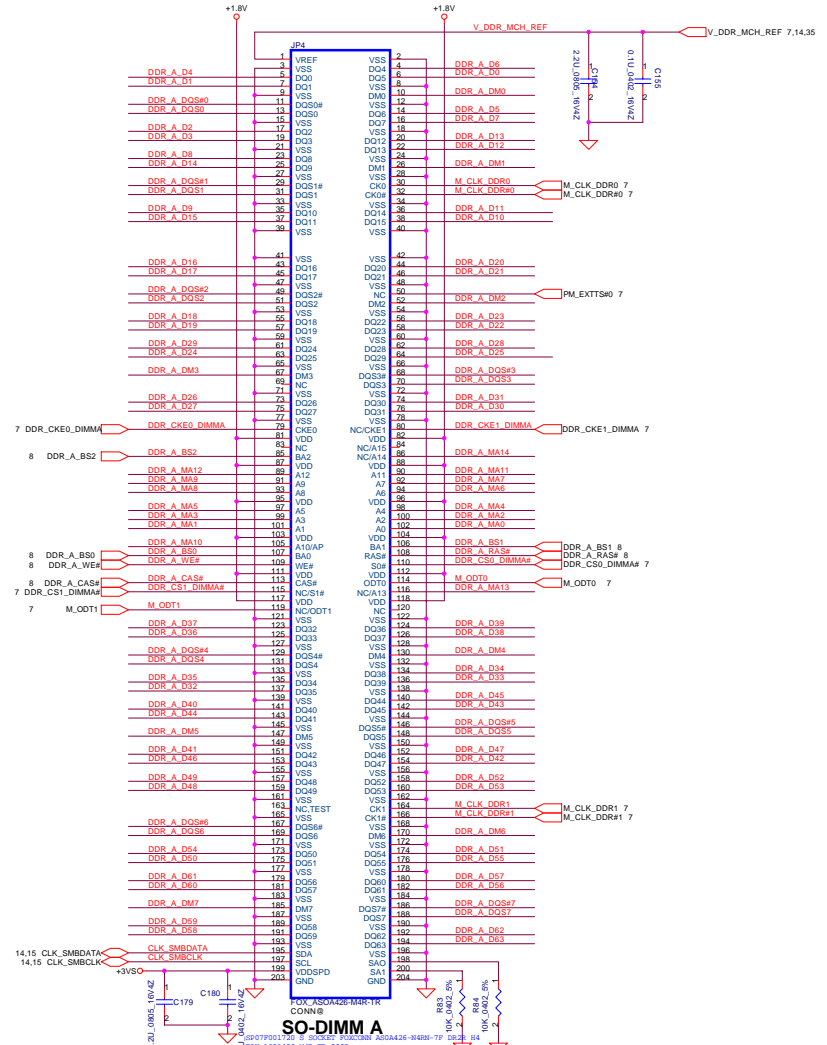
Layout Note:
Place near JP34



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V5

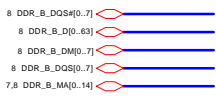


Layout Note:
Place these resistor closely JP34, all trace length Max=1.5"

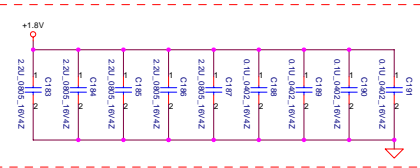


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				Date: Wednesday, October 24, 2007	Sheet 13 of 42

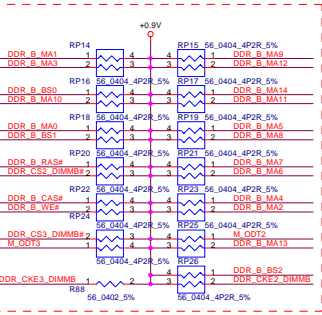
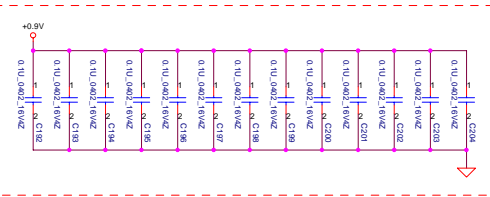
Compal Electronics, Inc.
DDR2-SODIMM SLOT



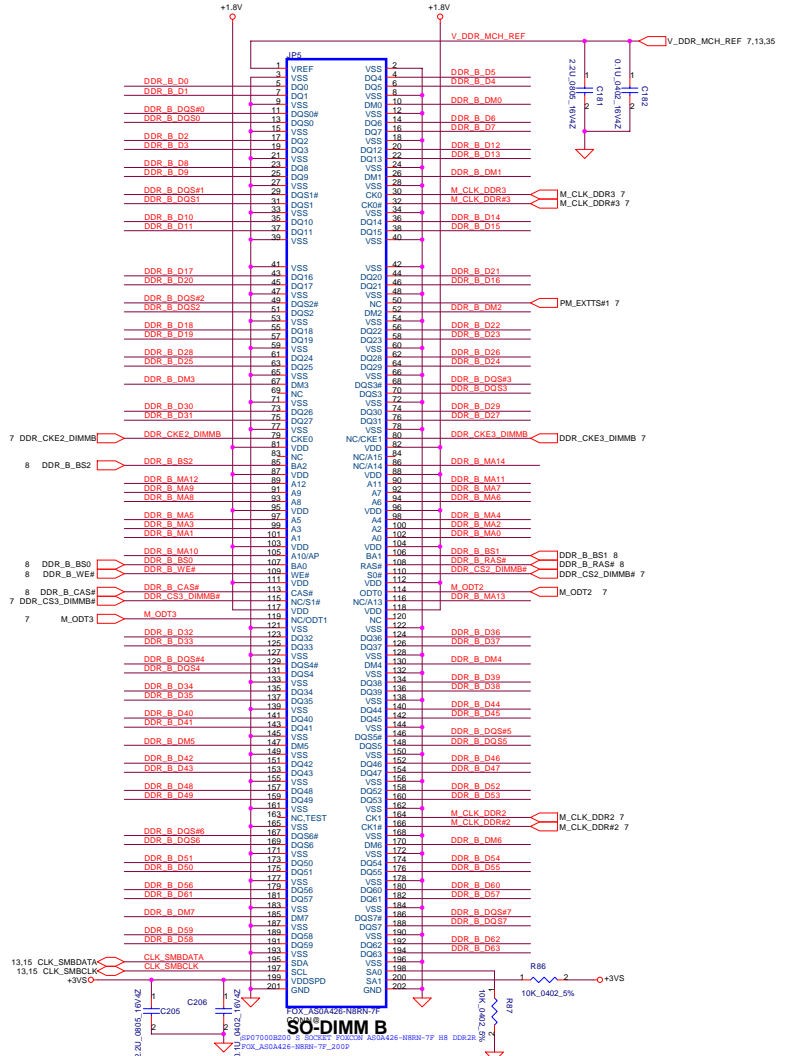
Layout Note:
Place near JP10



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP10, all trace length Max=1.5"



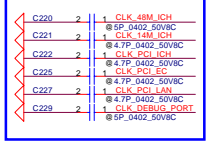
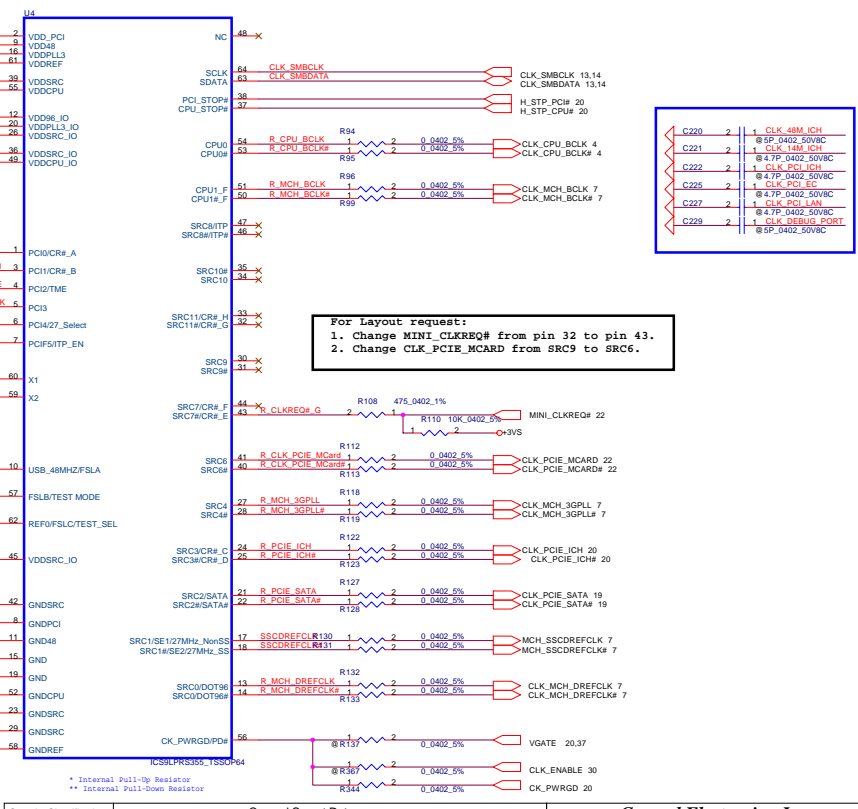
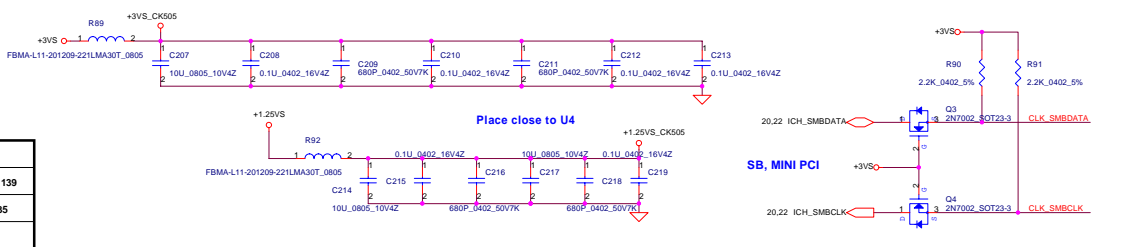
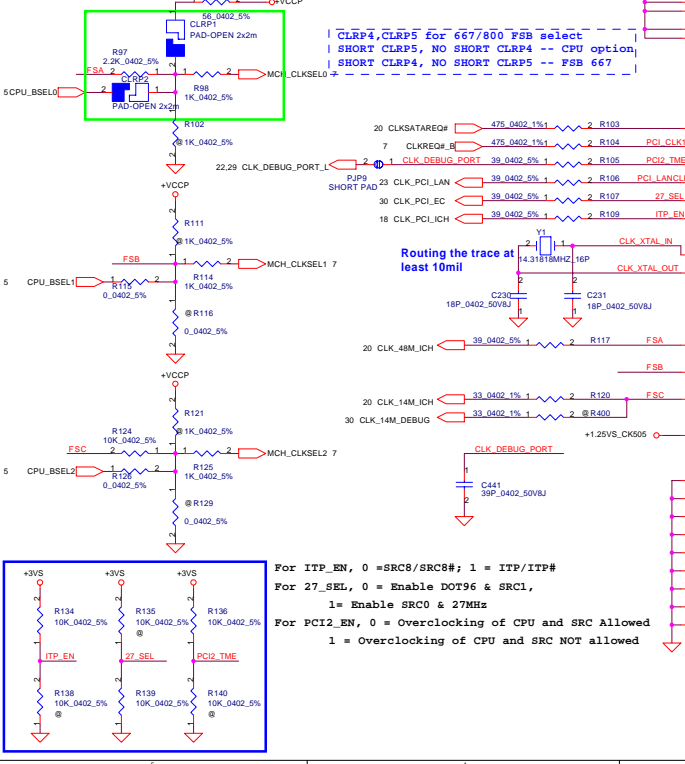
Compal Security Data				Title	
Security Classification	2007/03/26	Deciphered Date	2006/03/10	DDR1-SODIMM SLOT2	
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				LA-4031P	Rev 1.0
				Date: Wednesday, October 24, 2007	Sheet 14 of 42

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Select:

CPU Driven	Stuff	R107	R1135	R1083			
*(Default)	No Stuff	R1074	R1086	R1098	R1113	R1128	R1139
	Stuff	R1086	R1139	R1135	R1074	R1139	R1135
667MHz	No Stuff	R1083	R1107	R1128	R1113	R1098	
	Stuff	R1135	R1139				
800MHz	No Stuff	R1083	R1086	R1098	R1128		
	Stuff	R1074	R1107	R1113			

1015_Change CLR1P and CLR2 type like the same as RJP4.



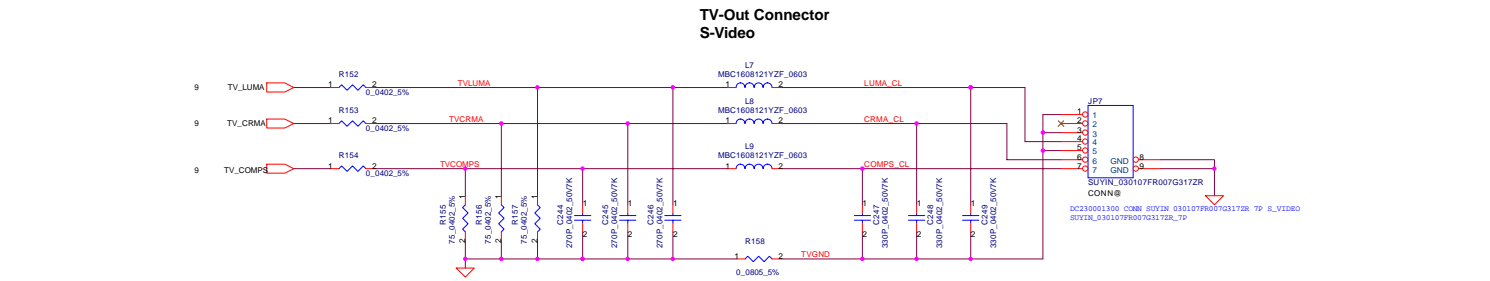
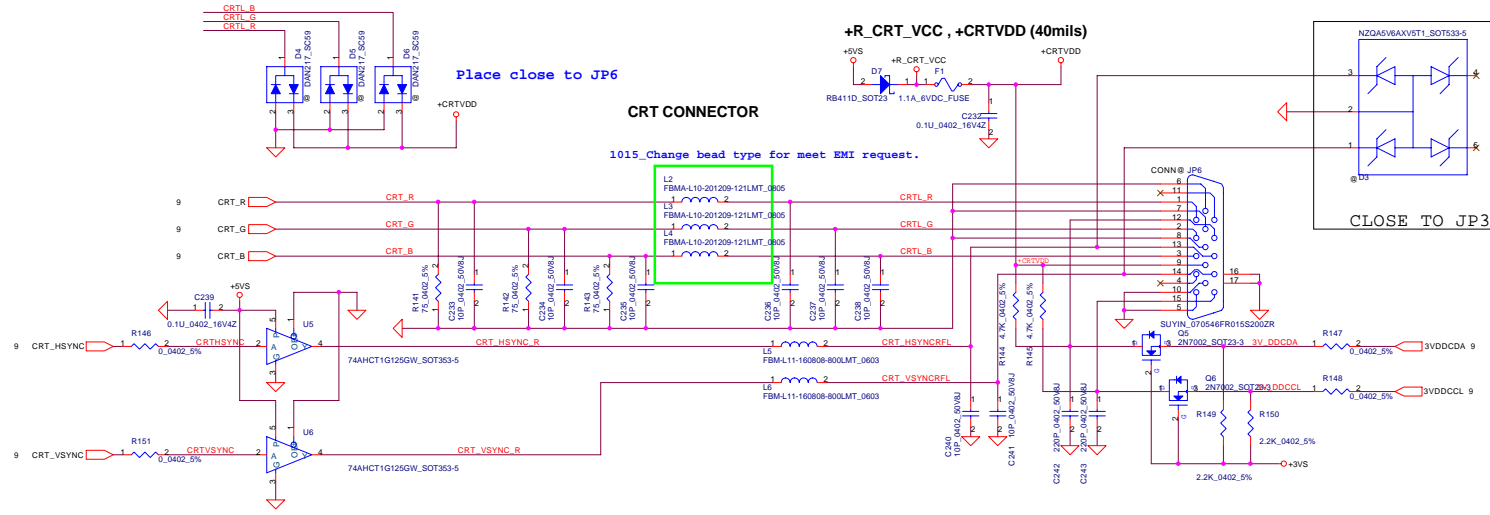
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Issued Date	2007/03/26	Deciphered Date	2006/03/10

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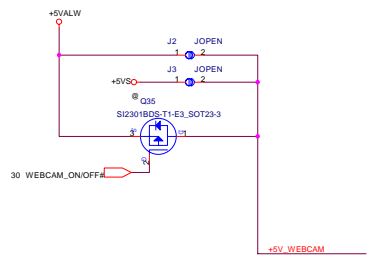
Size	Document Number	Rev
	LA-4031P	1.0

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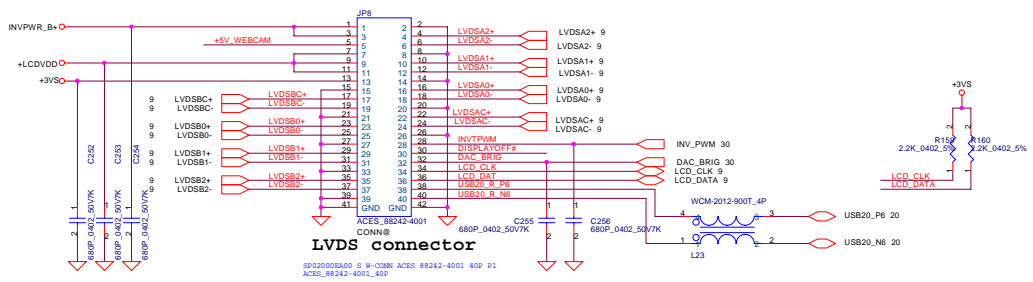
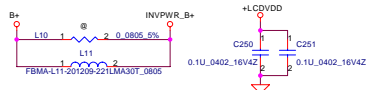
Compal Electronics, Inc.
Clock generator



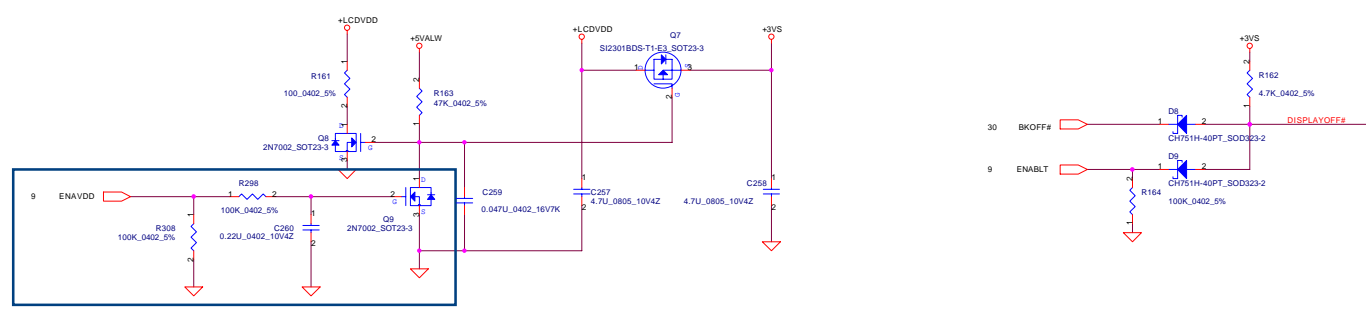
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/07/26
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Title			Compal Electronics, Inc.
Size			CRT & TVout Connector
Document Number			LA-4031P
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LVDS CONN

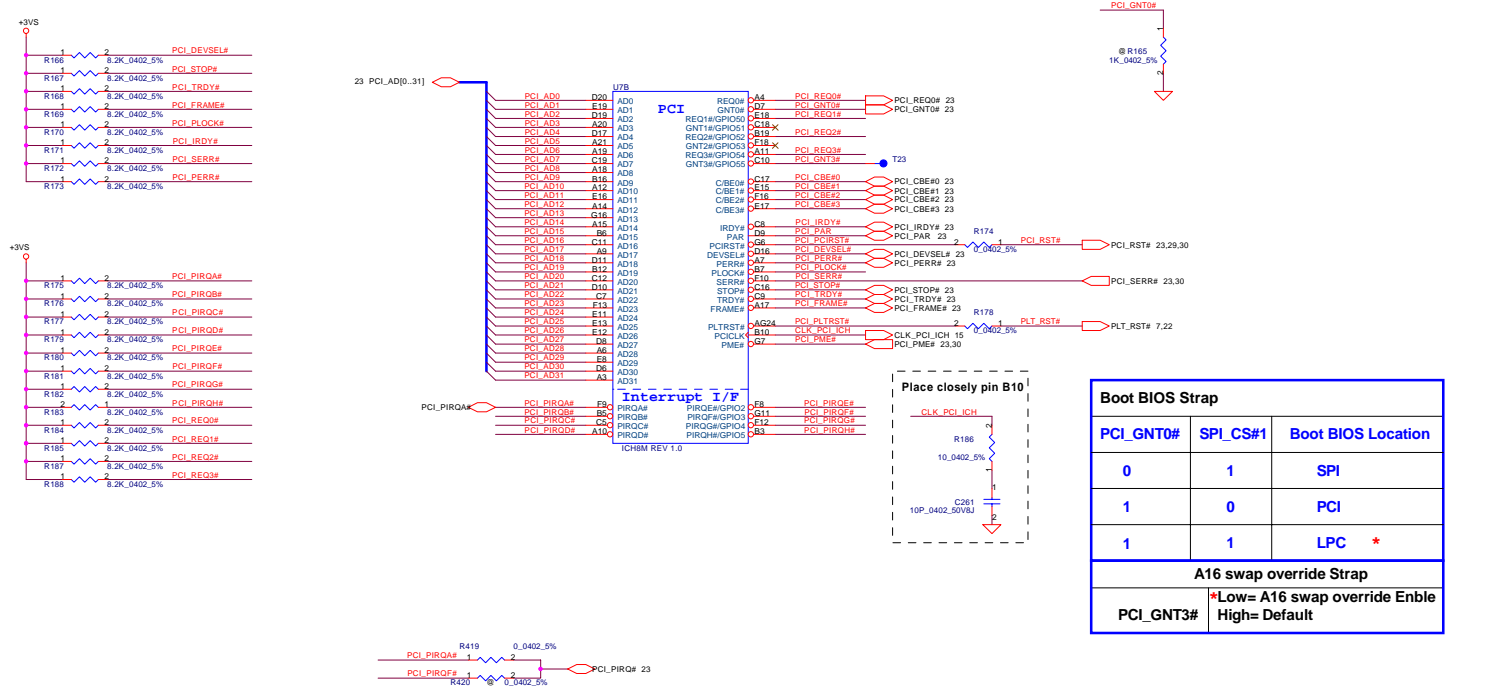


LVDS connector
 ACES_86242-4001
 CONN18
 680P_0402_50V7K
 C255
 680P_0402_50V7K
 WCM-2012-900T_4P
 L23
 ACES_86242-4001_40P_P1
 ACES_86242-4001_40P

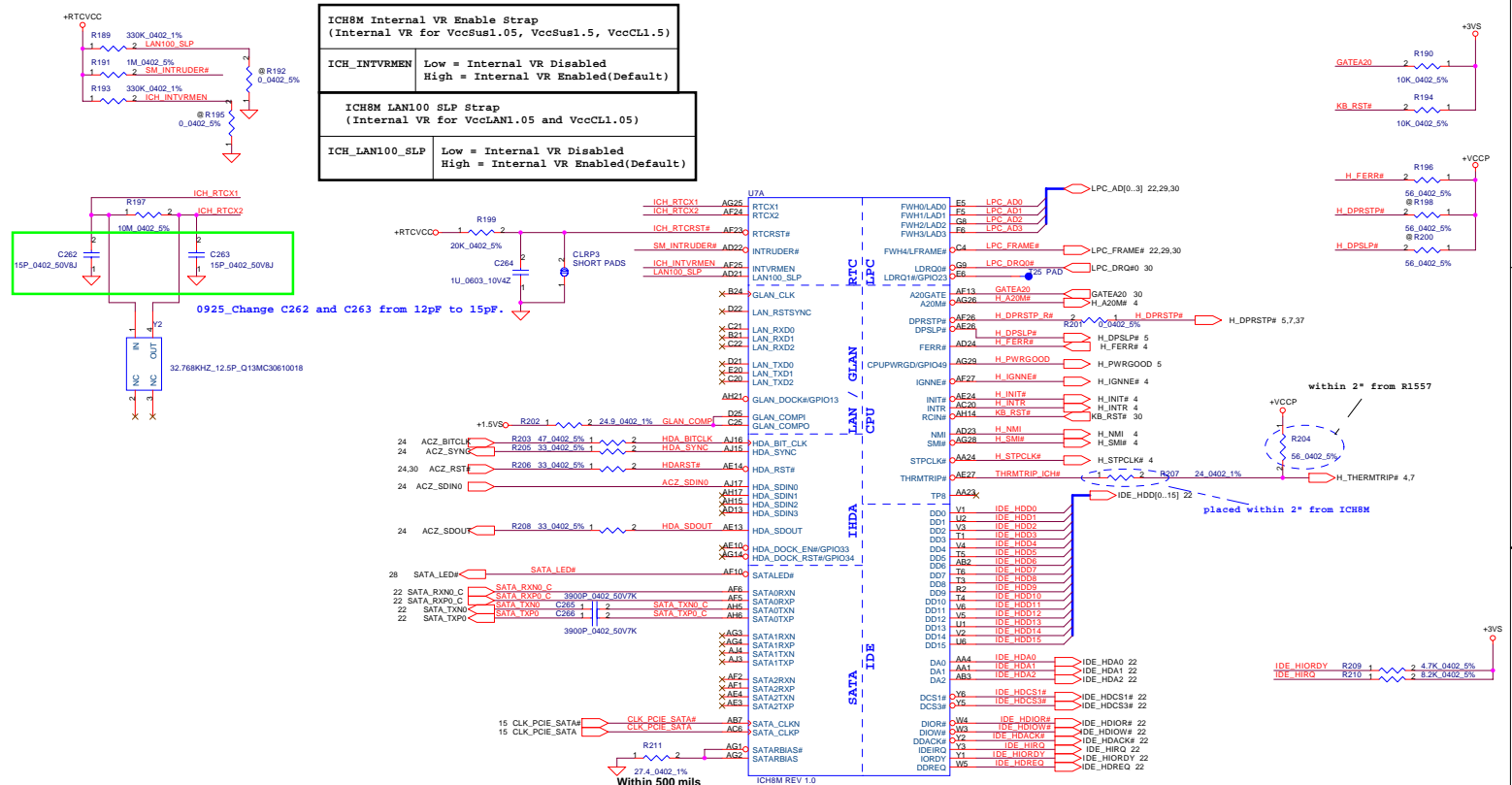


Avoid Panel display garbage after power on.

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Issued Date	2007/03/26	Deciphered Date	2006/07/26	LCD CONN.	
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Size	Document Number	Rev	Date: Wednesday, October 24, 2007 Sheet 17 of 42		
	LA-403P	1.0			

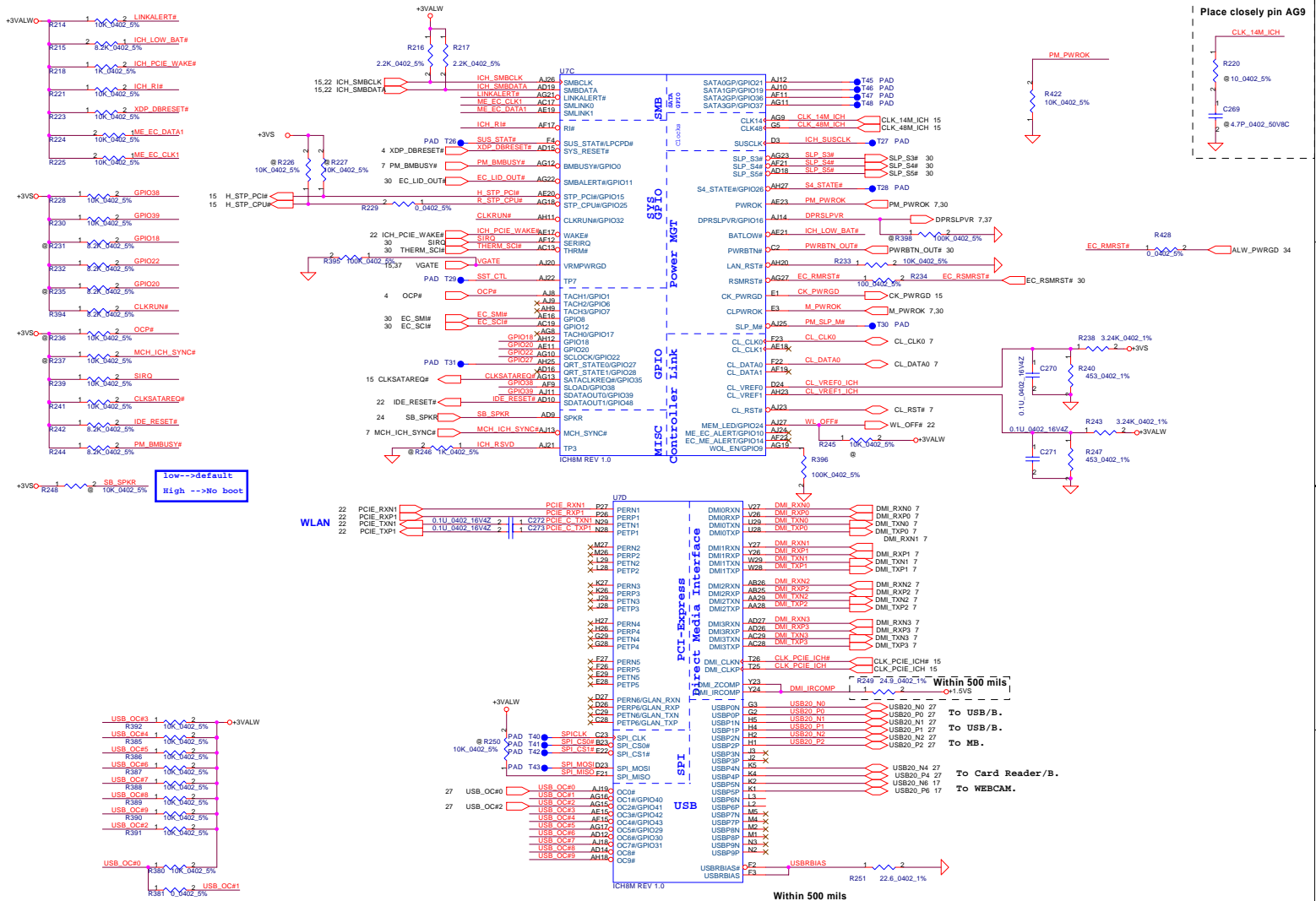


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				LA-4031P	Rev
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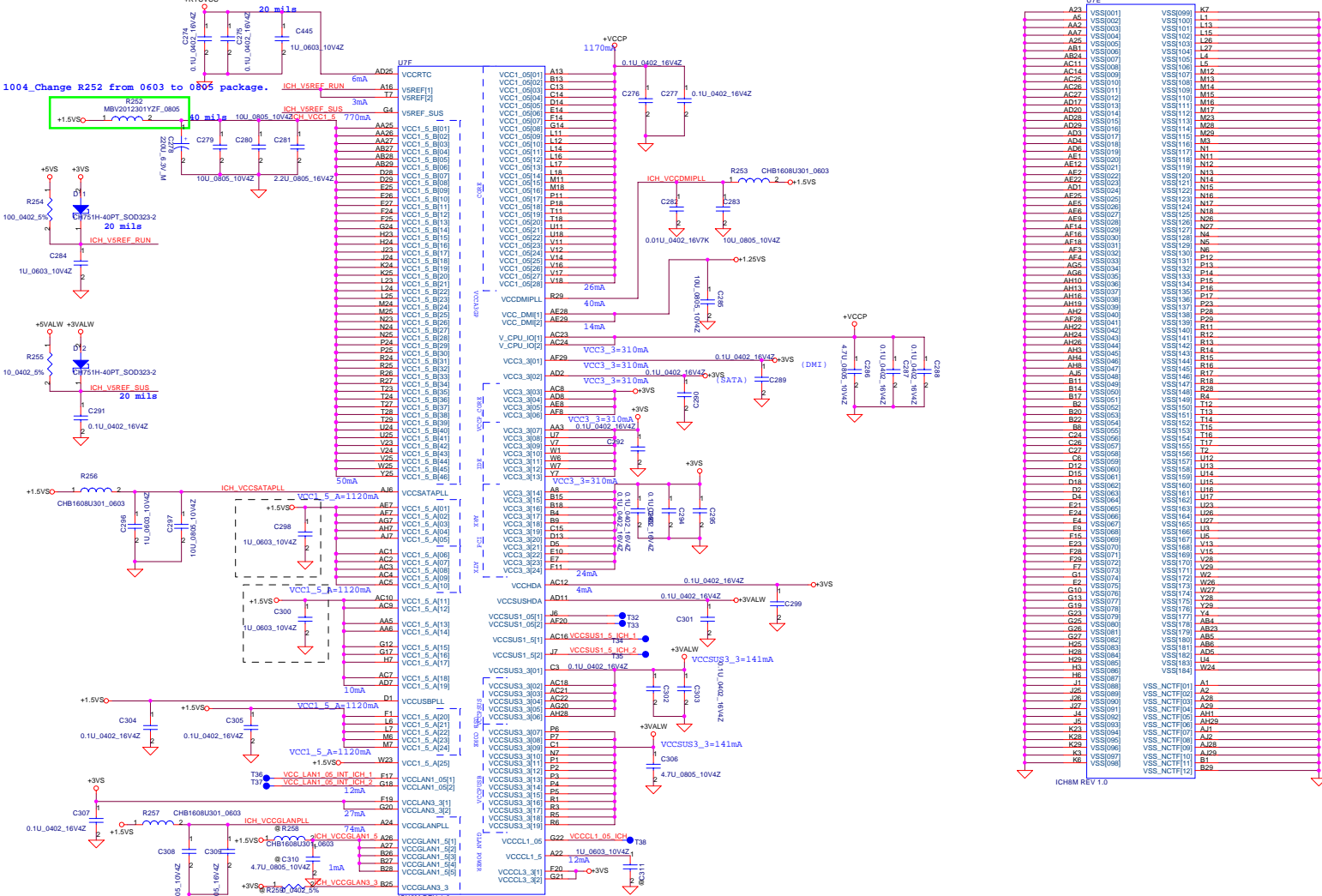


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Issued Date	2007/03/26	Deciphered Date	2006/03/10	Customer	LA-4031P
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Date	Wednesday, October 24, 2007	Sheet	18	of	42

Compal Electronics, Inc.
ICH8(2/4) LAN,HD,IDE,LPC



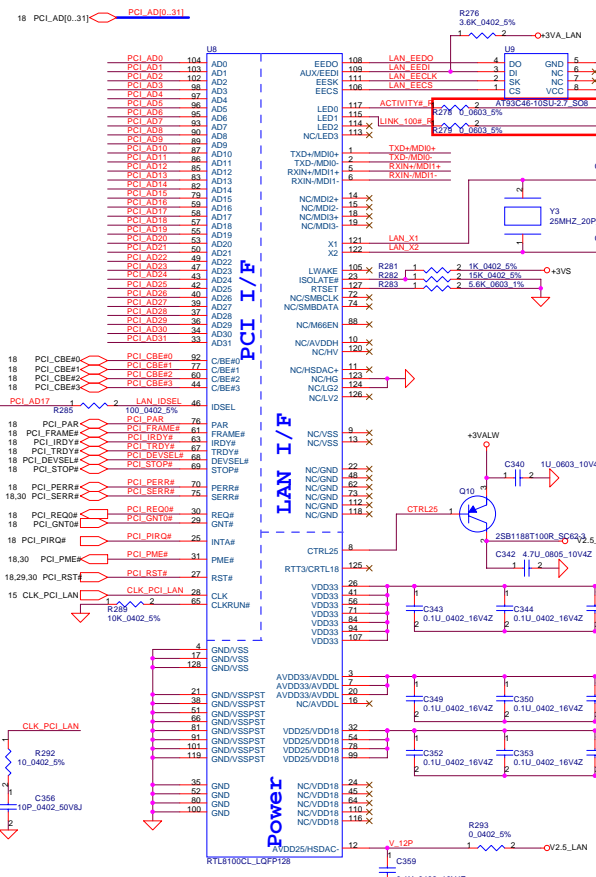
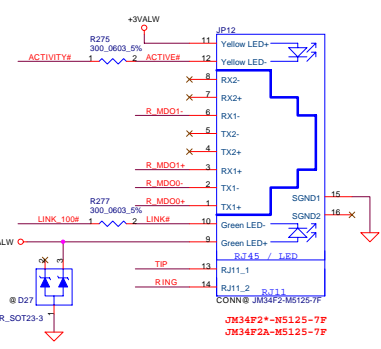
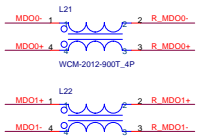
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Issued Date	2007/03/26	Deciphered Date	2006/03/10	
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Size	Document Number	Customer	Rev	
	LA-401P	I CH8(3/4) PM,USB,GPIO	1.0	
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Pin	Signal	Signal	Signal
K7	VSS099	L1	VSS099
K8	VSS001	L2	VSS001
K9	VSS003	L3	VSS003
K10	VSS004	L4	VSS004
K11	VSS005	L5	VSS005
K12	VSS006	L6	VSS006
K13	VSS007	L7	VSS007
K14	VSS008	L8	VSS008
K15	VSS009	L9	VSS009
K16	VSS010	L10	VSS010
K17	VSS011	L11	VSS011
K18	VSS012	L12	VSS012
K19	VSS013	L13	VSS013
K20	VSS014	L14	VSS014
K21	VSS015	L15	VSS015
K22	VSS016	L16	VSS016
K23	VSS017	L17	VSS017
K24	VSS018	L18	VSS018
K25	VSS019	L19	VSS019
K26	VSS020	L20	VSS020
K27	VSS021	L21	VSS021
K28	VSS022	L22	VSS022
K29	VSS023	L23	VSS023
K30	VSS024	L24	VSS024
K31	VSS025	L25	VSS025
K32	VSS026	L26	VSS026
K33	VSS027	L27	VSS027
K34	VSS028	L28	VSS028
K35	VSS029	L29	VSS029
K36	VSS030	L30	VSS030
K37	VSS031	L31	VSS031
K38	VSS032	L32	VSS032
K39	VSS033	L33	VSS033
K40	VSS034	L34	VSS034
K41	VSS035	L35	VSS035
K42	VSS036	L36	VSS036
K43	VSS037	L37	VSS037
K44	VSS038	L38	VSS038
K45	VSS039	L39	VSS039
K46	VSS040	L40	VSS040
K47	VSS041	L41	VSS041
K48	VSS042	L42	VSS042
K49	VSS043	L43	VSS043
K50	VSS044	L44	VSS044
K51	VSS045	L45	VSS045
K52	VSS046	L46	VSS046
K53	VSS047	L47	VSS047
K54	VSS048	L48	VSS048
K55	VSS049	L49	VSS049
K56	VSS050	L50	VSS050
K57	VSS051	L51	VSS051
K58	VSS052	L52	VSS052
K59	VSS053	L53	VSS053
K60	VSS054	L54	VSS054
K61	VSS055	L55	VSS055
K62	VSS056	L56	VSS056
K63	VSS057	L57	VSS057
K64	VSS058	L58	VSS058
K65	VSS059	L59	VSS059
K66	VSS060	L60	VSS060
K67	VSS061	L61	VSS061
K68	VSS062	L62	VSS062
K69	VSS063	L63	VSS063
K70	VSS064	L64	VSS064
K71	VSS065	L65	VSS065
K72	VSS066	L66	VSS066
K73	VSS067	L67	VSS067
K74	VSS068	L68	VSS068
K75	VSS069	L69	VSS069
K76	VSS070	L70	VSS070
K77	VSS071	L71	VSS071
K78	VSS072	L72	VSS072
K79	VSS073	L73	VSS073
K80	VSS074	L74	VSS074
K81	VSS075	L75	VSS075
K82	VSS076	L76	VSS076
K83	VSS077	L77	VSS077
K84	VSS078	L78	VSS078
K85	VSS079	L79	VSS079
K86	VSS080	L80	VSS080
K87	VSS081	L81	VSS081
K88	VSS082	L82	VSS082
K89	VSS083	L83	VSS083
K90	VSS084	L84	VSS084
K91	VSS085	L85	VSS085
K92	VSS086	L86	VSS086
K93	VSS087	L87	VSS087
K94	VSS088	L88	VSS088
K95	VSS089	L89	VSS089
K96	VSS090	L90	VSS090
K97	VSS091	L91	VSS091
K98	VSS092	L92	VSS092
K99	VSS093	L93	VSS093
K100	VSS094	L94	VSS094
K101	VSS095	L95	VSS095
K102	VSS096	L96	VSS096
K103	VSS097	L97	VSS097
K104	VSS098	L98	VSS098
K105	VSS099	L99	VSS099
K106	VSS100	L100	VSS100

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Customer	LA-401P	Sheet	21	of	42	Rev	1.0	
Date	Wednesday, October 24, 2007	Sheet	21	of	42			

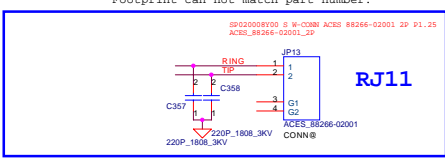
Close to JP12.



For RMI, locate close to LAN chip

close to chip

close to magnetic



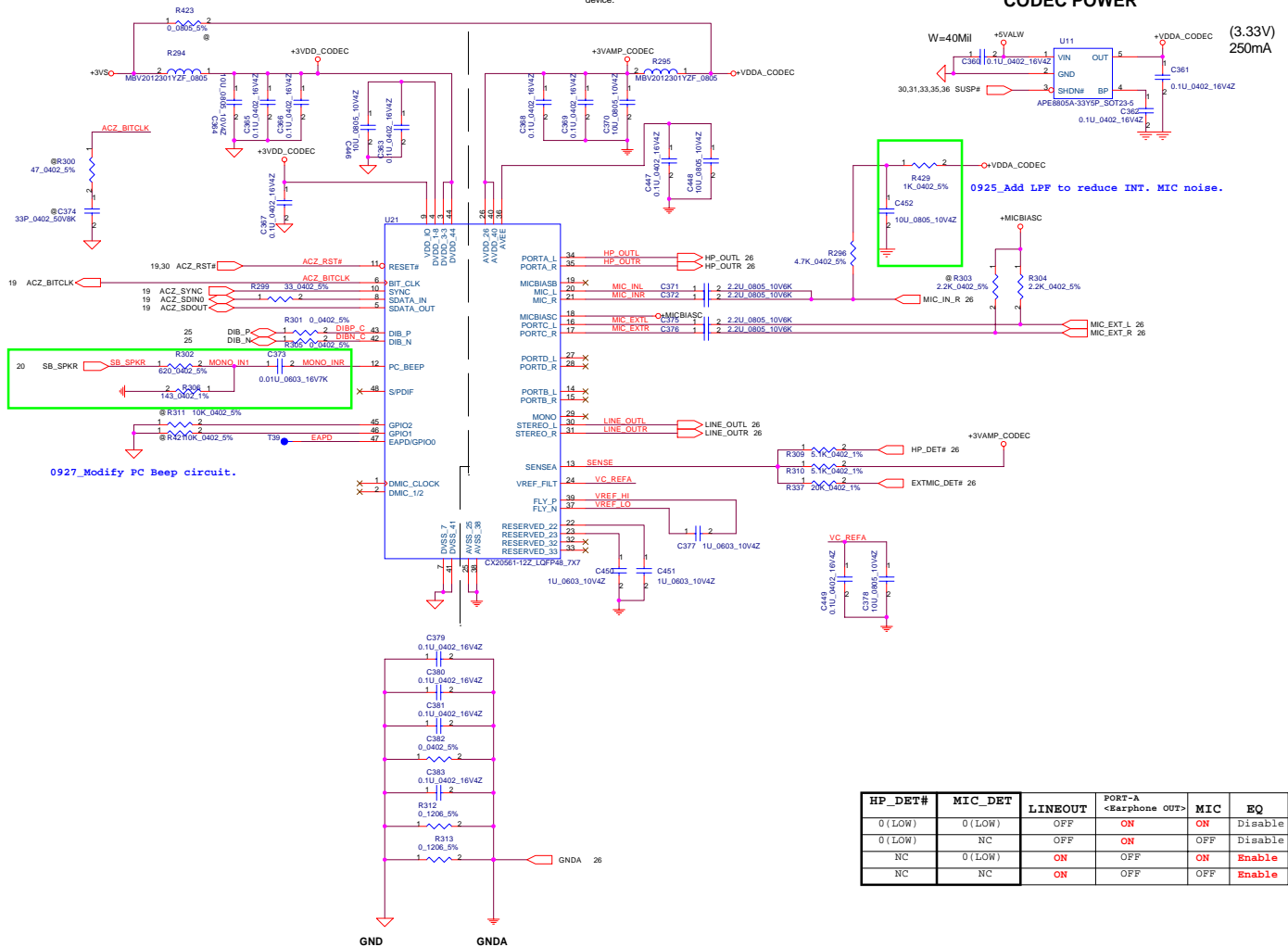
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Issued Date	2007/03/26	Deciphered Date	2007/08/29	LAN-8100CL	
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In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

AUDIO CODEC

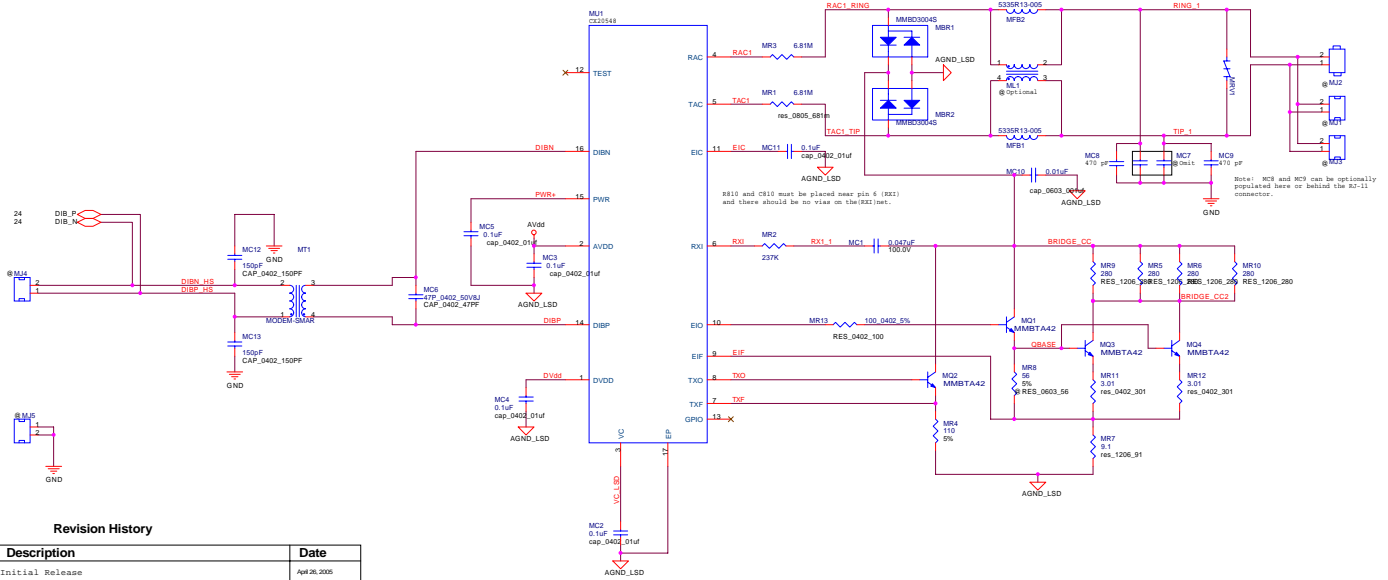
For Layout:
Place decoupling caps near the power pins of SmartAMC device.

CODEC POWER



HP_DET#	MIC_DET	LINEOUT	PORT-A <Earphone OUT>	MIC	EQ
0 (LOW)	0 (LOW)	OFF	ON	ON	Disable
0 (LOW)	NC	OFF	ON	OFF	Disable
NC	0 (LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

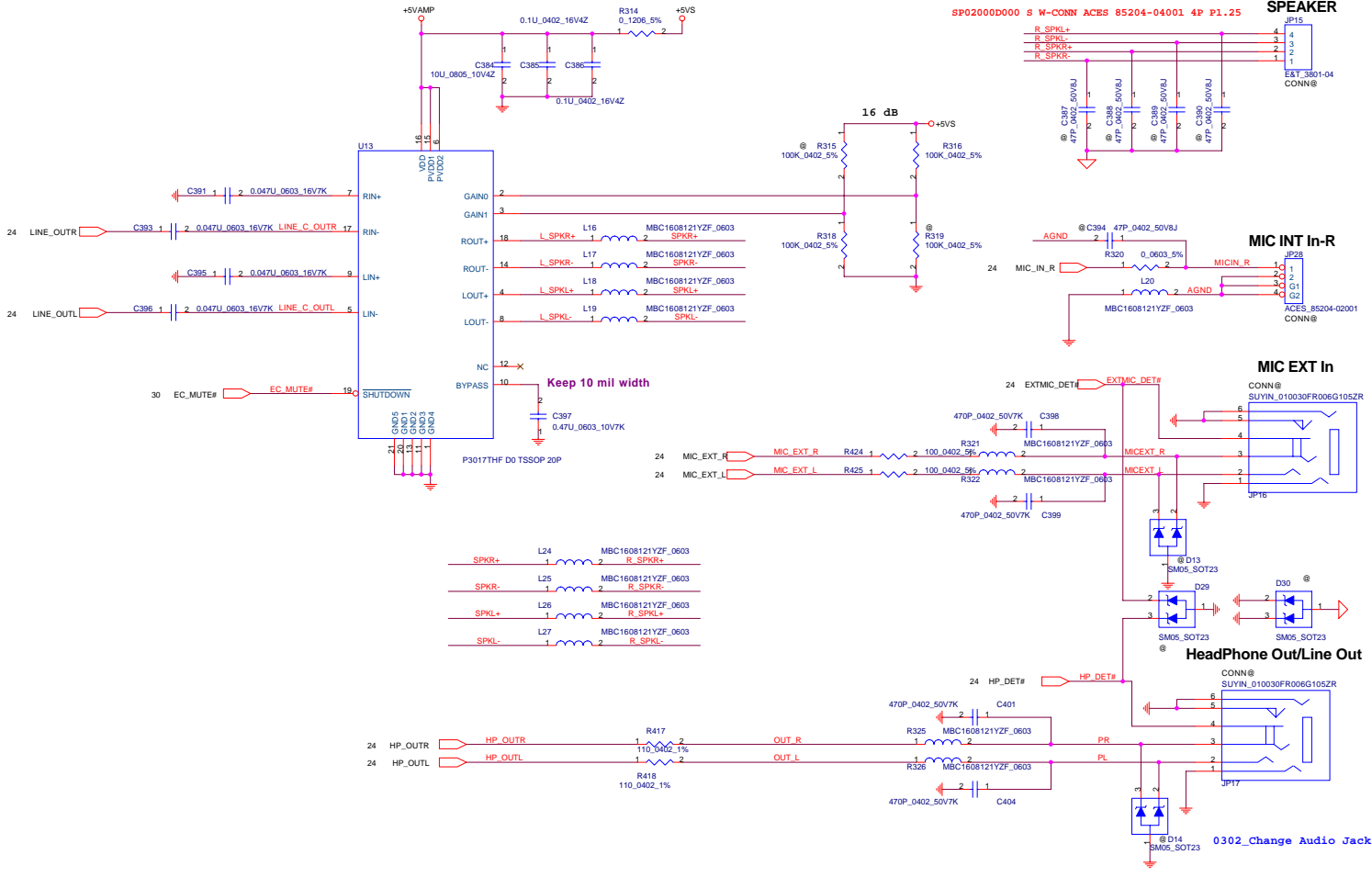
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				Date	Wednesday, October 24, 2007	Sheet	24 of 42



Revision History

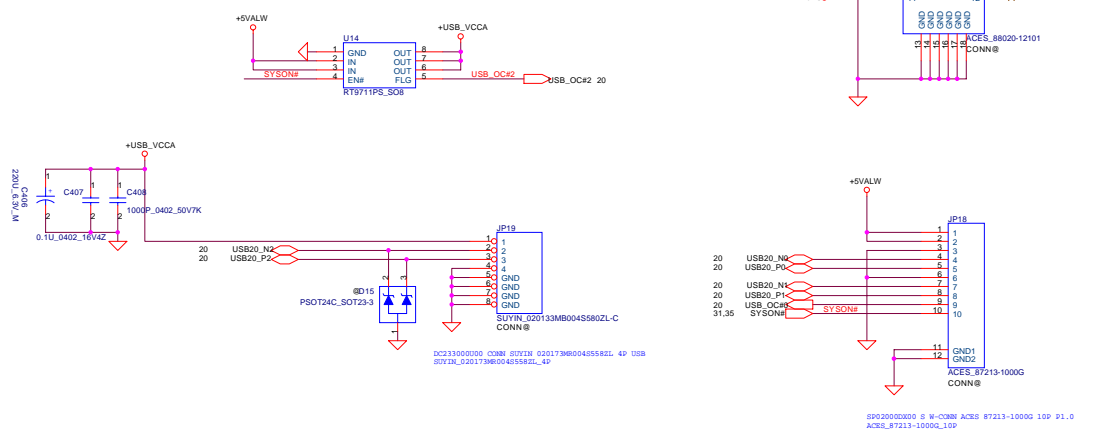
REV	Description	Date
0	Initial Release	April 26, 2005
1	No changes to schematic. PCB updated to -003. Updated footprints and corrected via spacing errors.	April 18, 2005
2	Changed MC8 and MC9 pads. No schematic changes. PCB updated to -005.	November 3, 2005
3	Added MR11 and MR12. PCB updated to -007.	November 18, 2005
4	Added MR13. PCB updated to -009.	January 3, 2006
4.01	AVL update only.	April 20, 2006

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				LA-403IP	Rev 1.0
				Date: Wednesday, October 24, 2007	Sheet 26 of 42

USB Port

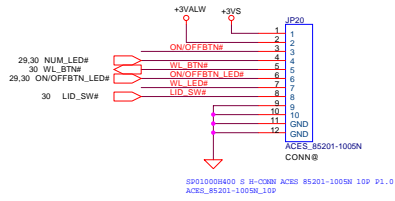


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Issued Date	2007/03/26	Deciphered Date	2006/07/26	USB CONN.
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Size	Document Number	Rev	Date	
	LA-403P	1.0	Wednesday, October 24, 2007	
			Sheet	27 of 42

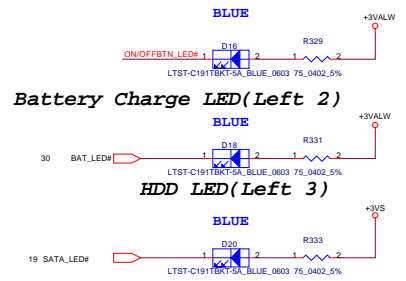
1015_Remove U22 and U23.



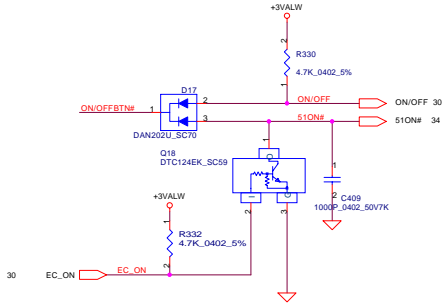
M/BtoS/B



POWER LED(Left 1)

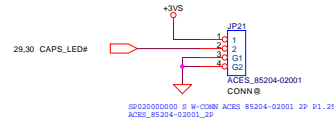


Power ON/OFF

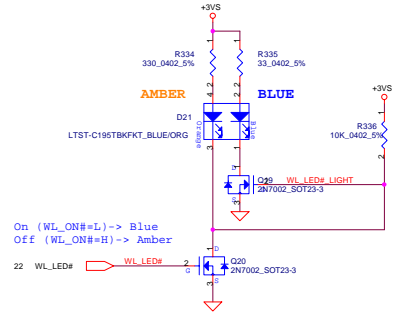


0426_Change all LED power source from 5V to 3V.

M/B to SB(Caps Lock LED)

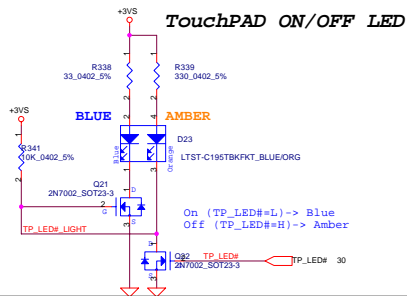


Wireless ON/OFF LED(Left 4)

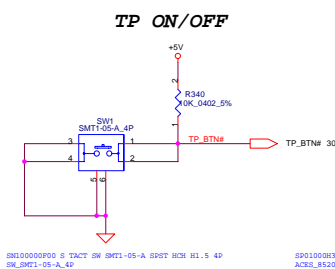


D21, D25, D23 Footprint can not match part number.

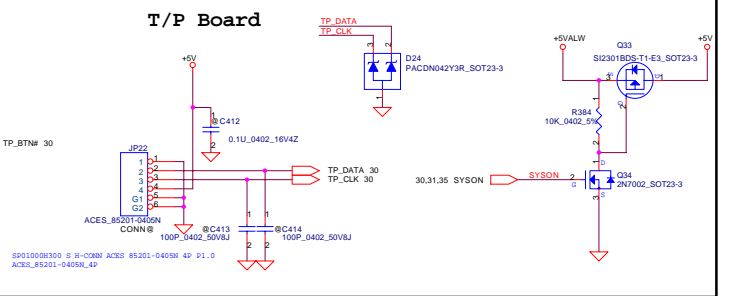
TouchPAD ON/OFF LED



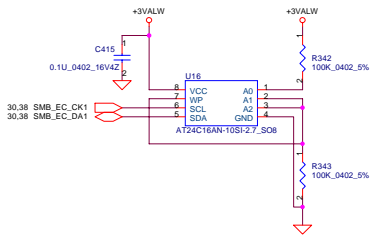
TP ON/OFF



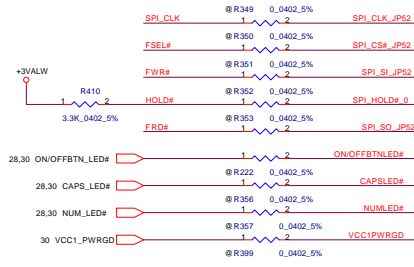
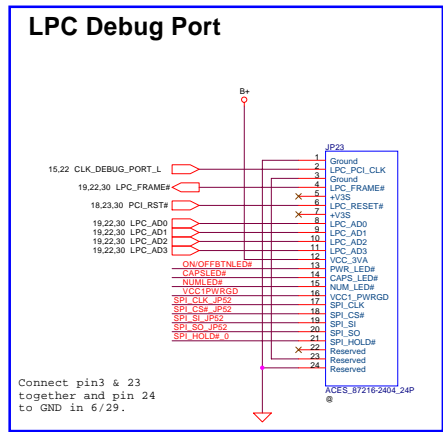
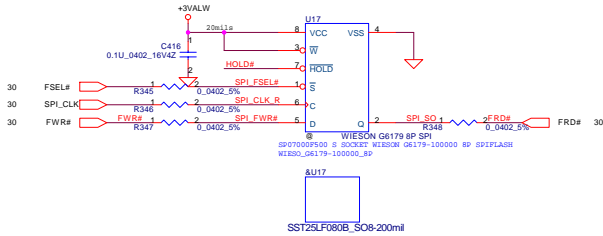
T/P Board



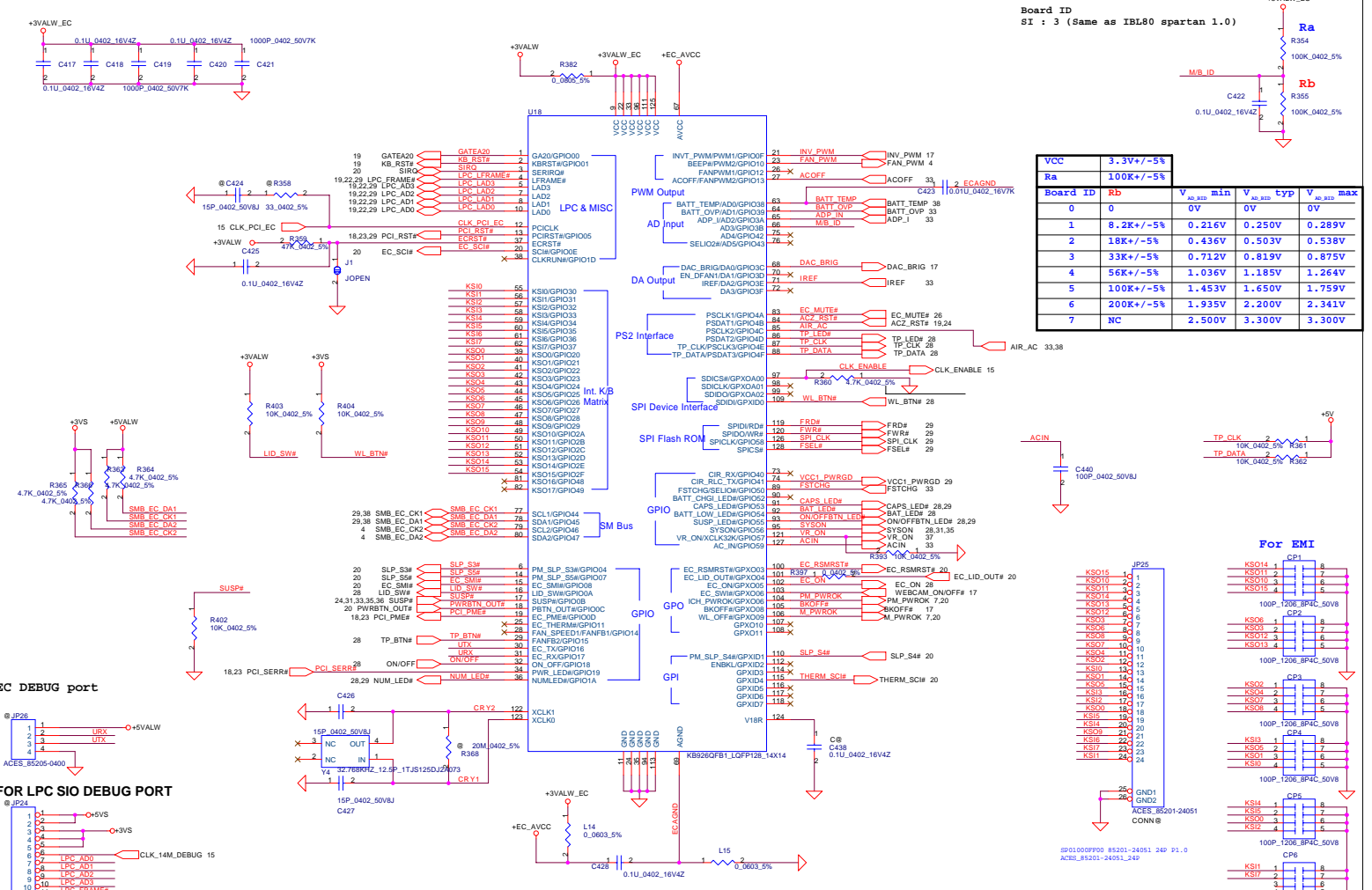
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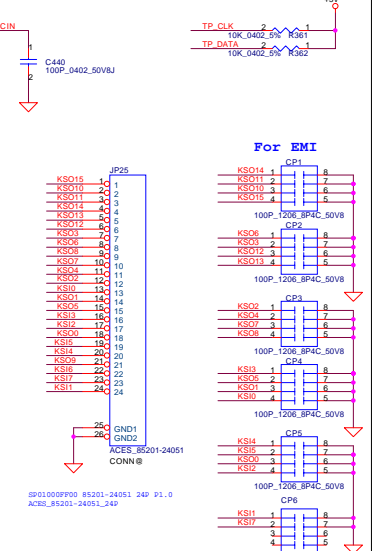
SPI ROM



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Date	Wednesday, October 24, 2007	Sheet	29	of 42

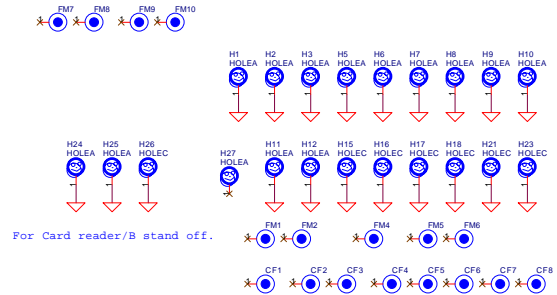
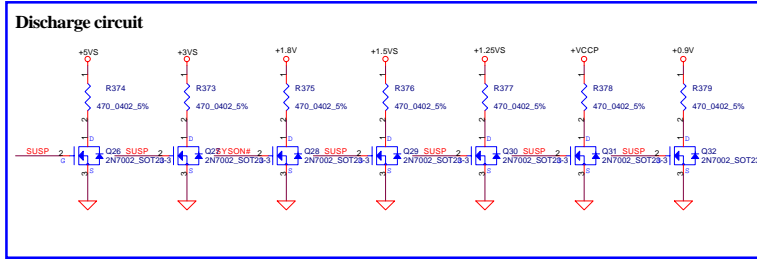
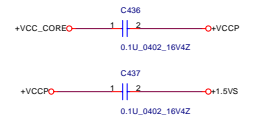
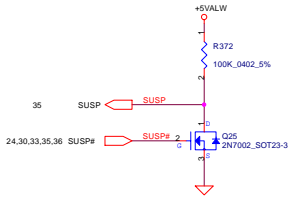
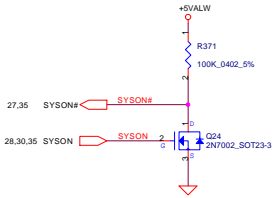
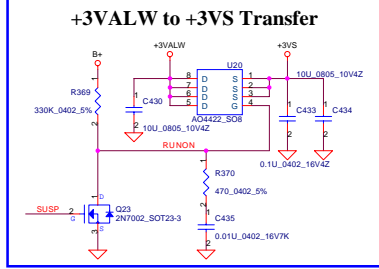
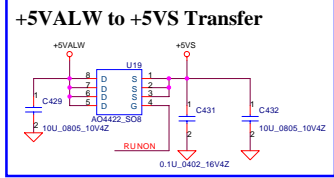


Board ID	Rb	V _{AD_MIN}	V _{AD_TYP}	V _{AD_MAX}
0	0	0V	0V	0V
1	8.2K+/-5%	0.216V	0.250V	0.289V
2	1.8K+/-5%	0.436V	0.503V	0.538V
3	33K+/-5%	0.712V	0.819V	0.875V
4	56K+/-5%	1.036V	1.185V	1.264V
5	100K+/-5%	1.453V	1.650V	1.759V
6	200K+/-5%	1.935V	2.200V	2.341V
7	NC	2.500V	3.300V	3.300V

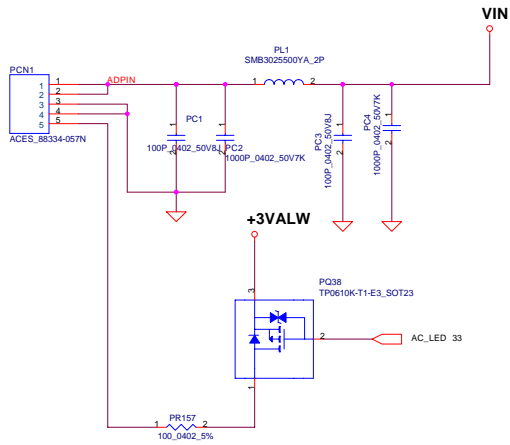


EC DEBUG port

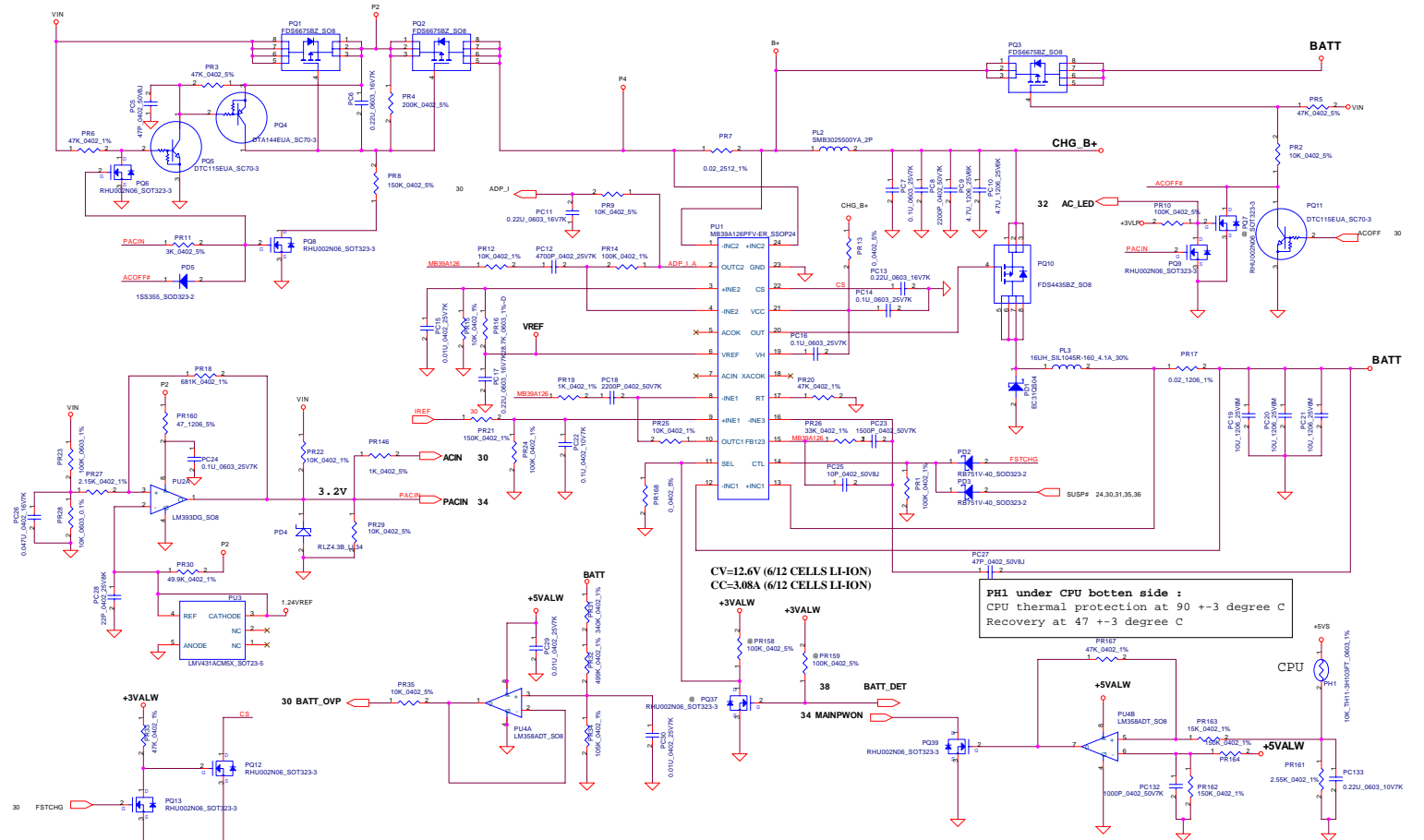
FOR LPC SIO DEBUG PORT



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Date	Wednesday, October 24, 2007	Sheet	31	of	42

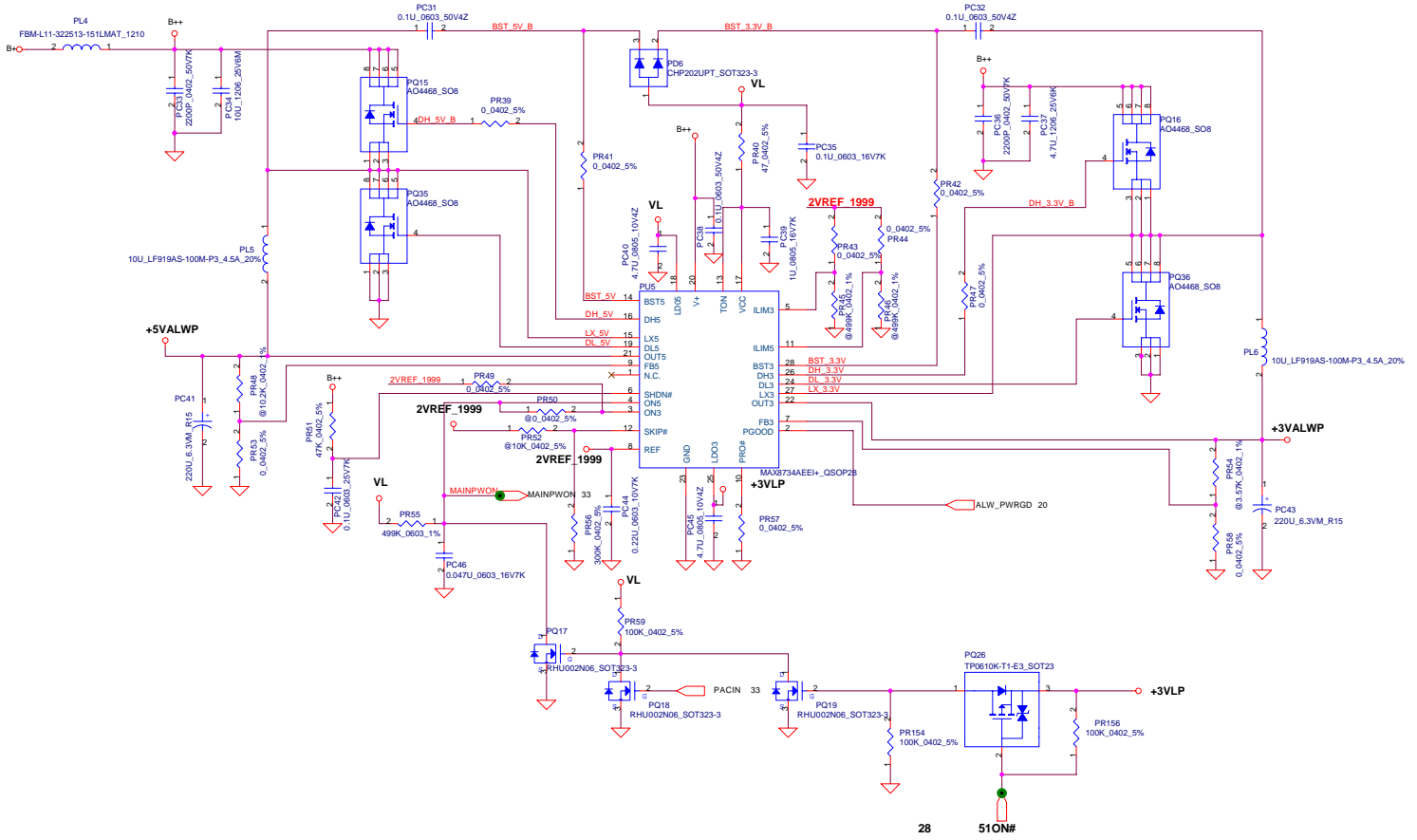


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Date	Wednesday, October 24, 2007	Sheet	32	of 42



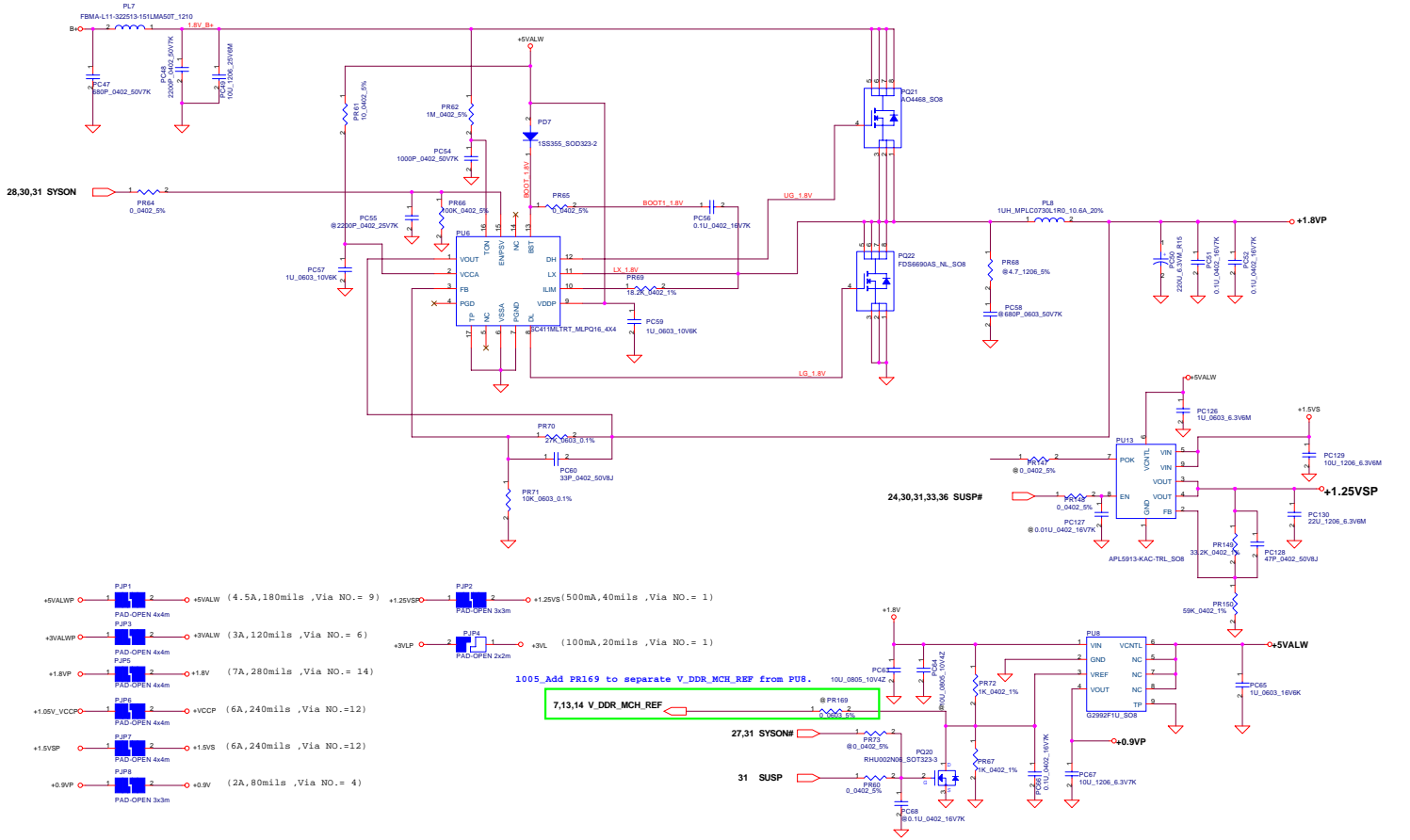
PH1 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 47 +/-3 degree C

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DATE	WSP20250701	DATE	33

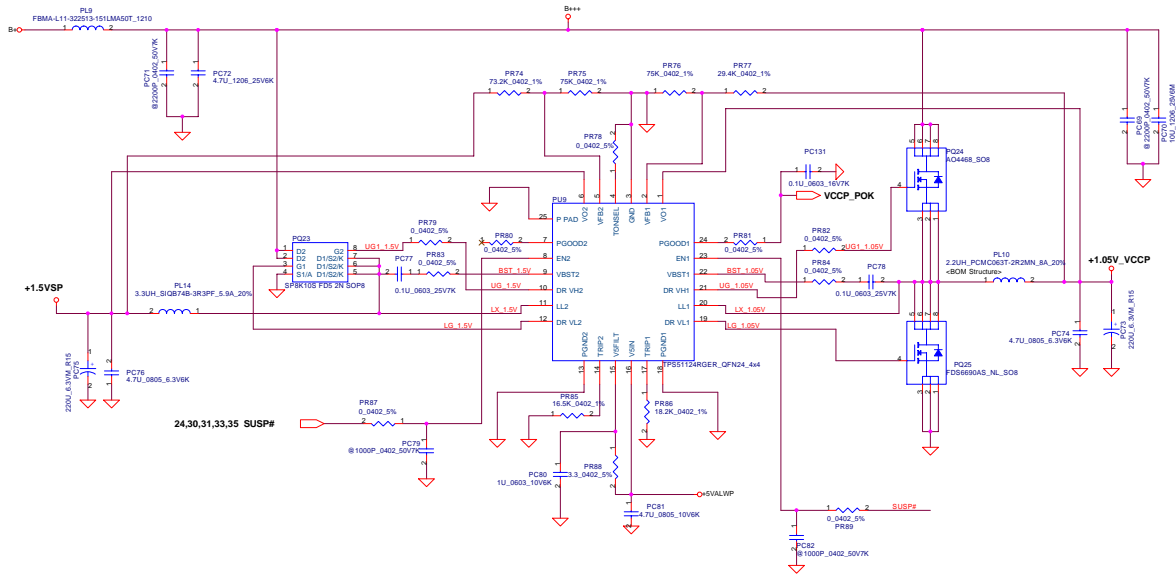


28 510N#

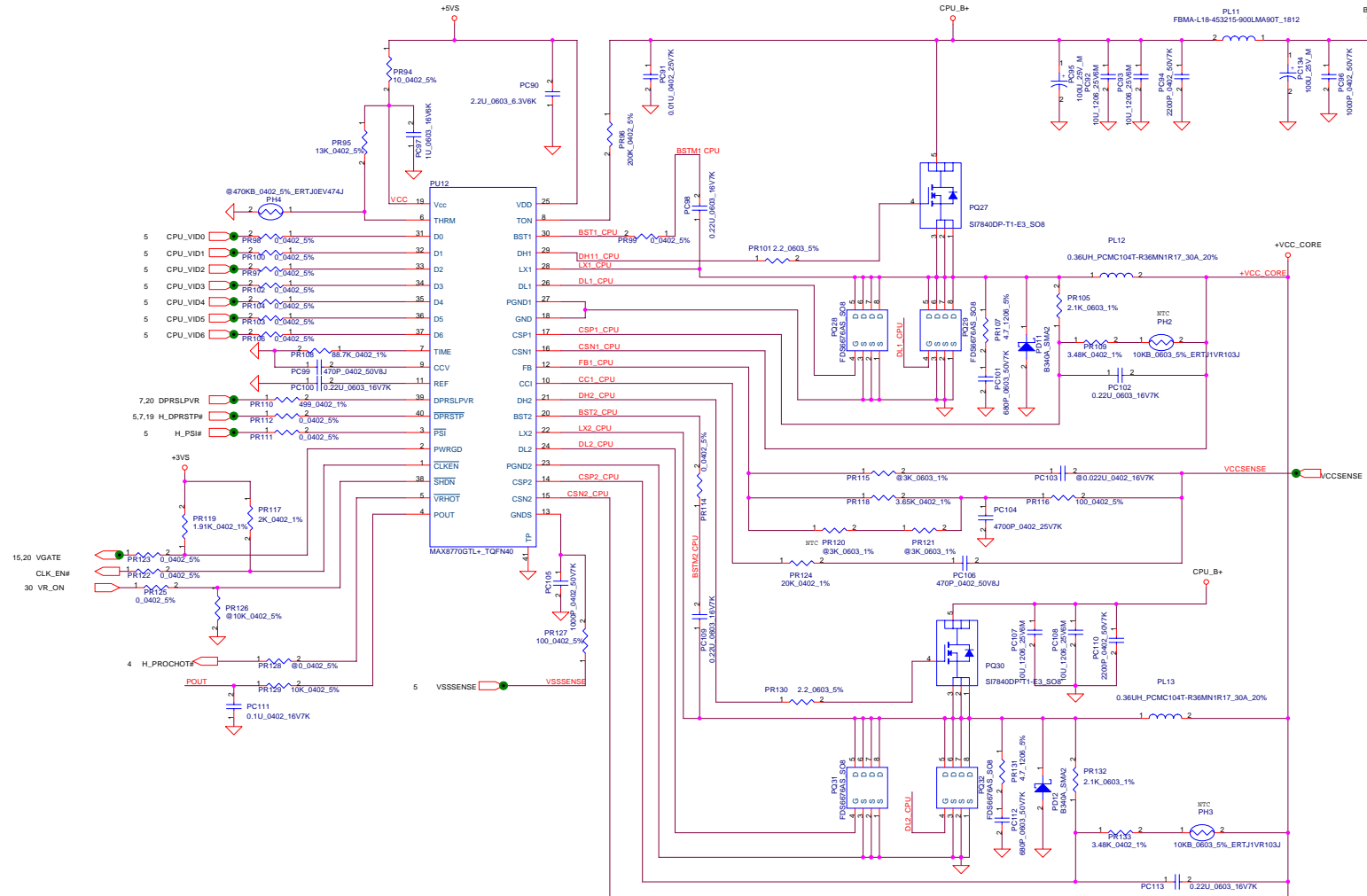
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Size	Document Number	Rev	1.0		
DATE	Wednesday, October 28, 2009	DESIGN	35	of	49

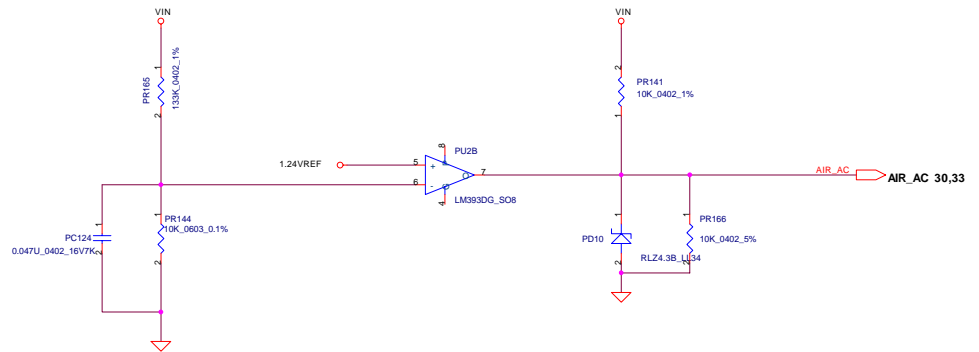
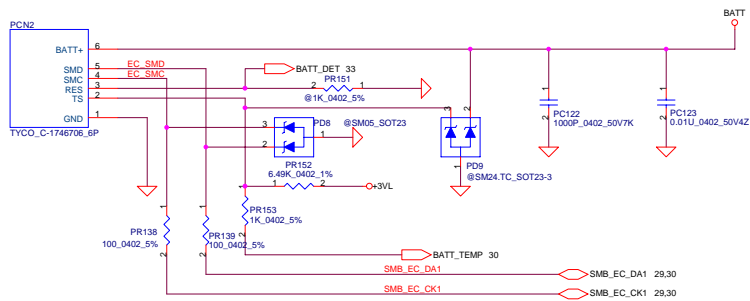


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Compal Electronics, Inc.		
File	+CPU CORE	
Doc No	Document Number	Rev
Cust No	10KB_0603_5%_ERTJ1VR103J	1.0
Date	Wednesday, October 24, 2007	Sheet 37 of 42



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				Size
		Customer	LA-4031P	
		Date	Wednesday, October 24, 2007	Sheet 42 of 38

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
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7					
8					
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14					

Security Classification	Compal Secret Data		Title	
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Version Change List (P. I. R. List) for HW Circuit

Item	Change item	Page	Date	Phase
1	Change R296 2.2K to 4.7K and Reserved R303	24	8/6	SI-->PV
2	Add R424 R425 100ohm on MIC_EXT_R and MIC_EXT_L	26	8/6	SI-->PV
3	Fine tune R298 C260 value	17	8/6	SI-->PV
4	Change PIRQ from F to A	18	8/14	SI-->PV
5	Connect PCI_SERR# to EC GPIO pin.	18	8/31	SI-->PV
6	Modify PC BEEP circuit.	20	8/31	SI-->PV
7	For support Intel Penryn CPU.	04	9/3	SI-->PV
8	For ESD request.	28	9/3	SI-->PV
9	For EMI request.	26	9/5	SI-->PV
10	Change C391, C393, C395, C396 from 0.47uF to 0.047uF.	26	9/7	SI-->PV
11	Add R417 and R418 to fine-tune Vp-p.	26	9/7	SI-->PV
12	For ESD request.	20	9/7	SI-->PV
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Date:	Wednesday, October 24, 2007	Sheet	40	of 42

Version Change List (P. I. R. List) for HW Circuit

Item	Change item	Page	Date	Phase
1	Solve Vref miss when entry S3 mode.	7	9/25	PV-->MV
2	Solve wave ripple on CRT and TV.	10	9/25	PV-->MV
3	Solve RTC timing too exceed.	18	9/25	PV-->MV
4	Reduce INT_MIC noise.	24	9/25	PV-->MV
5	Solve S3 resume fail when use Micron DDR module.	35	10/05	PV-->MV
6	Solve pop noise when entry or resume from S3.	24	9/27	PV-->MV
7	Solve EMI fail for Memory module.	7	9/27	PV-->MV
8	ICH 1.5V power rail 700mA current requirement.	21	10/04	PV-->MV
9	Remove U22 and U23.	28	10/15	PV-->MV
10	For EMI request.	16	10/15	PV-->MV
11	To avoid too easy to open solder for CLRP2.	15	10/15	PV-->MV
12	Solve acoustic noise issue.	10	10/22	PV-->MV
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