

Compal confidential

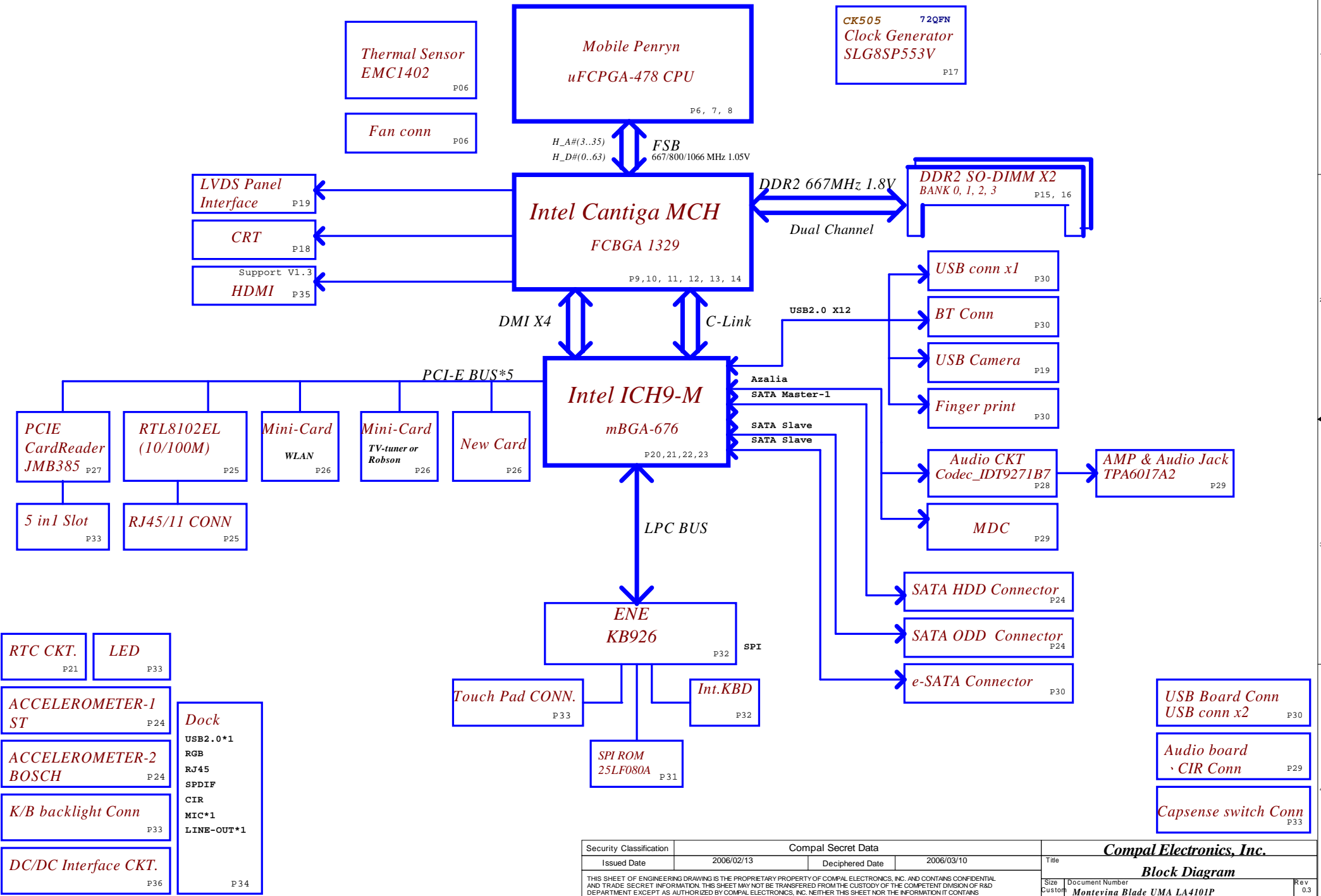
Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M core logic

2008-01-01

Security Classification	Compal Secret Data			Title Compal Electronics, Inc.		
Issued Date	2007/08/28	Deciphered Date	2006/03/10	Cover Sheet		
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				Custom	Montevina Blade UMA LA4101P	0.3
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Montevina Consumer 14" UMA



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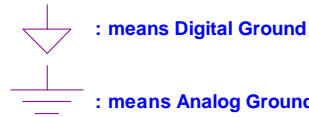
Block Diagram

Voltage Rails

O MEANS ON X MEANS OFF

power plane	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS
State				
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
DEBUG@ :	means just reserve for debug.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
ESATA @ :	means just reserve for ESATA
GS @ :	means just reserve for G sensor
FP @ :	means just reserve for Finger Print
Multi @ :	means just reserve for Multi Bay
NewC@ :	means just reserve for New card
DOCK@ :	means just reserve for Docking
Main@ :	means just reserve for Main stream
OPP@ :	means just reserve for OPP
2MiniC@ :	means just reserve for 2nd Mini card slot

USB assignment:

USB-0	Right side
USB-1	Right side
USB-2	Left side(with ESATA)
USB-3	Dock
USB-4	Camera
USB-5	WLAN
USB-6	Bluetooth
USB-7	Finger Printer
USB-8	MiniCard(WWAN/TV)
USB-9	Express card
USB-10	X
USB-11	X

PCIe assignment:

PCIe-1	TV /WWAN/Robeson
PCIe-2	X
PCIe-3	WLAN
PCIe-4	GLAN (Realtek)
PCIe-5	Card reader
PCIe-6	New Card

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X	V	V
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V	X	X	X

43154432L01 : Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/Multi@/2MiniC@
 43154432L02 : Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/2MiniC@
 43154432L03 : Main@/DEBUG@/DOCK@/NewC@/FP@/2MiniC@
 43154432L04 : OPP@/DEBUG@
 43154432L05 : OPP@/DEBUG@

I2C / SMBUS ADDRESSING

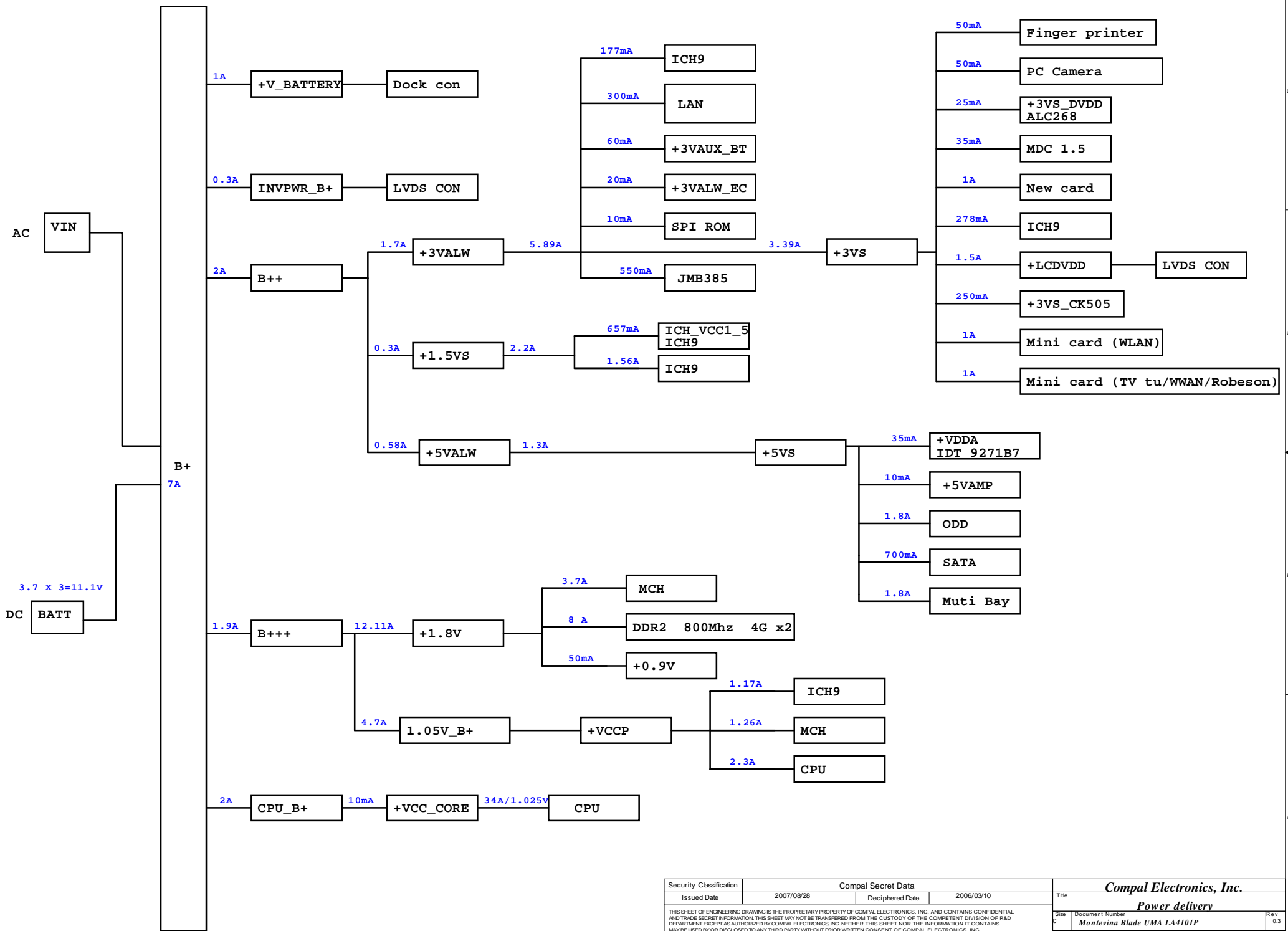
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

43154432L01 : UMA GM PA FF (SI-1)
 43154432L02 : UMA GM PR FF (SI-1)
 43154432L03 : UMA GL PR FF-
 43154432L04 : UMA GM OPP (SI-1)
 43154432L05 : UMA GL OPP

Cantiga GM45 B0(QR32) : SA00001P930
 ICH9M A2 ES2 Base : SA00002AN10

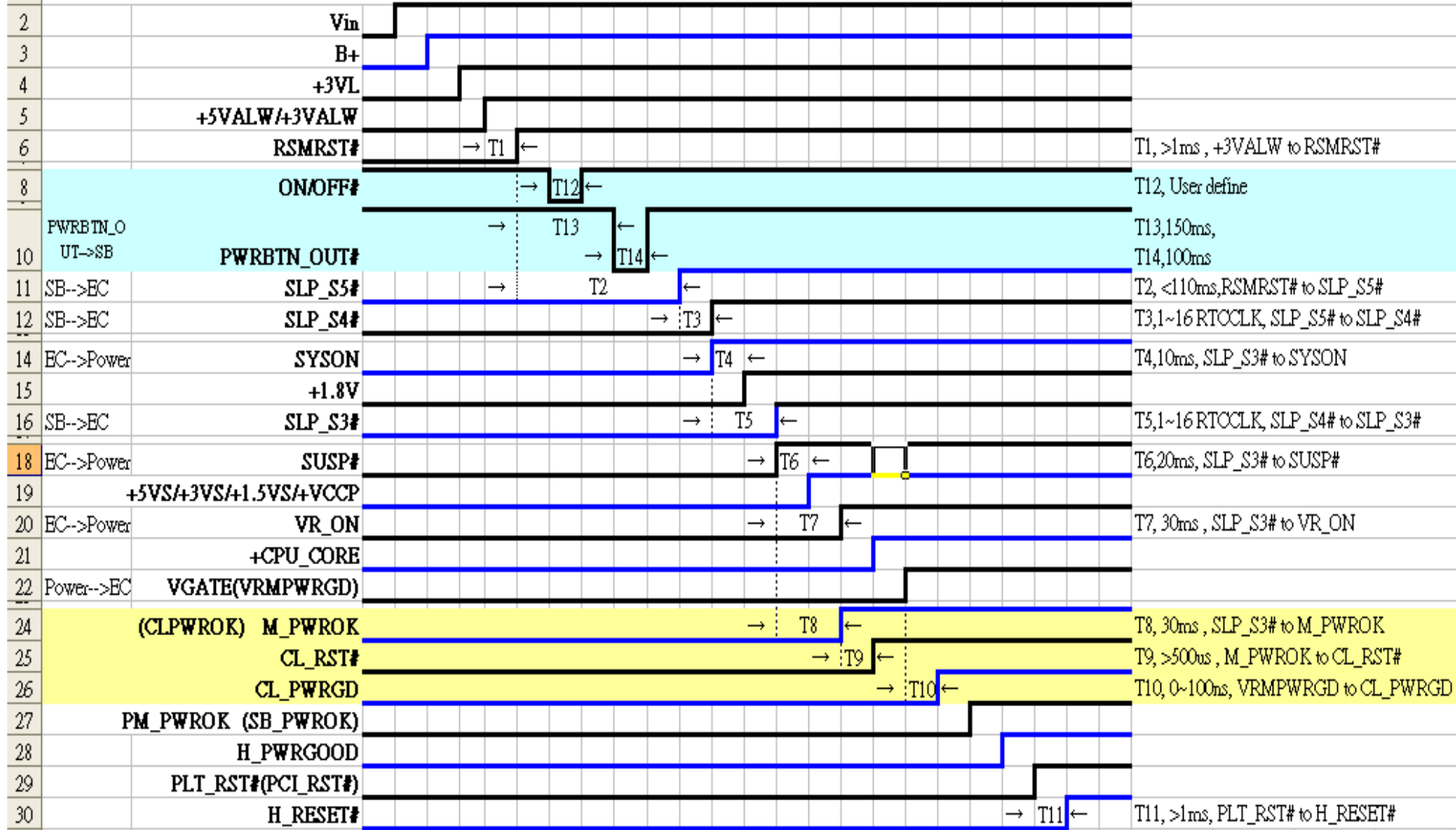
DA600007100 --->Main
 DAZ03V00100 --->OPP

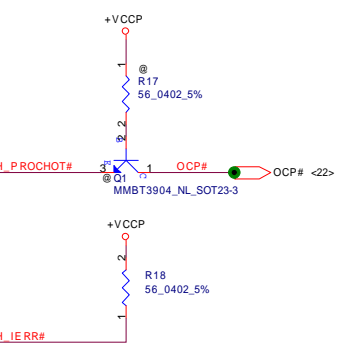
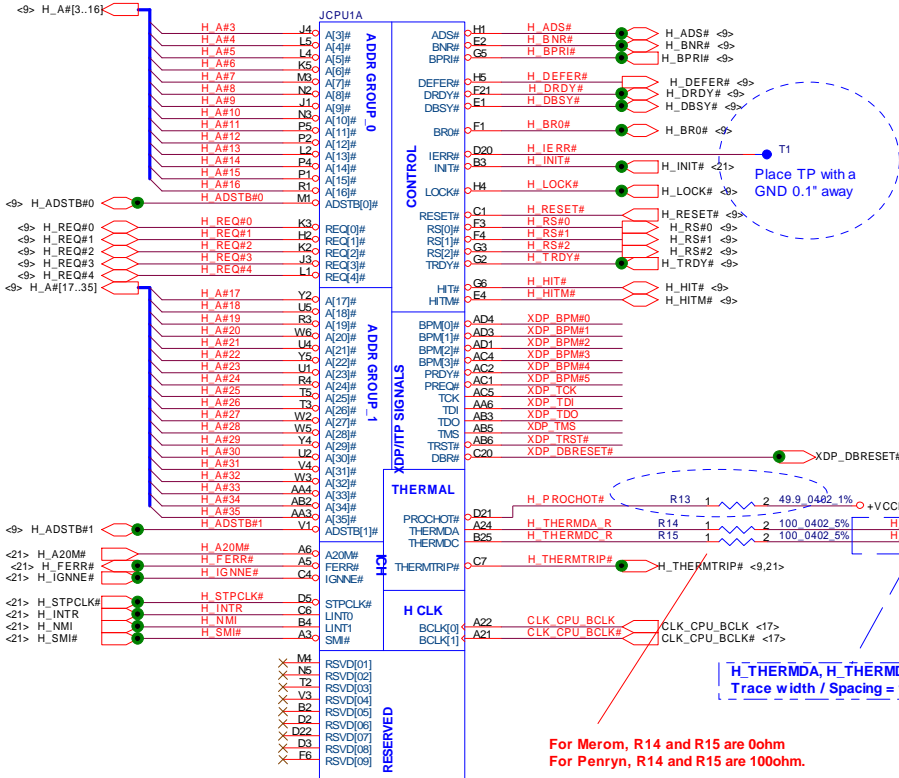
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JAL50 power sequence AC mode

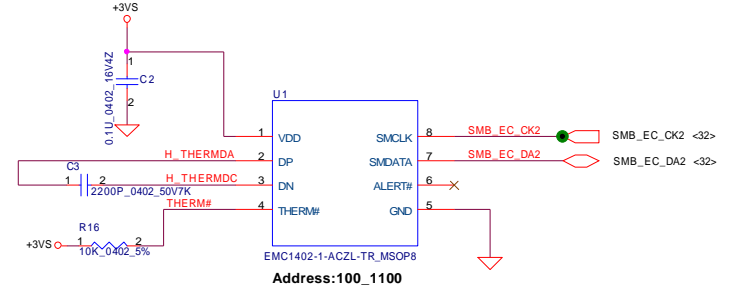
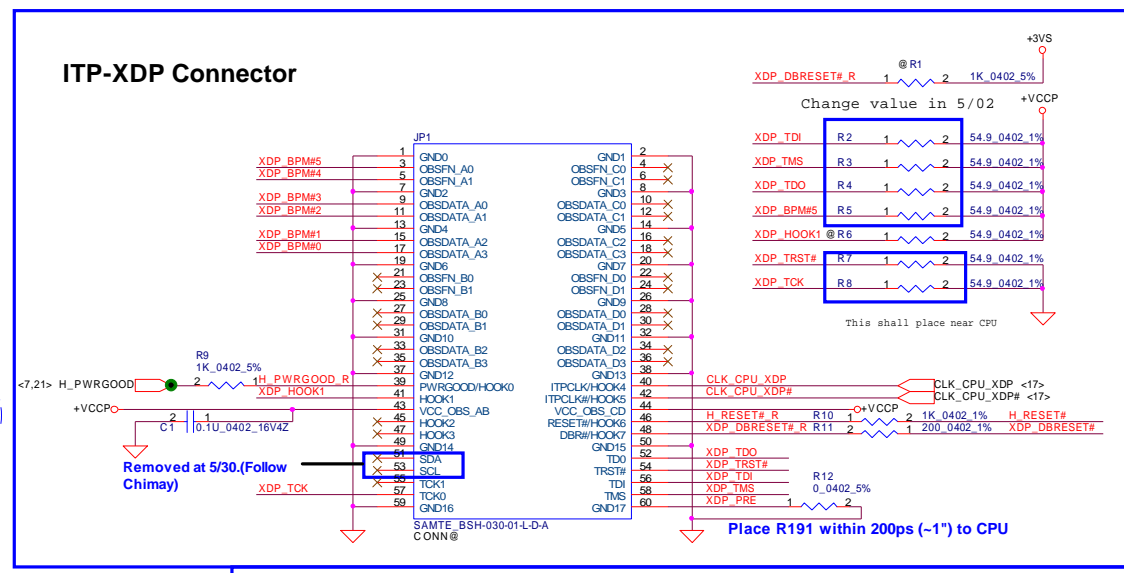
96.09.03.



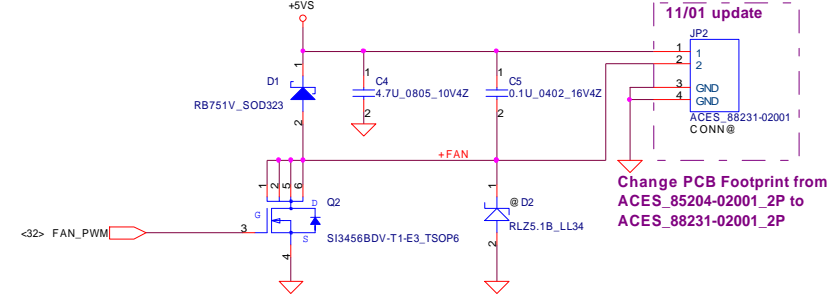


For Merom, R14 and R15 are 0ohm
For Penryn, R14 and R15 are 100ohm.

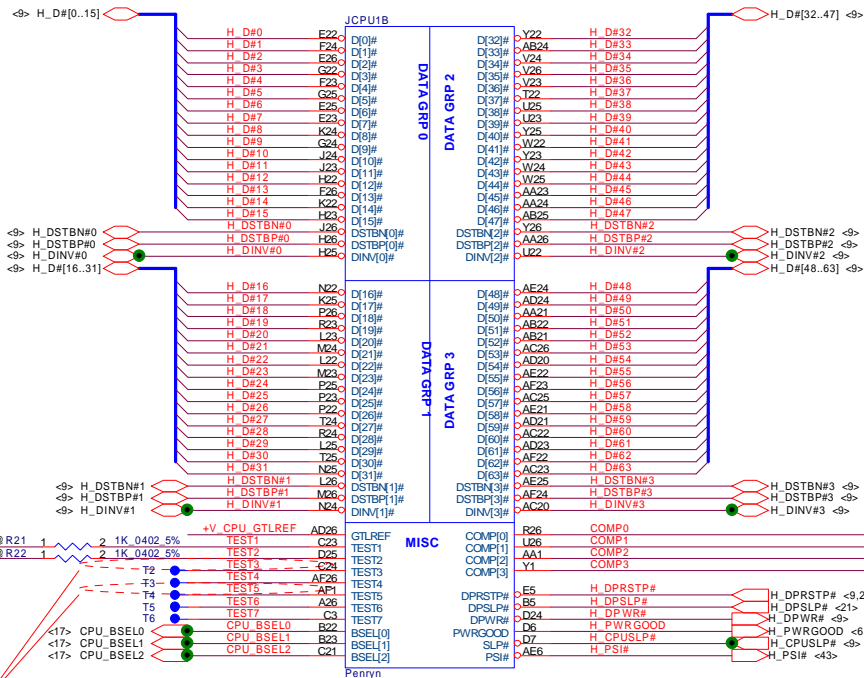
ITP-XDP Connector



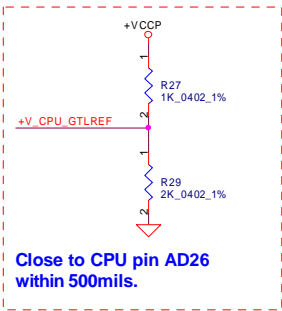
PWM Fan Control circuit



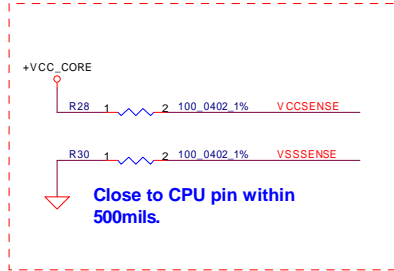
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Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

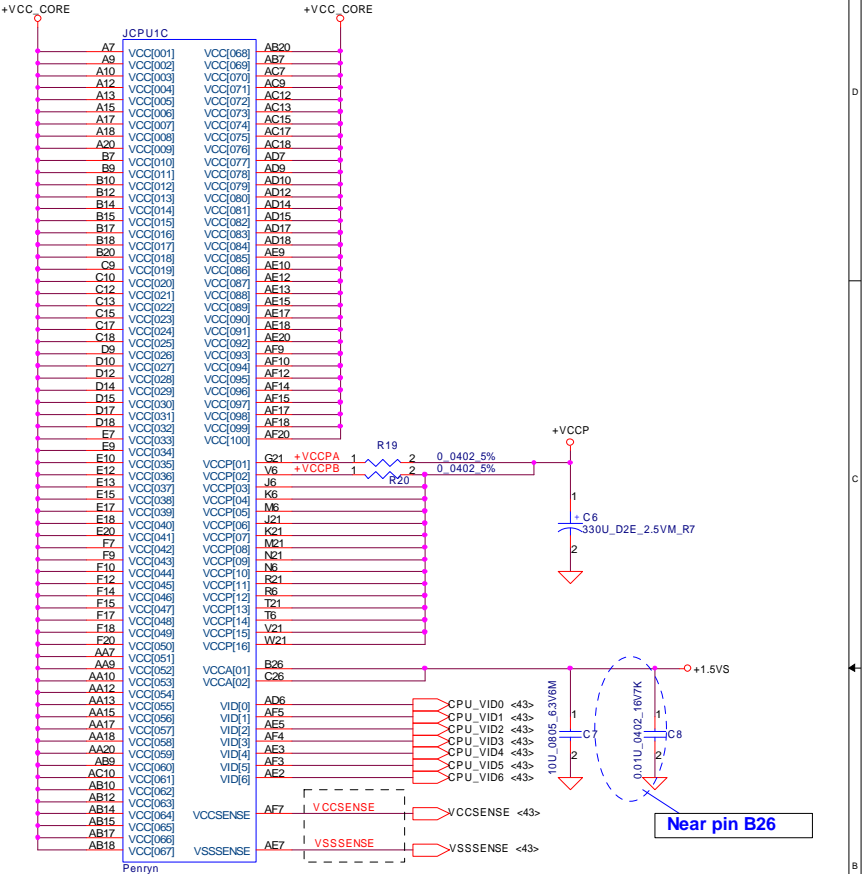


Length match within 25 mils. The trace width/space/other is 20/7/25.



* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

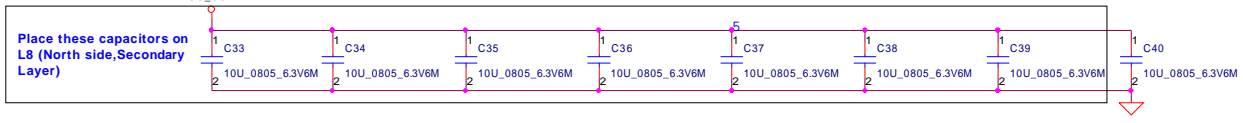
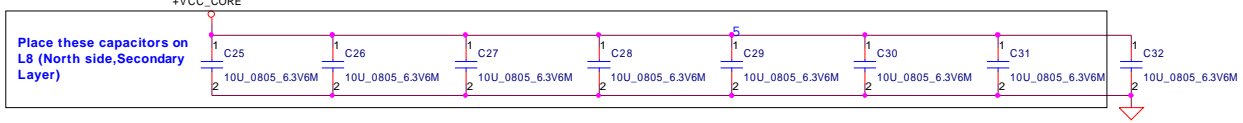
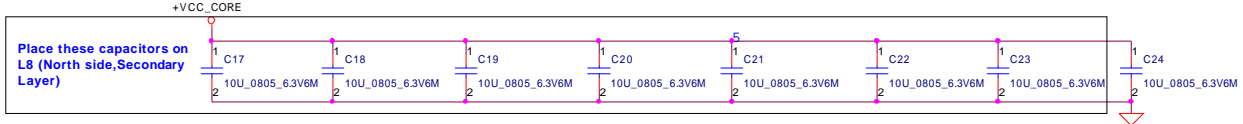
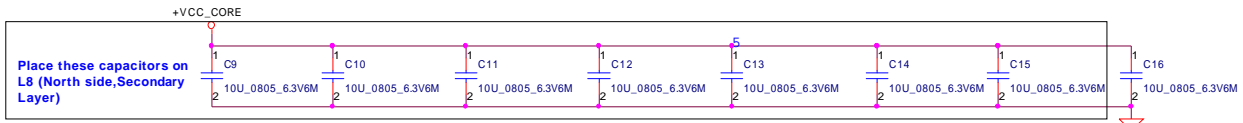


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Penryn(2/3)-AGTL+/ITP-XDP		
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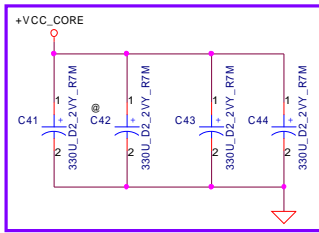
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JCPU1D		
A4	VSS1001	P6
A8	VSS1002	P21
A11	VSS1003	P24
A14	VSS1004	D2
A16	VSS1005	R5
A19	VSS1006	R22
A23	VSS1007	R25
A2	VSS1008	T1
A6	VSS1009	T4
B8	VSS1010	T23
B11	VSS1011	T26
B13	VSS1012	U8
B19	VSS1013	U21
B14	VSS1014	U25
B21	VSS1015	U24
B24	VSS1016	V2
C5	VSS1017	V5
C8	VSS1018	V22
C11	VSS1019	V25
C14	VSS1020	W1
C16	VSS1021	W4
C19	VSS1022	W23
C2	VSS1023	W26
C22	VSS1024	V6
C25	VSS1025	V21
D1	VSS1026	V24
D4	VSS1027	V28
D8	VSS1028	AA2
D11	VSS1029	AA5
D13	VSS1030	AA8
D16	VSS1031	AA11
D19	VSS1032	AA14
D23	VSS1033	AA16
D26	VSS1034	AA19
E3	VSS1035	AA22
E6	VSS1036	AA25
E8	VSS1037	AB1
E11	VSS1038	AB4
E14	VSS1039	AB8
E16	VSS1040	AB11
E19	VSS1041	AB13
E21	VSS1042	AB16
E24	VSS1043	AB19
F5	VSS1044	AB23
F8	VSS1045	AB26
F11	VSS1046	AC3
F13	VSS1047	AC6
F16	VSS1048	AC8
F19	VSS1049	AC11
F2	VSS1050	AC14
F22	VSS1051	AC16
F25	VSS1052	AC19
G4	VSS1053	AC21
G1	VSS1054	AC24
G23	VSS1055	AD2
G26	VSS1056	AD5
H3	VSS1057	AD8
H6	VSS1058	AD11
H21	VSS1059	AD13
H24	VSS1060	AD16
J2	VSS1061	AD19
J5	VSS1062	AD22
J22	VSS1063	AD25
J25	VSS1064	AE1
K1	VSS1065	AE4
K4	VSS1066	AE8
K23	VSS1067	AE11
K26	VSS1068	AE14
L3	VSS1069	AE16
L6	VSS1070	AE19
L21	VSS1071	AE23
L24	VSS1072	AE26
M2	VSS1073	A2
M5	VSS1074	AF6
M22	VSS1075	AF8
M25	VSS1076	AF11
N1	VSS1077	AF13
N4	VSS1078	AF16
N23	VSS1079	AF19
N26	VSS1080	AF21
P3	VSS1081	A25
	VSS1082	AF25
	VSS1083	

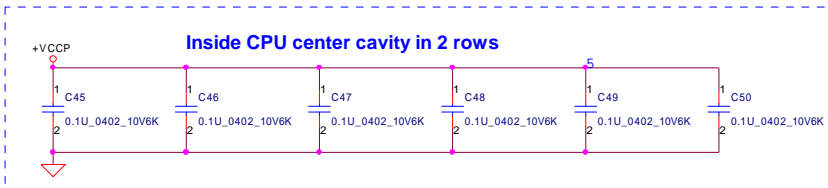


Mid Frequency Decoupling

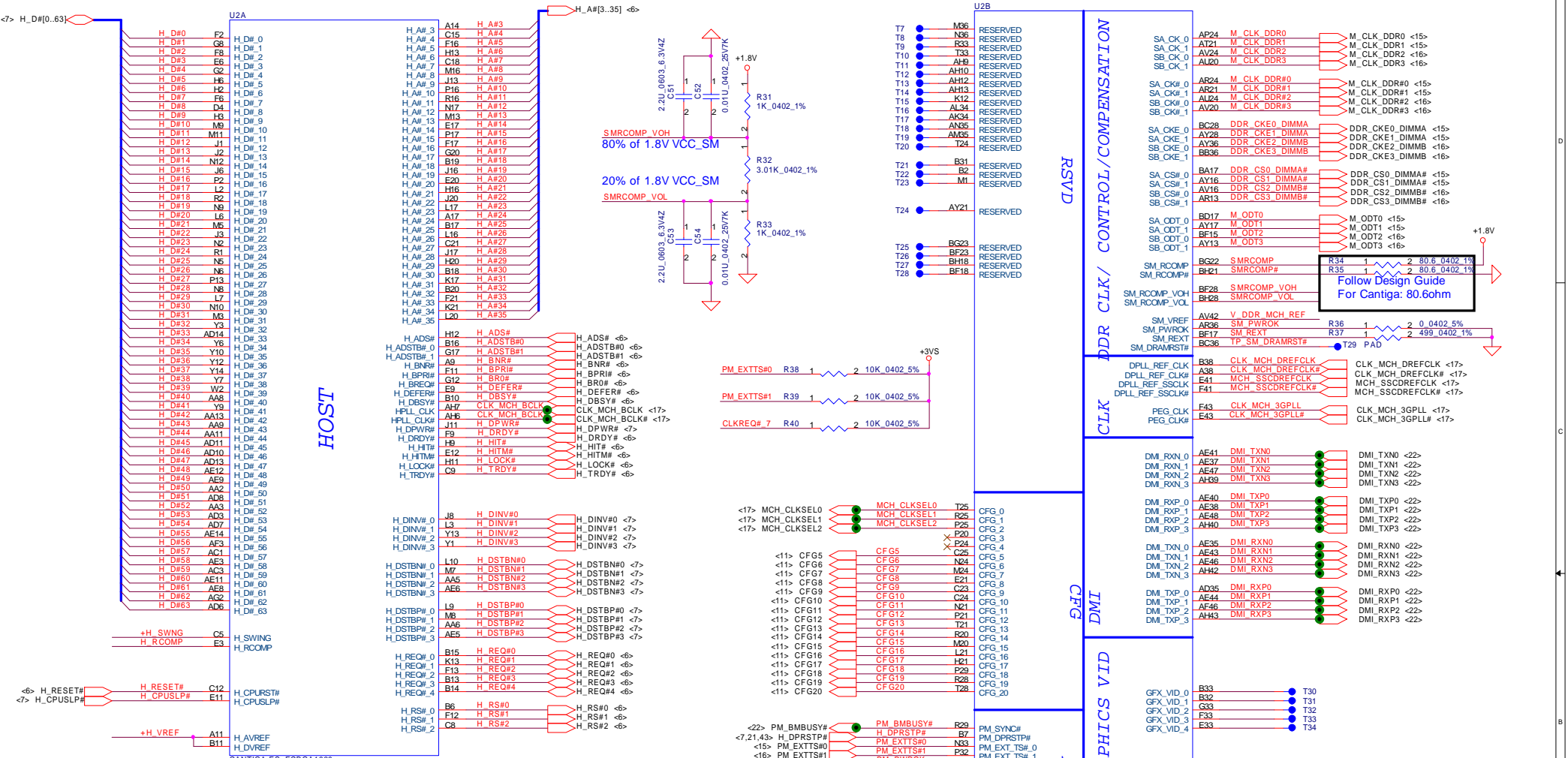
Near CPU CORE regulator
ESR <= 1.5m ohm
Capacitor > 1980uF



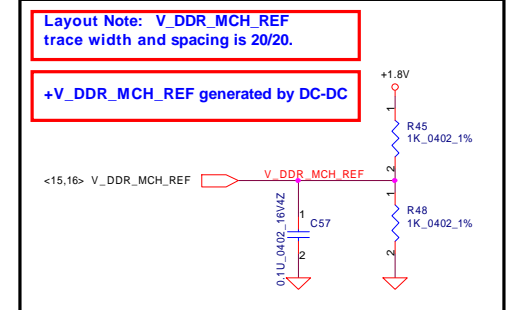
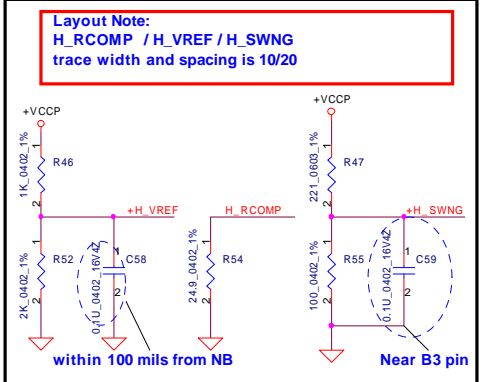
11/21 Change ESR=7m ohm



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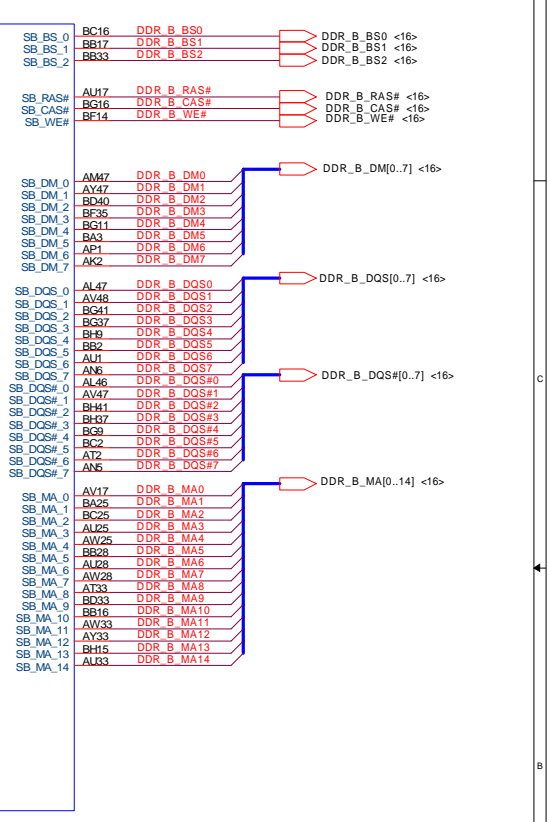
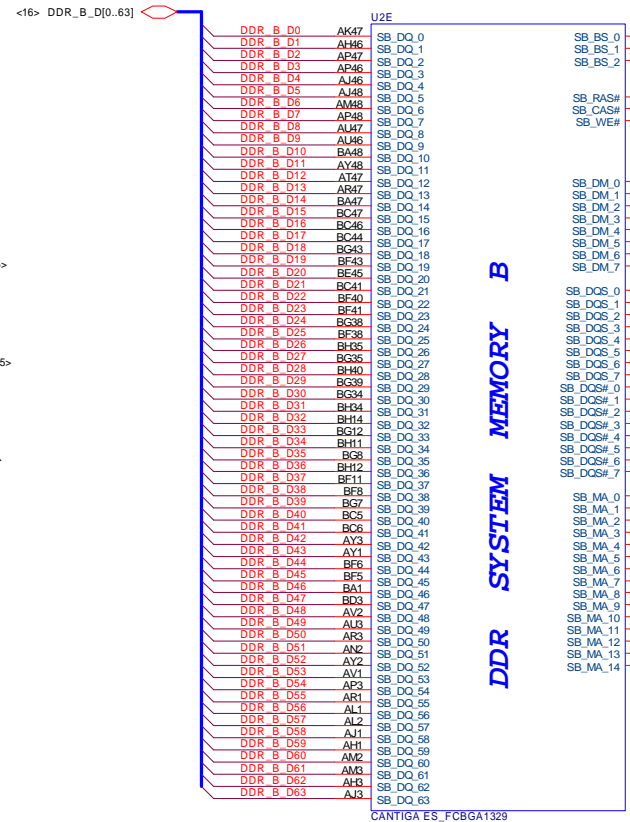
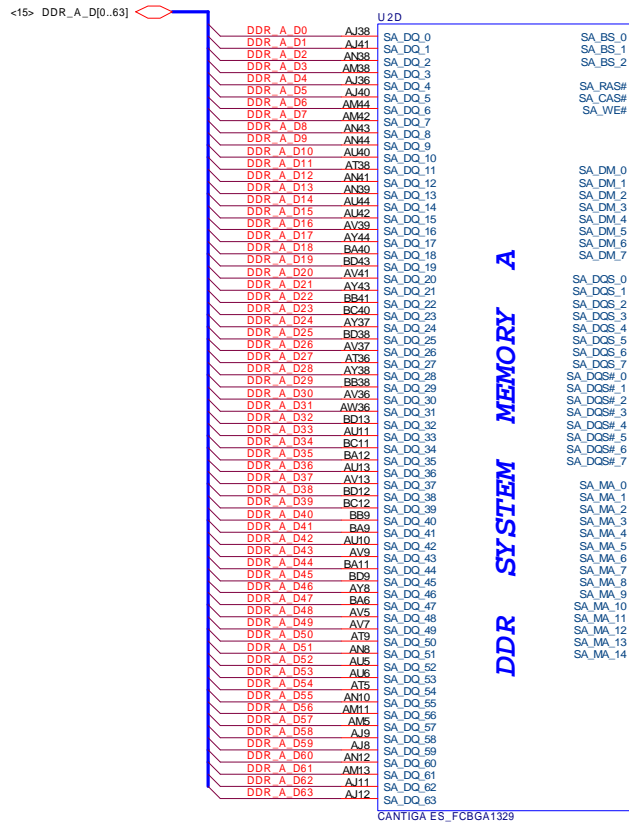
Layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces



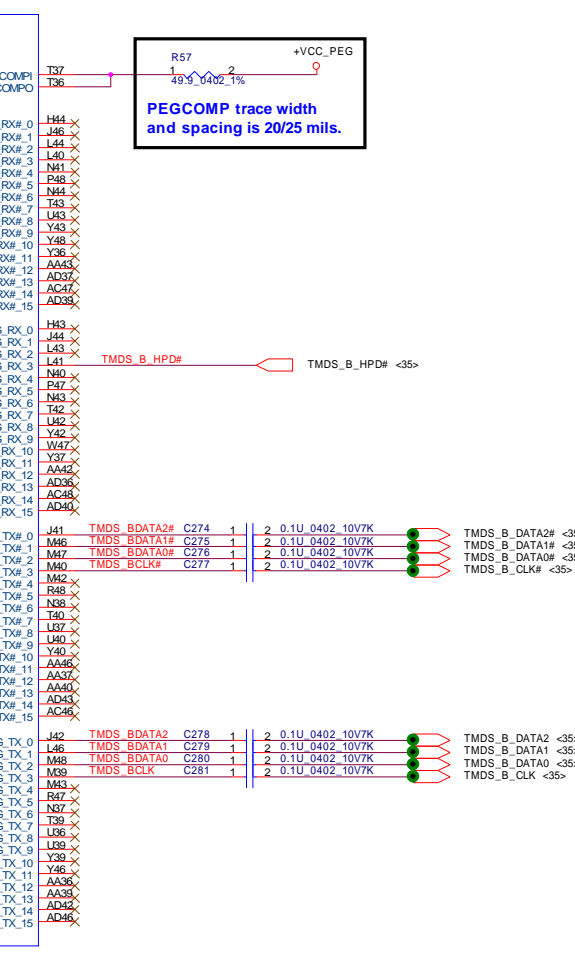
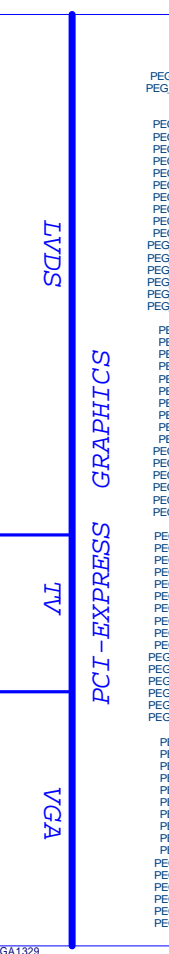
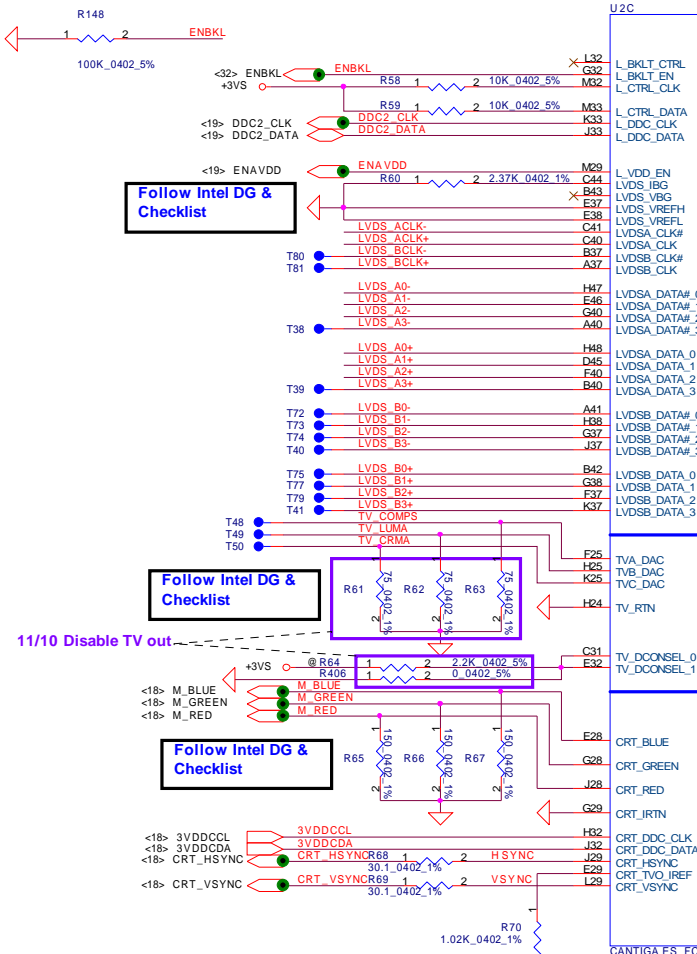
Follow Design Guide For Cantiga: 80.6ohm

R44 Follow Intel feedback

0830 Add pull-up and pull-down resistor.

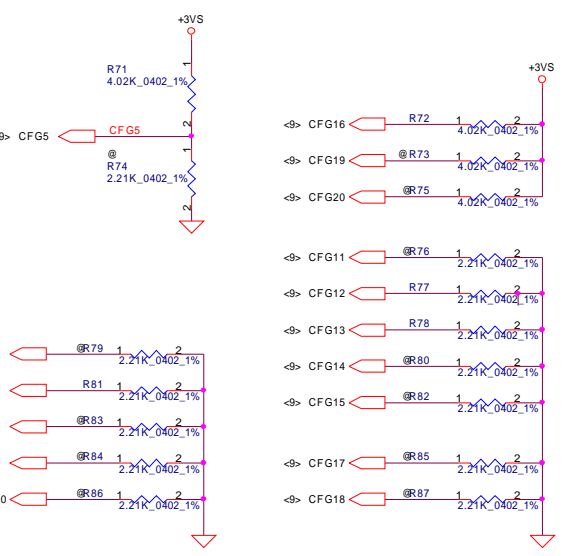
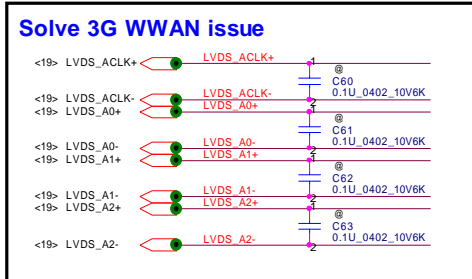


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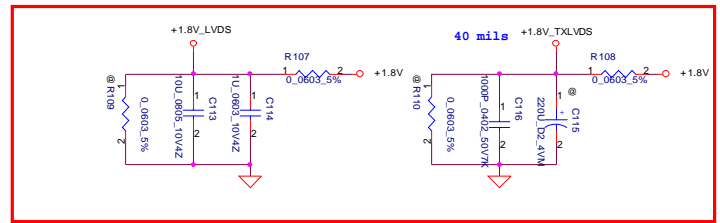
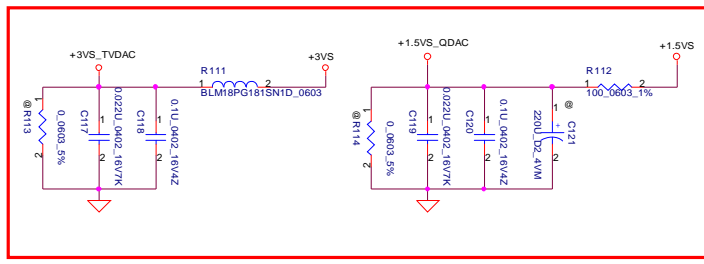
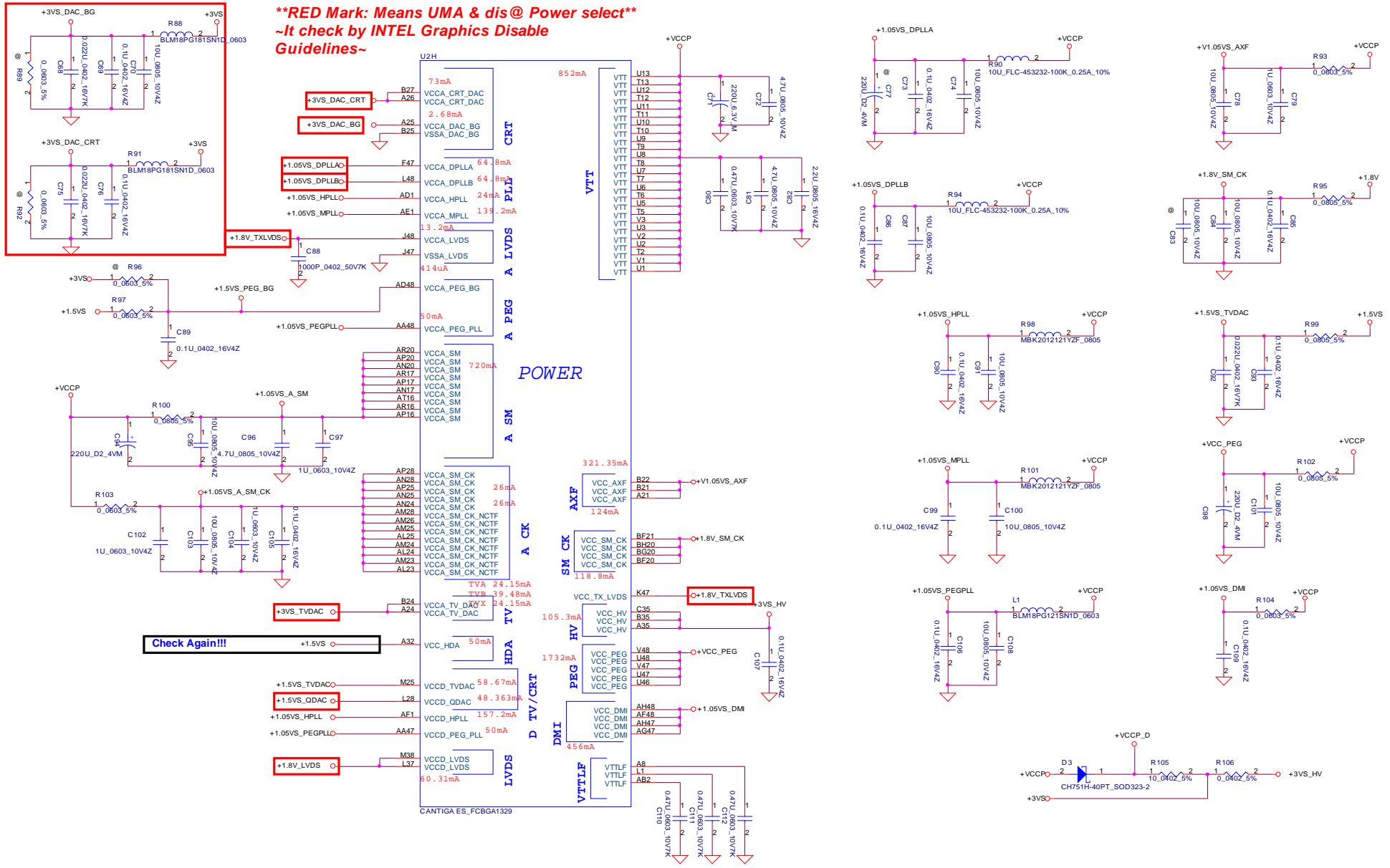
Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chiper suite with no confidentiality 1 = (TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled (Default) * 11 = Normal Operation
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

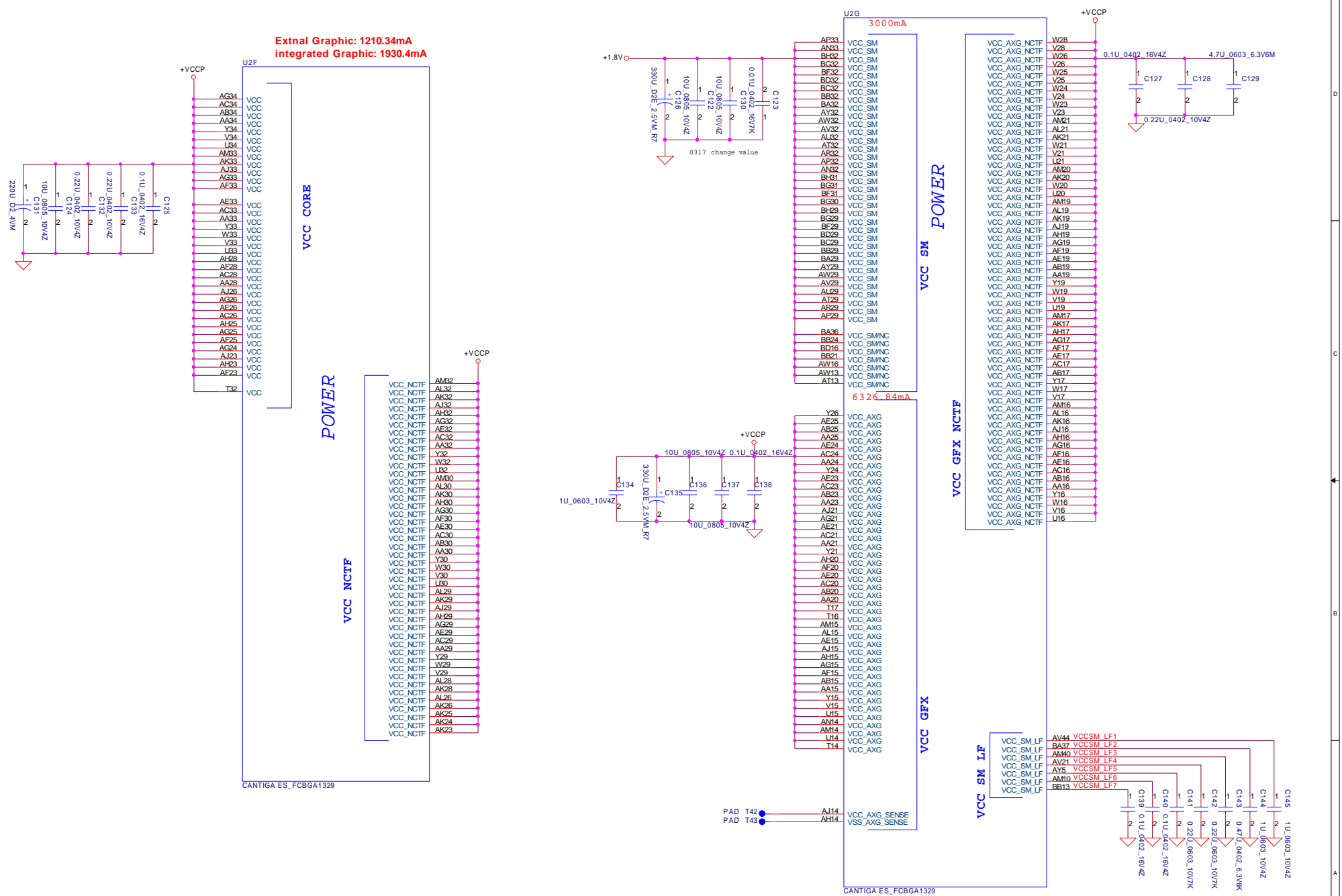


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****RED Mark: Means UMA & dis@ Power select****
~It check by INTEL Graphics Disable
Guidelines~



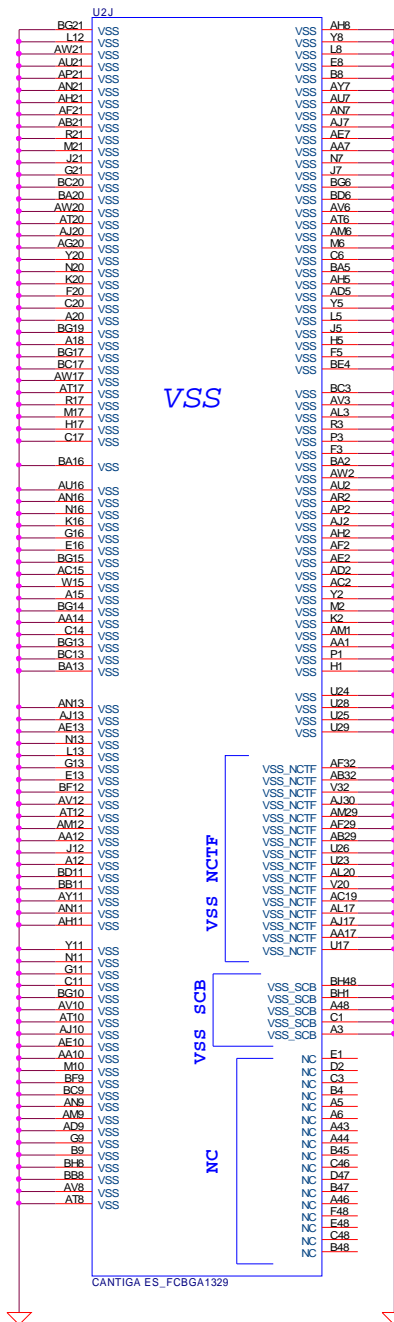
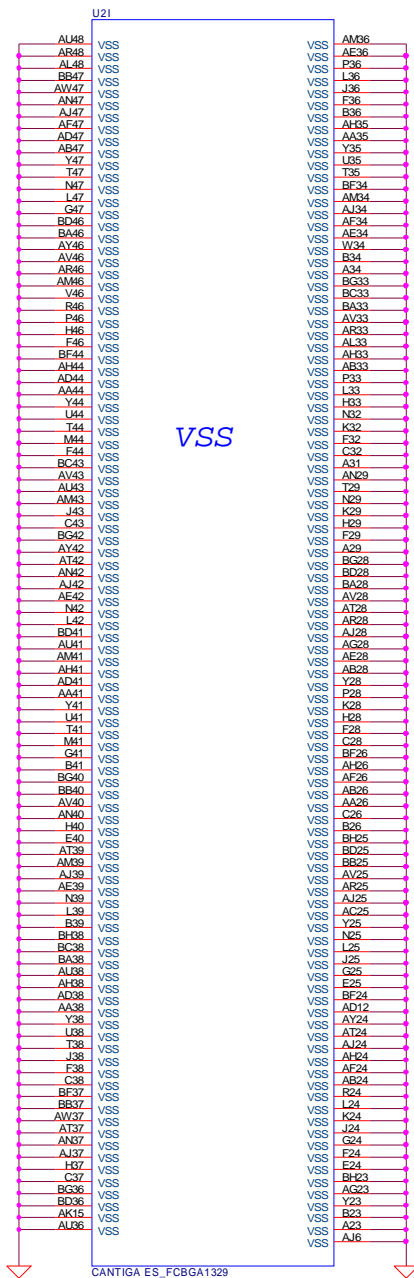
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Extnal Graphic: 1210.34mA
 Integrated Graphic: 1930.4mA

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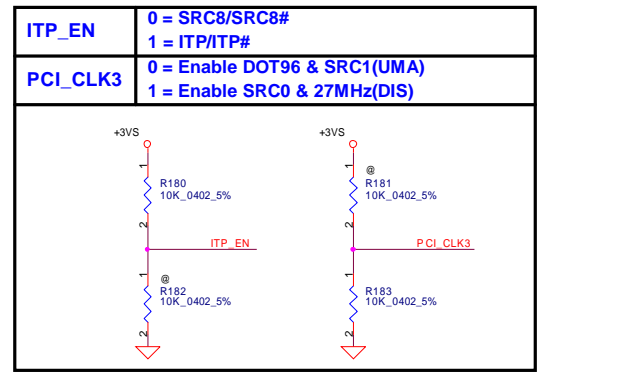
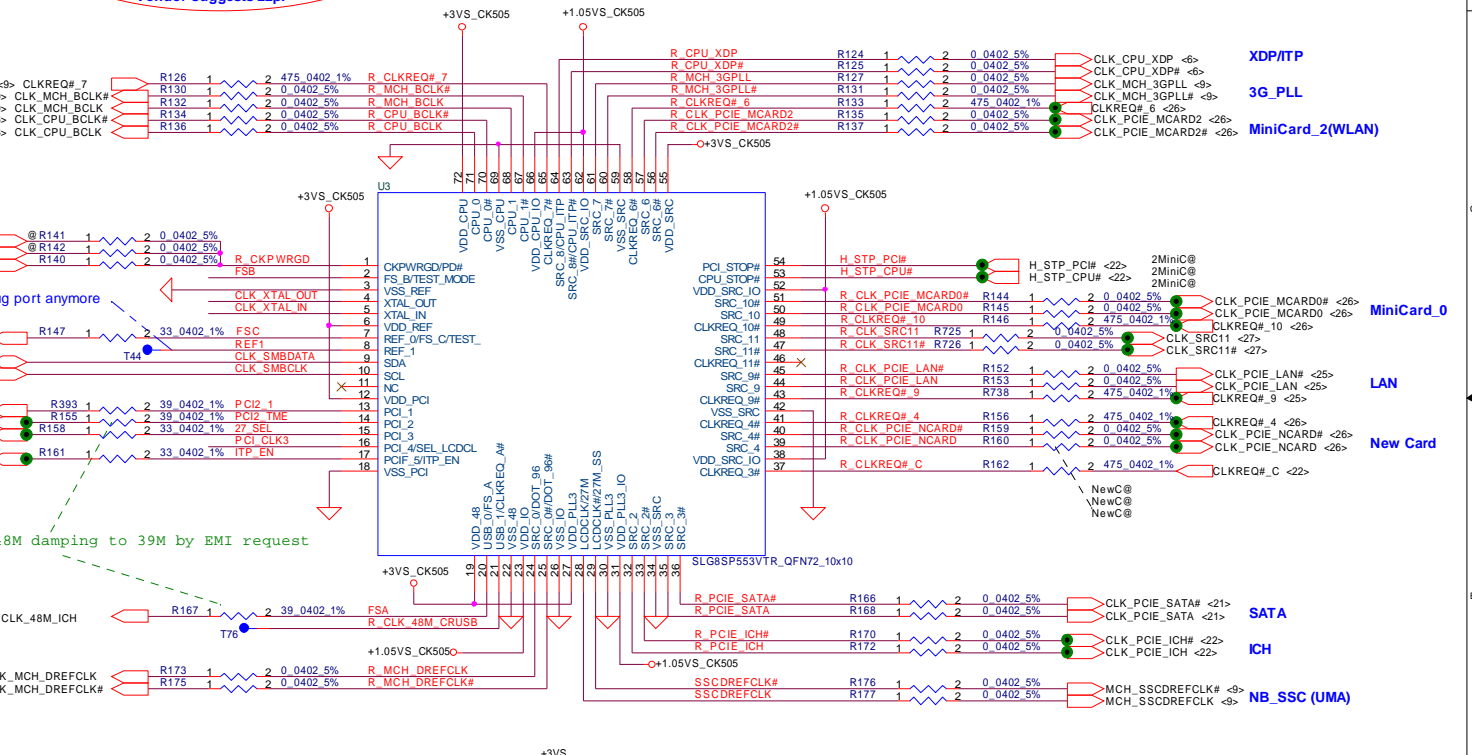
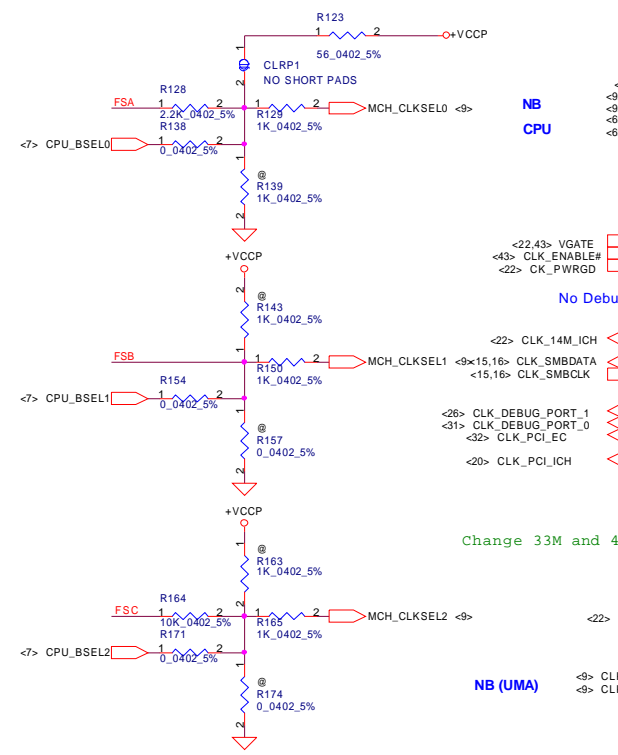
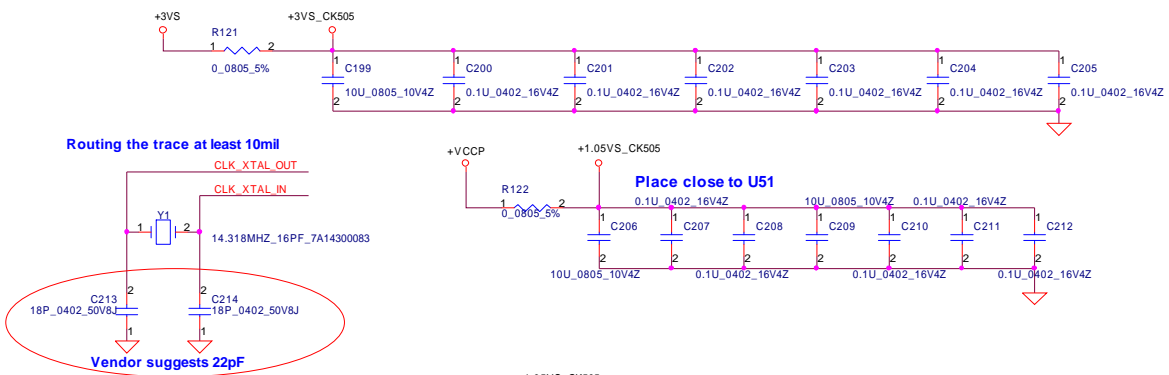
Title	
Compal Electronics, Inc.	
Cantiga(5/6)-PWR/GND	
Size	Document Number
Custom	Montevina Blade UMA LA4101P
Date:	Saturday, January 05, 2008
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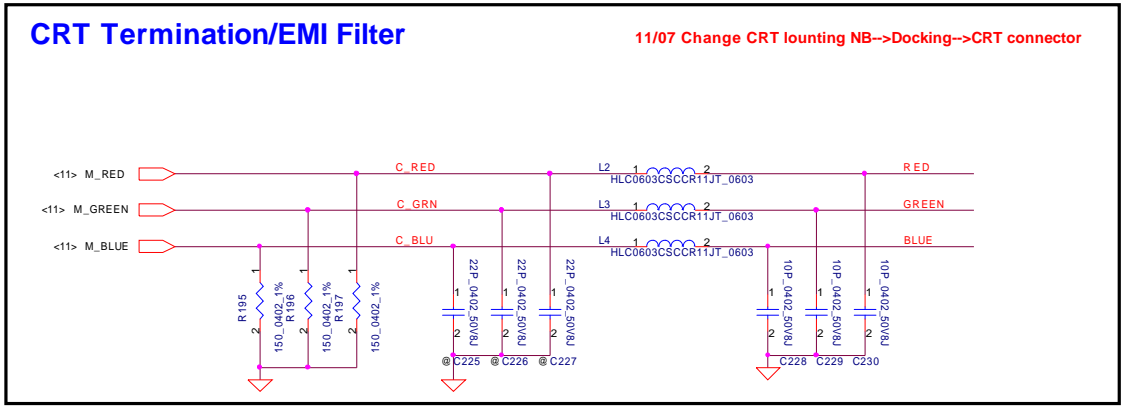
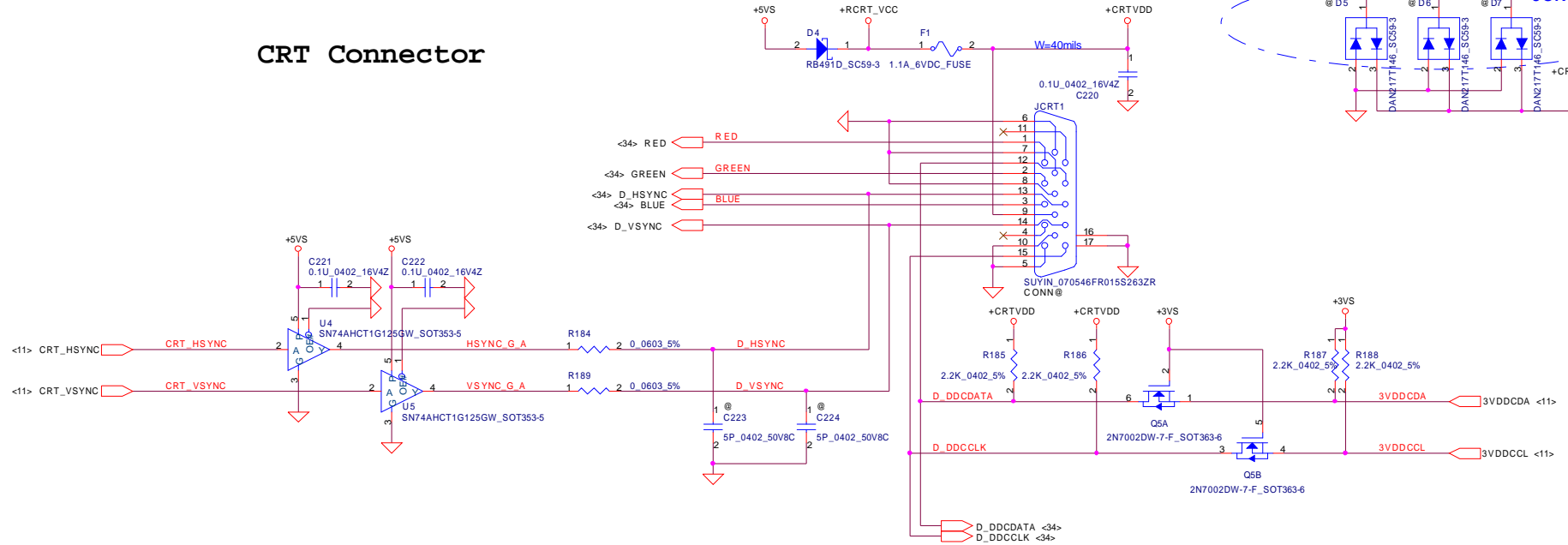
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CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						

Reserved

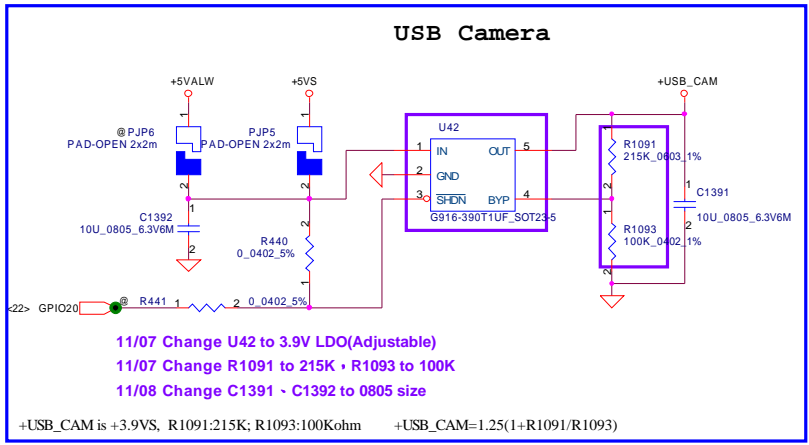
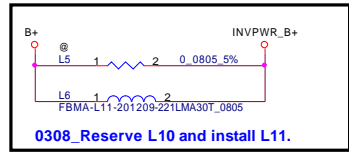
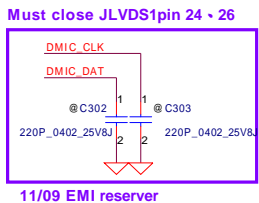
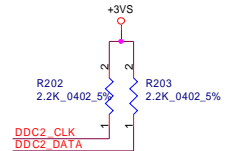
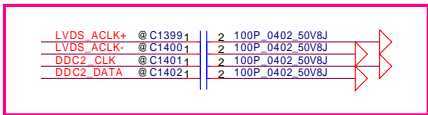
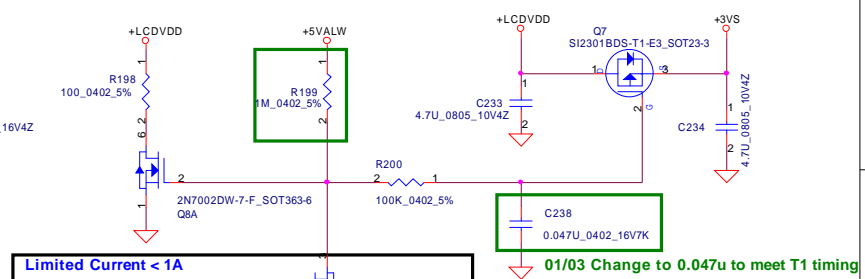
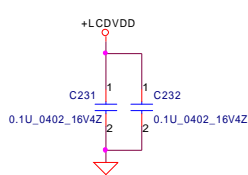
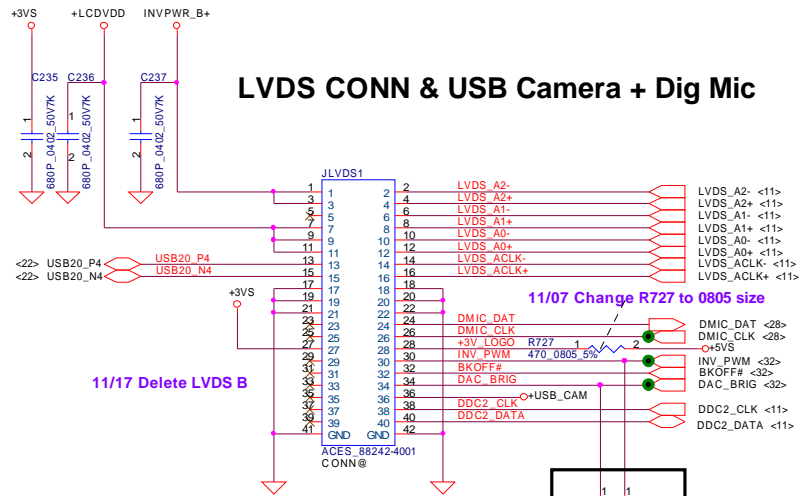


@C215	5P_0402_50V8C	2	1	CLK_48M_ICH
@C216	4.7P_0402_50V8C	2	1	CLK_14M_ICH
@C217	4.7P_0402_50V8C	2	1	CLK_PCI_ICH
@C218	4.7P_0402_50V8C	2	1	CLK_PCI_EC
@C219	5P_0402_50V8C	2	1	CLK_DEBUG_PORT_0

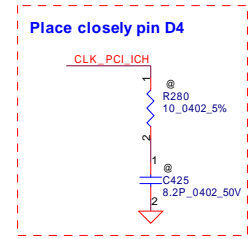
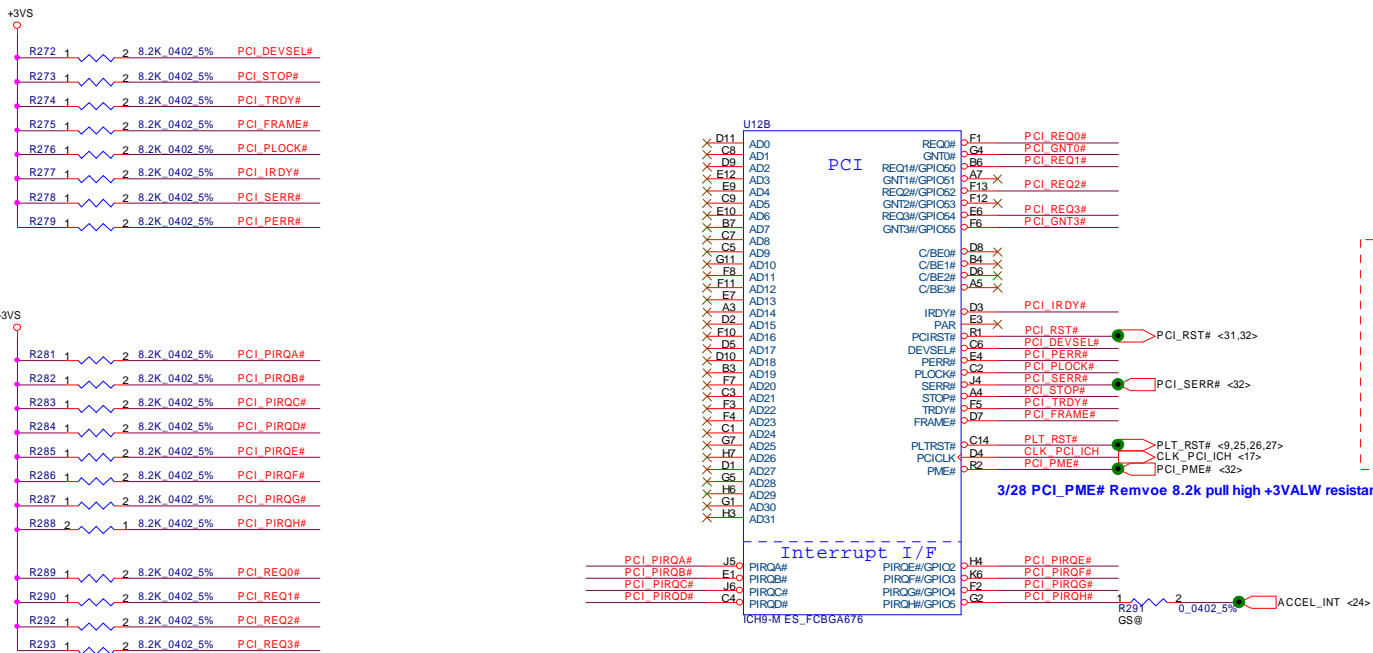
CRT Connector



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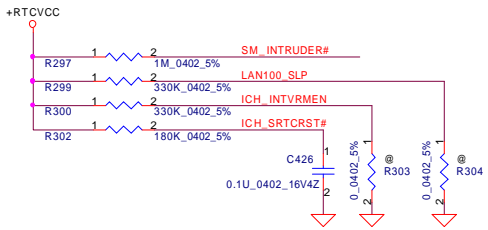
3/28 PCI_PME# Remove 8.2K pull high +3VALW resistance.

A16 swap override Strap

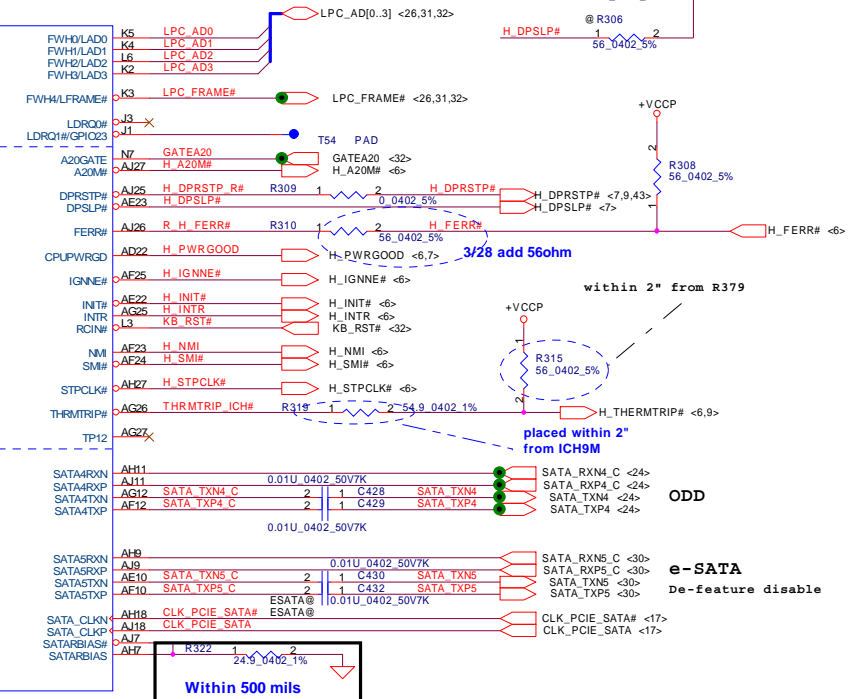
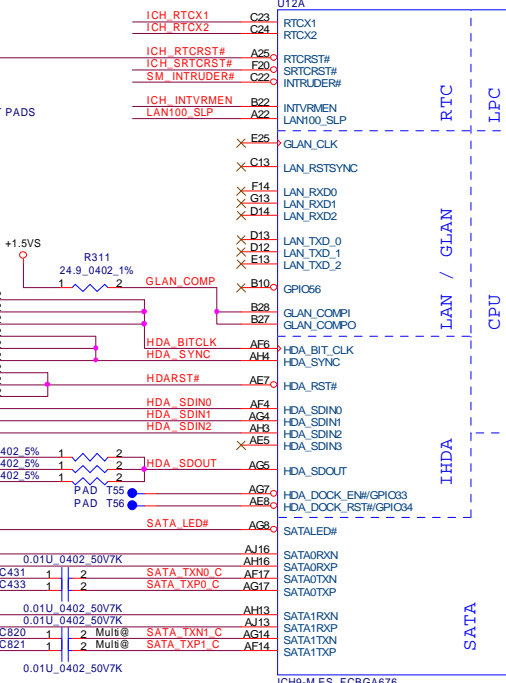
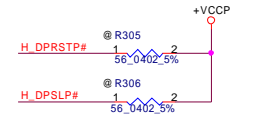
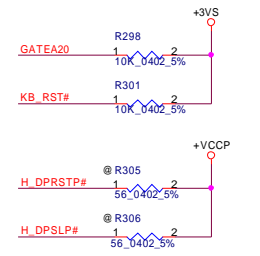
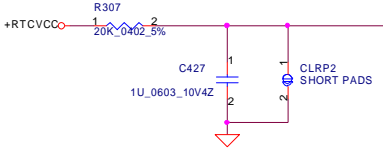
PCI_GNT3#	Low= A16 swap override Enable High= Default *
@R294 PCI_GNT3#	

Boot BIOS Strap

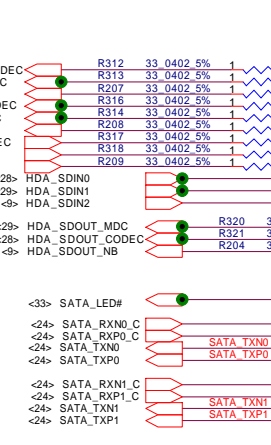
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



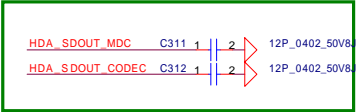
P-HDD



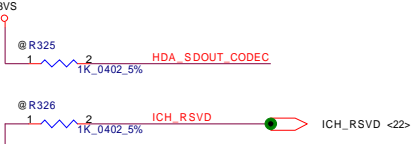
e-SATA
De-feature disable

Within 500 mils

Add 12p on HDA_SDO and HDA_SDO

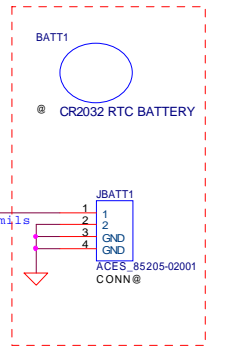
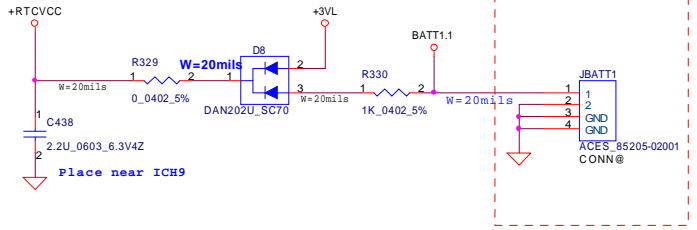
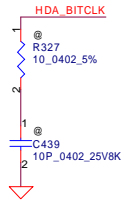
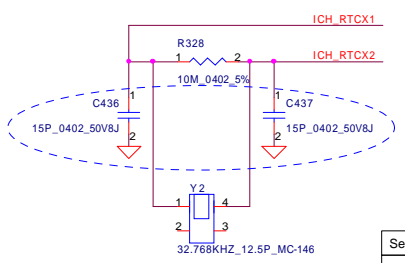


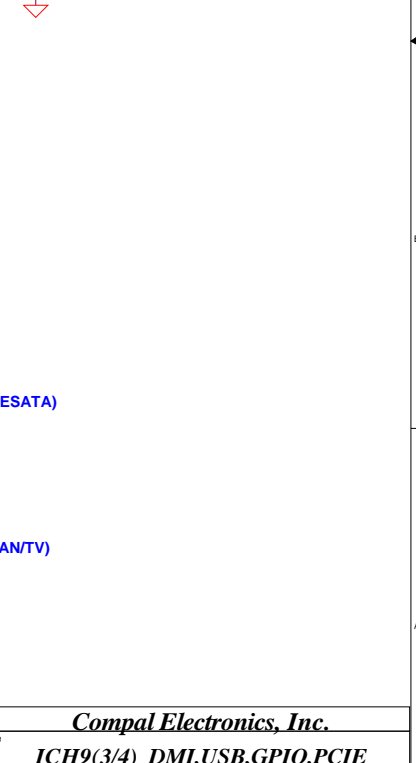
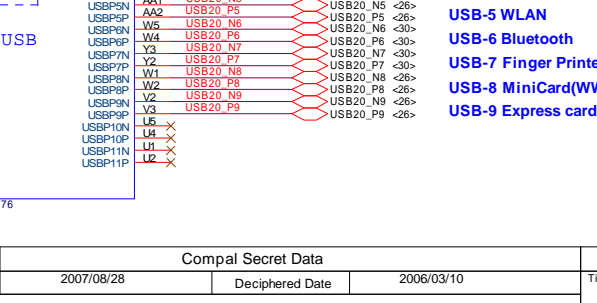
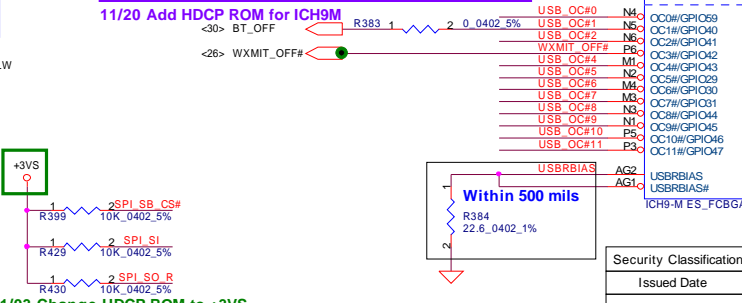
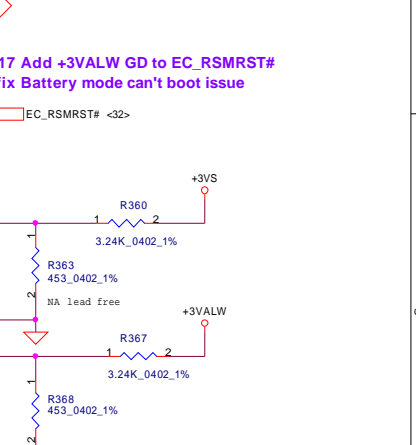
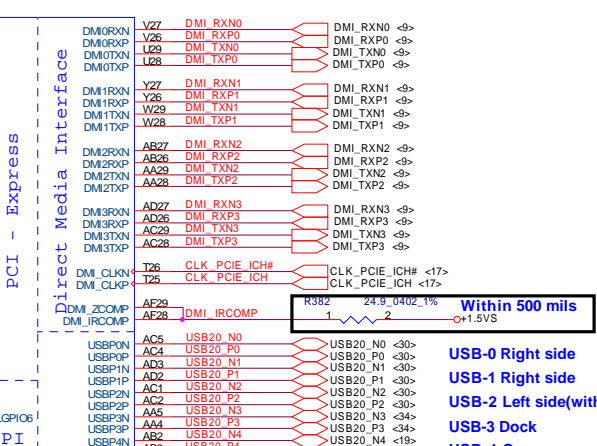
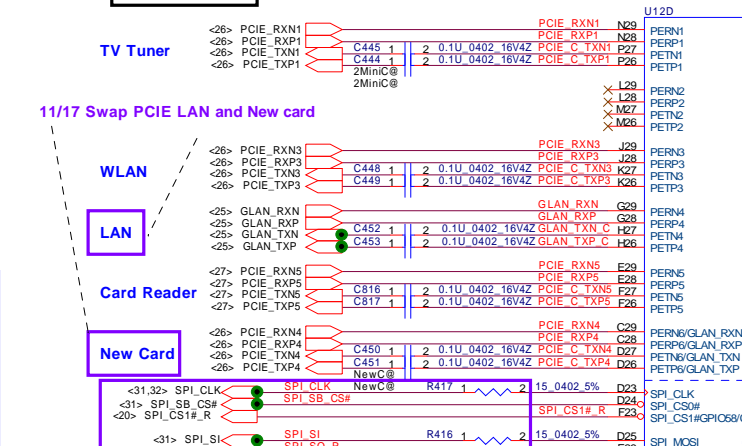
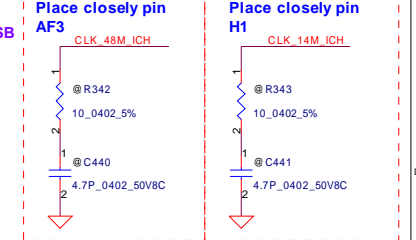
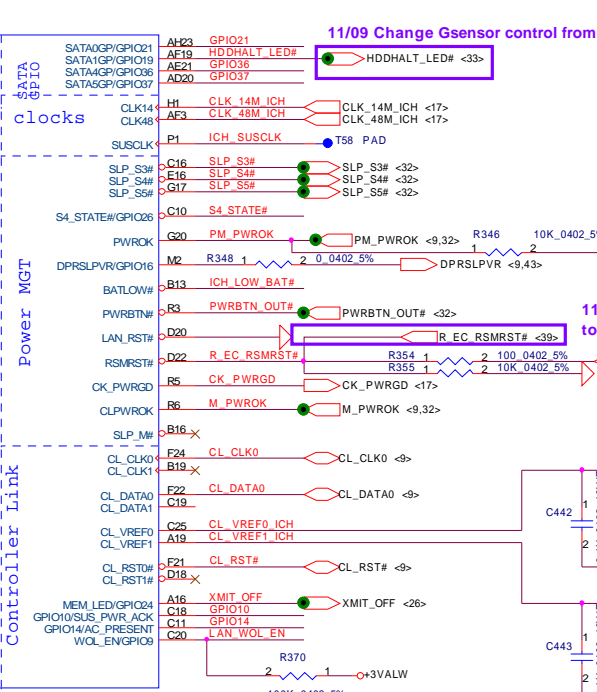
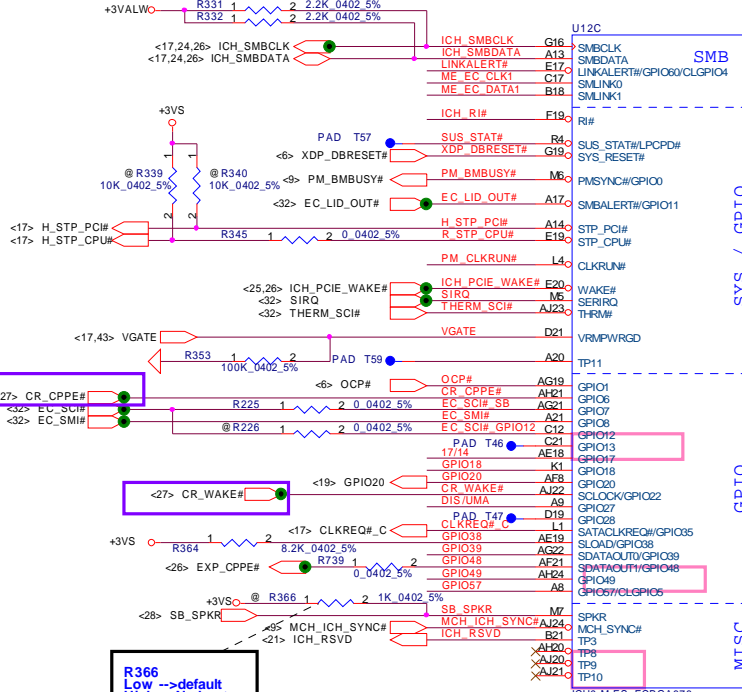
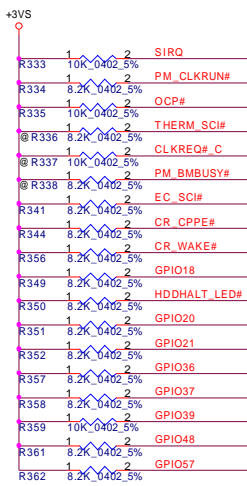
XOR CHAIN ENTRANCE STRAP:RSVD



ICH_RSVD	HDA_SDO_CODEC
0	0
0	1
1	0
1	1

0821 Change C528 and C516 to 15PF

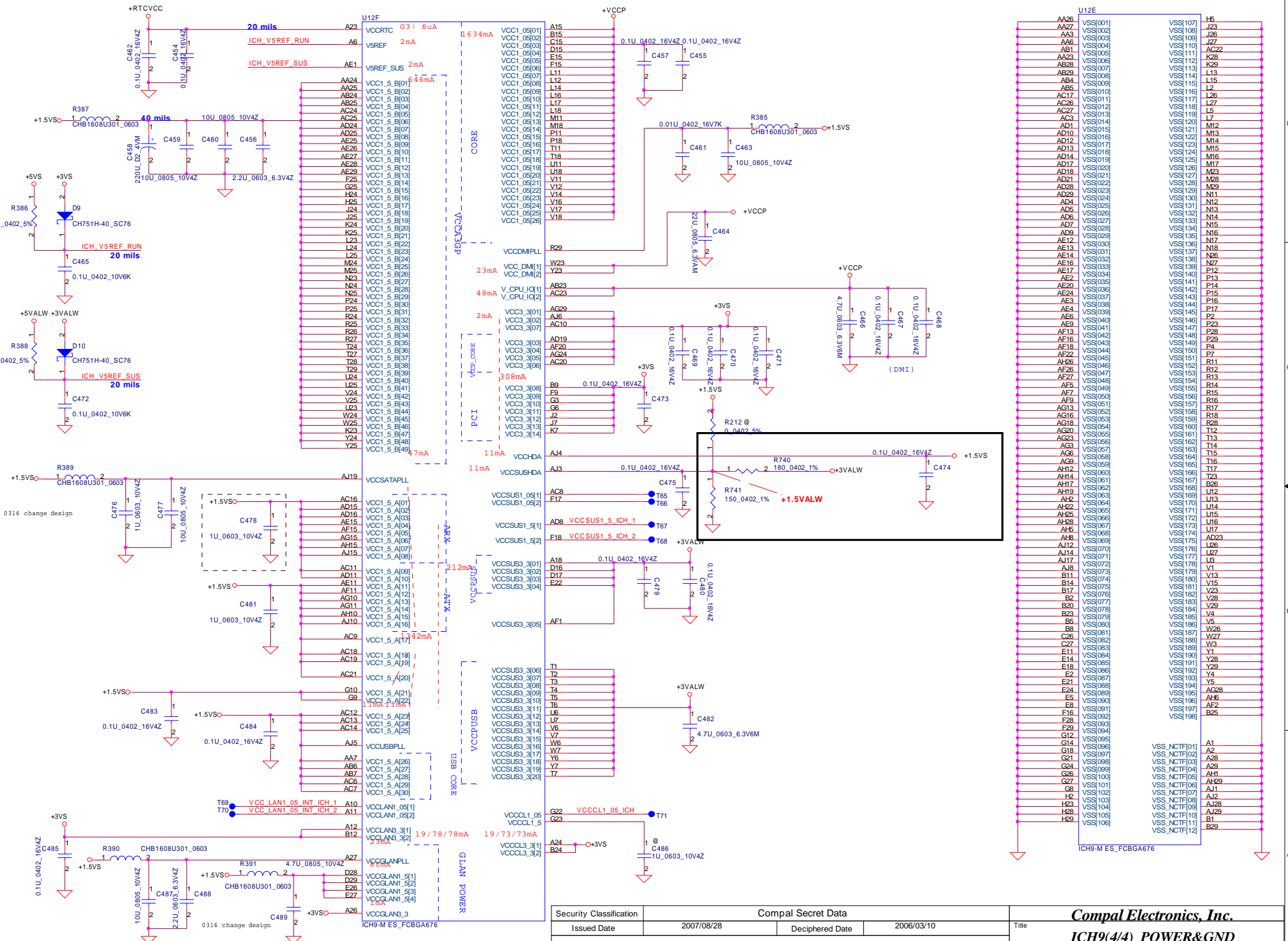




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ICH9(3/4) DMI,USB,GPIO,PCIE		
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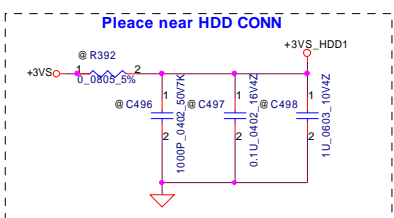
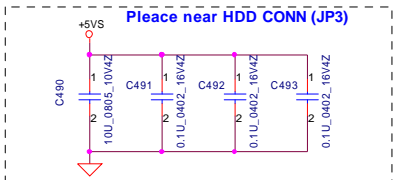
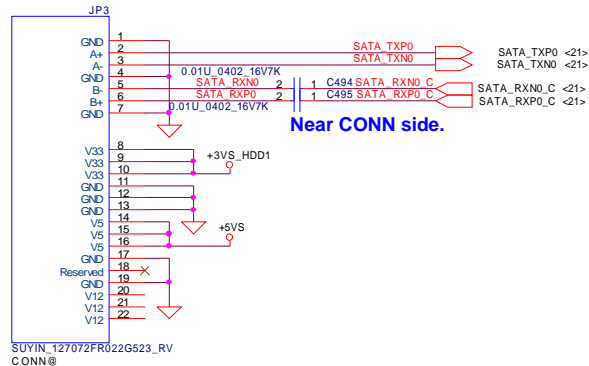
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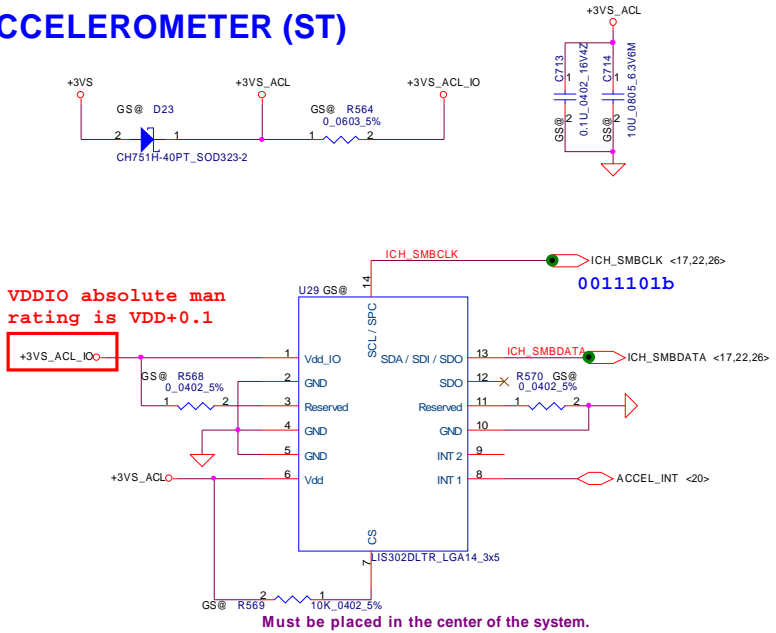
U12E	AA26	VSS[001]	VSS[107]	H5
	AA27	VSS[002]	VSS[108]	J23
	AA3	VSS[003]	VSS[109]	J26
	AA6	VSS[004]	VSS[110]	J27
	AB1	VSS[005]	VSS[111]	AC22
	AA23	VSS[006]	VSS[112]	K28
	AB28	VSS[007]	VSS[113]	K29
	AB29	VSS[008]	VSS[114]	L13
	AB4	VSS[009]	VSS[115]	L15
	AB5	VSS[010]	VSS[116]	L2
	AC17	VSS[011]	VSS[117]	L26
	AC26	VSS[012]	VSS[118]	L27
	AC27	VSS[013]	VSS[119]	L5
	AC3	VSS[014]	VSS[120]	L7
	AD1	VSS[015]	VSS[121]	M12
	AD10	VSS[016]	VSS[122]	M13
	AD11	VSS[017]	VSS[123]	M14
	AD13	VSS[018]	VSS[124]	M15
	AD14	VSS[019]	VSS[125]	M16
	AD17	VSS[020]	VSS[126]	M17
	AD18	VSS[021]	VSS[127]	M2
	AD21	VSS[022]	VSS[128]	M29
	AD28	VSS[023]	VSS[129]	M29
	AD29	VSS[024]	VSS[130]	N11
	AD4	VSS[025]	VSS[131]	N12
	AD6	VSS[026]	VSS[132]	N13
	AD7	VSS[027]	VSS[133]	N14
	AD9	VSS[028]	VSS[134]	N15
	AE12	VSS[029]	VSS[135]	N16
	AE13	VSS[030]	VSS[136]	N17
	AE14	VSS[031]	VSS[137]	N2
	AE15	VSS[032]	VSS[138]	N26
	AE16	VSS[033]	VSS[139]	N27
	AE17	VSS[034]	VSS[140]	N28
	AE2	VSS[035]	VSS[141]	P12
	AE24	VSS[036]	VSS[142]	P13
	AE3	VSS[037]	VSS[143]	P14
	AE4	VSS[038]	VSS[144]	P15
	AE9	VSS[039]	VSS[145]	P16
	AF1	VSS[040]	VSS[146]	P2
	AF16	VSS[041]	VSS[147]	P22
	AF18	VSS[042]	VSS[148]	P29
	AF22	VSS[043]	VSS[149]	P4
	AF24	VSS[044]	VSS[150]	P7
	AF25	VSS[045]	VSS[151]	R11
	AF27	VSS[046]	VSS[152]	R12
	AF3	VSS[047]	VSS[153]	R13
	AF7	VSS[048]	VSS[154]	R14
	AF9	VSS[049]	VSS[155]	R16
	AG13	VSS[050]	VSS[156]	R17
	AG16	VSS[051]	VSS[157]	R18
	AG18	VSS[052]	VSS[158]	R28
	AG20	VSS[053]	VSS[159]	T12
	AG23	VSS[054]	VSS[160]	T13
	AG3	VSS[055]	VSS[161]	T14
	AG6	VSS[056]	VSS[162]	T15
	AH1	VSS[057]	VSS[163]	T16
	AH12	VSS[058]	VSS[164]	T17
	AH14	VSS[059]	VSS[165]	T23
	AH17	VSS[060]	VSS[166]	B26
	AH22	VSS[061]	VSS[167]	U12
	AH25	VSS[062]	VSS[168]	U13
	AH28	VSS[063]	VSS[169]	U14
	AH5	VSS[064]	VSS[170]	U15
	AH8	VSS[065]	VSS[171]	U16
	AH12	VSS[066]	VSS[172]	U17
	AH14	VSS[067]	VSS[173]	AD23
	AH17	VSS[068]	VSS[174]	U26
	AH18	VSS[069]	VSS[175]	U27
	AH19	VSS[070]	VSS[176]	U3
	AH22	VSS[071]	VSS[177]	V1
	AH25	VSS[072]	VSS[178]	V13
	AH28	VSS[073]	VSS[179]	V22
	B11	VSS[074]	VSS[180]	V25
	B17	VSS[075]	VSS[181]	Y2
	B2	VSS[076]	VSS[182]	Y4
	B20	VSS[077]	VSS[183]	Y5
	B23	VSS[078]	VSS[184]	AC28
	B5	VSS[079]	VSS[185]	AH6
	B8	VSS[080]	VSS[186]	AF2
	C26	VSS[081]	VSS[187]	B25
	C27	VSS[082]	VSS[188]	W26
	E11	VSS[083]	VSS[189]	W27
	E14	VSS[084]	VSS[190]	W3
	E18	VSS[085]	VSS[191]	Y1
	E21	VSS[086]	VSS[192]	Y2
	E22	VSS[087]	VSS[193]	Y4
	E24	VSS[088]	VSS[194]	Y5
	E5	VSS[089]	VSS[195]	AC29
	E8	VSS[090]	VSS[196]	AH6
	F16	VSS[091]	VSS[197]	AF2
	F18	VSS[092]	VSS[198]	B25
	F28	VSS[093]	VSS[199]	
	F29	VSS[094]	VSS[200]	
	G12	VSS[095]	VSS[201]	
	G14	VSS[096]	VSS[202]	
	G17	VSS[097]	VSS[203]	
	G21	VSS[098]	VSS[204]	
	G24	VSS[099]	VSS[205]	
	G26	VSS[100]	VSS[206]	
	G27	VSS[101]	VSS[207]	
	G8	VSS[102]	VSS[208]	
	H2	VSS[103]	VSS[209]	
	H23	VSS[104]	VSS[210]	
	L28	VSS[105]	VSS[211]	
	H29	VSS[106]	VSS[212]	
		VSS_NCTF[01]	A1	
		VSS_NCTF[02]	A2	
		VSS_NCTF[03]	A28	
		VSS_NCTF[04]	A29	
		VSS_NCTF[05]	AH	
		VSS_NCTF[06]	AH23	
		VSS_NCTF[07]	AJ1	
		VSS_NCTF[08]	AJ2	
		VSS_NCTF[09]	AJ28	
		VSS_NCTF[10]	AJ29	
		VSS_NCTF[11]	B1	
		VSS_NCTF[12]	B29	

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			Rev: 0.3 Sheet 23 of 46

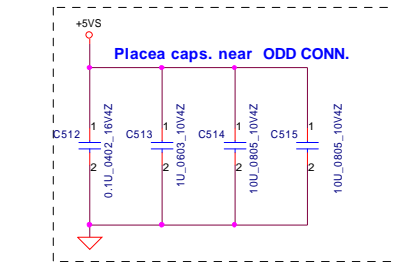
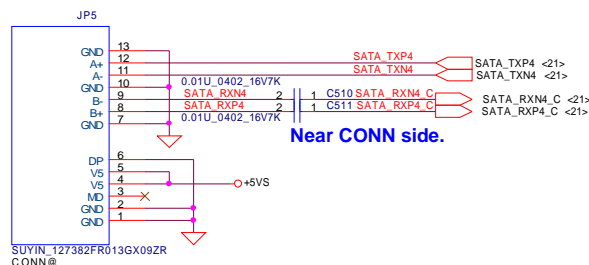
HDD Connector



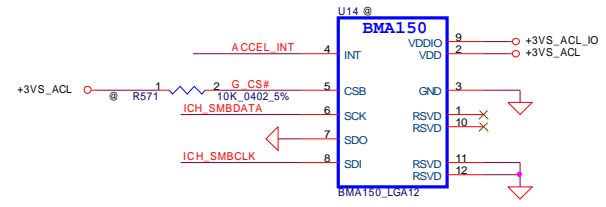
ACCELEROMETER (ST)



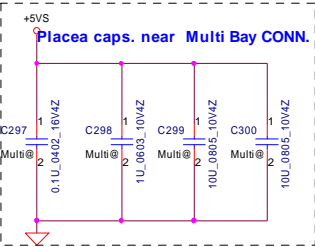
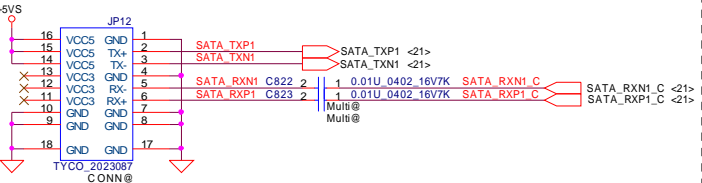
CD-ROM Connector



ACCELEROMETER (Bosch)



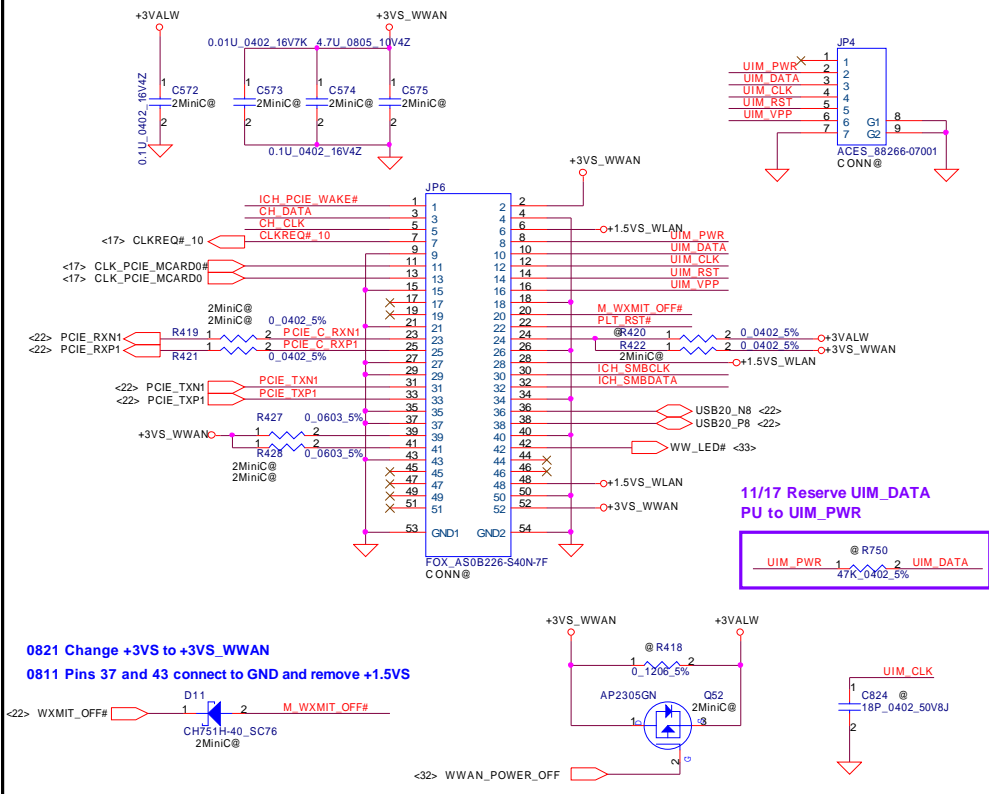
Multi Bay



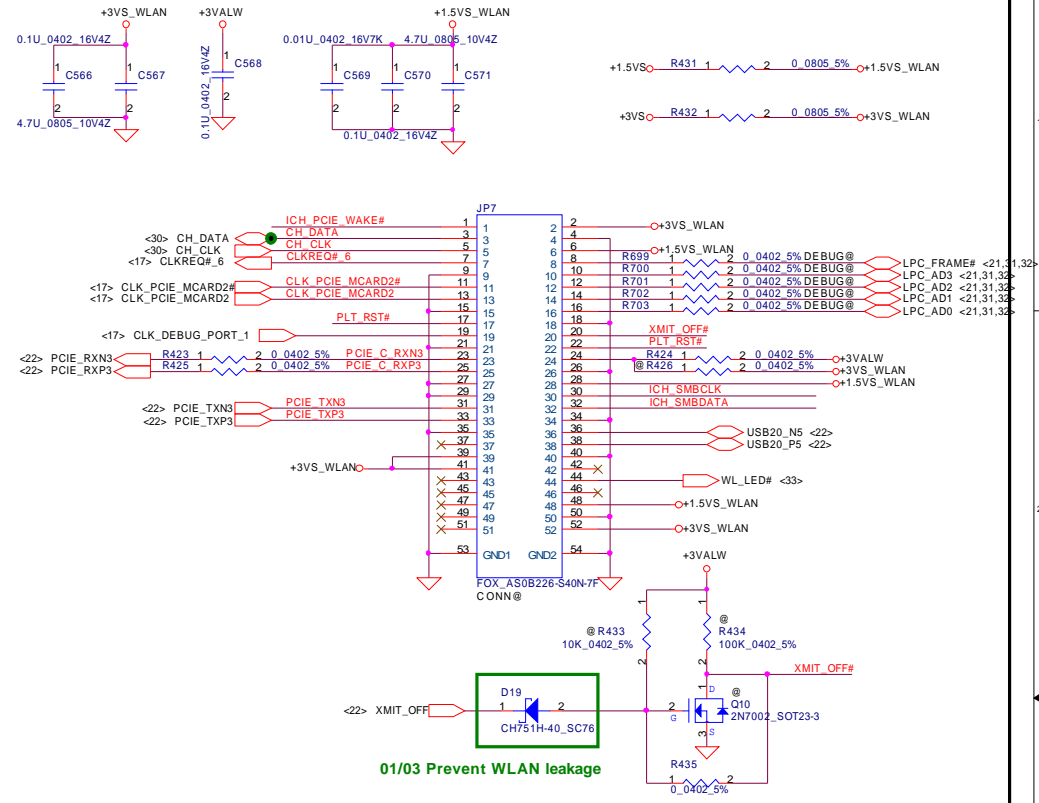
Security Classification	Compal Secret Data	
Issued Date	2007/08/28	Deciphered Date
		2006/03/10
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Compal Electronics, Inc.	
HDD & CDROM	
Size	Document Number
Custom	Montevina Blade UMA LA410P
Date:	Saturday, January 05, 2008
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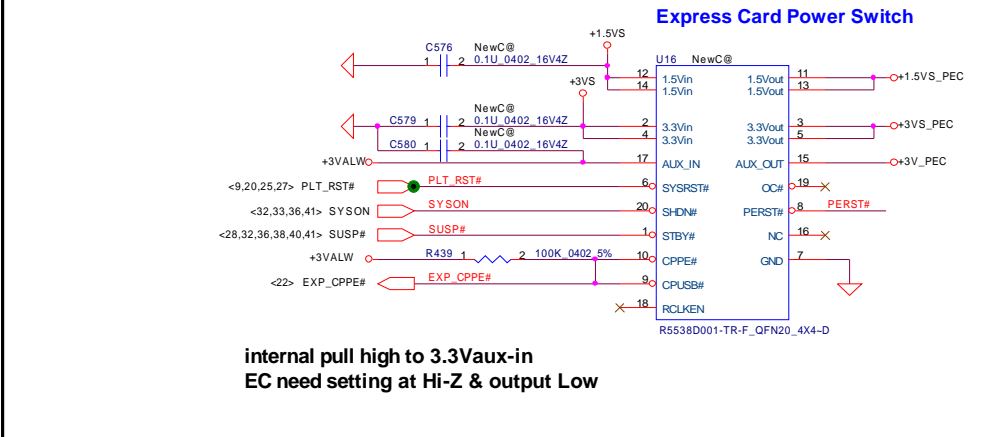
Mini Card 0--TV tuner/WWAN/Robson SIM card Connector



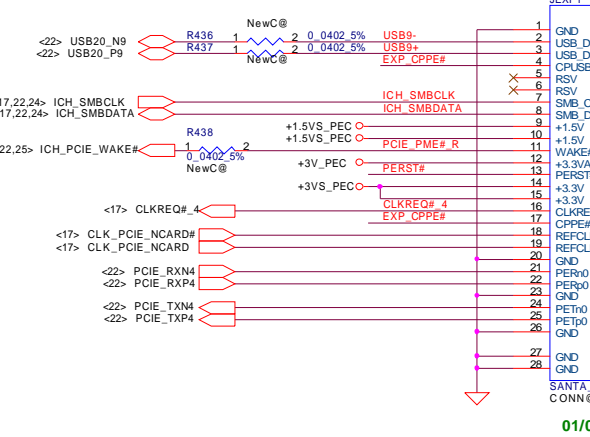
Mini Card 2---WLAN



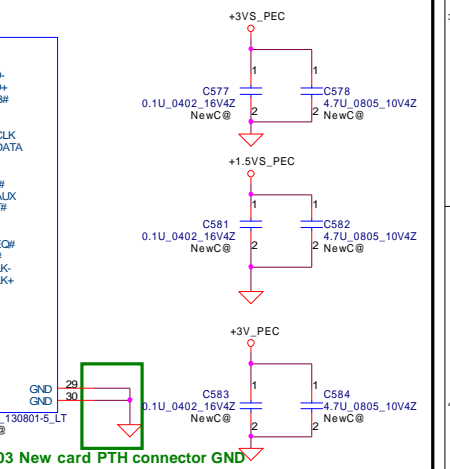
New Card



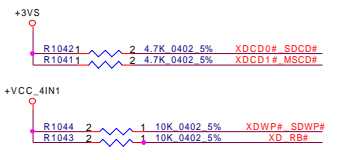
Close to JEXP



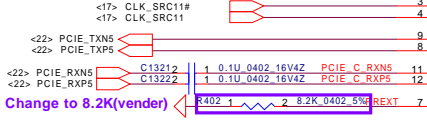
Near to Express Card slot.



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					Montevina Blade UMA LA4101P	0.3
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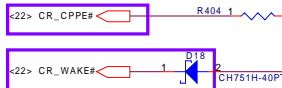


09/26 (JMicron)recommend width/length: 12mil / <250mil for PREXT signal (pin 7)



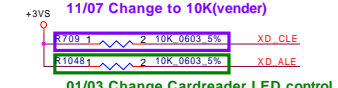
11/07 Change to 8.2K(vender)

09/26 (JMicron)recommend add a test point for pin 13 - 14



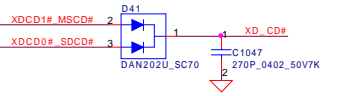
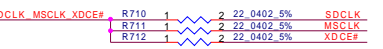
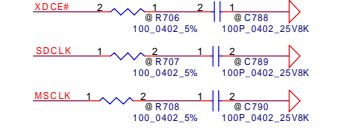
11/09 Add D18 for cardreader wake up

use for PWR_EN#
CR_LED#
8mA sink current



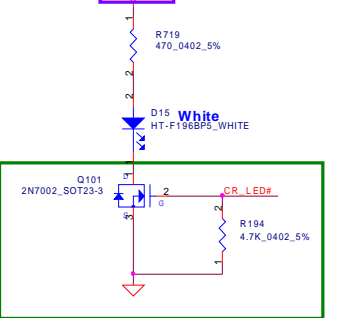
11/07 Change to 10K(vender)

01/03 Change Cardreader LED control

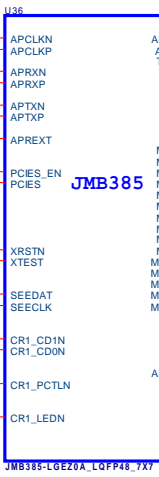


White LED: VF=3V, IF = 5mA, Res = 56ohm

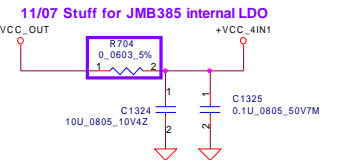
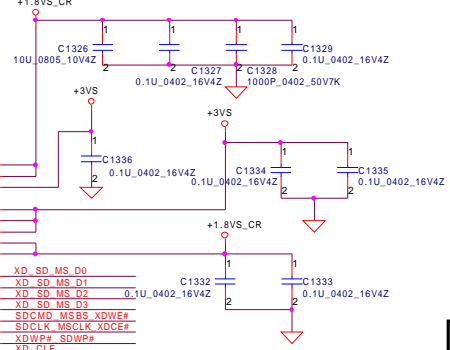
11/09 don't support DIM function



01/03 Change Cardreader LED control

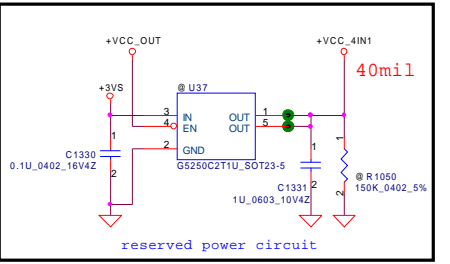


09/26 (JMicron)recommend C1328/1000pF close to U36 pin5
09/26 (JMicron)recommend place C1329/0.1uF near by C1328
09/26 (JMicron)recommend (APVDD, 20 mil width, less than 120mil long)



Use 0603 type and over 20 mils trace width on both side

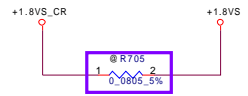
09/26 (JMicron)recommend change to 0805 size
09/26 (JMicron)recommend +VCC_OUT >30mil



11/07 Change U37 correct PCBFootprint SOT23

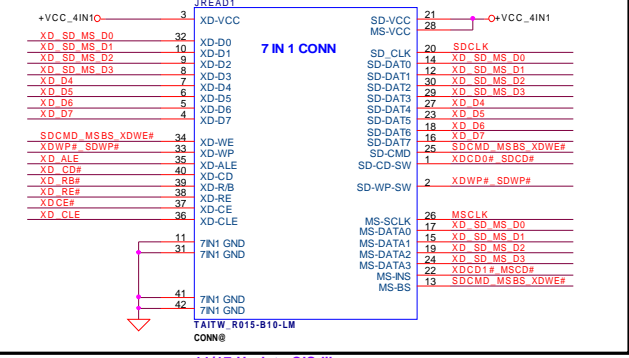
11/07 BOM delete for JMB385 internal LDO

09/26 Must change P mos FET



11/07 Don't stuff for JMB385 internal LDO

Card Reader Connector

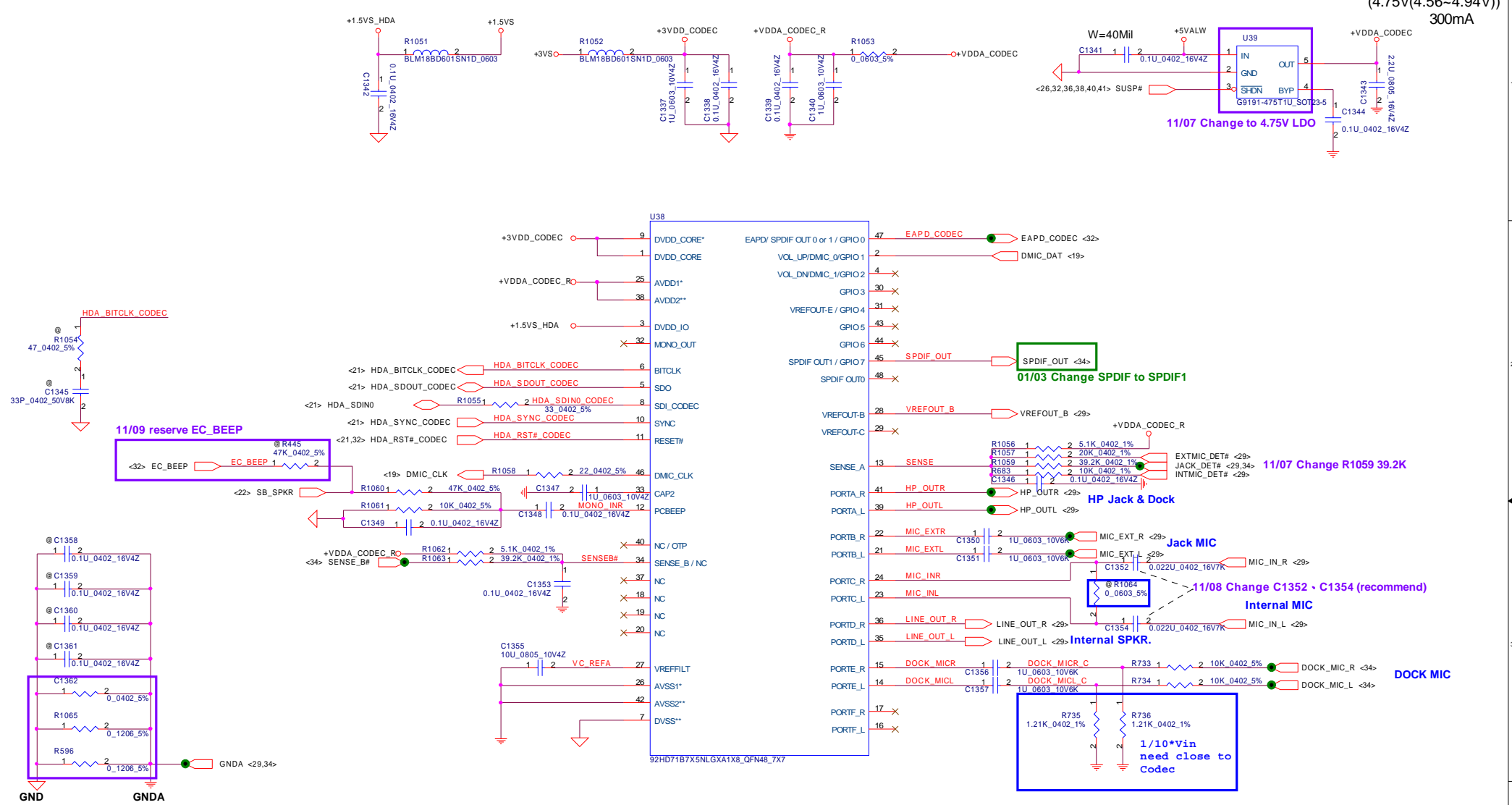


11/17 Update CIS library

Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2007/08/28	Deciphered Date	2006/10/06	USB CardReader&CONN	
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CODEC POWER

(4.75V(4.56~4.94V))
300mA

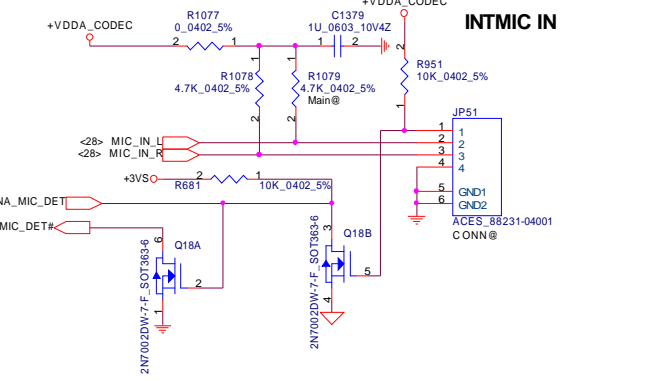
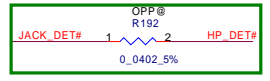
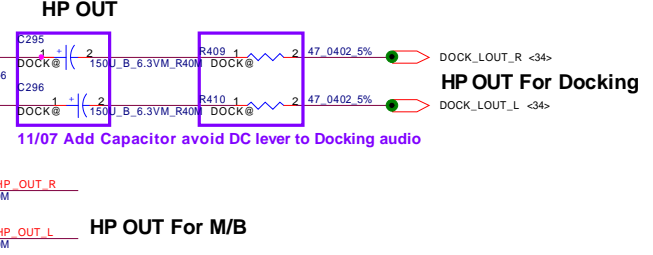
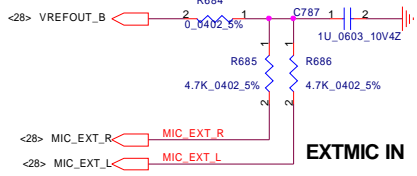
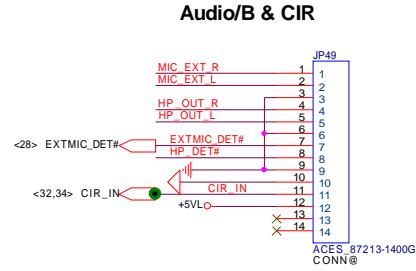
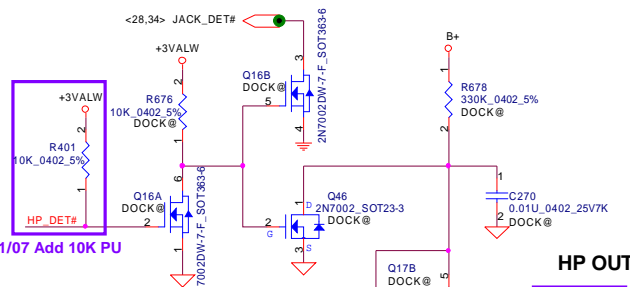
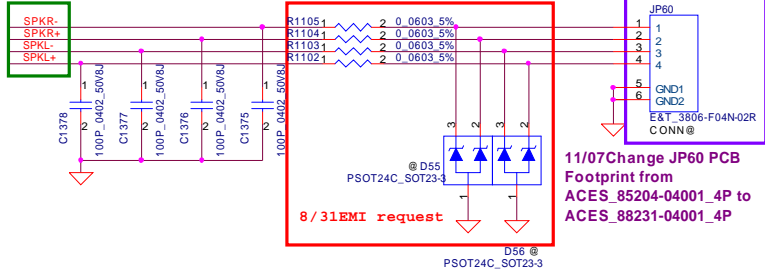
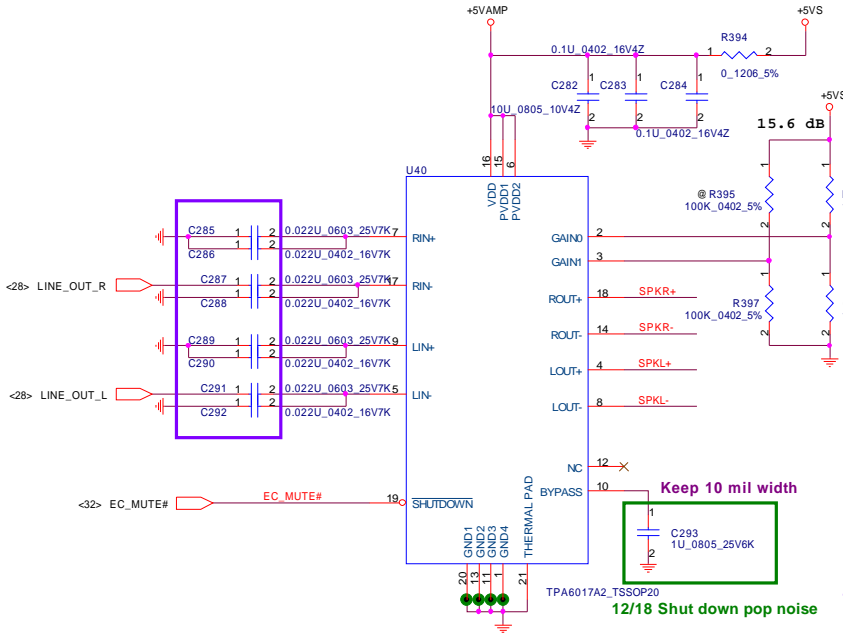


11/07 Stuff 0 Ohm for AGND and GND

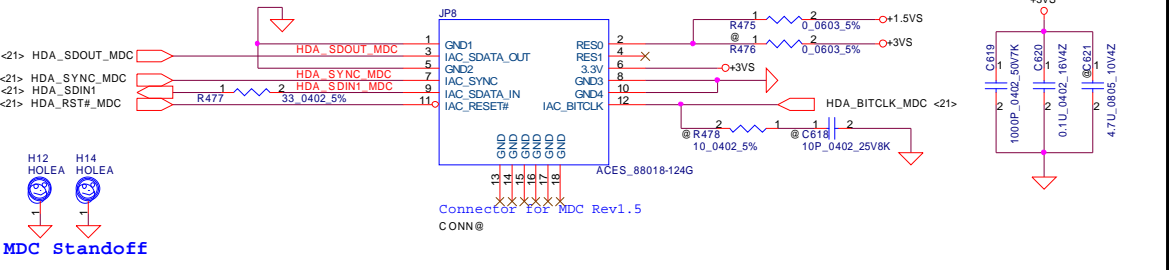
SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

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Issued Date	2007/08/28	Deciphered Date	2006/07/26	Size	Document Number	Rev	
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				Date:	Saturday, January 05, 2008	Sheet	28 of 46

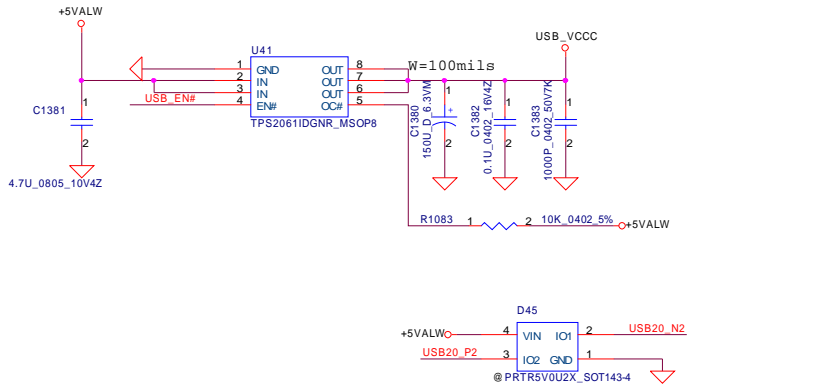
GAIN0	GAIN1	Av (inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB



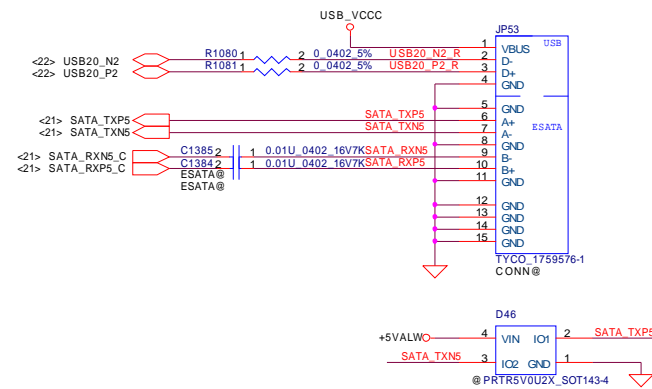
MDC 1.5 Conn.



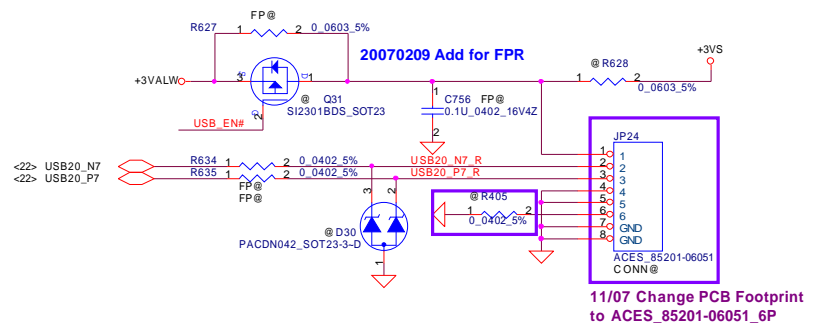
Left side USB Connector



Left side ESATA/USB combination Connector

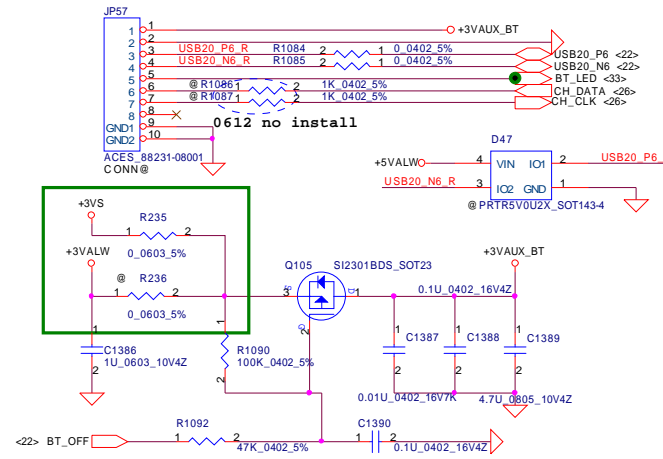


Finger printer

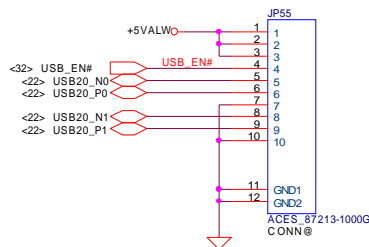


BT Connector

Need change to New version

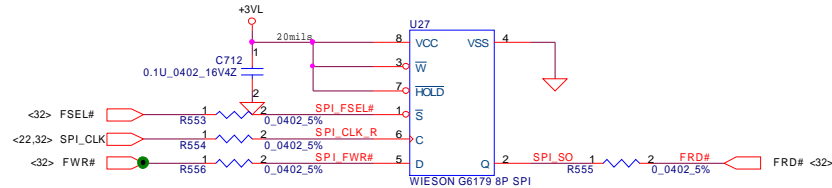


USB cable connector for Right side

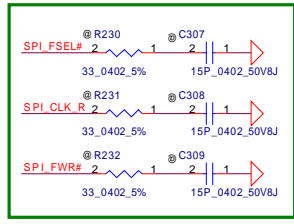


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				Montevina Blade UMA LA4101P	
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SPI ROM

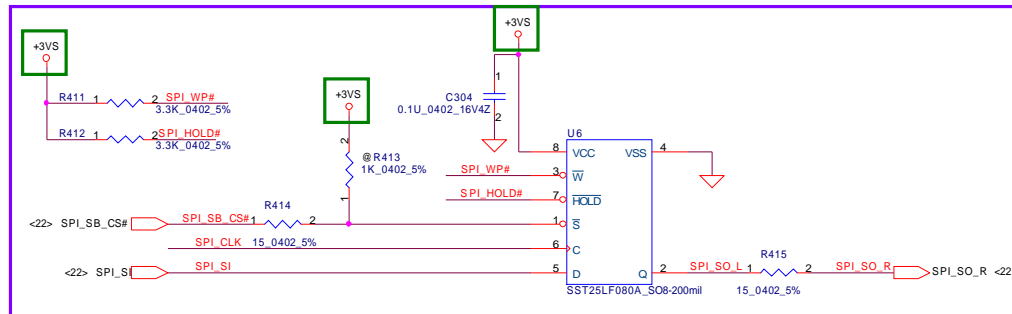
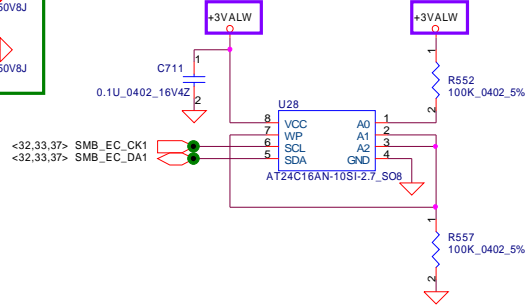


SP07000F500 S SOCKET WIESON G6179-100000 8P SPIFLASH
WIESO_G6179-100000_8P



12/27EMI request

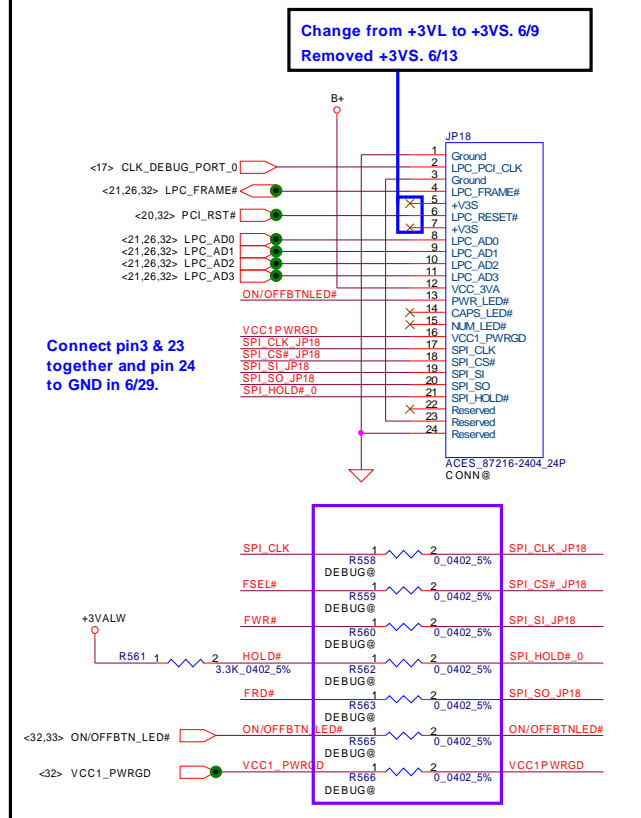
11/16 Change TO +3VALW



11/17 Add SB HDCP ROM

01/03 Change HDCP ROM to +3VS

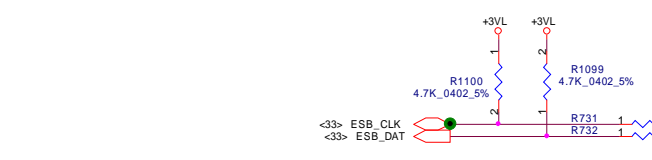
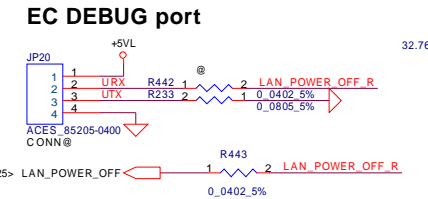
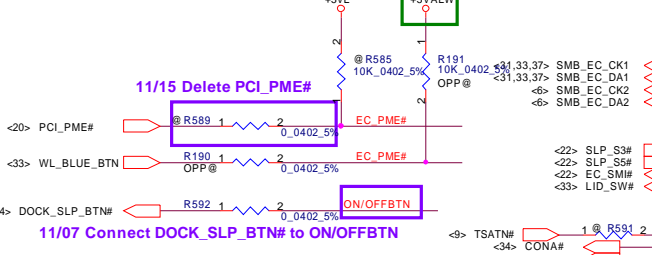
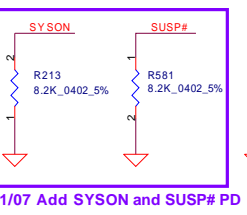
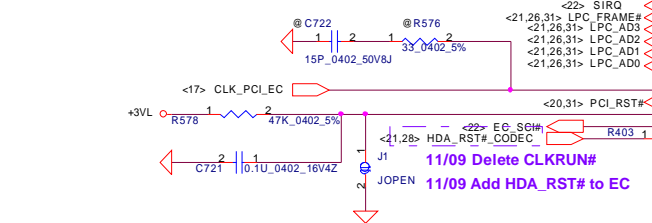
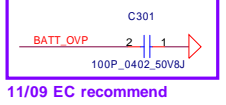
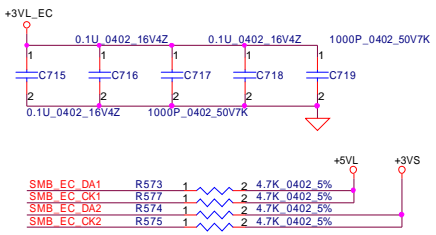
LPC Debug Port



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		2006/07/26

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Title		
Compal Electronics, Inc.		
BIOS ROM		
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- <21> GATEA20
- <21> KB_RST#
- <22> SIRQ
- <21,26,31> LPC_FRAME#
- <21,26,31> LPC_AD3
- <21,26,31> LPC_AD2
- <21,26,31> LPC_AD1
- <21,26,31> LPC_ADD0

- PCICLK
- PCIRST#
- PCIRST#
- PCIRST#
- PCIRST#
- PCIRST#
- PCIRST#
- PCIRST#
- PCIRST#
- PCIRST#

- KS10
- KS11
- KS12
- KS13
- KS14
- KS15
- KS16
- KS17
- KS18
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- KS66
- KS67
- KS68
- KS69
- KS70

- SMB_EC CK1
- SMB_EC DA1
- SMB_EC CK2
- SMB_EC DA2

- SLP_S3#
- SLP_S4#
- SLP_S5#
- EC_SMI#
- LID_SW#
- SSB_CLK R
- SSB_DAT R
- EC PME#
- TSATN#
- CONA#
- WLAN_POWER_OFF
- UTX
- LAN_POWER_OFF R
- ON/OFFBTN
- DIM_LED
- NUM_LED#

- XCLK1
- XCLK0

- ESB_CLK R
- ESB_DAT R

- GA20/GPIO0
- KB_RST#/GPIO1
- SERIRQ#/GPIO2
- UFRAME#/GPIO3
- LAD3
- LAD2
- LAD1
- LAD0

- PCICLK
- PCIRST#/GPIO5
- ECRST#
- CHI/GPIOQE
- CLKRUN#/GPIOID

- KS10/GPIO30
- KS11/GPIO31
- KS12/GPIO32
- KS13/GPIO33
- KS14/GPIO34
- KS15/GPIO35
- KS16/GPIO36
- KS17/GPIO37
- KS18/GPIO38
- KS19/GPIO39
- KS20/GPIO40
- KS21/GPIO41
- KS22/GPIO42
- KS23/GPIO43
- KS24/GPIO44
- KS25/GPIO45
- KS26/GPIO46
- KS27/GPIO47
- KS28/GPIO48
- KS29/GPIO49
- KS30/GPIO50
- KS31/GPIO51
- KS32/GPIO52
- KS33/GPIO53
- KS34/GPIO54
- KS35/GPIO55
- KS36/GPIO56
- KS37/GPIO57
- KS38/GPIO58
- KS39/GPIO59
- KS40/GPIO60
- KS41/GPIO61
- KS42/GPIO62
- KS43/GPIO63
- KS44/GPIO64
- KS45/GPIO65
- KS46/GPIO66
- KS47/GPIO67
- KS48/GPIO68
- KS49/GPIO69
- KS50/GPIO70

- SCL1/GPIO44
- SDA1/GPIO45
- SCL2/GPIO46
- SDA2/GPIO47

- PM_SLP_S3#/GPIO04
- PM_SLP_S4#/GPIO07
- EC_SMI#/GPIO08
- LID_SW#/GPIO10A
- SUSP#/GPIO0B
- SSB_CLK R
- SSB_DAT R
- EC PME#
- TSATN#
- CONA#
- WLAN_POWER_OFF
- UTX
- LAN_POWER_OFF R
- ON/OFFBTN
- DIM_LED
- NUM_LED#

- XCLK1
- XCLK0

- ESB_CLK R
- ESB_DAT R

- INVT_PWM/PWM1/GPIOF
- BEEP#/PWM2/GPIO10
- SERIRQ#/FANPWM1/GPIO12
- ACOFF#/FANPWM2/GPIO13

- BATT_TEMP/AD0/GPIO38
- BATT_OVP/AD1/GPIO39
- ADP_I#/GPIO3
- ADP_ID#/GPIO3B
- AD4/GPIO42
- SELIOZ#/AD5/GPIO43

- PSCLK1/GPIO4A
- PSDAT1/GPIO4B
- PSCLK2/GPIO4C
- PSDAT2/GPIO4D
- TP_CLK/PSCLK3/GPIO4E
- TP_DATA/PSDAT3/GPIO4F

- SDICS#/GPXA00
- SDICLK/GPXA01
- SDID0/GPXA02
- SDIDI/GPXD0

- CIR_RX/GPIO40
- CIR_RLC_TX/GPIO41
- FSTCHG/STELLOW/GPIO50
- BATT_CHG_LED#/GPIO52
- CAPS_LED#/GPIO53
- BATT_LOW_LED#/GPIO54
- SUSP_LED#/GPIO55
- SYSON/GPIO56
- VR_ONXCLK3/GPIO57
- AC_IN#/GPIO59

- EC_RSMRST#/GPX003
- EC_LID_OUT#/GPX004
- EC_ON#/GPX005
- EC_SW#/GPX006
- ICH_PWROK/GPX006
- BKOFF#/GPX008
- WL_OFF#/GPX009
- WL_ON#/GPX010
- GPX011

- PM_SLP_S4#/GPIXD1
- ENBK1/GPIXD2
- GPXD3
- GPXD4
- GPXD5
- GPXD6
- GPXD7

- ENBK1
- EAPD_CODEC
- THERM_SCI#
- SUSP#
- PWRBTN_OUT#
- NMI_DBS#

- INV_PWM
- FAN_PWM
- EC_BEEP
- ACOFF

- BATT_TEMP
- BATT_OVP
- ADP_I
- ADP_ID
- TP_BTN
- ANA_MIC_DET

- DAC_BRIG
- VCTRL
- IREF
- AC_SET

- EC_MUTE#
- USB_EN#
- I2C_INT
- MUTE_LED

- FRD#
- FWR#
- SPI_CLK
- FSEL#

- CIR_IN
- VCC1_PWRGD
- FSTCHG
- STD_ADP
- CAPS_LED#
- BAT_LED#
- ON/OFFBTN_LED#
- SYSON
- VR_ON
- AC_IN

- EC_RSMRST#
- EC_LID_OUT#
- EC_ON#
- WL_BLUE_LED#
- PM_PWROK
- BKOFF#
- TP_LED#

- ENBK1
- EAPD_CODEC
- THERM_SCI#
- SUSP#
- PWRBTN_OUT#
- NMI_DBS#

- INV_PWM
- FAN_PWM
- EC_BEEP
- ACOFF

- BATT_TEMP
- BATT_OVP
- ADP_I
- ADP_ID
- TP_BTN
- ANA_MIC_DET

- DAC_BRIG
- VCTRL
- IREF
- AC_SET

- EC_MUTE#
- USB_EN#
- I2C_INT
- MUTE_LED

- FRD#
- FWR#
- SPI_CLK
- FSEL#

- CIR_IN
- VCC1_PWRGD
- FSTCHG
- STD_ADP
- CAPS_LED#
- BAT_LED#
- ON/OFFBTN_LED#
- SYSON
- VR_ON
- AC_IN

- EC_RSMRST#
- EC_LID_OUT#
- EC_ON#
- WL_BLUE_LED#
- PM_PWROK
- BKOFF#
- TP_LED#

- ENBK1
- EAPD_CODEC
- THERM_SCI#
- SUSP#
- PWRBTN_OUT#
- NMI_DBS#

- KS015 @ C792 1 2 100P_0402_50V8J
- KS010 @ C793 1 2 100P_0402_50V8J
- KS011 @ C794 1 2 100P_0402_50V8J
- KS014 @ C795 1 2 100P_0402_50V8J
- KS013 @ C796 1 2 100P_0402_50V8J
- KS012 @ C797 1 2 100P_0402_50V8J
- KS03 @ C798 1 2 100P_0402_50V8J
- KS06 @ C799 1 2 100P_0402_50V8J
- KS08 @ C800 1 2 100P_0402_50V8J
- KS07 @ C801 1 2 100P_0402_50V8J
- KS04 @ C802 1 2 100P_0402_50V8J
- KS02 @ C803 1 2 100P_0402_50V8J
- KS10 @ C804 1 2 100P_0402_50V8J
- KS01 @ C805 1 2 100P_0402_50V8J
- KS05 @ C806 1 2 100P_0402_50V8J
- KS13 @ C807 1 2 100P_0402_50V8J
- KS12 @ C808 1 2 100P_0402_50V8J
- KS00 @ C809 1 2 100P_0402_50V8J
- KS15 @ C810 1 2 100P_0402_50V8J
- KS14 @ C811 1 2 100P_0402_50V8J
- KS09 @ C812 1 2 100P_0402_50V8J
- KS16 @ C813 1 2 100P_0402_50V8J
- KS17 @ C814 1 2 100P_0402_50V8J
- KS11 @ C815 1 2 100P_0402_50V8J

- R407 10K_0402_5% +3V_S
- R408 10K_0402_5%

- R407 10K_0402_5%
- R408 10K_0402_5%

- R407 10K_0402_5%
- R408 10K_0402_5%

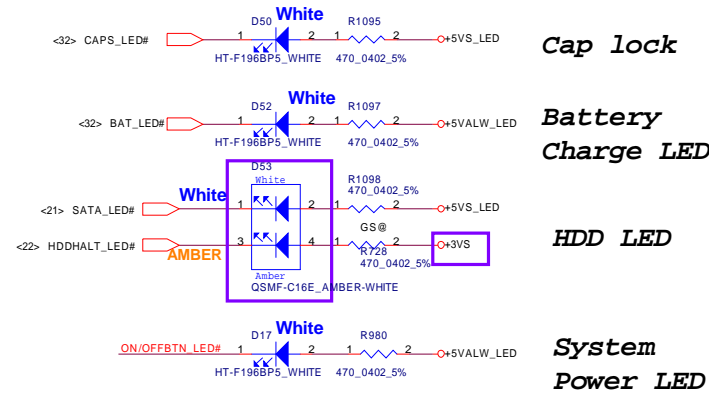
- R407 10K_0402_5%
- R408 10K_0402_5%

- R407 10K_0402_5%
- R408 10K_0402_5%

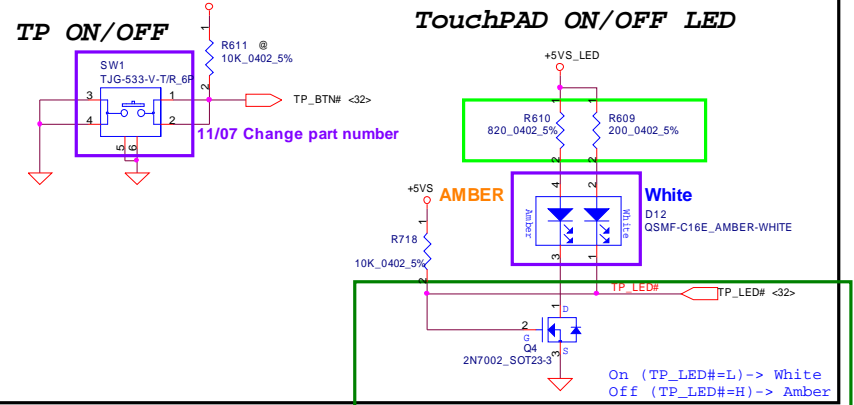
- R407 10K_0402_5%
- R408 10K_0402_5%

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Issued Date	2007/08/28	Deciphered Date	2006/07/26	Title
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Date:	Saturday, January 05, 2008	Sheet	32	of 46

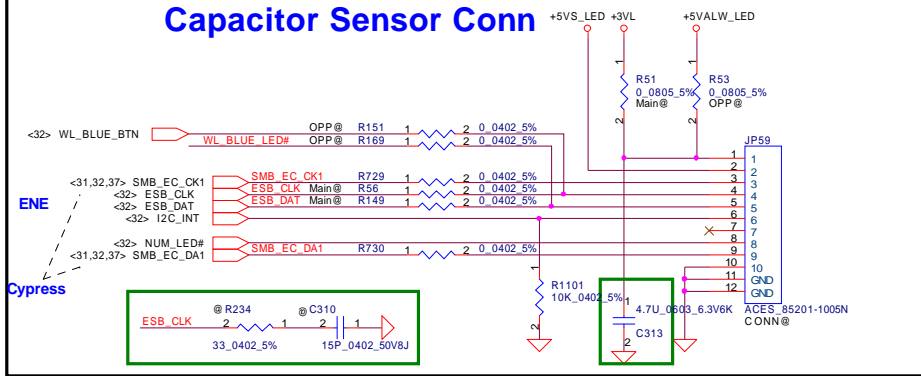
System LED



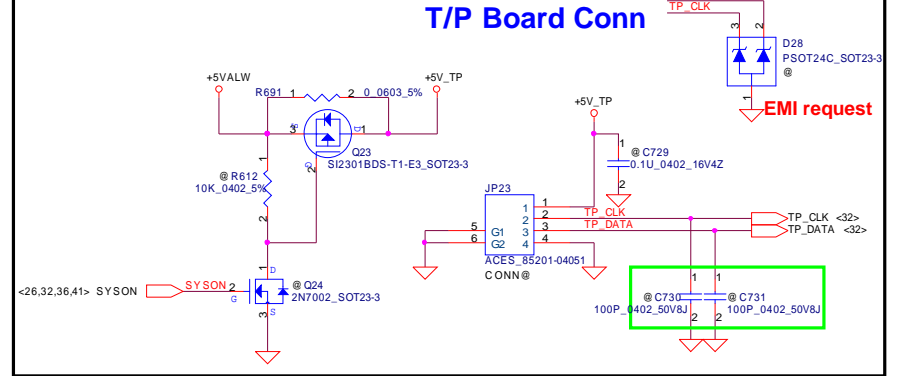
T/P Board (Include T/P_ON/OFF)



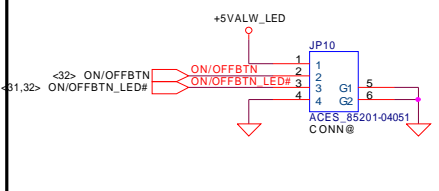
Capacitor Sensor Conn



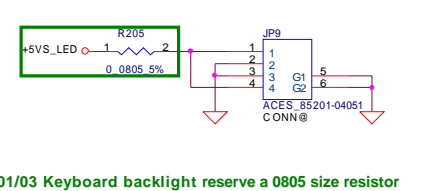
T/P Board Conn



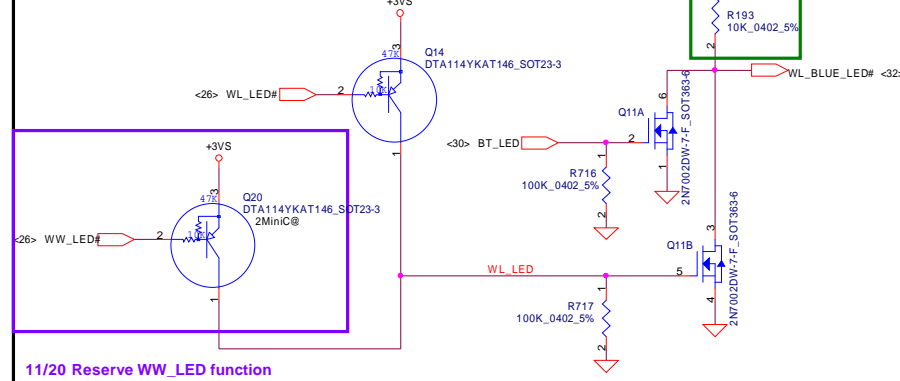
ON/OFF Button Connector



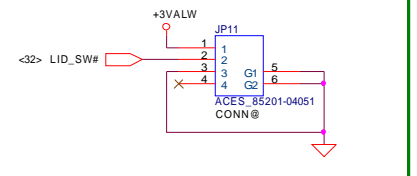
Keyboard backlight Conn



Mini card LED



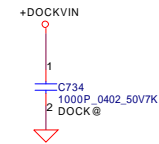
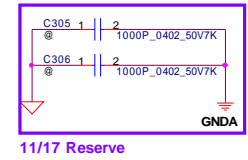
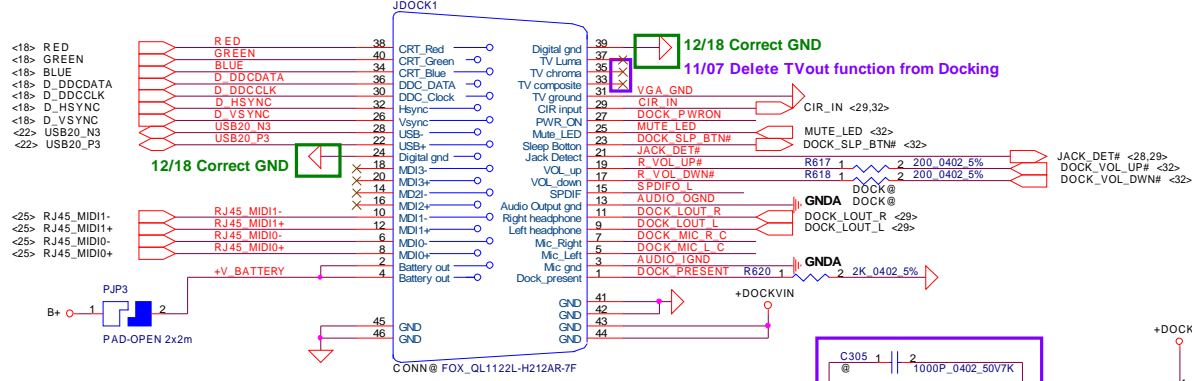
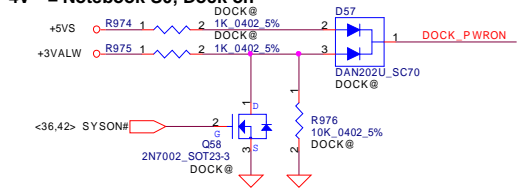
Lid Switch Connector



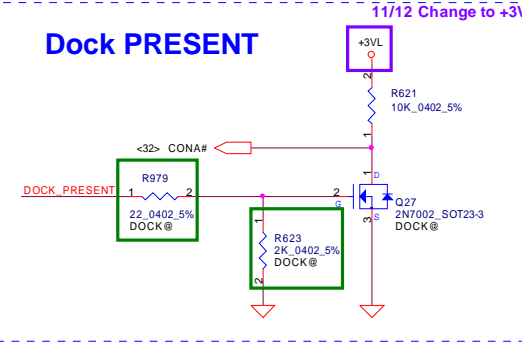
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Issued Date	2007/08/28	Deciphered Date	2006/07/26	Compal Electronics, Inc.
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				Document Number
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Atlas/ Saturn Dock

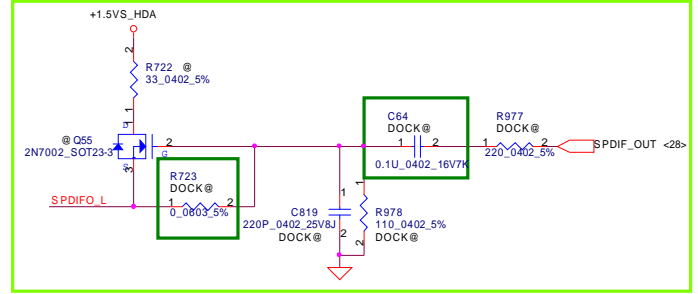
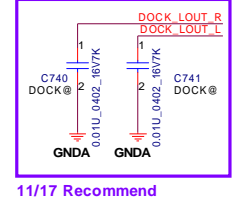
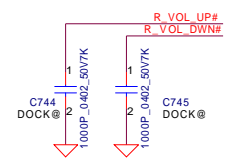
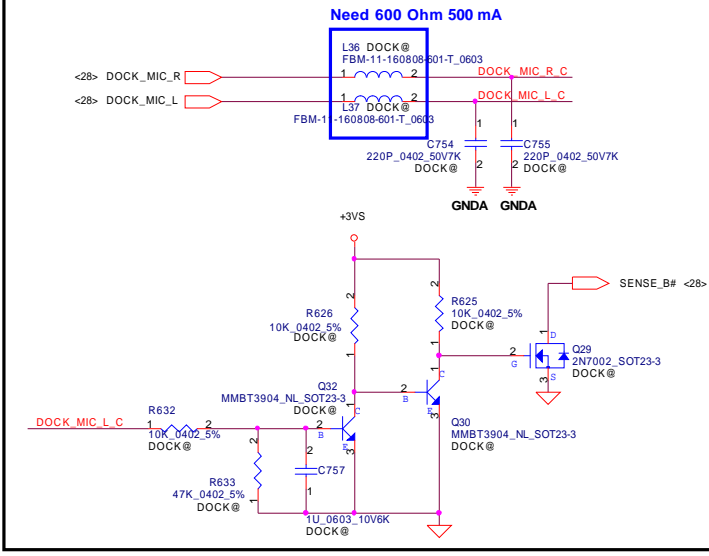
DOCK_PWR_ON Spec
0V = Notebook S4/S5, Dock off
2.5V = Notebook S3, Dock on
4V = Notebook S0, Dock on



Dock PRESENT



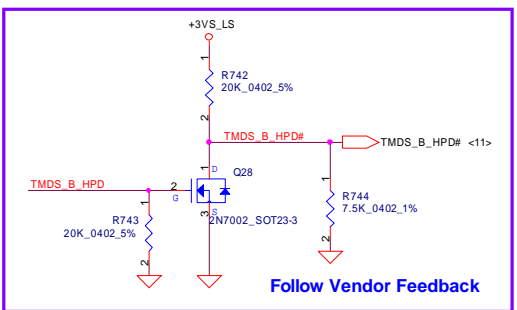
MIC_Dock



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Custor	Montevina Blade UMA LA4101P	0.3		
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Follow Intel Feedback putting 2.2K ohm

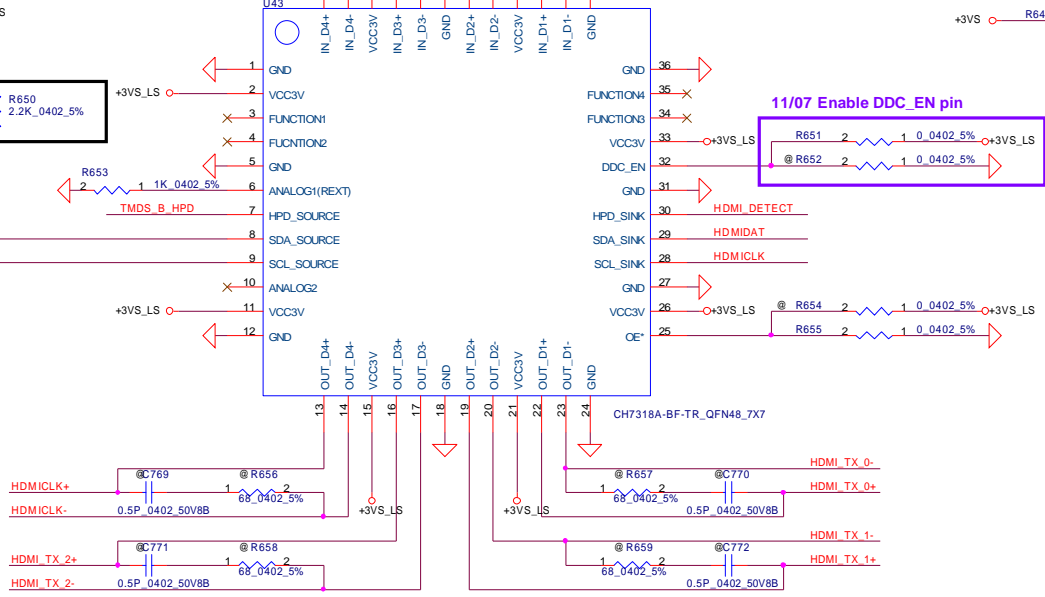
<9> HDMIDAT_NB
<9> HDMICKL_NB



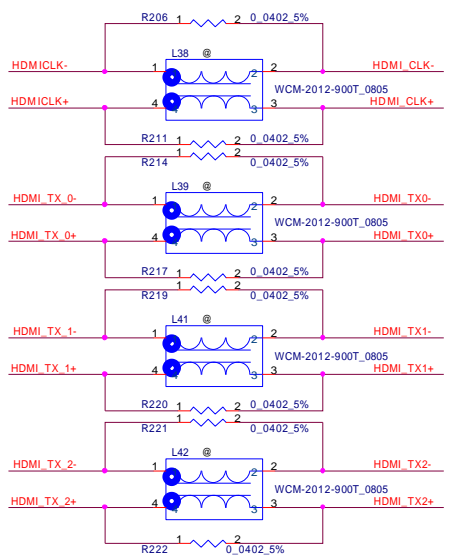
Follow Vendor Feedback

11/07 correct TMDS_B_HPD# connection to North bridge

<11> TMDS_B_DATA2#
<11> TMDS_B_DATA2
<11> TMDS_B_CLK#
<11> TMDS_B_CLK
TMDS_B_DATA1 <11>
TMDS_B_DATA1# <11>
TMDS_B_DATA0 <11>
TMDS_B_DATA0# <11>



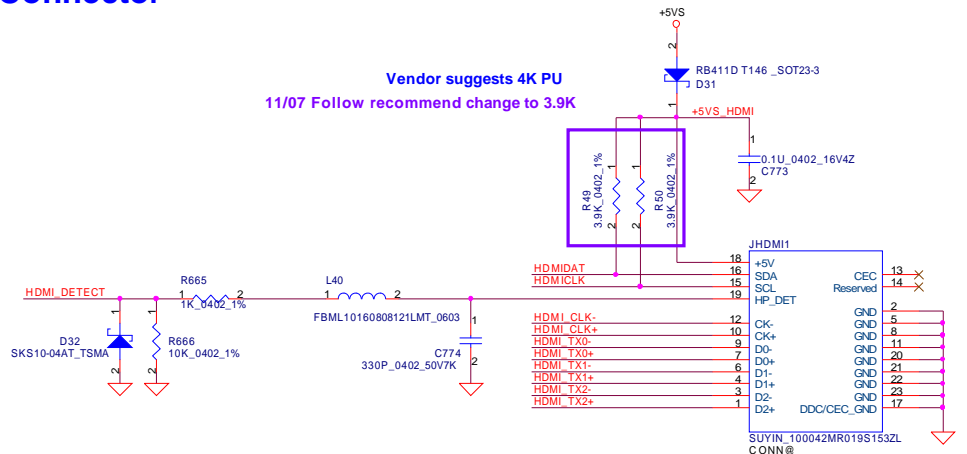
11/07 Enable DDC_EN pin



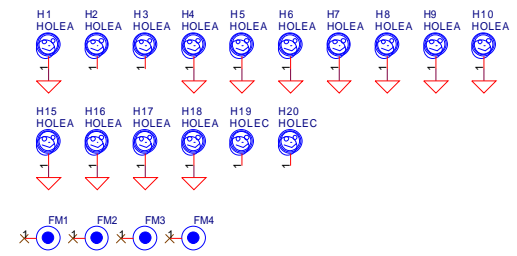
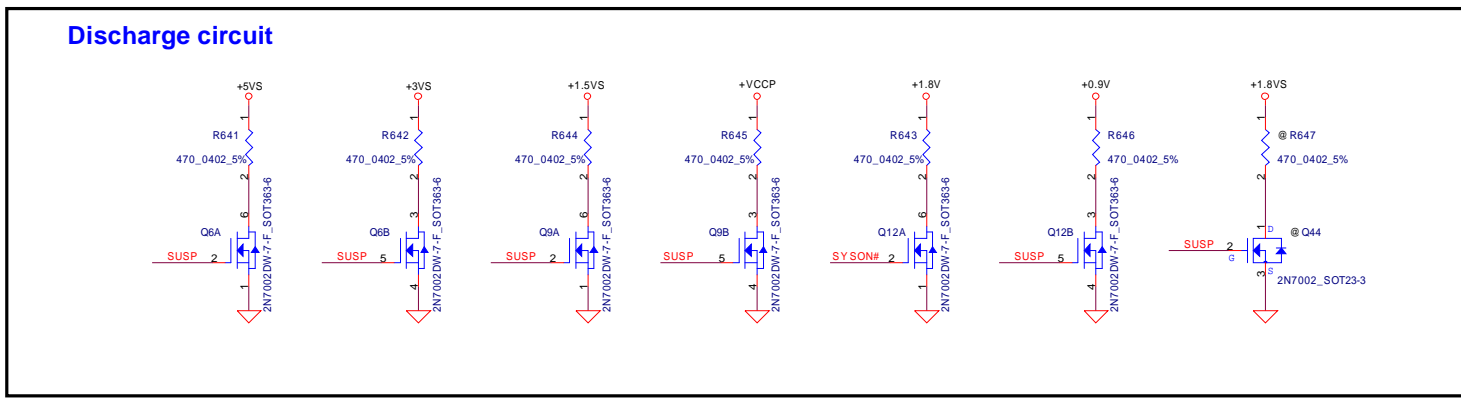
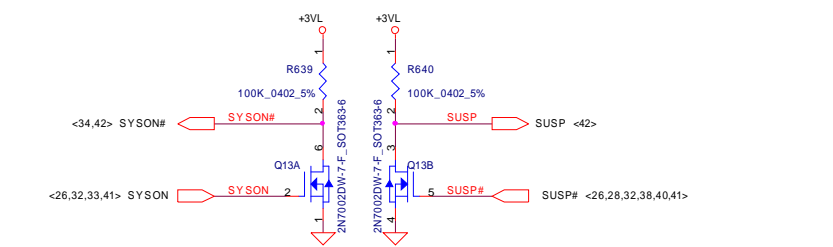
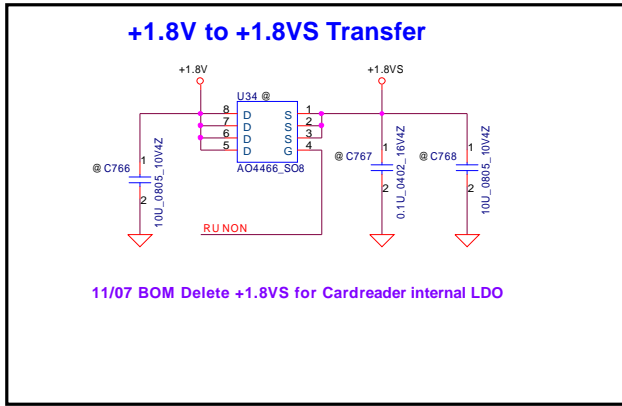
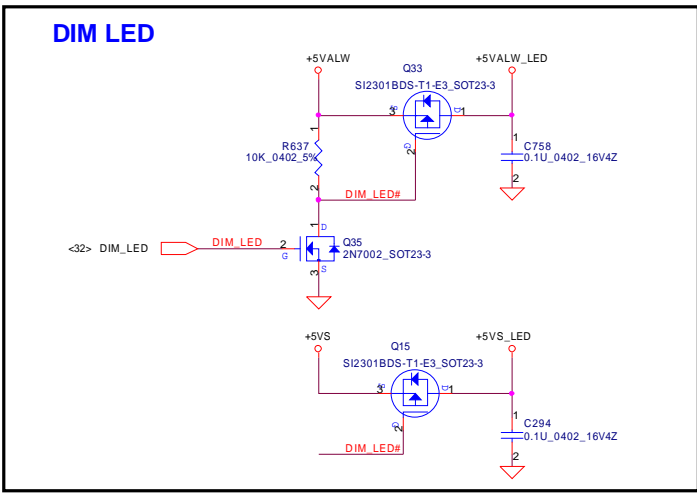
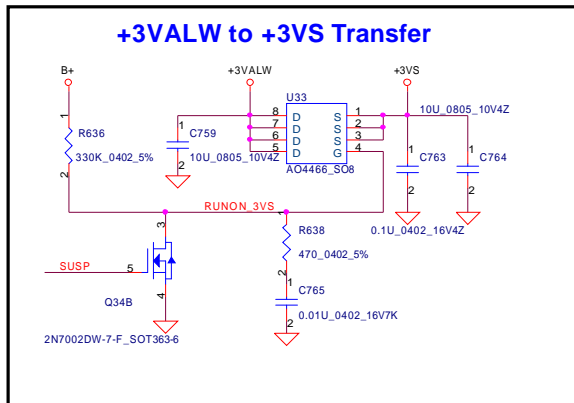
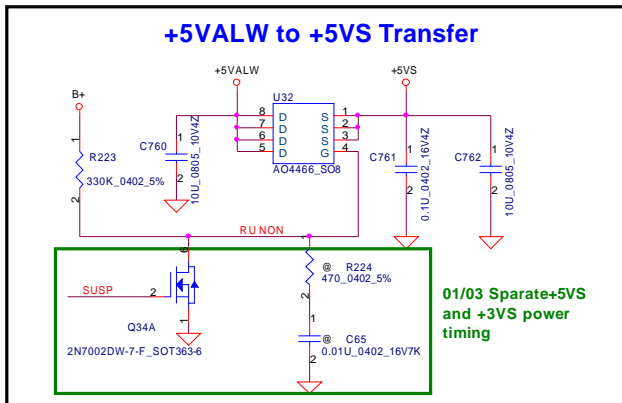
01/03 Reserver 0 ohm co lay with common choke

HDMI Connector

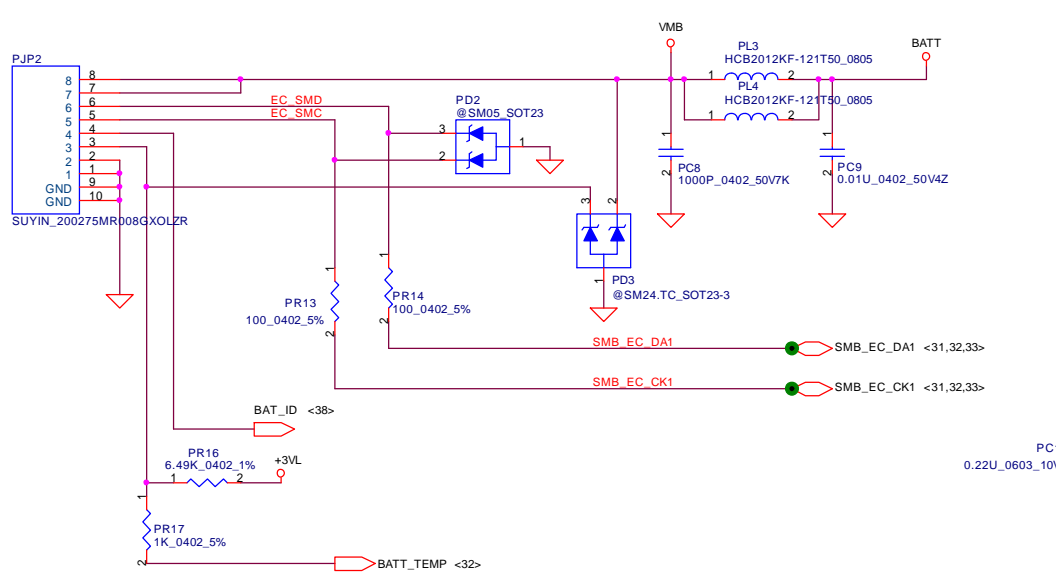
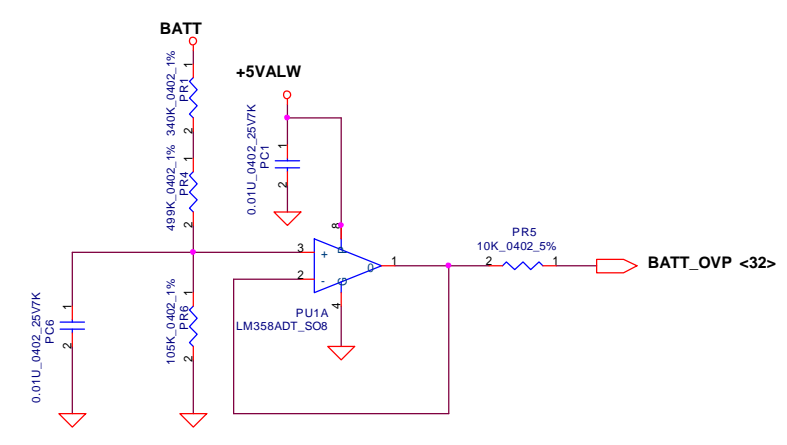
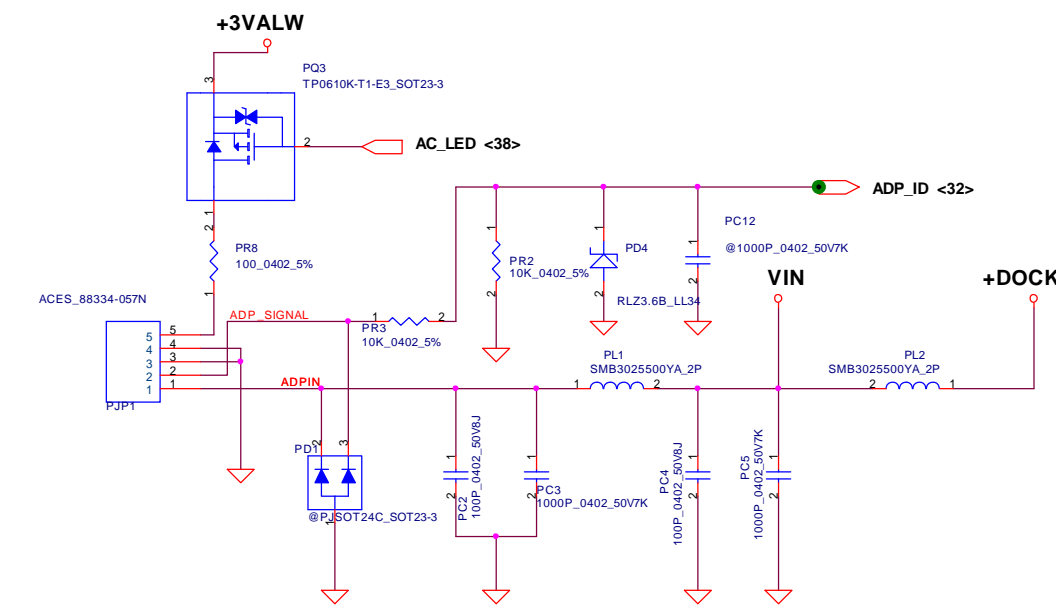
Vendor suggests 4K PU
11/07 Follow recommend change to 3.9K



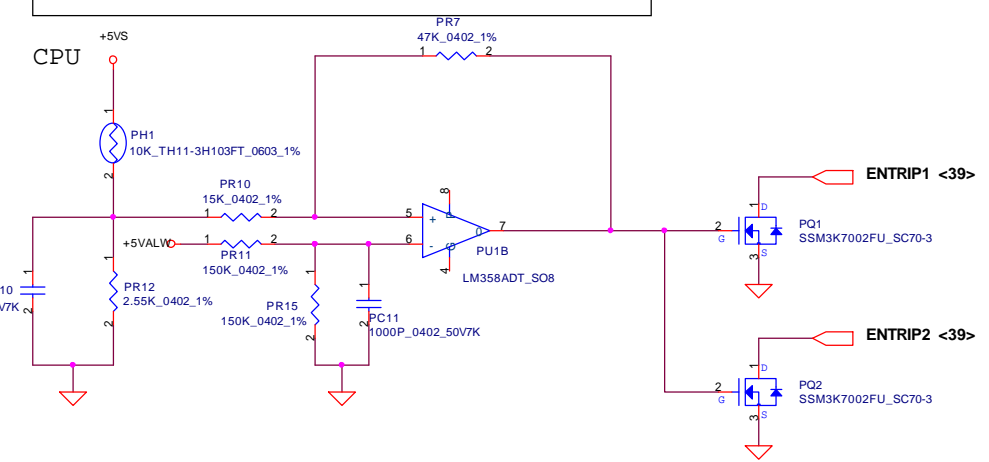
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Issued Date	2007/08/28	Deciphered Date	2006/03/10	Compal Electronics, Inc. HDMI LS & Conn.	
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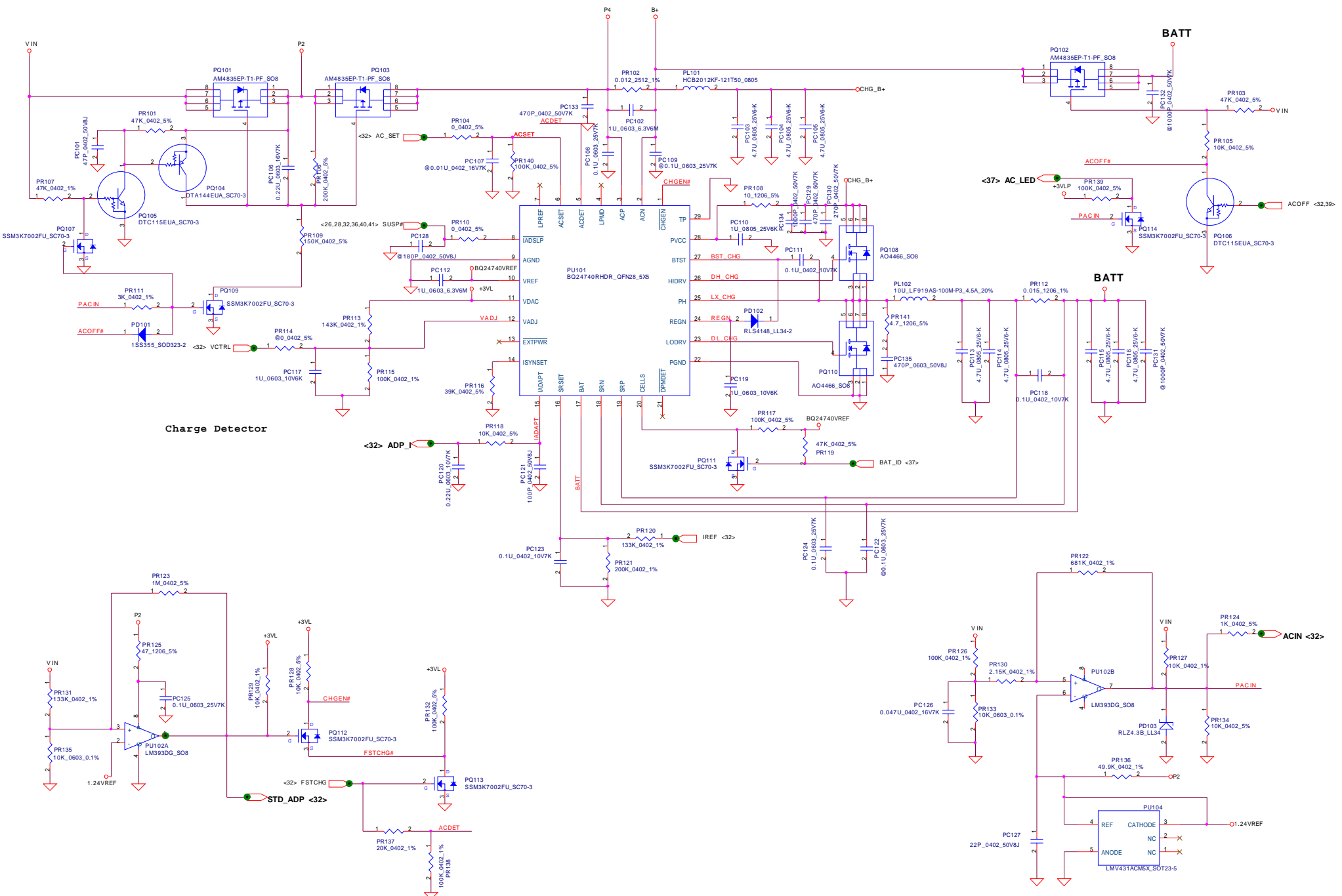
Security Classification	Compal Secret Data			Title Compal Electronics, Inc. DC/DC Interface	
Issued Date	2007/08/28	Deciphered Date	2006/07/26		
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PH1 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 47 +/-3 degree C

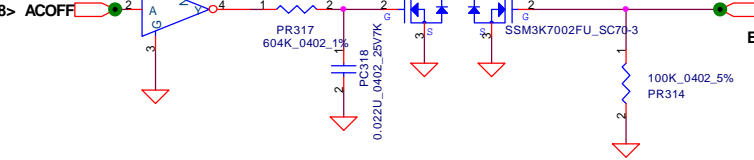
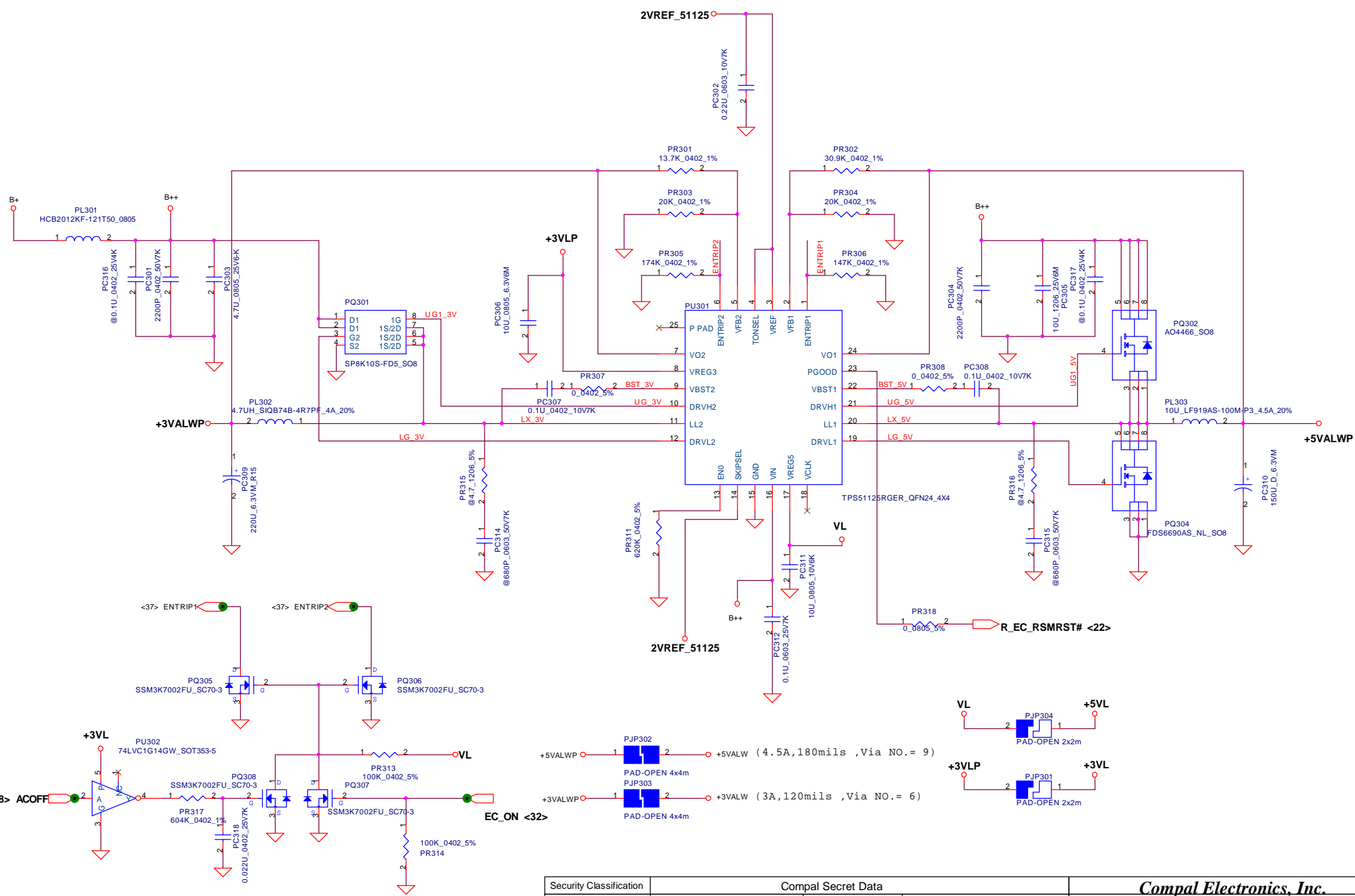


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Issued Date	2007/05/29	Deciphered Date	2008/05/29		
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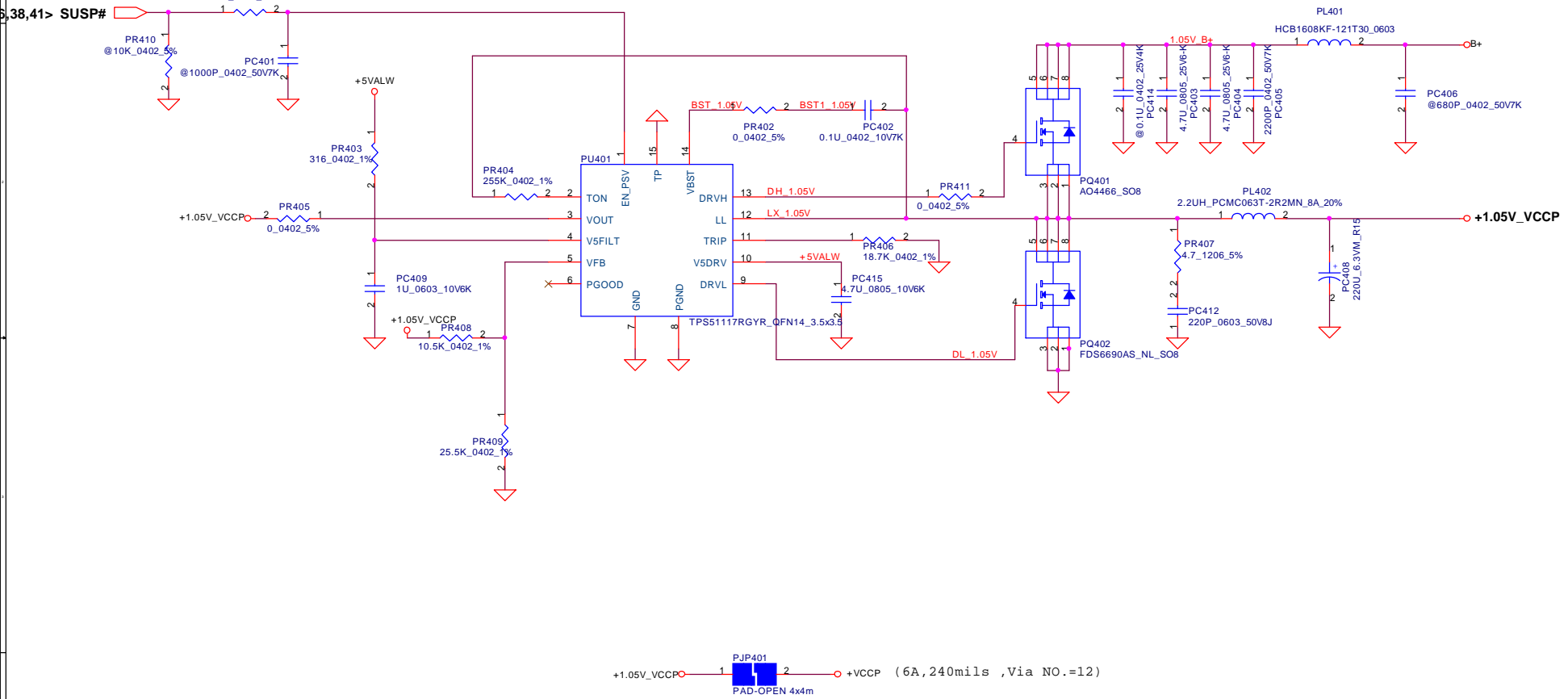
Charge Detector

Security Classification		Compal Secret Data		Title	
Issued Date	2007/05/29	Deciphered Date	2008/05/29	Charger	
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Date:	Saturday, January 05, 2008	Sheet	38	of 46	

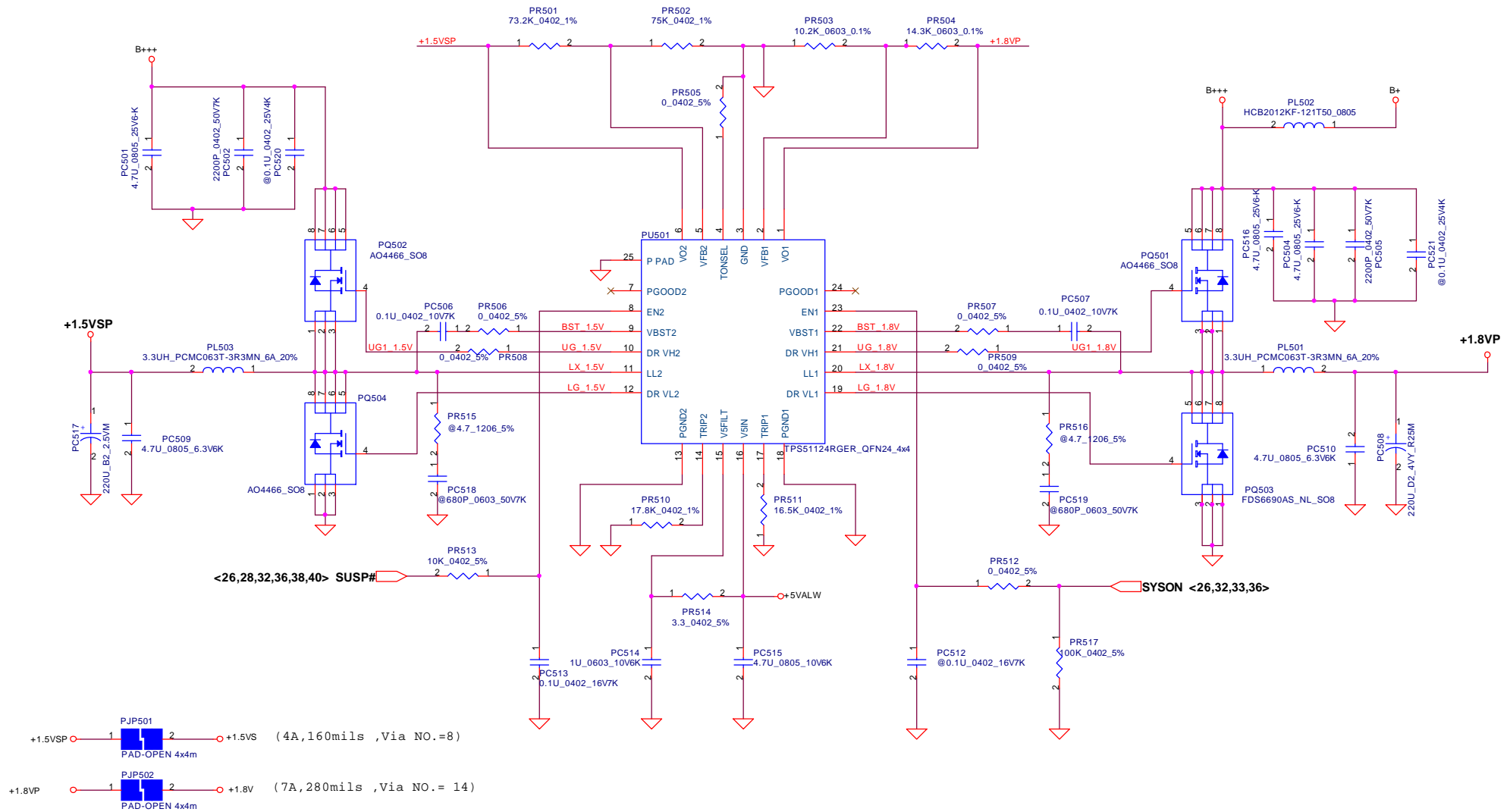


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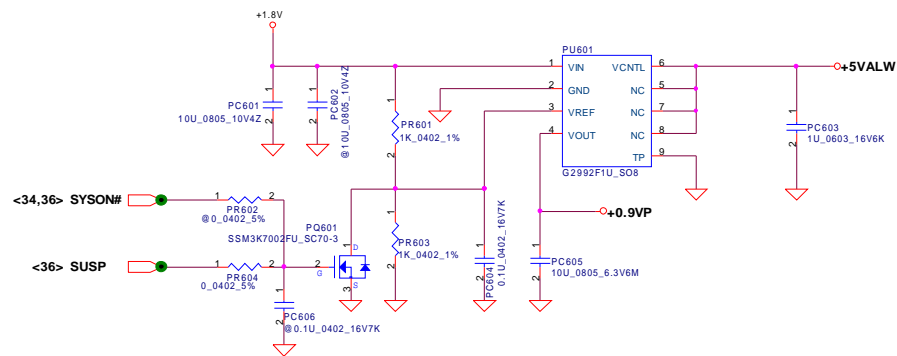
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Document Number	Montevina Blade UMA LA4101P		Rev	0.3	
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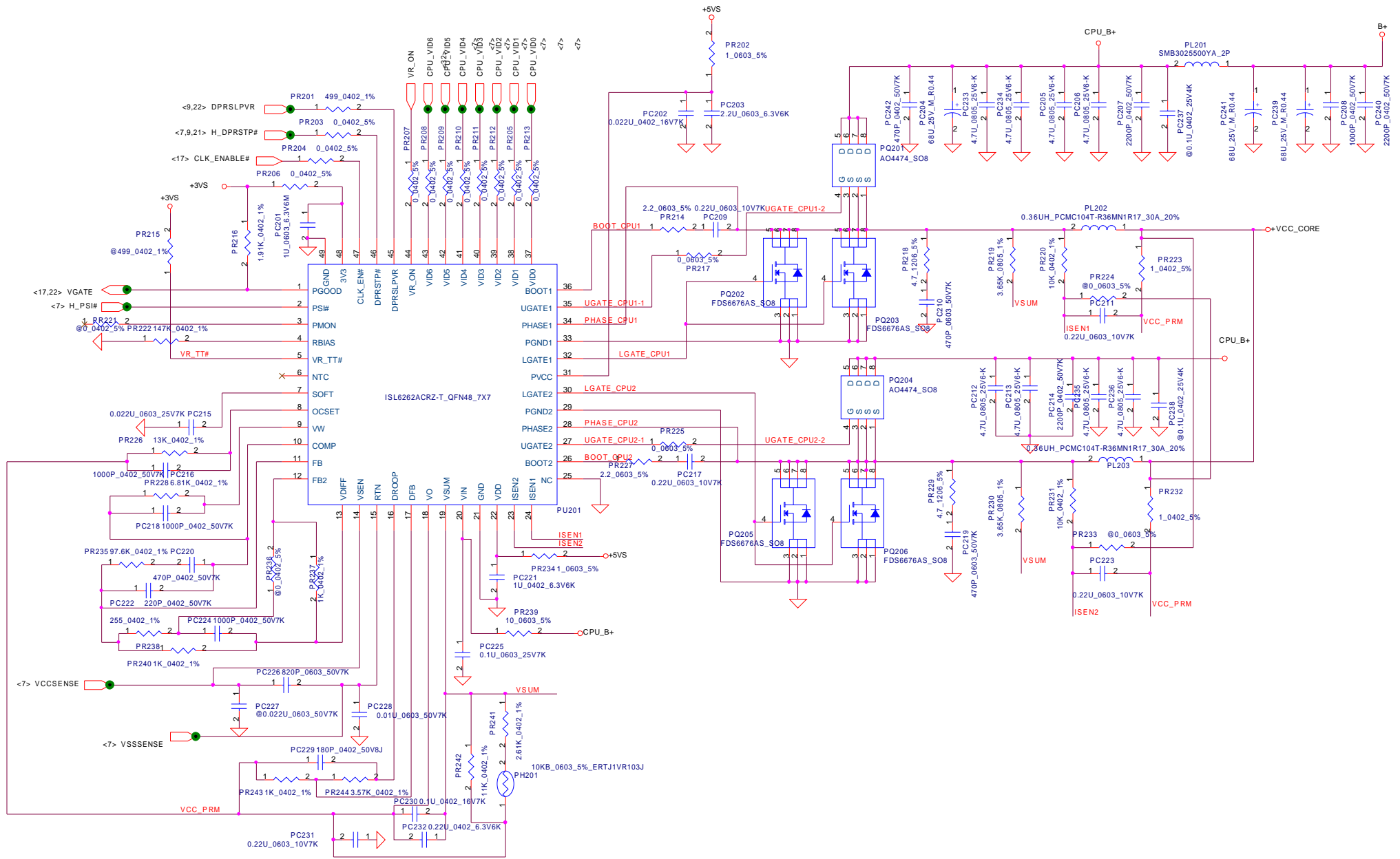
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Security Classification		Compal Secret Data		Title	
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Compal Electronics, Inc.			
Title: +CPU_CORE			
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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Transation Fail	08	C41、C42、C43、C44 Change ESR=7m ohm	11/21	SI-1
2	Disable TV out function from Docking	11、34	R61、R62、R63 change to 75 Ohm、TV_DCONSEL_0、TV_DCONSEL_1 connect to GND	11/07	SI-1
3	Update Connetor Library		CRT(JCRT1)、HDMI(JHDMI1)、ESATA(JP53)、Finger print(JJP24)、FAN(JP2)、Speaker(JP60)、Multi bay(JP12)、Dual LED(D53、D12)	11/17	SI-1
4	Delete LVDS B channel	11、19	Schematic Delete	11/17	SI-1
5	USB camera Footprint error	19	Change U42 to G916-390T1UF SOT23, it adjustable mode, R1091=215K、R1093=100K	11/07	SI-1
6	Reserve Card reader D3E function	22、27	GPIO6= CR_CPPE#、GPIO22=CR_WAKE#	11/17	SI-1
7	Swap PCIE LAN and New card	22	Swap PCIE4 and PICE6	11/17	SI-1
8	Add HDCP ROM for ICH9M	22、31	Add HDCP ROM for ICH9M	11/17	SI-1
9	Change G sensor control from SB、LED drive by +5VS	22、33	Change G sensor control from SB	11/17	SI-1
10	Avoid Battery mode can't boot issue	22、39	Add +3VALW GD to EC_RSMRST# to fix Battery mode can't boot issue	11/17	SI-1
11	Add G sensor ST and Bosch	24	Add G sensor ST and Bosch	11/17	SI-1
12	Change LAN solution (Marvell to Realtek)	25	Change LAN solution (Marvell to Realtek)	11/17	SI-1
13	LAN can't work	25	U46 Change to correct transformer type	11/17	SI-1
14	Cardreader schematic review and update, add D3E function	27	R709-->10K、R402-->8.2K、R704-->Stuff、R705-->@、U37-->@、Cardreader LED-->+5VS、add D3E function	11/17	SI-1
15	Jack can't detect normal	28	R1059 change from 39.2 to 39.2K	11/17	SI-1
16	Speaker work un normal	28	Add and Stuff C1362、R1065、R596	11/17	SI-1
17	HP audio team recommend	28、29	C285-C292、C1352、C1354 change to 0.022U、Amp output setup to 15.6 dB、Reserve C305、C306 for GNDA and GND	11/17	SI-1
18	Audio jack can't detect normal	29	Add Pull up resistor R401 to +3VALW	11/17	SI-1
19	Docking HP audio test fail	29	Add C295、BC296 to avoid DC level, and add R409、R410 to reduce HP out level	11/17	SI-1
20	Leakage problem	32	Correct direction prectect leakage	11/07	SI-1
21	EC pin define update	32	Delete EC_PME#、SYSON PU、SUSP# PU、LID_SW# change to +3VALW、Delete CLKRUN#、R582->@ for C0 chip、CIR PU+5VL、add 100P to BATT_OVP(EC recommend)	11/07	SI-1
22	Can't Hibernation(SLP_S4#)	32	Connect SLP_S4# to SB	11/17	SI-1
23	EC can't receive docking present	34	CONA# change +3VL	11/12	SI-1
24	HDMI can't detect	35	DDC_EN must enable、TMDS_B_HPD# inverse	11/07	SI-1
25	LVDS power on timing	19	C238 change to 0.047u to meet TI timing	01/03	SI-2
26	Prevent WWAN nosie	21	Add 12p on HDA_SDOOUT and HDA_SDOOUT	01/03	SI-2
27	Power leakage	21、31	Change HDCP ROM to +3VS power plane	01/03	SI-2
28	Prevent WLAN leakage	26	Add Diode prevent WLAN leakage	01/03	SI-2

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
29	New card PTH connector GND	26	New card PTH connector GND	01/03	SI-2
30	Change Cardreader LED control	27	Change Cardreader LED control	01/03	SI-2
31	Change SPDIF to SPDIF1	28	Change to SPDIF1	01/03	SI-2
32	Shut down pop noise	29	Change C293 to 1U	01/03	SI-2
33	Change BT power to +3VS	30	Change BT power to +3VS	01/03	SI-2
34	EMI Request	31	SPI_FSEL#、SPI_CLK_R、SPI_FWR# reserver RC	01/03	SI-2
35	Reserver 0 ohm co lay with common choke	35	Reserver 0 ohm co lay with common choke	01/03	SI-2
36	Sparate+5VS and +3VS power timing	36	Sparate+5VS and +3VS power timing	01/03	SI-2
37	Keyboard backlight reserve a 0805 size resistor	33	Keyboard backlight reserve a 0805 size resistor	01/03	SI-2
38	Change Lid switch connector type	33	Change Lid switch connector type	01/03	SI-2
39					
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Version Change List (P. I. R. List) for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	DC Connector /CPU_OTP	11/06	Compal	Add PD4 & PC12	Add PD4 & PC12	
2	39	3.3VALWP/5VALWP	11/06	Compal	for Layout	Change PQ301 cancel PQ303	
3	38	Charger	11/06	Compal	EMI solution	Add pc128	
4	43	+CPU_CORE	11/06	Compal	EMI solution	Add PC240	
5	39	3.3VALWP/5VALWP	11/14	Compal	for Layout	Change PL303 and PC310	
6	38	Charger	12/31	Compal	EMI solution	Add PC129, PC130, PC131, PC132, PC133	
7	43	+CPU_CORE	12/31	Compal	EMI solution	Add PC242	
8	39	3.3VALWP/5VALWP	12/31	Compal	PWR request	Add PU302, control signal changed to ACOFF	
9							
10							
11							
12							
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14							

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