

Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M core logic

2009-02-16

REV:1.0



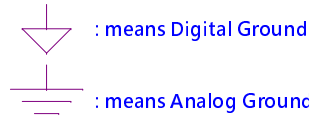
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Issued Date	2007/08/28	Deciphered Date	2006/03/10	Cover Sheet	
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Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +2.5VS +1.8V
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note:



@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
DEBUG@ :	means just reserve for debug.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
ESATA @ :	means just reserve for ESATA
GS @ :	means just reserve for G sensor
FP @ :	means just reserve for Finger Print
Multi @ :	means just reserve for Multi Bay
NewC@ :	means just reserve for New card
Main@ :	means just reserve for Main stream
OPP@ :	means just reserve for OPP
2MiniC@ :	means just reserve for 2nd Mini card slot
PA @ :	means just reserve for PA
PR @ :	means just reserve for PR

USB assignment:

USB-0	Right side(with eSATA)
USB-1	Left side
USB-2	Left side
USB-3	Cardreader
USB-4	Camera
USB-5	WLAN
USB-6	Bluetooth
USB-7	Finger Printer
USB-8	MiniCard(WWAN/TV)
USB-9	Express card
USB-10	X
USB-11	X

PCIe assignment:

PCIe-1	WWAN
PCIe-2	X
PCIe-3	WLAN
PCIe-4	GLAN (Realtek)
PCIe-5	X
PCIe-6	New Card

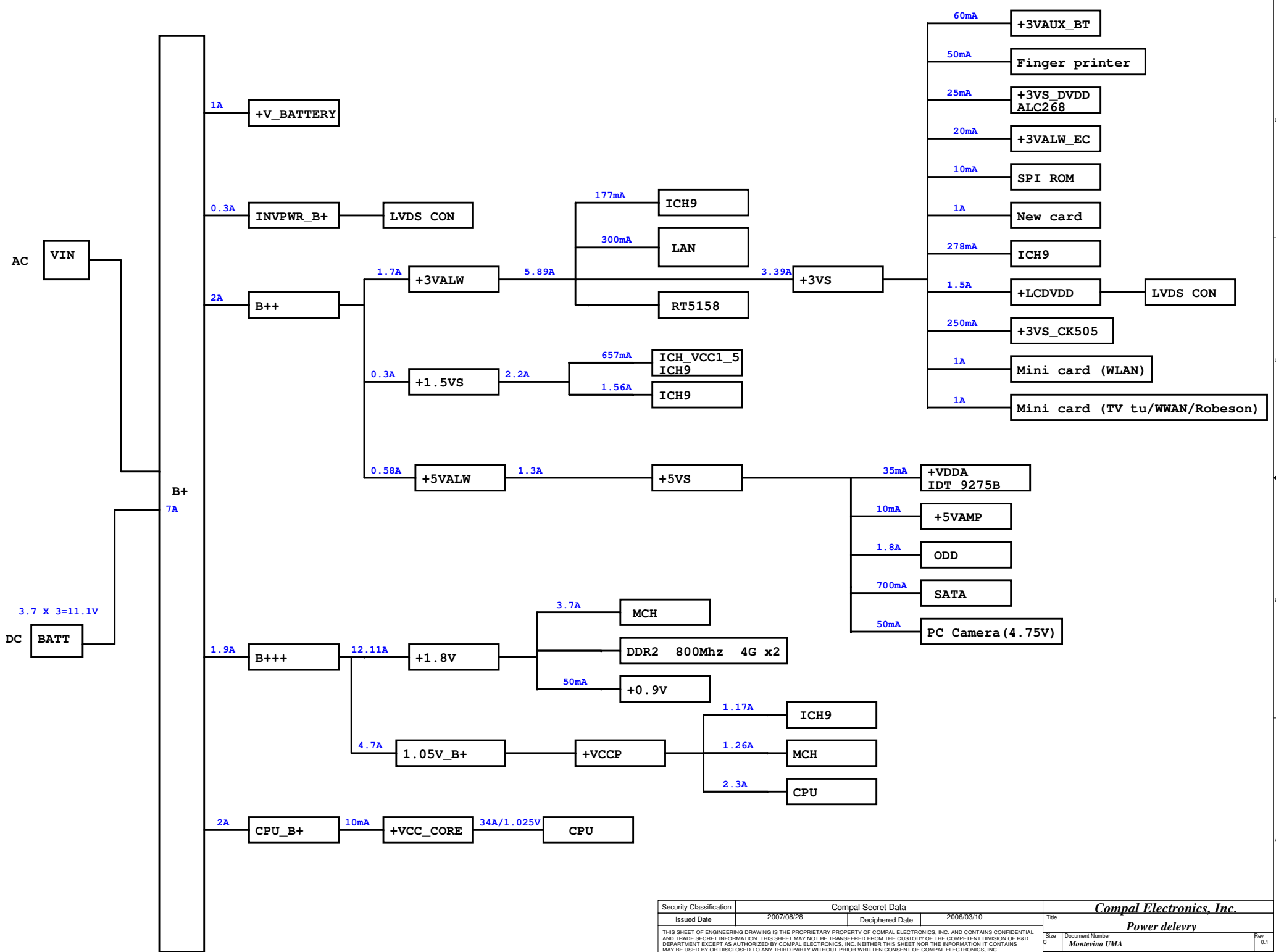
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10 10 0 0 0
DDR SO-DIMM 1	A4	10 10 0 1 0
CLOCK GENERATOR (EXT.)	D2	11 0 1 0 1 0

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X	V	V
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V	X	X	X

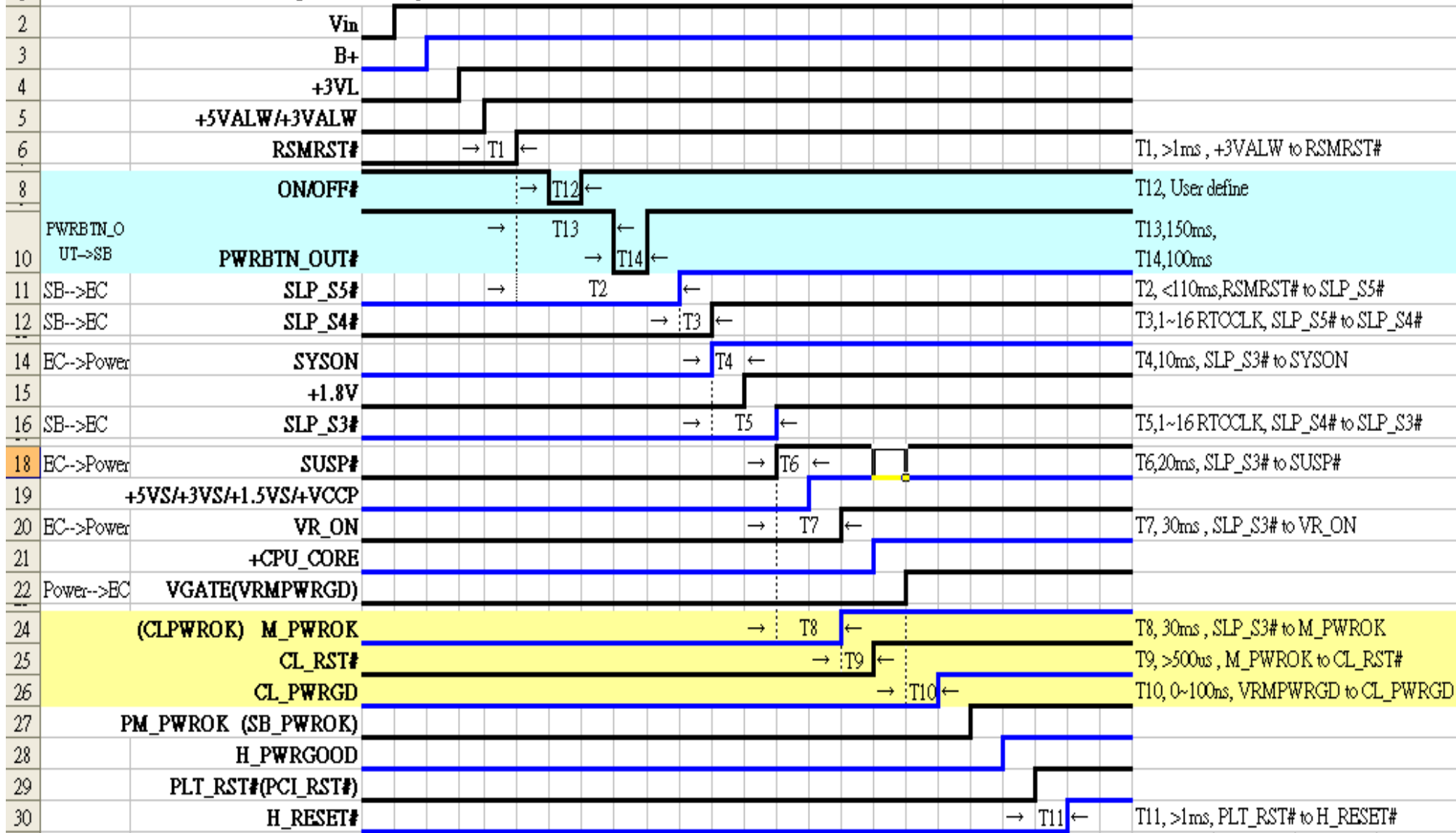
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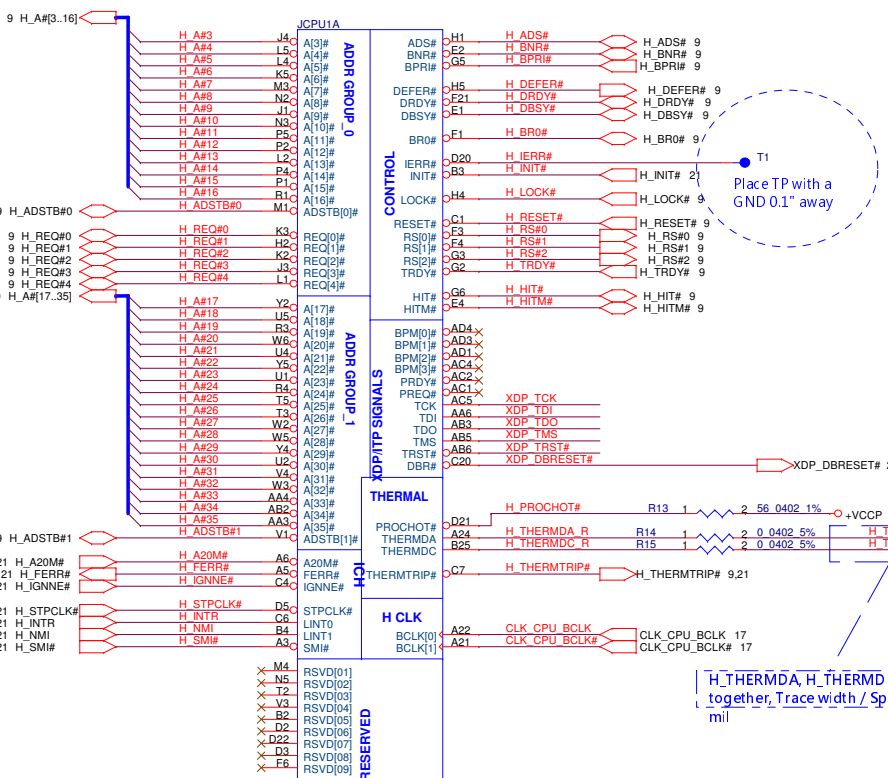


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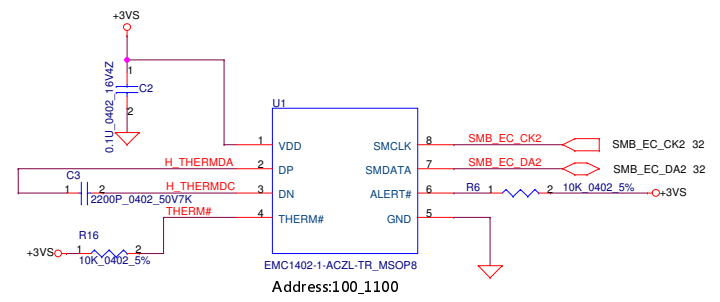
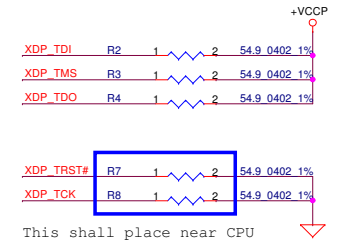
JAL50 power sequence AC mode

96.09.03.

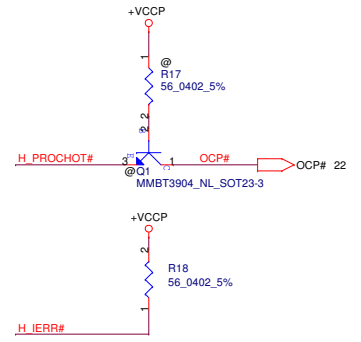
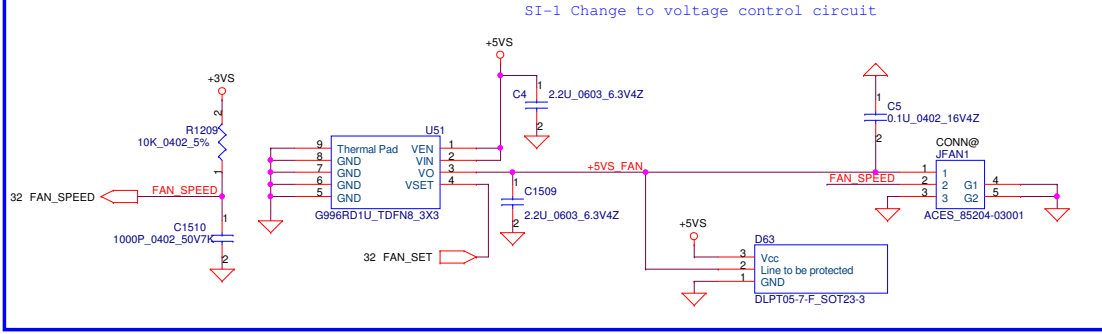




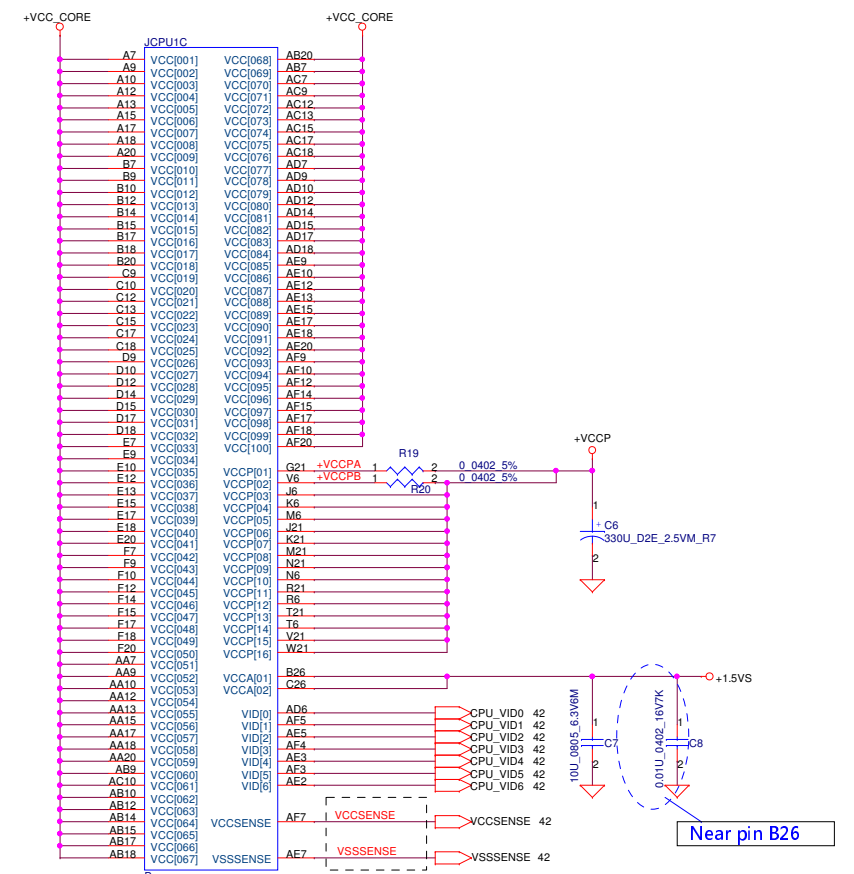
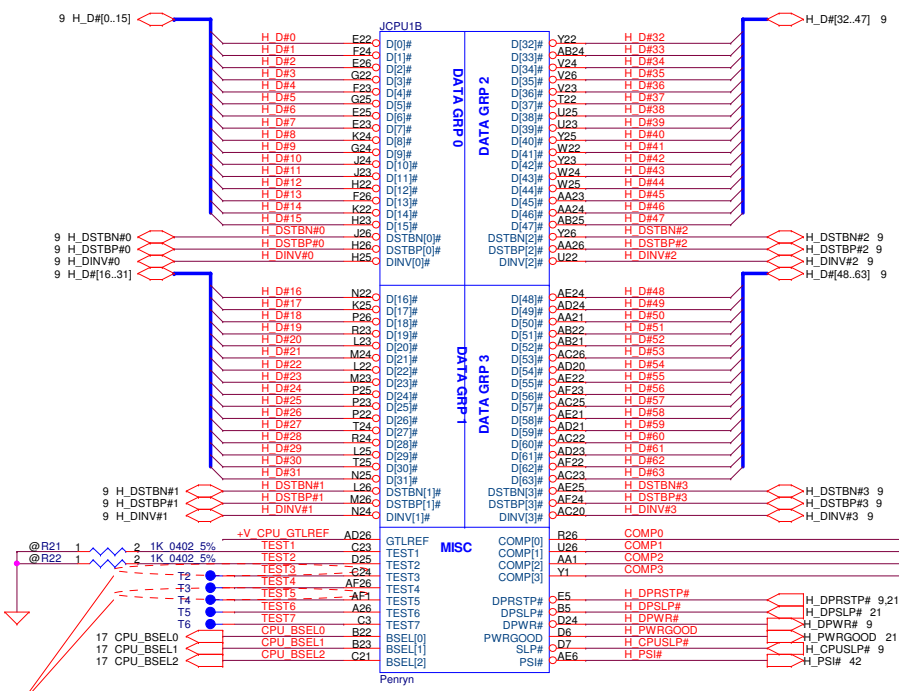
ITP-XDP Connector



Fan Control circuit



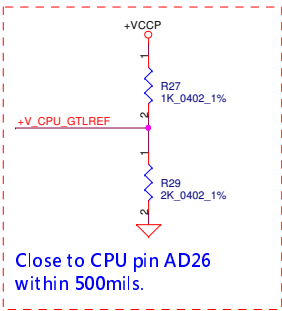
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
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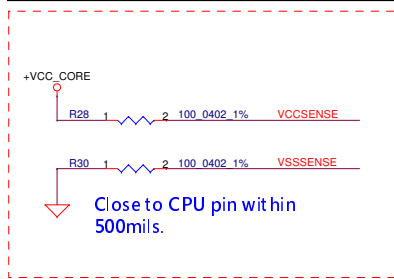
* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

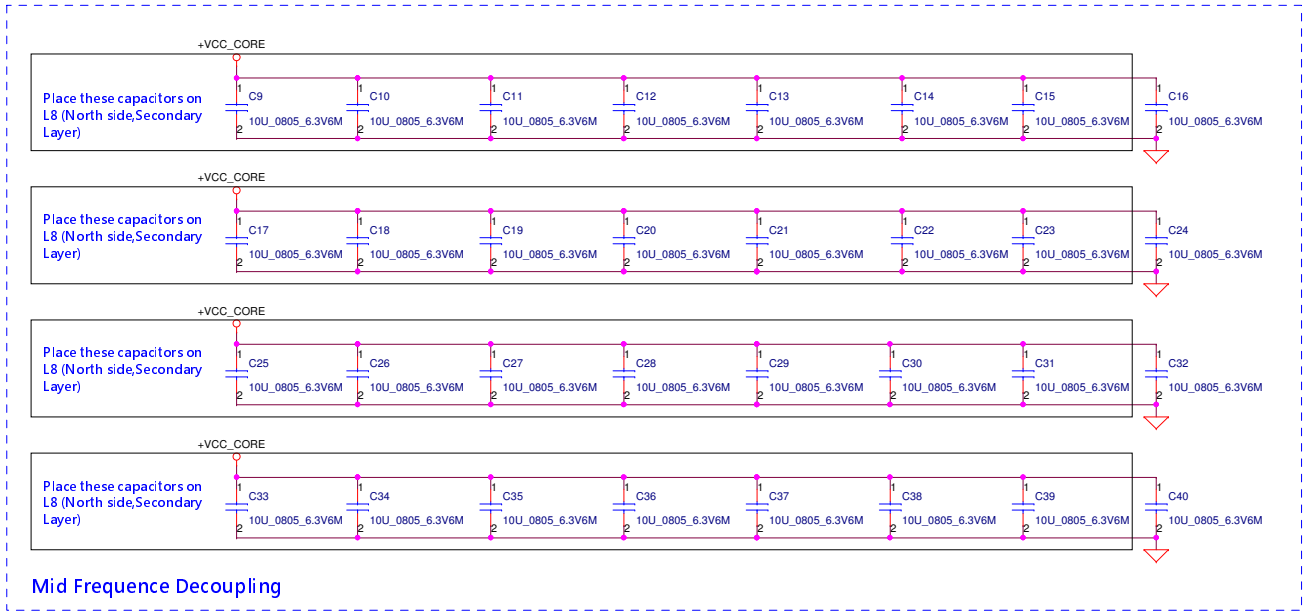
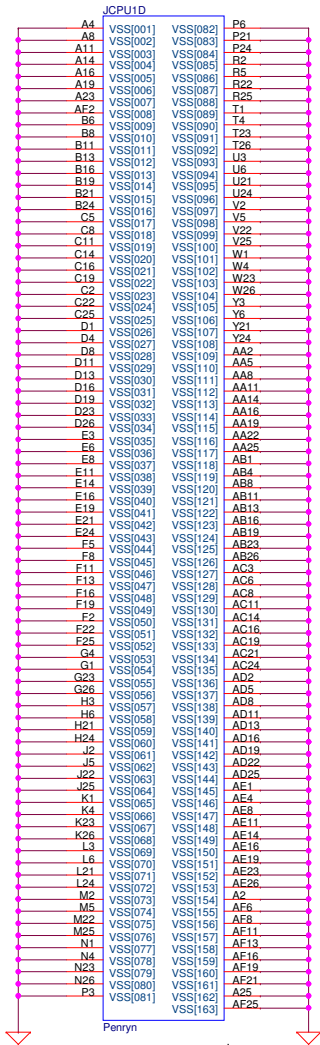
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



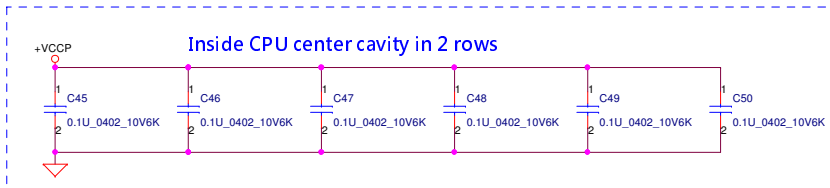
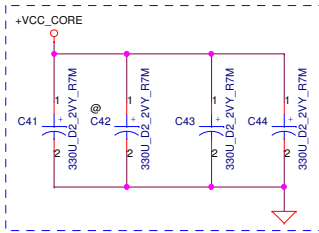
Length match within 25 mils. The trace width/space/other is 20/7/25.



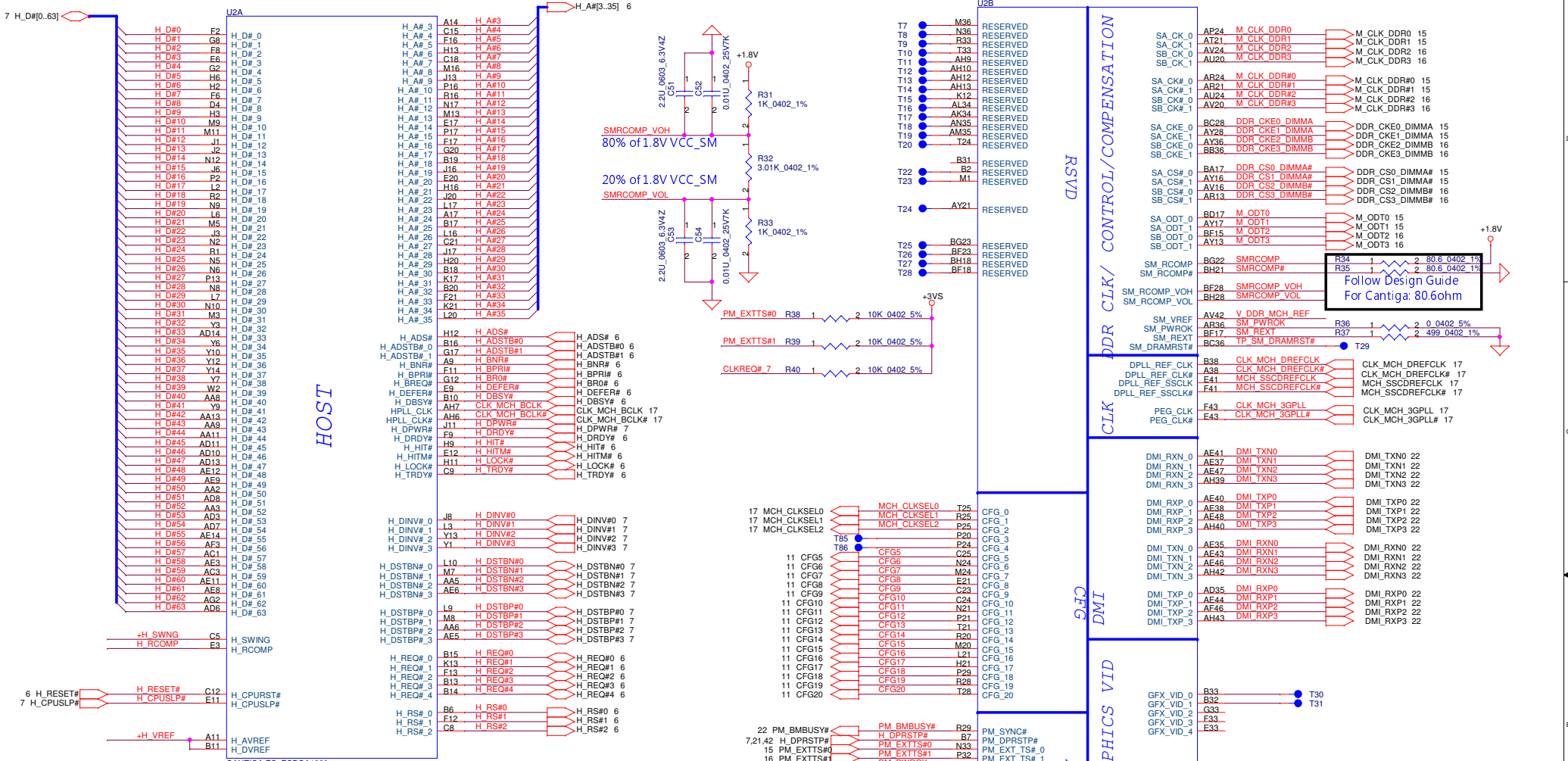


Mid Frequency Decoupling

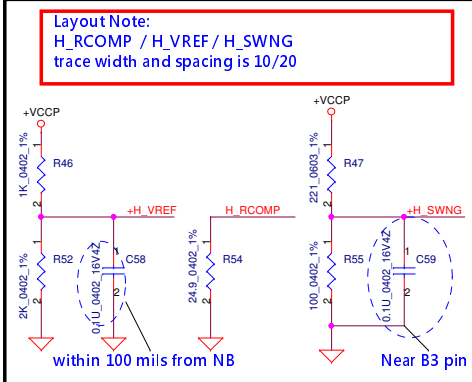
Near CPU CORE regulator
 ESR <= 1.5m ohm
 Capacitor > 1980uF



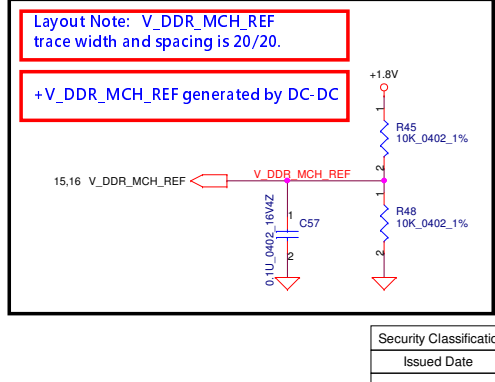
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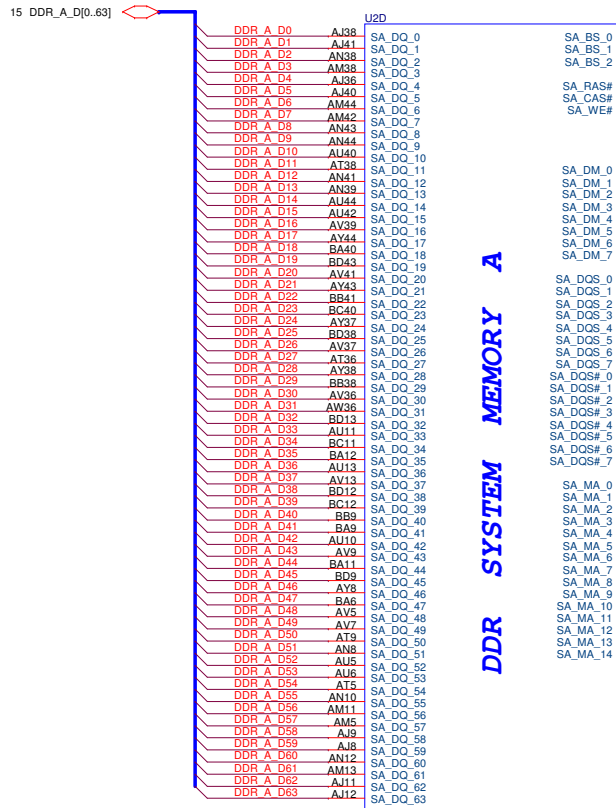
Layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces



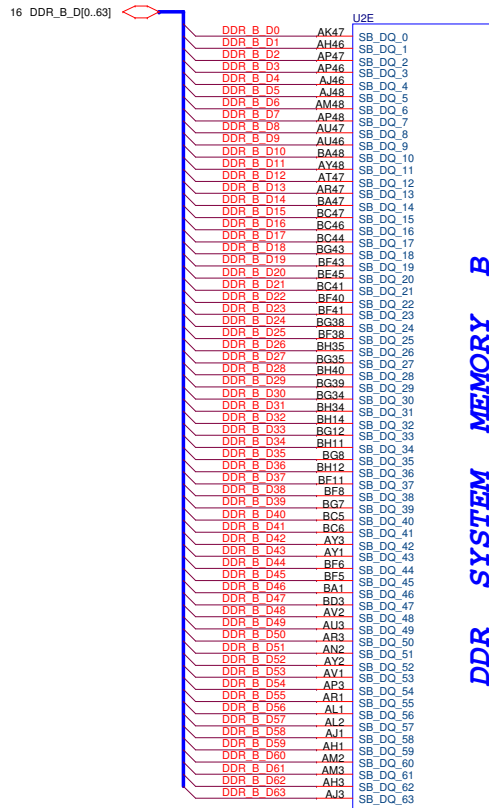
Layout Note: V_DDR_MCH_REF trace width and spacing is 20/20.



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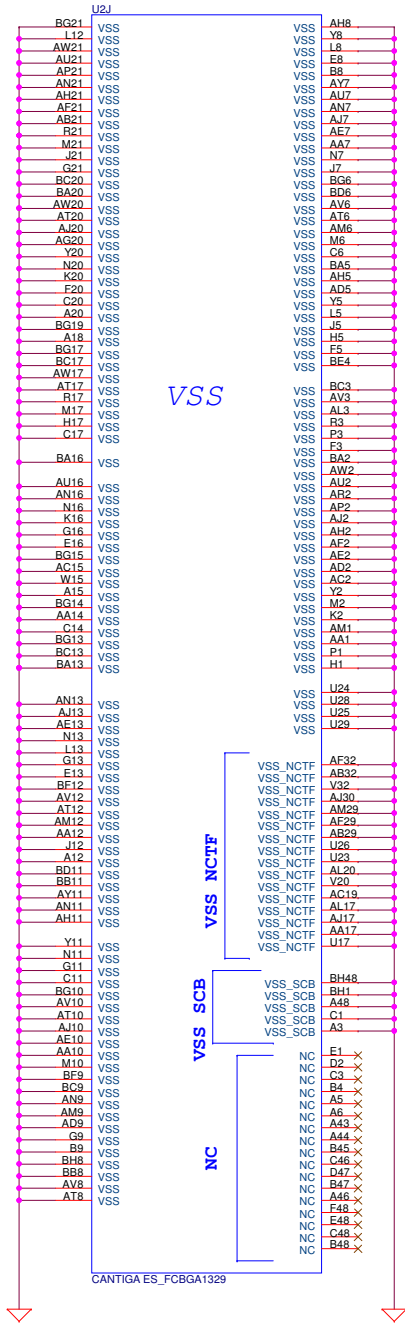
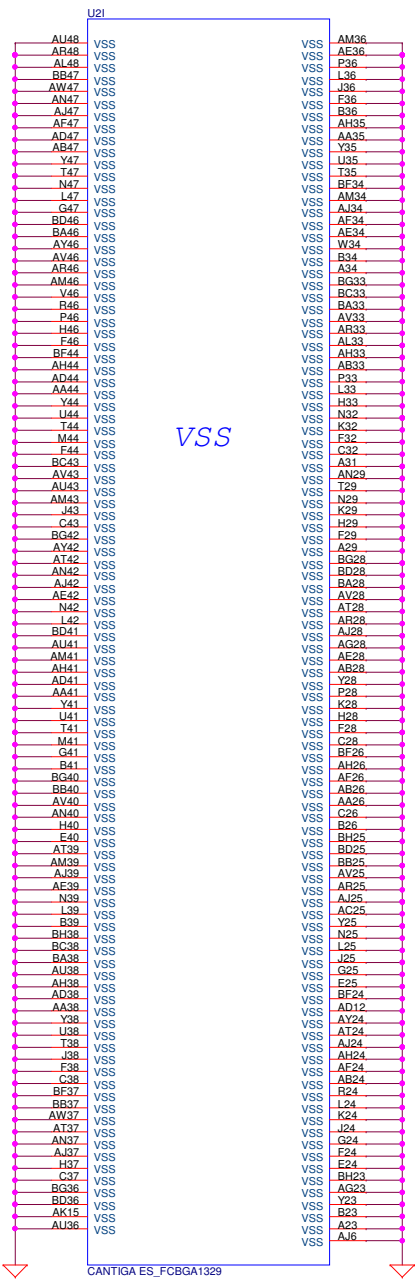


CANTIGA ES_FCBGA1329

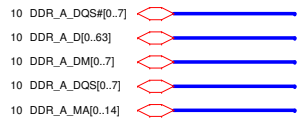


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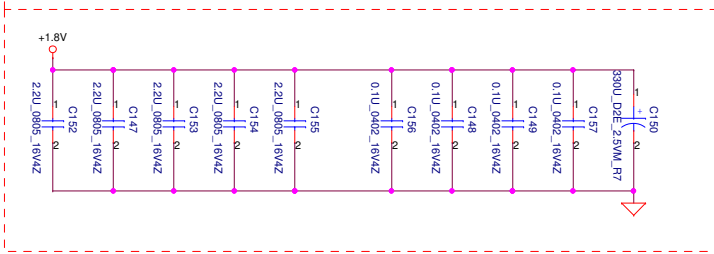
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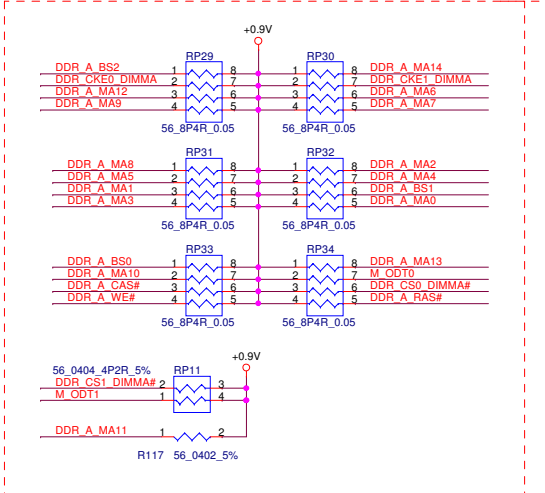
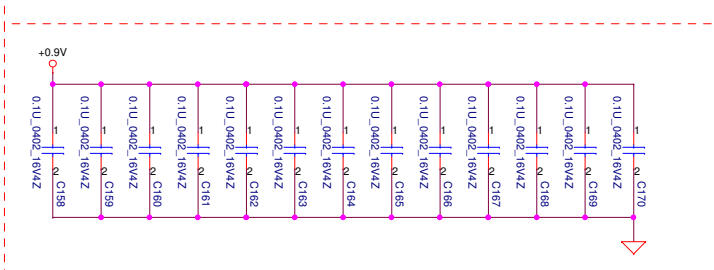
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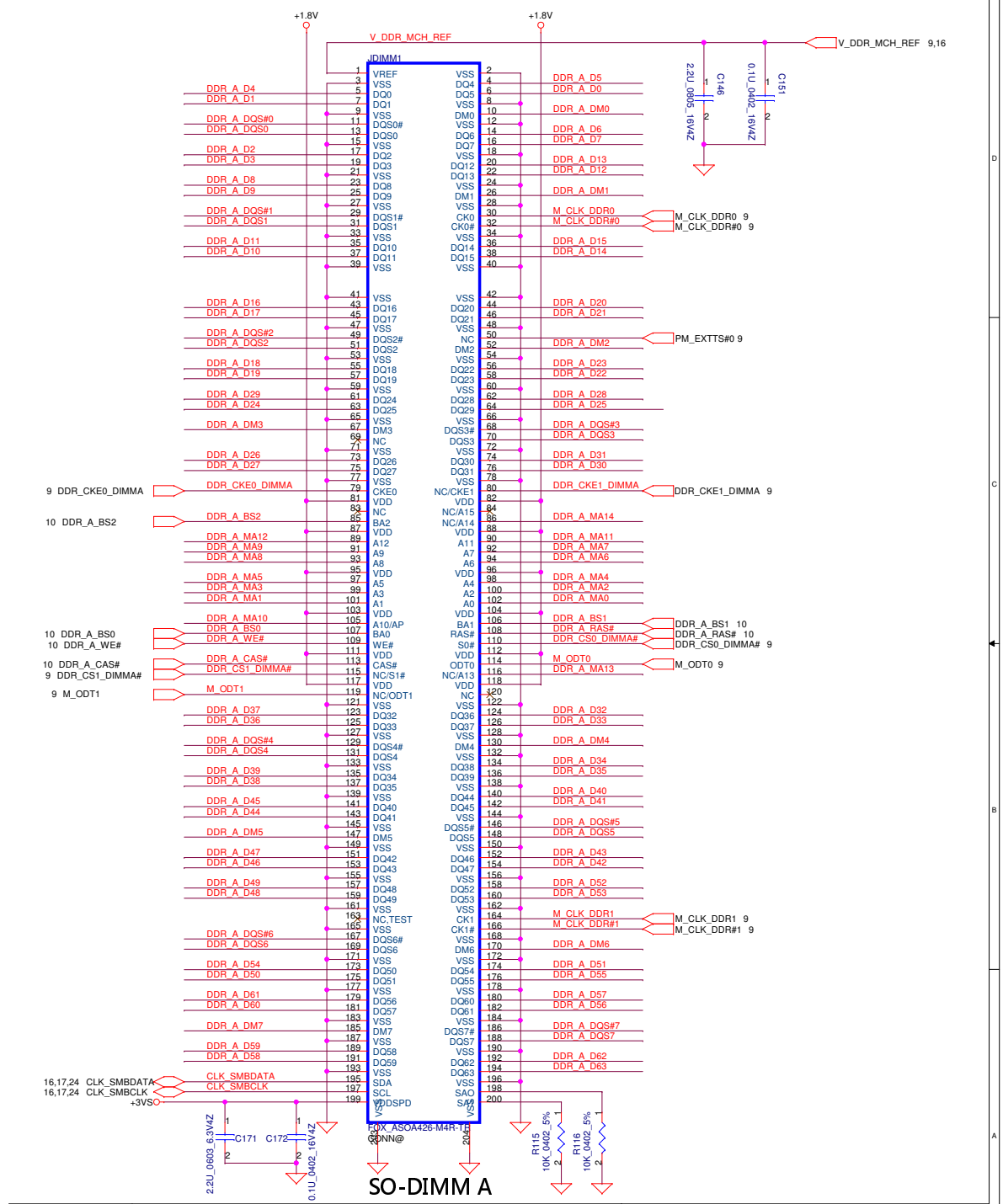
Layout Note:
Place near JP3



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V5

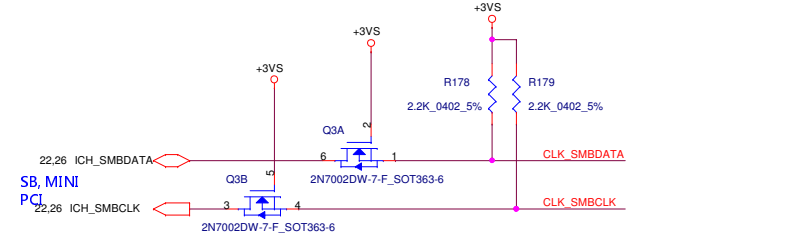
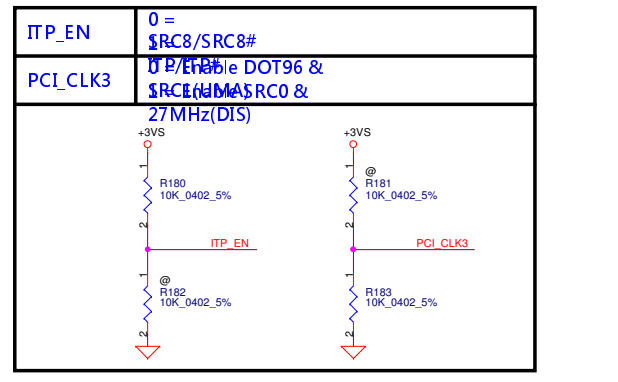
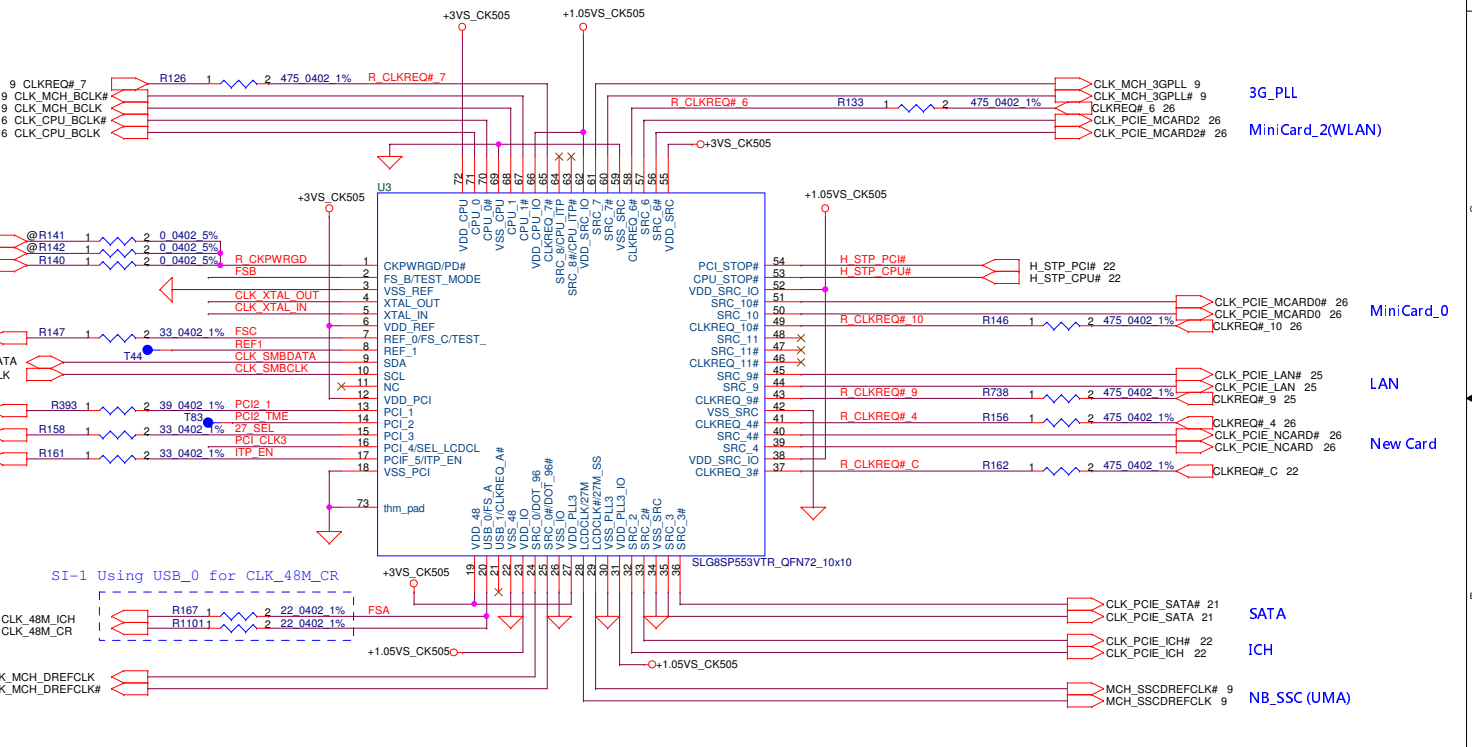
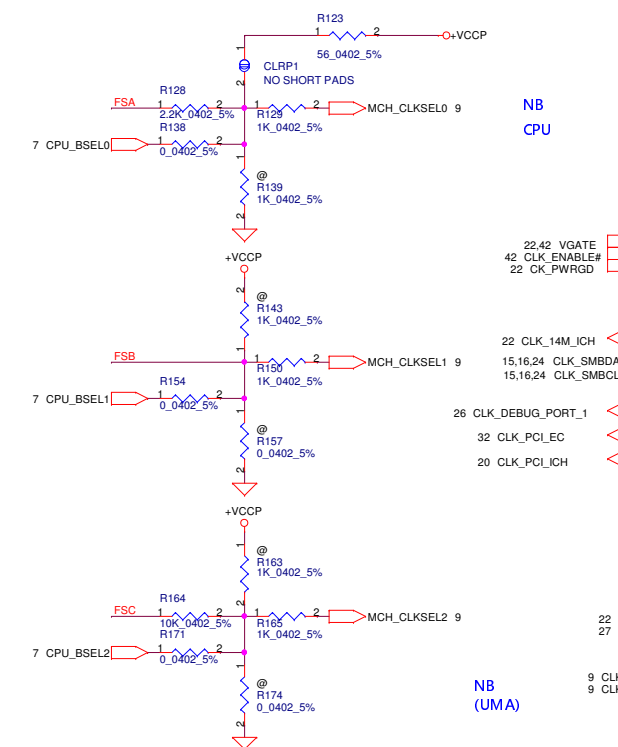
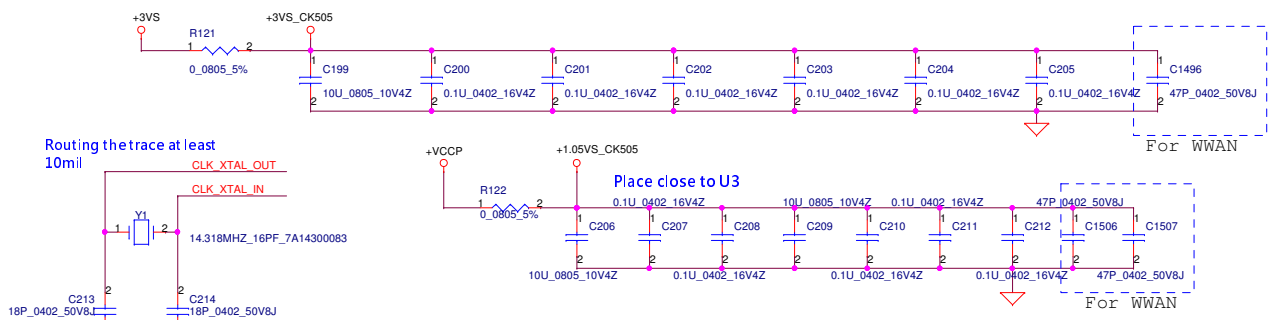


Layout Note:
Place these resistor closely JP3, all trace length Max=1.5"



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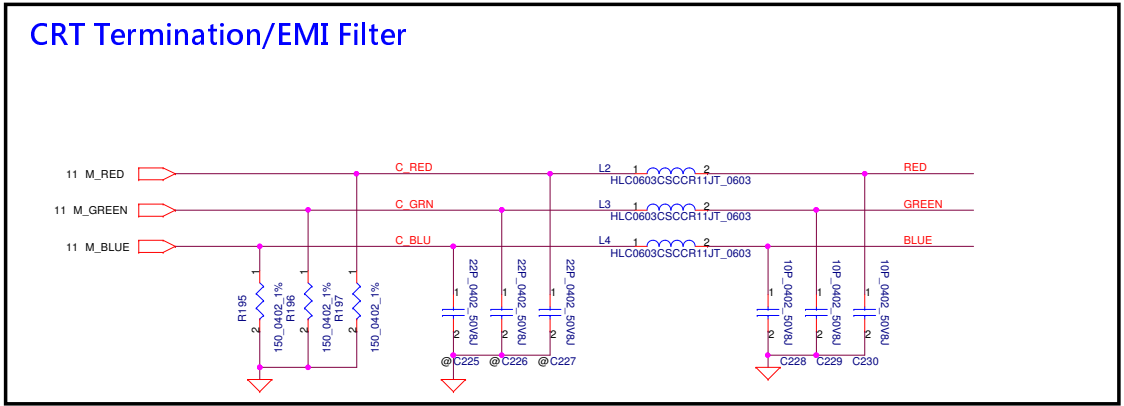
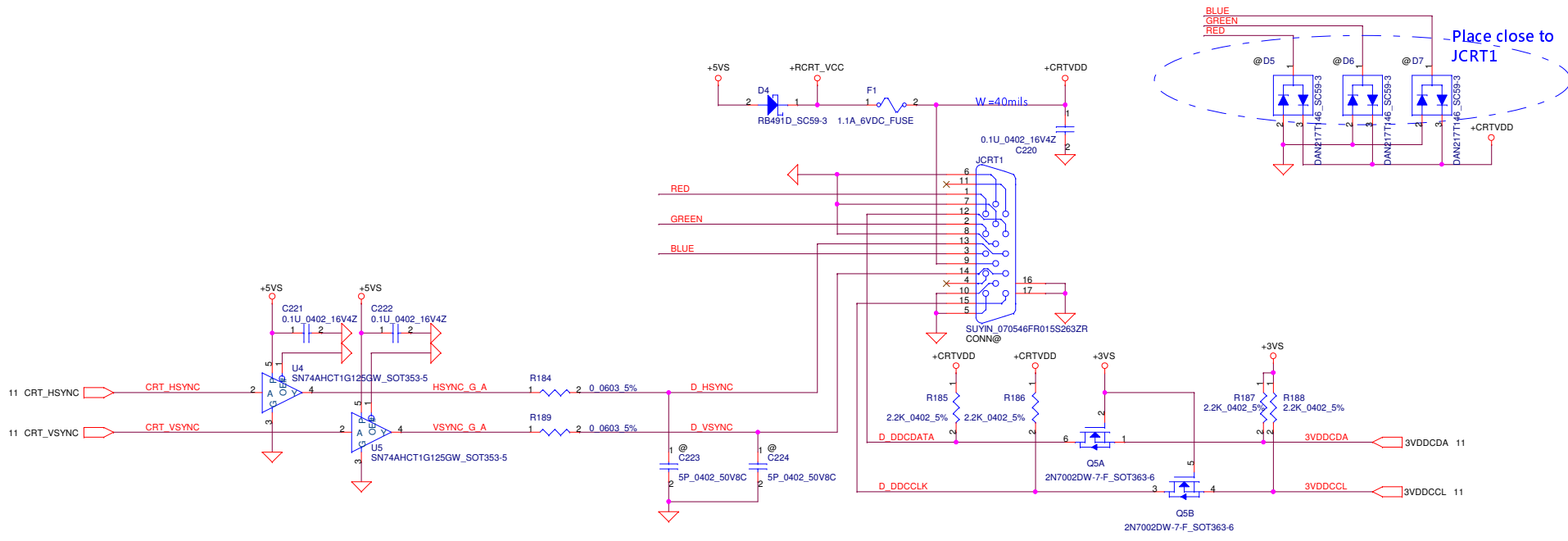
FSC	FSA	FSE	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								



EMI			
@C1482	2	1	CLK 48M_CR
5P_0402_50V8C	2	1	CLK 48M_ICH
5P_0402_50V8C	2	1	CLK 14M_ICH
C216	2	1	CLK PCI_ICH
12P_0402_50V8J	2	1	CLK PCI_EC
@C217	2	1	CLK PCI_EC
47P_0402_50V8J	2	1	CLK DEBUG_PORT_1
@C218	2	1	CLK PCI_EC
47P_0402_50V8J	2	1	CLK DEBUG_PORT_1
@C219	2	1	CLK DEBUG_PORT_1
47P_0402_50V8J	2	1	CLK DEBUG_PORT_1

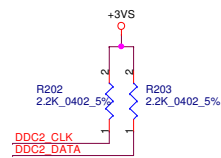
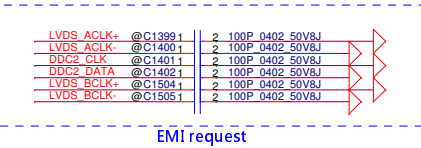
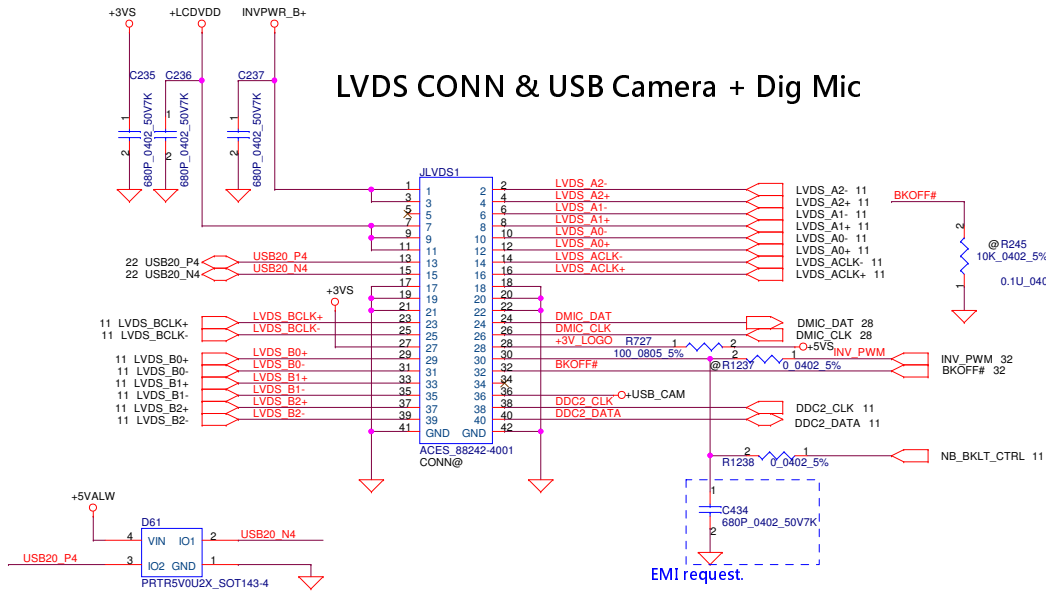
Install C217,C218,C219 for WWAN noise

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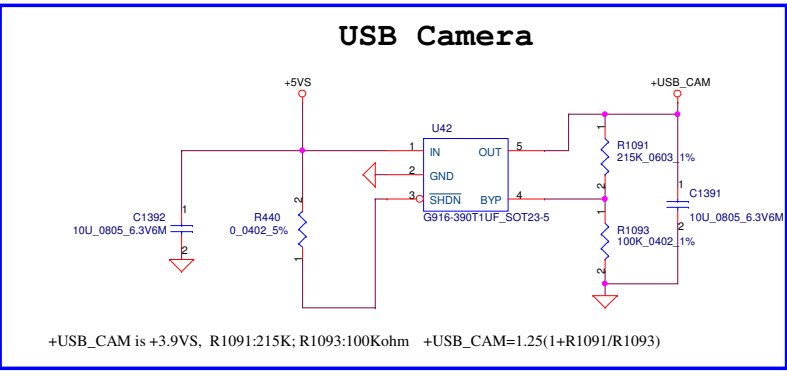
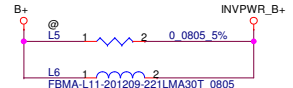
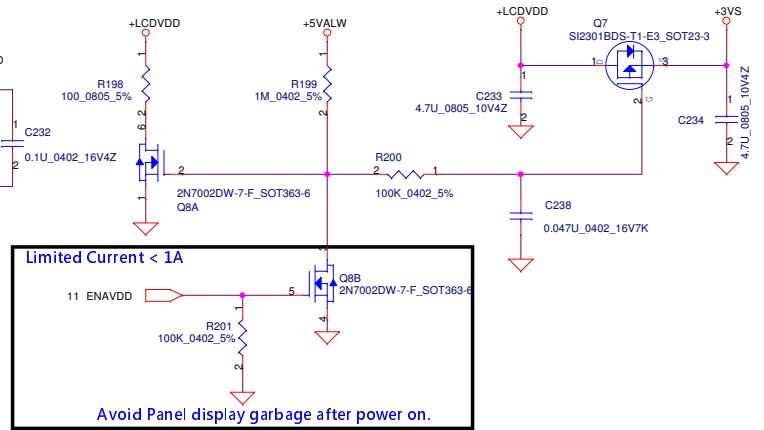
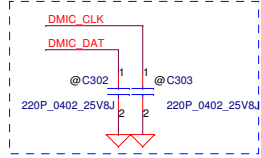


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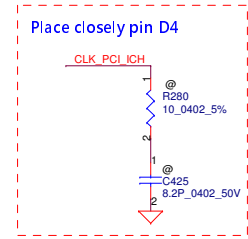
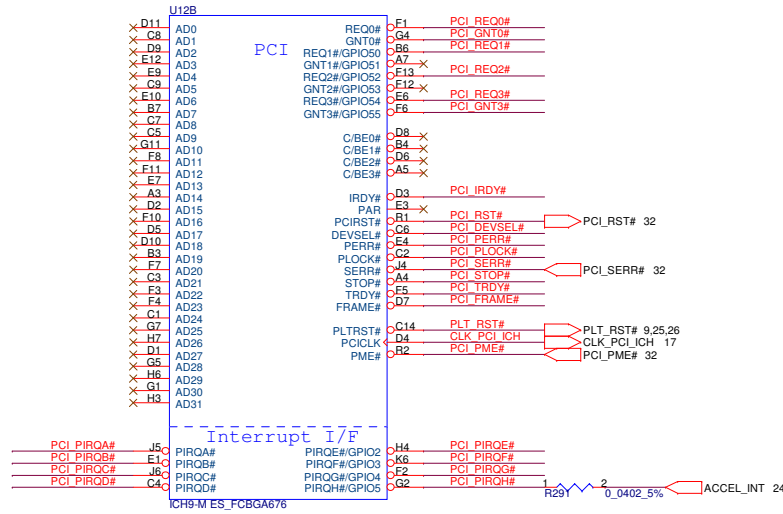
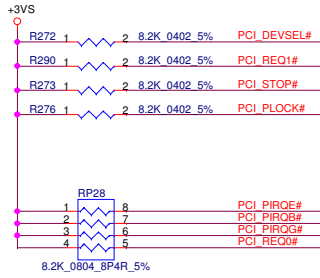
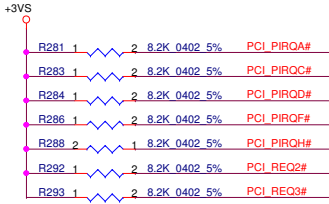
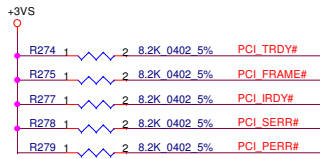
LVDS CONN & USB Camera + Dig Mic



Must close JLVDS1pin 24, 26

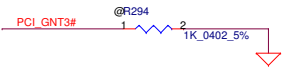


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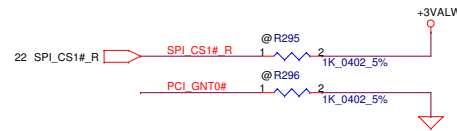
A16 swap override Strap

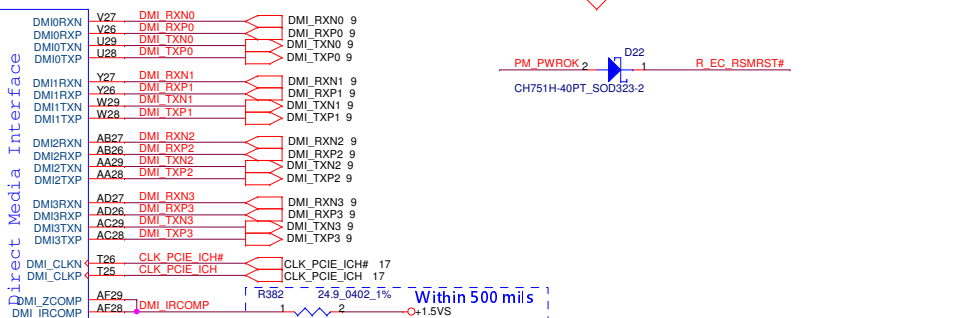
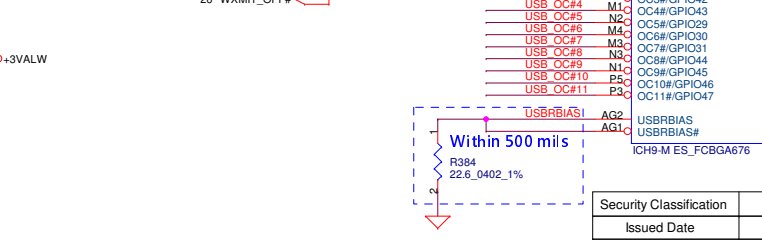
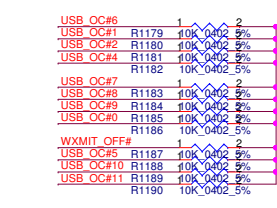
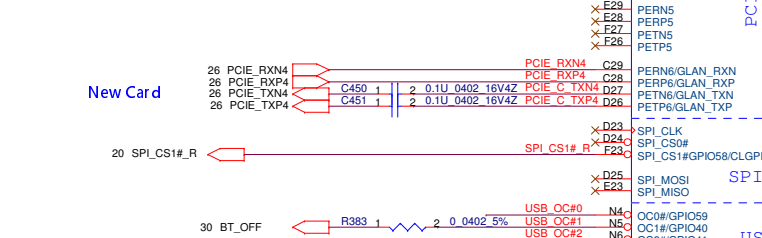
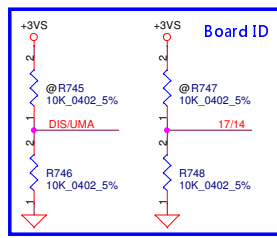
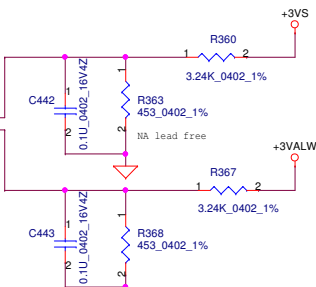
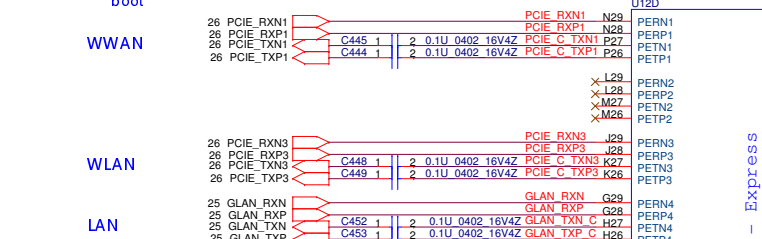
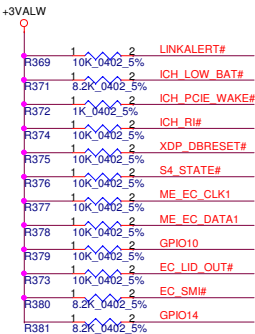
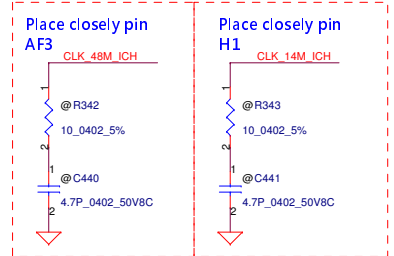
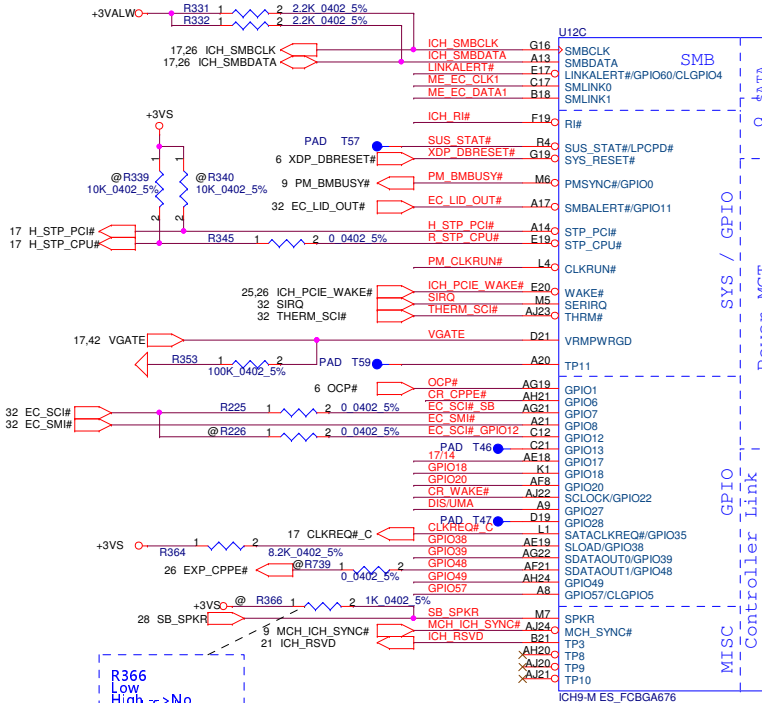
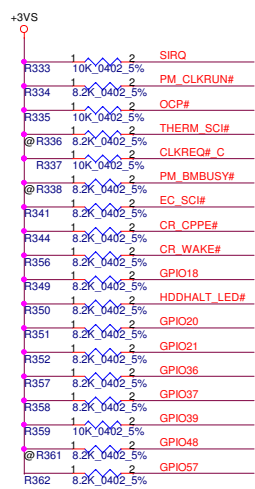
PCI_GNT3# Low= A16 swap override Enable
 High= Default*



Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

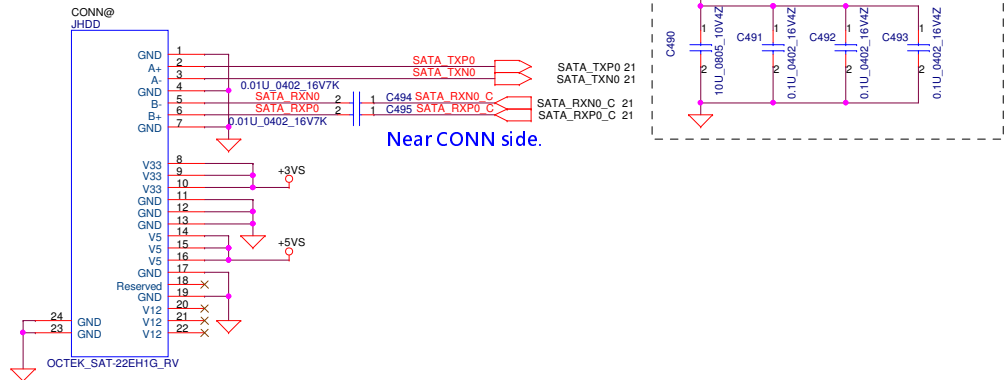




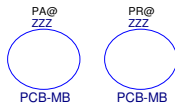
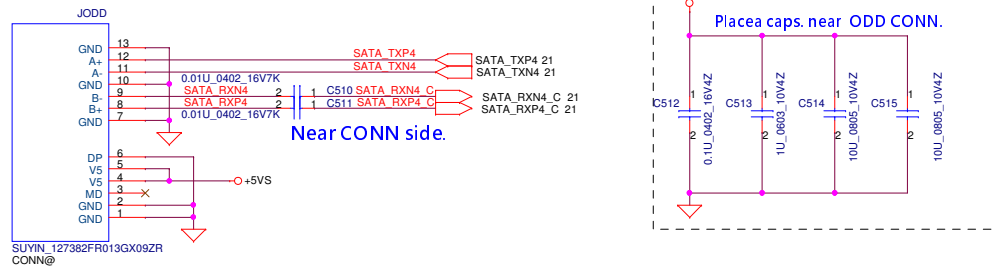
- USB-0 Right side (with ESATA)
- USB-1 Left side
- USB-2 Left side
- USB-3 Cardreader
- USB-4 Camera
- USB-5 WLAN
- USB-6 Bluetooth
- USB-7 Finger Printer
- USB-8
- Mini-Card (WLAN/WiMAX)

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Customer	Montevina UMA	Document Number	IC99(3/4) DMI,USB,GPIO,PCIE	Rev 0.1
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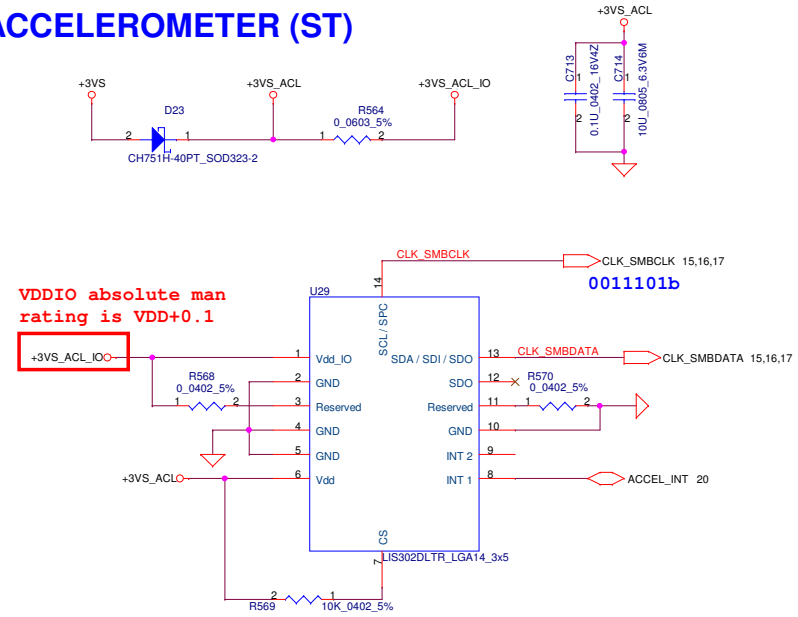
HDD Connector



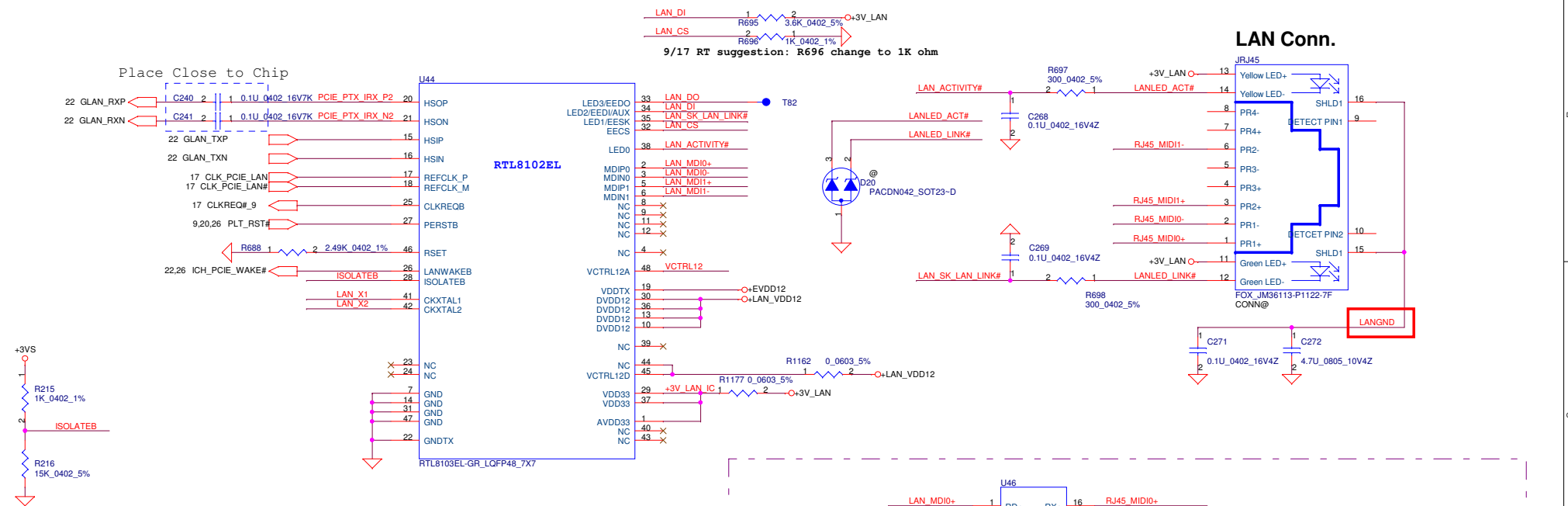
CD-ROM Connector



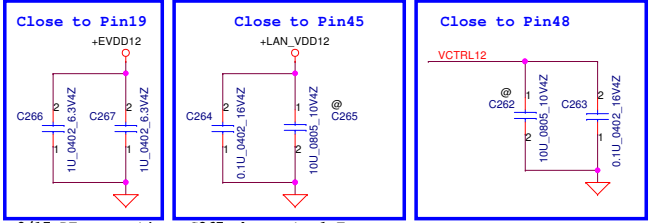
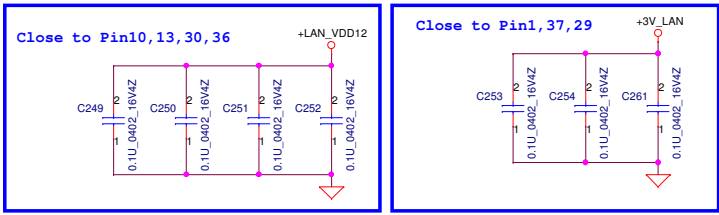
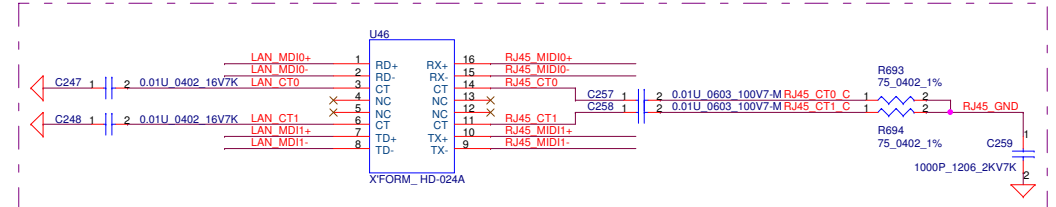
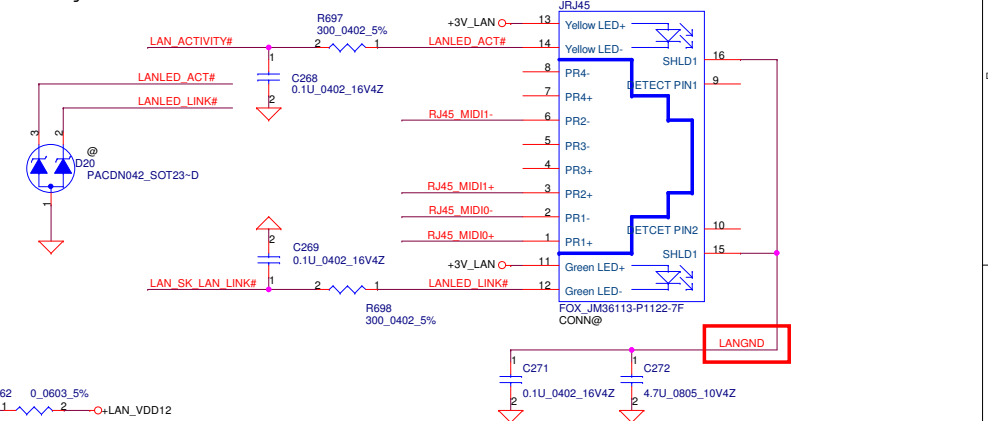
ACCELEROMETER (ST)



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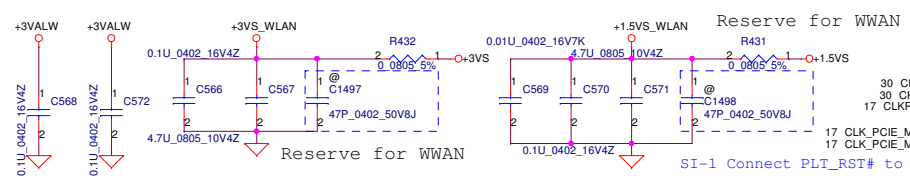
LAN Conn.



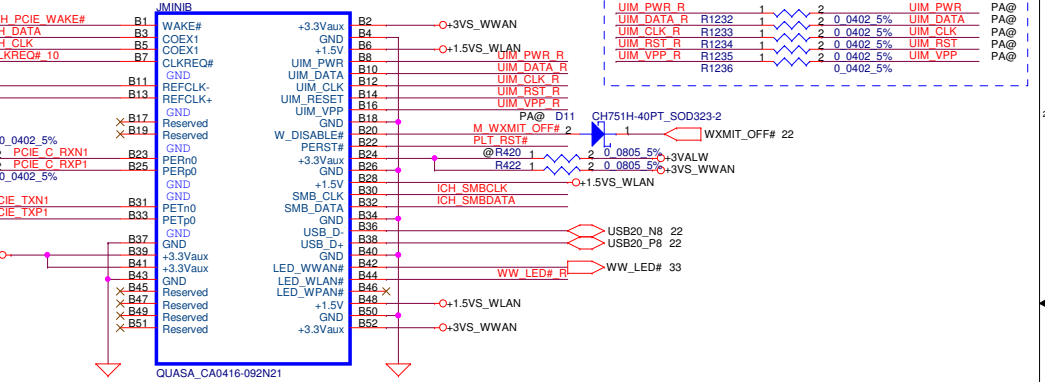
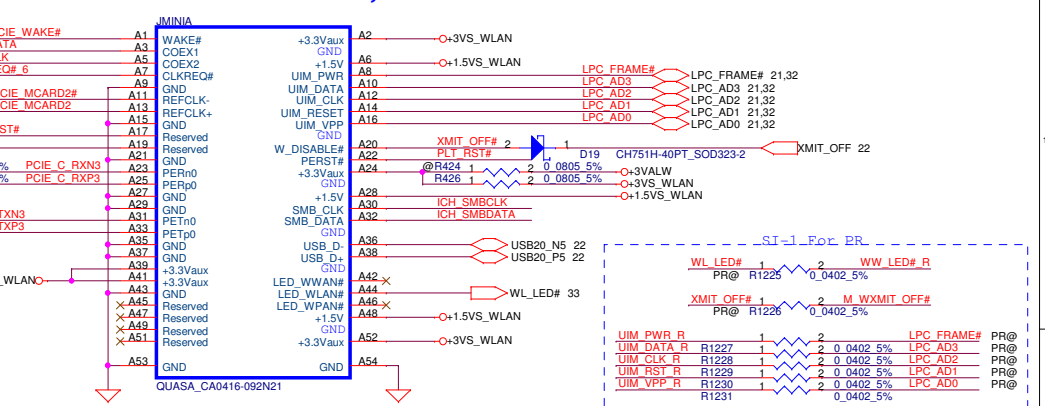
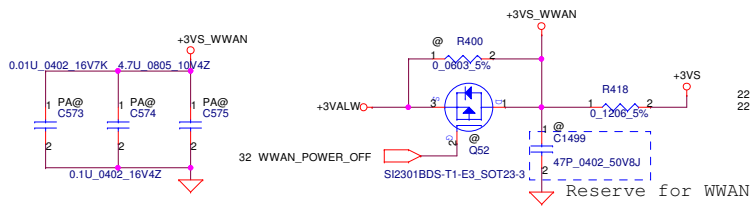
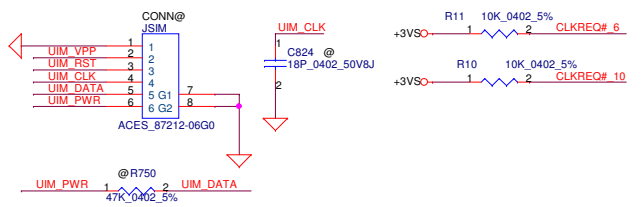
9/17 RT suggestion: C267 change to 1uF

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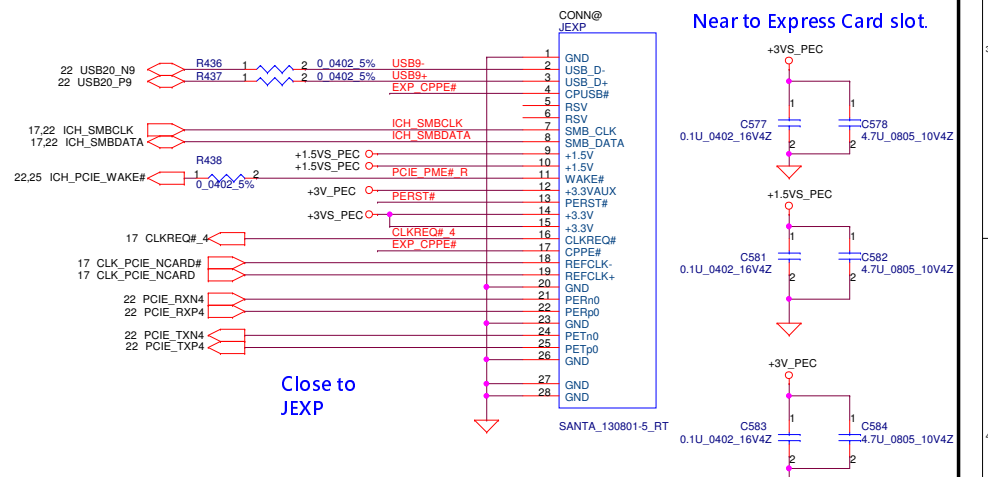
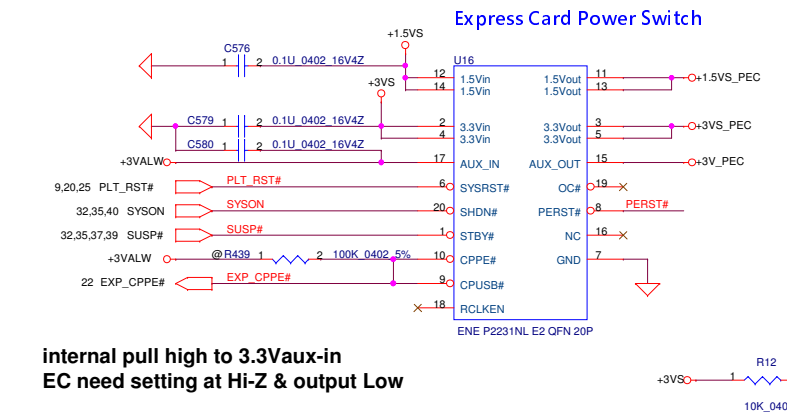
Mini Card Slot ---WLAN,WWAN



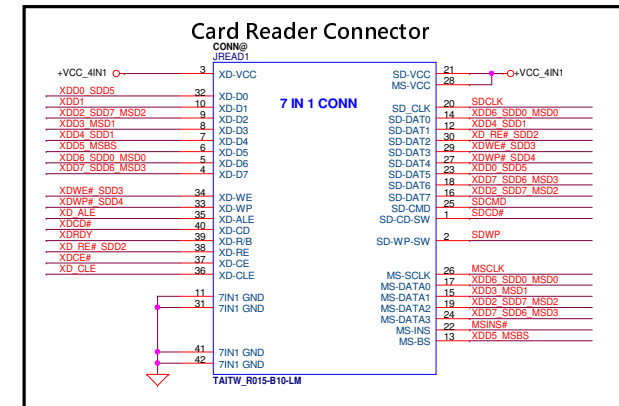
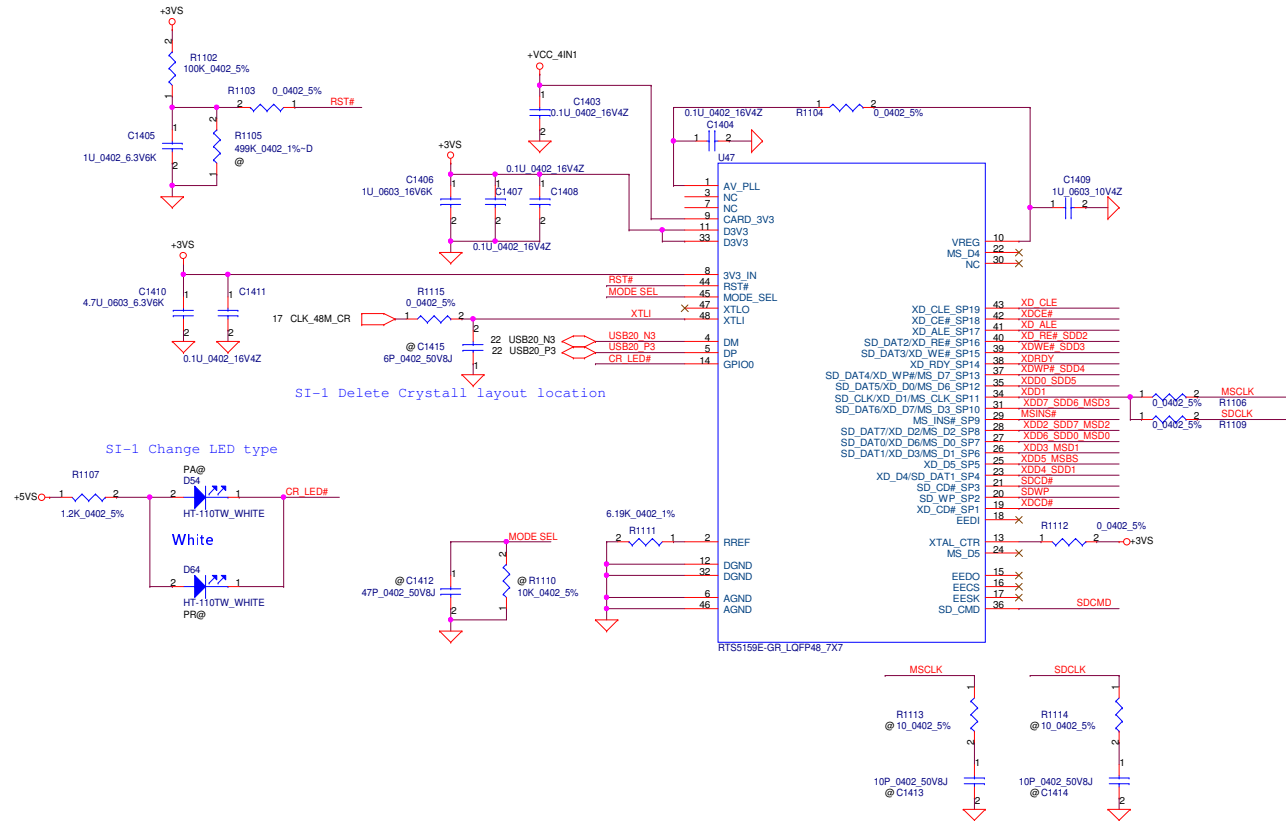
SIM card Connector



New Card



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Document Number Montevina UMA			Rev 0.1	
Date: Wednesday, February 18, 2009 Sheet 26 of 46				

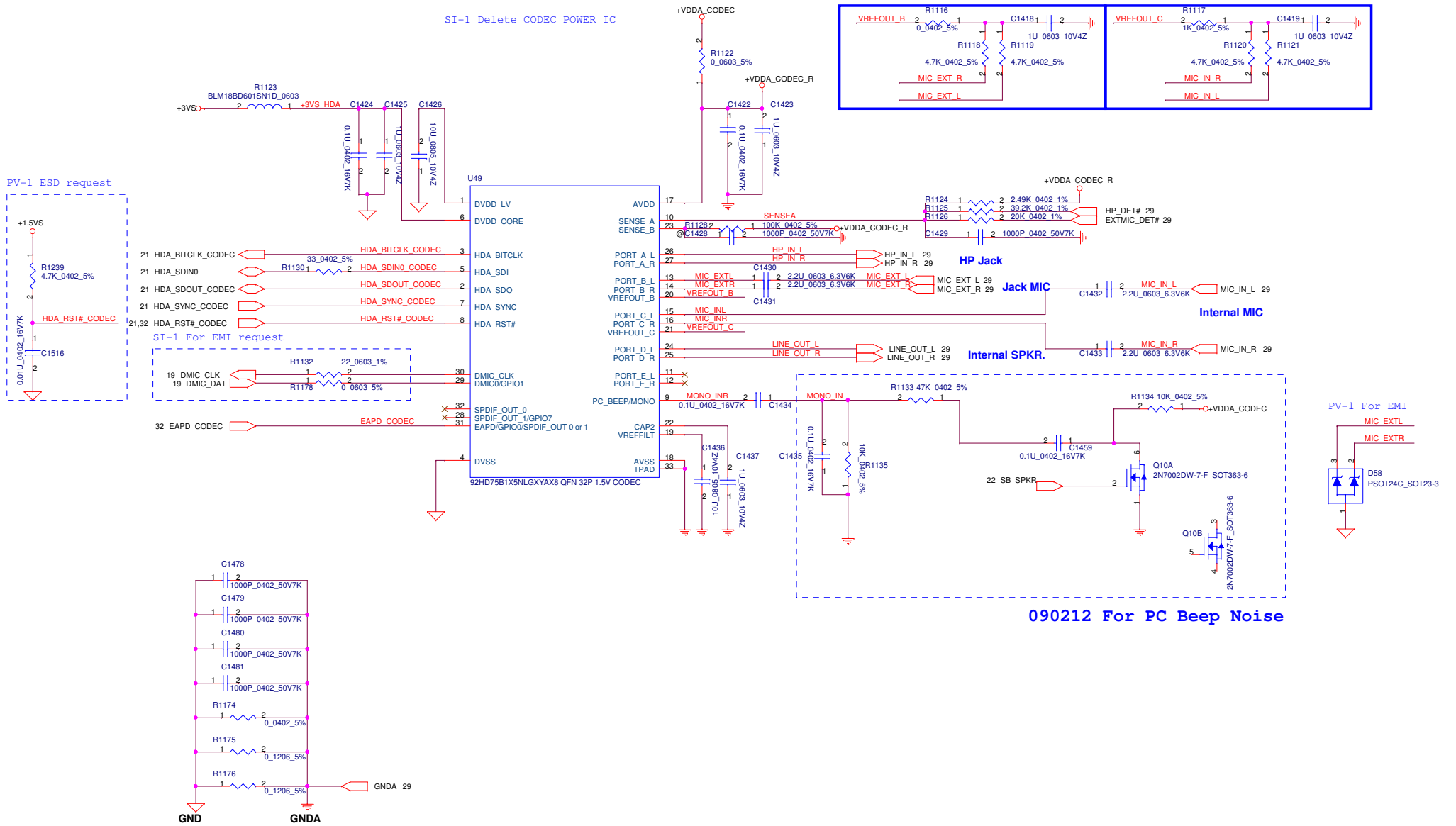


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Issued Date	2007/08/28	Deciphered Date	2006/10/06	Size		Document Number
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Date:	Wednesday, February 18, 2009	Sheet	27	of	46	Rev
						0.1

CODEC POWER

(4.75V(4.56-4.94V)) 300mA

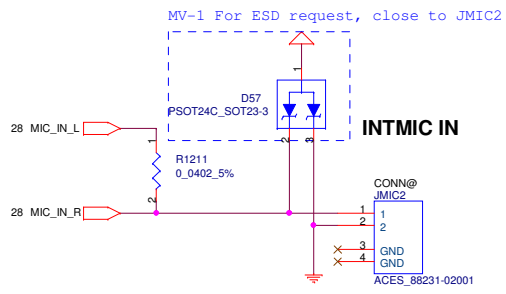
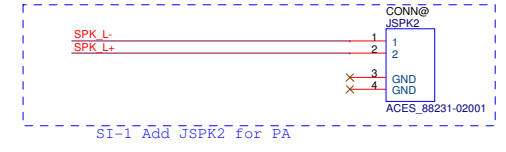
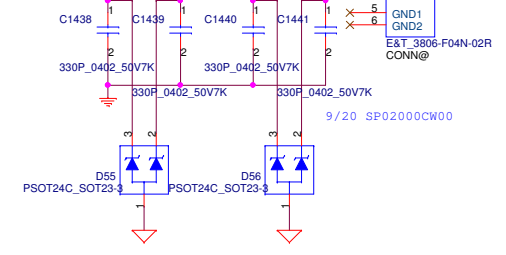
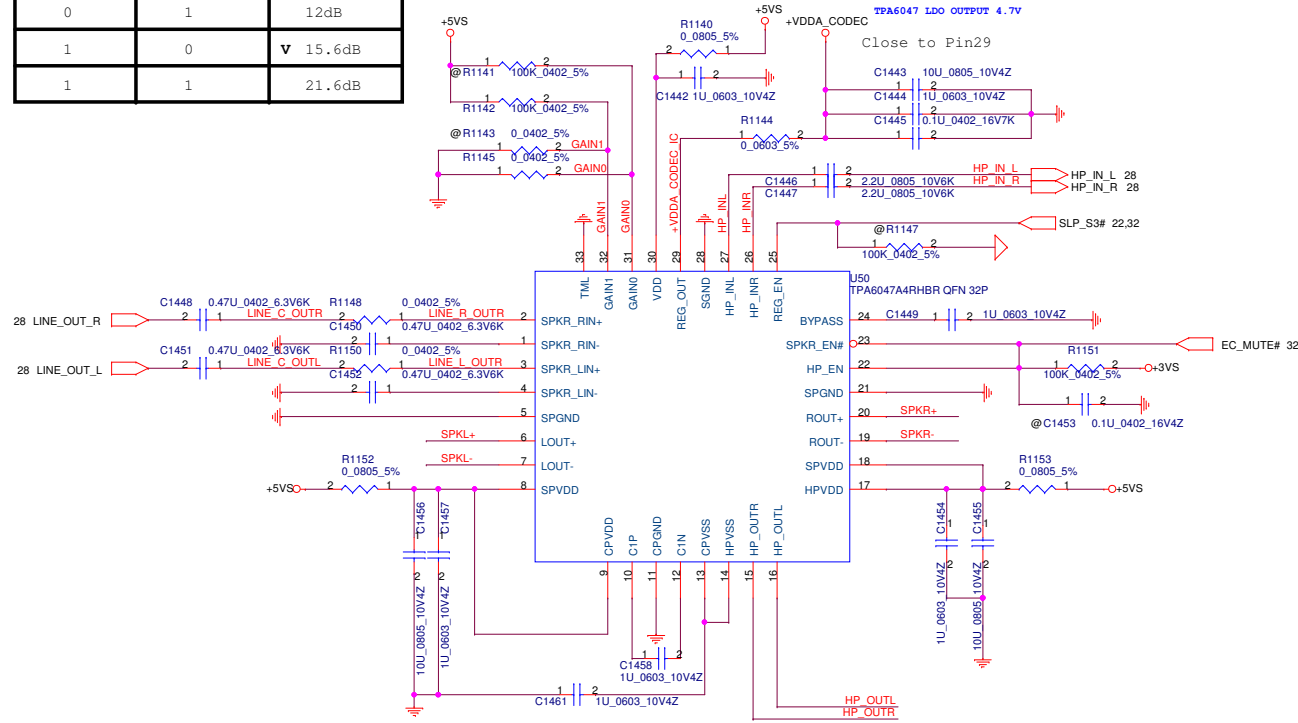
SI-1 Delete CODEC POWER IC



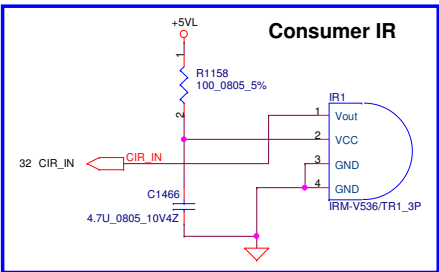
Security Classification	Compal Secret Data		Title	Codec_IDT9275B
Issued Date	2007/08/28	Deciphered Date	2006/07/26	Rev
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AMP. FOR INTERNAL SPEAKER

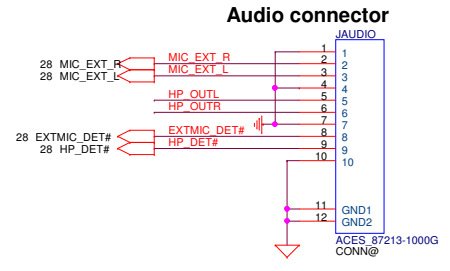
GAIN1	GAIN0	Av (inv)
0	0	10dB
0	1	12dB
1	0	V 15.6dB
1	1	21.6dB



SI-1 Change IR1 to SCR00000E00

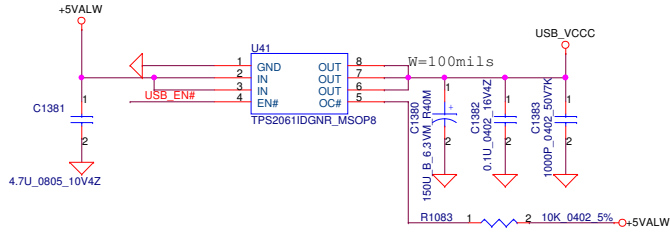


SI-1 Add Audio board connector

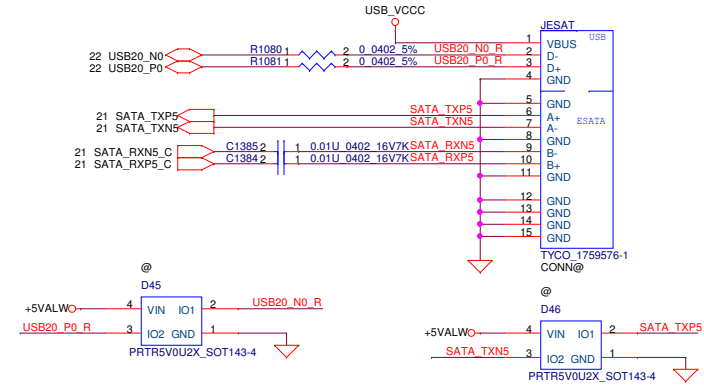


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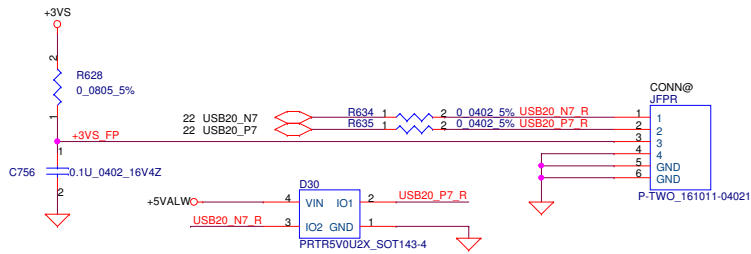
Right side USB Power Switch



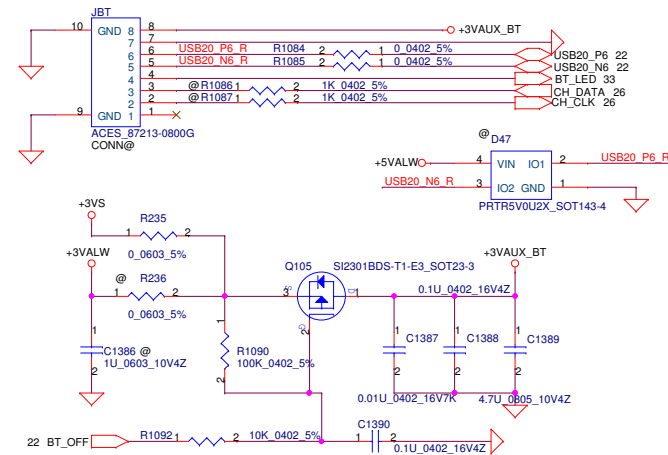
Right side eSATA/USB combination Connector



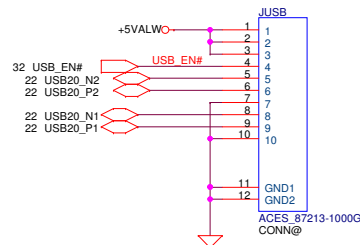
Finger printer



BT Connector

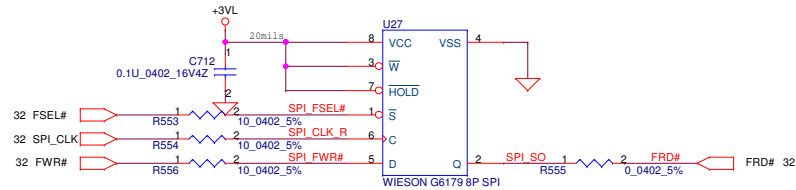


USB cable connector for Right side

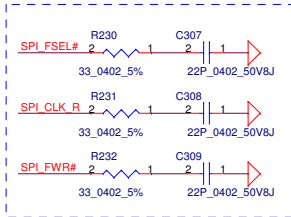


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SPI ROM

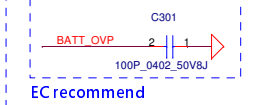
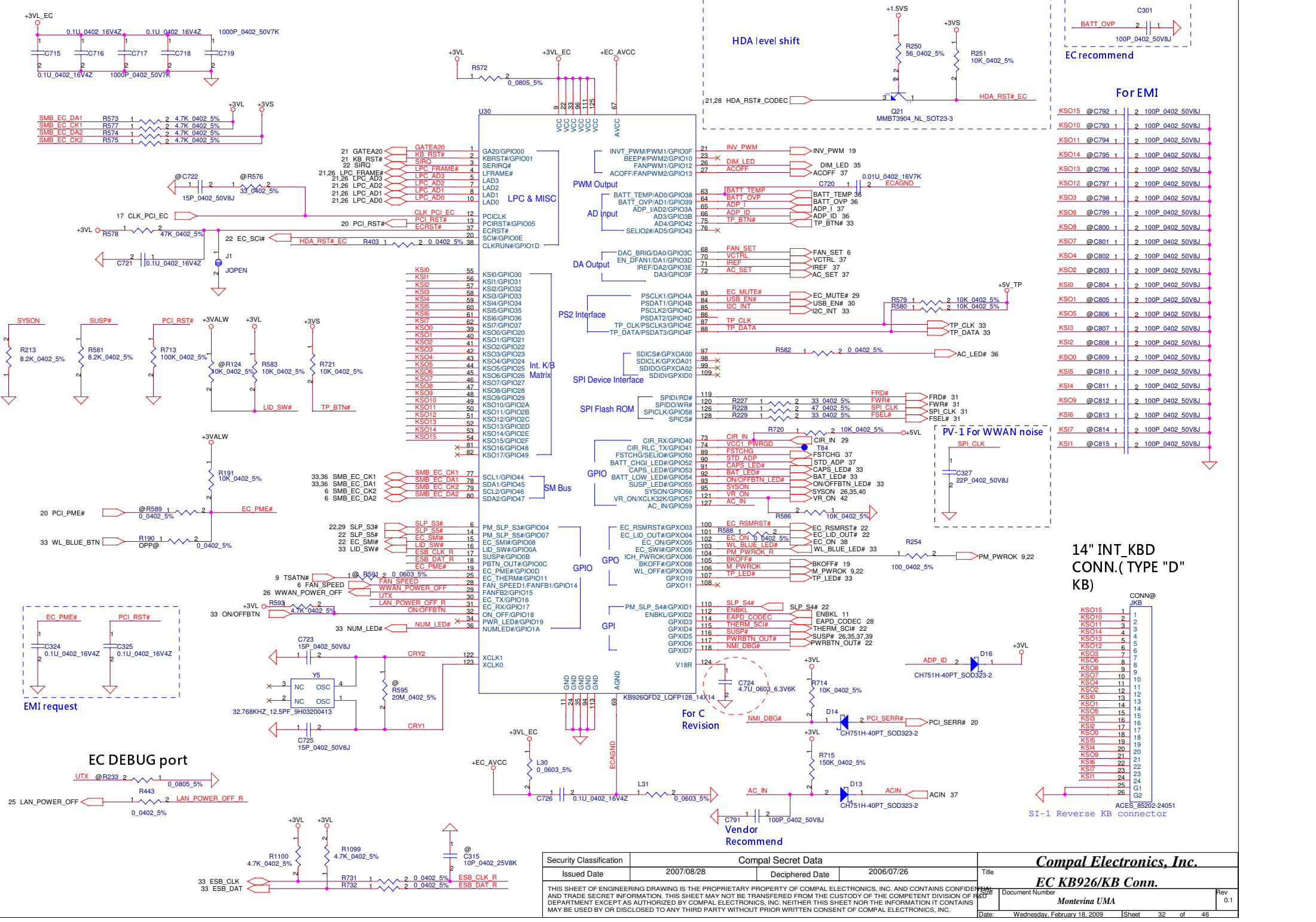


SP07000F500 S SOCKET WIESON G6179-100000 8P SPIFLASH
WIESO_G6179-100000_8P



EMI request

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For EMI

KS015 @C792	1	2	100P_0402_50V8J
KS010 @C793	1	2	100P_0402_50V8J
KS011 @C794	1	2	100P_0402_50V8J
KS014 @C795	1	2	100P_0402_50V8J
KS013 @C796	1	2	100P_0402_50V8J
KS012 @C797	1	2	100P_0402_50V8J
KS03 @C798	1	2	100P_0402_50V8J
KS06 @C799	1	2	100P_0402_50V8J
KS08 @C800	1	2	100P_0402_50V8J
KS07 @C801	1	2	100P_0402_50V8J
KS04 @C802	1	2	100P_0402_50V8J
KS02 @C803	1	2	100P_0402_50V8J
KS10 @C804	1	2	100P_0402_50V8J
KS01 @C805	1	2	100P_0402_50V8J
KS05 @C806	1	2	100P_0402_50V8J
KS13 @C807	1	2	100P_0402_50V8J
KS12 @C808	1	2	100P_0402_50V8J
KS00 @C809	1	2	100P_0402_50V8J
KS15 @C810	1	2	100P_0402_50V8J
KS14 @C811	1	2	100P_0402_50V8J
KS09 @C812	1	2	100P_0402_50V8J
KS16 @C813	1	2	100P_0402_50V8J
KS17 @C814	1	2	100P_0402_50V8J
KS11 @C815	1	2	100P_0402_50V8J

14" INT_KBD CONN.(TYPE "D" KB)

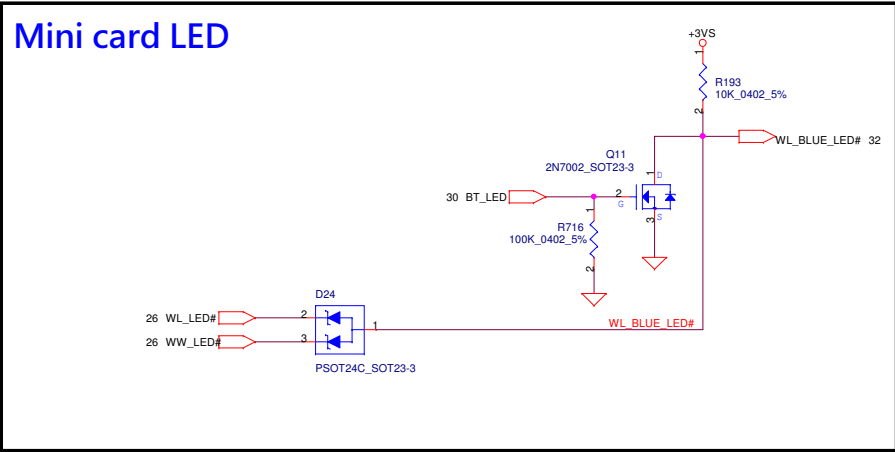
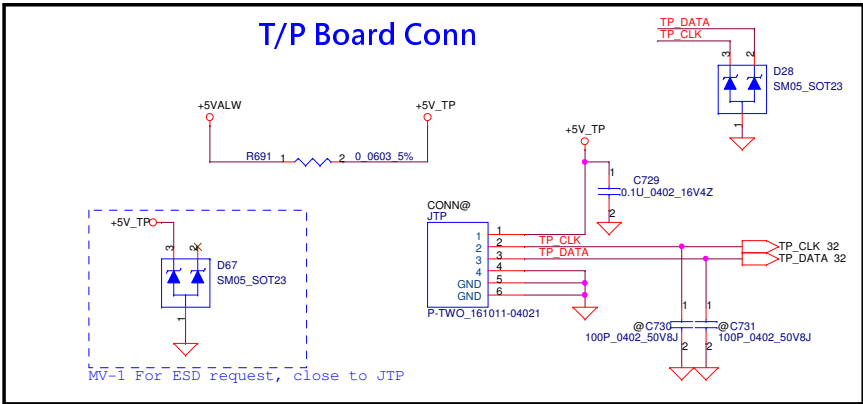
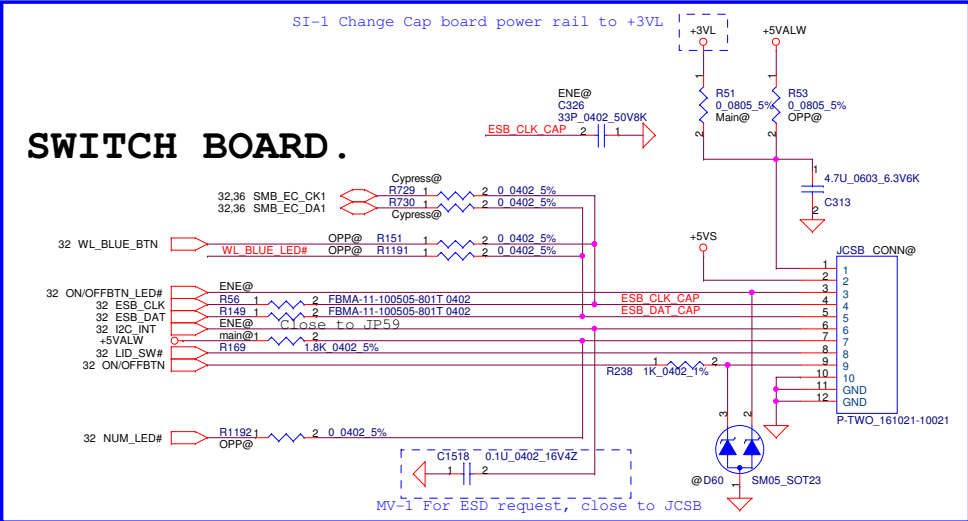
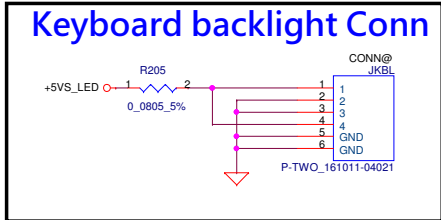
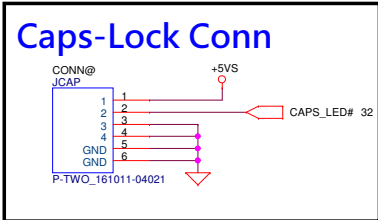
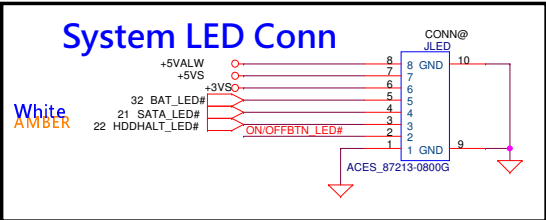
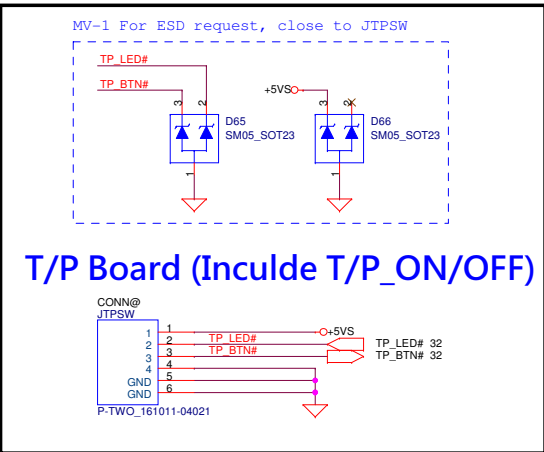
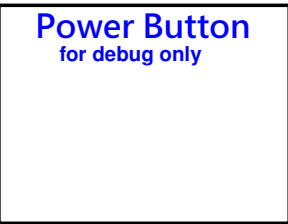
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KS01	2
KS011	3
KS014	4
KS013	5
KS012	6
KS06	7
KS08	8
KS07	9
KS04	10
KS10	11
KS01	12
KS10	13
KS01	14
KS05	15
KS16	16
KS12	17
KS15	18
KS15	19
KS14	20
KS09	21
KS16	22
KS17	23
KS11	24
G1	25
G1	26

ACES_B5202-24051
SI-1 Reverse KB connector

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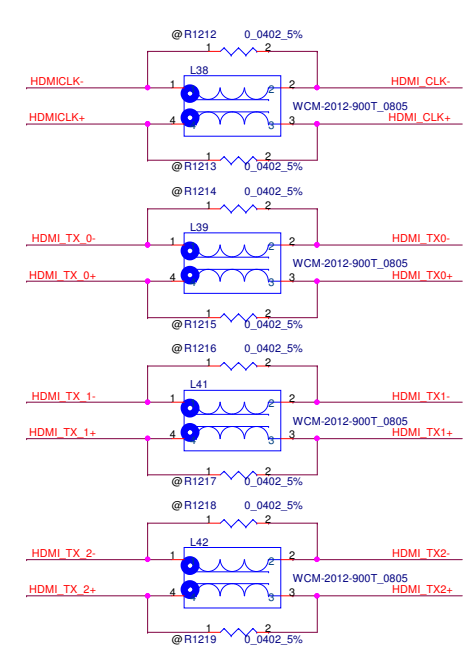
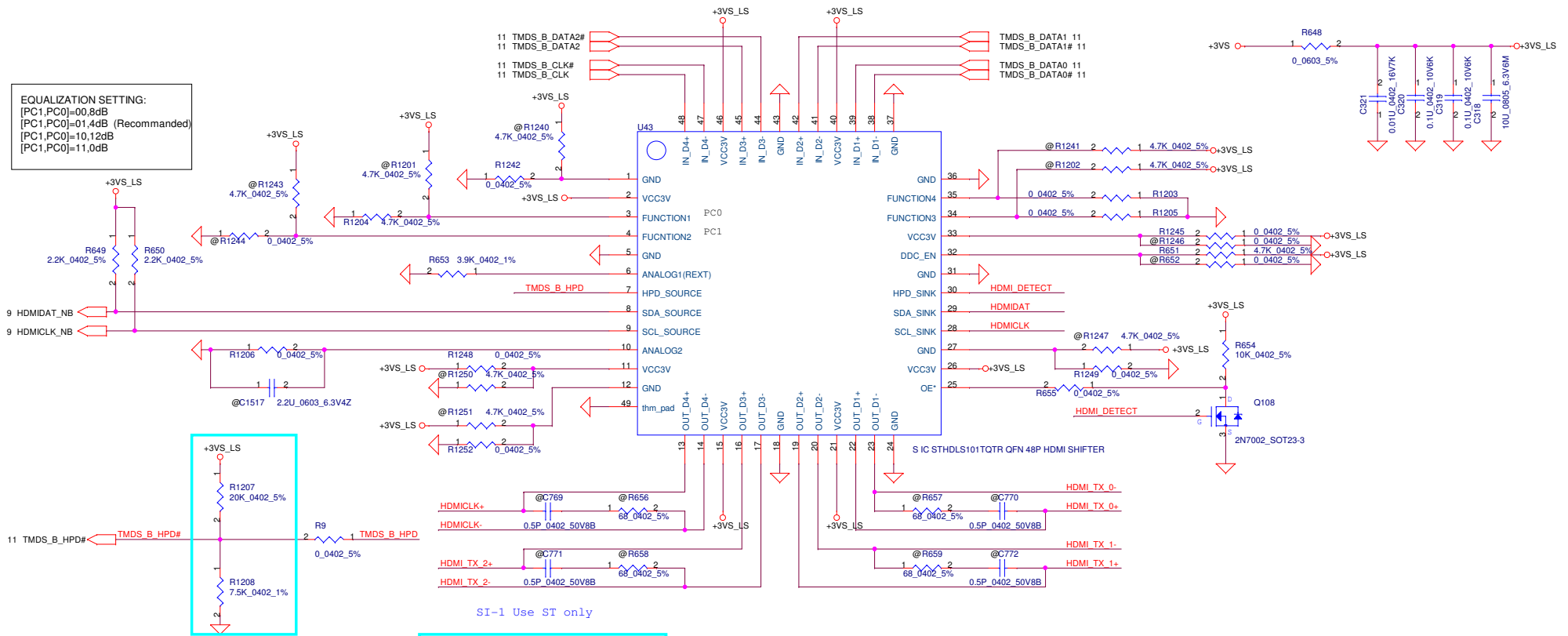
Compal Electronics, Inc.	
EC KB926/KB Conn.	
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SI-1 Delete SW2



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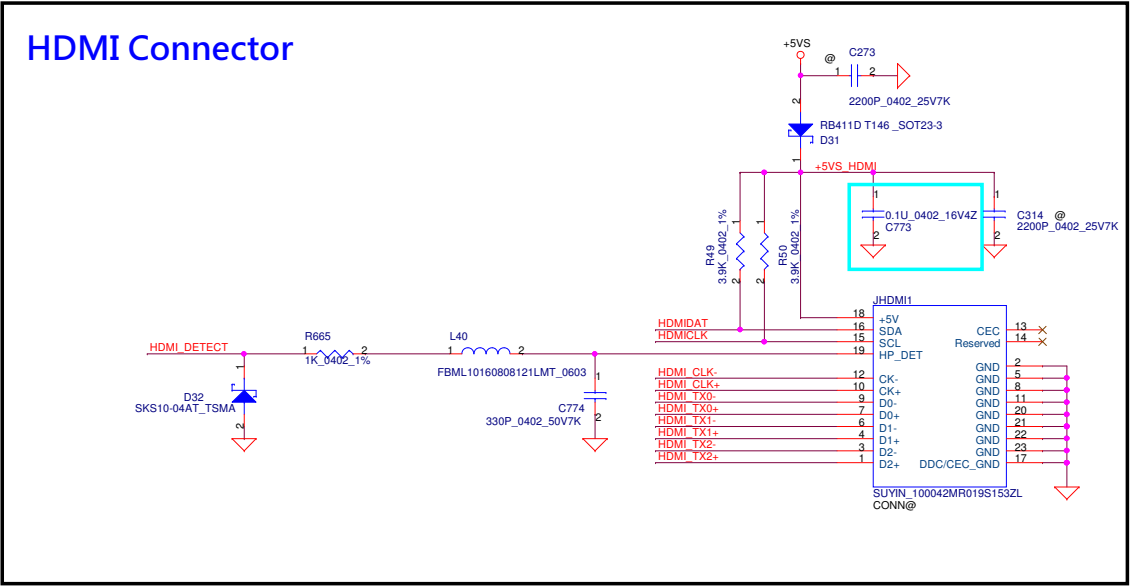
EQUALIZATION SETTING:
 [PC1,PC0]=00,8dB
 [PC1,PC0]=01,4dB (Recommended)
 [PC1,PC0]=10,12dB
 [PC1,PC0]=11,0dB

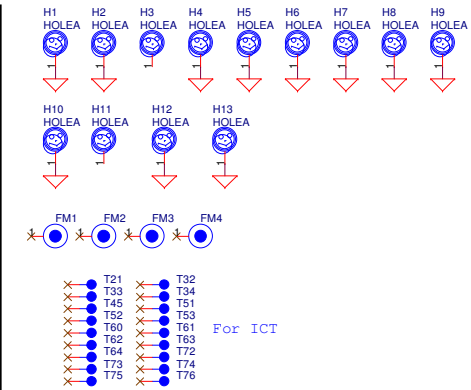
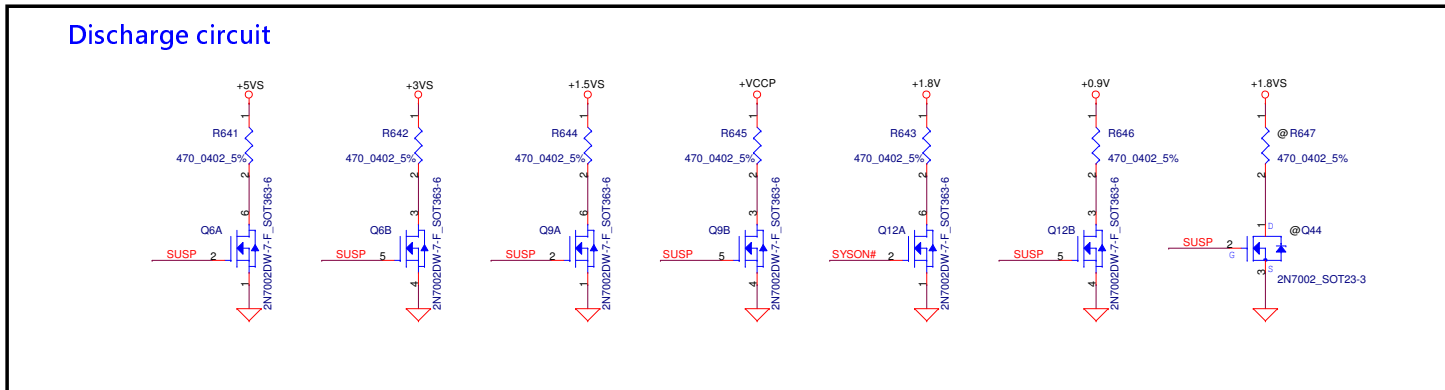
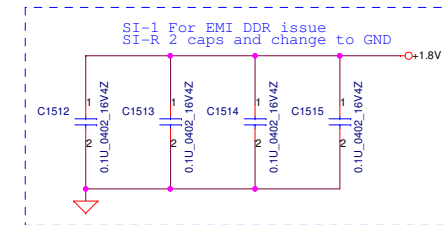
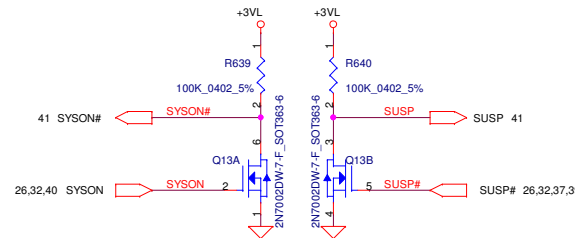
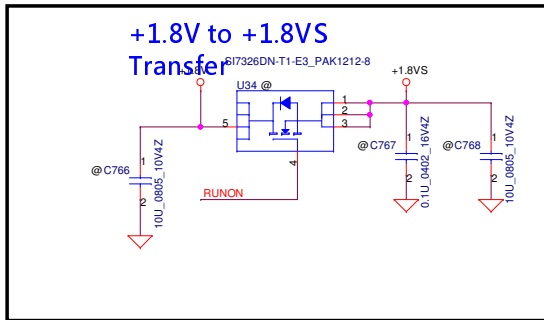
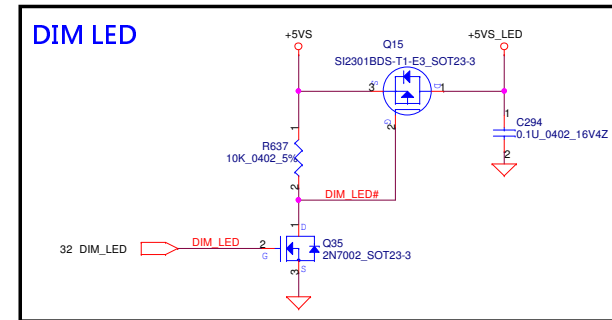
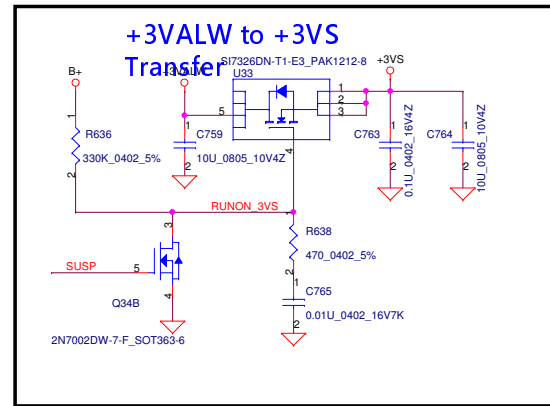
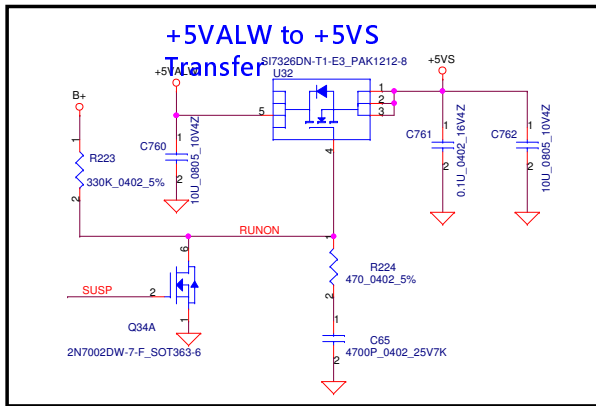


To option use ST or Parade

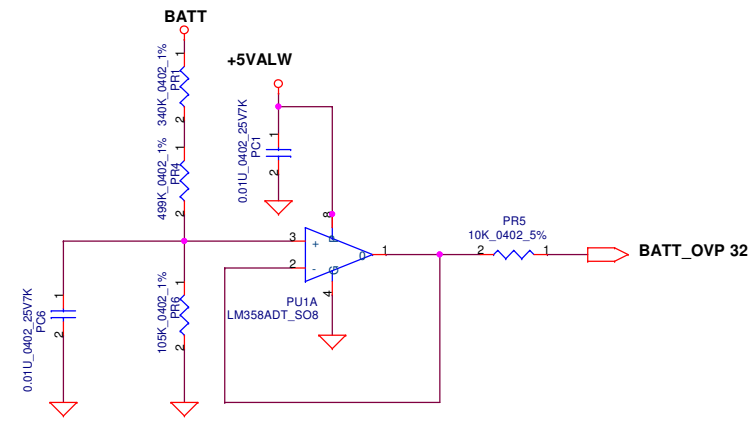
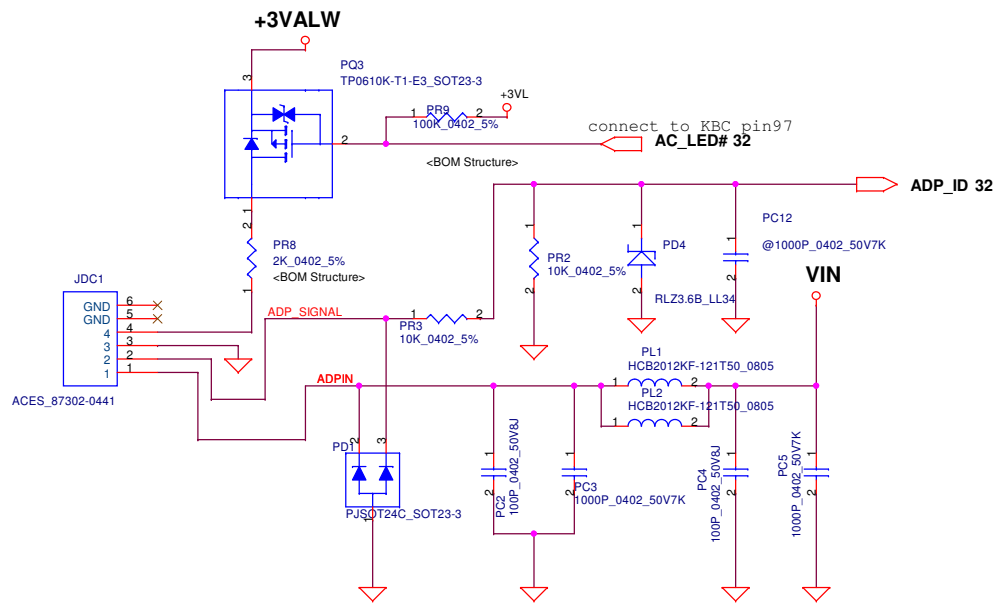
	ST	Parade 81011	Parade 8171
R1240	X	X	X
R1242	0 ohm	0 ohm	4.7K ohm
R1201	X	4.7K ohm	X
R1204	4.7K ohm	X	4.7K ohm
R1243	X	X	4.7K ohm
R1244	X	X	X
R653	3.9K ohm	499 ohm	499 ohm
R1206	0 ohm	X	X
C1517	X	X	2.2uF
R1248	0 ohm	0 ohm	X
R1250	X	X	4.7K ohm
R1251	X	X	4.7K ohm
R1252	0 ohm	0 ohm	X
R1247	X	X	4.7K ohm
R1249	0 ohm	0 ohm	X
R1245	0 ohm	0 ohm	X
R1246	X	X	4.7K ohm
R1203	0 ohm	X	4.7K ohm
R1241	X	X	X
R1205	0 ohm	X	X
R1202	X	X	4.7K ohm
C773	0.1uF	1uF	1uF
R1207	V	X	X
R1208	V	X	X

HDMI Connector

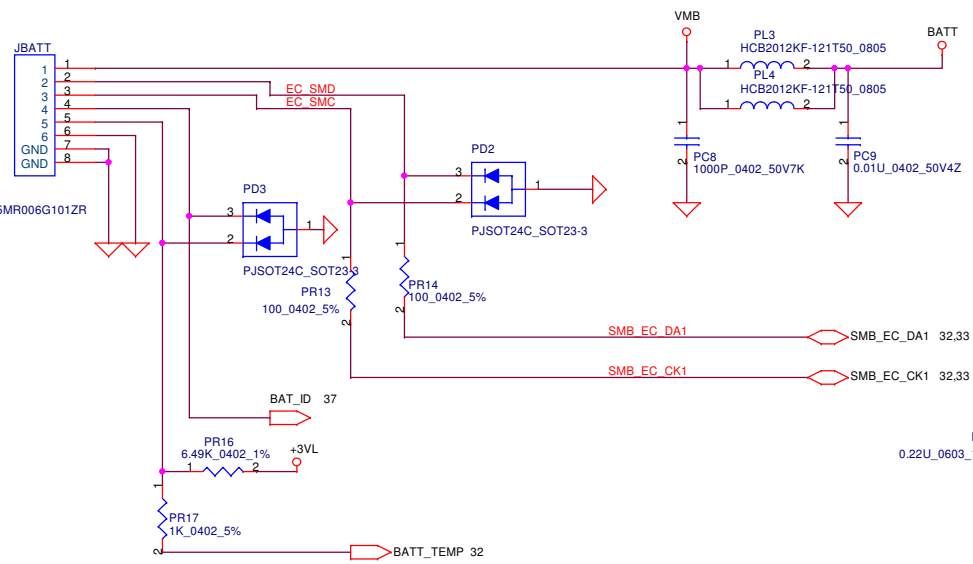
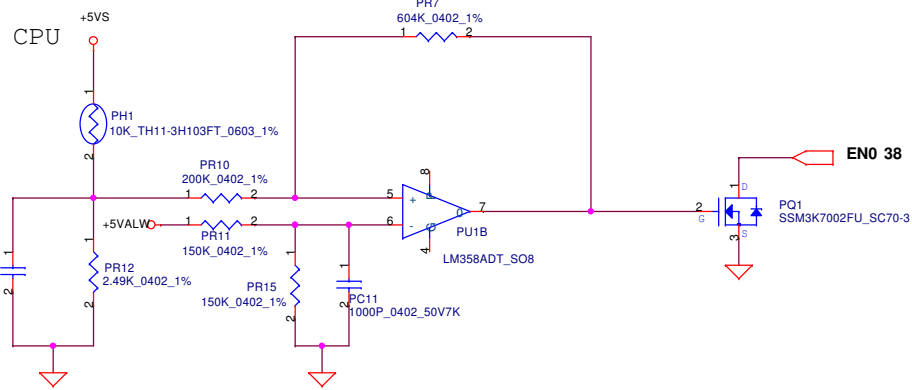




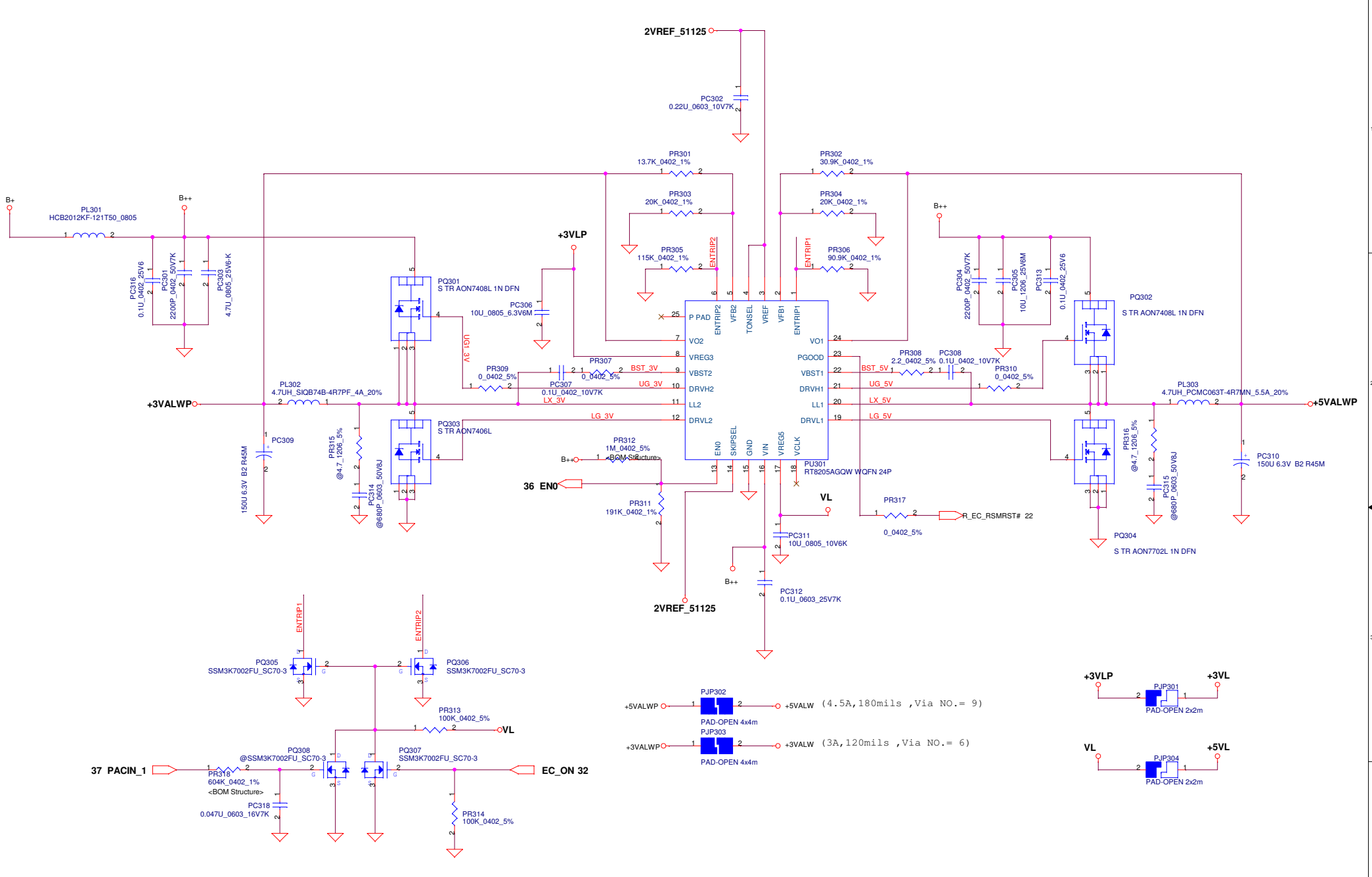
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Issued Date	2007/08/28	Deciphered Date	2006/07/26	DC/DC Interface	
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PH1 under CPU bottom side :
CPU thermal protection at 90 +/-3 degree C

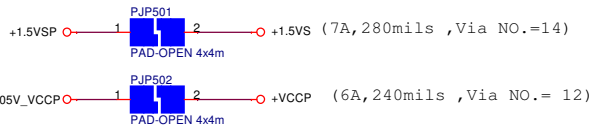
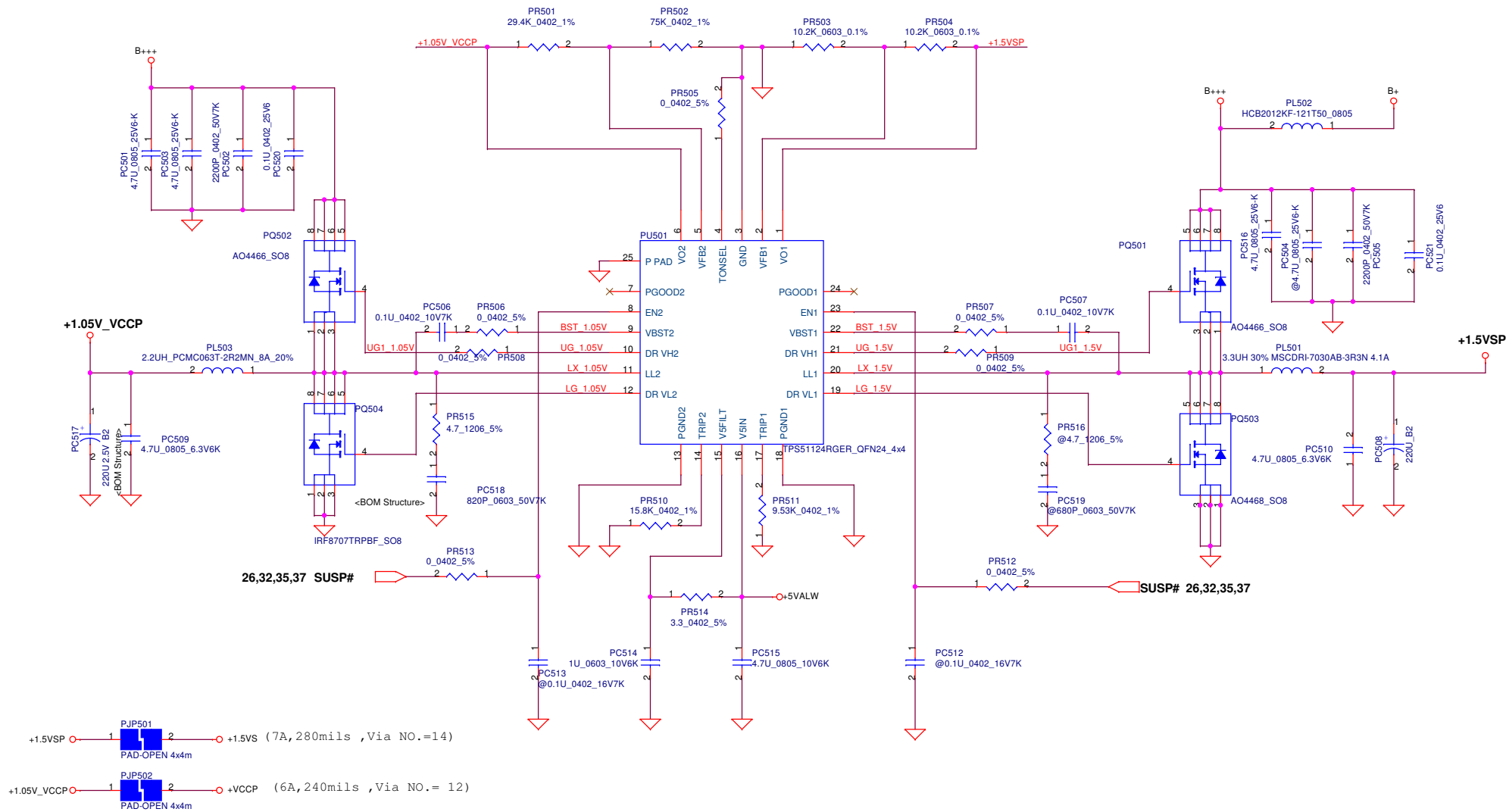


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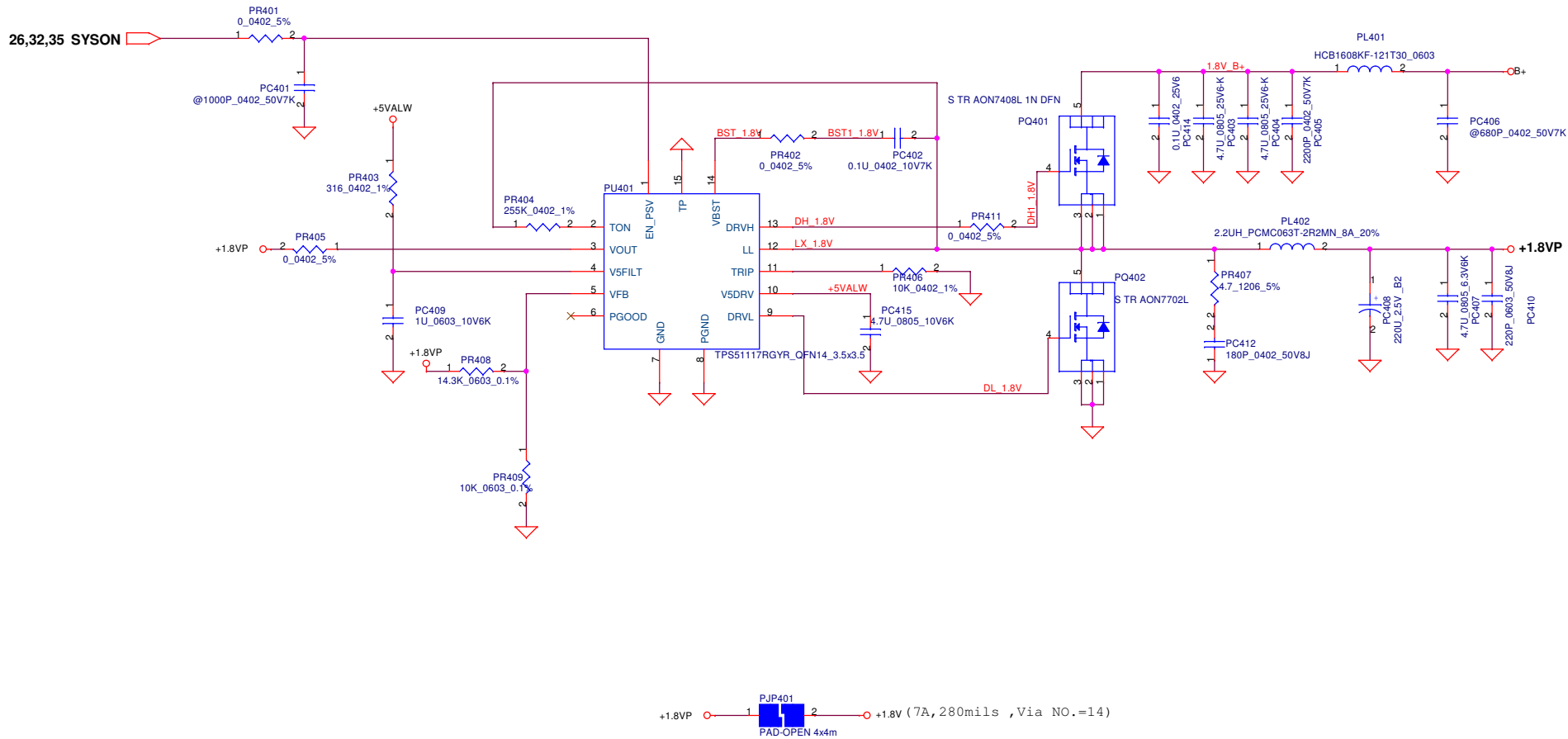
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3.3VALWP/5VALWP	
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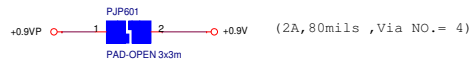
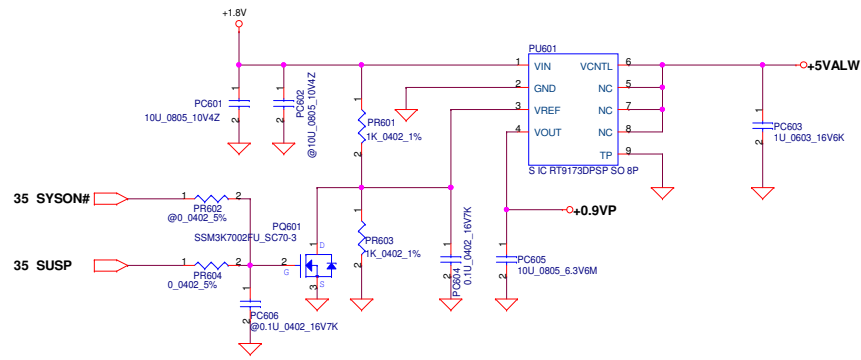
26,32,35,37 SUSP#

SUSP# 26,32,35,37

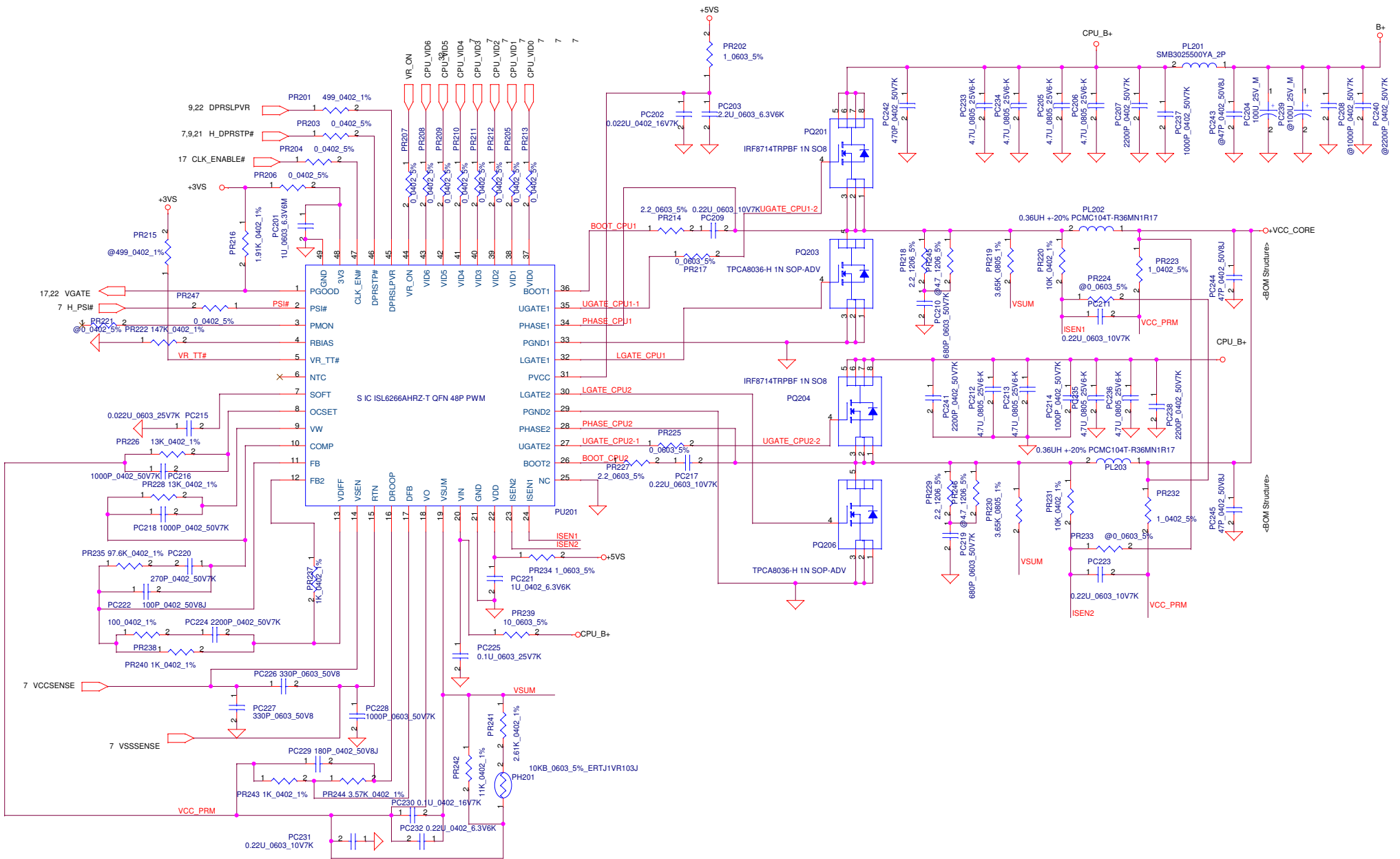
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Compal Electronics, Inc.
+CPU_CORE

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	CardReader clock issue	17	Using USB_0 for CLK_48M_CR	2008/10/08	SI-1
2	Debug Card issue	26	Connect PLT_RST# to JP7.A17	2008/10/08	SI-1
3	SMT issue	29	Change IR1 to SCR00000E00	2008/10/08	SI-1
4	Add Audio board	29	Add JAUDIO for audio board	2008/10/08	SI-1
5	SW2 is for DB1 debug	33	Delete SW2	2008/10/08	SI-1
6	Cap board issue	33	Change Cap board power rail to +3VL	2008/10/08	SI-1
7	Support GM47	13	Add C1503 for GM47	2008/10/08	SI-1
8	Change FAN control circuit to voltage control	6	Add U51,D63	2008/10/08	SI-1
9	Delete HDA SSC	21	Remove U8 for layout spacing	2008/10/08	SI-1
10	For PR mini card connector	26	Add R1225 -- R1236	2008/10/08	SI-1
11	PA/PR CardReader LED	27	D54 for PA, D64 for PR	2008/10/08	SI-1
12	EMI request	28	Change R1132 to bead	2008/10/08	SI-1
13	Use audio board	29	Add audio board connector, change NIC to 2pin and add SPK connector	2008/10/08	SI-1
14	Change JFPR to 6 pin connector	30	Add Q109, C1518, R1210	2008/10/08	SI-1
15	EMI request	35	Add C1512 -- C1517	2008/10/08	SI-1
16	Change JFPR to 4 pin connector	30	Delete Q109, C1518, R1210	2008/11/21	SI-R
17	Delete resistor for Debug card	26	Delete R1220-R1224	2008/11/21	SI-R
18	EMI request	35	Delete C1516,C1517 and connect to GND	2008/11/21	SI-R
19	For Intel DPST	19	Add R1237,R1238	2008/11/25	SI-R
20	EMI and WWAN request	17 28	Install C217, C218, C219, C435, C312, C316, C66, C67, C1478, C1479, C1480, C1481, D58, C1516, R1239, C327	2008/12/18	PV-1
21	Audio board connector	29	Change pin define	2008/12/18	PV-1
22	ST and Parade level shift	34	Add R for Parade	2008/12/18	PV-1
23	ESD request	33	Add C1518,D65,D66,D67	2008/1/19	MV-1
24	ESD/ EMI request	18 38 32	C217-C219, D5-D7, D45-D47, D20, C792-C815 no stuff	2008/2/13	MV-1
25	AUDIO issue	29	C1446, C1447 change to 0805 size	2008/2/13	MV-1
26	PC Beep issue	28	change to analog GND and add separate diode	2008/2/13	MV-1
27					
28					

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Item	Fixed Issue	(Reason for change)	PAGE	Modify List	Date	Phase
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Issued Date	2007/08/28	Deciphered Date	2006/07/26	PIR 2	
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