

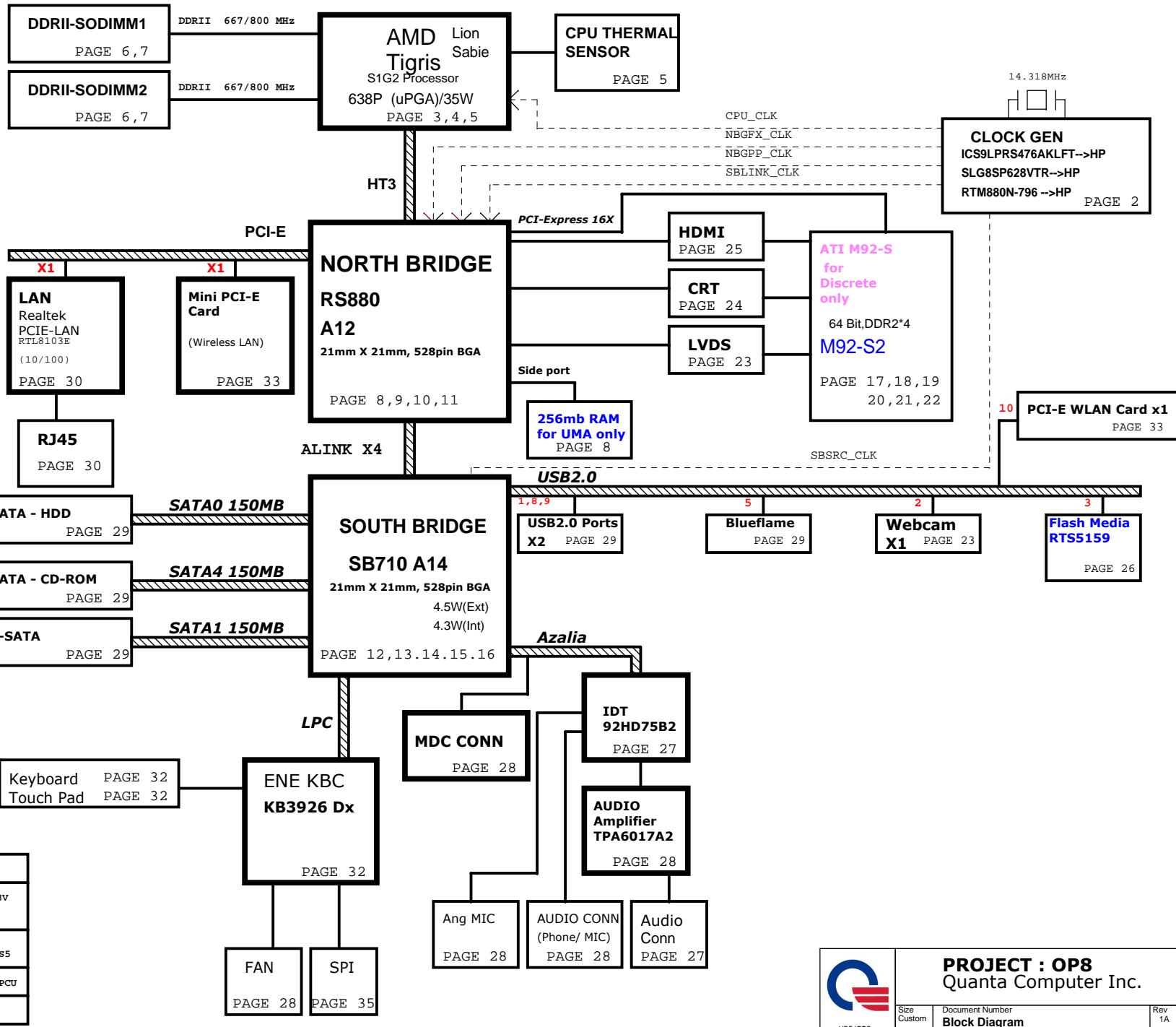
# OP8 SYSTEM DIAGRAM



01

## PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : IN1
- LAYER 3 : IN2
- LAYER 4 : VCC
- LAYER 5 : IN3
- LAYER 6 : BOT

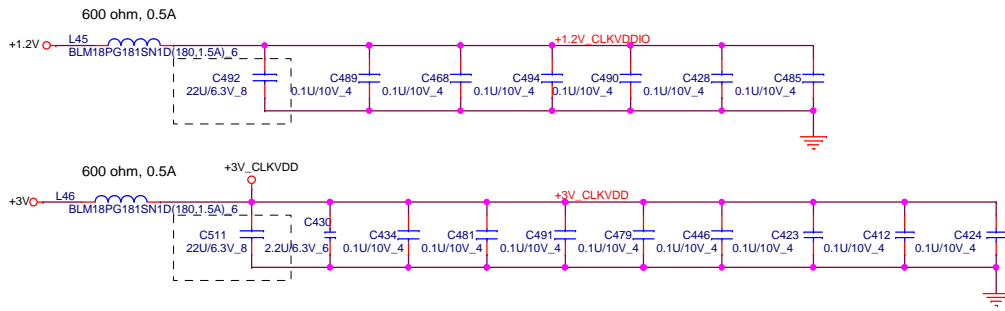


- SYSTEM CHARGER (ISL6251) PAGE 40
- SYSTEM POWER ISL6237 PAGE 34
- DDR II SMD DR\_VTERM 1.8V/1.8VSUS (RT8207) PAGE 37
- VCCP +1.1V AND +1.2V (RT8204) PAGE 35
- VGACORE (1.1V-1.2V) Oz8118 PAGE 38
- CPU CORE ISL6265HRTZ-T PAGE 36

SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card	
	Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

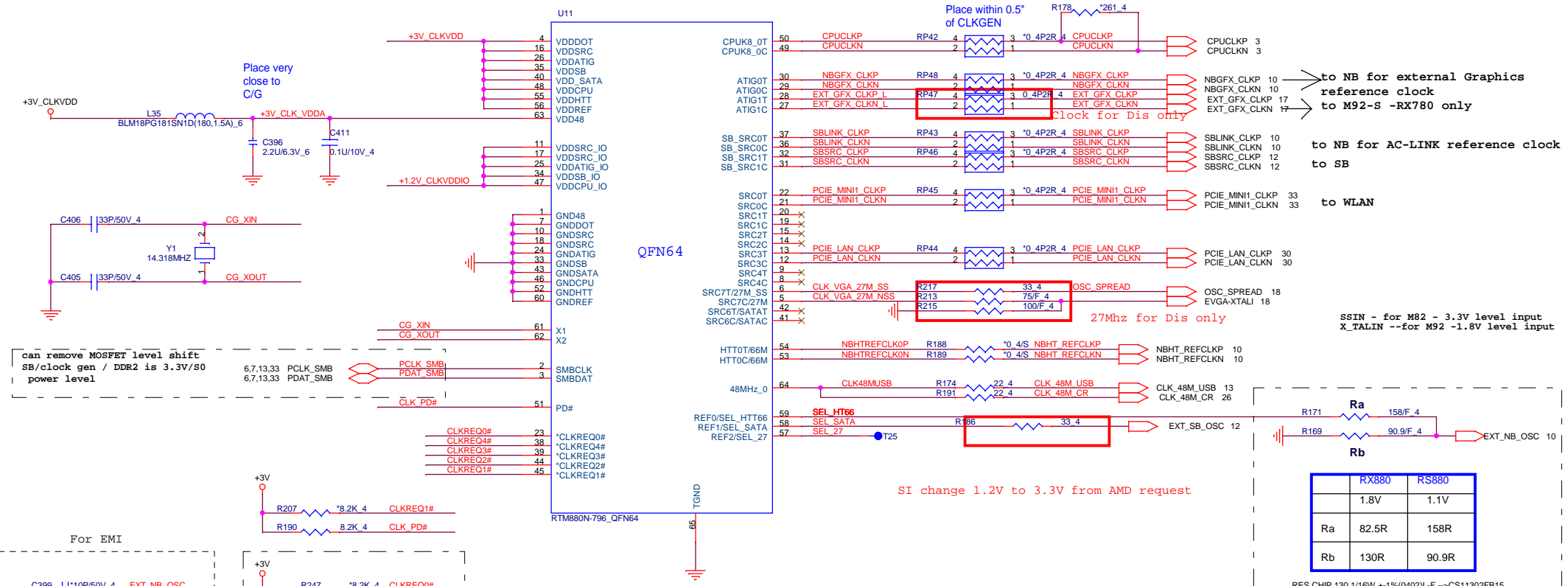
**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
<b>Block Diagram</b>		
Date: Friday, March 20, 2009		Sheet 1 of 42



CLOCKS name	RX780	RS780	Clock pin function
NBGF_X_CLKP NBGF_X_CLKN	RP48 STUFF	RP48 STUFF	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP47 STUFF	RP47 NC	to M92-S external reference clock -RX780 only
SBLINK_CLKP SBLINK_CLKN	RP43 STUFF	RP43 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R213, R215 STUFF	R213, R215 NC	To M92-S 27Mhz - RX780 only

Need check the net name for the short pad



can remove MOSFET level shift  
SB/clock gen / DDR2 is 3.3V/S0  
power level

For EMI

if use clock request pin, need to pull Hi for default setting

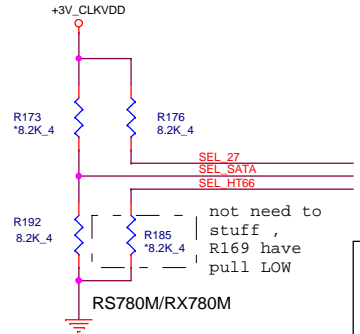
SLG8SP628VTR--AL8SP628000  
RTM880N-796-- AL000880001

* default	
SEL_HT66	1 0*
SEL_SATA	1 0*
SEL_27	1*

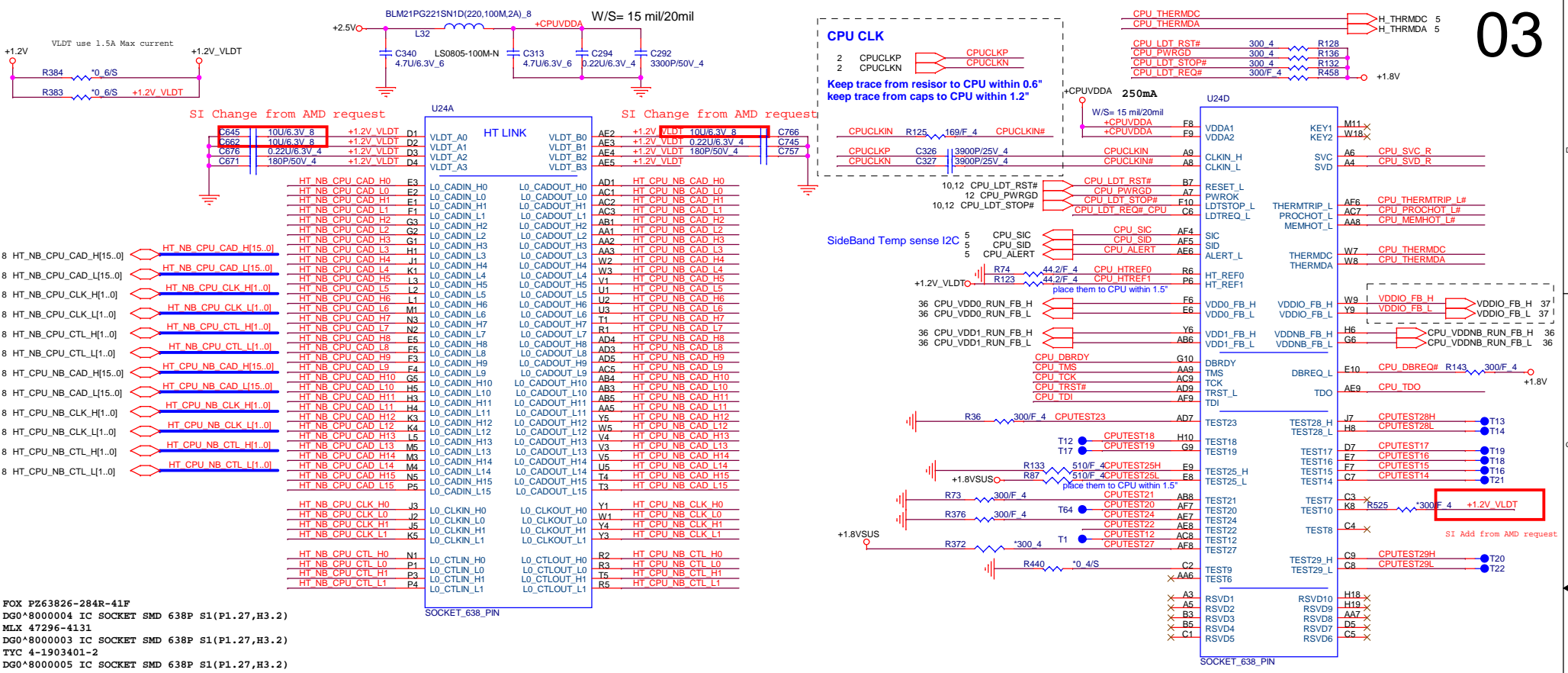
1	66 MHz 3.3V single ended HTT clock
0*	100 MHz differential HTT clock
1	100 MHz non-spreading differential SRC clock
0*	100 MHz spreading differential SRC clock
1*	27MHz non-spreading singled clock
0	100 MHz spreading differential SRC clock

	RX880	RS880
	1.8V	1.1V
Ra	82.5R	158R
Rb	130R	90.9R

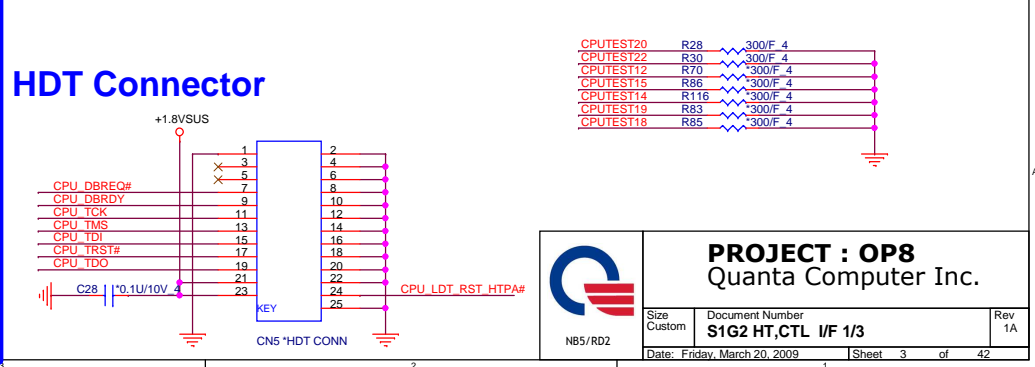
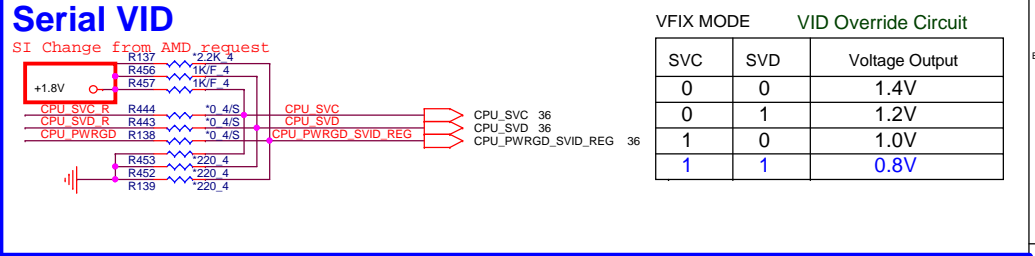
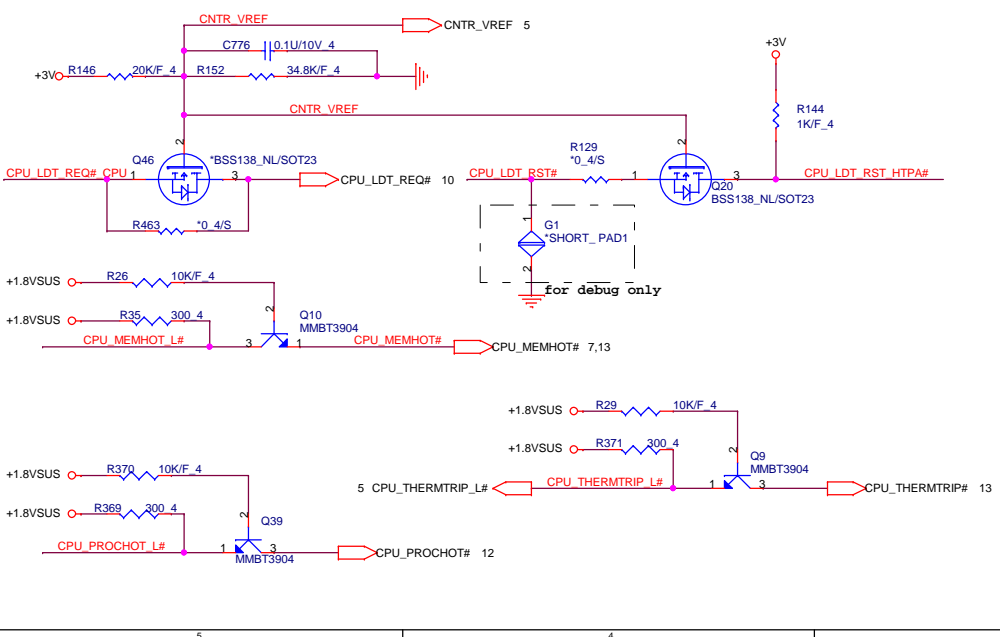
RES CHIP 130 1/16W +-1%(0402)L-F -->CS11302FB15  
RES CHIP 158 1/16W +-1%(0402) -->CS11582FB00  
RES CHIP 90.9 1/16W +-1%(0402) -->CS09092FB15  
RES CHIP 82.5 1/16W +-1%(0402) -->CS08252FB11



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

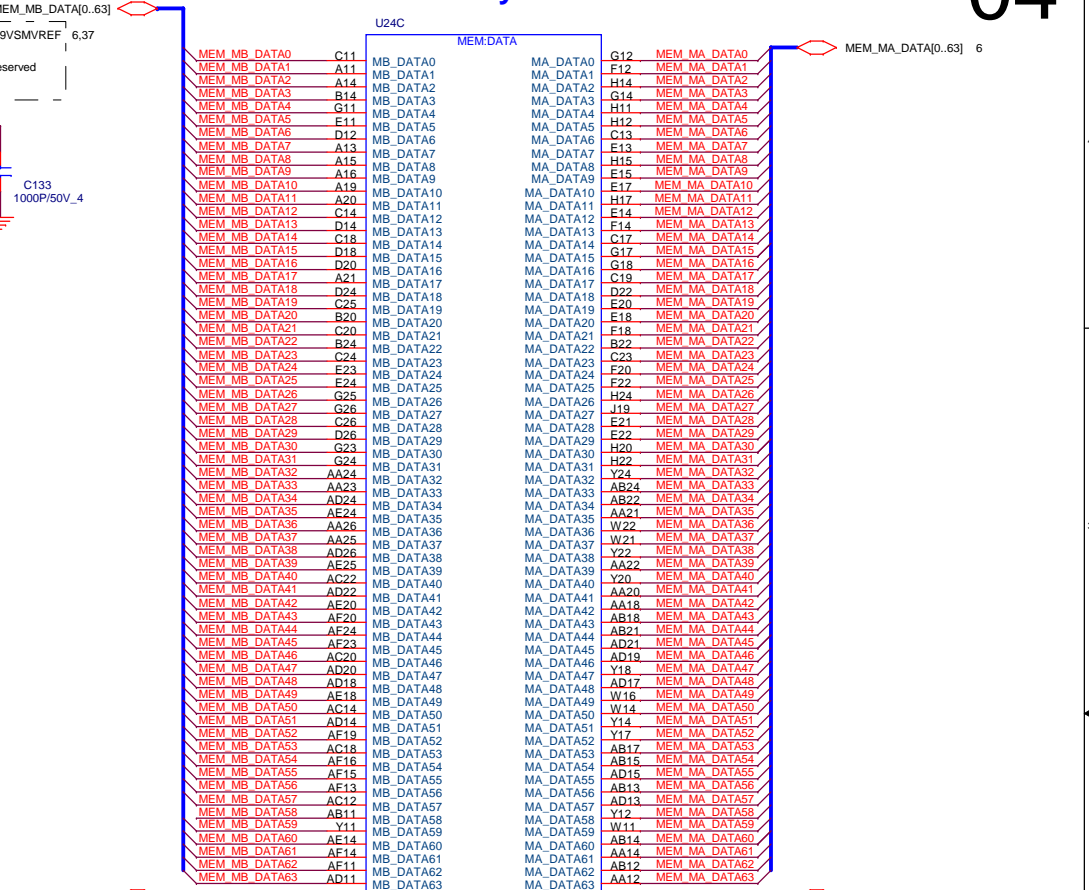
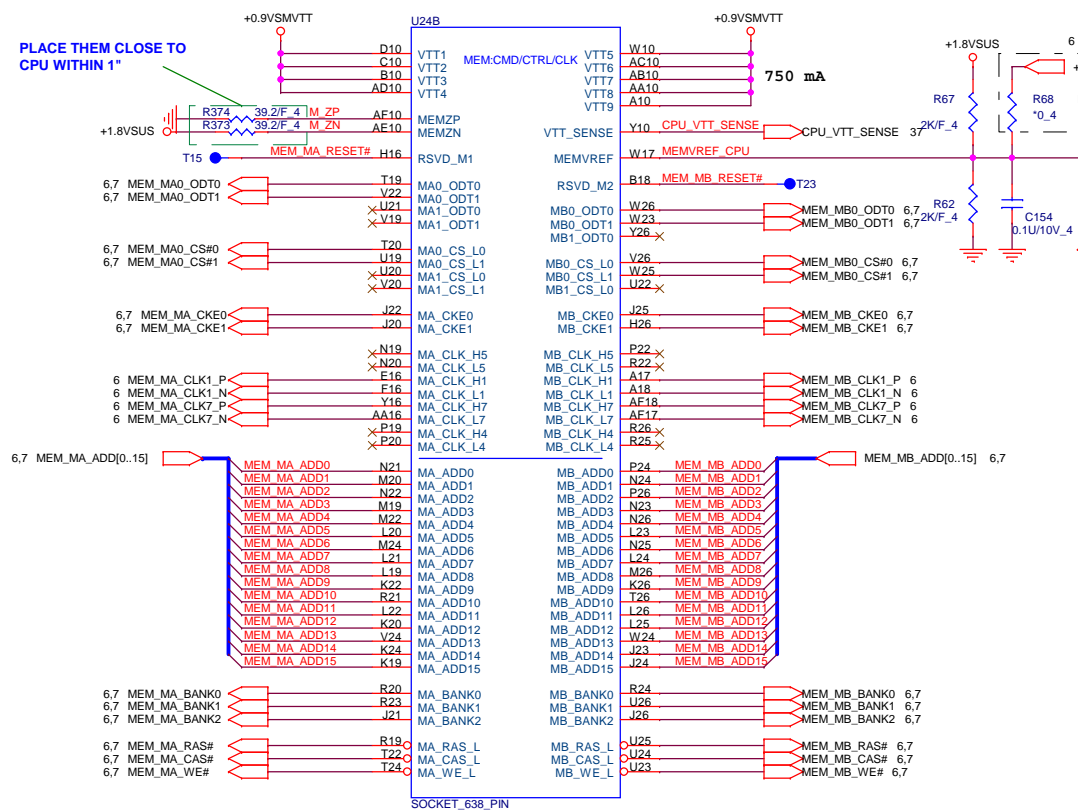


FOX PZ63826-284R-41F  
 DG0\*8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)  
 MLX 47296-4131  
 DG0\*8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)  
 TYC 4-1903401-2  
 DG0\*8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)

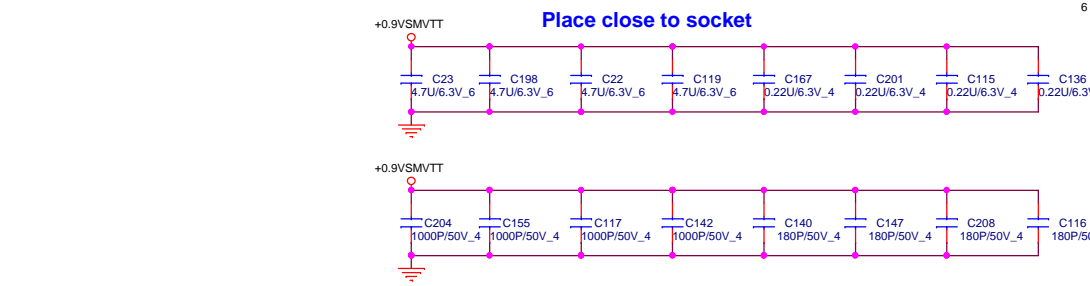


# Processor Memory Interface

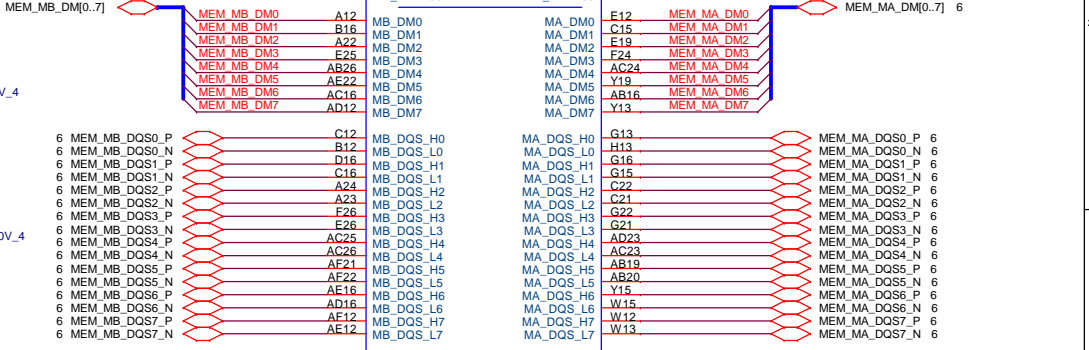
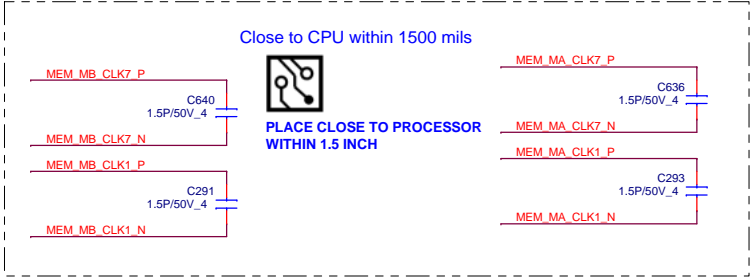
PLACE THEM CLOSE TO CPU WITHIN 1"



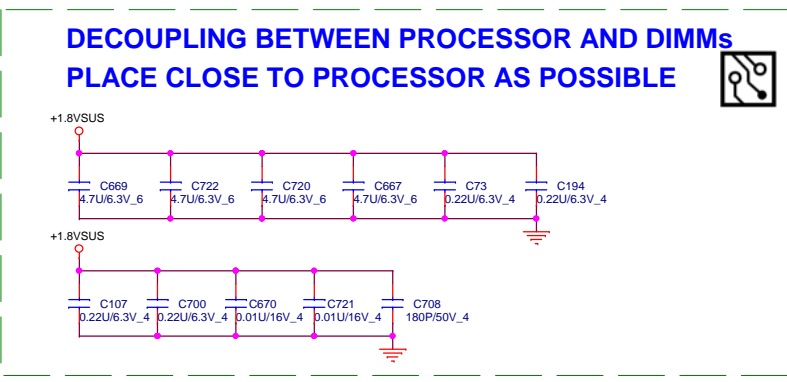
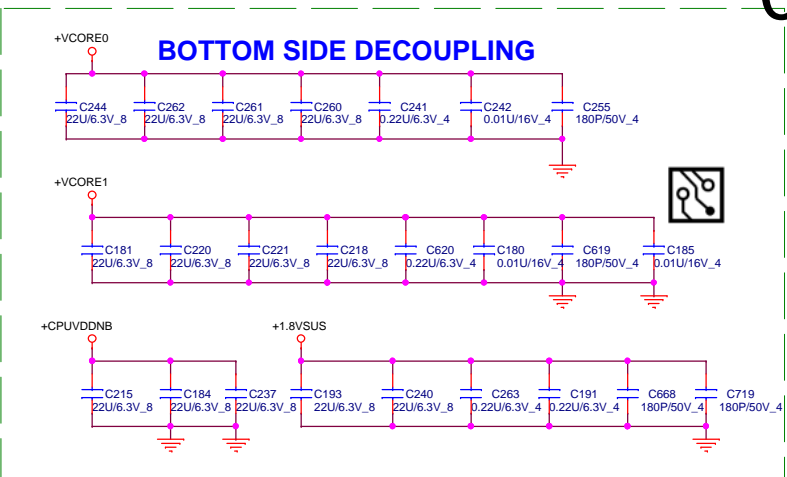
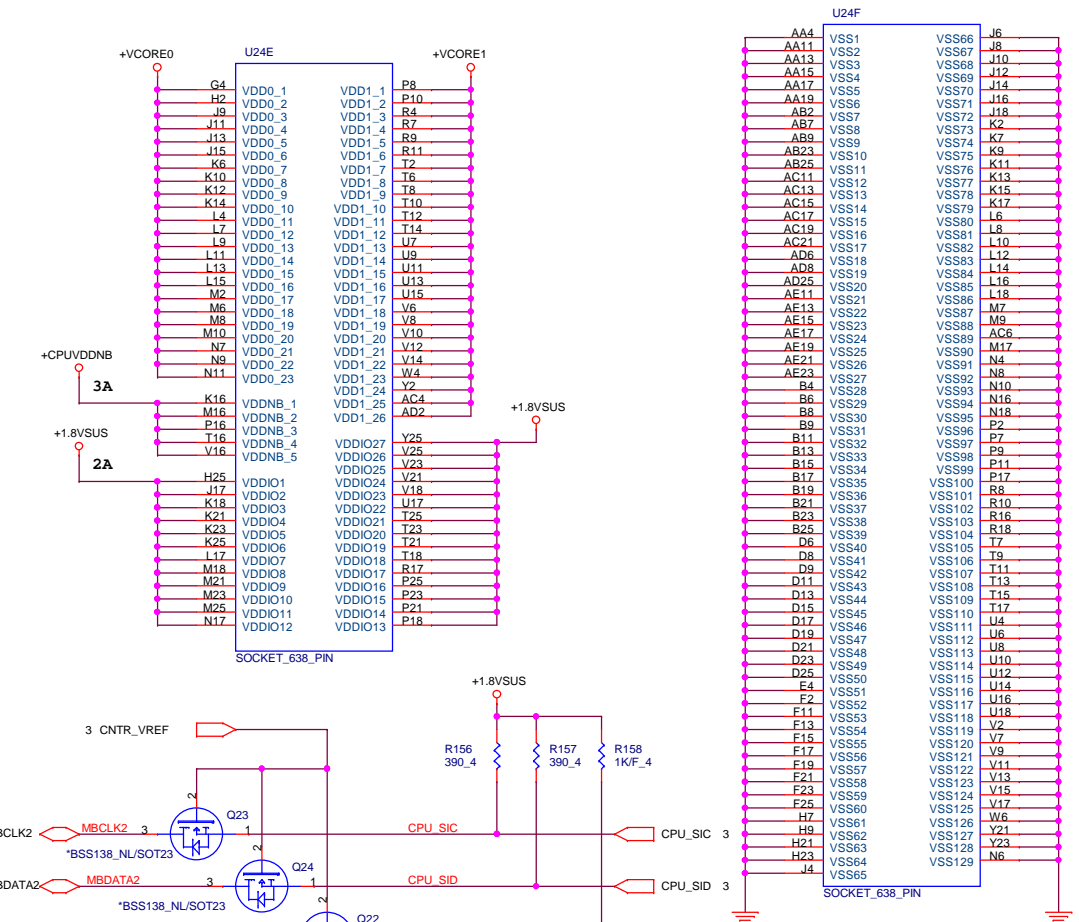
Place close to socket



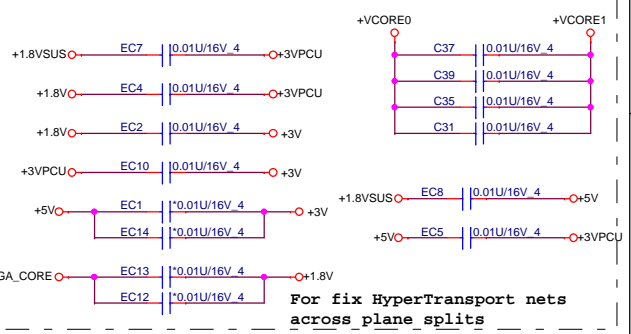
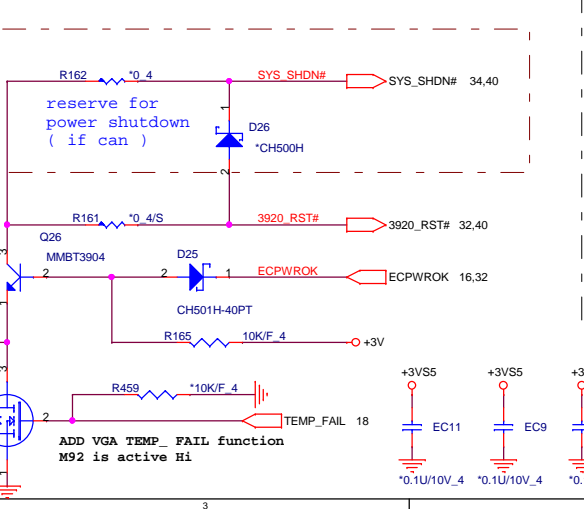
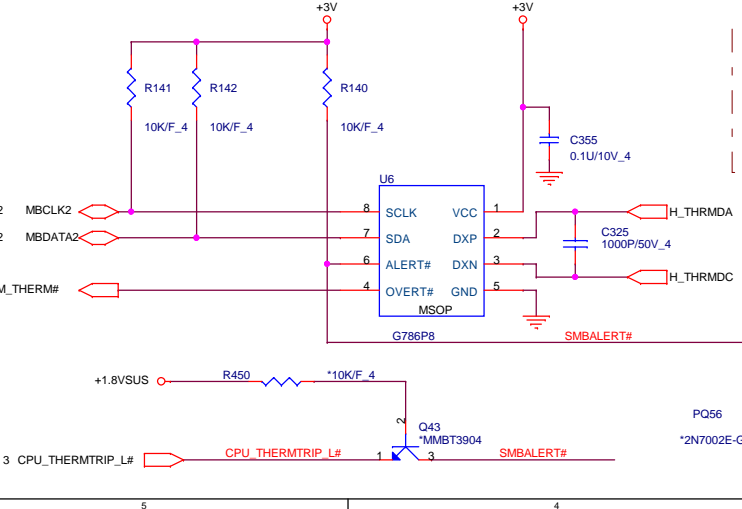
Close to CPU within 1500 mils



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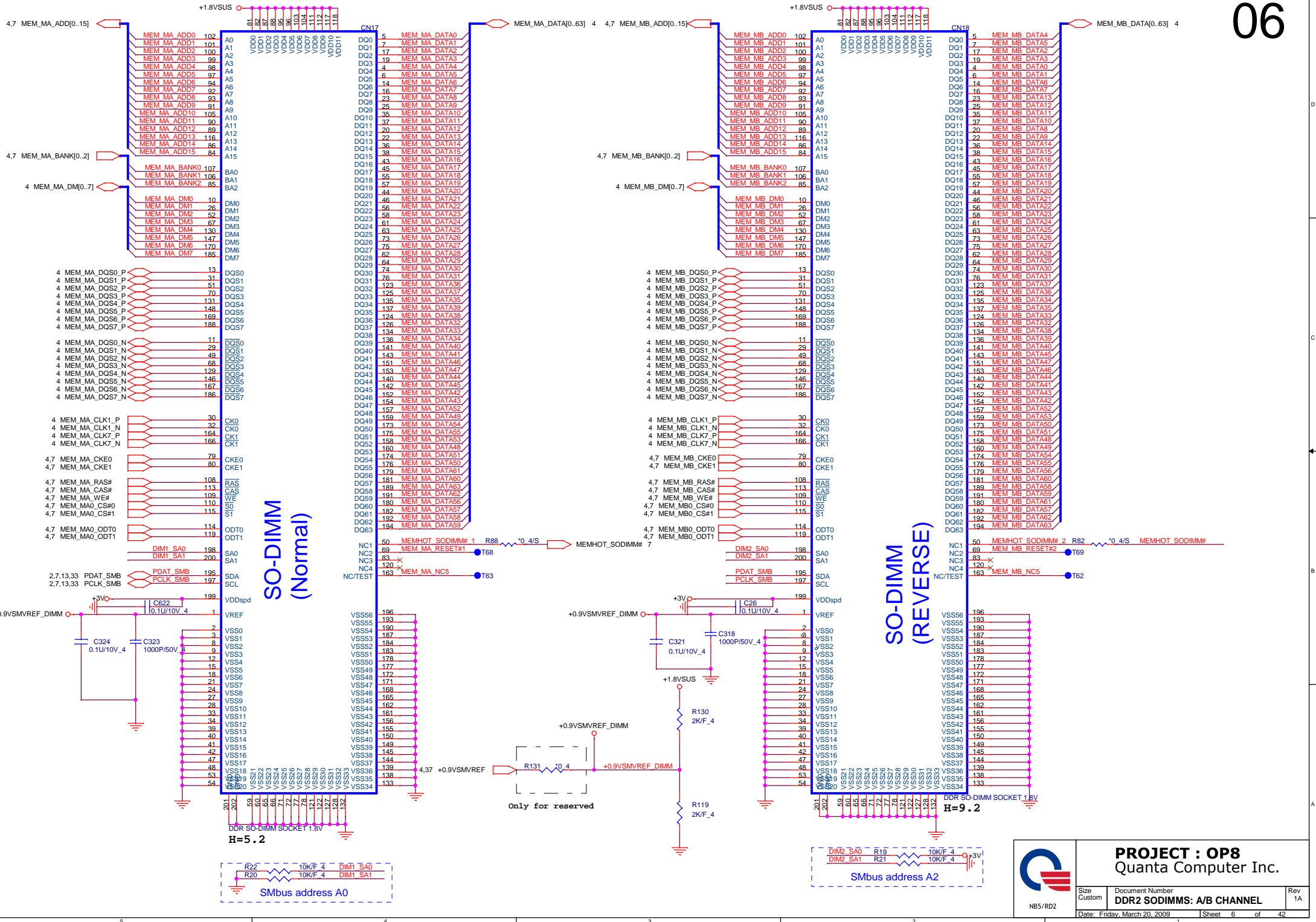
# PROCESSOR POWER AND GROUND



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Quanta Computer Inc.

Size Custom    Document Number **S1G2 PWR & GND 3/3**    Rev 1A

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**PROJECT : OP8**  
**Quanta Computer Inc.**

Size Custom Document Number **DDR2 SODIMMS: A/B CHANNEL** Rev 1A  
 Date: Friday, March 20, 2009 Sheet 6 of 42

NB5/RD2



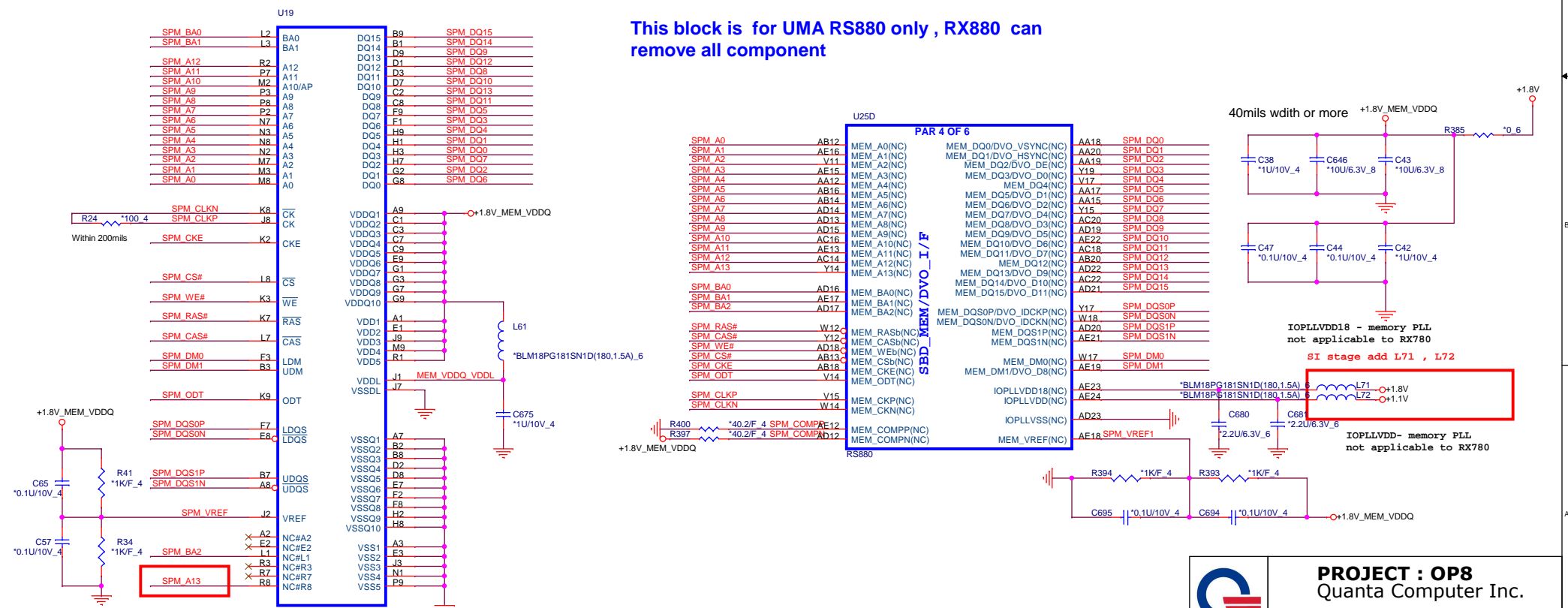


signals	RS880	RX880
HT_TXCALP	R430 301 ohm 1%	R430 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R434 301 ohm 1%	R434 1.21k ohm 1%
HT_RXCALN		

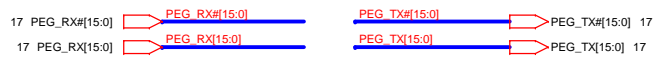
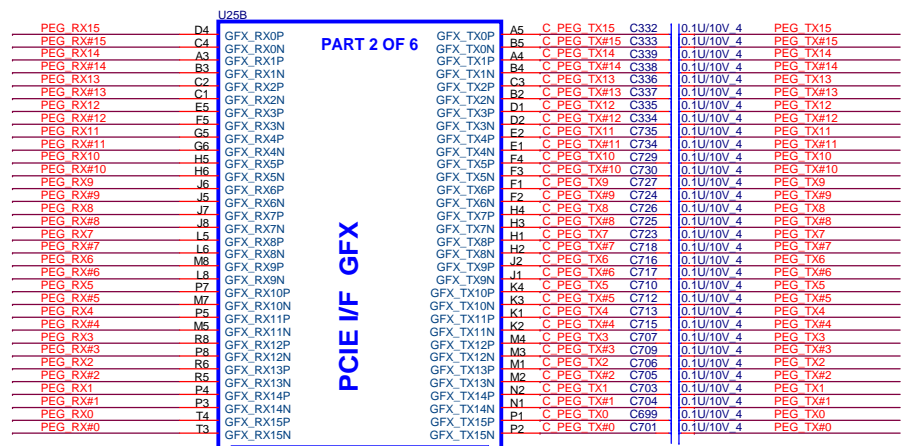
RES CHIP 1.21K 1/16W +-1%(0402)  
P/N : CS21212FB18

RES CHIP 301 1/16W +-1%(0402)  
P/N : CS13012FB14

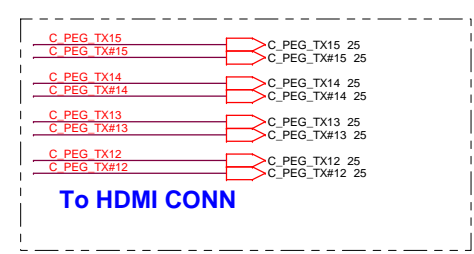
**This block is for UMA RS880 only , RX880 can remove all component**



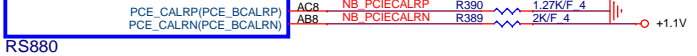
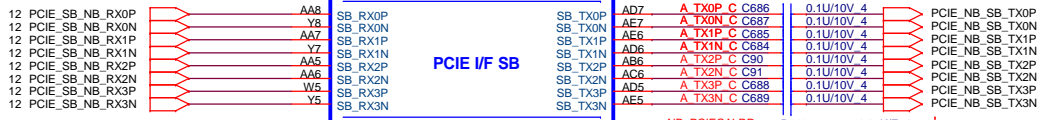




Close to North Bridge



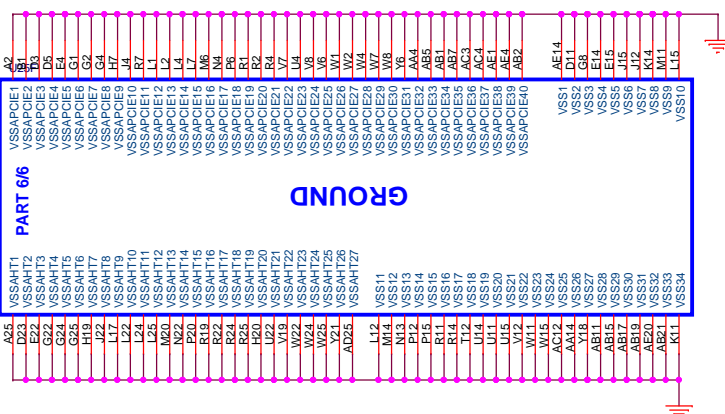
TO WLAN  
TO PCIE-LAN



RS880 Display Port Support (muxed on GFX)

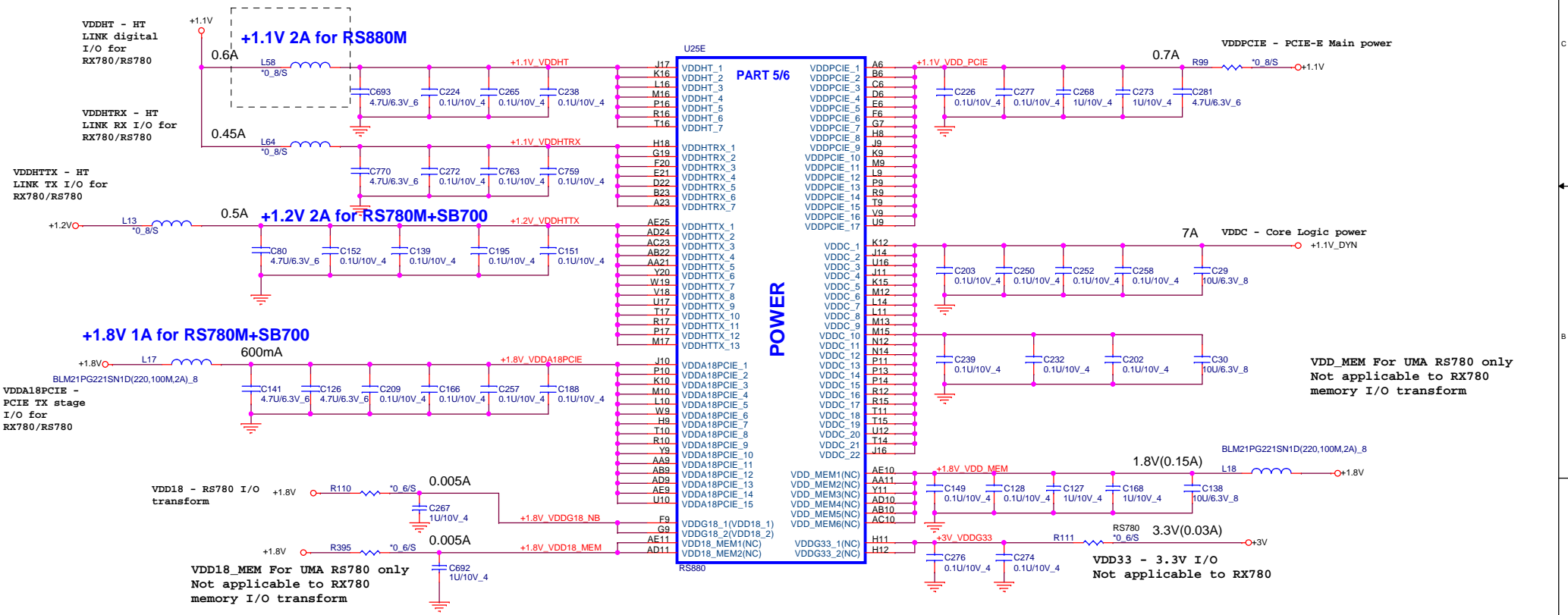
DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1





**RX780/RS780 POWER DIFFERENCE TABLE**

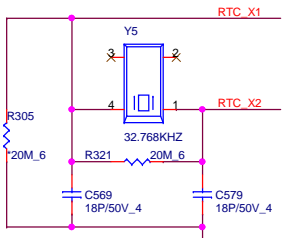
PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDL18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDL33	NC	NC



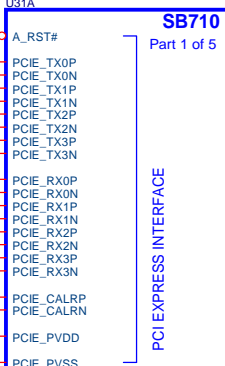
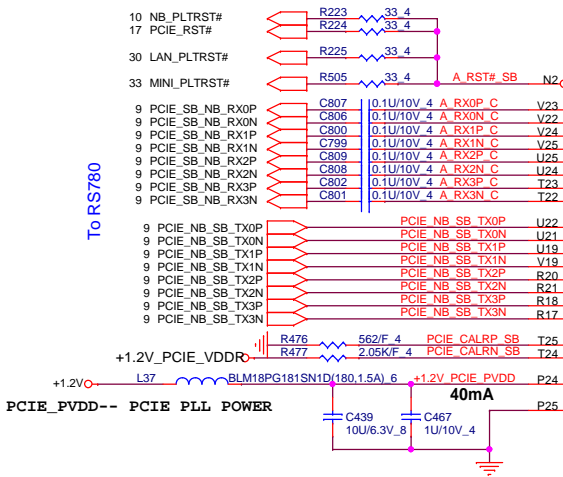
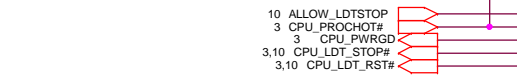
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PLACE THESE  
PCIE AC  
COUPLING CAPS  
CLOSE TO U600

To RS780

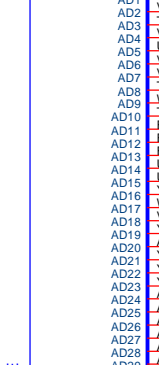


Change for SB710 chip  
FOR A14 chip

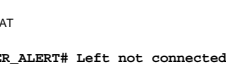
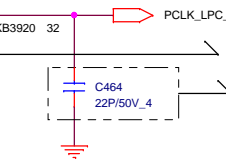
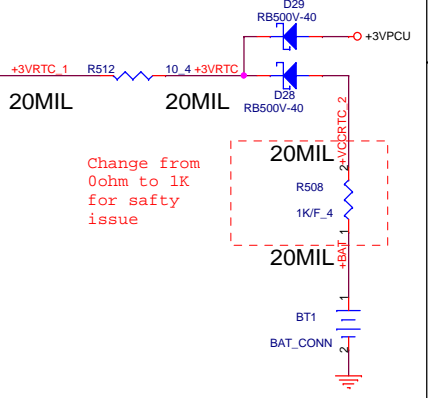
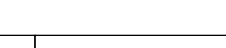
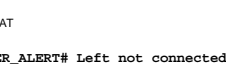
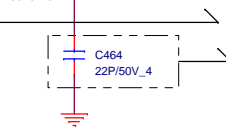
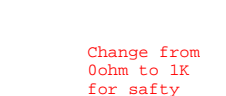
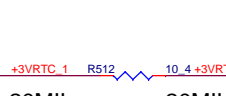
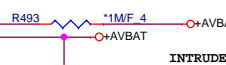
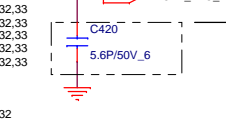
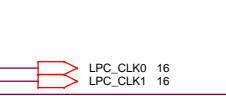
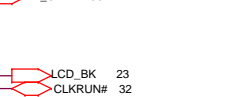
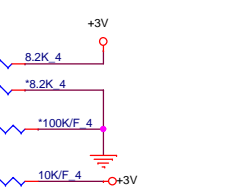
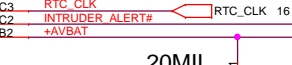
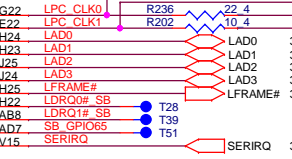
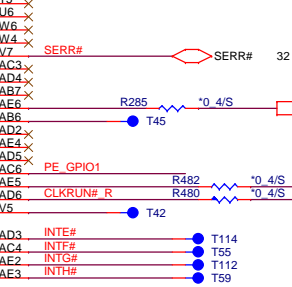


SB710  
IC CTRL(528P) SB710 A14(218-0660017)  
P/N : AJ066000T01

SB710  
Part 1 of 5



All the PCI bus has  
build-in Pull-UP/Down  
resistors



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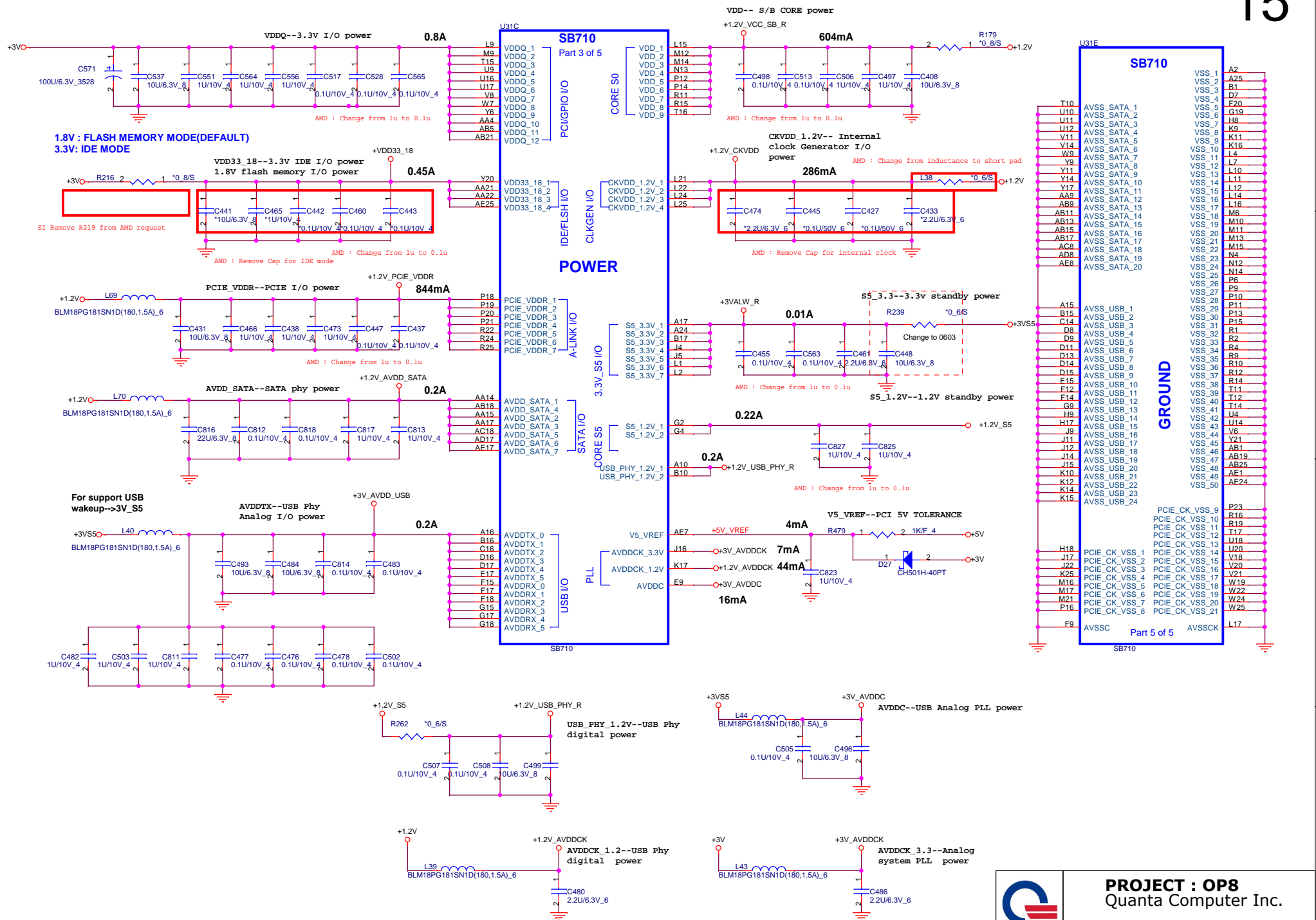
Size Custom	Document Number <b>SB700-PCIE/PCI/CPU/LPC 1/4</b>	Rev 1A
Date: Friday, March 20, 2009		Sheet 12 of 42

NB5/RD2





PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



**PROJECT : OP8**  
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Size Custom	Document Number <b>SB700-PWR/DECOUPLING 4/4</b>	Rev 1A
Date: Friday, March 20, 2009		Sheet 15 of 42

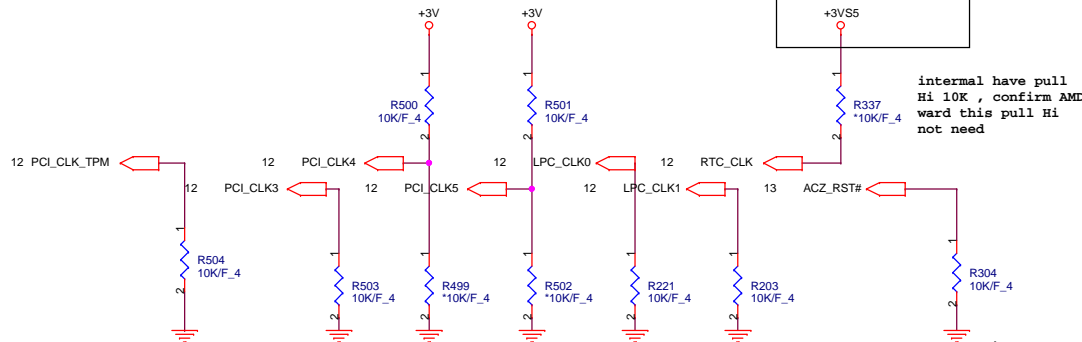
NB5/RD2



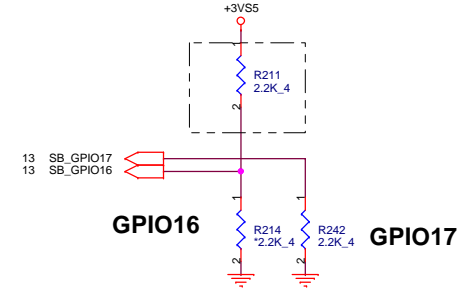
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

It must ready refore RSMRST#

### REQUIRED STRAPS



internal have pull Hi 10K , confirm AMD ward this pull Hi not need

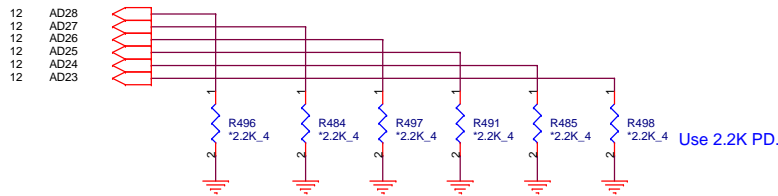


TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
<b>PULL HIGH</b>	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
<b>PULL LOW</b>	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT

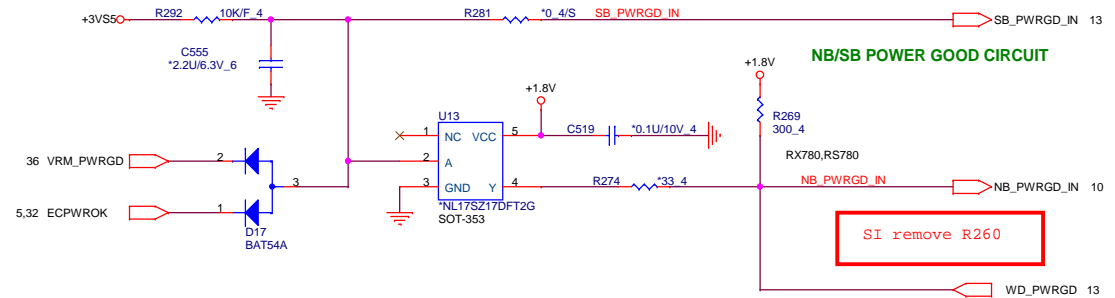
### DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
<b>PULL LOW</b>	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB\_PWRGD\_IN: RS780/RX780 = 1.8V; RS740 = 3.3V Do NOT share it with SB\_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353  
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

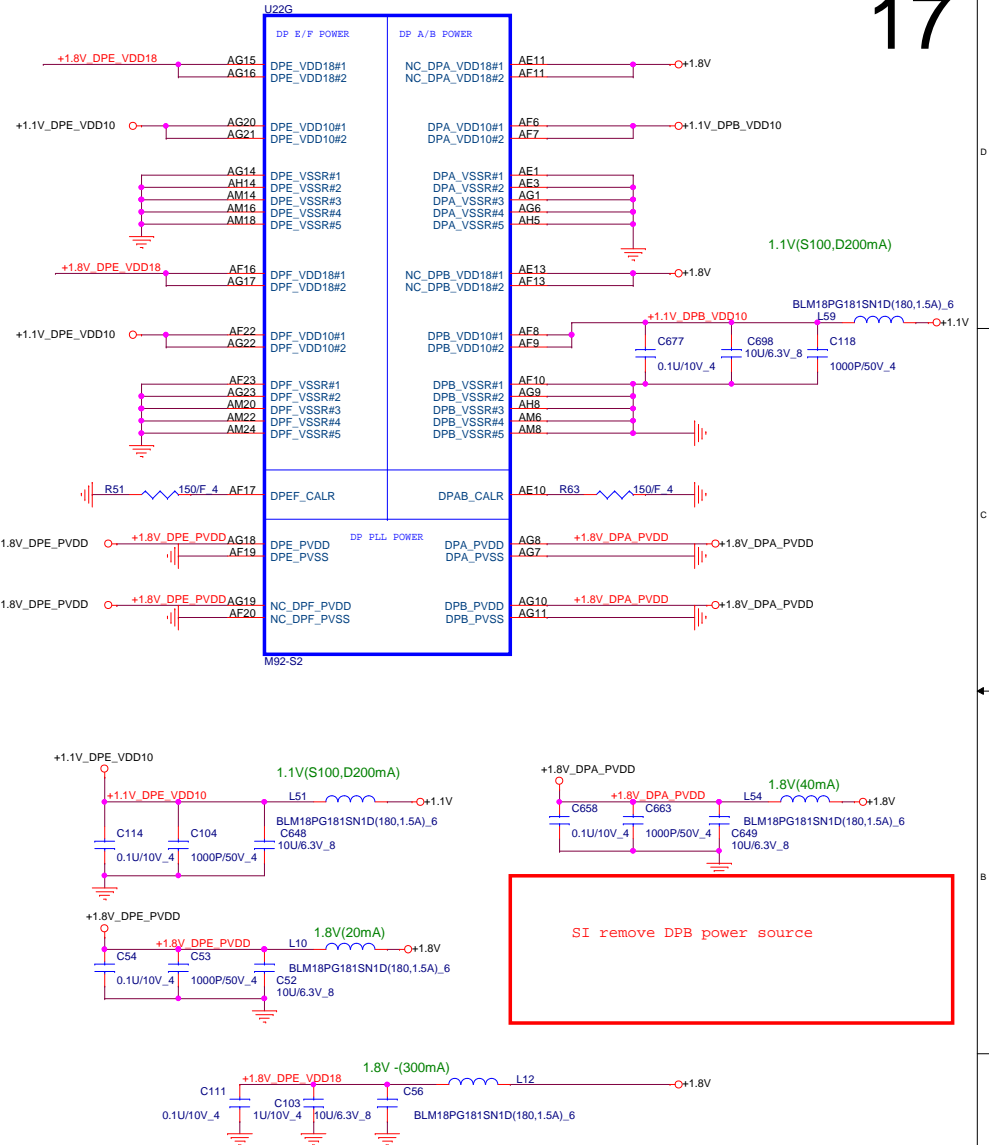
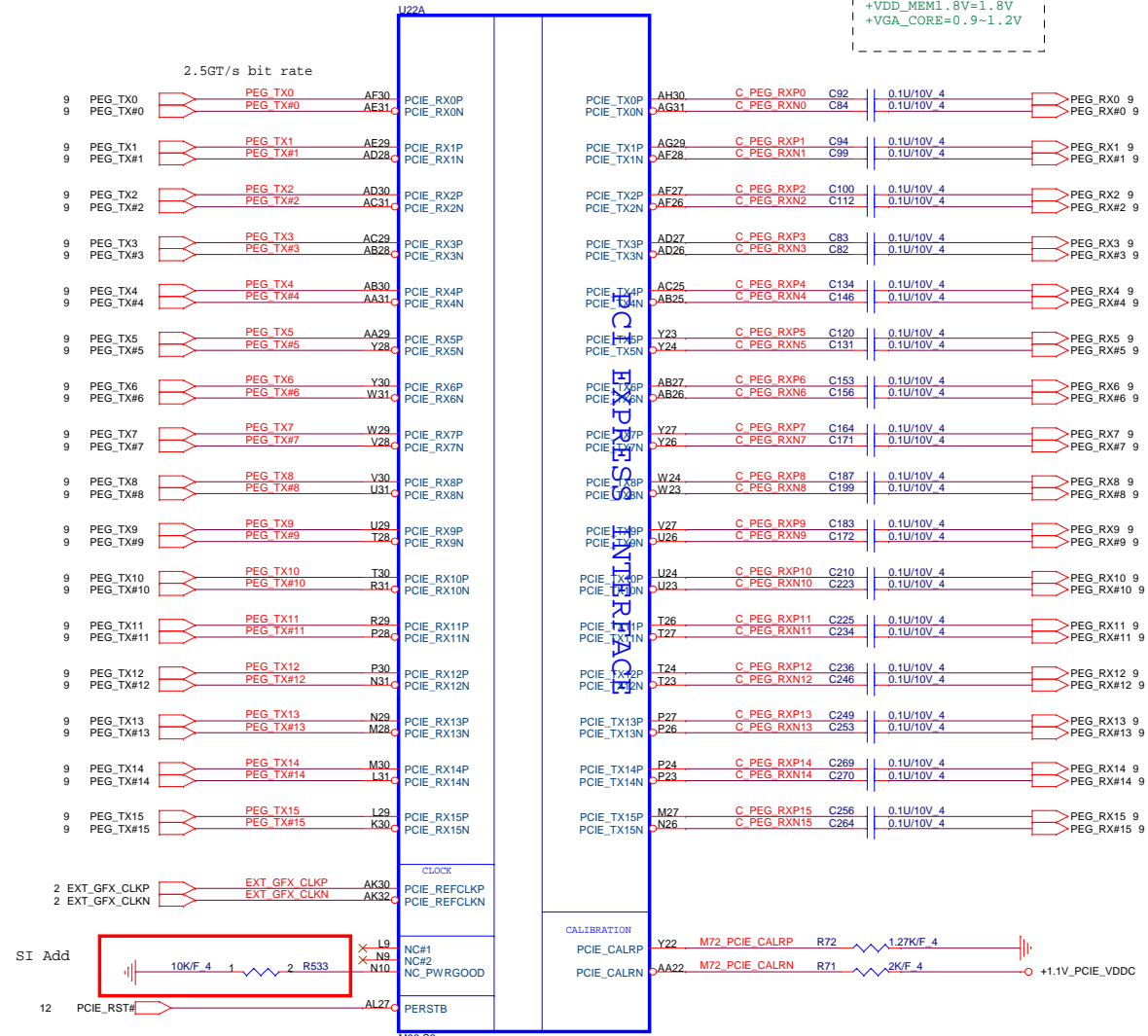


PROJECT : OP8  
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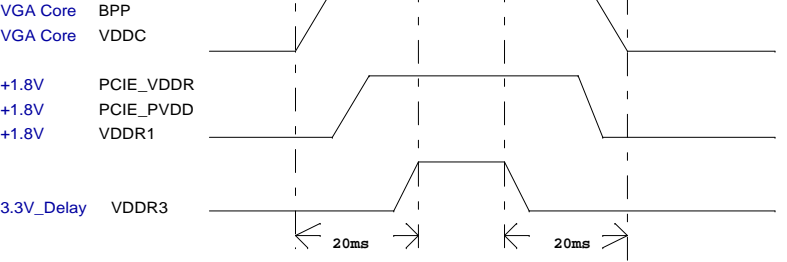
Size Custom Document Number SB700-STRAPS Rev 1A  
Date: Friday, March 20, 2009 Sheet 16 of 42



POWER  
+PCIE\_VDDR=1.2V  
+VDD\_MEM1.8V=1.8V  
+VGA\_CORE=0.9-1.2V



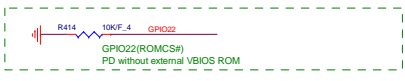
SI Add  
10K/F 4 1 R533  
1.00MHz (+/-300ppm) input frequency,  
0-0.7V single-ended swing



SI remove DPB power source

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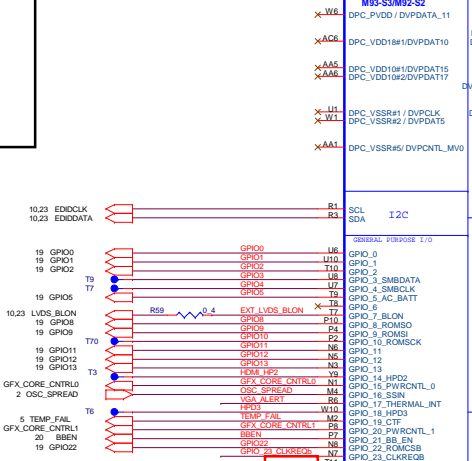
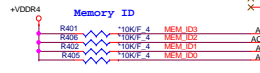
Size Custom	Document Number	Rev 1A
M7X/M8X_PCIE_Interface		
Date: Friday, March 20, 2009	Sheet 17 of 42	



MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hynix	4*16-500MHZ	HP510E13E7R-20L
0001	Samsung (E die)	4*16-500MHZ	K9NIG164QE-HC20
0010	Qimonda (Infineon)	4*16-500MHZ	TD
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		
1000	Reserved		
1001	Reserved		
1010	Reserved		
1011	Reserved		
1100	Reserved		
1101	Reserved		
1110	Reserved		
1111	Reserved		

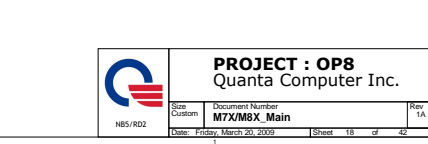
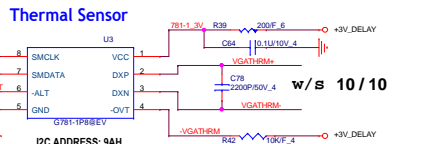
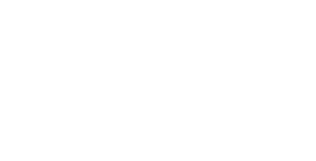
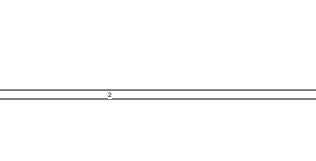
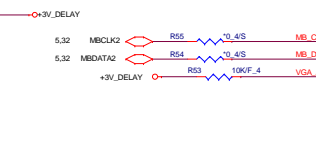
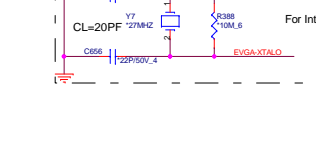
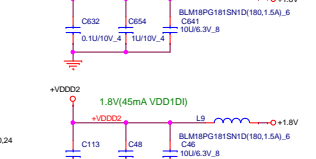
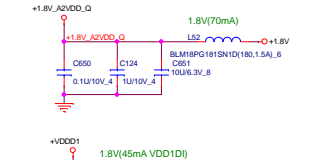
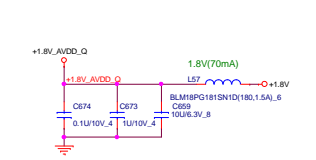
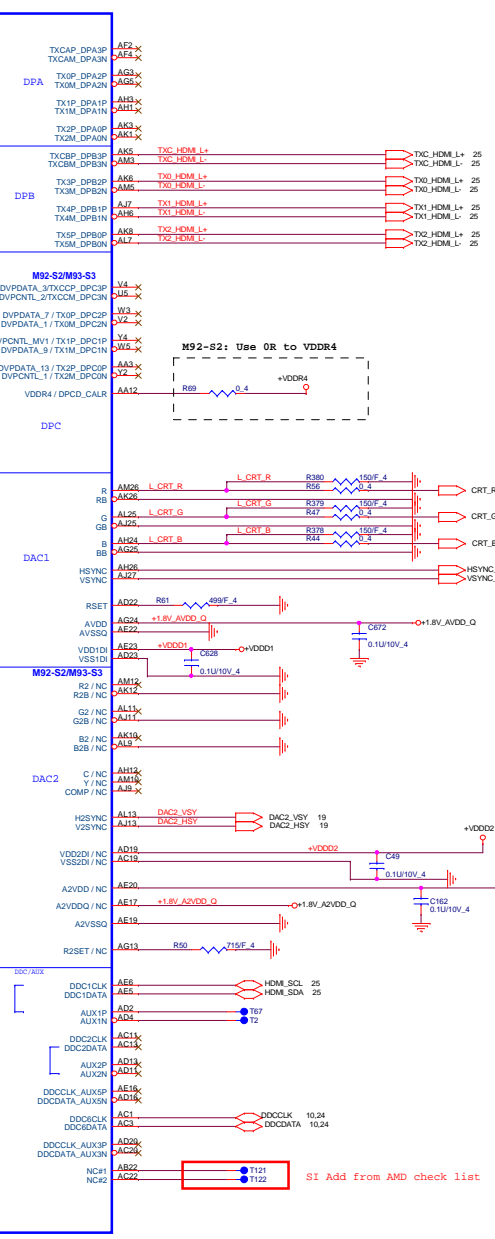
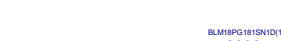
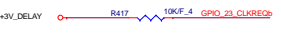
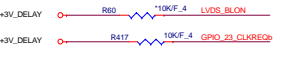
	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V

	BBEN	BBP
L	0	V-CORE
H	1	+1.8V



Need check again

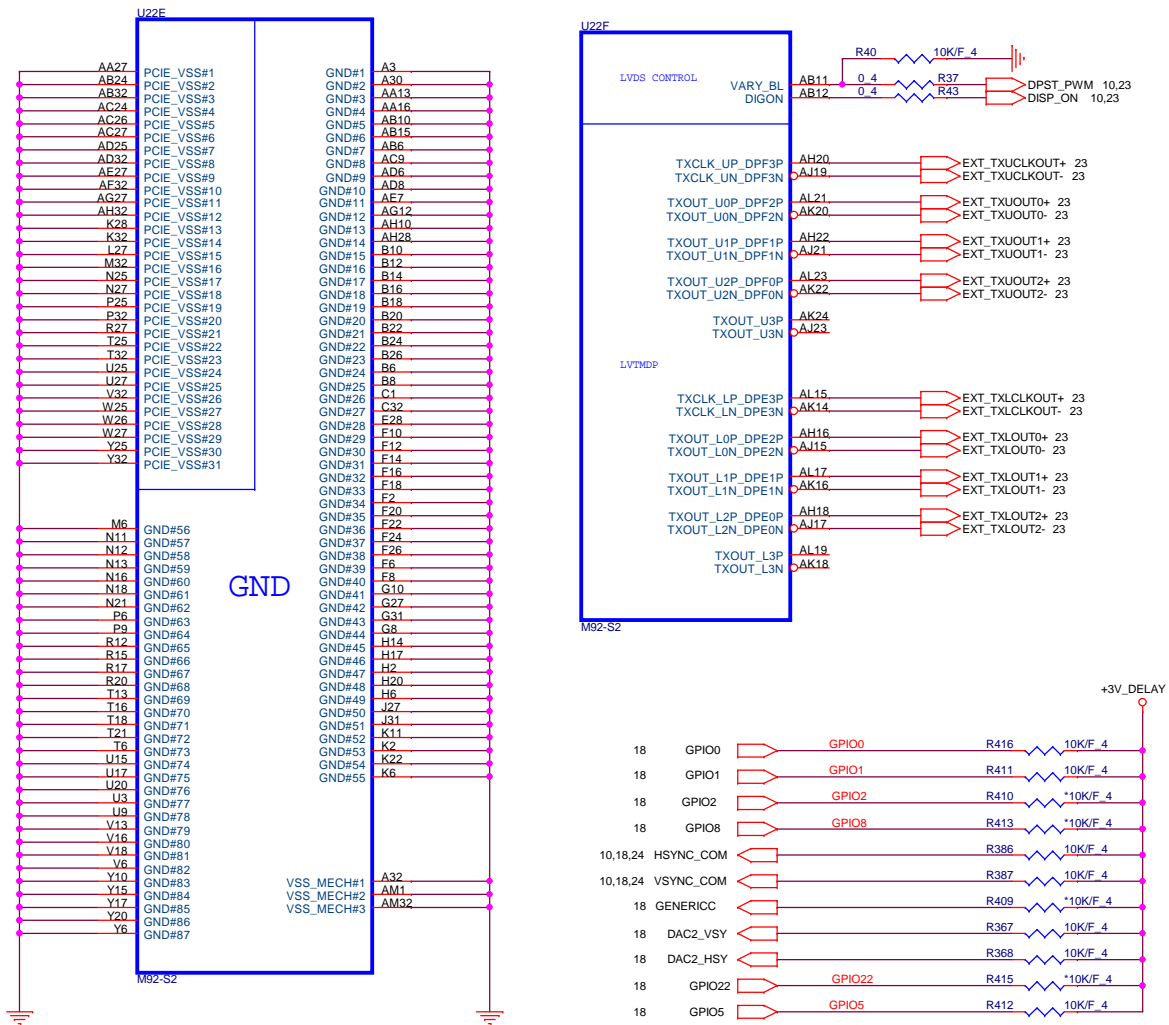
SI Add GND from Check list



**PROJECT : OP8**  
Quanta Computer Inc.

Site: Custom  
Document Number: **M7X/M8X\_Main**  
Date: Friday, March 20, 2009 Sheet 18 of 22

NBS/RD2 Rev 1A



Strap Name	Pin Straps description	Default Value	
TX_PWRS_ENB	GPIO0 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1	
TX_DEEMPH_EN	GPIO1 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1	
BIF_GEN2_EN	GPIO2 0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0	
STRAP_BIF_CLK_PM_EN	GPIO8 Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0	
BIOS_ROM_EN	GPIO22 Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0	
AUDIO[0]	VSYN	1	
AUD(1)	HSYN	HSYN - HDMI_EN HDMI connector presence. 0 ?No HDMI connector is present on PCB 1 - HDMI connector is present on the PCB HDMI	1
VIP_DEVICE_STRAP_DIS	DAC2_VSY	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
SMS_EN_HARD	DAC2_HSY		0
CCBYPASS	GENERIC		0

Memory Aperture size

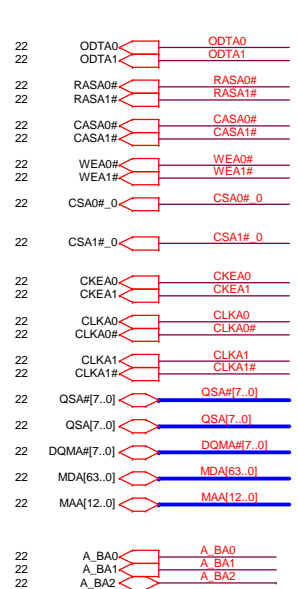
GPIO9		GPIO13	GPIO12	GPIO11
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS\_ROM\_EN is set to 0.

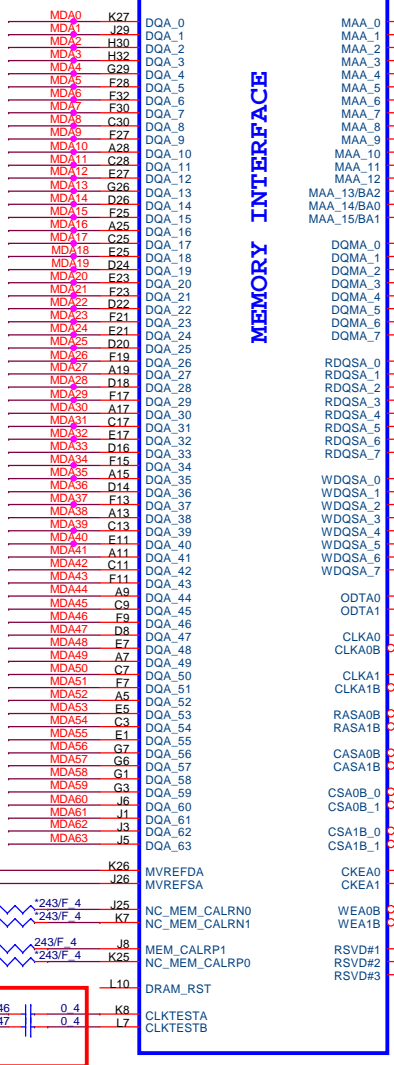


PROJECT : OP8  
Quanta Computer Inc.

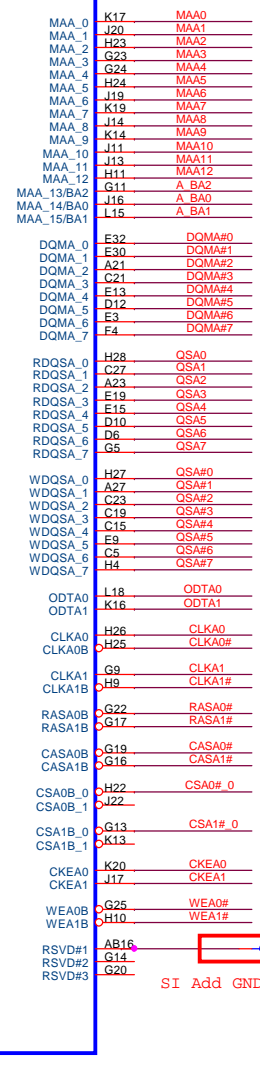




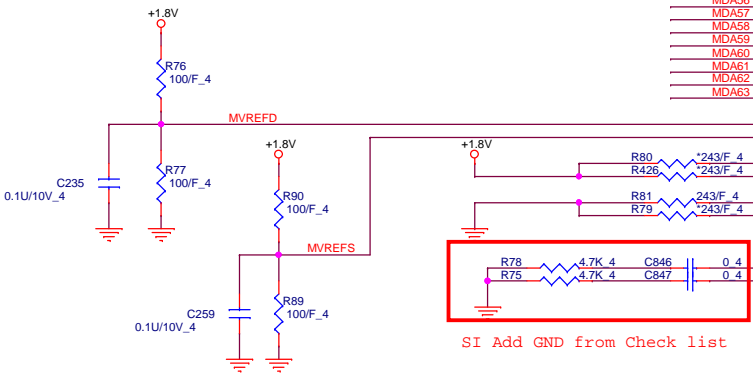
support 1Gbit  
VRAM ( 64M X 16 )



MEMORY INTERFACE



SI Add GND from Check list



SI Add GND from Check list

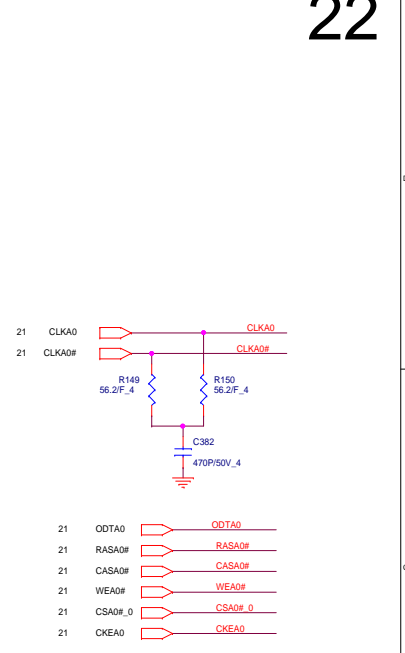
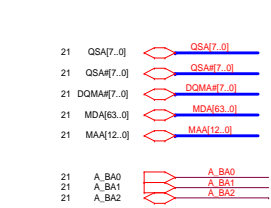
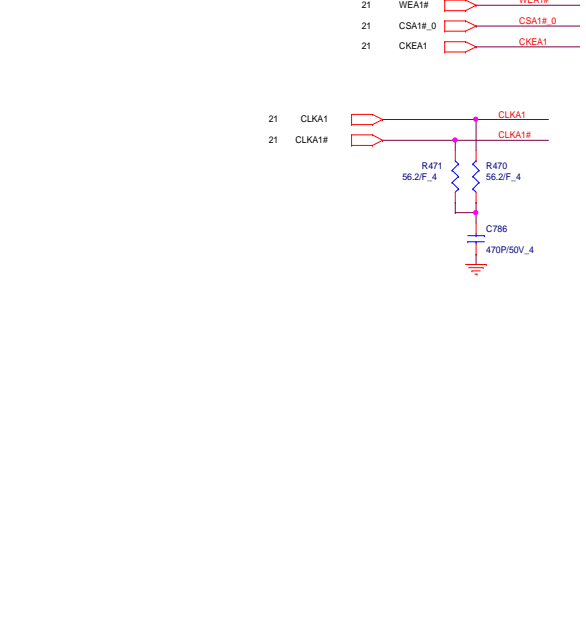
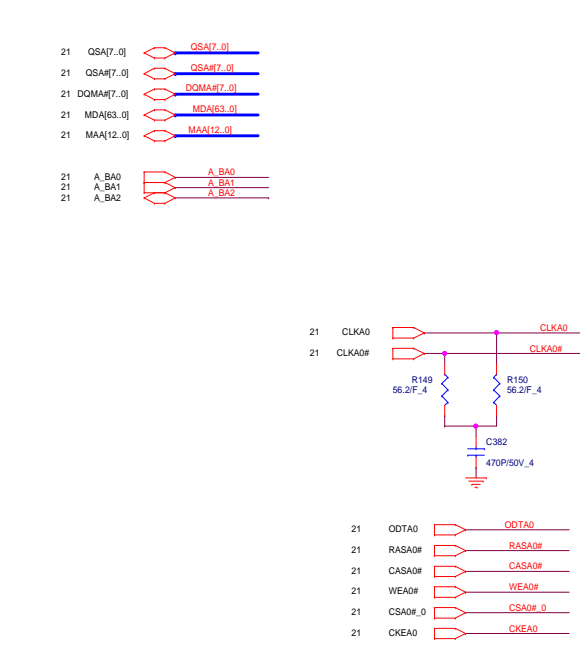
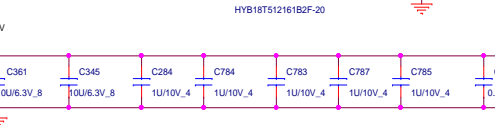
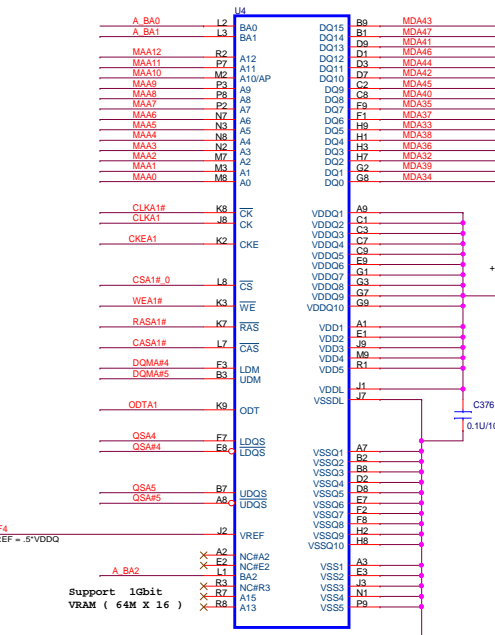
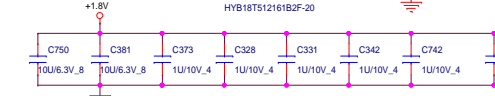
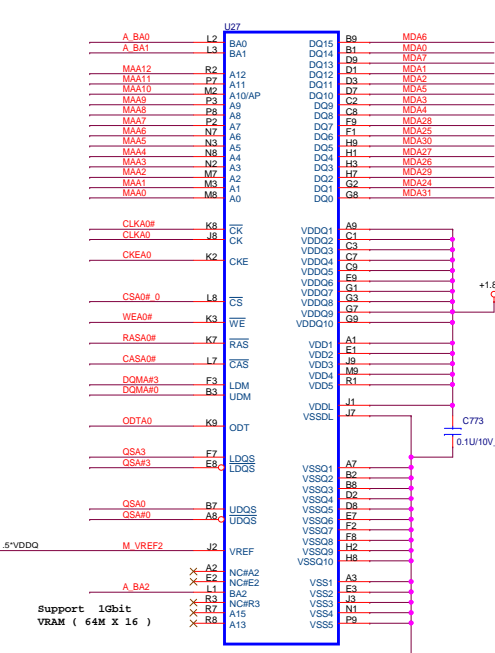
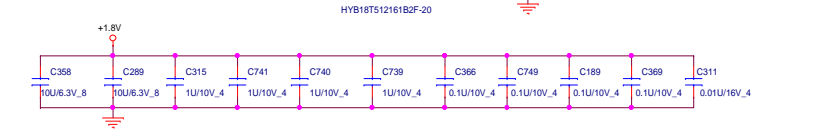
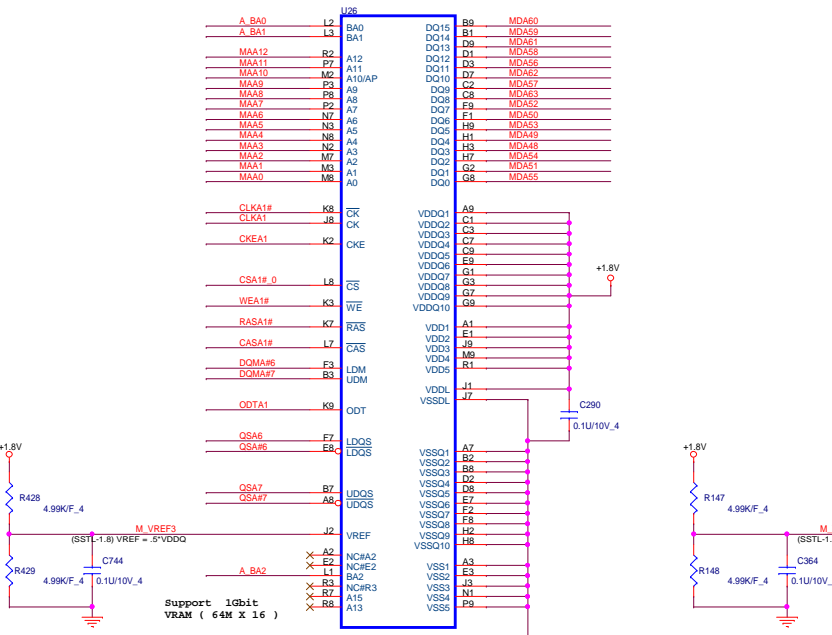
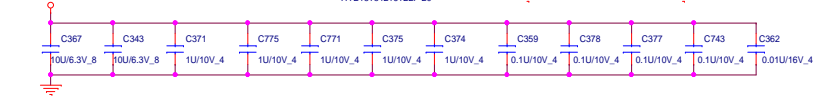
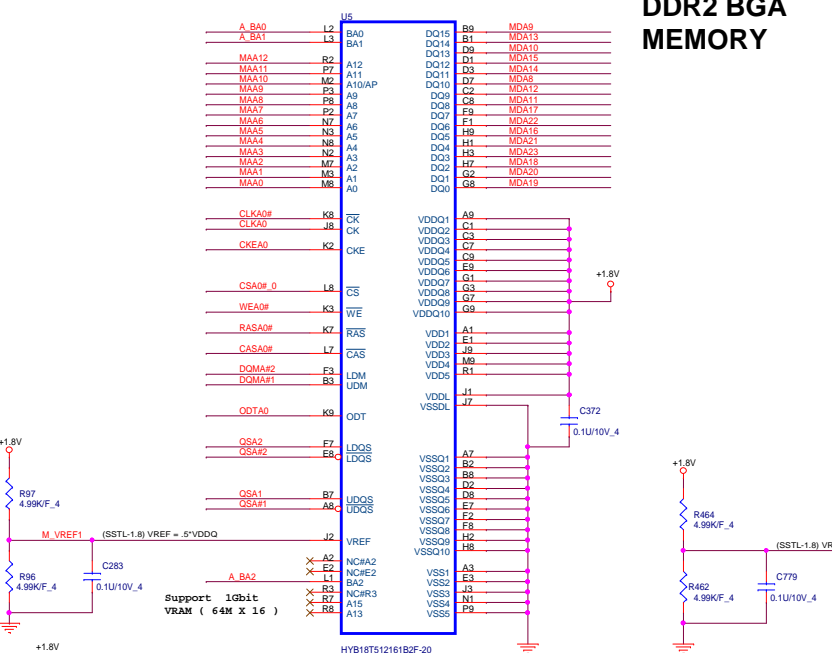
Change MEMTEST to 240 1%  
ohm to GND , AMD update



PROJECT : OP8  
Quanta Computer Inc.

Size Custom	Document Number M7X/M8X/MEM_Interface	Rev 1A
Date: Friday, March 20, 2009	Sheet 21	of 42

# DDR2 BGA MEMORY



DDR2 BGA MEMORY

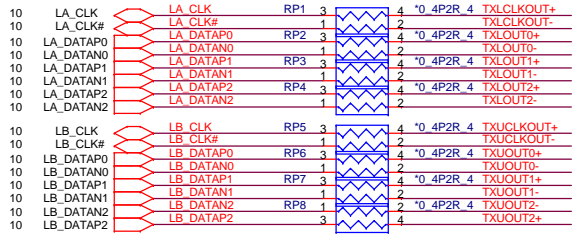
**PROJECT : OP8**  
Quanta Computer Inc.

Size C Document Number M92/VRAM\_A0,A1 Rev 1A

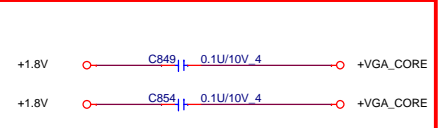
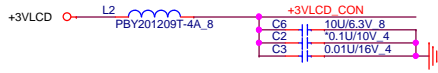
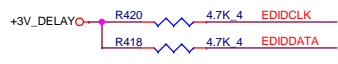
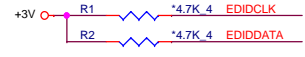
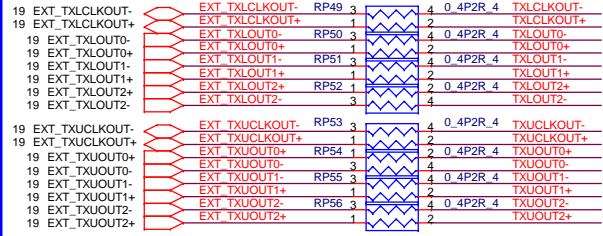
Date: Friday, March 20, 2009 Sheet 22 of 42

- 1. If LCD connector near GPU, then place these series Resistors near GPU
- 2. If LCD connector near N/B, then place these series Resistors near N/B

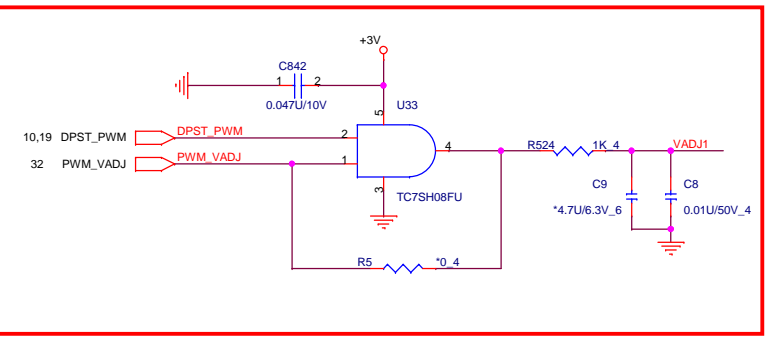
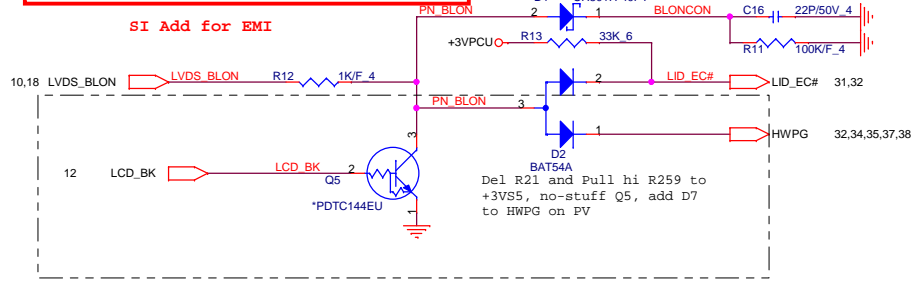
OPTION SIGNAL FROM NB to LVDS for UMA



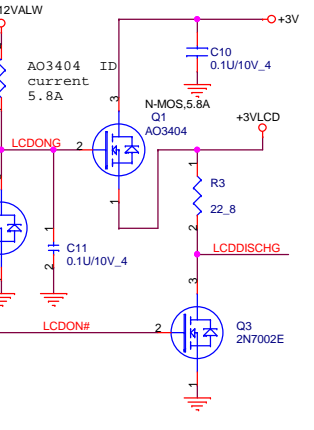
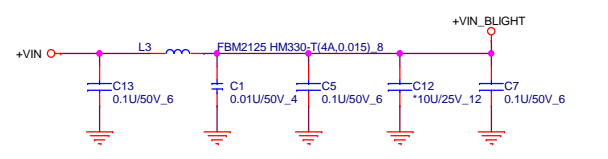
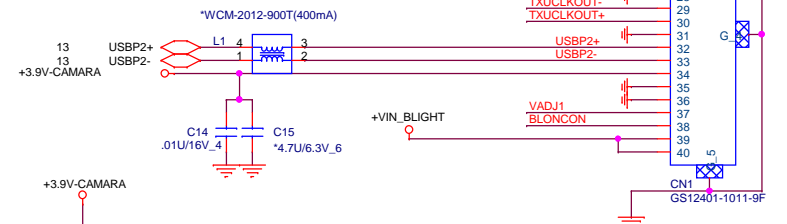
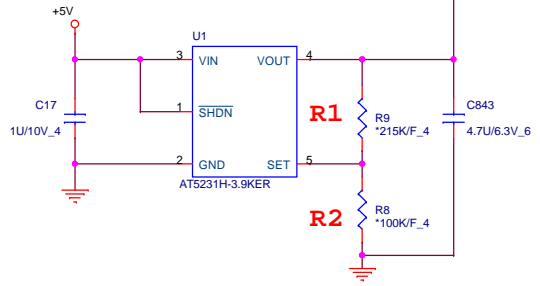
OPTION SIGNAL FROM M92 to LVDS for discrete



SI Add for EMI



SI add U33,R524,C842 for Vari bright function

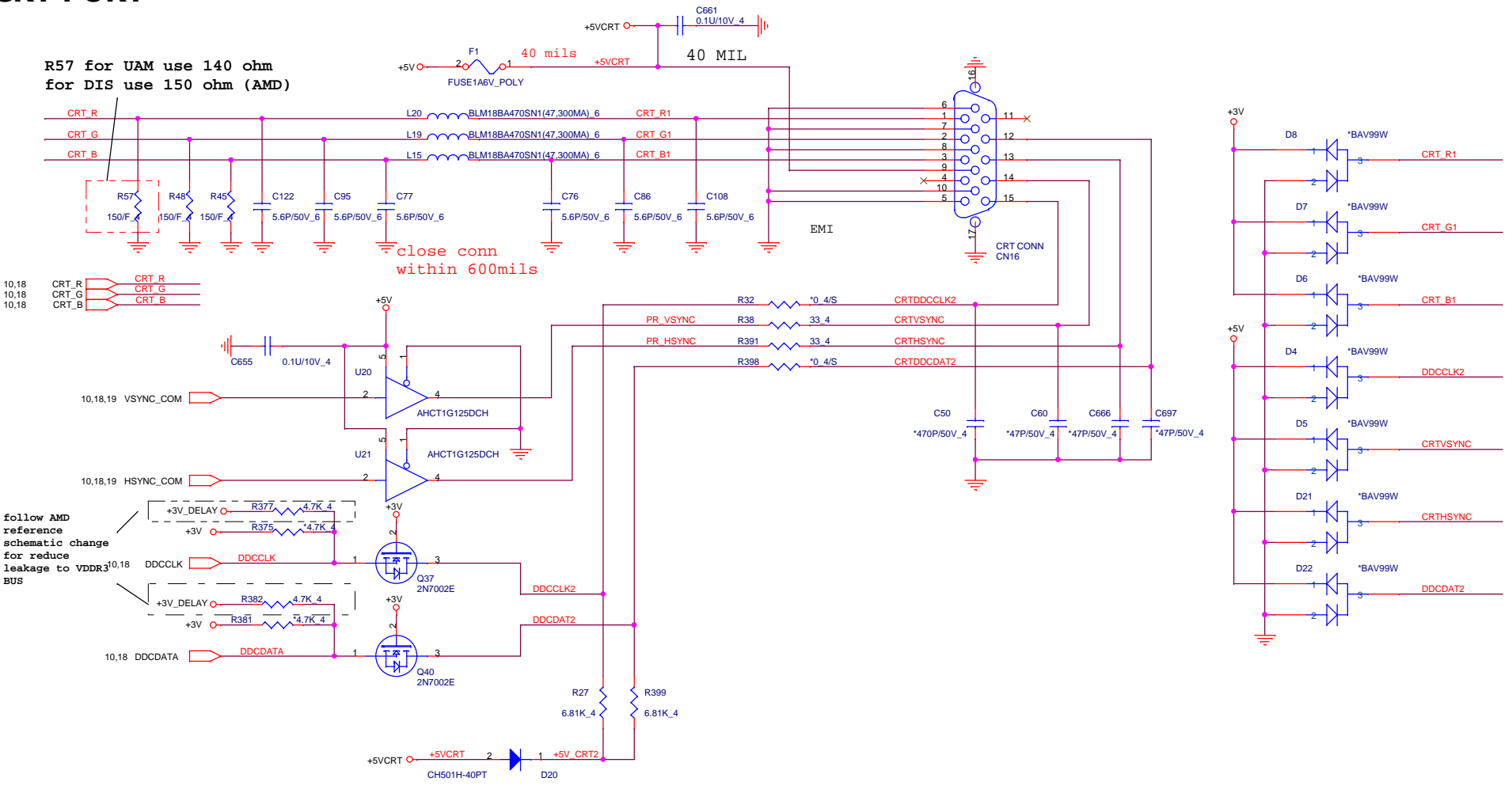


PROJECT : OP8  
Quanta Computer Inc.

Size Custom	Document Number LCD CONN	Rev 1A
Date: Friday, March 20, 2009	Sheet 23 of 42	

# CRT PORT

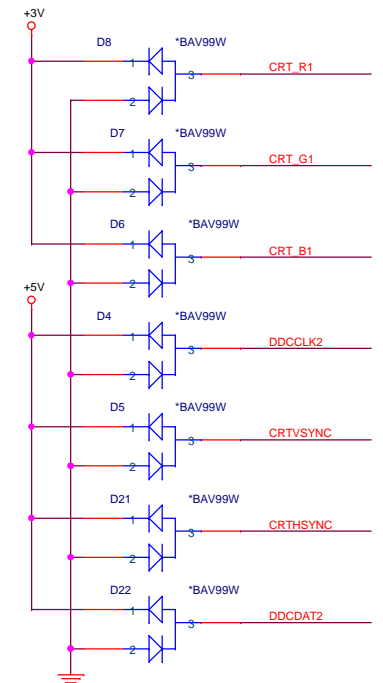
R57 for UAM use 140 ohm  
for DIS use 150 ohm (AMD)



close conn  
within 600mils



follow AMD  
reference  
schematic change  
for reduce  
leakage to VDDR3  
BUS



**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom	Document Number <b>CRT</b>	Rev 1A
Date: Friday, March 20, 2009		Sheet 24 of 42

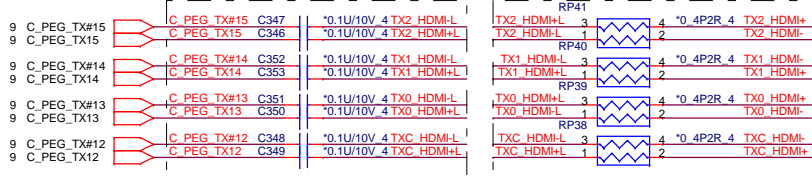


**UMA/DISCRETE select for HDMI**

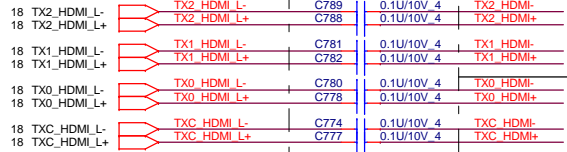
**From RS780M**

for Layout concern  
,placement close  
north bridge

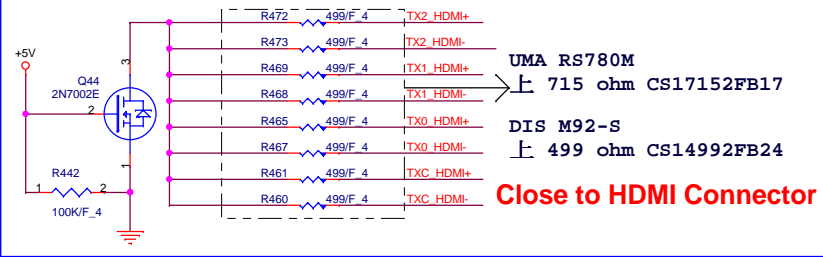
for Layout concern  
,placement close  
HDMI conn



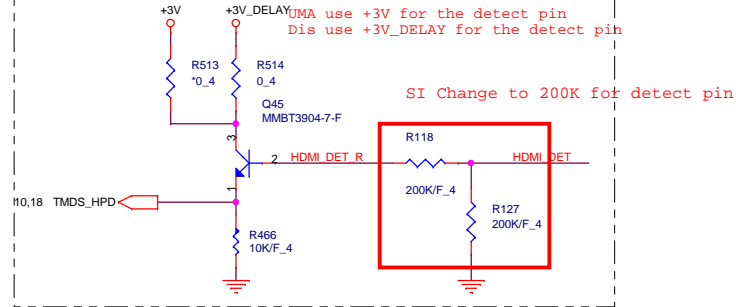
**From M92-S2**



for Layout concern  
,placement close  
HDMI conn

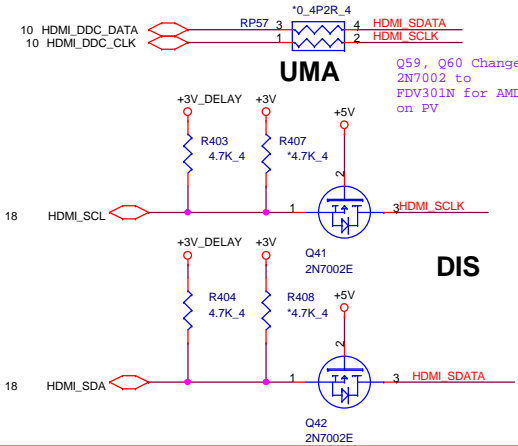


**HDMI HPD SENSE**



**UMA AND DISCRETE HDMI I2C SELECT**

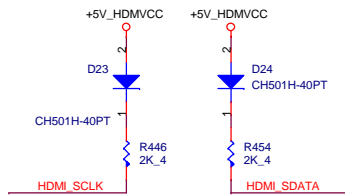
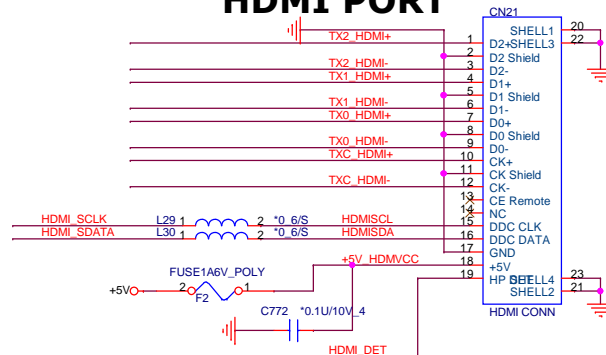
**Close to HDMI Connector**



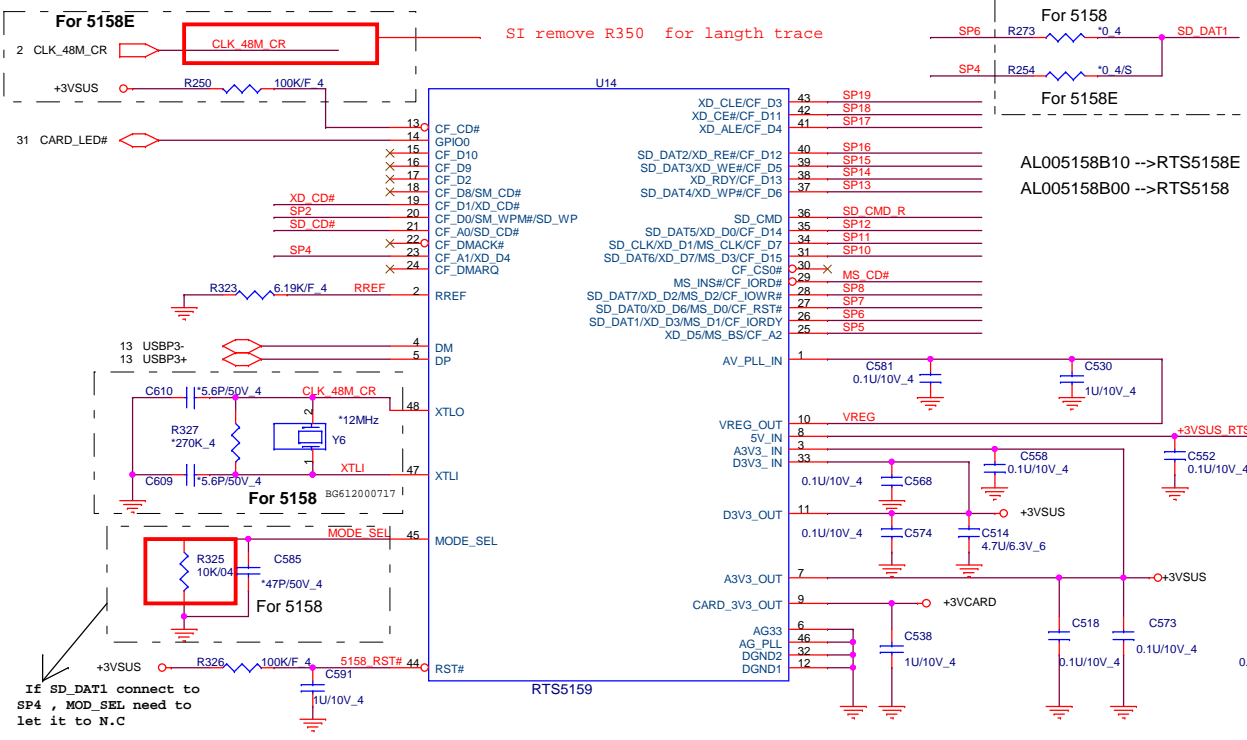
Discrete DDC4 is 5V tolerance, the MOSFET level shifter no need  
UMA DDC is 3V tolerance, the MOSFET level shifter is need

SI Change for DIS HDMI

**HDMI PORT**



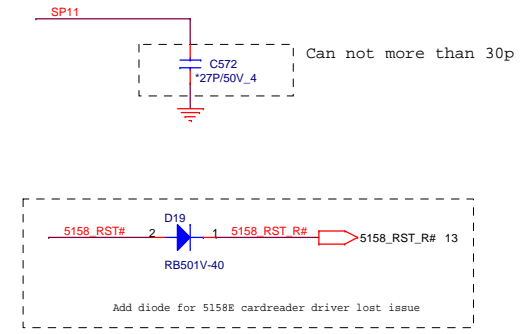
**PROJECT : OP8**  
Quanta Computer Inc.



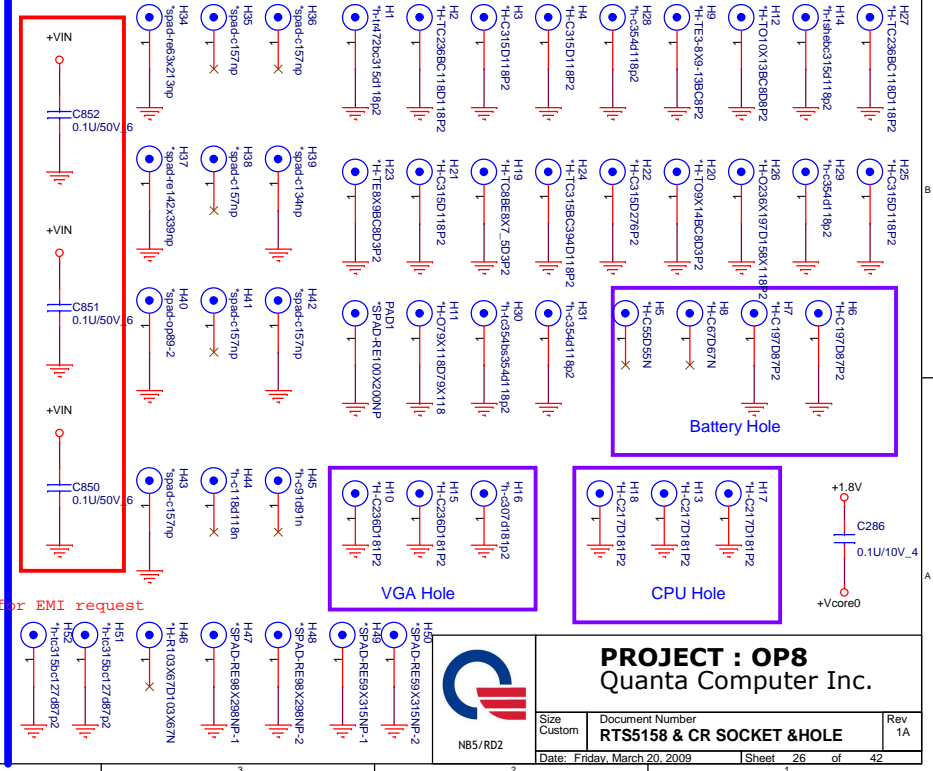
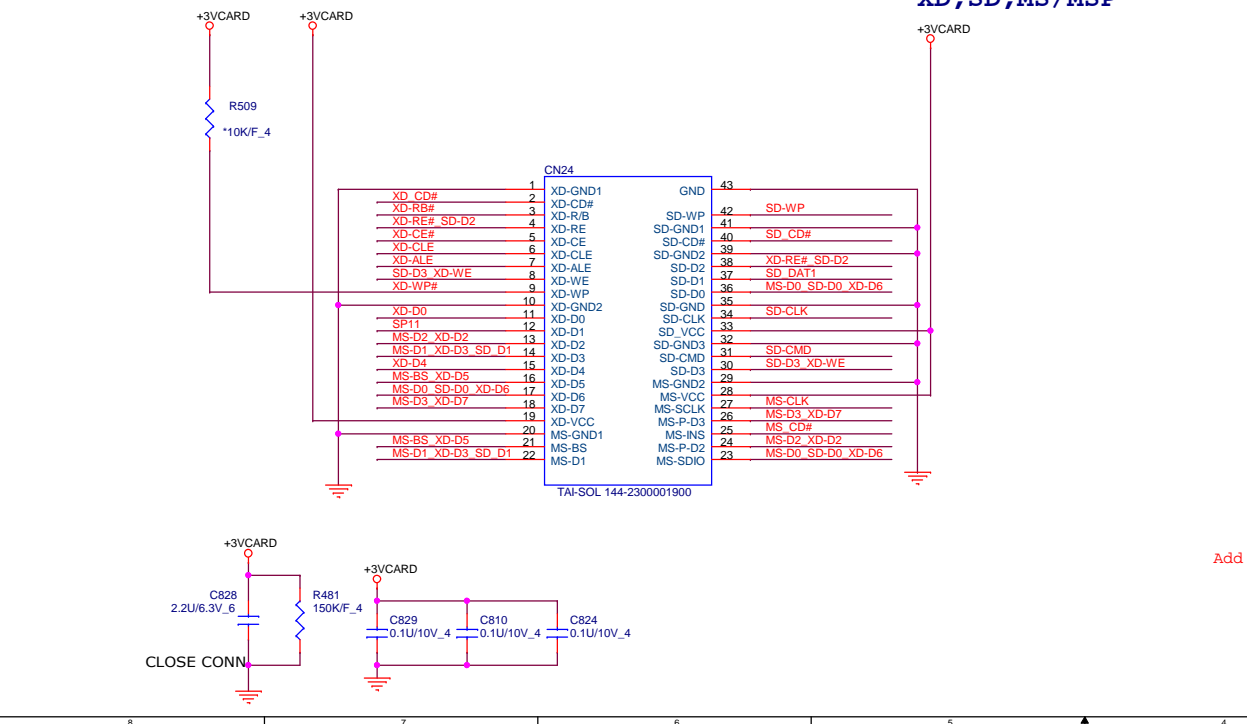
**Note:**

SD/MMC	MS	XD
SP1		XD_CD#
SP2	SD_WP	
SP3	SD_CD#	
SP4	SD_DAT1	XD_D4
SP5	MS_BS	XD_D5
SP6	MS_D1	XD_D3
SP7	SD_DAT0	MS_D0
SP8	SD_DAT7	MS_D2
SP9		MS_INS#
SP10	SD_DAT6	MS_D3
SP11	SD_CLK	MS_SCLK
SP12	SD_DAT5	XD_D0
SP13	SD_DAT4	XD_WP#
SP14		XD_R/#
SP15	SD_DAT3	XD_WE#
SP16	SD_DAT2	XD_RE#
SP17		XD_ALE
SP18		XD_CE#
SP19		XD_CLE

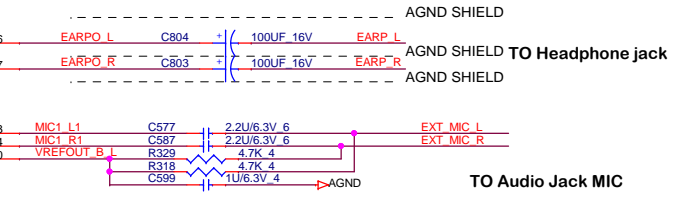
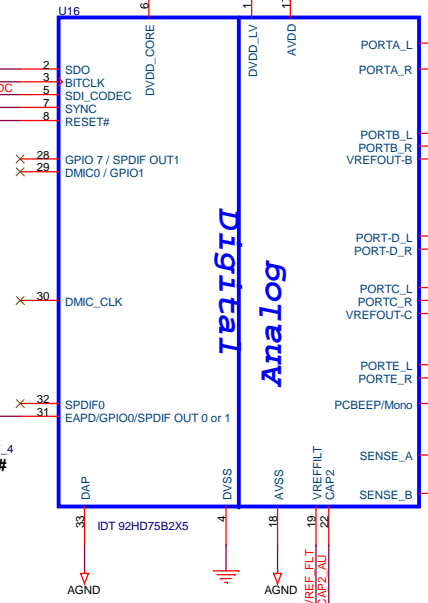
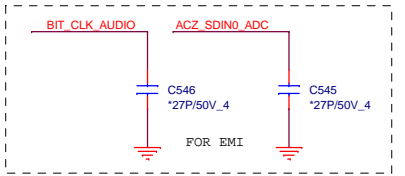
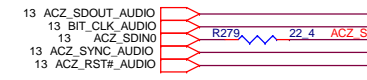
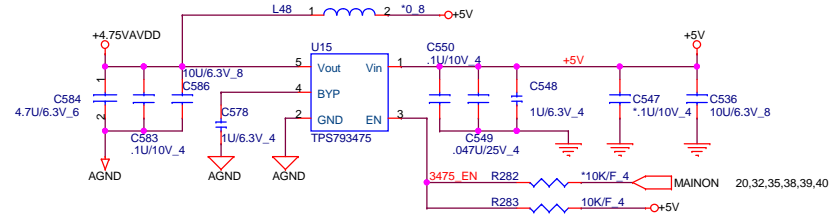
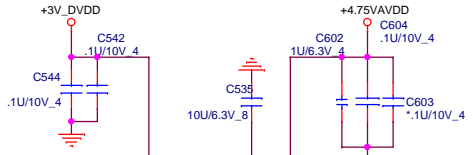
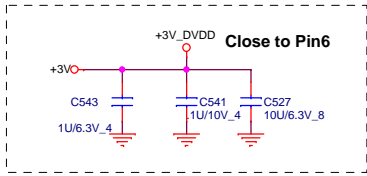
SP7	R280	*0.4/S	MS-D0	SD-D0	XD-D6
SP8	R268	*0.4/S	MS-D1	XD-D3	SD-D1
SP6	R252	*0.4/S	MS-D2	XD-D2	
SP16	R343	*0.4/S	XD-RE#	SD-D2	
SP6	R258	*0.4/S	MS-BS	XD-D5	
SP15	R342	*0.4/S	SD-D3	XD-WE	
SP11	R314	*0.4/S	SD-CLK		
SP2	R523	*0.4/S	MS-CLK		
SP3	R255	*0.4/S	SD_WP		
SP19	R345	*0.4/S	XD_WP#		
SP4	R253	*0.4/S	XD-D4		
SP10	R291	*0.4/S	MS-D3	XD-D7	
SP14	R353	*0.4/S	XD-R/#		
SP12	R322	*0.4/S	XD-D0		
SP17	R354	*0.4/S	XD-ALE		
SP18	R344	*0.4/S	XD-CE#		
SD_CMD_R	R331	*0.4/S	SD-CMD		



**4 IN1 CARD READER  
XD, SD, MS/MSP**



**PROJECT : OP8**  
Quanta Computer Inc.

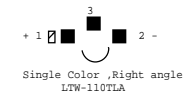
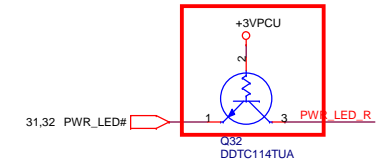
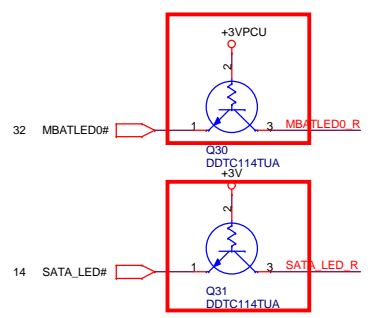
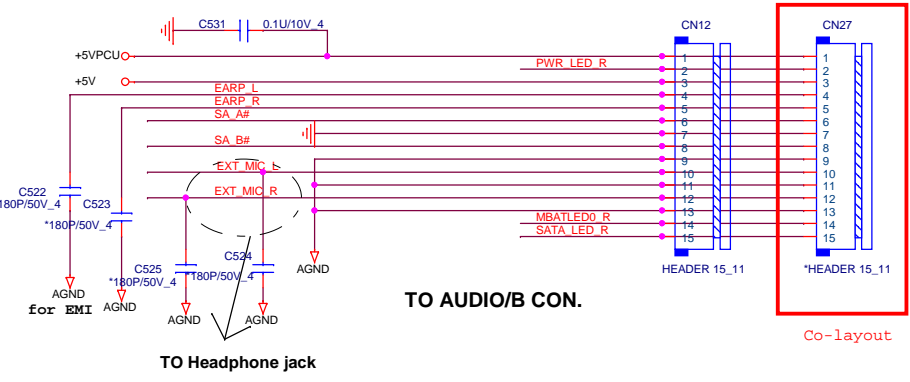
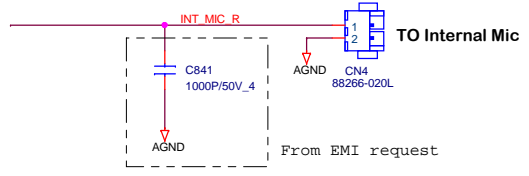
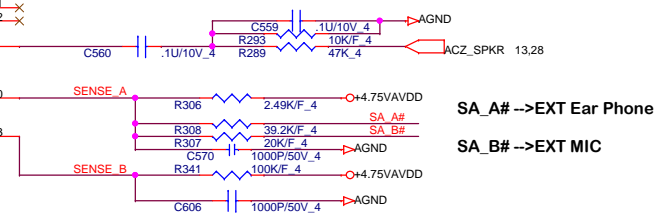
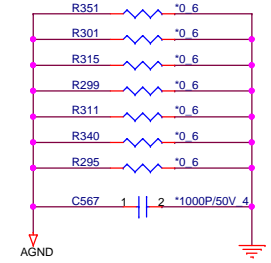
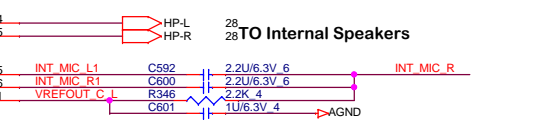


**Audio JACK: Normal Open**

SA\_A# -->EXT HP

SA\_B# -->EXT MIC

Sense\_B -->INT MIC



**PROJECT : OP8**  
Quanta Computer Inc.

NB5/RD2

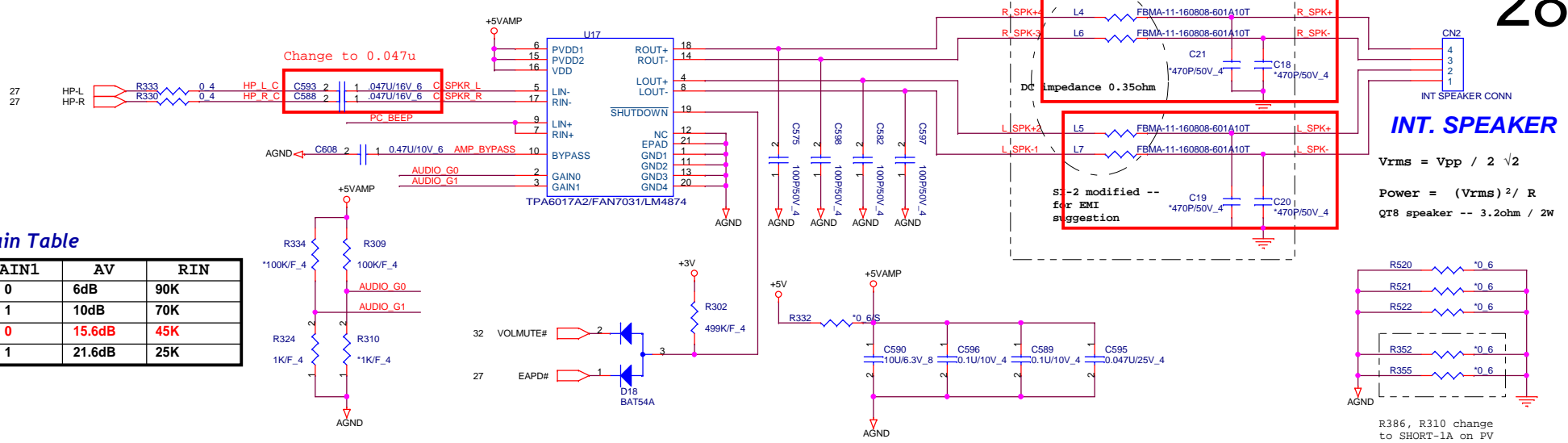
Size Custom

Document Number **Azalia 92HD75B2X5**

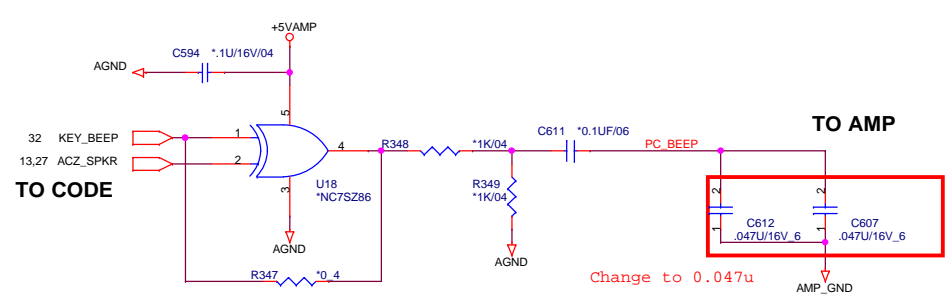
Date: Friday, March 20, 2009

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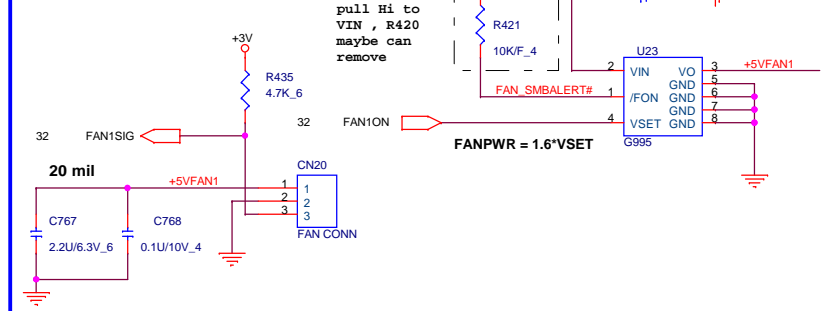
Rev 1A



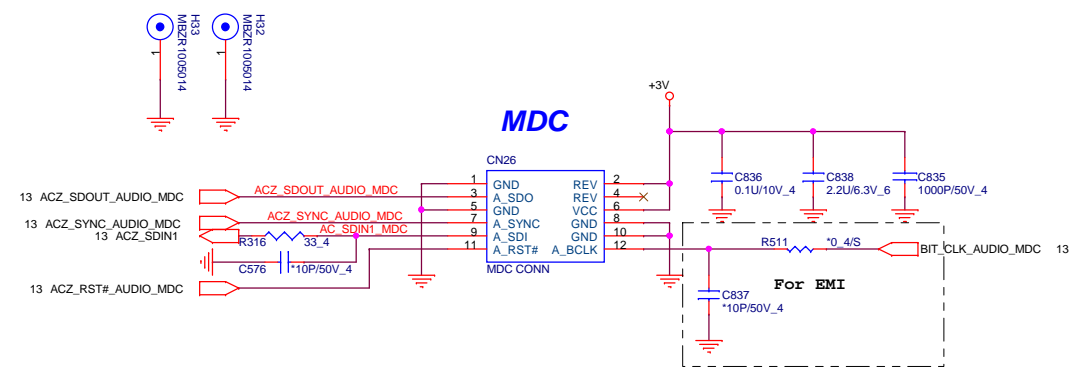
## PC-BEEP



## CPU FAN

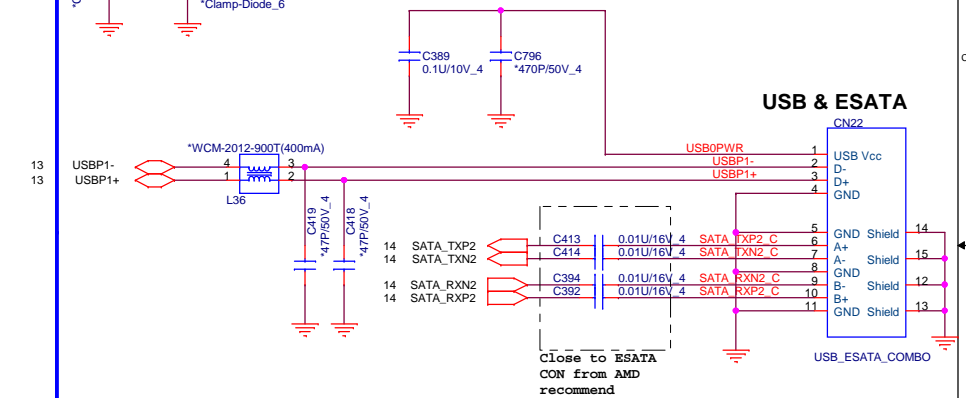
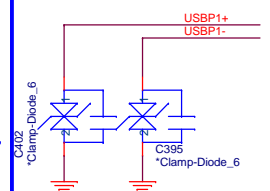
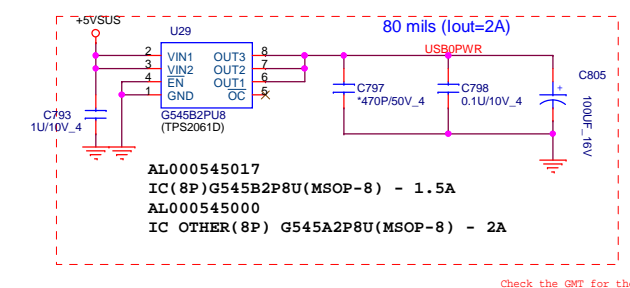
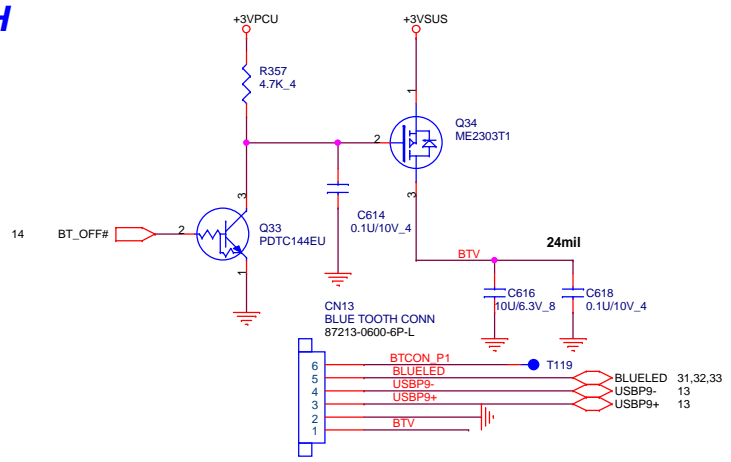


## Modem CONN

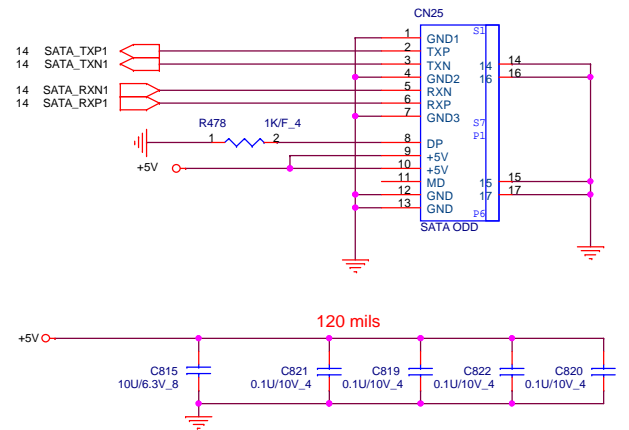


**PROJECT : OP8**  
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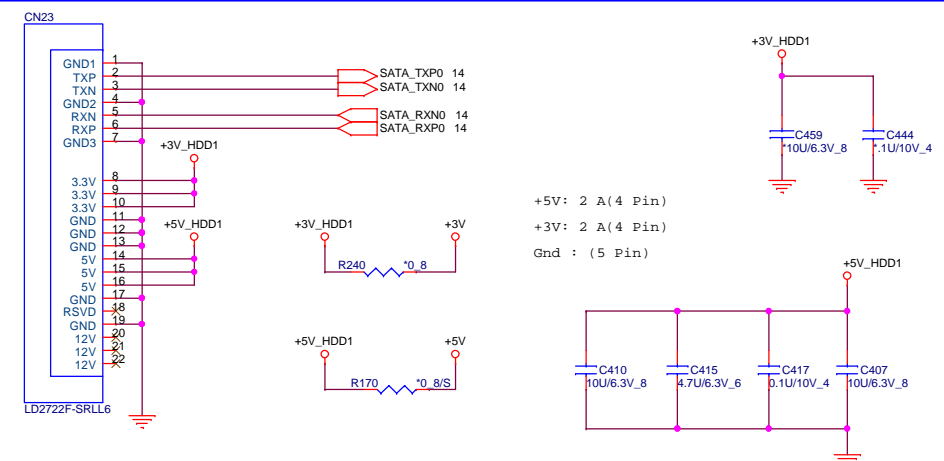
Size Custom	Document Number <b>AMP_TPA6017/MDC1.5/CPU FAN</b>	Rev 1A
Date: Friday, March 20, 2009		Sheet 28 of 42



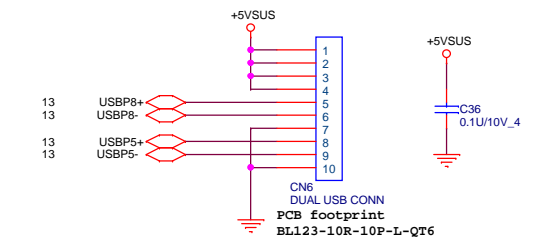
SATA CD-ROM

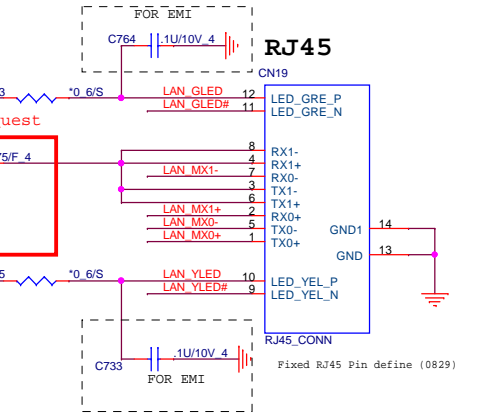
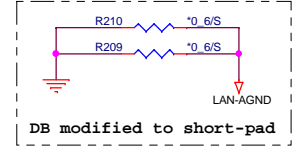
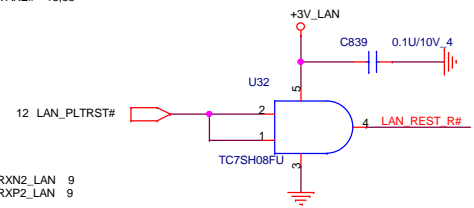
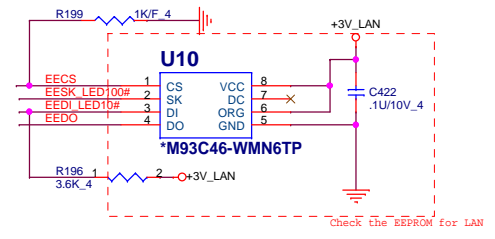
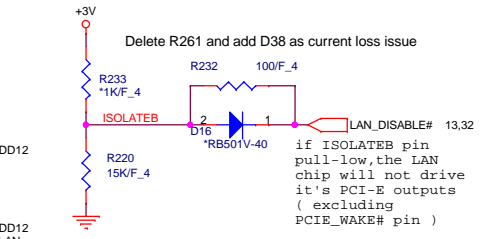
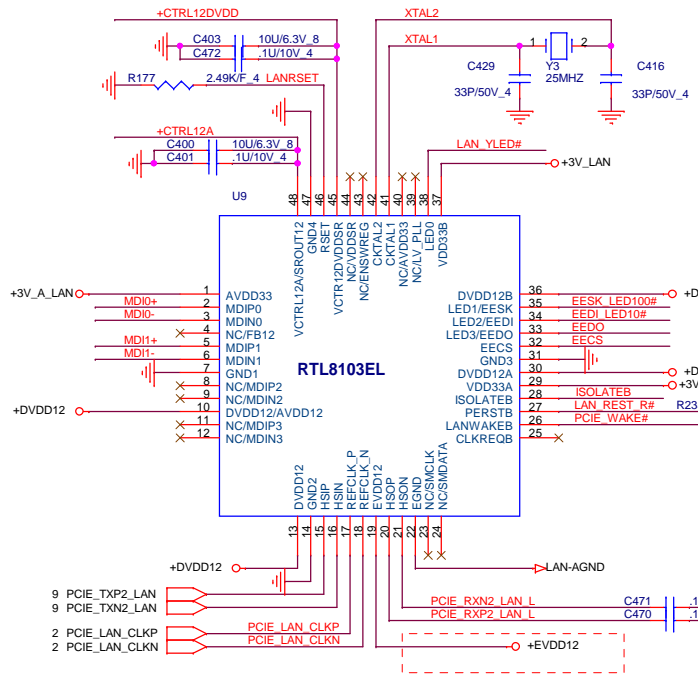
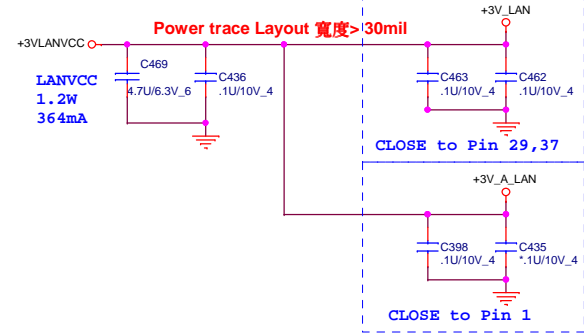
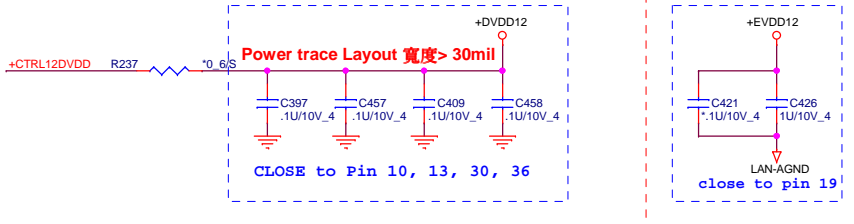


SATA HDD

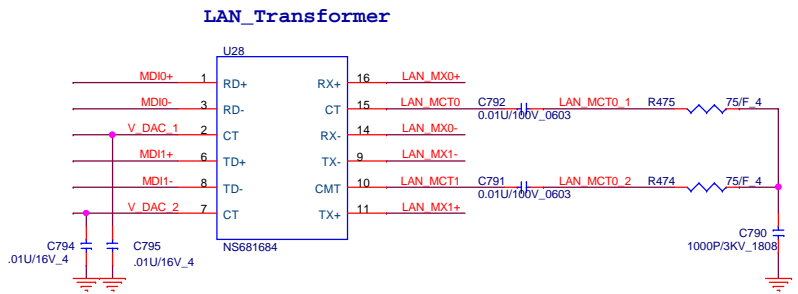
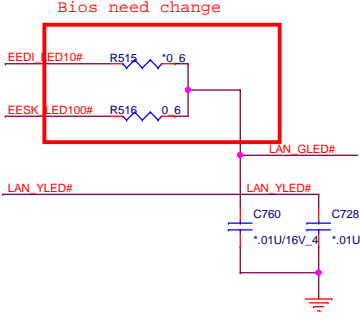


RIGHT SIDE USBX2





Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
LED0	O	57	38	LED0 Tx/Rx
LED1	O	56	35	LED1 LNK100
LED2	O	55	34	LED2 LNK10
LED3	O	54	33	LED3 NA

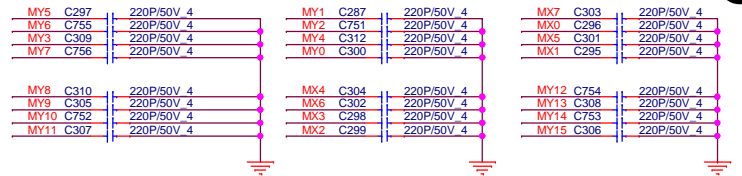
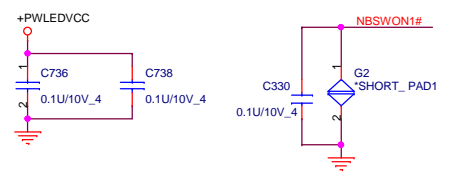


**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom	Document Number <b>RTL8102EL/RJ45</b>	Rev 1A
Date: Friday, March 20, 2009		Sheet 30 of 42

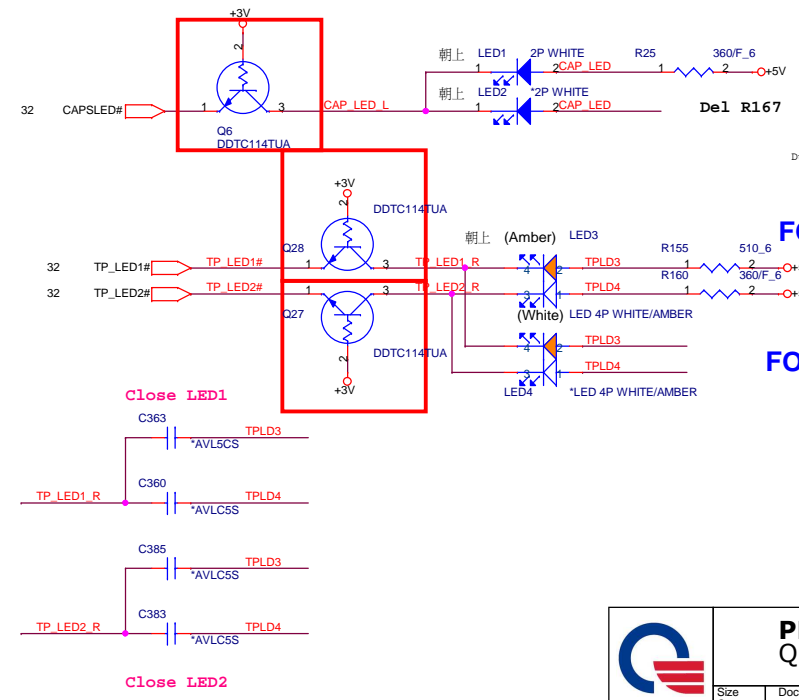
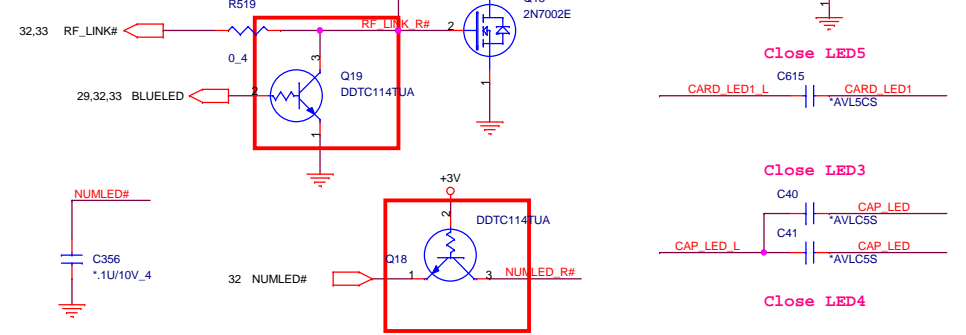
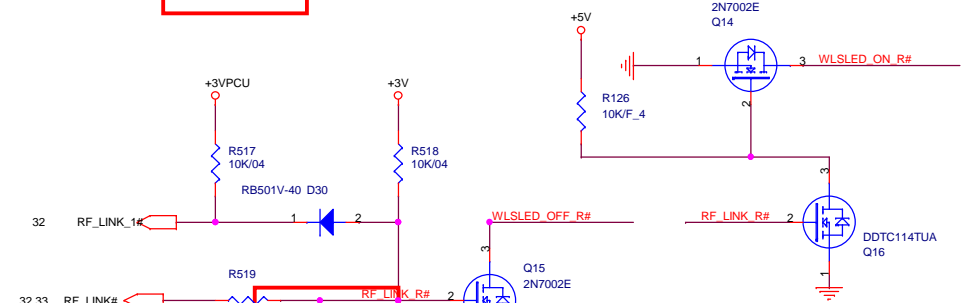
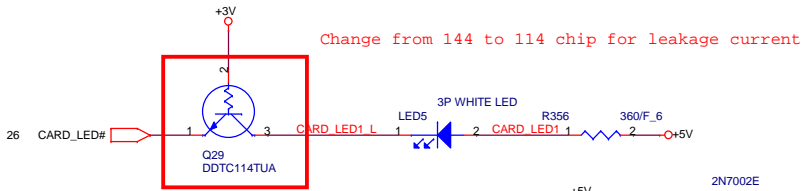
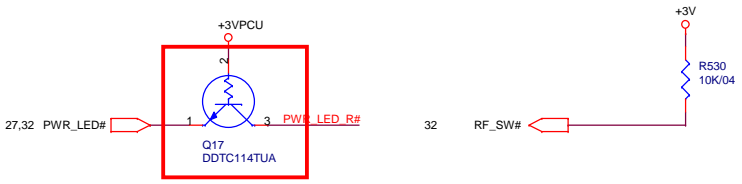
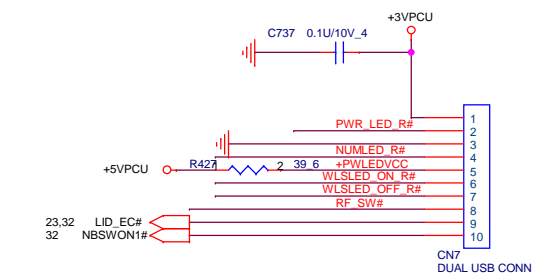
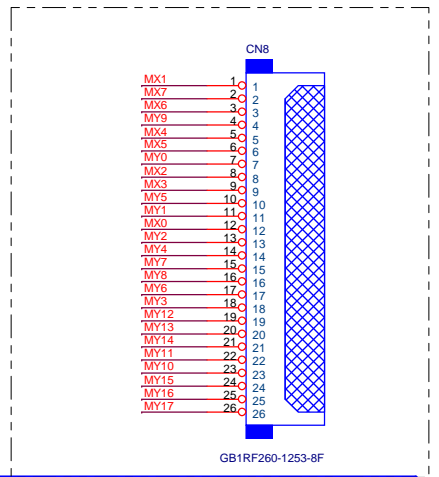
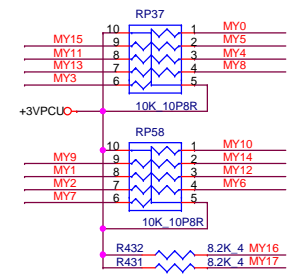
# POWER BUTTON CONNECT

31



1. +3VPCU(LIDSWITCH PWR)
2. PWR\_LED#
3. GND
4. NumLED
5. +5VPCU (PWRLED PWR)
6. WLSLED\_ON#
7. WLSLED\_OFF#
8. RF\_SW#
9. LIDSWITCH
10. POWERON#

## KEYBOARD PULL-UP

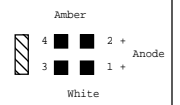


FOR 16"  
FOR 17.3"

Dual Color ,Right angle

FOR 16"

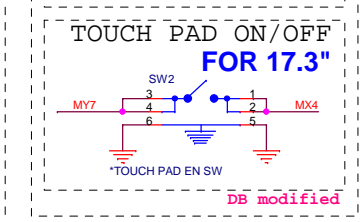
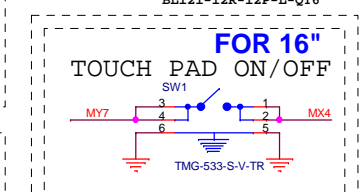
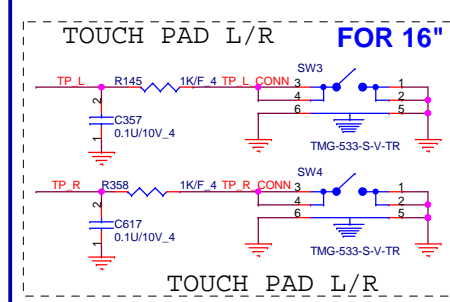
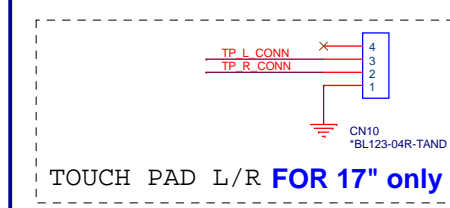
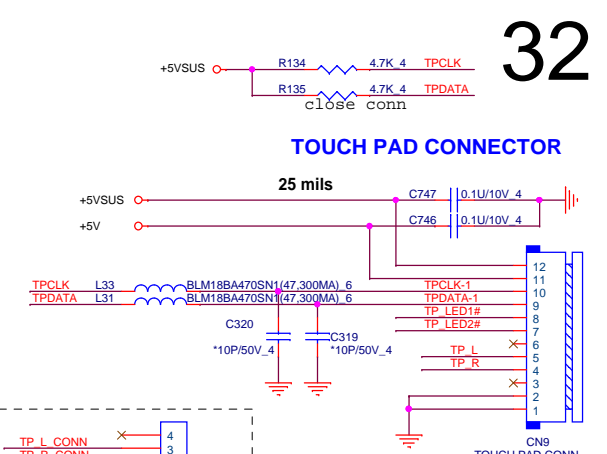
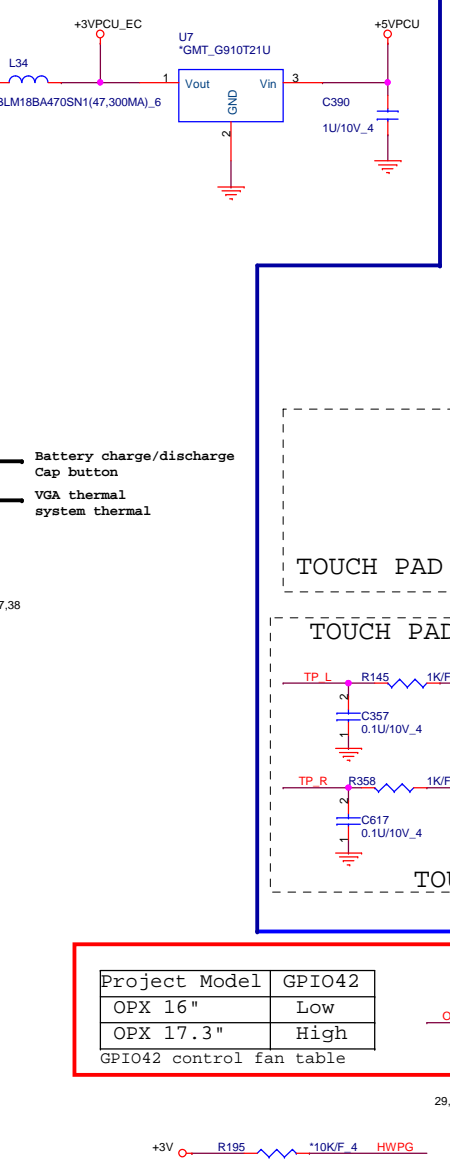
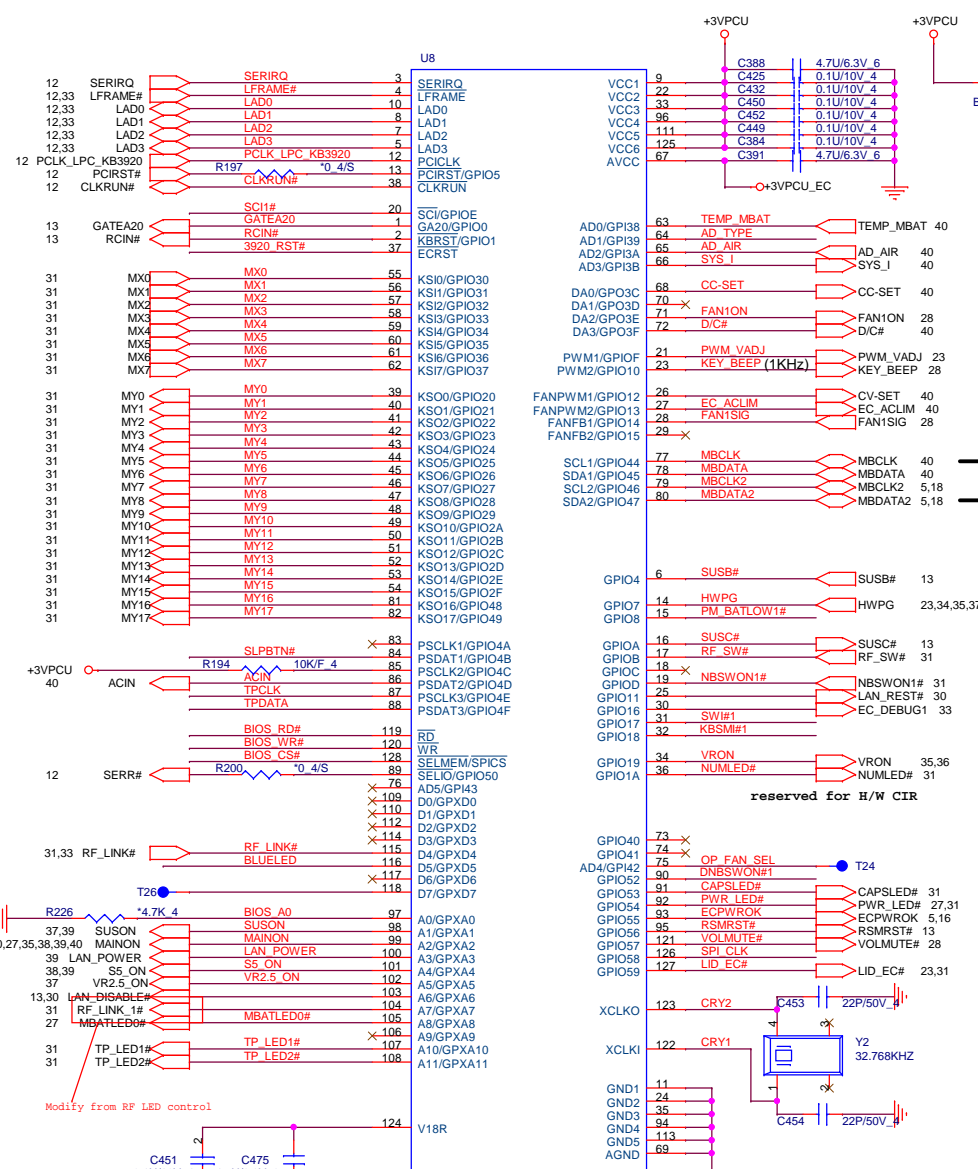
FOR 17.3"



**PROJECT : OP8**  
Quanta Computer Inc.

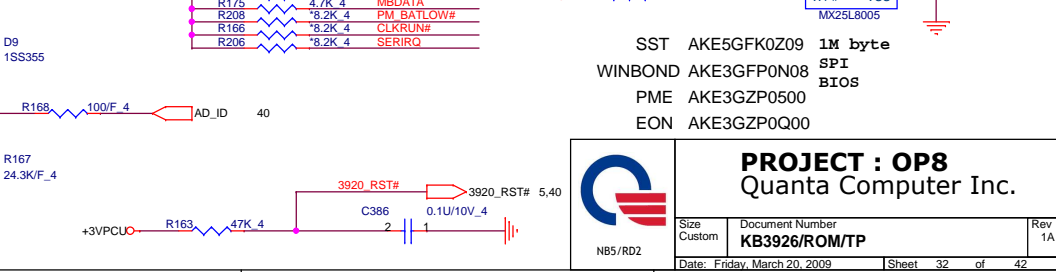
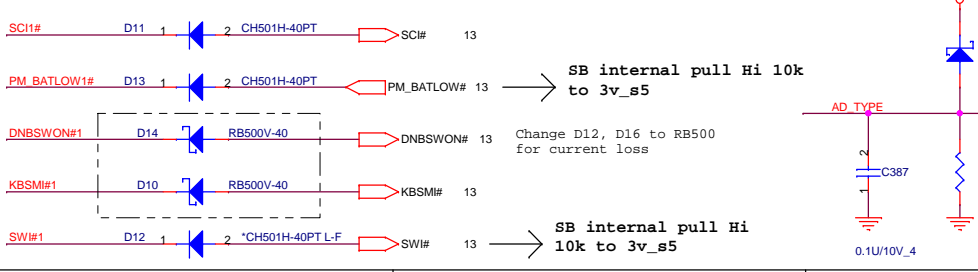
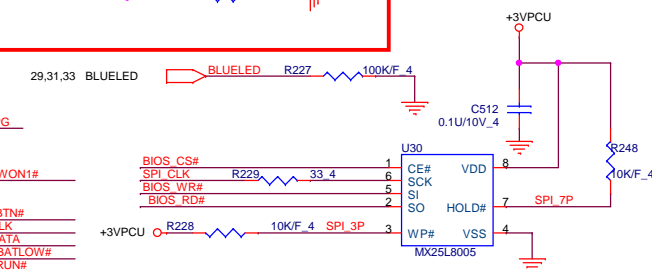
Size Custom	Document Number	Rev 1A
LED/KEYBOARD/SW_BOARD		
Date: Friday, March 20, 2009		Sheet 31 of 42

NB5/RD2



Project Model	GPIO42
OPX 16"	Low
OPX 17.3"	High

GPIO42 control fan table



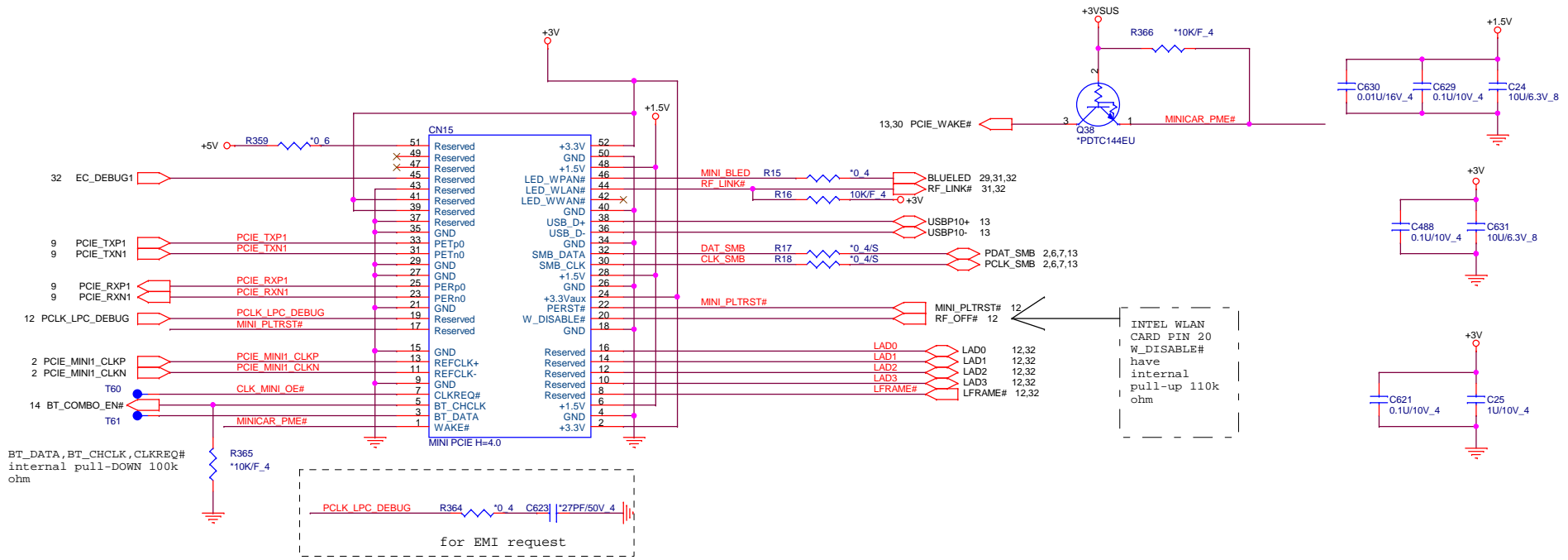
**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom Document Number KB3926/ROM/TP Rev 1A

Date: Friday, March 20, 2009 Sheet 32 of 42



# Mini PCI-E Card 1 WLAN



**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom	Document Number <b>Mini CARD</b>	Rev 1A
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NBS/RD2



$$T_{on} = 3.85p * R_{TON} * V_{OUT} / (V_{IN} - 0.5)$$

$$Frequency = V_{out} / (V_{IN} * T_{ON})$$

reserved for pwr seq -- andrew

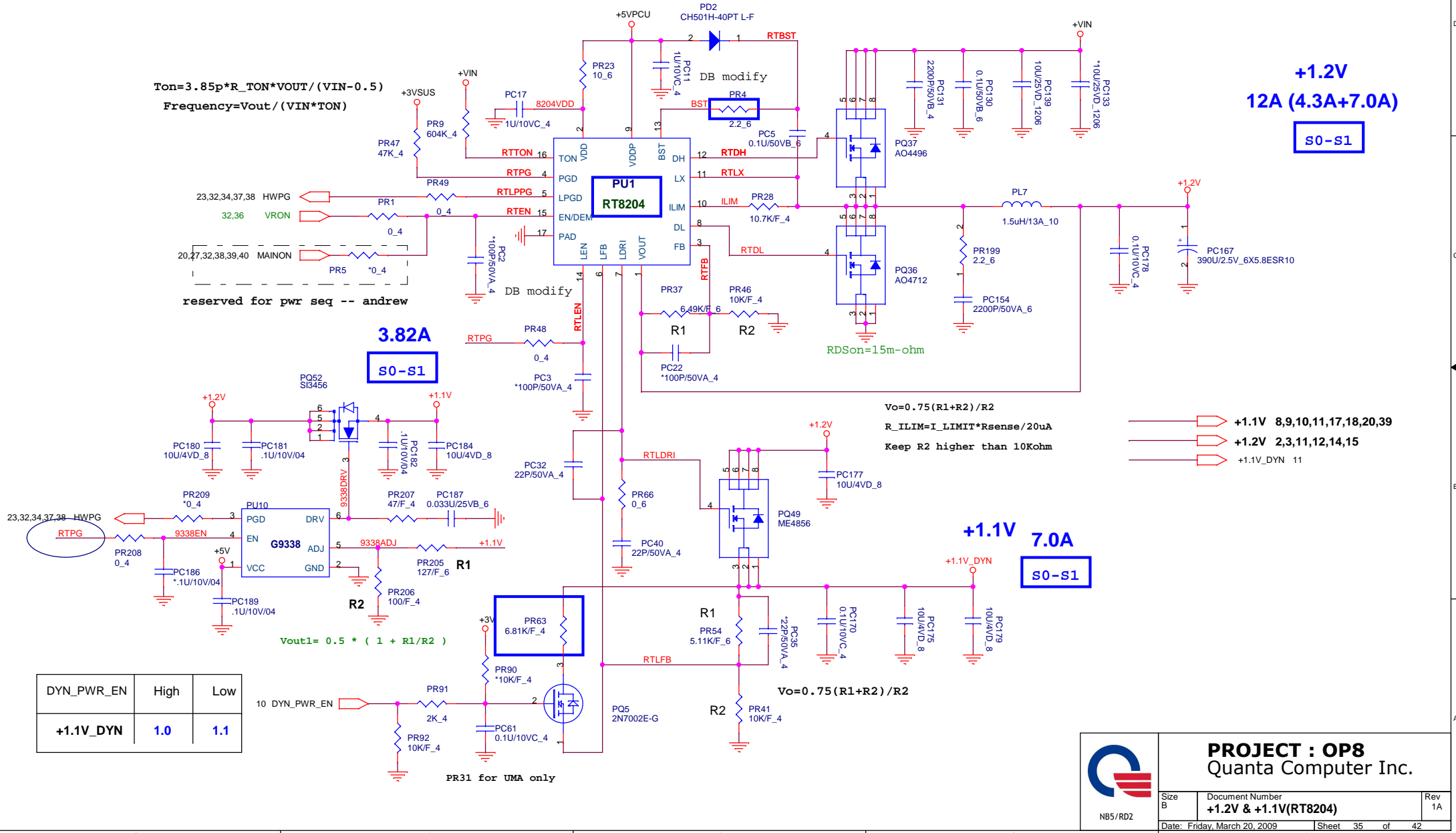
**3.82A**  
**S0-S1**

**+1.2V**  
**12A (4.3A+7.0A)**  
**S0-S1**

**+1.1V**  
**7.0A**  
**S0-S1**

- +1.1V 8,9,10,11,17,18,20,39
- +1.2V 2,3,11,12,14,15
- +1.1V\_DYN 11

DYN_PWR_EN	High	Low
+1.1V_DYN	1.0	1.1



$$V_o = 0.75 (R1 + R2) / R2$$

$$R_{ILIM} = I_{LIMIT} * R_{sense} / 20\mu A$$

Keep R2 higher than 10Kohm

$$V_o = 0.75 (R1 + R2) / R2$$

PR31 for UMA only



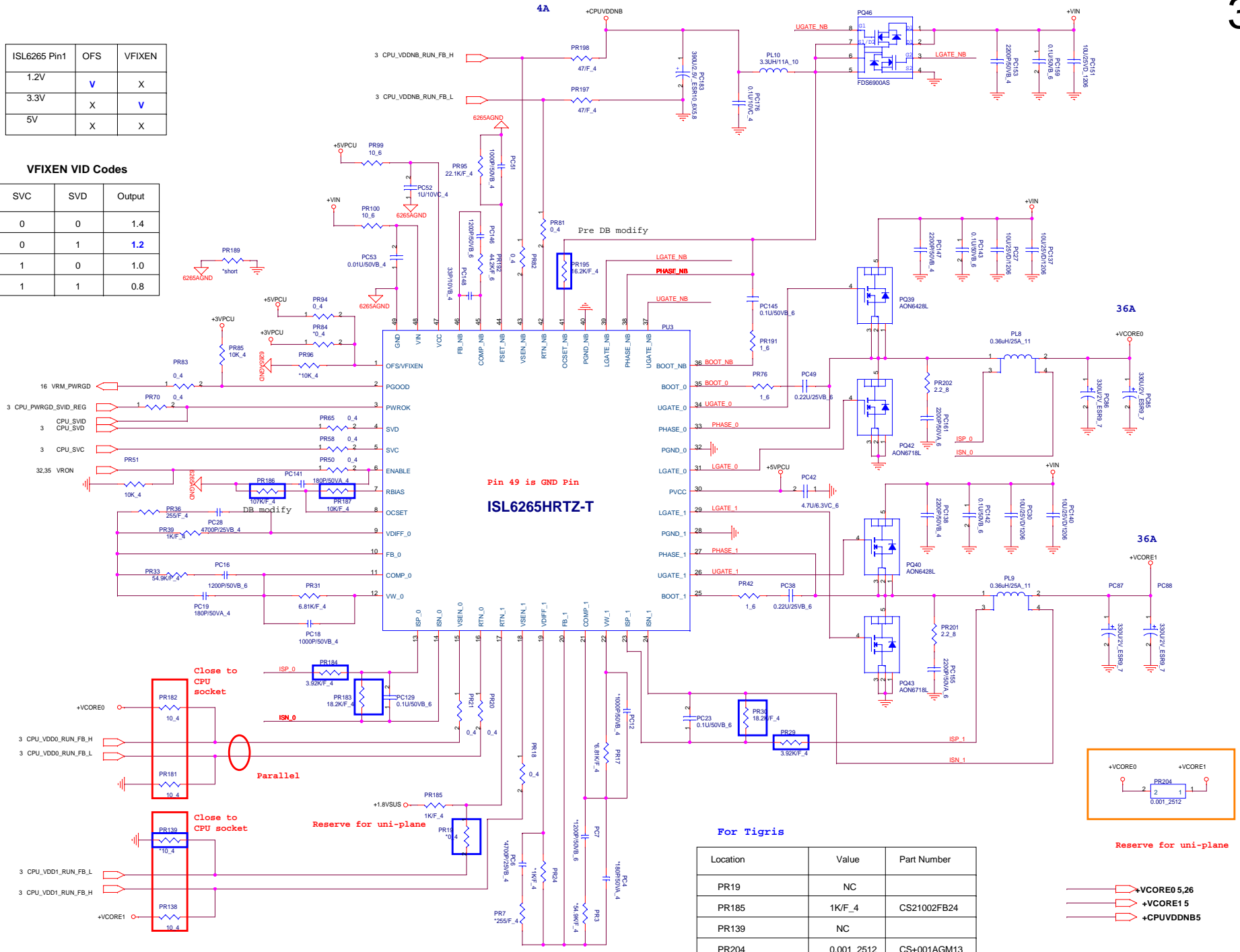
**PROJECT : OP8**  
**Quanta Computer Inc.**

Size B	Document Number <b>+1.2V &amp; +1.1V(RT8204)</b>	Rev 1A
Date: Friday, March 20, 2009 Sheet 35 of 42		

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

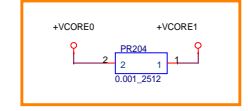
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



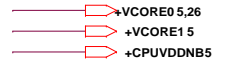
Pin 19 is GND Pin  
ISL6265HRTZ-T

For Tigris

Location	Value	Part Number
PR19	NC	
PR185	1K/F_4	CS21002FB24
PR139	NC	
PR204	0.001_2512	CS+001AGM13
PC12,PR17,PC4,PC7, PR3,PR24,PC6,PR7	NC	

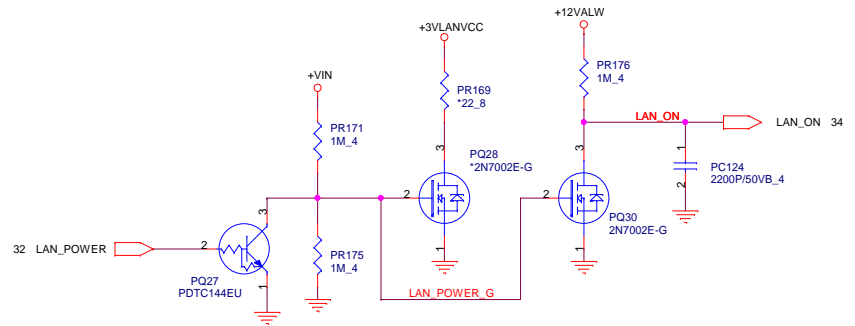
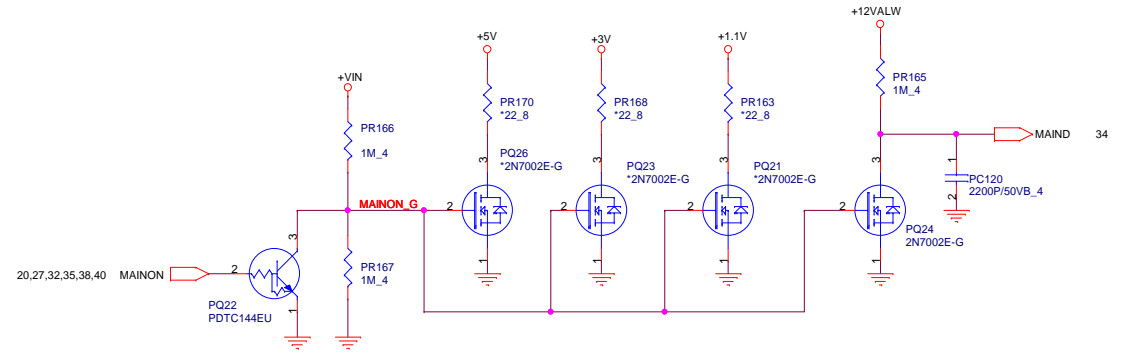
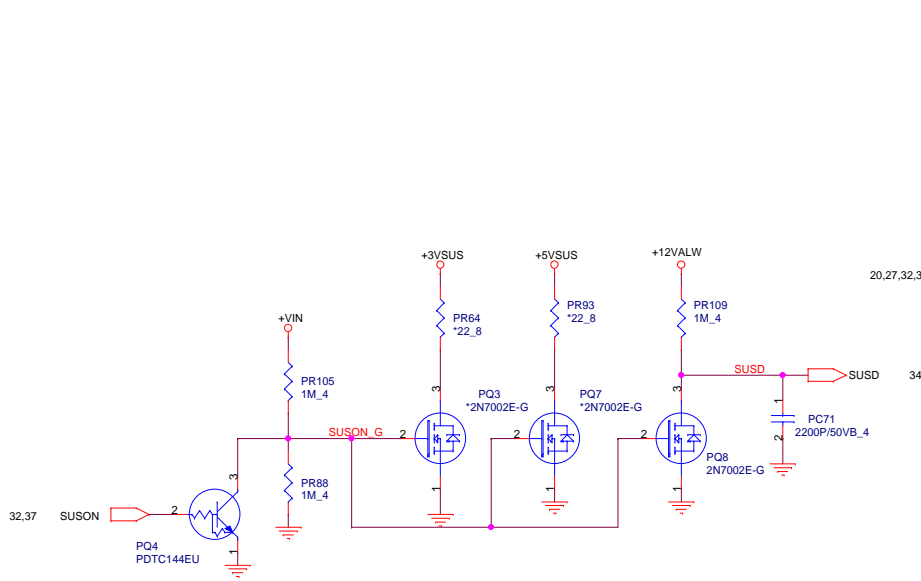


Reserve for uni-plane

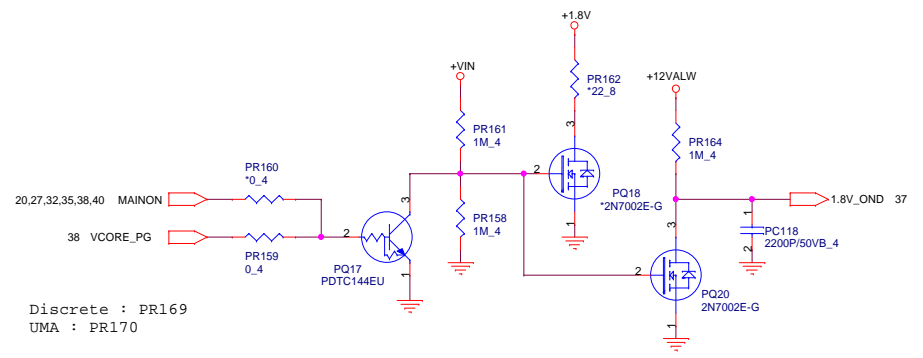
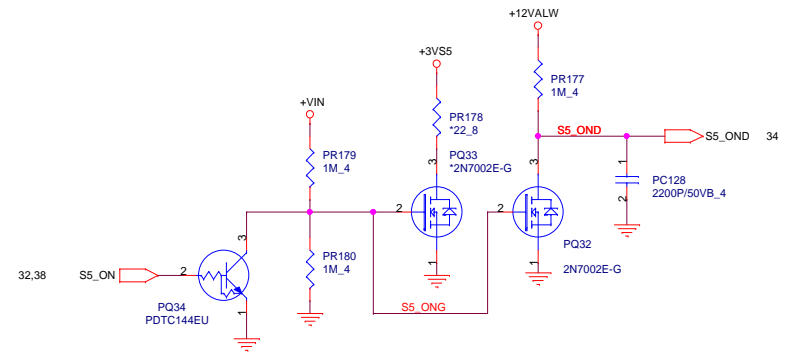








*For Discrete Only*



Discrete : PR169  
UMA : PR170





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