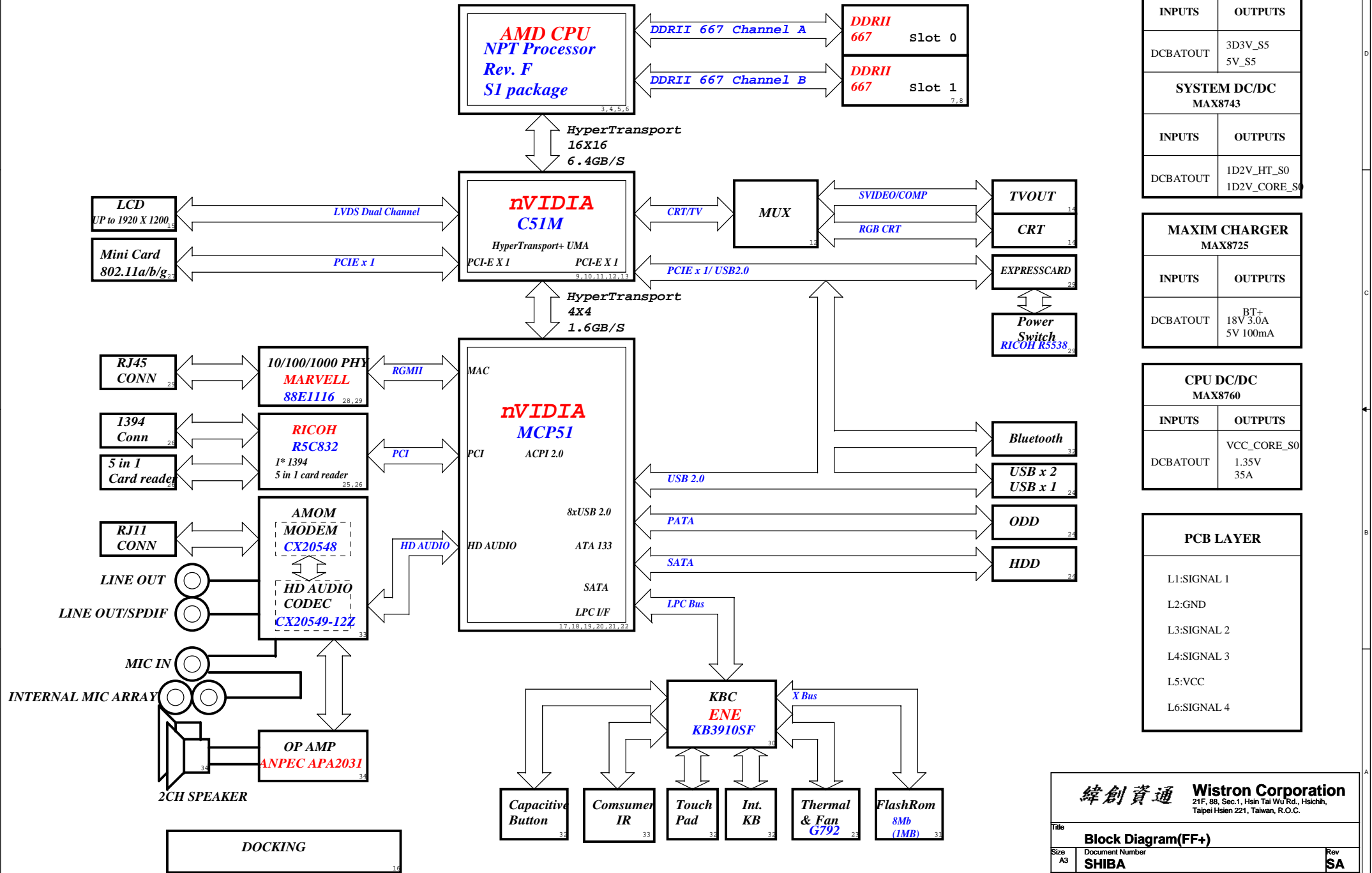


# Shiba Block Diagram(FF+)

Project Code: 91.4F701.001  
 Project Name: Shiba  
 PCB Number: 05234



SYSTEM DC/DC MAX8734A	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D2V_HT_S0 1D2V_CORE_S0

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8760	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 1.35V 35A

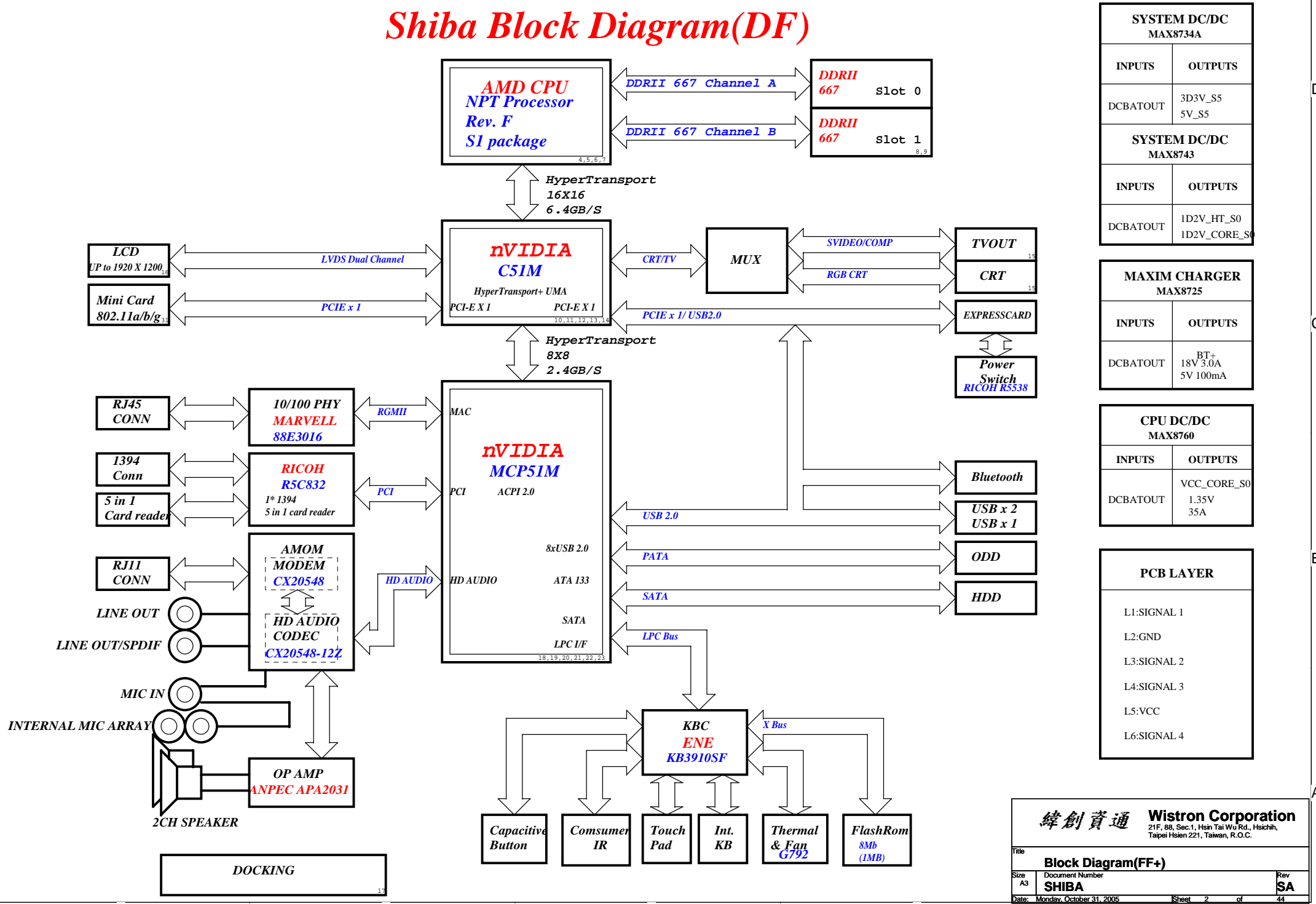
PCB LAYER	
L1:	SIGNAL 1
L2:	GND
L3:	SIGNAL 2
L4:	SIGNAL 3
L5:	VCC
L6:	SIGNAL 4

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram(FF+)**

Size: A3	Document Number: SHIBA	Rev: SA
Date: Friday, November 11, 2005	Sheet: 1 of	44

# Shiba Block Diagram(DF)



SYSTEM DC/DC MAX8734A	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5
SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D2V_HT_S0 1D2V_CORE_S0

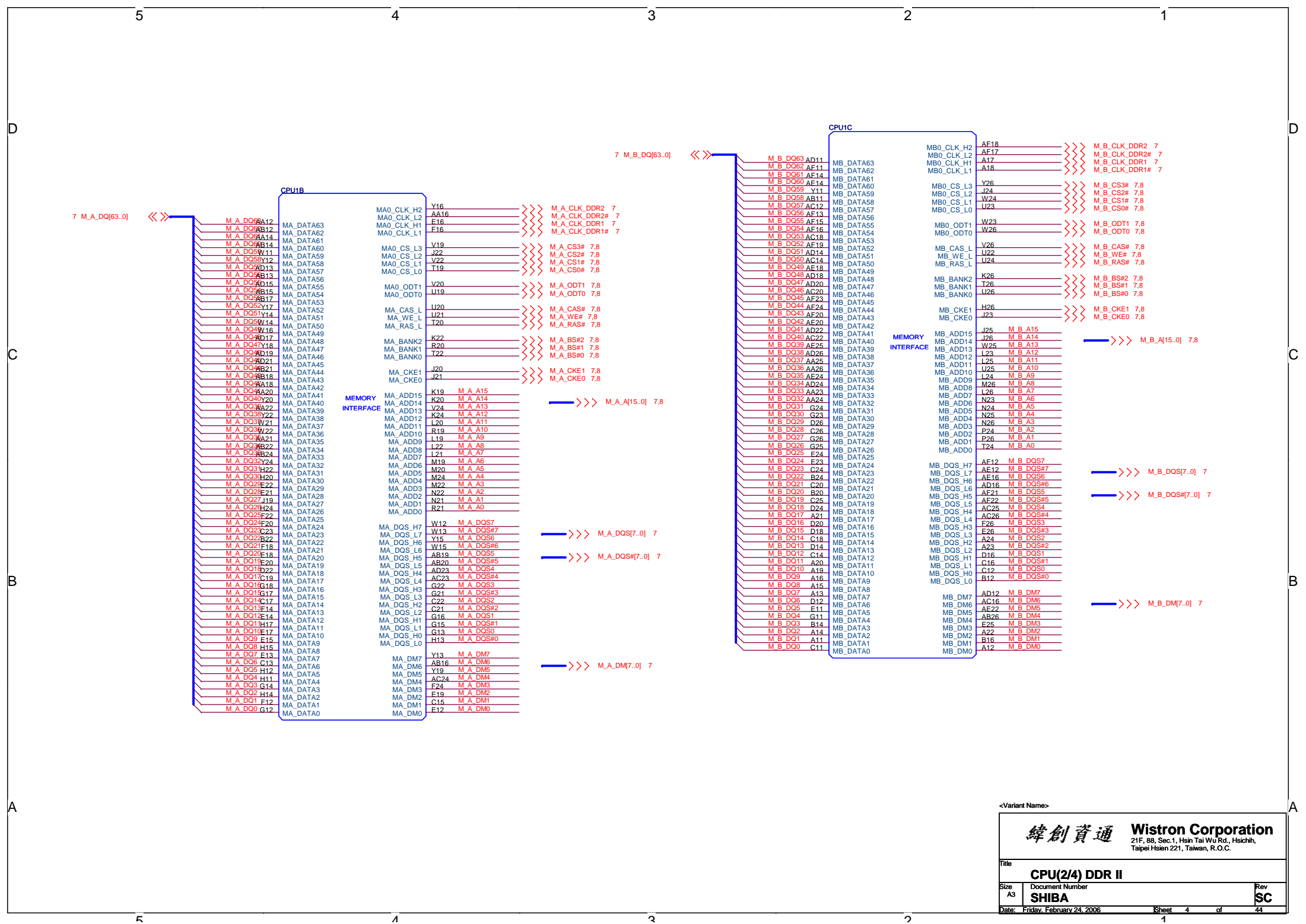
MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8760	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 1.35V 35A

PCB LAYER	
L1: SIGNAL 1	
L2: GND	
L3: SIGNAL 2	
L4: SIGNAL 3	
L5: VCC	
L6: SIGNAL 4	

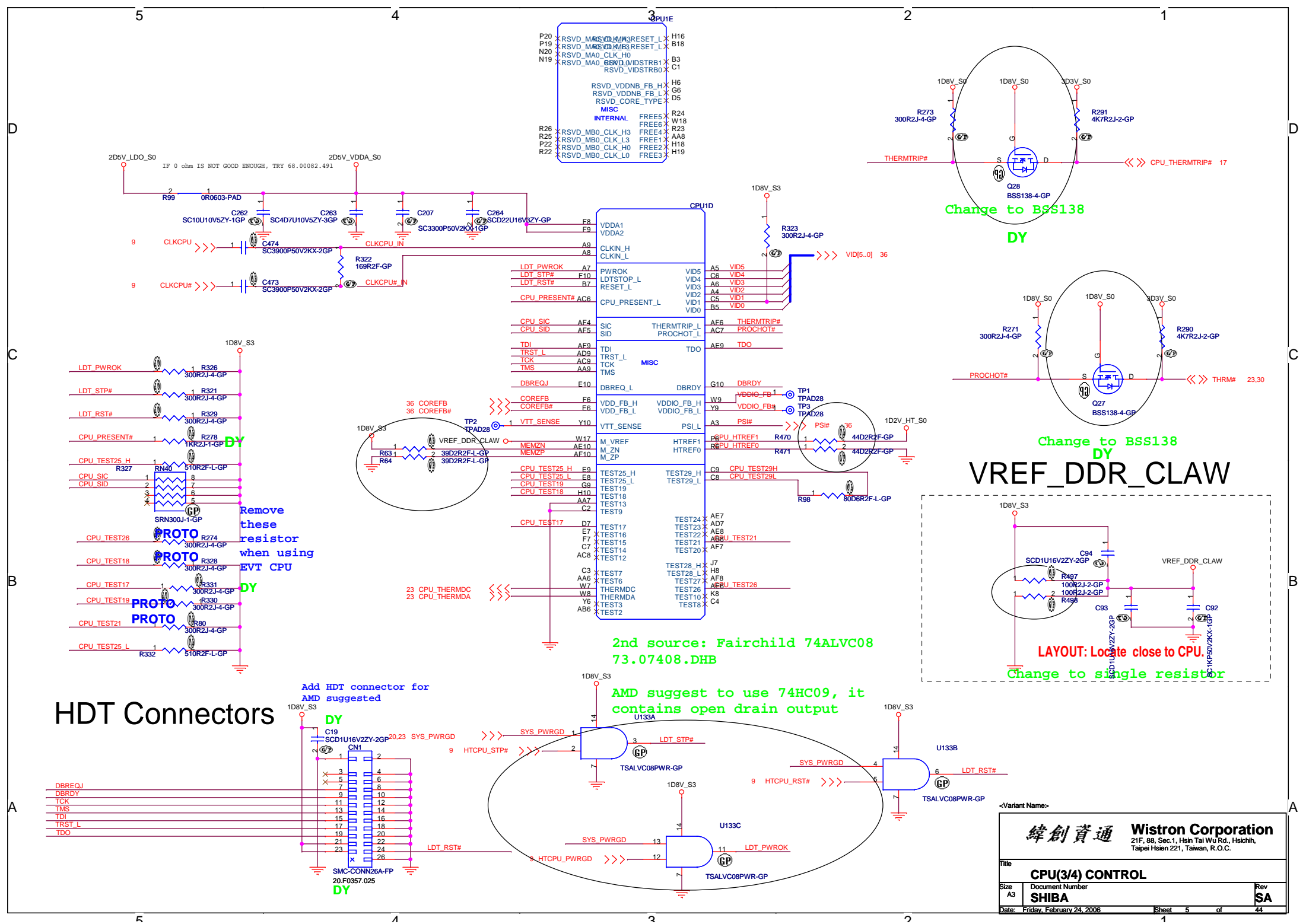
<b>緯創資通 Wistron Corporation</b>	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: <b>Block Diagram(FF+)</b>	
Size: A3	Document Number: <b>SHIBA</b>
Date: Monday, October 31, 2005	Rev: <b>SA</b>
Sheet 2 of 44	1





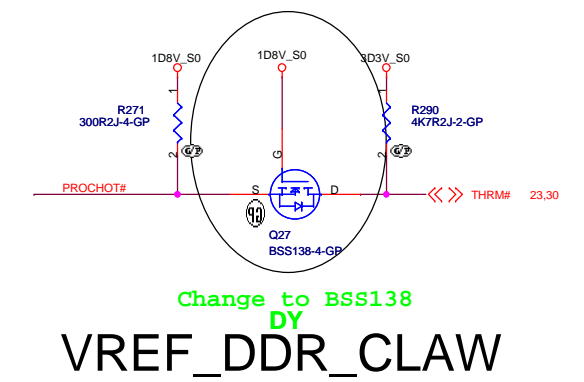
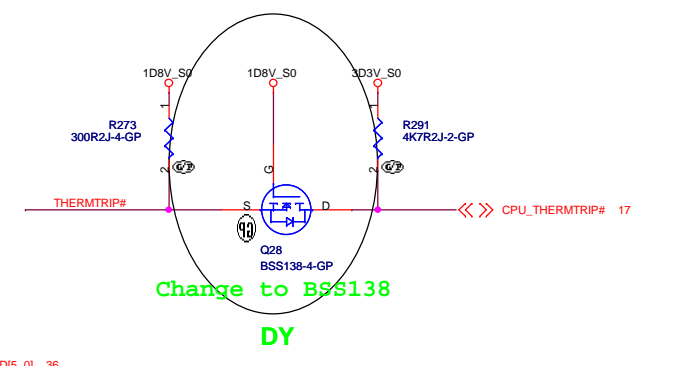
<Variant Name>

<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
<b>Title</b> <b>CPU(2/4) DDR II</b>		
<b>Size</b>	<b>Document Number</b>	<b>Rev</b>
A3	SHIBA	SC
Date: Friday, February 24, 2006		Sheet 4 of 44



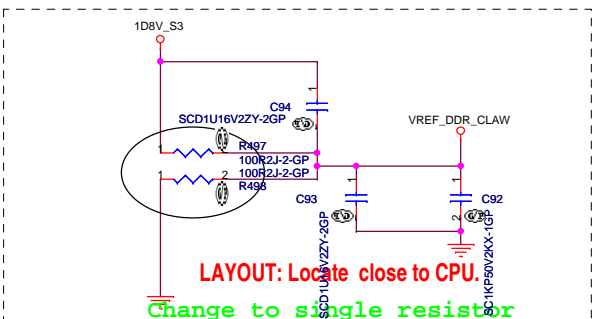
Pin List for CPU1E:

P20	RSVD_MAO_VDDH0	W3	RESET_L_X	H16
P19	RSVD_MAO_VDDH0	W3	RESET_L_X	B18
N20	RSVD_MAO_CLK_H0			B3
N19	RSVD_MAO_BSWD0	VIDSTRB1_X		C1
			RSVD_VIDSTRB0_X	
	RSVD_VDDNB_FB_H_X			H6
	RSVD_VDDNB_FB_L_X			G6
	RSVD_CORE_TYPE			D5
	MISC			
	INTERNAL	FREE5_X		R24
		FREE6_X		W18
R26	RSVD_MBO_CLK_H3	FREE4_X		R23
R25	RSVD_MBO_CLK_L3	FREE1_X		AA8
P22	RSVD_MBO_CLK_H0	FREE2_X		H18
R22	RSVD_MBO_CLK_L0	FREE3_X		H19



Change to BSS138  
DY

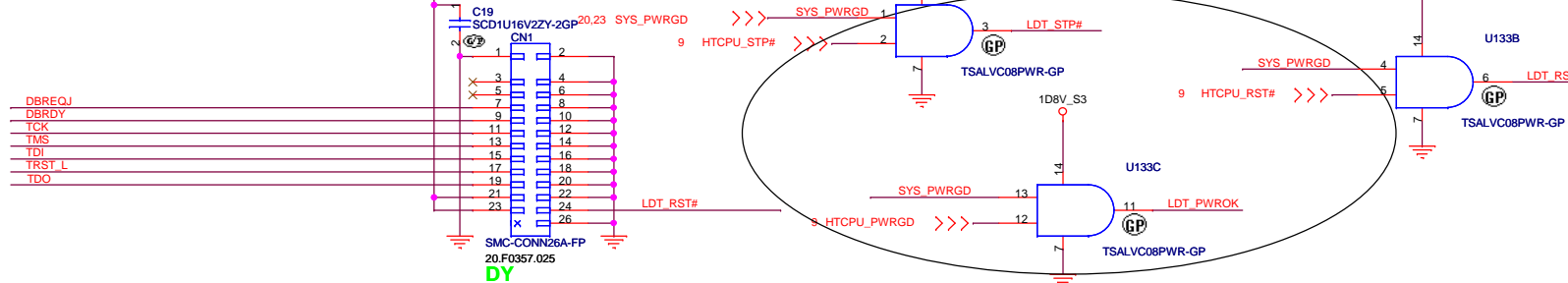
VREF\_DDR\_CLAW



2nd source: Fairchild 74ALVC08  
73.07408.DHB

AMD suggest to use 74HC09, it  
contains open drain output

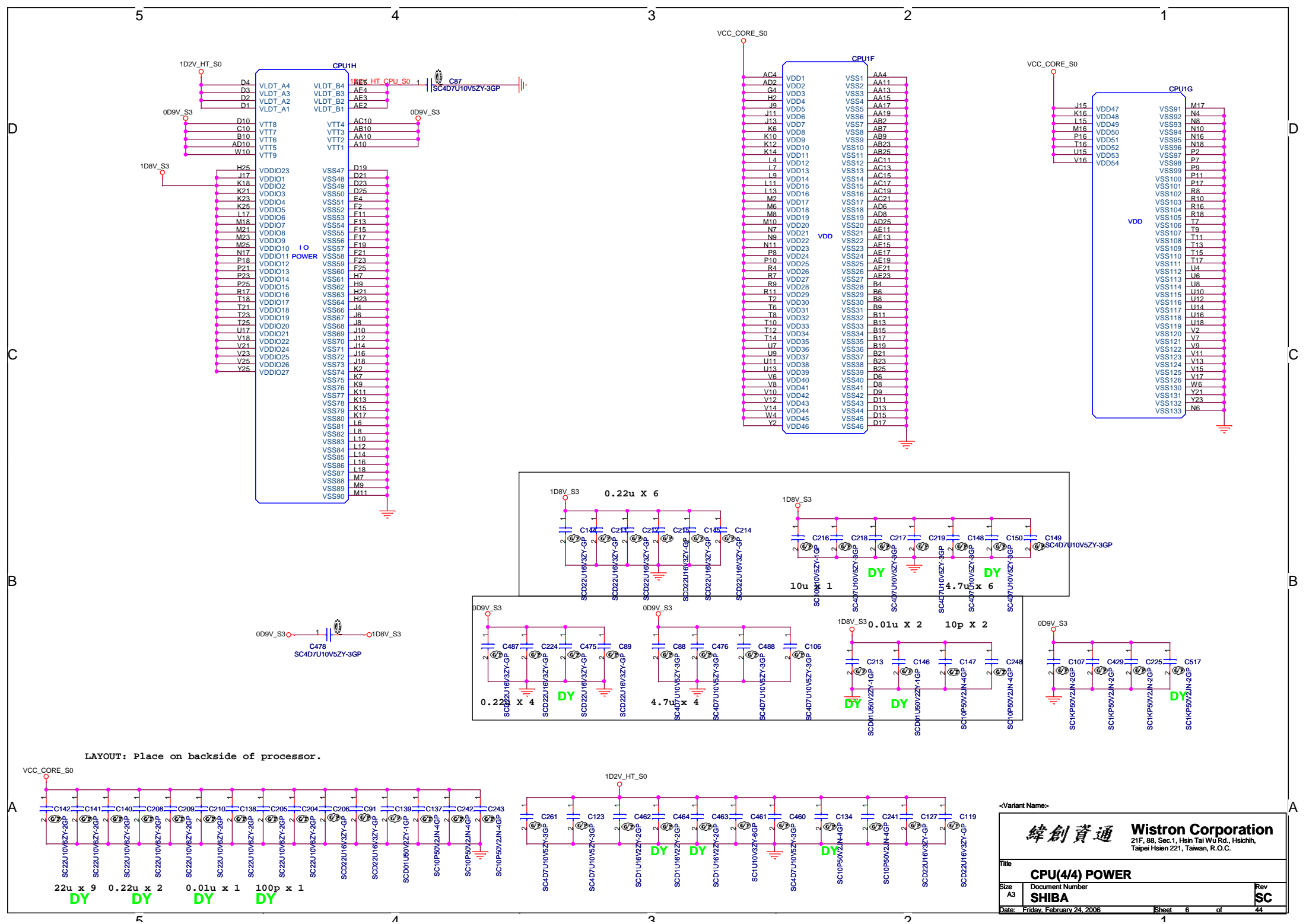
# HDT Connectors



緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(3/4) CONTROL

Size A3	Document Number SHIBA	Rev SA
Date: Friday, February 24, 2006	Sheet 5 of 44	



LAYOUT: Place on backside of processor.

<Variant Name>

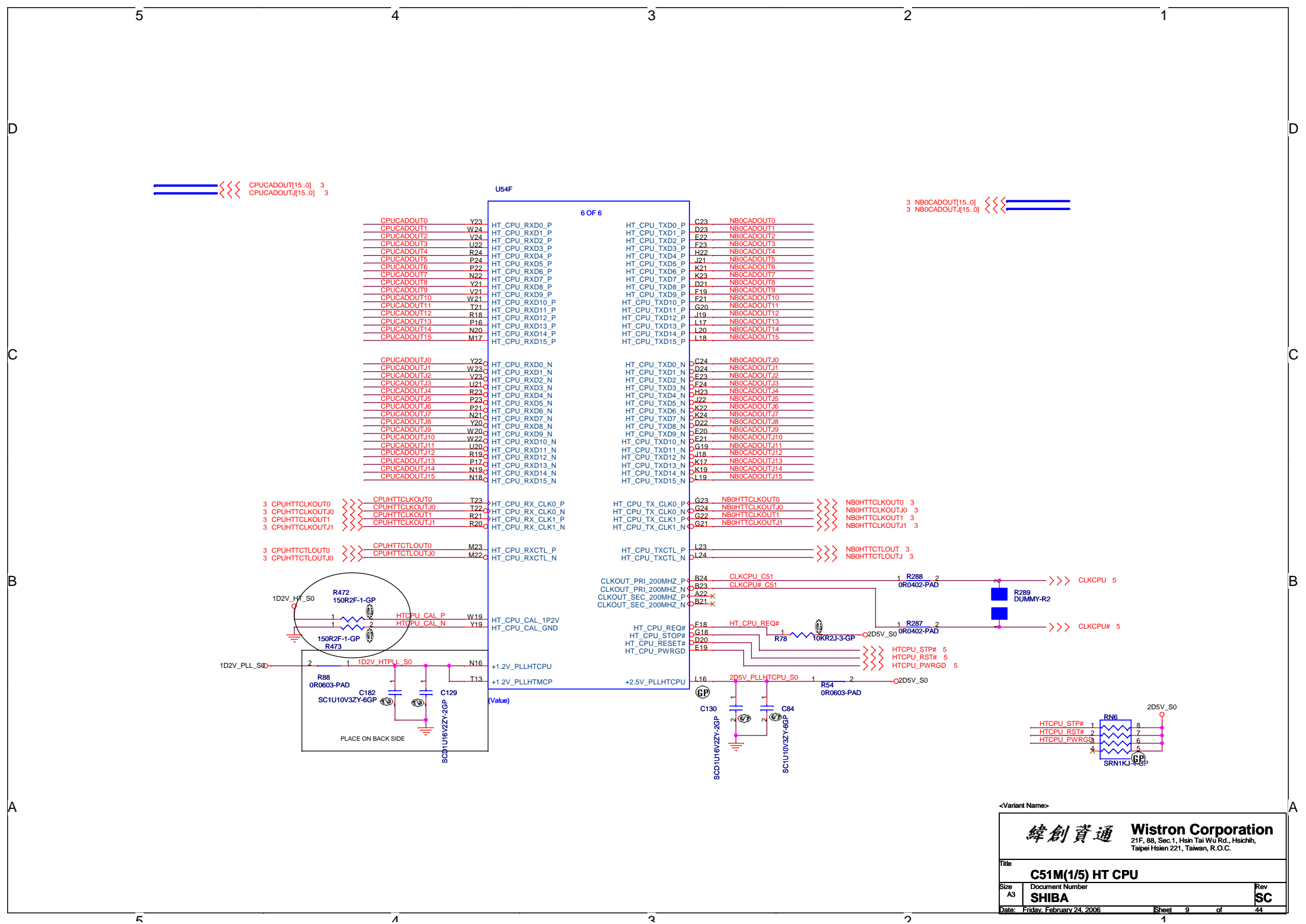
**緯創資通** **Wistron Corporation**  
 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title		<b>CPU(4/4) POWER</b>	
Size	Document Number	Rev	
A3	<b>SHIBA</b>	<b>SC</b>	
Date: Friday, February 24, 2006	Sheet 6	of 44	



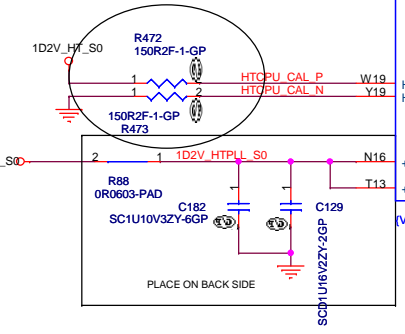






CPUCADOUT[15..0] 3  
 CPUCADOUTJ[15..0] 3

NB0CADOUT[15..0] 3  
 NB0CADOUTJ[15..0] 3



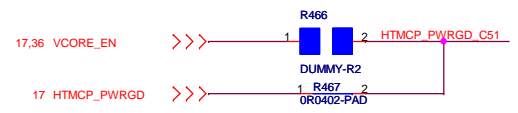
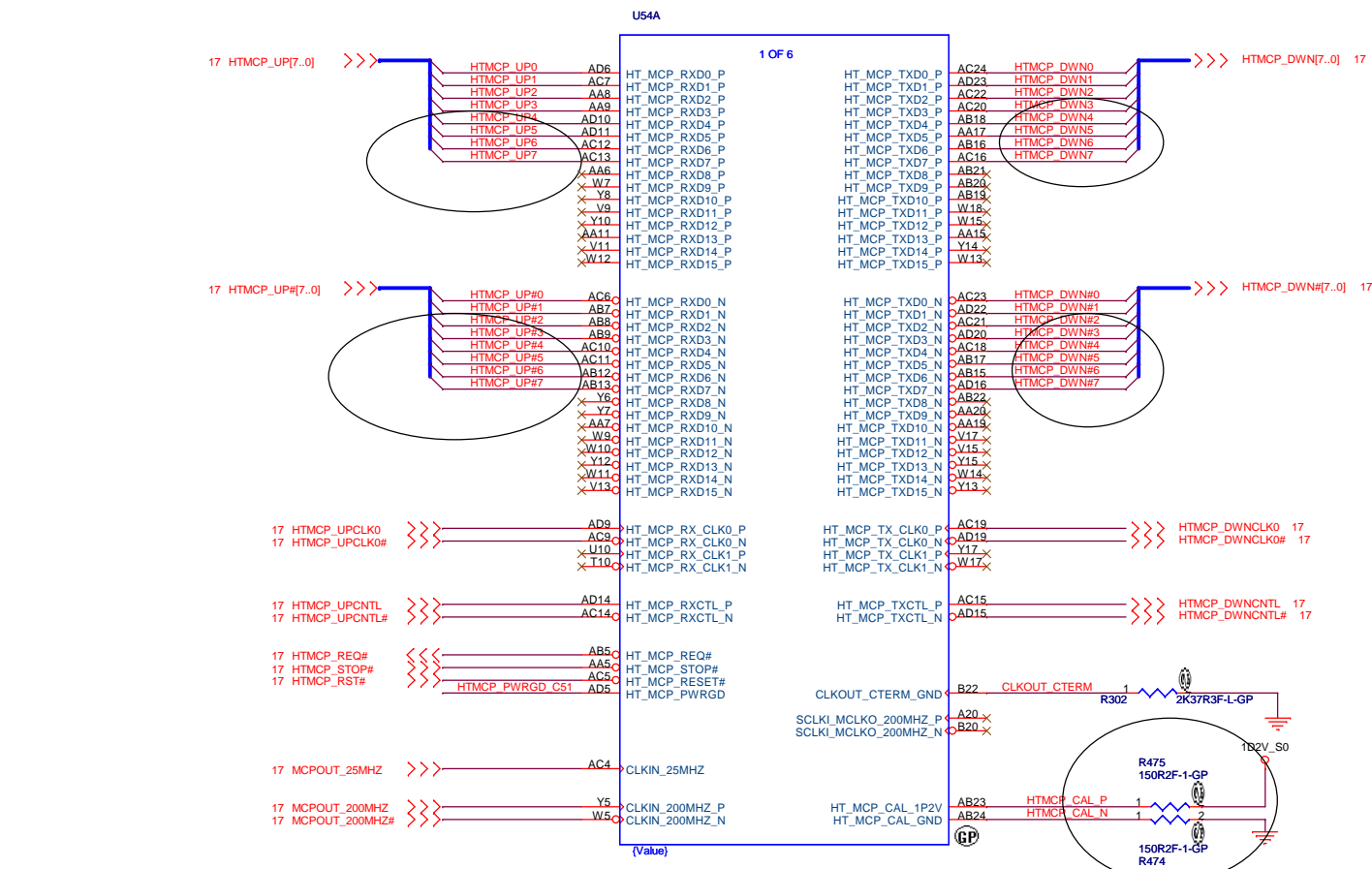
<Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **C51M(1/5) HT CPU**

Size	Document Number	Rev
A3	SHIBA	SC

Date: Friday, February 24, 2006 Sheet 9 of 44

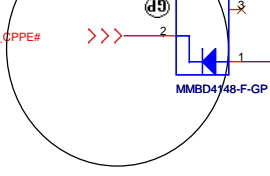


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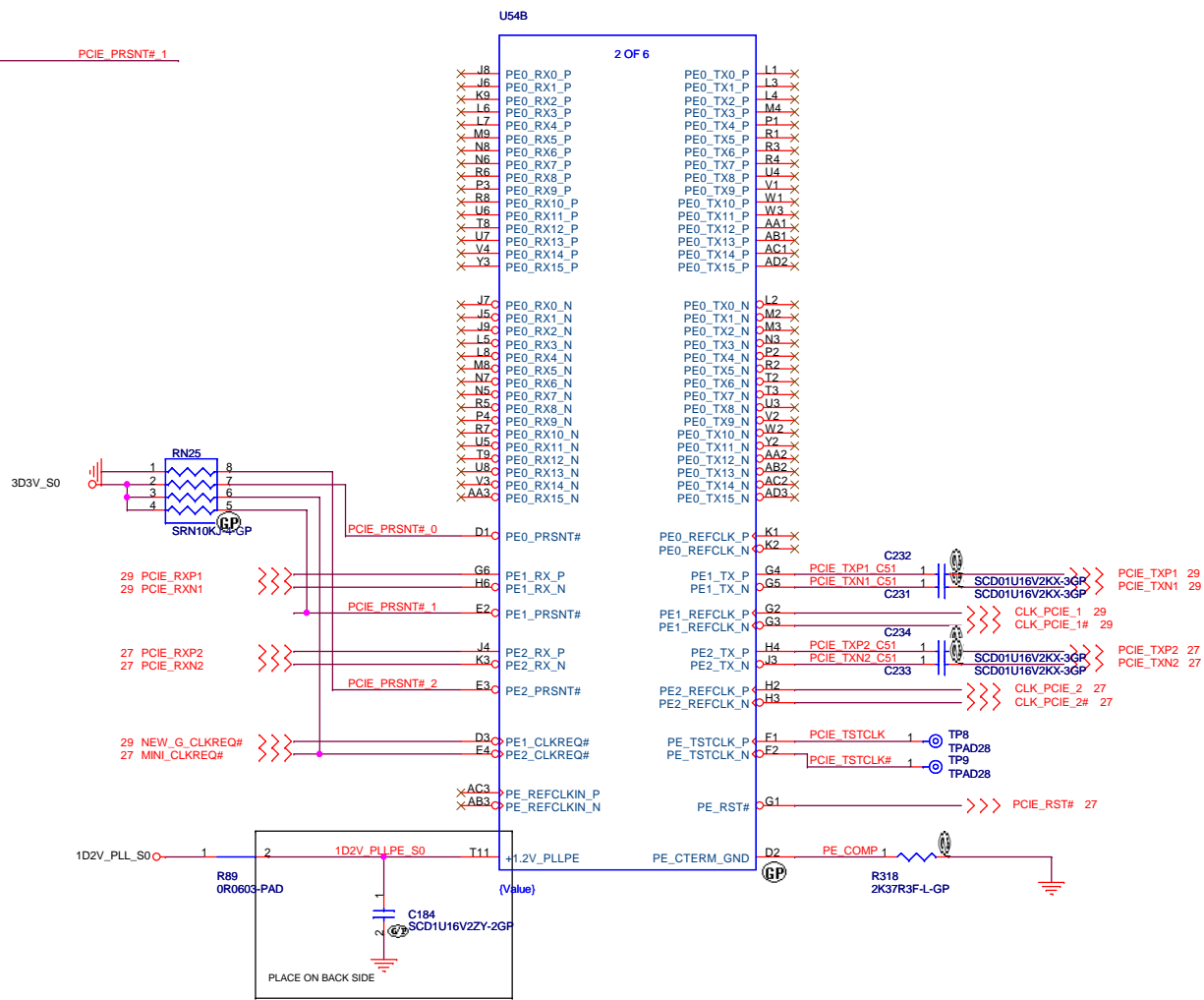
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **C51M(2/5)HT MCP**

Size: A3	Document Number: <b>SHIBA</b>	Rev: <b>SC</b>
Date: Friday, February 24, 2006	Sheet: 10	of 44

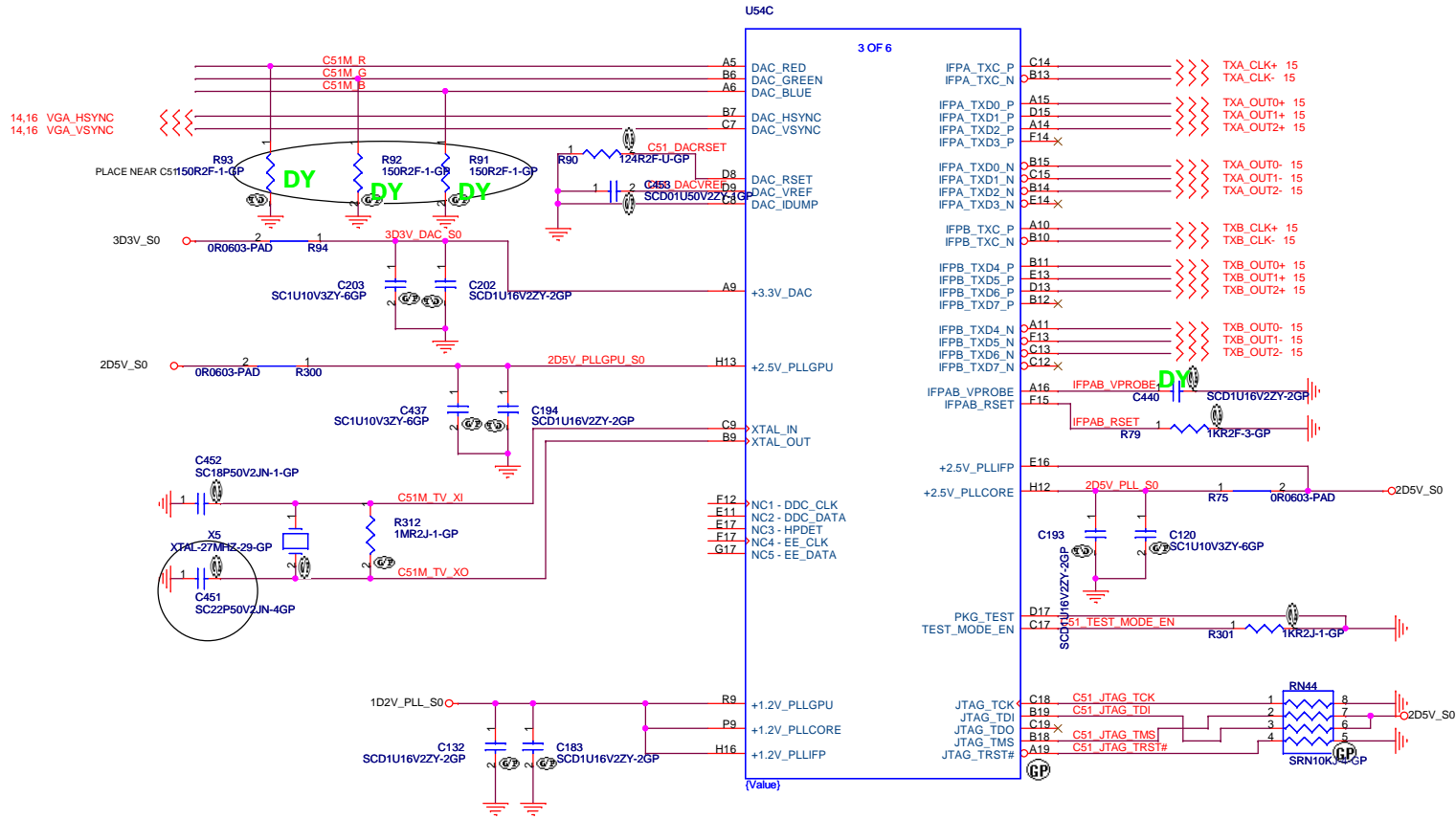


CHECK LEAKAGE CURRENT

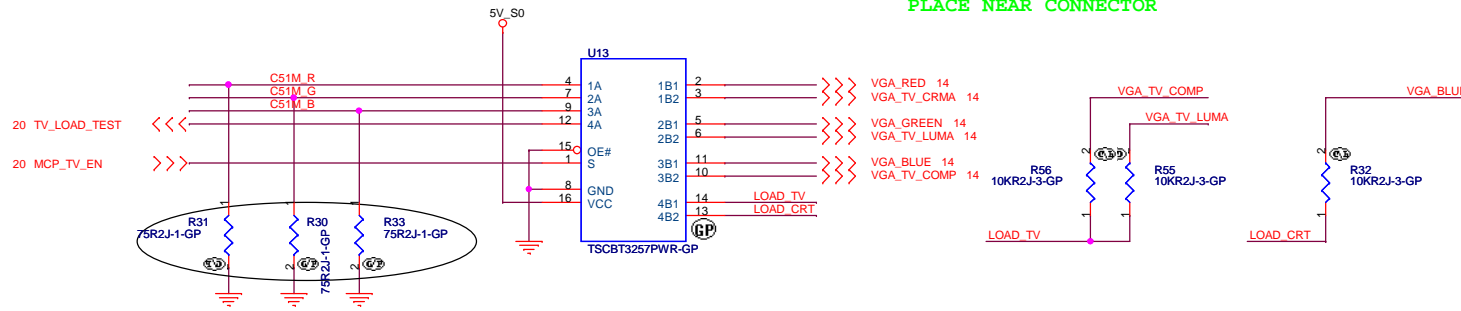


<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b>			
<b>C51M(3/5)PCIE</b>			
Size	Document Number	Rev	
A3	<b>SHIBA</b>	<b>SA</b>	
Date:	Monday, February 27, 2006	Sheet	11 of 44



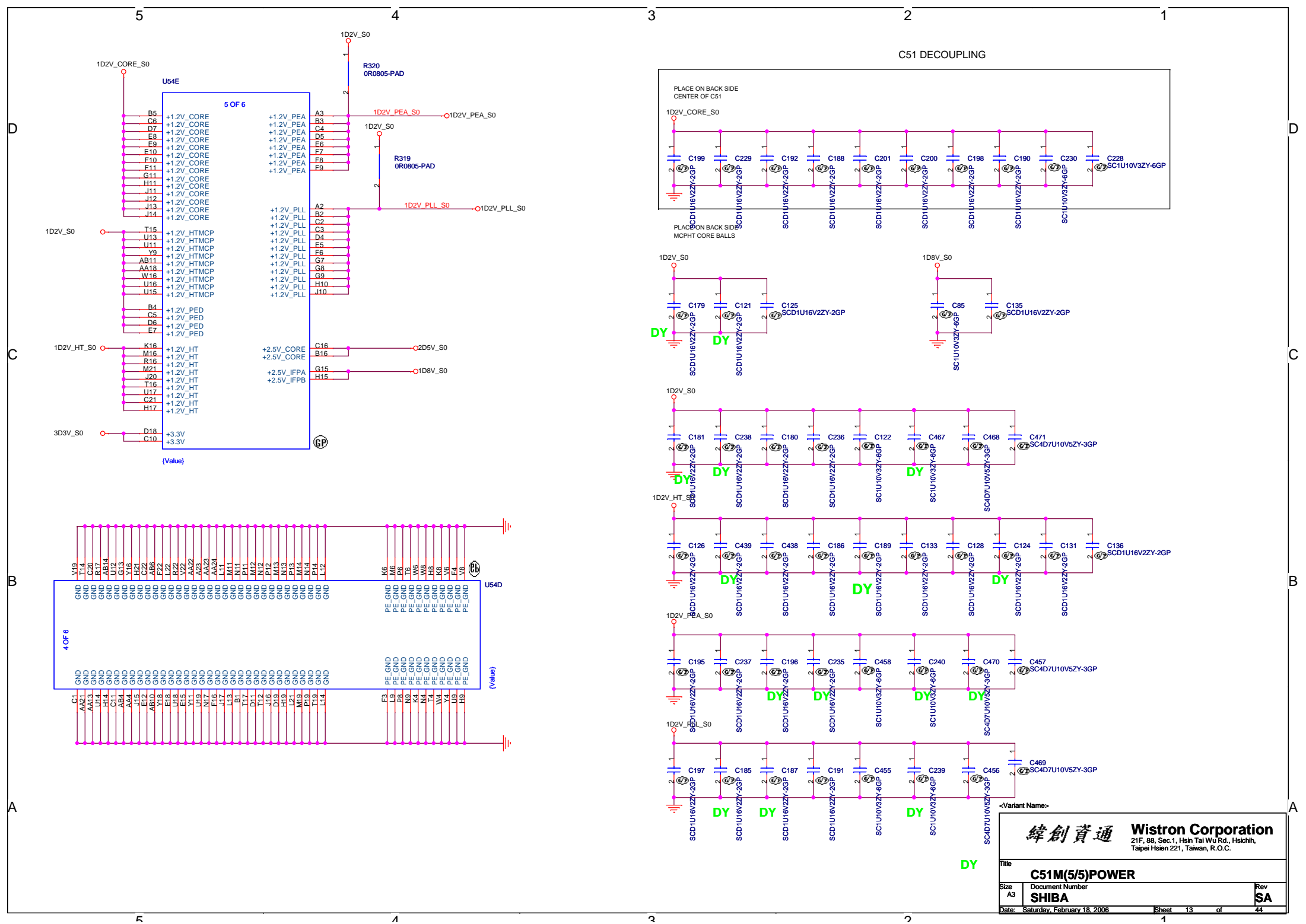
PLACE NEAR CONNECTOR



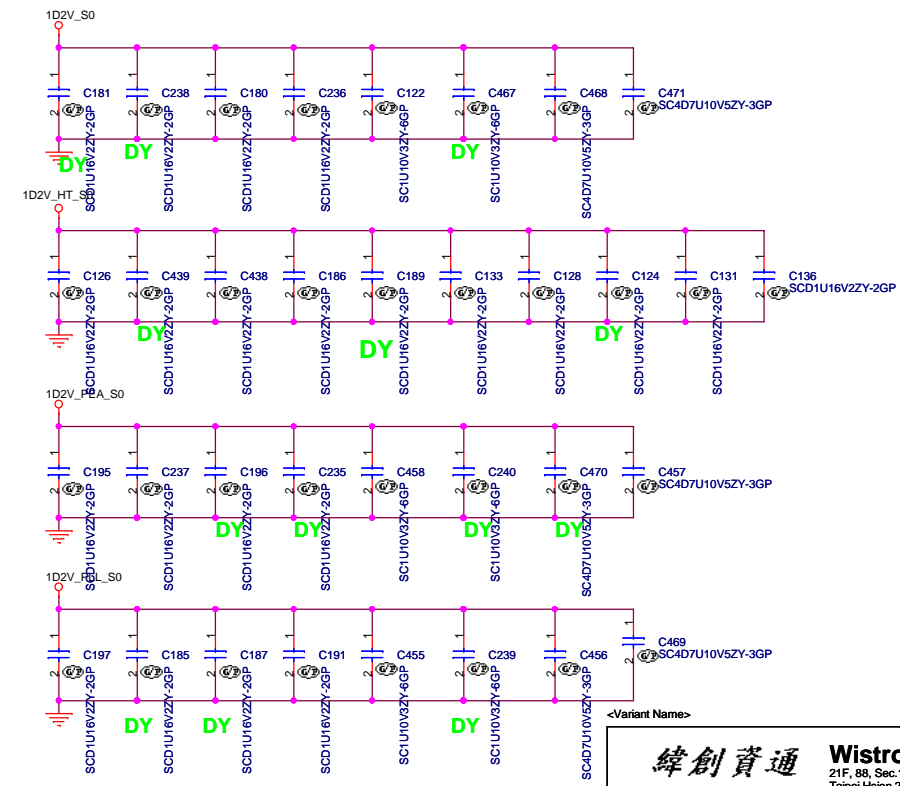
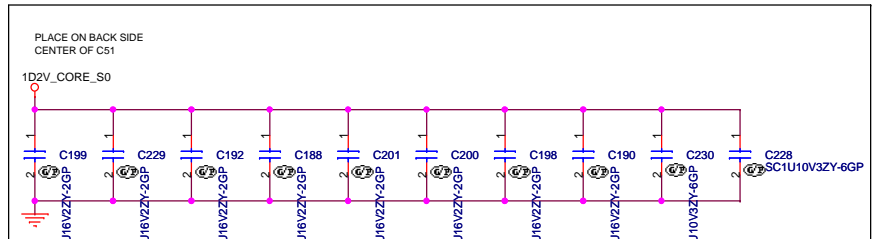
<Variant Name>

**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title <b>C51M(4/5)CRT/LVDS</b>		
Size A3	Document Number <b>SHIBA</b>	Rev <b>SA</b>
Date: Wednesday, March 15, 2006	Sheet 12 of 44	



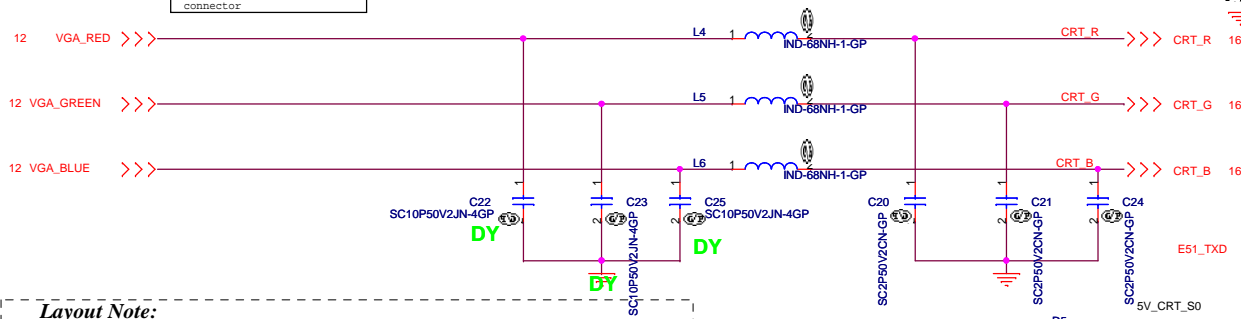
C51 DECOUPLING



<p><b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
<p>Title: <b>C51M(5/5)POWER</b></p>		
Size: A3	Document Number: <b>SHIBA</b>	Rev: <b>SA</b>
Date: Saturday, February 18, 2006	Sheet: 13 of 44	

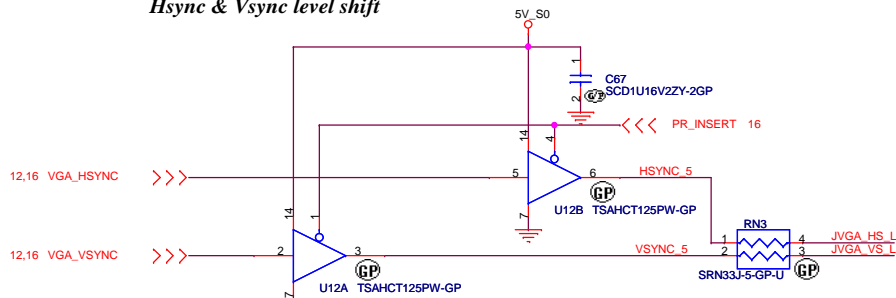
# CRT I/F & CONNECTOR

Layout Note:  
Place these resistors  
close to the CRT-out  
connector



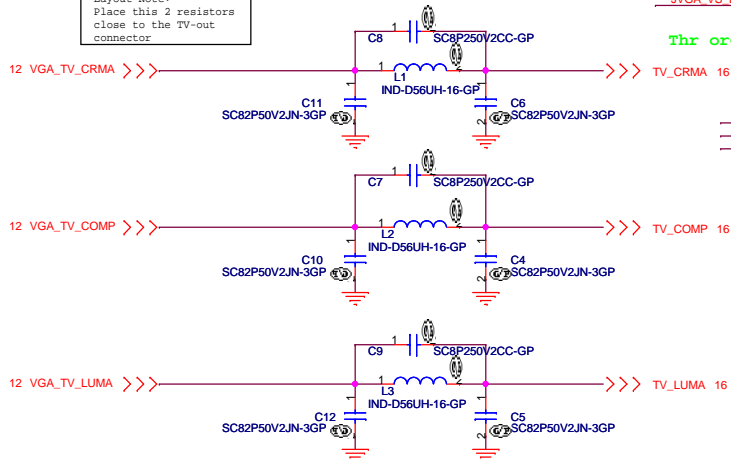
**Layout Note:**  
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

## Hsync & Vsync level shift

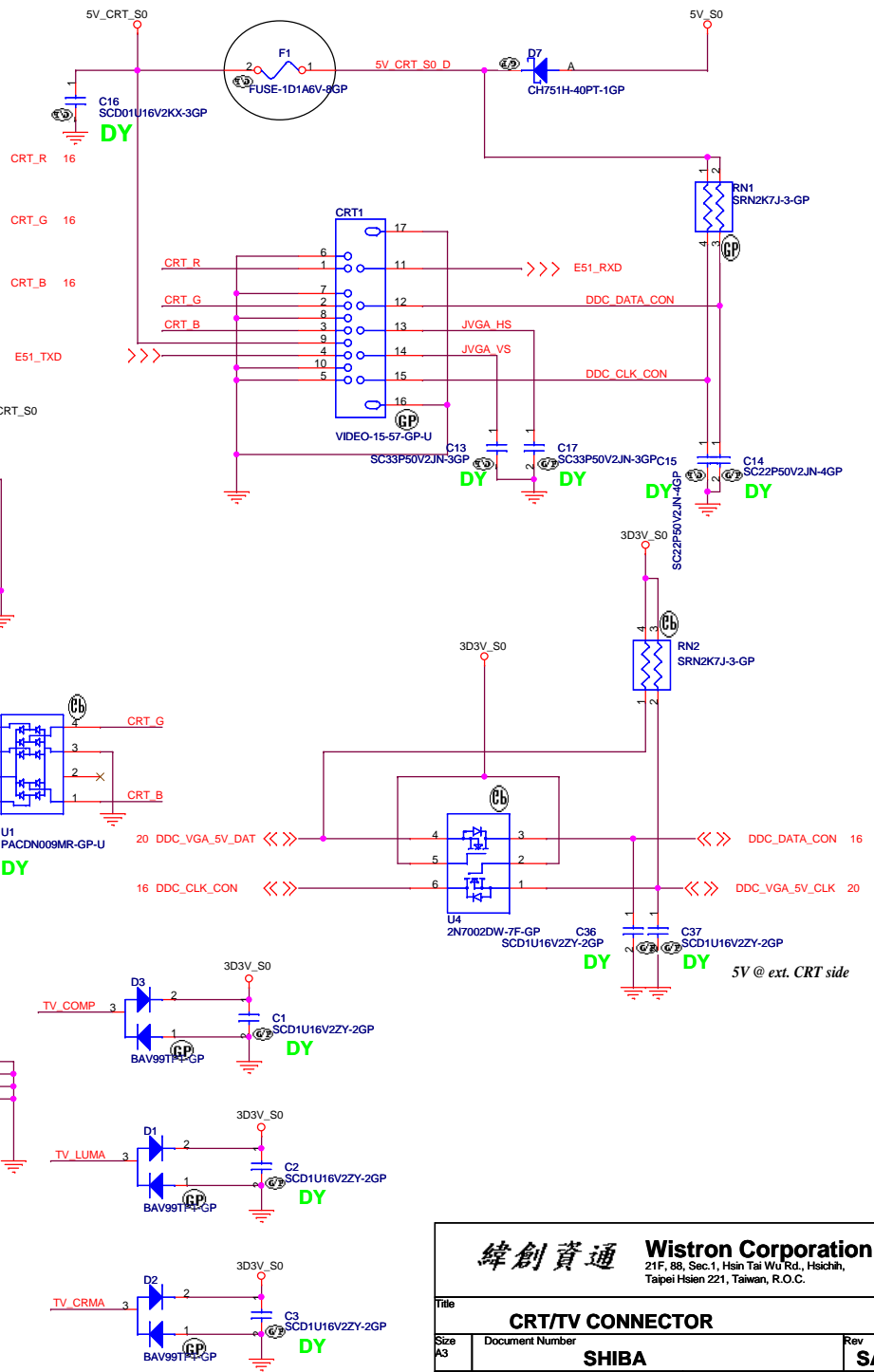
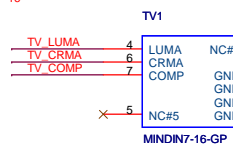


## TV OUT CONN

Layout Note:  
Place this 2 resistors  
close to the TV-out  
connector

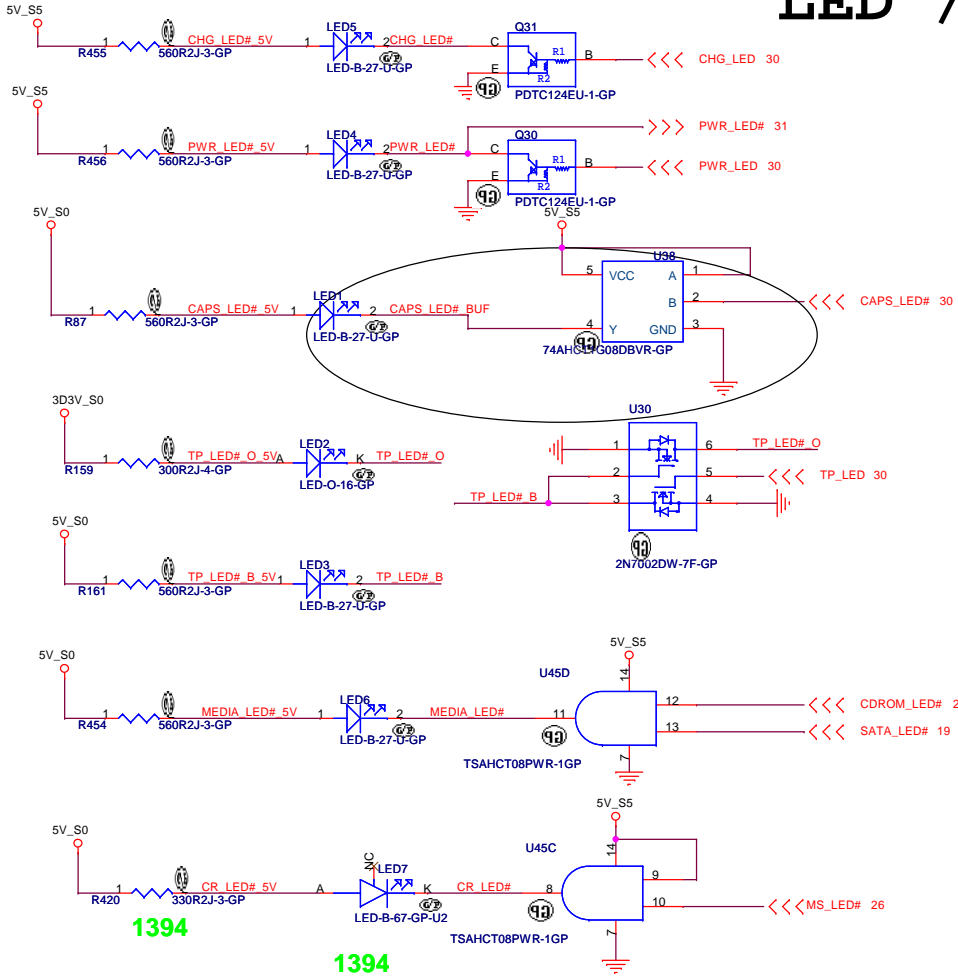


JVGA HS L 1 2 JVGA HS  
0R0402-PAD  
JVGA VS L 1 2 JVGA VS  
0R0402-PAD  
Thr org part is 68.2703N.10B

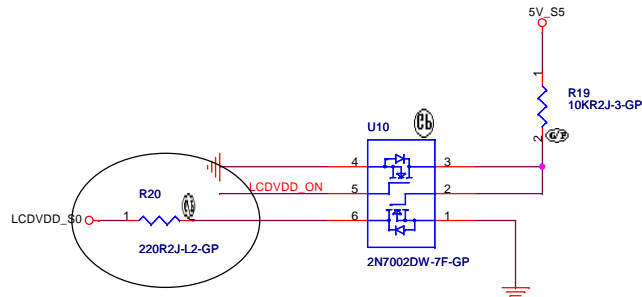
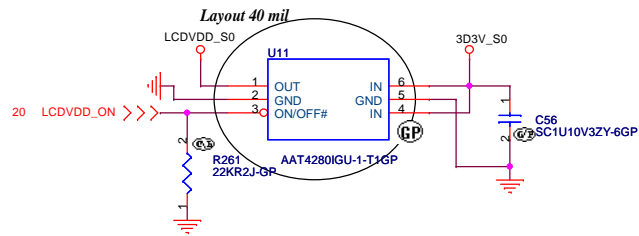
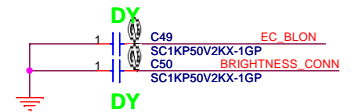
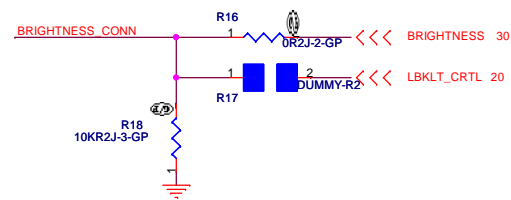
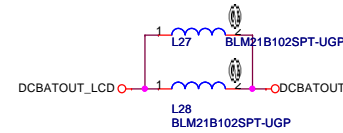
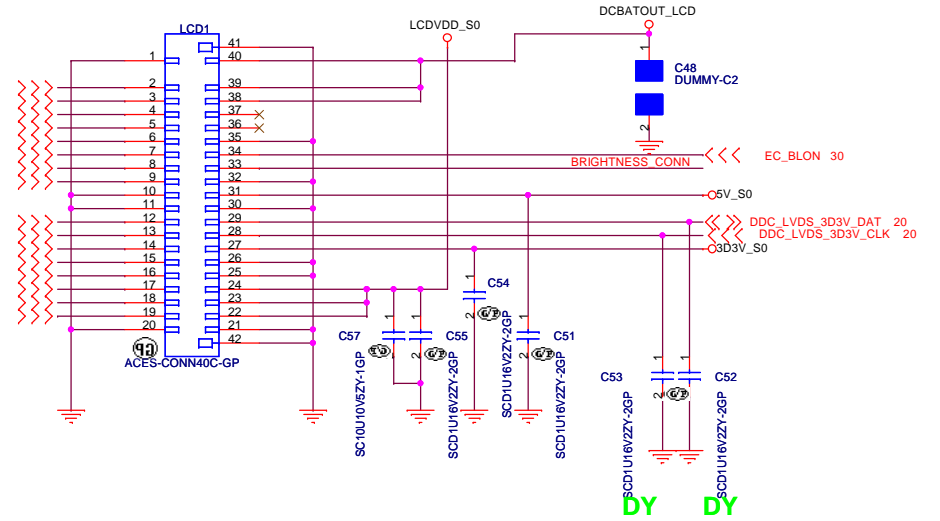


<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>CRT/TV CONNECTOR</b>			
Size A3	Document Number <b>SHIBA</b>	Rev <b>SA</b>	
Date: Thursday, February 23, 2006		Sheet 14	of 44

# LED / INVERTER INTERFACE



- 12 TXB\_OUT2+
- 12 TXB\_OUT2-
- 12 TXB\_OUT1+
- 12 TXB\_OUT1-
- 12 TXB\_OUT0+
- 12 TXB\_OUT0-
- 12 TXB\_CLK+
- 12 TXB\_CLK-
- 12 TXA\_OUT2+
- 12 TXA\_OUT2-
- 12 TXA\_OUT1+
- 12 TXA\_OUT1-
- 12 TXA\_OUT0+
- 12 TXA\_OUT0-
- 12 TXA\_CLK+
- 12 TXA\_CLK-



<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
<b>LCD/Inverter Connector</b>			
Title	Document Number	Rev	
Size Custom	<b>SHIBA</b>	<b>SA</b>	
Date: Friday, February 24, 2006	Sheet 15 of 44		





D

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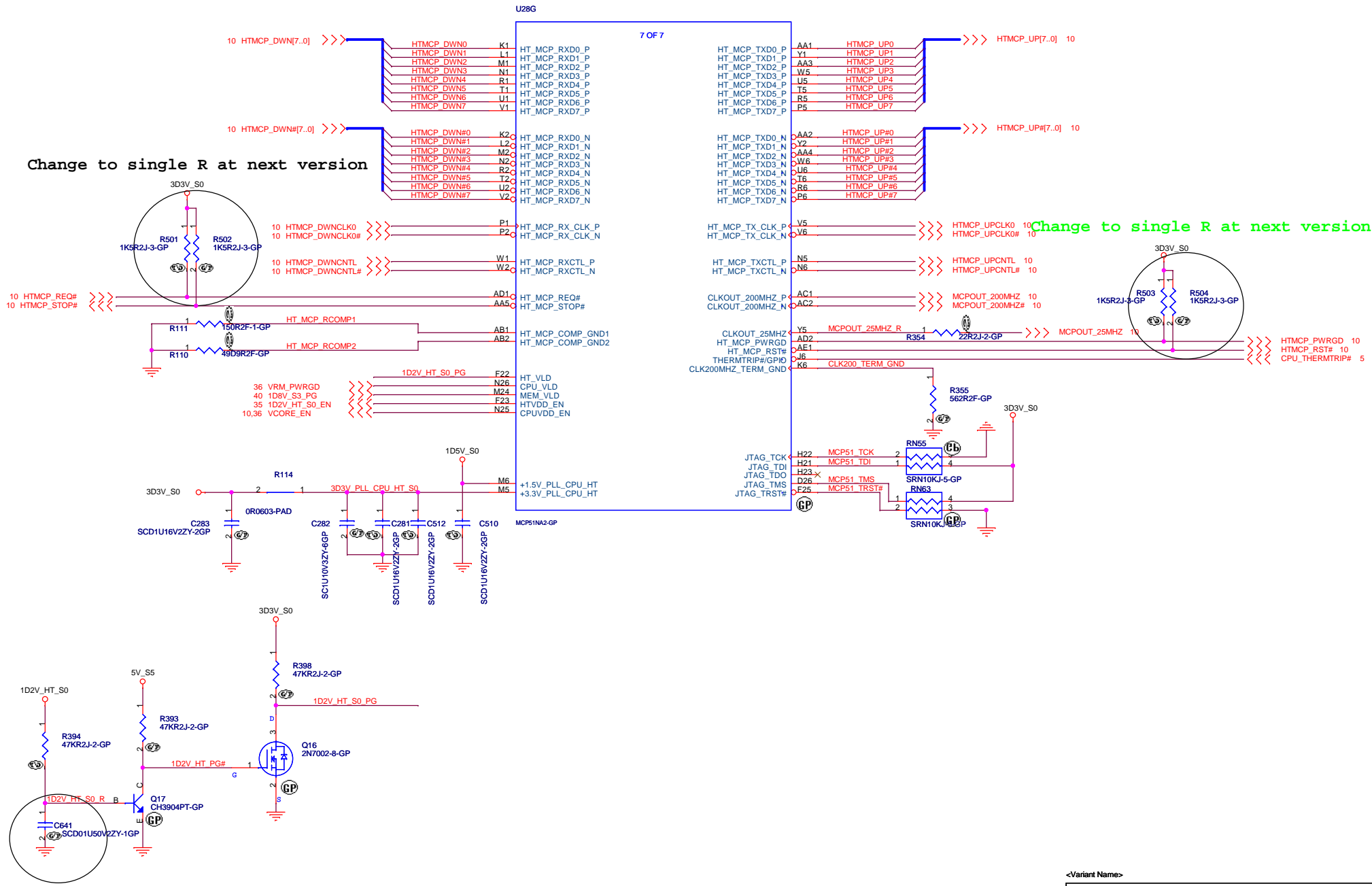
C

B

B

A

A



<Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title <b>MCP51(1/6)HT</b>		
Size A3	Document Number <b>SHIBA</b>	Rev <b>SA</b>
Date: Monday, February 20, 2006	Sheet 17 of 44	

D

25 PCI\_AD[0..31] <<<>>

25 PCI\_C/BE#0 <<<>> AD19 PCI\_CBE#0  
 25 PCI\_C/BE#1 <<<>> AB17 PCI\_CBE#1  
 25 PCI\_C/BE#2 <<<>> AA15 PCI\_CBE#2  
 25 PCI\_C/BE#3 <<<>> AA13 PCI\_CBE#3

25 PCI\_FRAME# <<<>> AC15 PCI\_FRAME#  
 25 PCI\_IRDY# <<<>> AD15 PCI\_IRDY#  
 25 PCI\_TRDY# <<<>> AB16 PCI\_TRDY#  
 25 PCI\_STOP# <<<>> AE16 PCI\_STOP#  
 25 PCI\_DEVSEL# <<<>> AA19 PCI\_DEVSEL#  
 25 PCI\_PAR <<<>> AE17 PCI\_PAR  
 25 PCI\_PERR# <<<>> AF16 PCI\_PERR#/GPIO  
 25 PCI\_SERR# <<<>> AF17 PCI\_SERR#  
 25.30 PM\_CLKRUN# <<<>> AD11 PCI\_PME#/GPIO  
 AF25 PCI\_CLKRUN#/GPIO

25 PCIRST# <<<>> R388 22R2J-2-GP PCIRST# R AE25 PCI\_RESET#0  
 24 PCIRST#\_IDE <<<>> R389 22R2J-2-GP PCIRST#\_IDE R AD24 PCI\_RESET#1  
 29 PCIRST#\_NEW <<<>> R167 22R2J-2-GP PCIRST#\_NEW R AE26 PCI\_RESET#2  
 30,31 LPC\_RST# <<<>> R199 22R2J-2-GP LPC\_RST# R L26 PCI\_RESET#3

U28A

1 OF 7

PCI_AD0	AF19	PCI_AD0
PCI_AD1	AB21	PCI_AD1
PCI_AD2	AC19	PCI_AD2
PCI_AD3	AA20	PCI_AD3
PCI_AD4	AA19	PCI_AD4
PCI_AD5	AE20	PCI_AD5
PCI_AD6	AE19	PCI_AD6
PCI_AD7	AE20	PCI_AD7
PCI_AD8	AB20	PCI_AD8
PCI_AD9	AB19	PCI_AD9
PCI_AD10	AA18	PCI_AD10
PCI_AD11	AB18	PCI_AD11
PCI_AD12	AE18	PCI_AD12
PCI_AD13	AF18	PCI_AD13
PCI_AD14	AC17	PCI_AD14
PCI_AD15	AA17	PCI_AD15
PCI_AD16	AB15	PCI_AD16
PCI_AD17	AE15	PCI_AD17
PCI_AD18	AE15	PCI_AD18
PCI_AD19	AF14	PCI_AD19
PCI_AD20	AE14	PCI_AD20
PCI_AD21	AA14	PCI_AD21
PCI_AD22	AB14	PCI_AD22
PCI_AD23	AC13	PCI_AD23
PCI_AD24	AB13	PCI_AD24
PCI_AD25	AE13	PCI_AD25
PCI_AD26	AF13	PCI_AD26
PCI_AD27	AA12	PCI_AD27
PCI_AD28	AB12	PCI_AD28
PCI_AD29	AE12	PCI_AD29
PCI_AD30	AE12	PCI_AD30
PCI_AD31	AF11	PCI_AD31

MCP51NA2-GP

PCI\_REQ#0 <<<>> AA22 PCI\_REQ#0 <<<>> PCI\_REQ#0 25  
 AE22 PCI\_REQ#1  
 PCI\_REQ#2 <<<>> AF21 PCI\_REQ#2  
 AE22 PCI\_REQ#3  
 AE23 PCI\_REQ#4

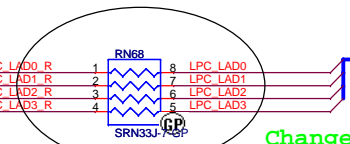
PCI\_GNT#0 <<<>> AE21 PCI\_GNT#0 <<<>> PCI\_GNT#0 25  
 AC21  
 PCI\_GNT#1 <<<>> AA21  
 PCI\_GNT#2 <<<>> AB24  
 PCI\_GNT#3/GPIO <<<>> AB24  
 PCI\_GNT#4/GPIO <<<>> AB24

PCI\_INTW# <<<>> AE11 PCI\_INTW# <<<>> PCI\_INTW# 25  
 PCI\_INTX# <<<>> AB11 PCI\_INTX# <<<>> PCI\_INTX# 25  
 PCI\_INTY# <<<>> AC11 PCI\_INTY#  
 PCI\_INTZ# <<<>> AA11 PCI\_INTZ#

AE24 PCI\_CLK# R <<<>> PCI\_CLK# 25  
 R168 22R2J-2-GP

AC23 PCI\_CLKIN <<<>> PCI\_CLKIN  
 R375 22R2J-2-GP

1394

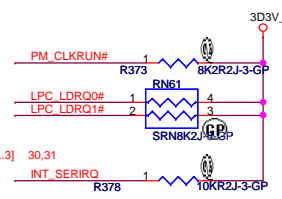
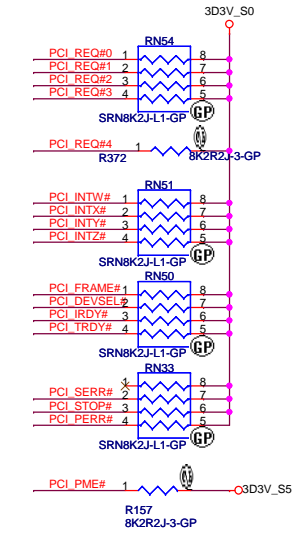


LPC\_FRAME# <<<>> G25 LPC\_LFRAME# 30,31  
 LPC\_DRQ#0 <<<>> K21 LPC\_LDRQ0#  
 LPC\_DRQ#1/LPC\_CS# <<<>> K23 LPC\_LDRQ1#  
 LPC\_SERIRQ <<<>> L22 INT\_SERIRQ 25,30

LPC\_PWRDWN#/GPIO <<<>> H24

LPC\_CLK#0 <<<>> F26 LPC\_CLK# R <<<>> LPC\_CLK# 30  
 R202 22R2J-2-GP

LPC\_CLK#1 <<<>> G26 PCI\_CLK1# R <<<>> PCI\_CLK# GOLD 31  
 R201 22R2J-2-GP



<Variant Name>

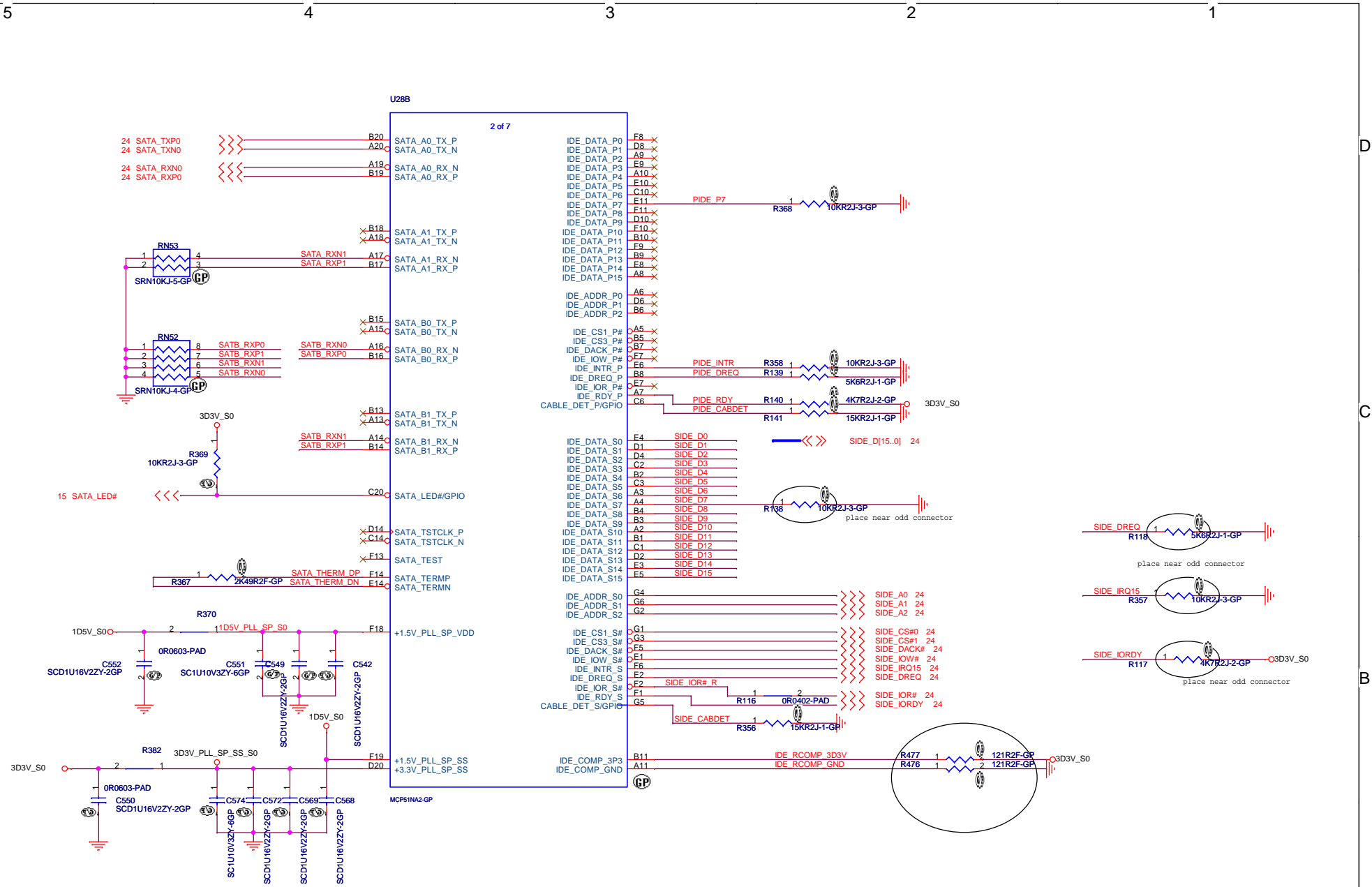
<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b>			
<b>MCP51(2/6)PCI</b>			
<b>Size</b>			
A3		Document Number	
SHIBA		SA	
Date: Monday, February 20, 2006		Sheet 18 of 44	

D

C

B

A



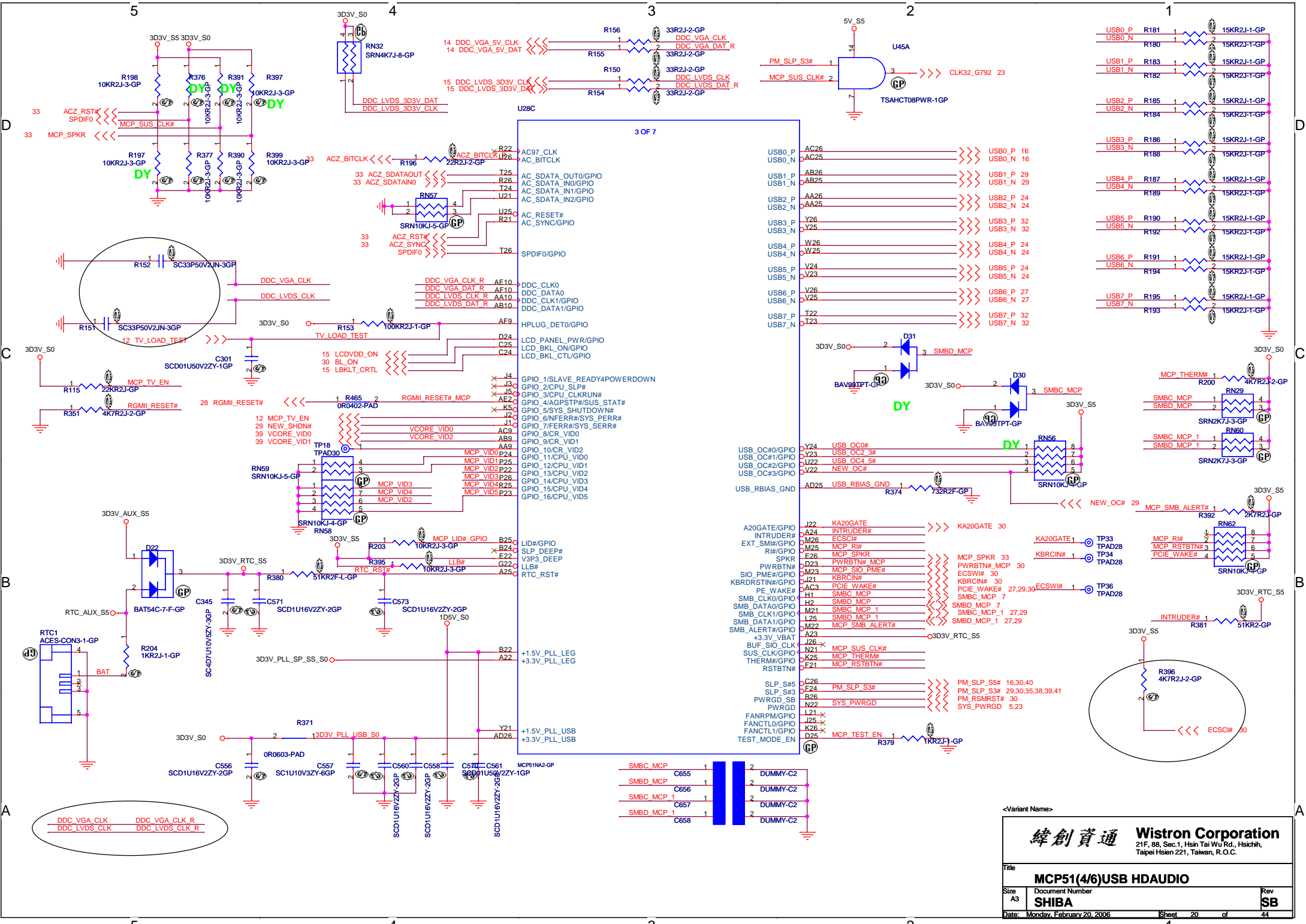
<Variant Name>

**緯創資通** **Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP51(3/6)SATA/PATA**

Size: A3  
 Document Number: **SHIBA**  
 Date: Monday, February 20, 2006

Rev: **SA**  
 Sheet: 19 of 44

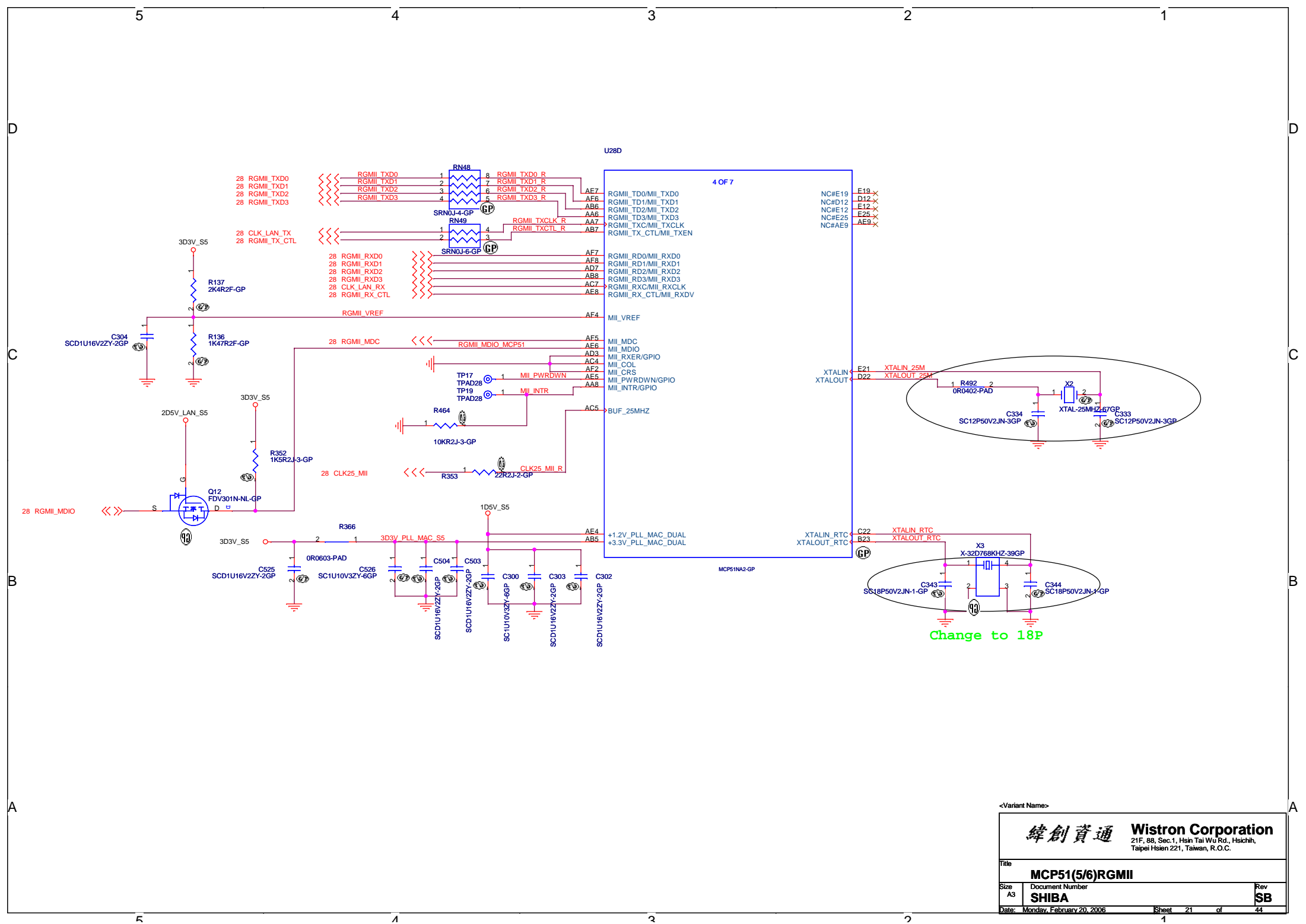


SMB_C MCP	1	2	DUMMY-C2
SMB_D MCP	1	2	DUMMY-C2
SMB_C MCP	1	2	DUMMY-C2
SMB_D MCP	1	2	DUMMY-C2

<Variant Name>

**緯創資通** **Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

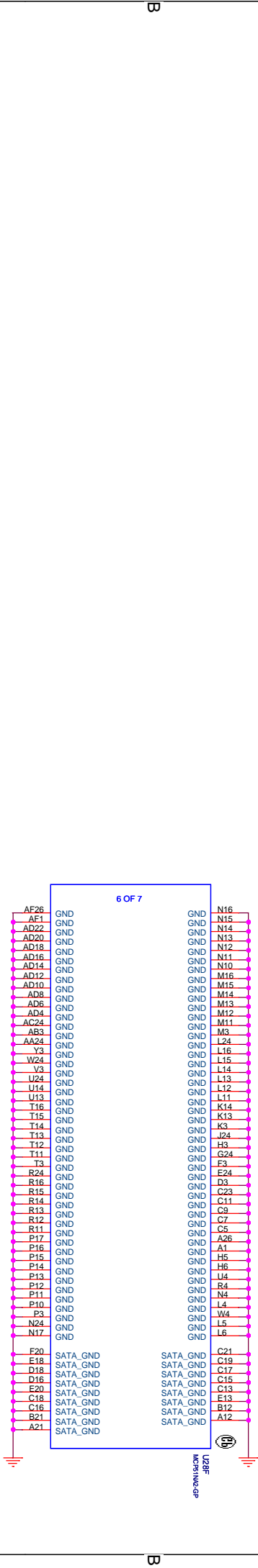
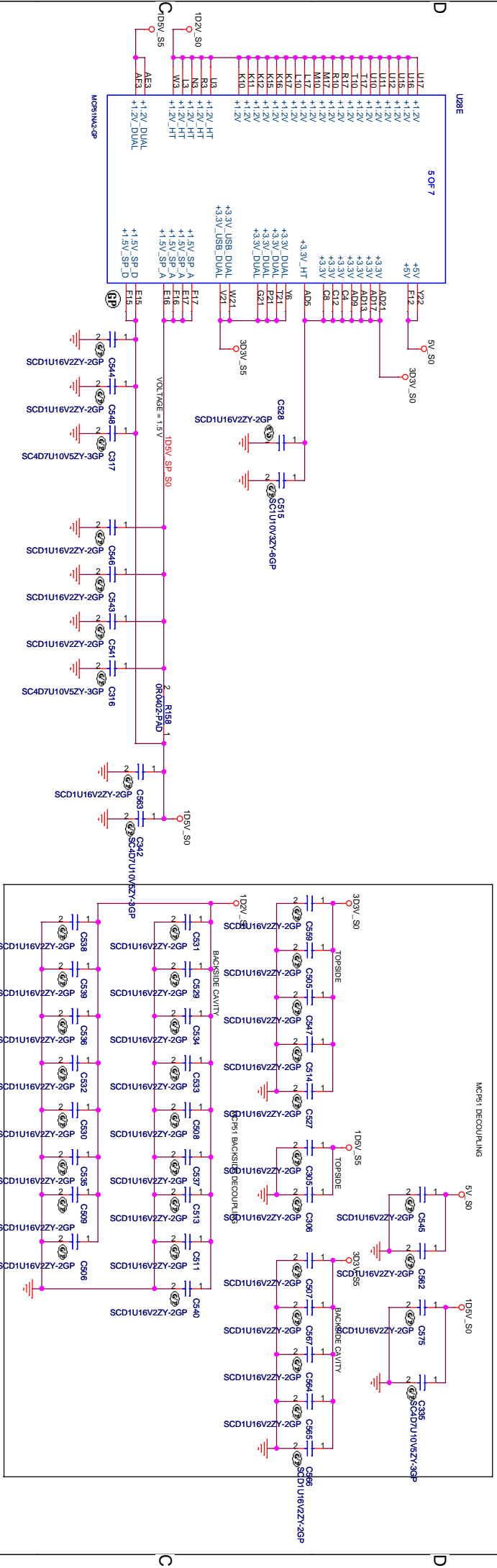
Title <b>MCP51(4/6)USB HDAUDIO</b>		
Size A3	Document Number <b>SHIBA</b>	Rev <b>SB</b>
Date: Monday, February 20, 2006	Sheet 20 of 44	



<Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title <b>MCP51(5/6)RGMII</b>		
Size A3	Document Number <b>SHIBA</b>	Rev <b>SB</b>
Date: Monday, February 20, 2006	Sheet 21	of 44



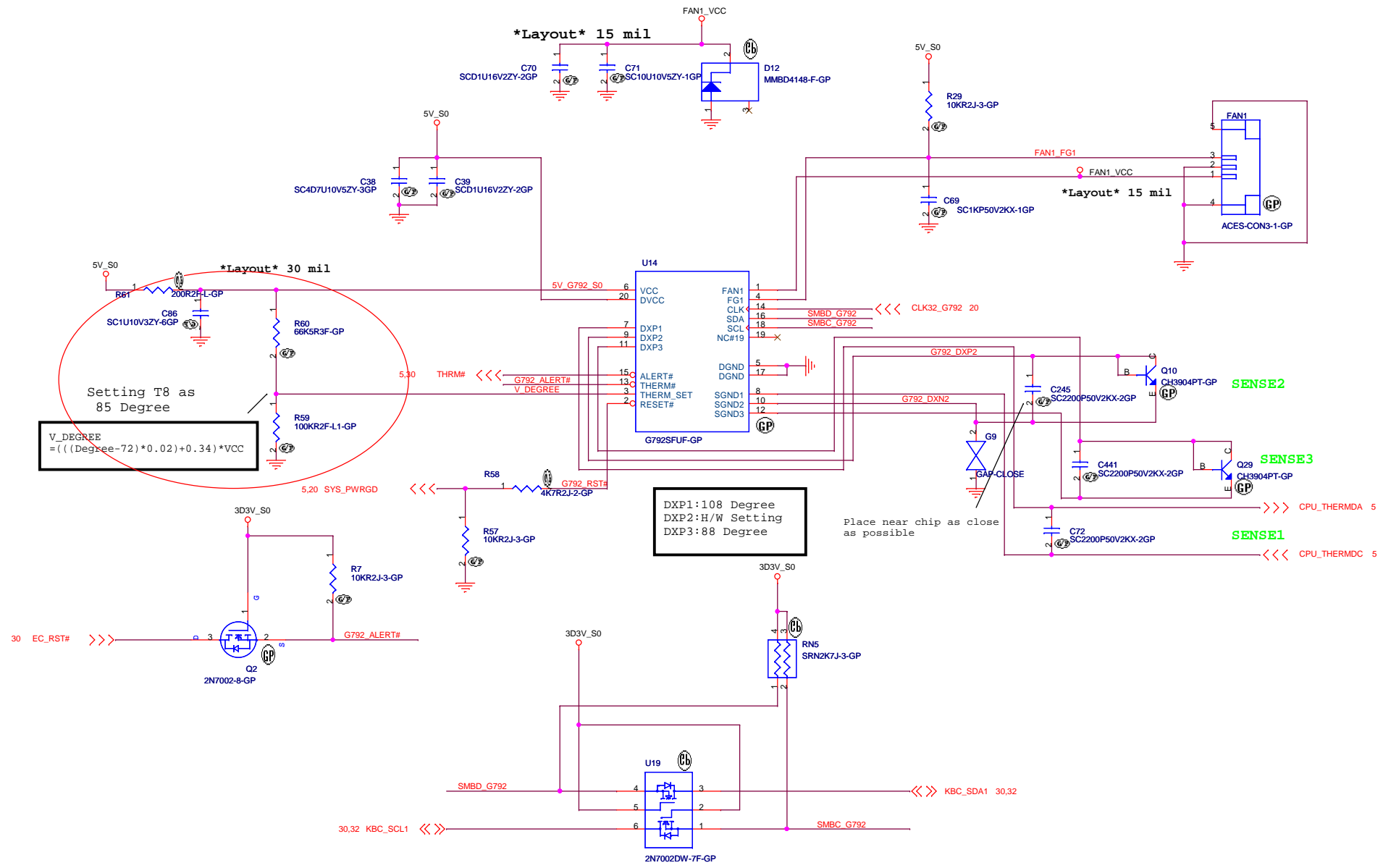
**Variant Names**

Title	MCP51(6)POWER
Document Number	SHIBA
Rev	SB

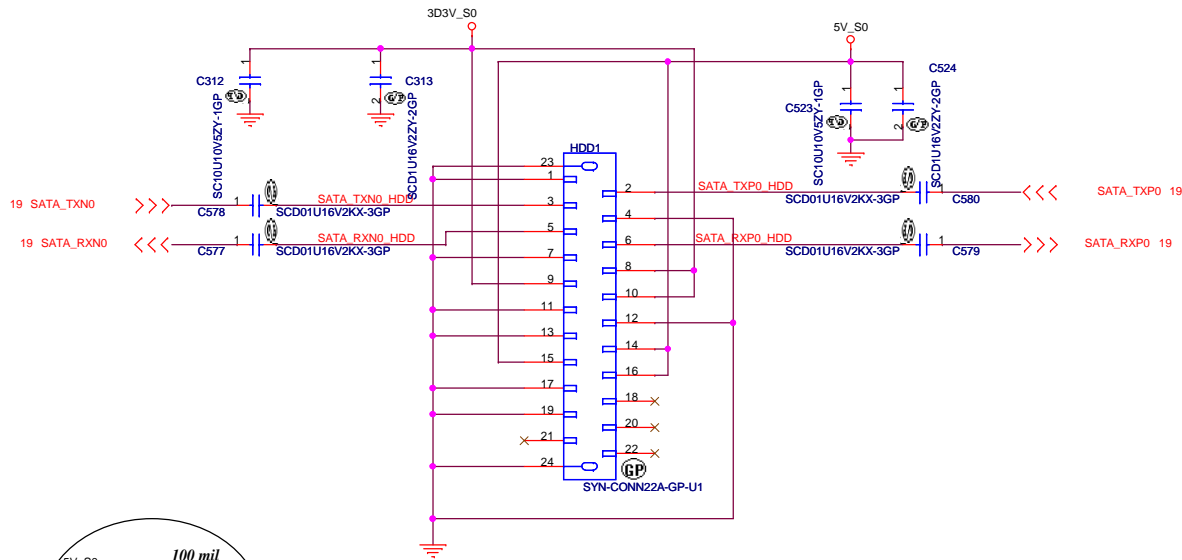
**Wistron Corporation**  
2/F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinshui, Taipei, Taiwan, R.O.C.

Model: ECU000V\_20\_2006

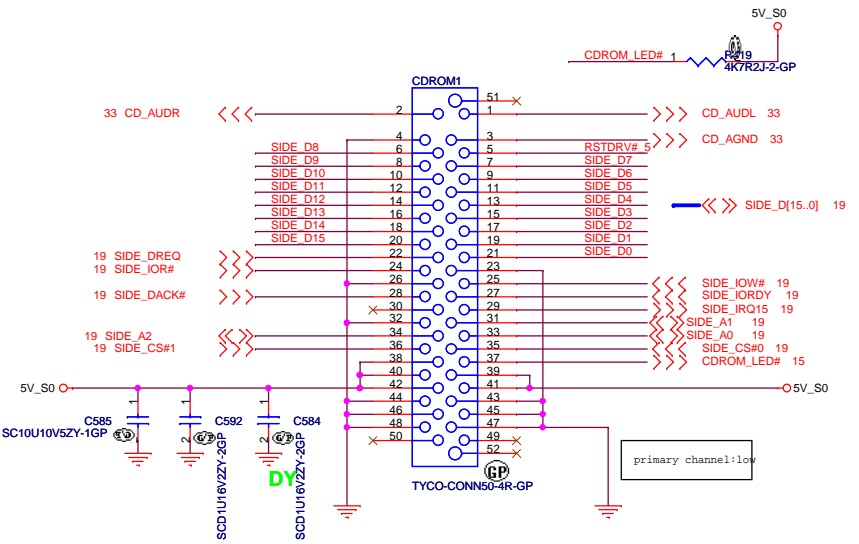
Sheet: 22 of 44



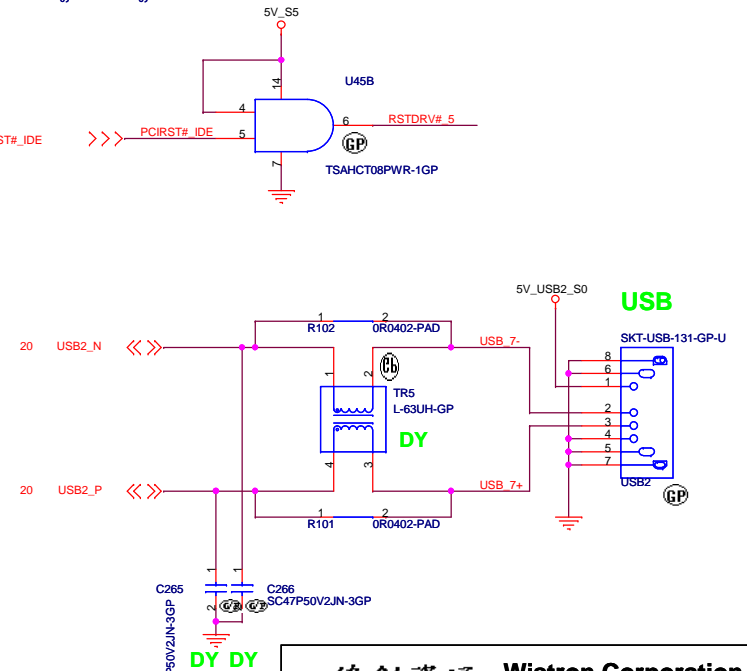
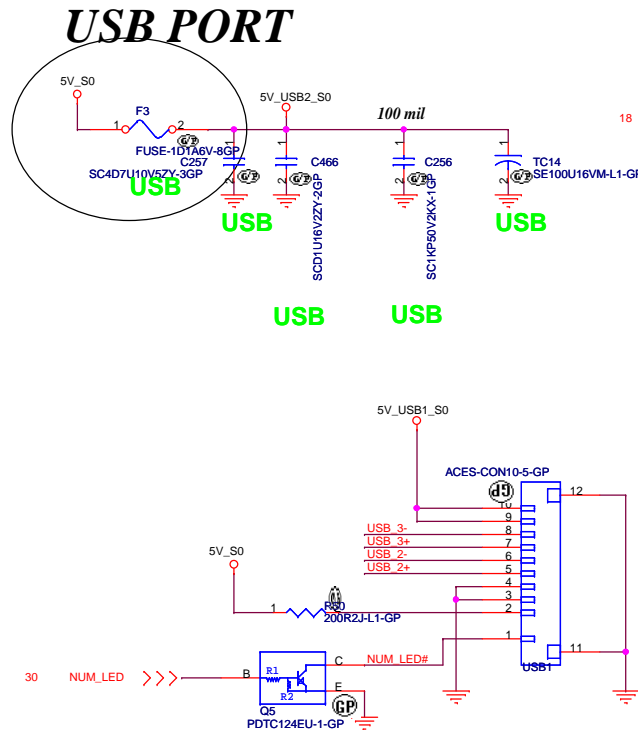
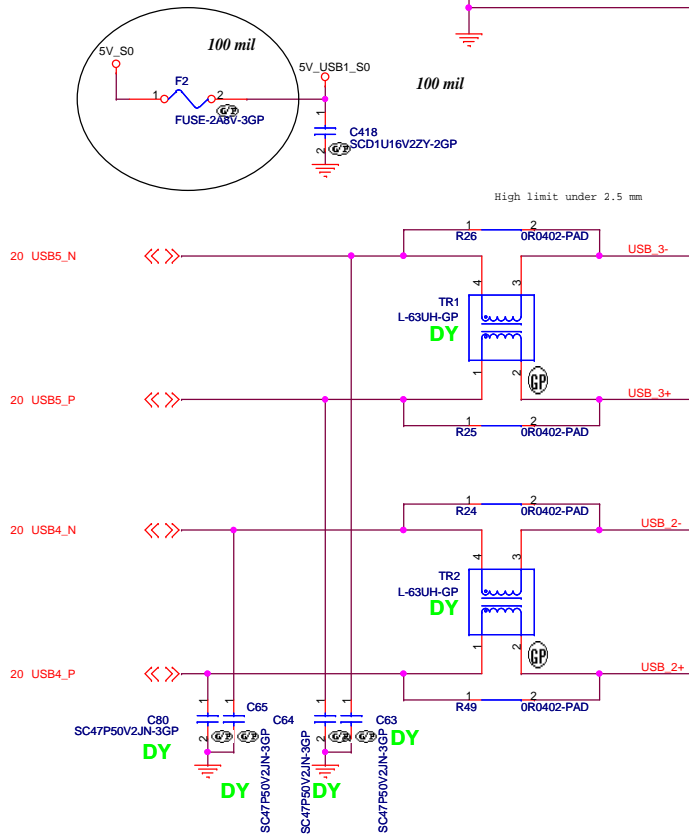
# SATA HD Connector



# CD-ROM CONNECTOR

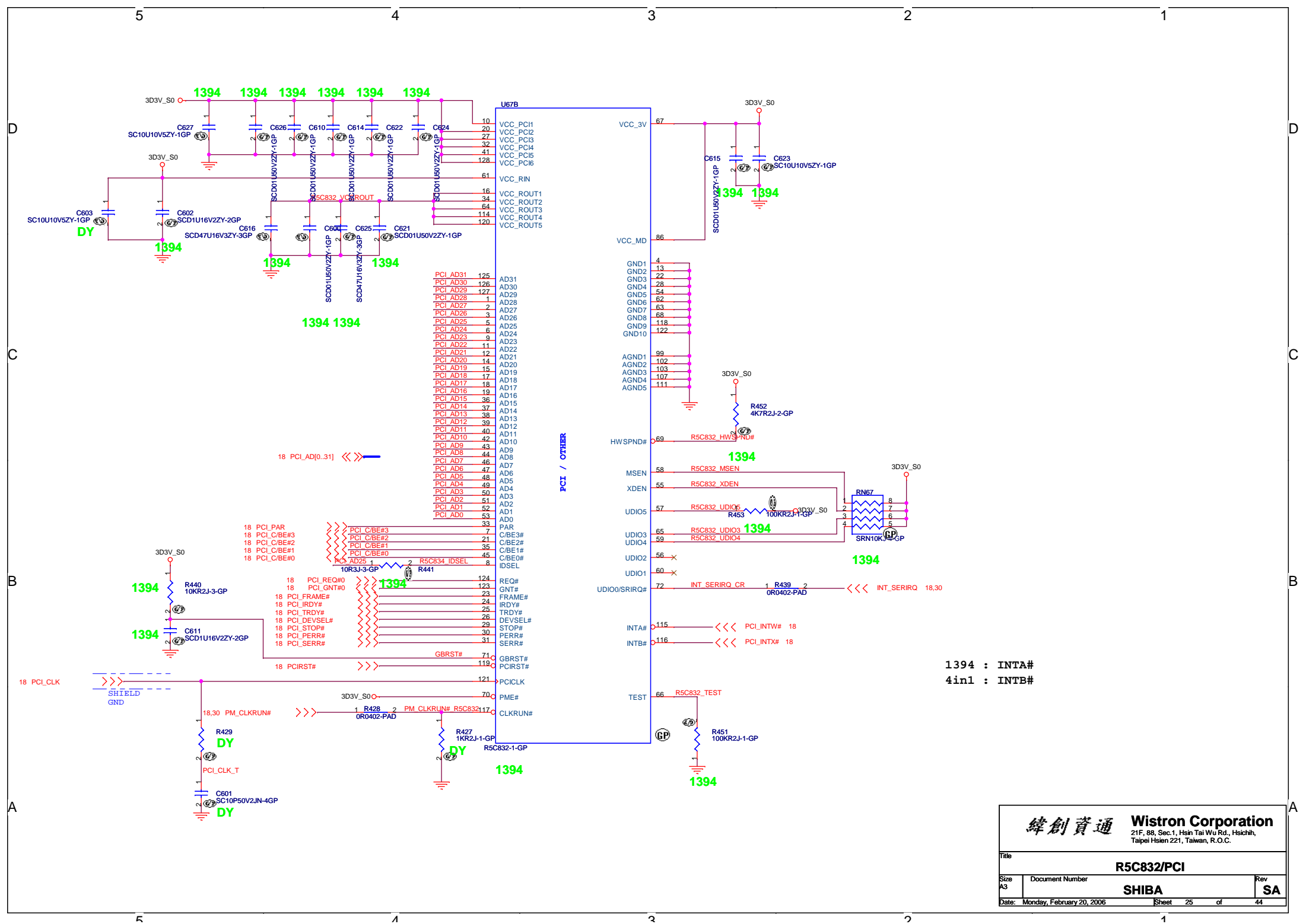


# USB PORT

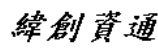


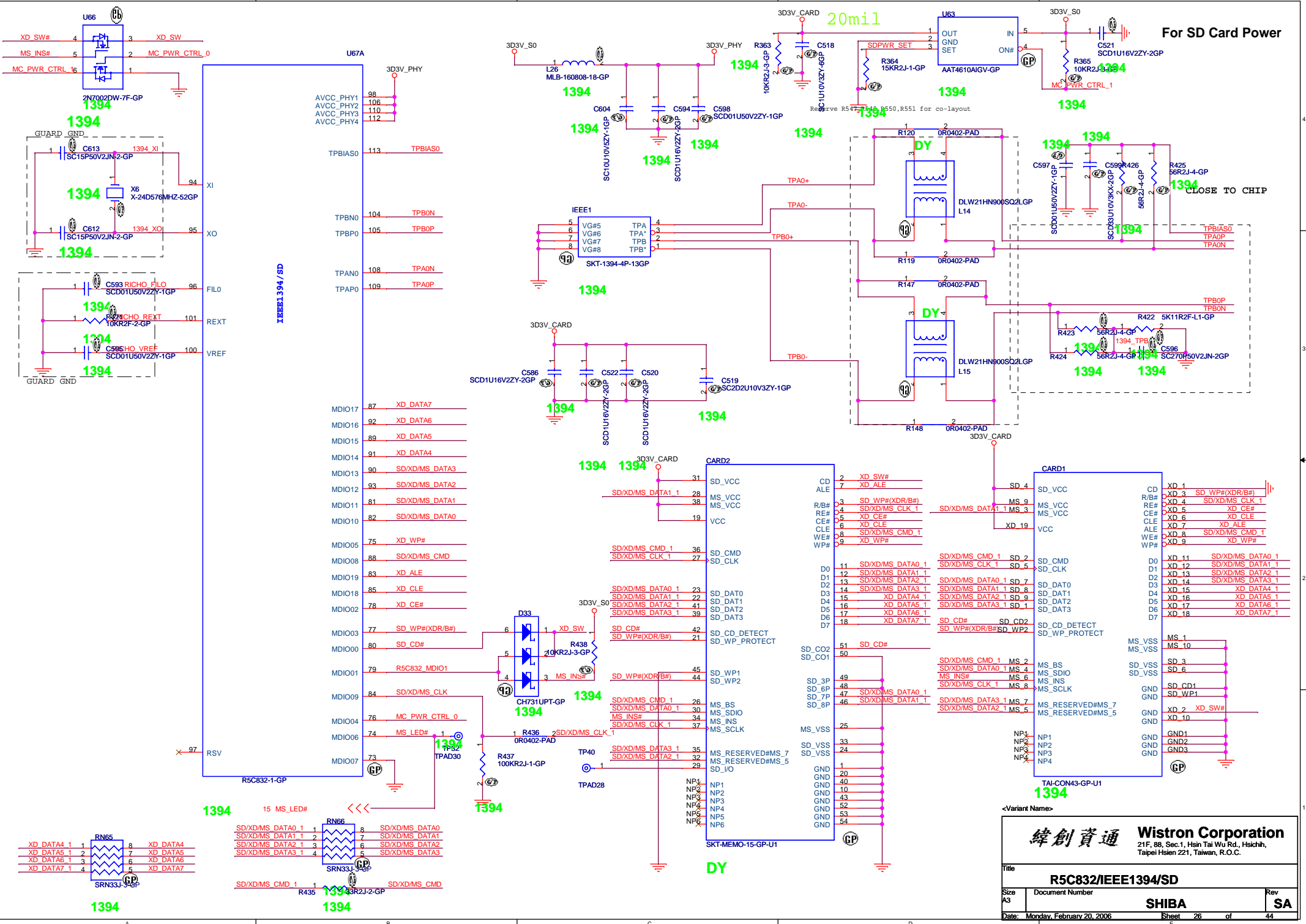
		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>HD/CDROM</b>			
Size A3	Document Number <b>SHIBA</b>		Rev <b>SA</b>
Date: Saturday, March 04, 2006	Sheet 24	of 44	





1394 : INTA#  
 4in1 : INTB#

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
<b>R5C832/PCI</b>	
Size	Document Number
A3	<b>SHIBA</b>
Date:	Rev
Monday, February 20, 2006	<b>SA</b>
Sheet	of
25	44



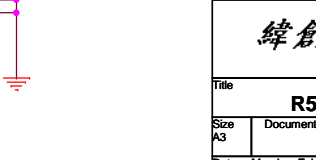
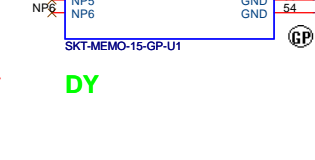
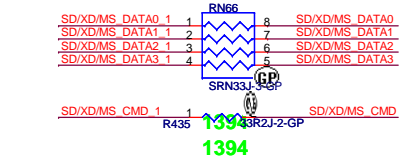
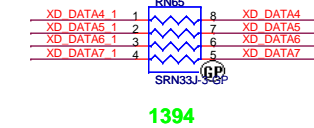
For SD Card Power

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **R5C832/IEEE1394/SD**

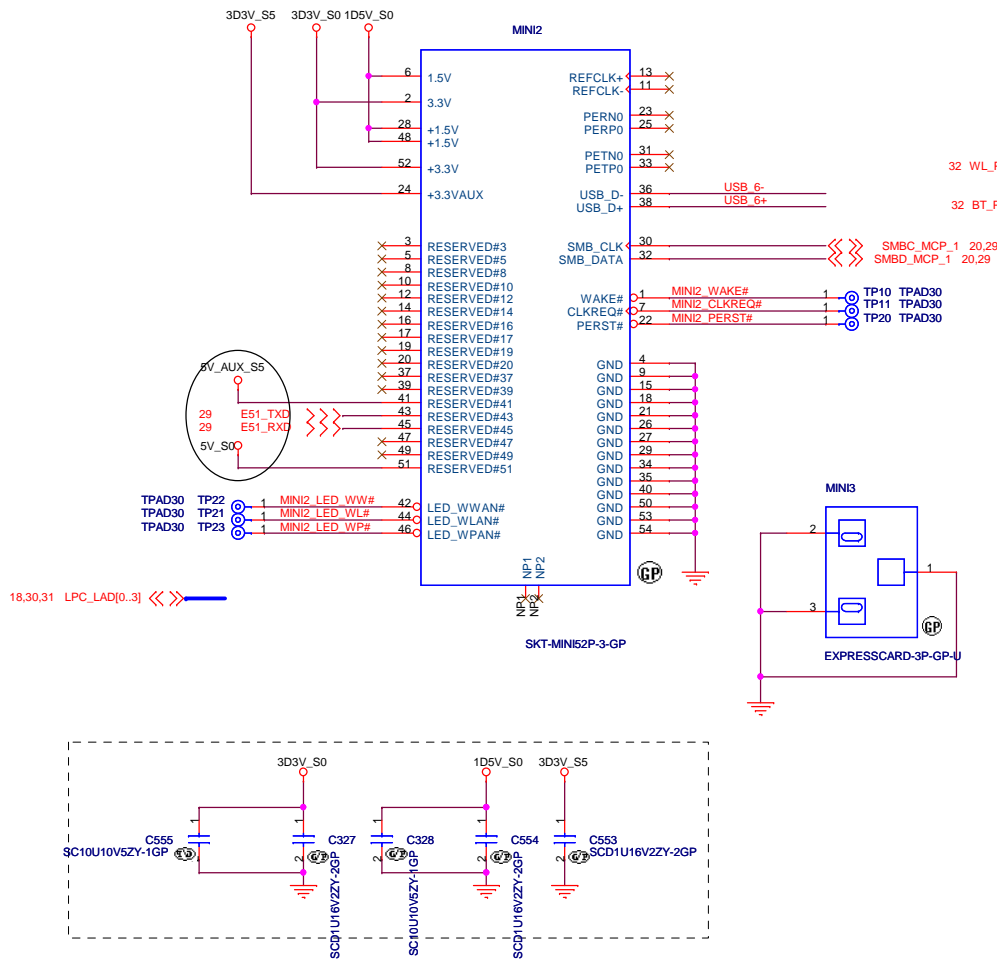
Size: A3 Document Number: **SHIBA** Rev: **SA**

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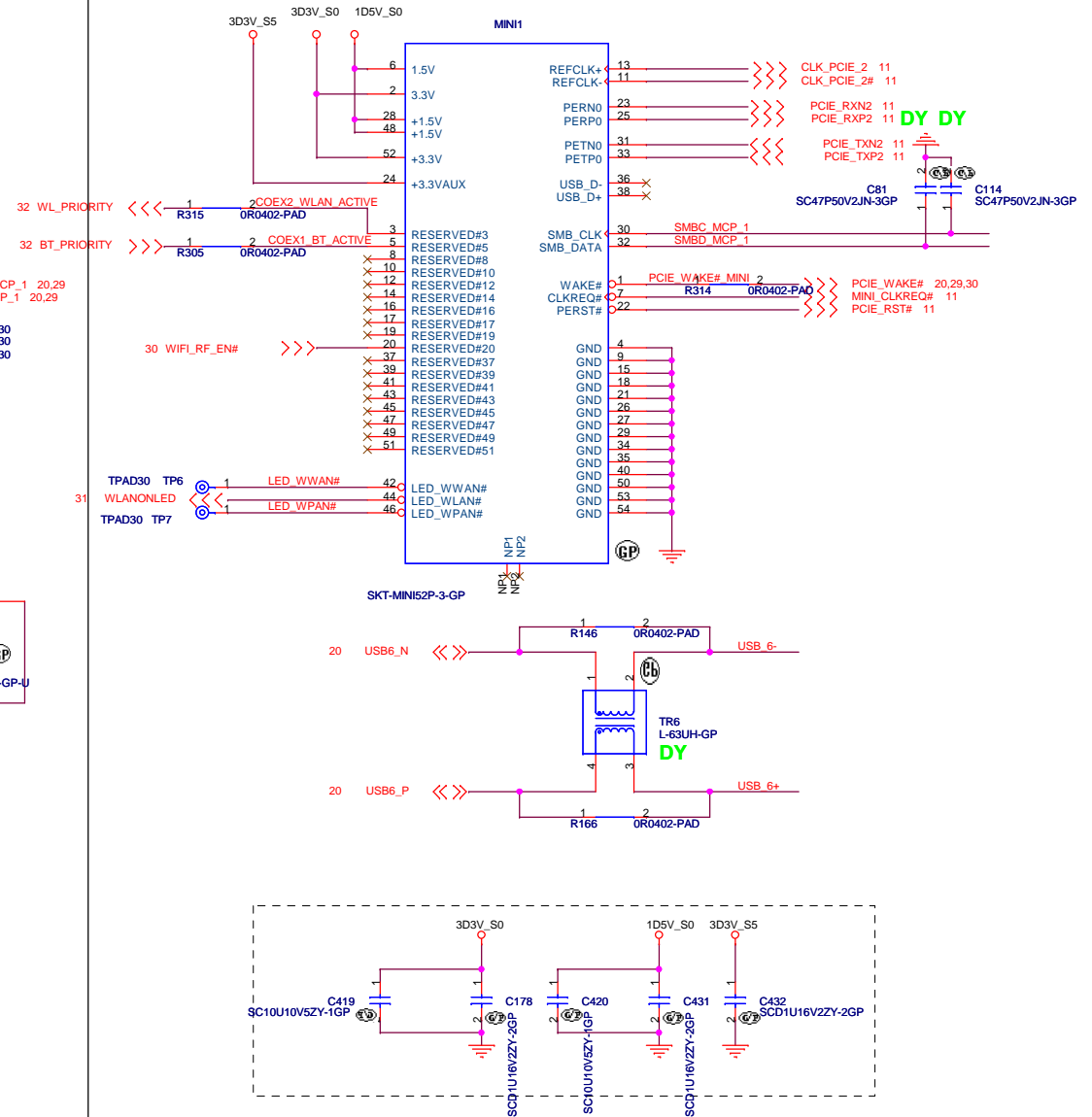


# Mini Card Connector

## Mini Card Connector 1



## Mini Card Connector 2

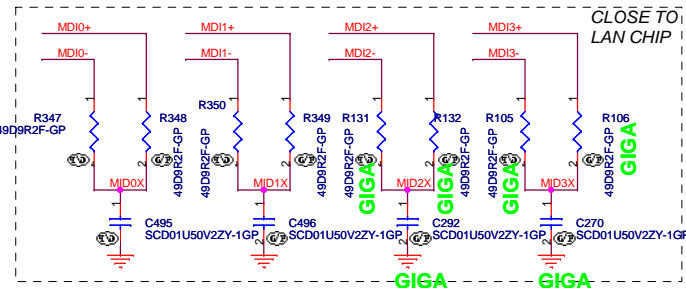
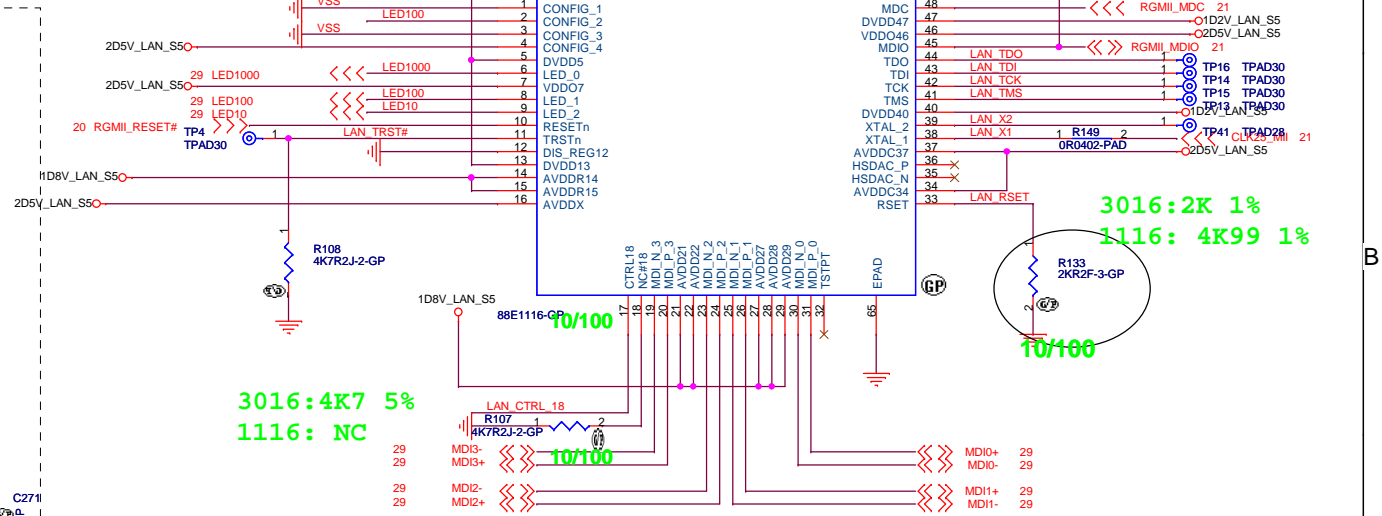
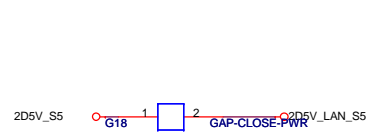
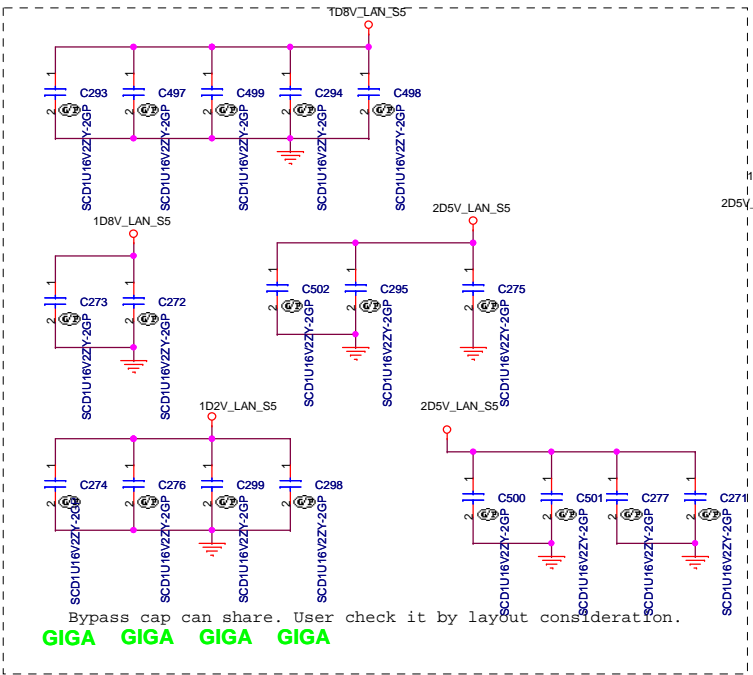
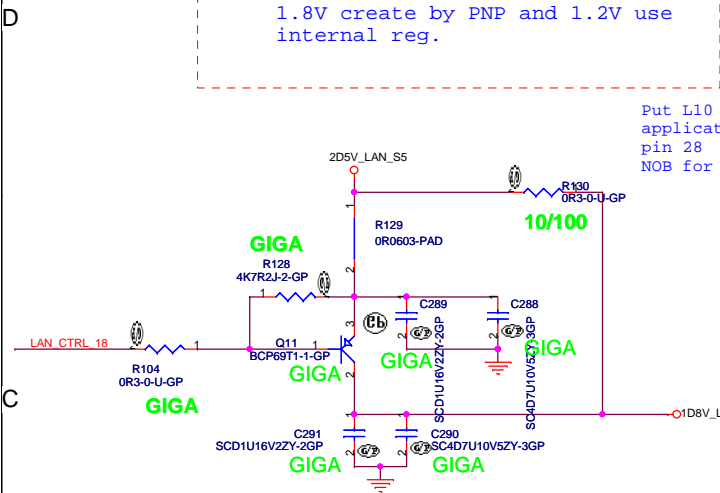


Hardware Configuration: See config\_0:4

1. PHY address:00001
2. ENA\_XC:Enable Auto-Crossover
3. RGMII\_TX:Transmit clock not internally delayed
4. RGMII\_RX:Receive clock transition when data transitions
5. Advertise all capabilities

E1116 use external 2.5V single power supply.  
1.8V create by PNP and 1.2V use internal reg.

Put L10 for E3016 application since pin 28 NOB for E1116

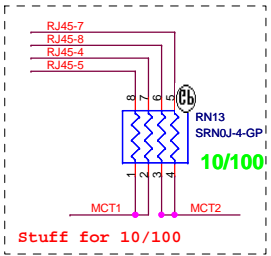
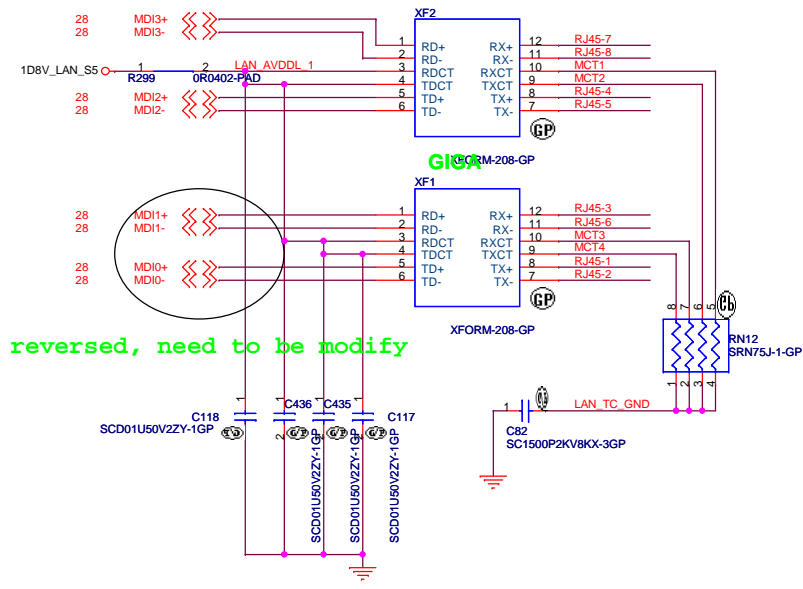


<Variant Name>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchi, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN MARVELL 88E1116**

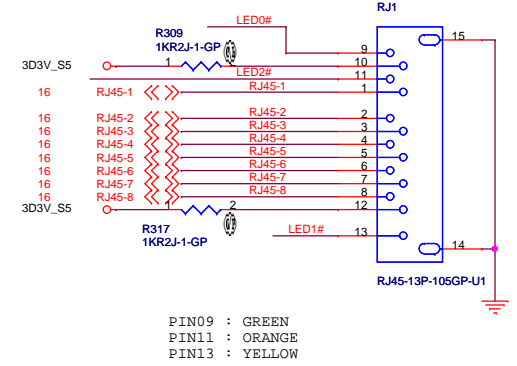
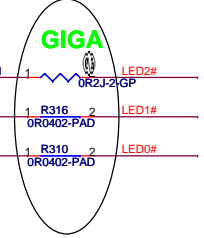
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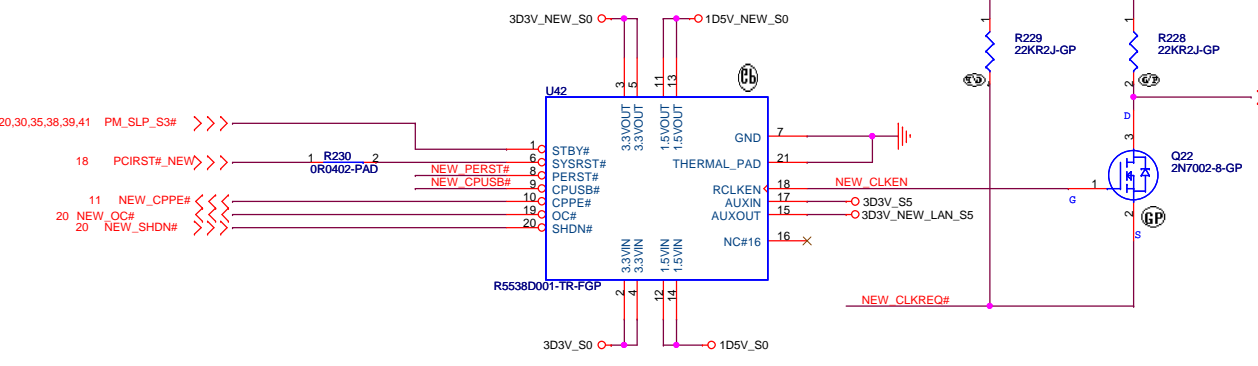
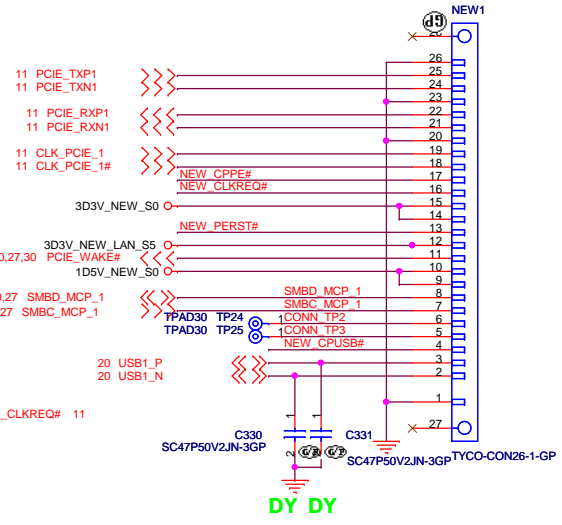
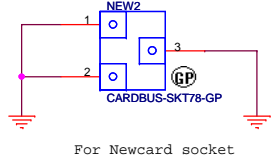
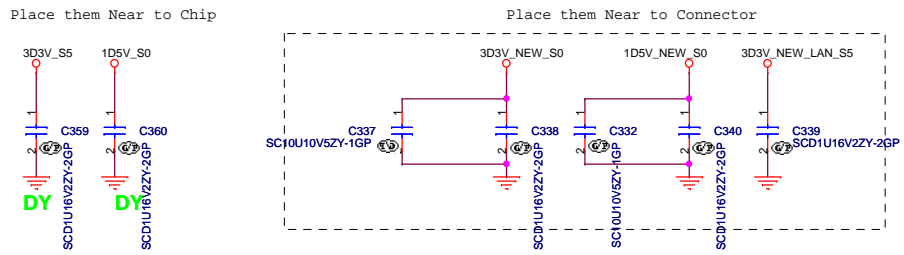
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

**GREEN: LINK 10/100 Mbps**  
**YELLOW: TX/RX ACTIVITY**  
**ORANGE: LINK 1000Mbps**

reversed, need to be modify



## NEWCARD Connector

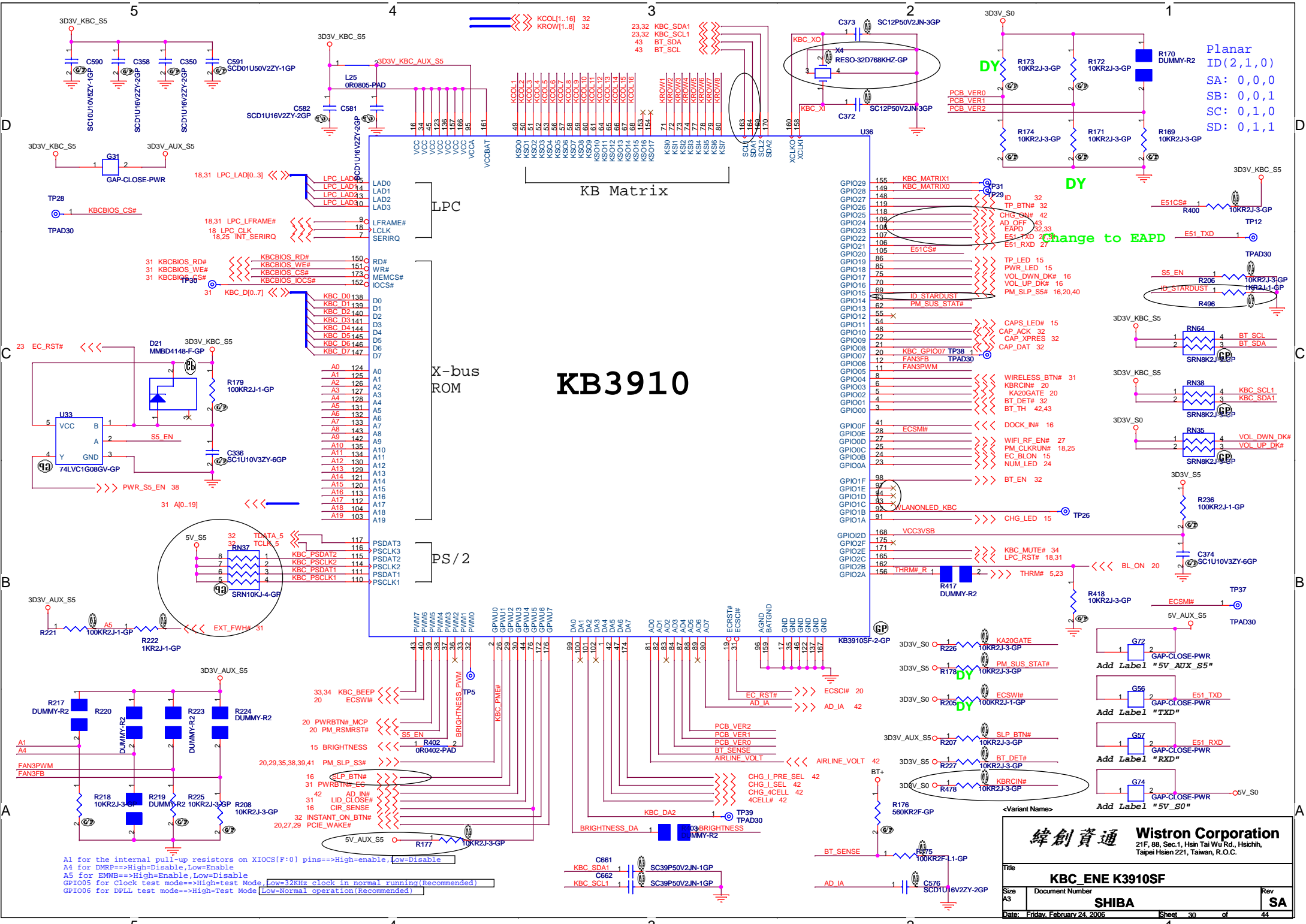


**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **New Card**

Size: A3 Document Number: **SHIBA** Rev: **SA**

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Planar  
ID(2,1,0)  
SA: 0,0,0  
SB: 0,0,1  
SC: 0,1,0  
SD: 0,1,1

# KB3910

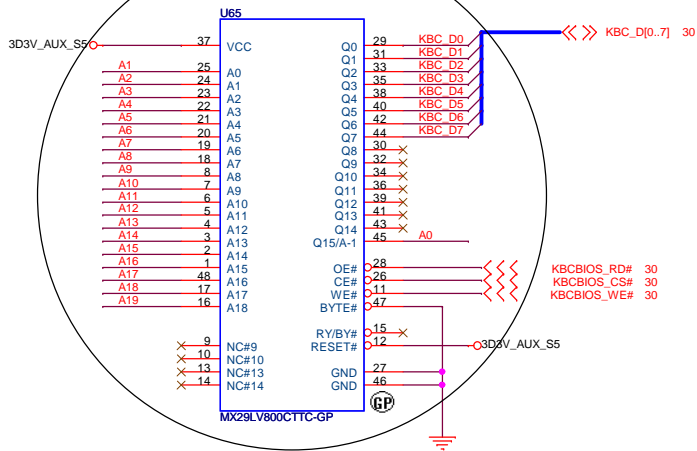
**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **KBC\_ENE K3910SF**

Size: A3	Document Number: <b>SHIBA</b>	Rev: <b>SA</b>
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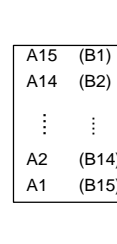
A1 for the internal pull-up resistors on XIOCS[0:1] pins==>High=enable, Low=Disable  
 A4 for DMRP==>High=Disable, Low=Enable  
 A5 for EMWB==>High=Enable, Low=Disable  
 GPI005 for clock test mode==>High=Test Mode, Low=32KHz clock in normal running(Recommended)  
 GPI006 for DPLL test mode==>High=Test Mode [Low=Normal operation(Recommended)]

30 A[0..19]



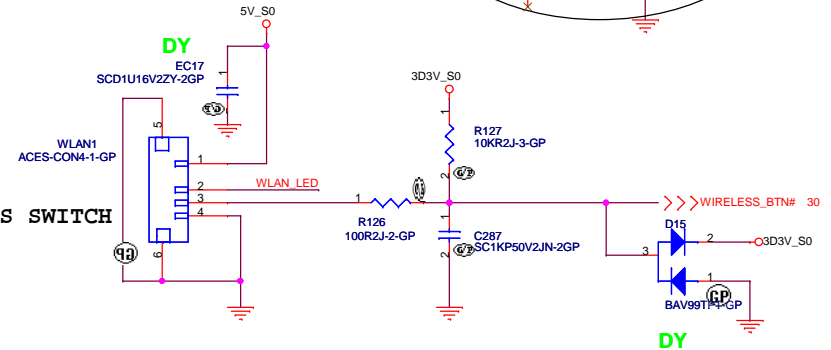
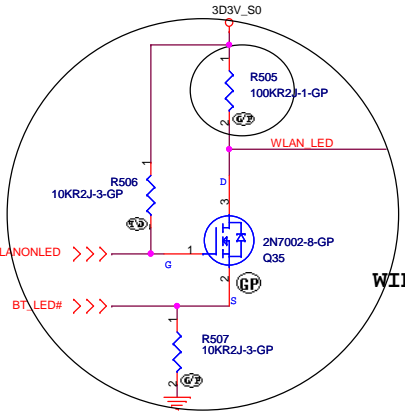
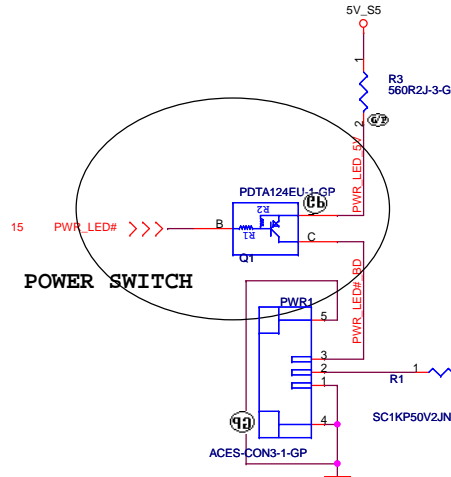
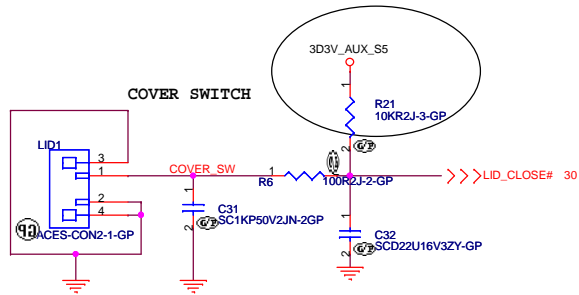
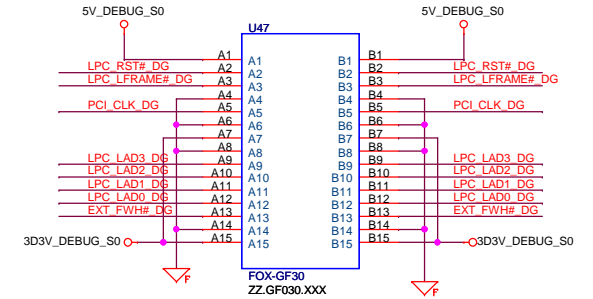
Change to MX29LV800CTTC  
72.29800.0B9

### TOP VIEW



### (BOTTOM VIEW)

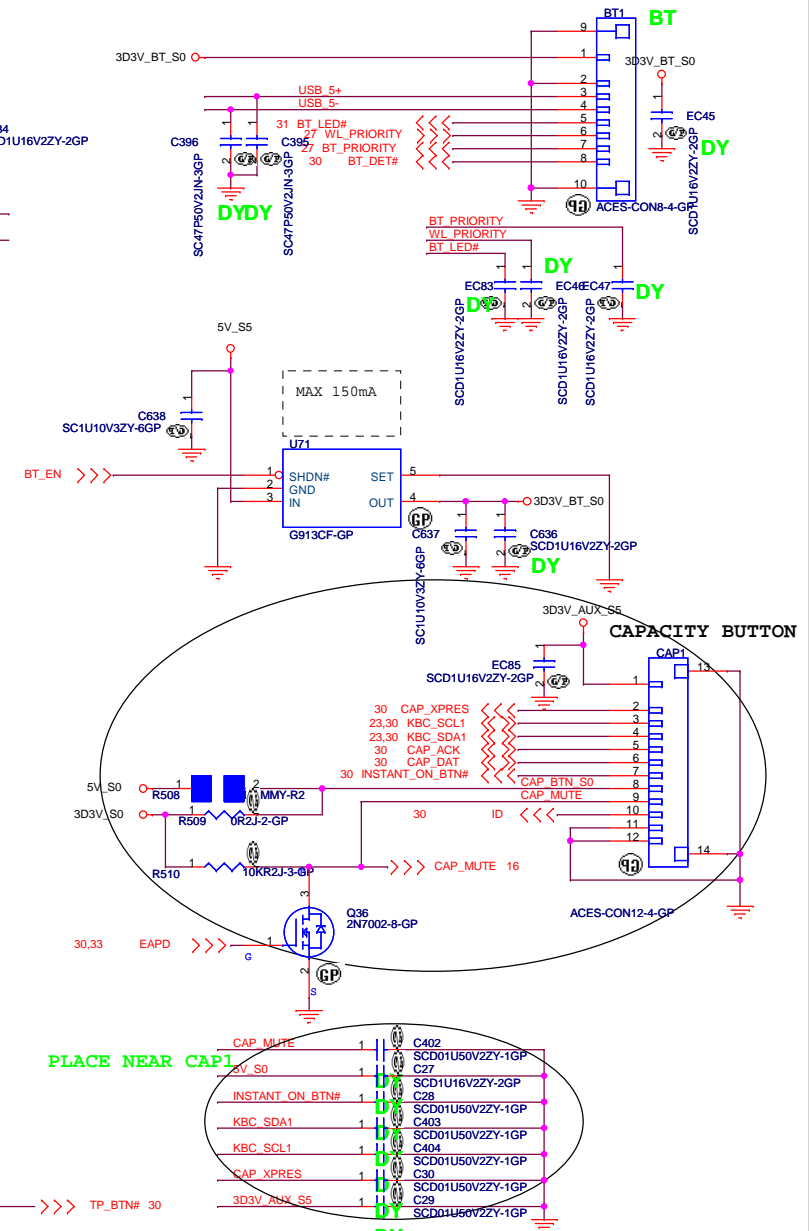
### GOLDEN FINGER FOR DEBUG BOARD



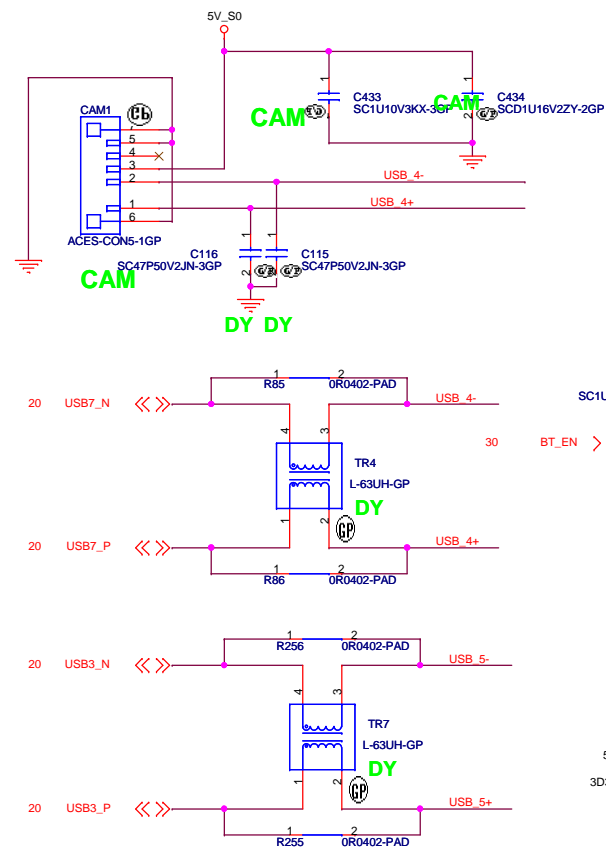
Put near board edge

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>FLASH and Debug</b>			
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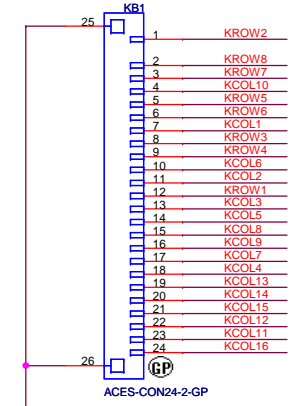
# Blue thumb



# CAMERA



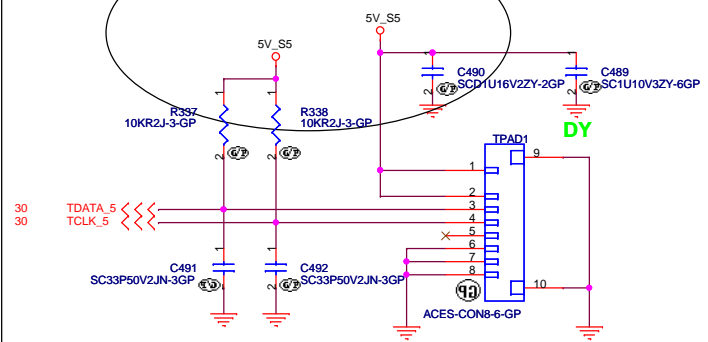
# Internal Keyboard Connector



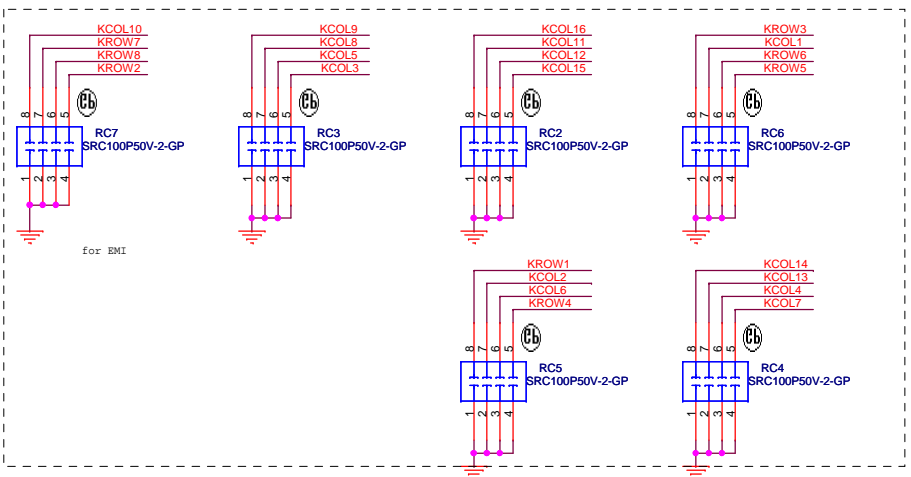
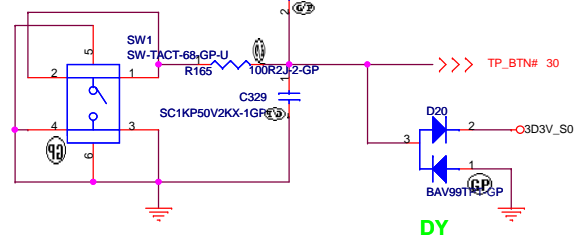
Keyboard matrix ( from vendor )

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

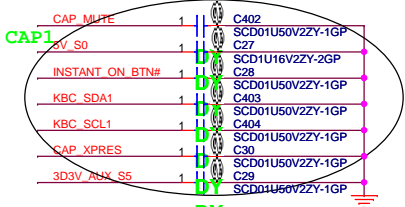
# TouchPad Connector



# TOUCH-PAD SWITCH



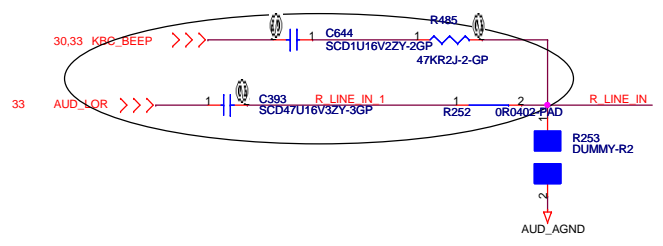
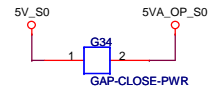
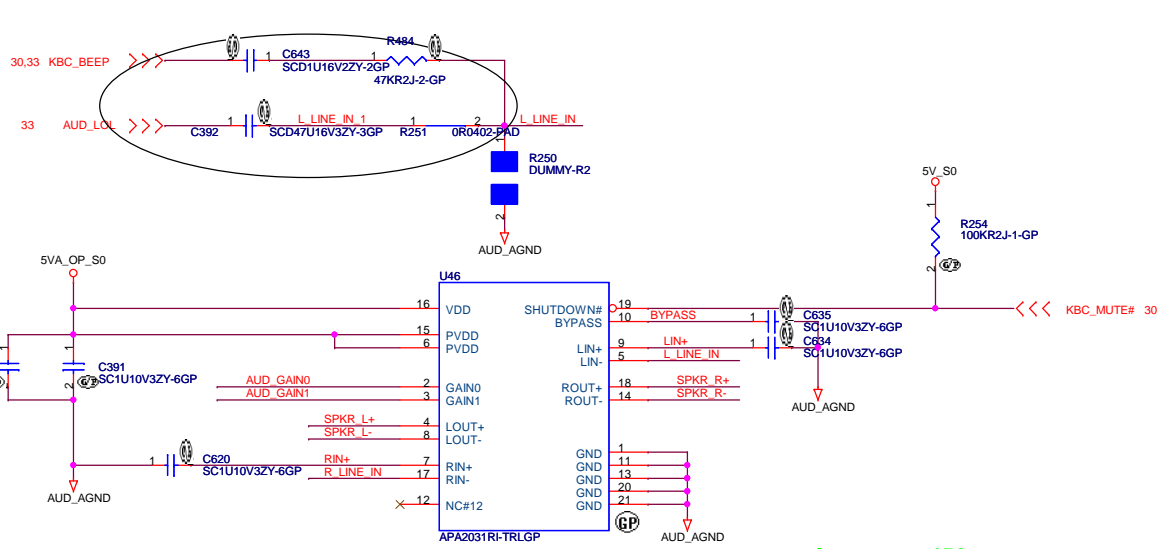
PLACE NEAR CAP1



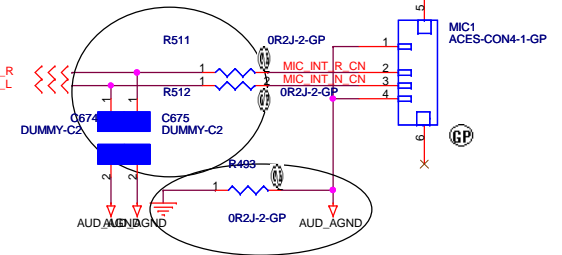
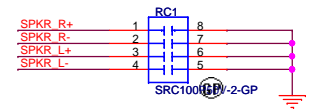
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.



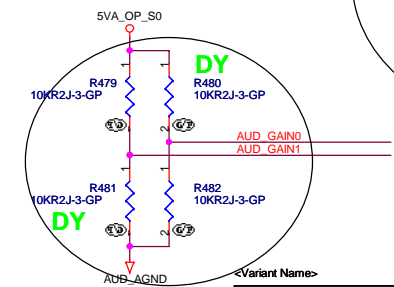
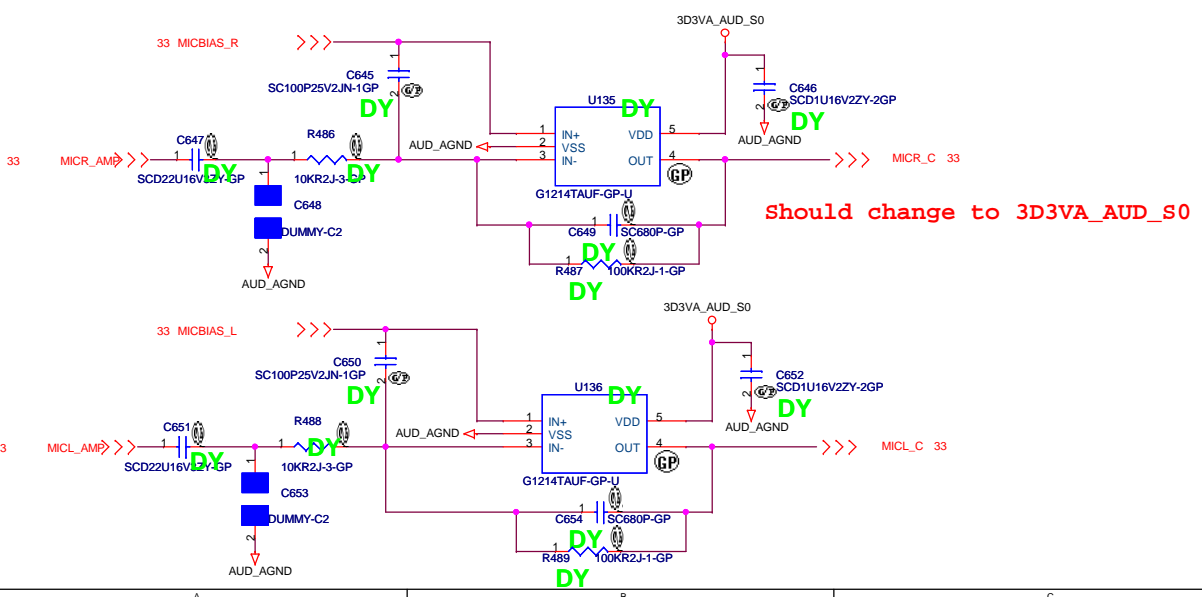
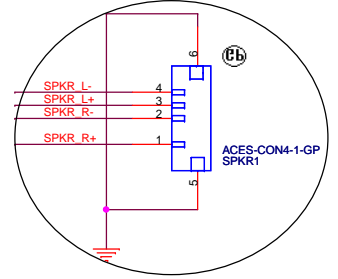




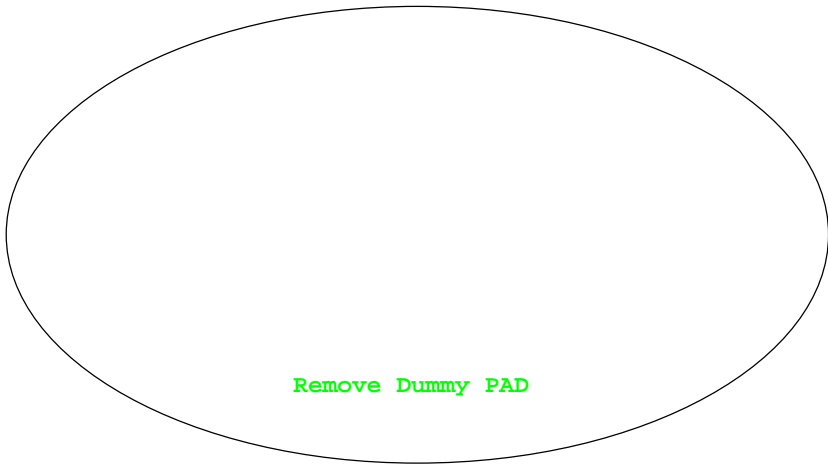
change to 470P



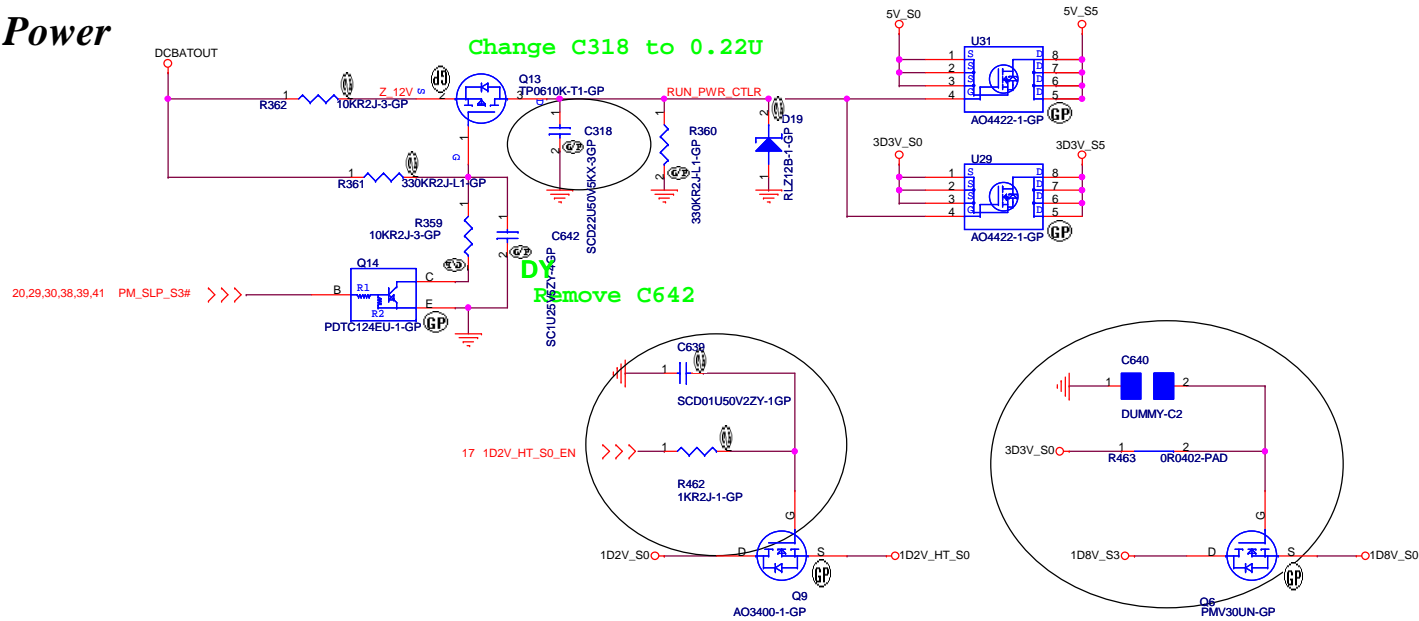
# Speaker



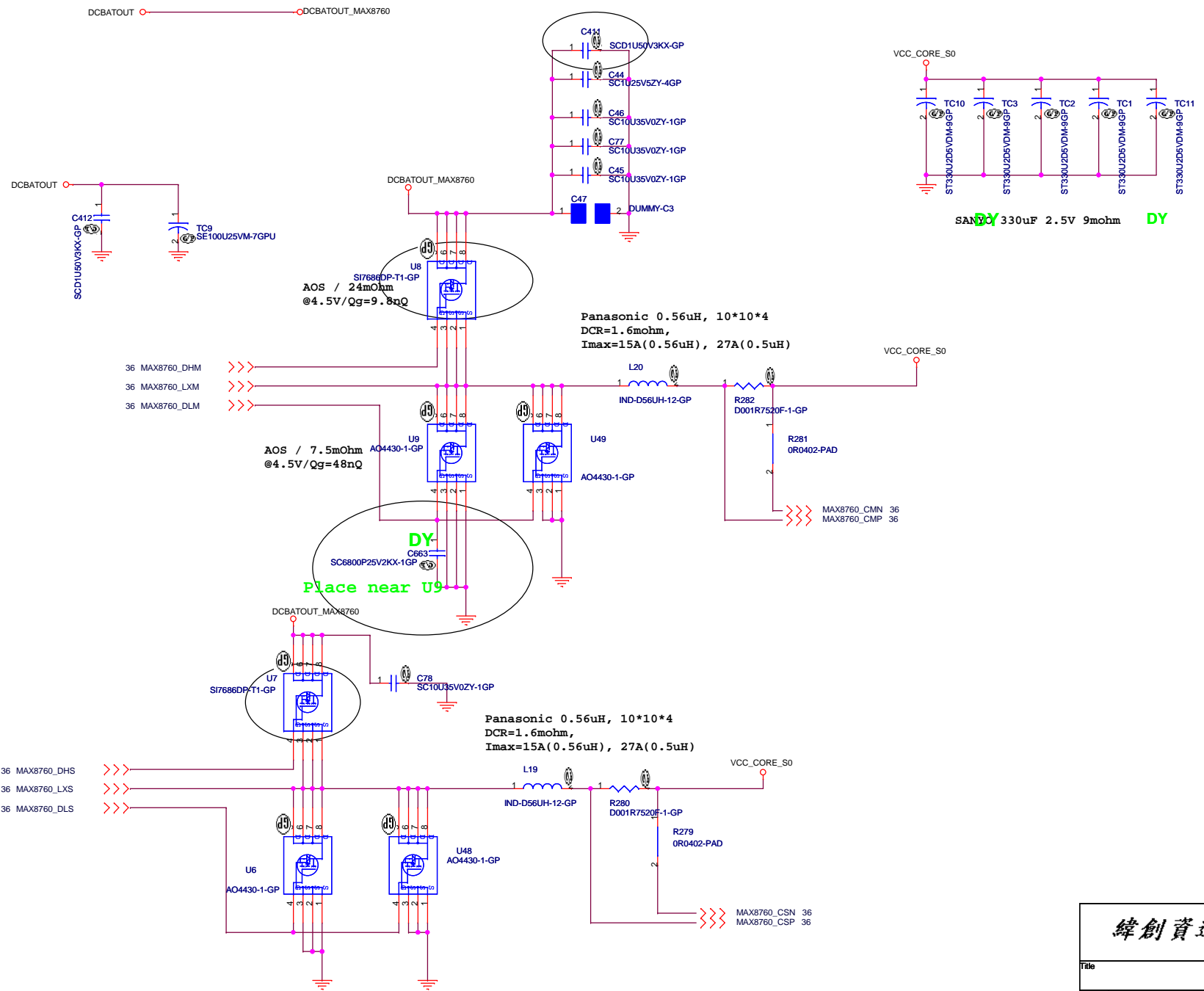
# Suspend Power



# Run Power



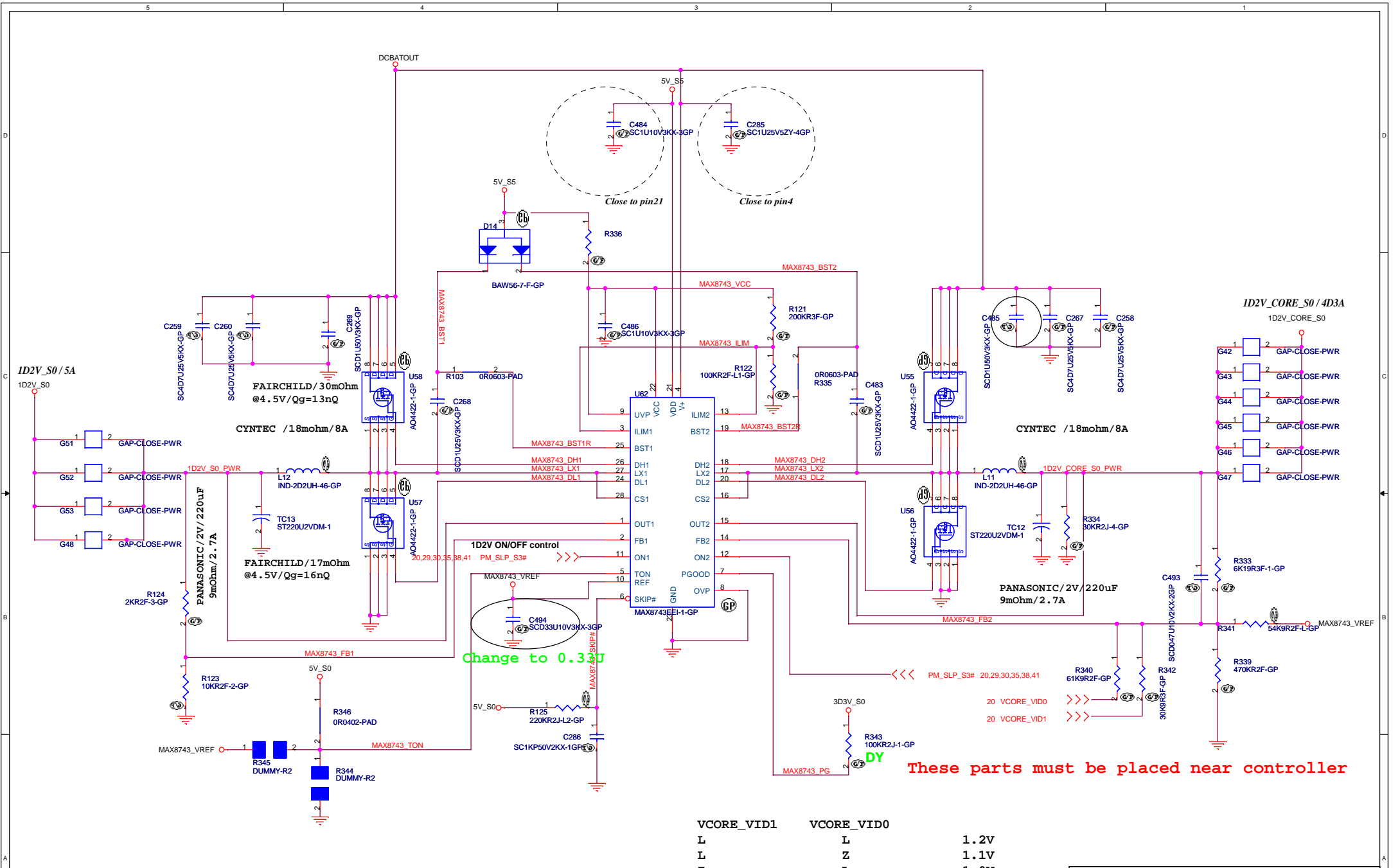




(Power Team)

<b>緯創資通 Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>File CPU CORE MAX8760(2/2)</b>	
Size A3	Document Number <b>SHIBA</b>
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Rev SA	

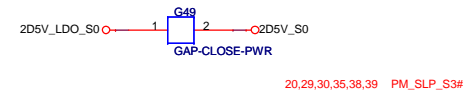
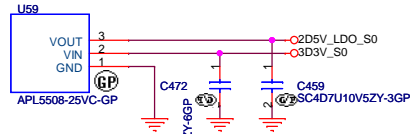




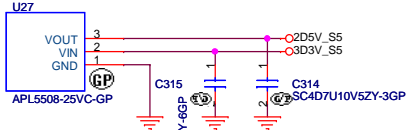
VCORE_VID1		VCORE_VID0	
L	1.2V	L	1.2V
L	1.1V	Z	1.1V
Z	1.0V	L	1.0V
Z	Reserved	Z	Reserved



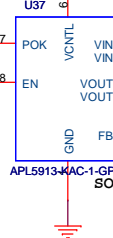
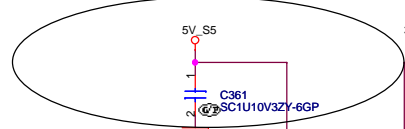




G50



Change to S5 power plane

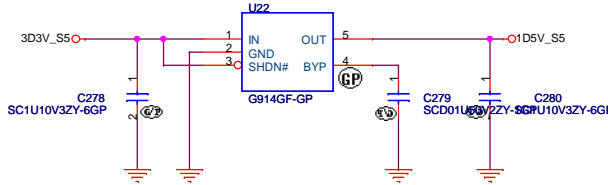


$V_o(\text{cal.}) = 1.512V$

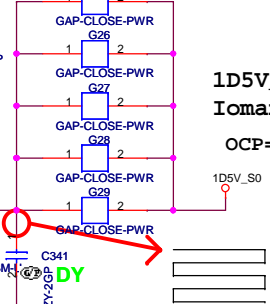
$V_o = 0.8 * (1 + (R1/R2))$

KEMET  
100uF, 4V, B2 Size, NTD:5.615  
Iripple=1.1A, ESR=70mohm

$V_o = 0.8 * (1 + (R1/R2))$



2nd source : 74.00916.D3F

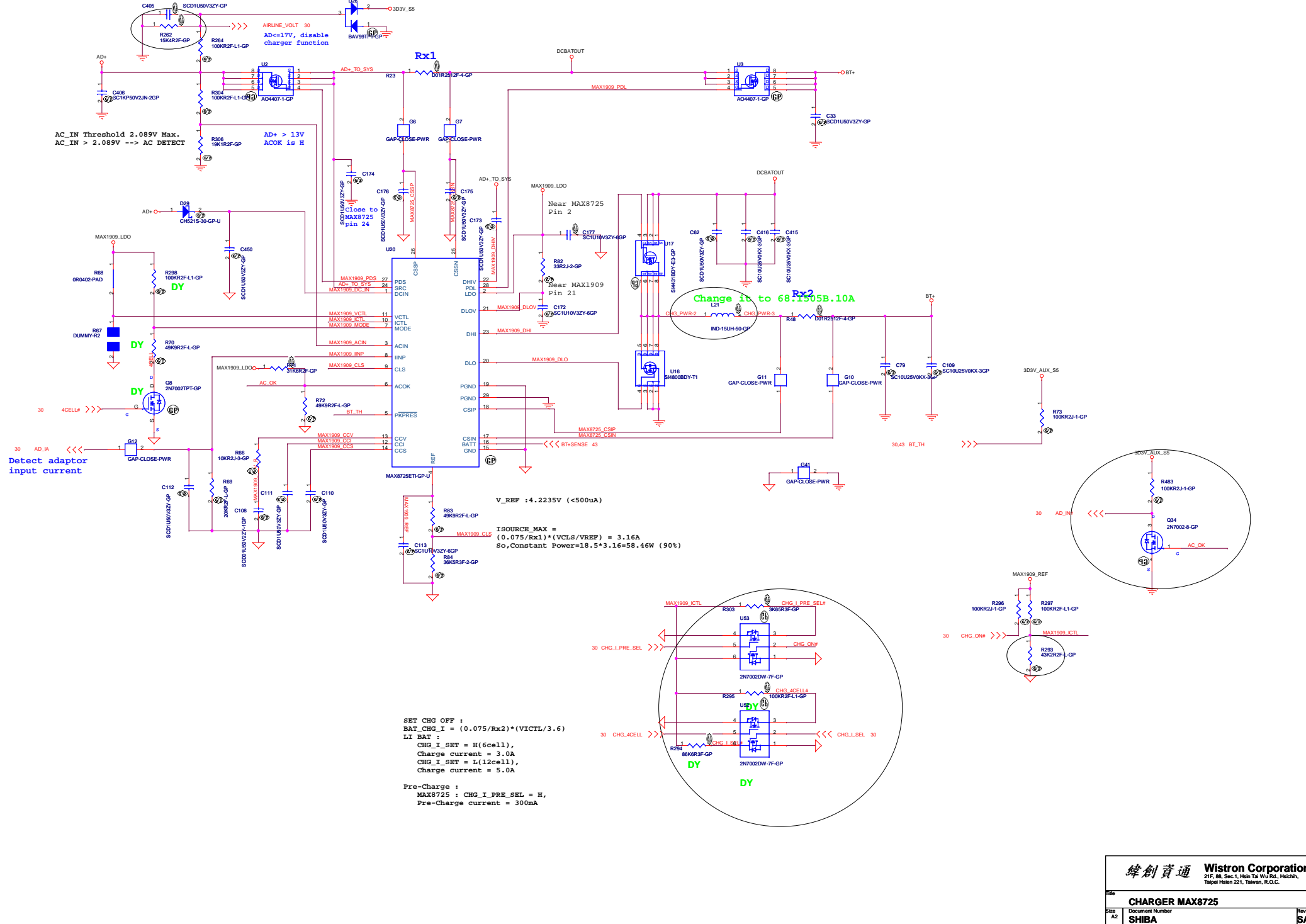


1D5V\_S0  
Iomax=1.3A  
OCP=2.6A

Trace Length=3cm  
Trace Width=5mils  
Trace Resistance>80mohm

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
1D5V/2D5V/3D3V/5V_AUX		
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AC\_IN Threshold 2.089V Max.  
AC\_IN > 2.089V -> AC DETECT

AD+ > 13V  
ACOK is H

Change it to 68.1505B.10A  
L24

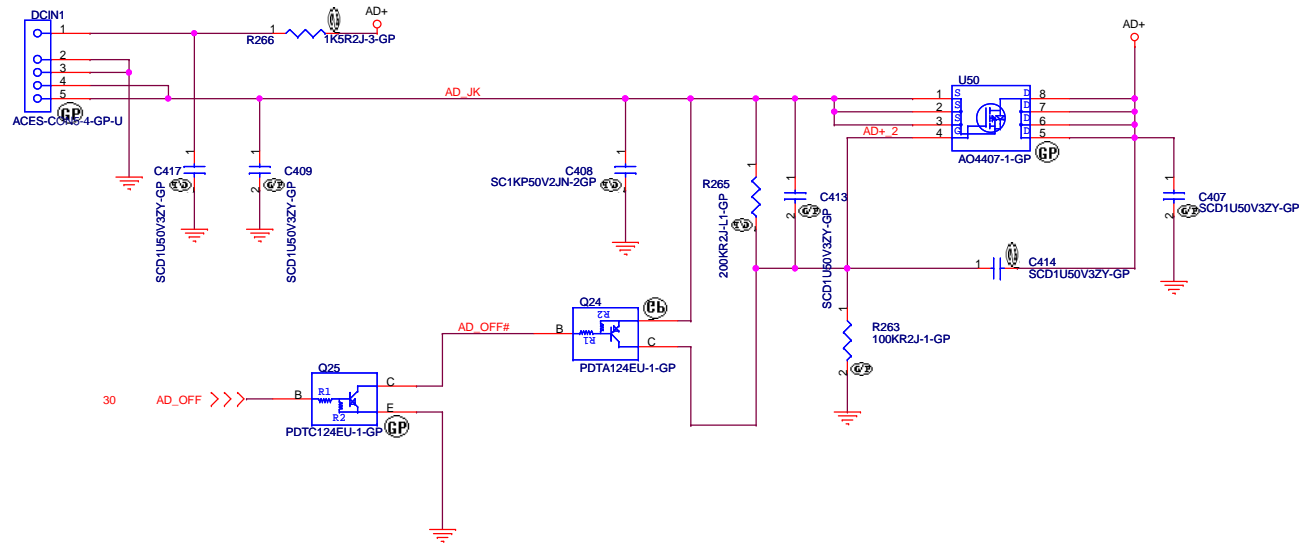
Detect adaptor  
input current

V\_REF : 4.2235V (<500uA)  
ISOURCE\_MAX =  
(0.075/Rx1)\*(VCLS/VREF) = 3.16A  
So, Constant Power=18.5\*3.16=58.46W (90%)

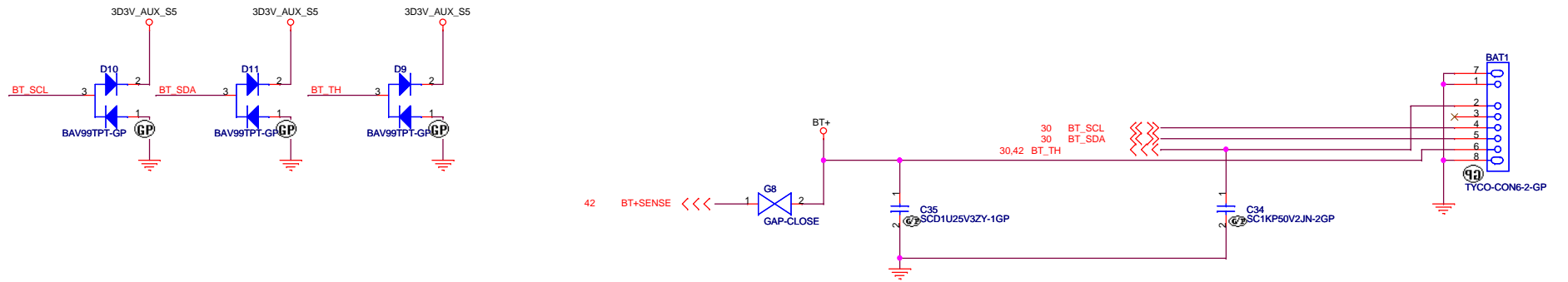
SET CHG OFF :  
BAT\_CHG\_I = (0.075/Rx2)\*(VICTL/3.6)  
LI BAT :  
CHG\_I\_SET = H(6cell),  
Charge current = 3.0A  
CHG\_I\_SET = L(12cell),  
Charge current = 5.0A

Pre-Charge :  
MAX8725 : CHG\_I\_PRE\_SEL = H,  
Pre-Charge current = 300mA

### Adaptor in to generate DCBATOUT



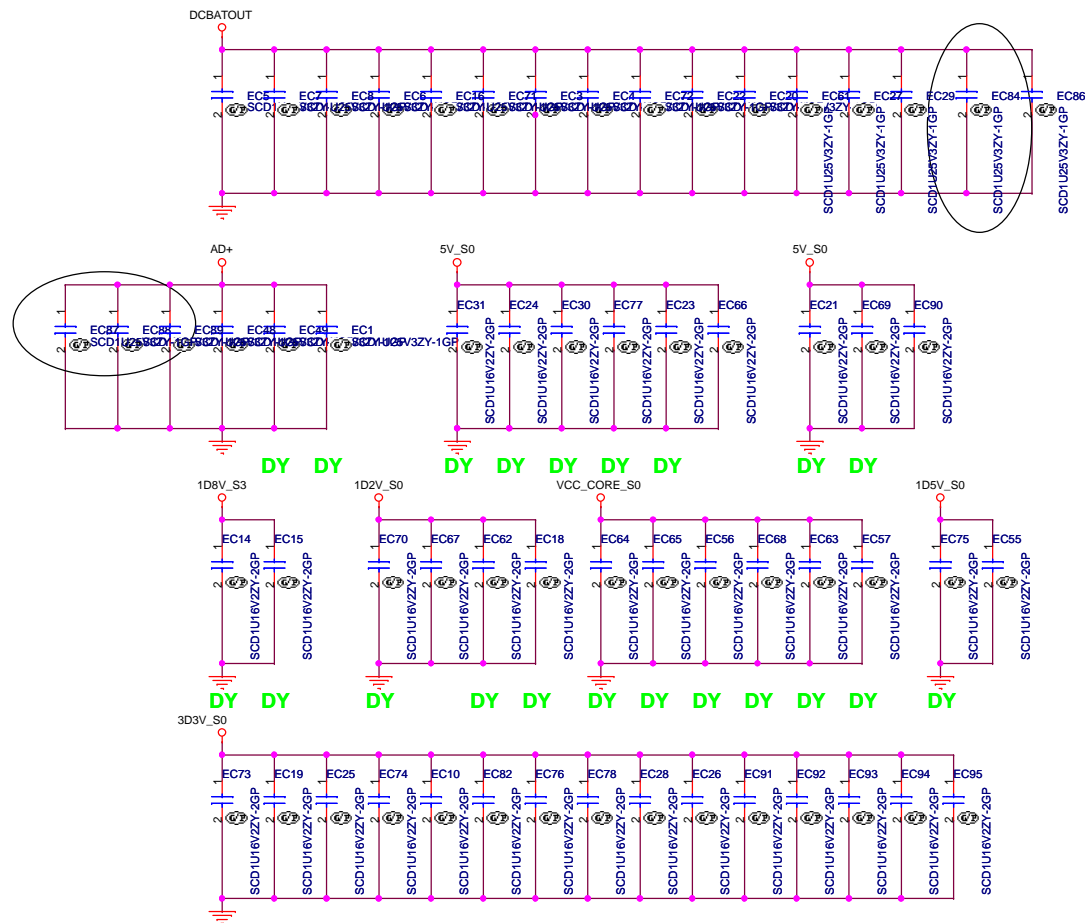
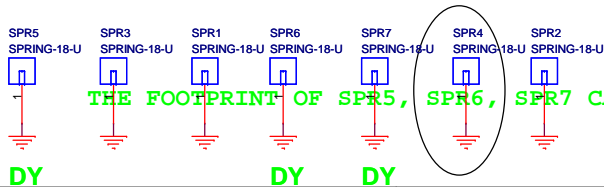
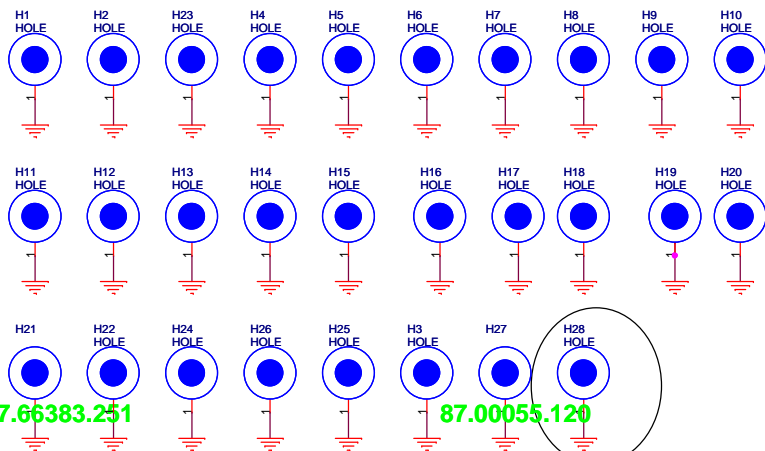
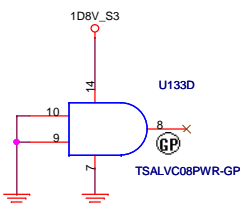
### BATTERY CONNECTOR



緯創資通 **Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title <b>AD/BATT CONN</b>		
Size A3	Document Number <b>SHIBA</b>	Rev <b>SA</b>
Date: Thursday, February 23, 2006	Sheet 43 of 44	

	FF	DF
CAMERA	○	×
LAN	10/100	10/100
1394/5 IN 1	○	×
EXTRA USB	○	×
MIC	○	×
CR LED	○	×



		<b>Wistron Corporation</b> 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: <b>MISC</b>			
Size: A3	Document Number:		Rev: SA
Date: Saturday, March 04, 2006	Sheet 44 of 44		

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