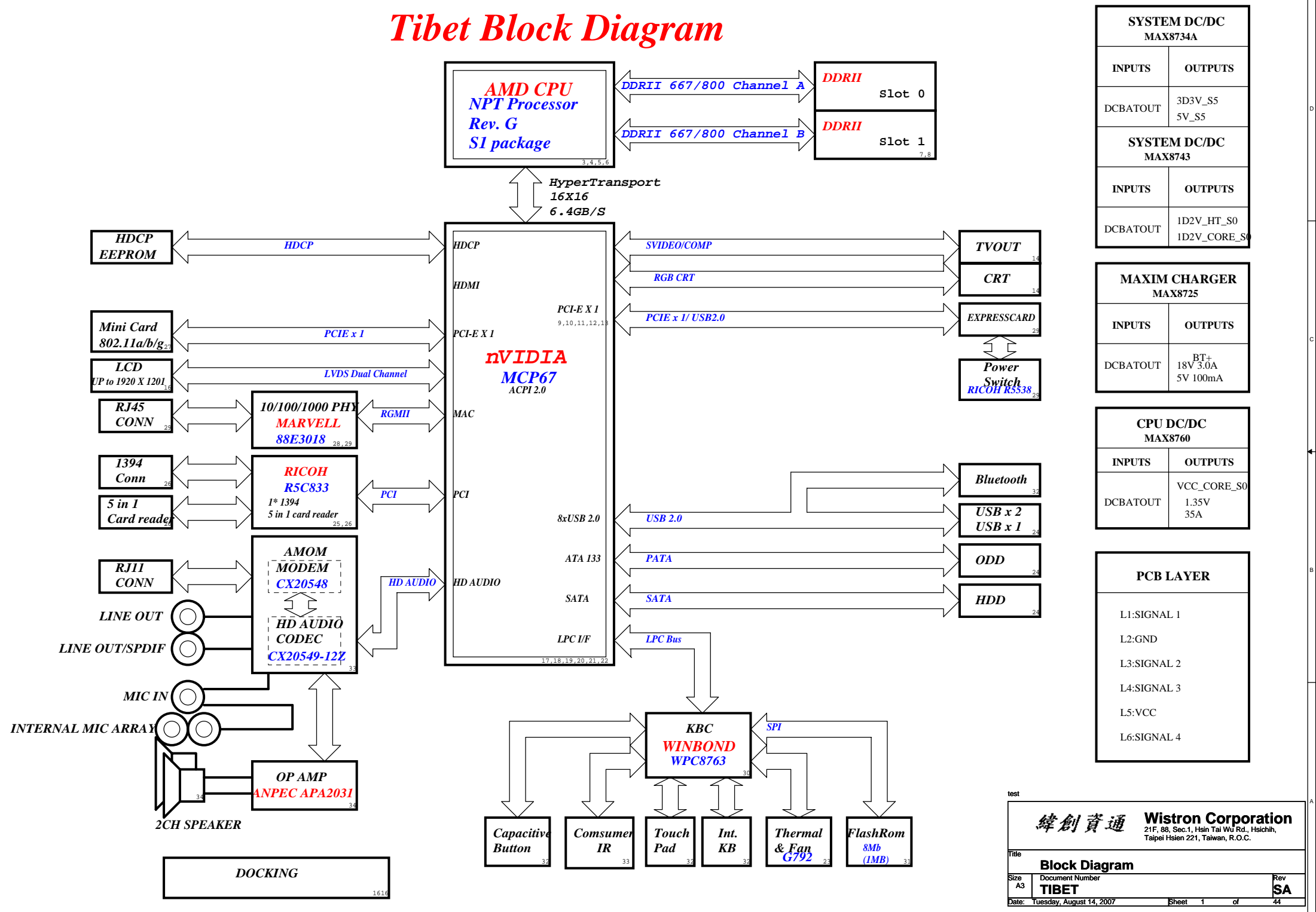


# Tibet Block Diagram

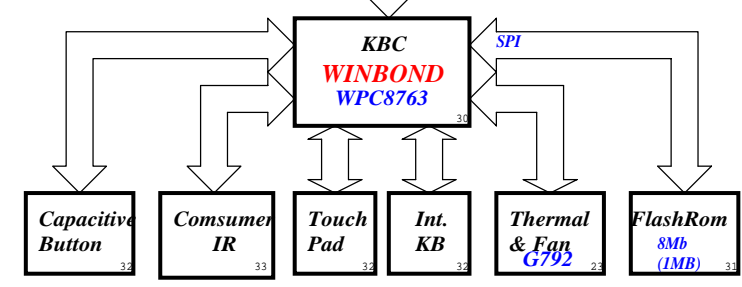


SYSTEM DC/DC MAX8734A	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5
SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D2V_HT_S0 1D2V_CORE_S0

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8760	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 1.35V 35A

PCB LAYER	
L1: SIGNAL 1	
L2: GND	
L3: SIGNAL 2	
L4: SIGNAL 3	
L5: VCC	
L6: SIGNAL 4	



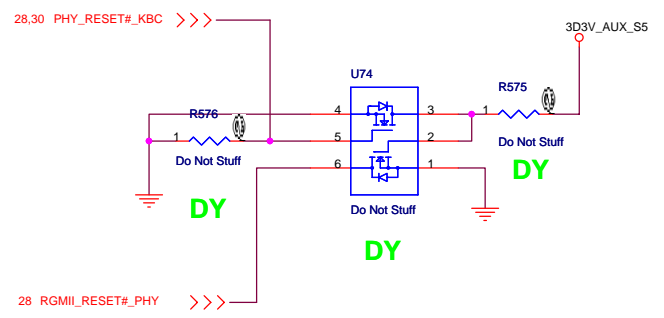
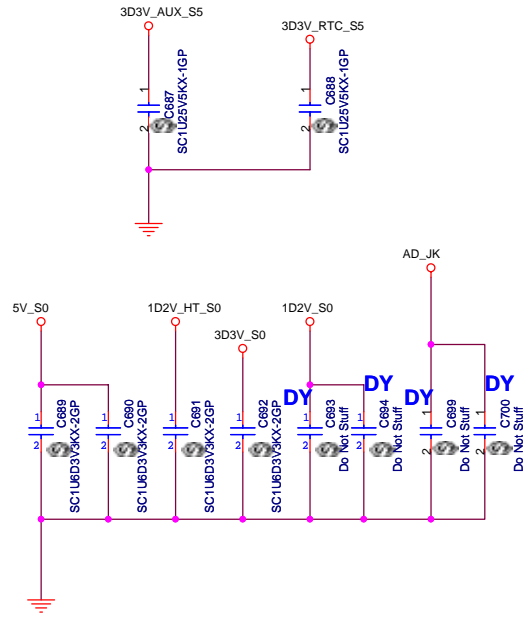
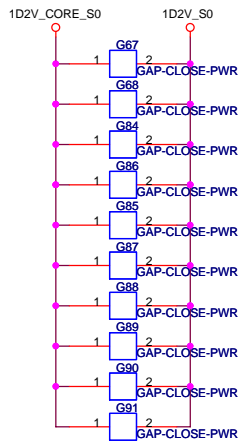
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**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

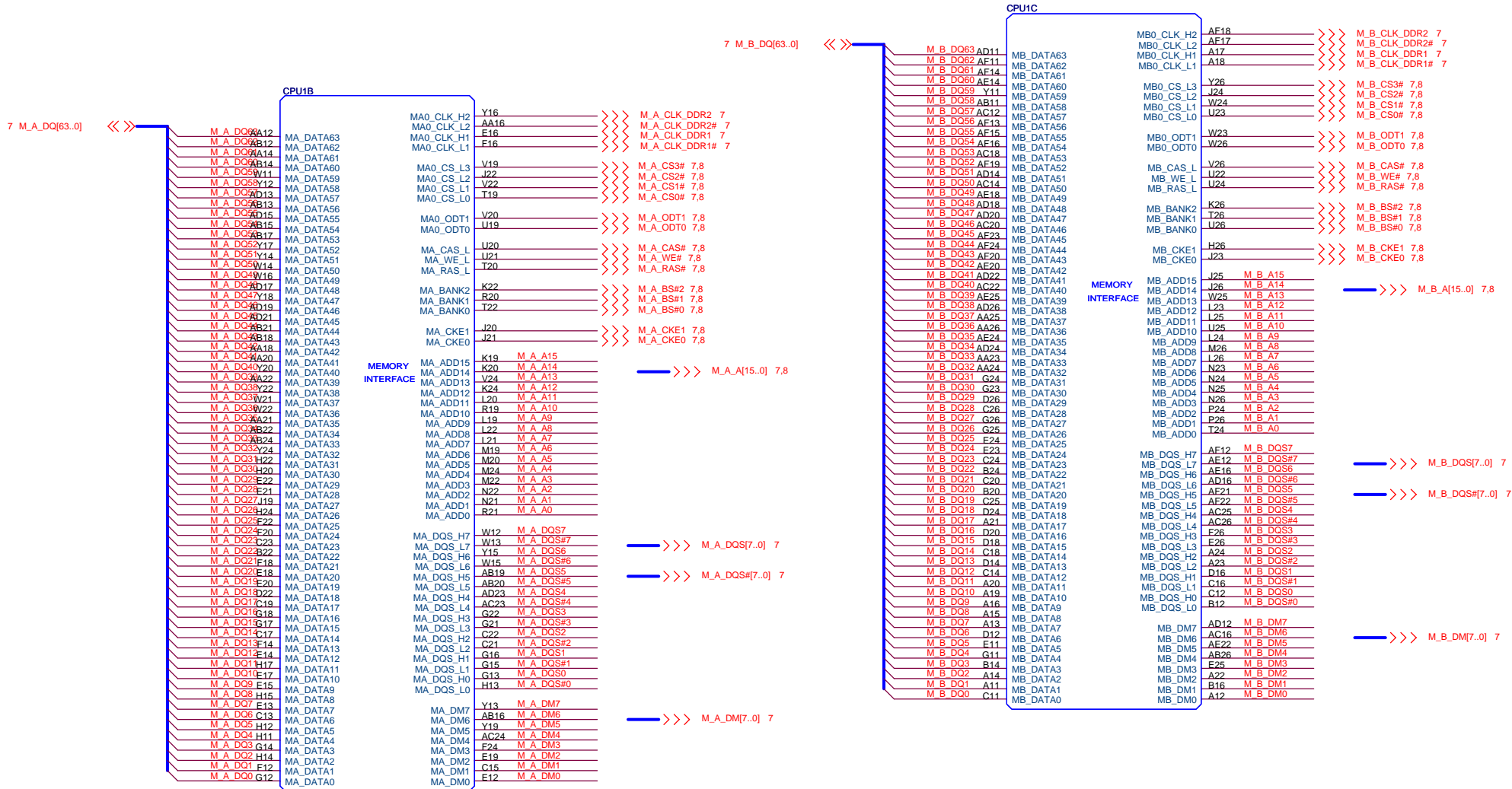
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Date: Tuesday, August 14, 2007 Sheet 1 of 44

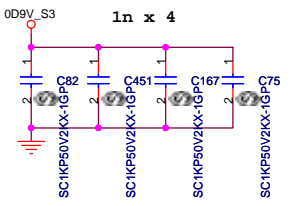
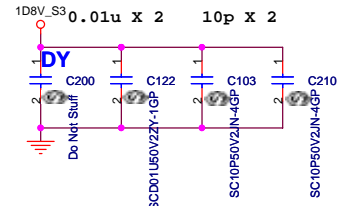
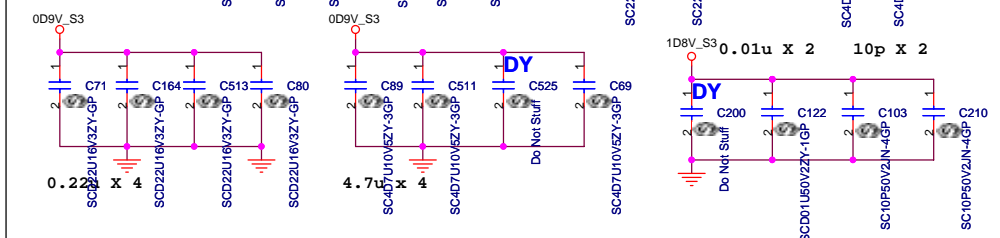
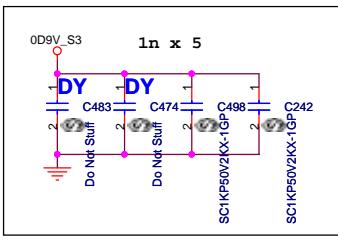
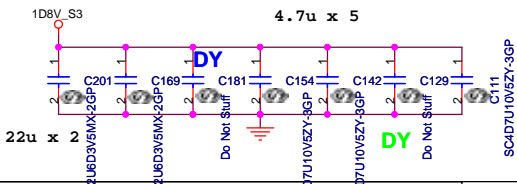
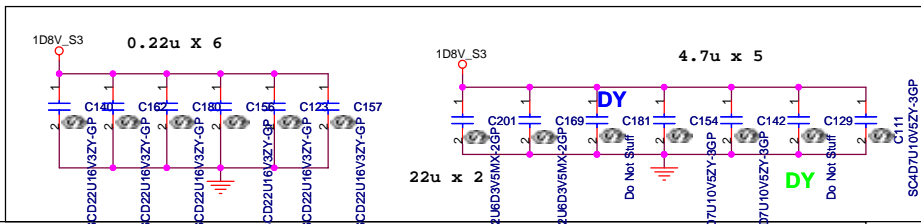
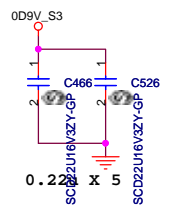
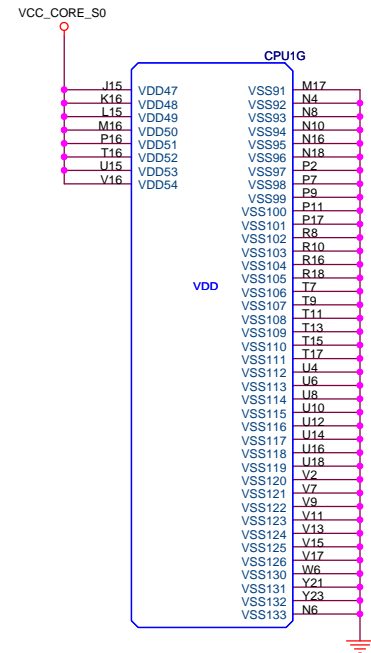
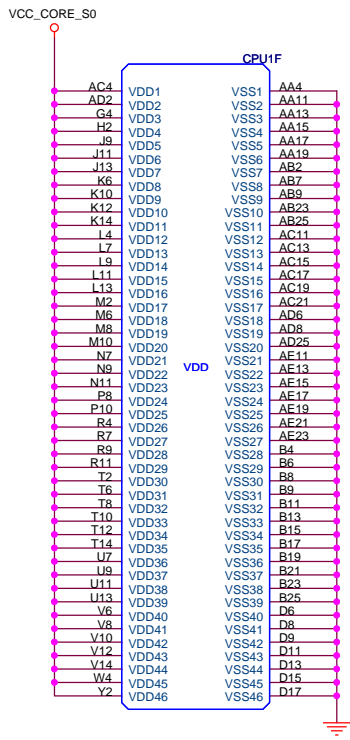
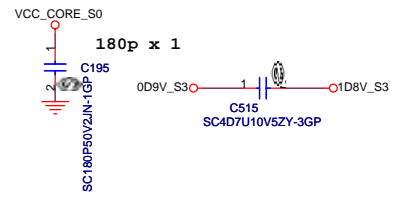
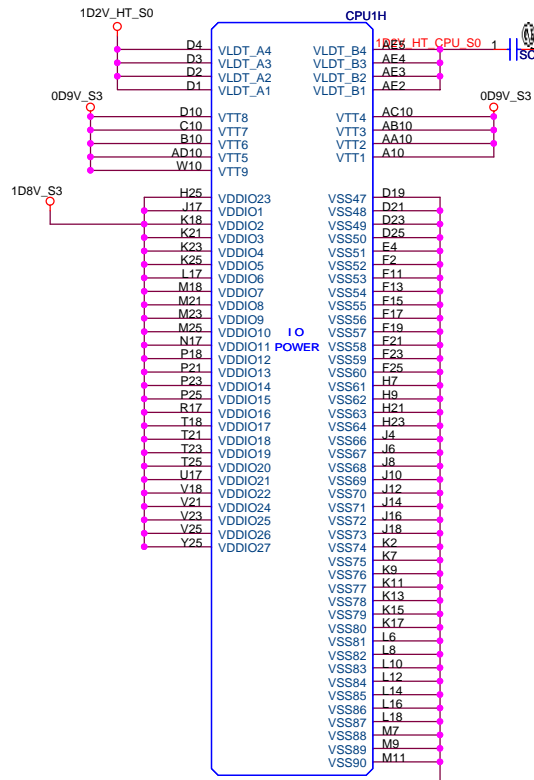




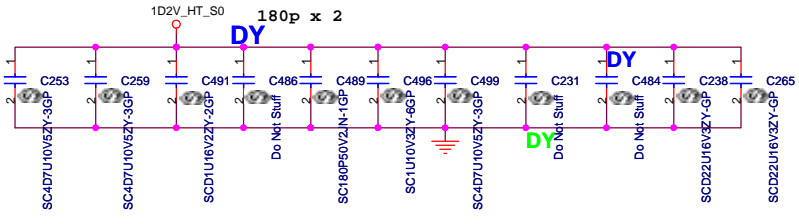
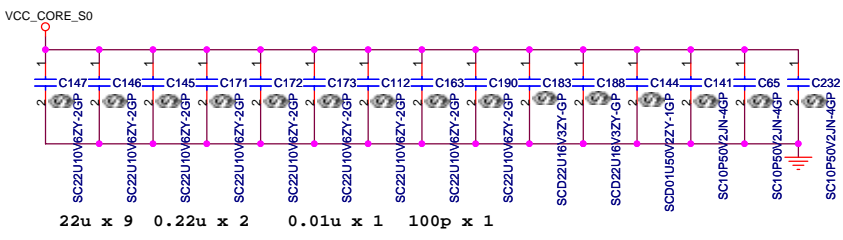
test







LAYOUT: Place on backside of processor.



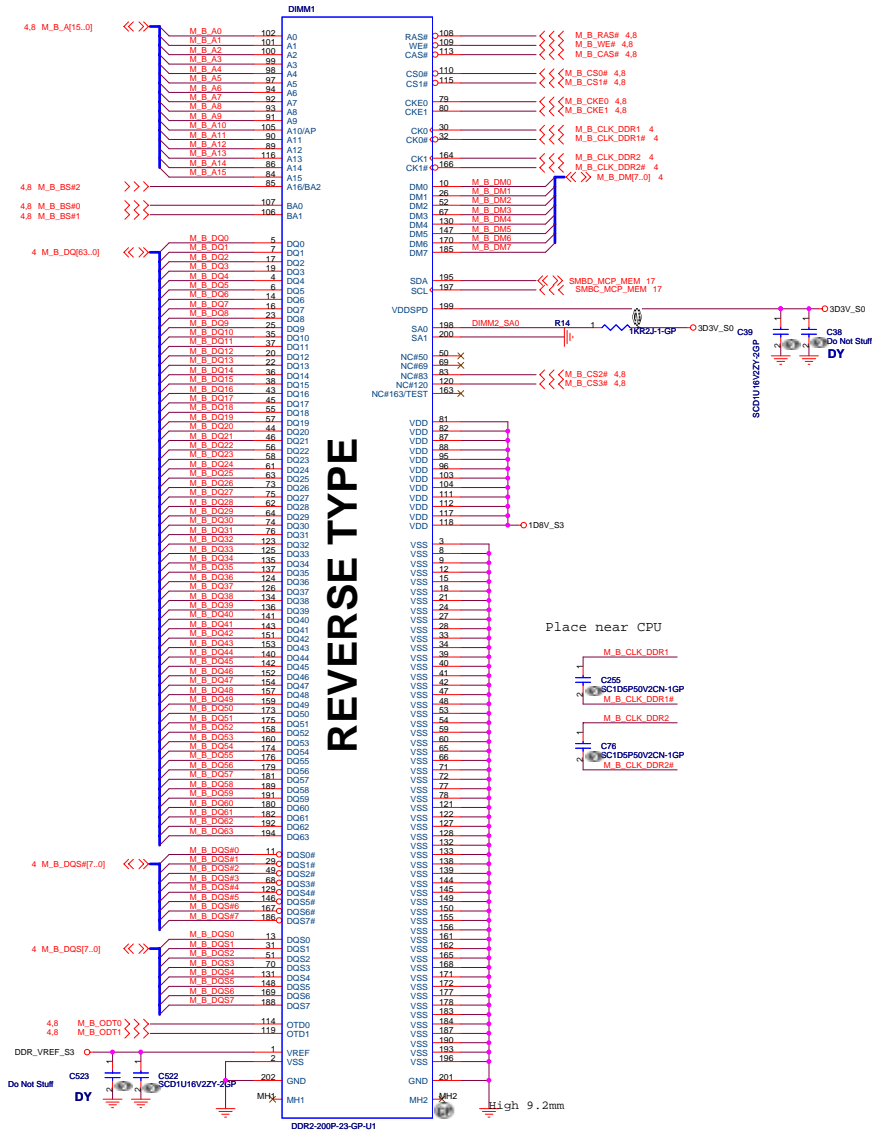
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**緯創資通** **Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(4/4) POWER**

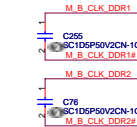
Size: A3 Document Number: **TIBET** Rev: **SA**

Date: Tuesday, August 14, 2007 Sheet 6 of 44



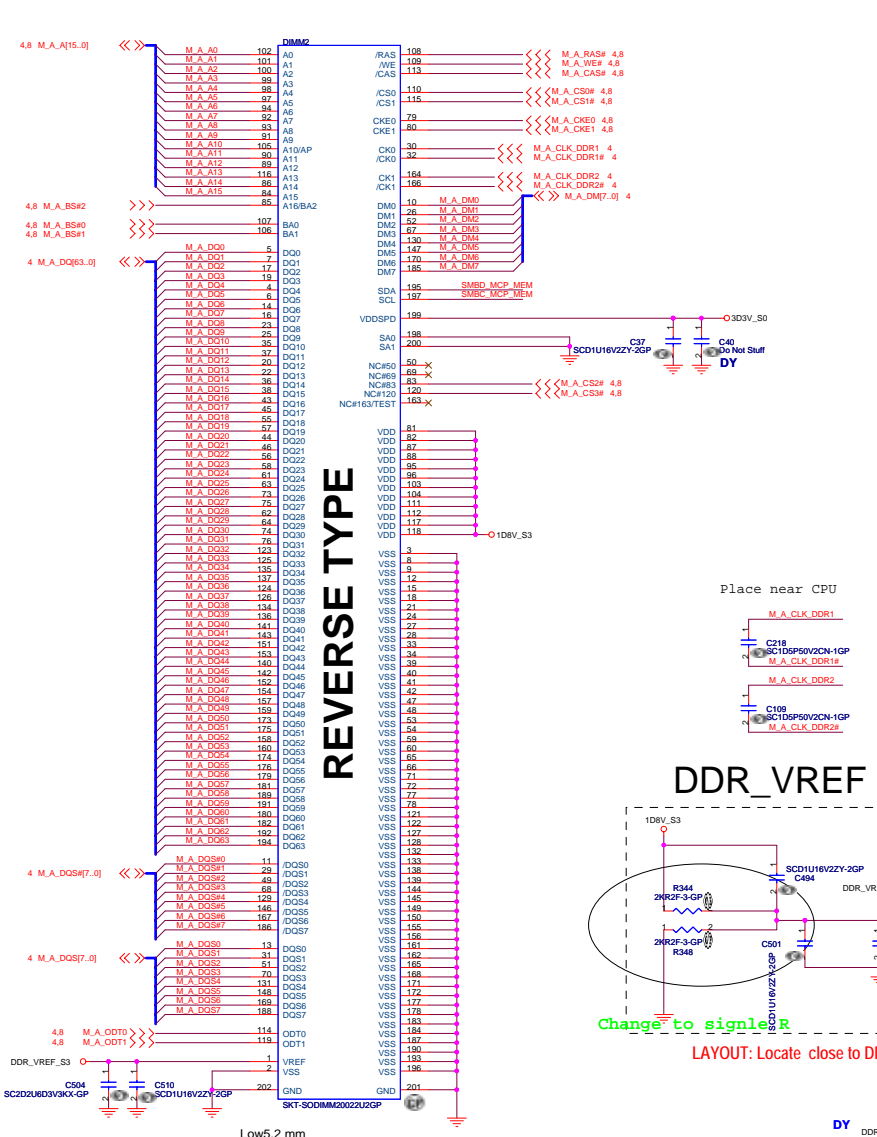
REVERSE TYPE

Place near CPU



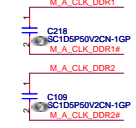
High 9.2 mm

Hi 9.2 mm

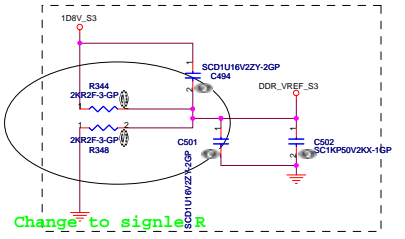


REVERSE TYPE

Place near CPU



### DDR\_VREF



LAYOUT: Locate close to DIMM

Change to signal

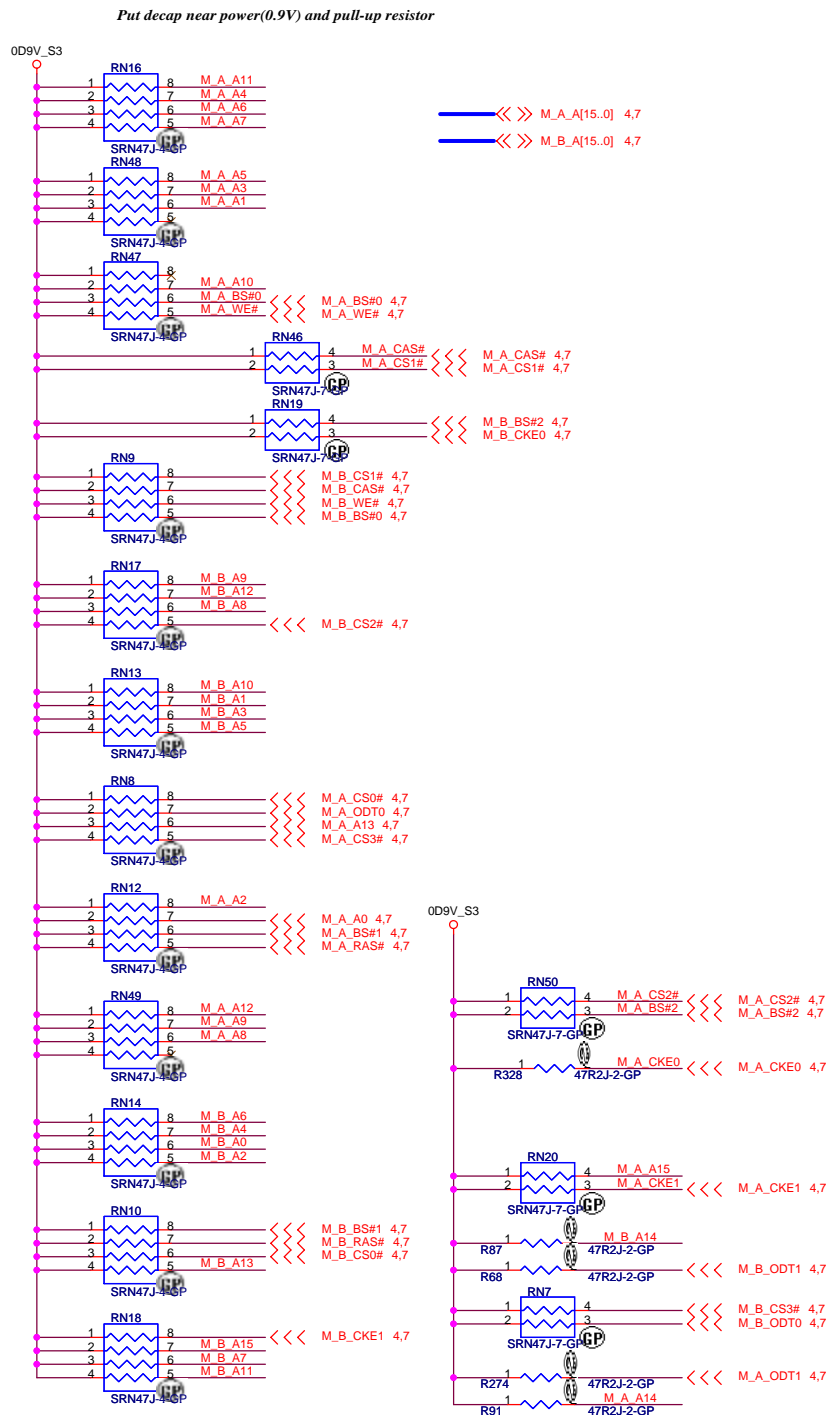
Do Not Stuff

40 VTTREF\_DDR >>>

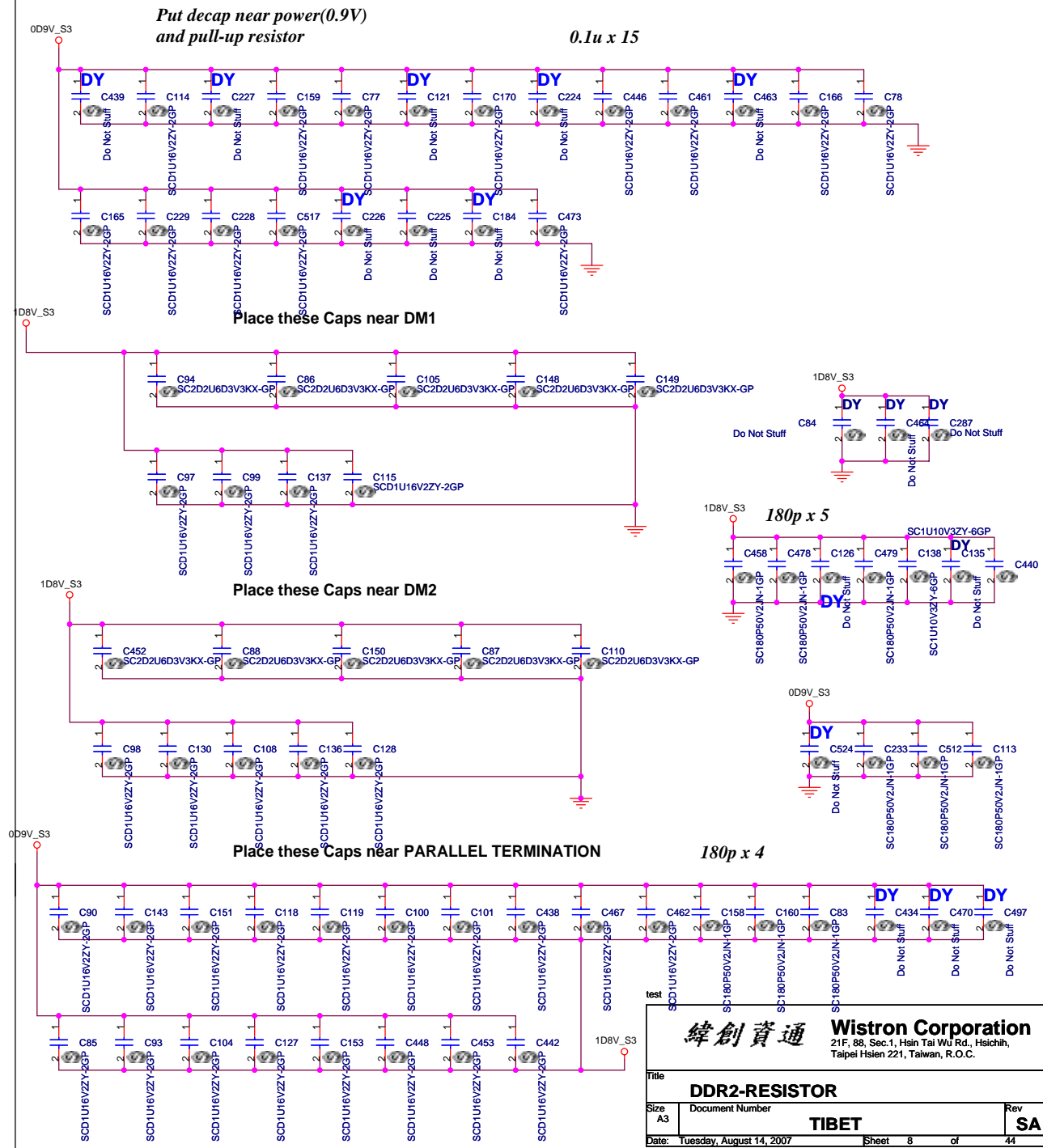
Do Not Stuff



# PARALLEL TERMINATION



# Decoupling Capacitor



緯創資通 Wistron Corporation  
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Title: **DDR2-RESISTOR**

Size: A3 Document Number: **TIBET** Rev: SA

Date: Tuesday, August 14, 2007 Sheet 8 of 44



CPUCADOUT[15..0] 3  
CPUCADOUTJ[15..0] 3

3 NB0CADOUT[15..0] 3  
3 NB0CADOUTJ[15..0] 3

U55A 1 OF 8

HT

CPUCADOUT0	AF16	HT_MCP_RXD0_P	AK27	NB0CADOUT0
CPUCADOUTJ0	AG16	HT_MCP_RXD0_N	AJ27	NB0CADOUTJ0
CPUCADOUT1	AH16	HT_MCP_RXD1_P	AK26	NB0CADOUT1
CPUCADOUTJ1	AJ16	HT_MCP_RXD1_N	AJ26	NB0CADOUTJ1
CPUCADOUT2	AJ15	HT_MCP_RXD2_P	AK25	NB0CADOUT2
CPUCADOUTJ2	AK15	HT_MCP_RXD2_N	AL25	NB0CADOUTJ2
CPUCADOUT3	AK16	HT_MCP_RXD3_P	AL24	NB0CADOUT3
CPUCADOUTJ3	AL16	HT_MCP_RXD3_N	AK24	NB0CADOUTJ3
CPUCADOUT4	AG17	HT_MCP_RXD4_P	AK22	NB0CADOUT4
CPUCADOUTJ4	AF17	HT_MCP_RXD4_N	AL22	NB0CADOUTJ4
CPUCADOUT5	AL17	HT_MCP_RXD5_P	AK21	NB0CADOUT5
CPUCADOUTJ5	AK17	HT_MCP_RXD5_N	AL21	NB0CADOUTJ5
CPUCADOUT6	AL18	HT_MCP_RXD6_P	AJ21	NB0CADOUT6
CPUCADOUTJ6	AK18	HT_MCP_RXD6_N	AJ20	NB0CADOUTJ6
CPUCADOUT7	AJ19	HT_MCP_RXD7_P	AL20	NB0CADOUT7
CPUCADOUTJ7	AK19	HT_MCP_RXD7_N	AM20	NB0CADOUTJ7
CPUCADOUT8	AD14	HT_MCP_RXD8_P	AG27	NB0CADOUT8
CPUCADOUTJ8	AE14	HT_MCP_RXD8_N	AH27	NB0CADOUTJ8
CPUCADOUT9	AF14	HT_MCP_RXD9_P	AE25	NB0CADOUT9
CPUCADOUTJ9	AG14	HT_MCP_RXD9_N	AG25	NB0CADOUTJ9
CPUCADOUT10	AH14	HT_MCP_RXD10_P	AH25	NB0CADOUT10
CPUCADOUTJ10	AJ14	HT_MCP_RXD10_N	AJ25	NB0CADOUTJ10
CPUCADOUT11	AL13	HT_MCP_RXD11_P	AE23	NB0CADOUT11
CPUCADOUTJ11	AK13	HT_MCP_RXD11_N	AE23	NB0CADOUTJ11
CPUCADOUT12	AC15	HT_MCP_RXD12_P	AD21	NB0CADOUT12
CPUCADOUTJ12	AD15	HT_MCP_RXD12_N	AE21	NB0CADOUTJ12
CPUCADOUT13	AD16	HT_MCP_RXD13_P	AE21	NB0CADOUT13
CPUCADOUTJ13	AE16	HT_MCP_RXD13_N	AG21	NB0CADOUTJ13
CPUCADOUT14	AE17	HT_MCP_RXD14_P	AC20	NB0CADOUT14
CPUCADOUTJ14	AD17	HT_MCP_RXD14_N	AD20	NB0CADOUTJ14
CPUCADOUT15	AB17	HT_MCP_RXD15_P	AE19	NB0CADOUT15
CPUCADOUTJ15	AC17	HT_MCP_RXD15_N	AE19	NB0CADOUTJ15

3 CPUHTTCLKOUT0	>>>	CPUHTTCLKOUT0	AJ17	HT_MCP_RX_CLK0_P
3 CPUHTTCLKOUTJ0	>>>	CPUHTTCLKOUTJ0	AH17	HT_MCP_RX_CLK0_N
3 CPUHTTCLKOUT1	>>>	CPUHTTCLKOUT1	AL14	HT_MCP_RX_CLK1_P
3 CPUHTTCLKOUTJ1	>>>	CPUHTTCLKOUTJ1	AK14	HT_MCP_RX_CLK1_N

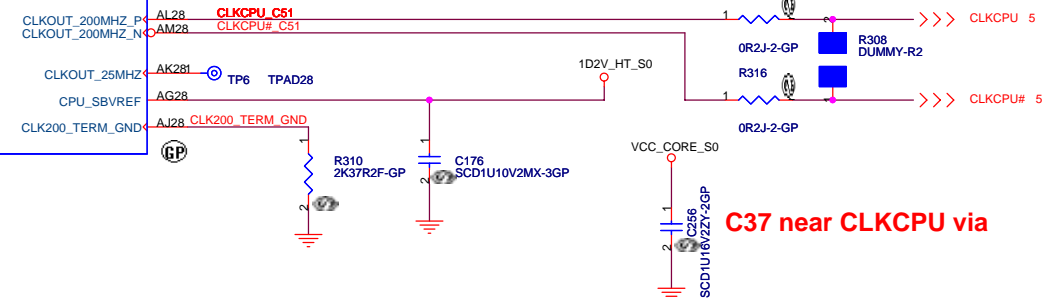
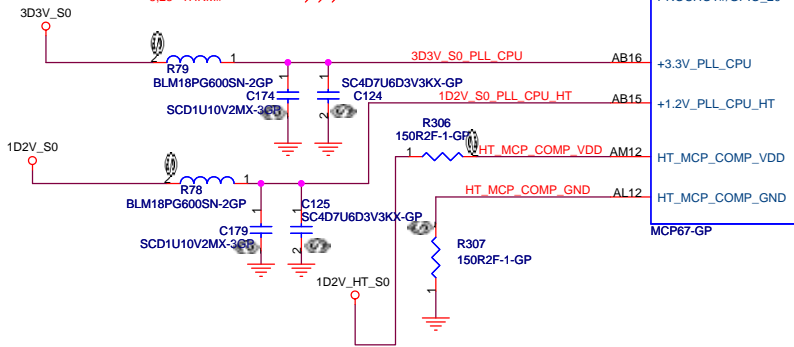
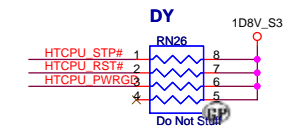
HT_MCP_TX_CLK0_P	AK23	NB0HTTCLKOUT0	>>>	NB0HTTCLKOUT0 3
HT_MCP_TX_CLK0_N	AJ23	NB0HTTCLKOUTJ0	>>>	NB0HTTCLKOUTJ0 3
HT_MCP_TX_CLK1_P	AG23	NB0HTTCLKOUT1	>>>	NB0HTTCLKOUT1 3
HT_MCP_TX_CLK1_N	AH23	NB0HTTCLKOUTJ1	>>>	NB0HTTCLKOUTJ1 3

3 CPUHTTCTLOUT0	>>>	CPUHTTCTLOUT0	AH19	HT_MCP_RXCTL0_P
3 CPUHTTCTLOUTJ0	>>>	CPUHTTCTLOUTJ0	AG19	HT_MCP_RXCTL0_N
			AC18	RESERVED#AC18
			AD18	RESERVED#AD18

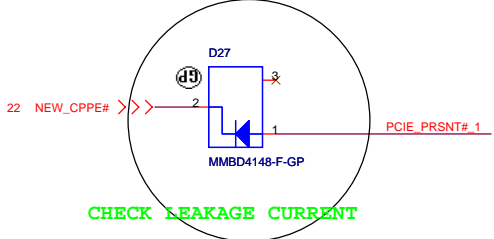
HT_MCP_TXCTL0_P	AK20	NB0HTTCTLOUT 3	>>>	NB0HTTCTLOUT 3
HT_MCP_TXCTL0_N	AJ20	NB0HTTCTLOUTJ 3	>>>	NB0HTTCTLOUTJ 3
RESERVED#AD19	AD19			
RESERVED#AC19	AC19			

5 CPU_THERMTRIP#	>>>	AC13	THERMTRIP#/GPIO_58
5.23 THRM#	>>>	AB13	PROCHOT#/GPIO_20

HT_MCP_REQ#	AD23	HT_CPU_REQ#	1
HT_MCP_STOP#	AB20		
HT_MCP_RST#	AC21		
HT_MCP_PWRGD	AD22		



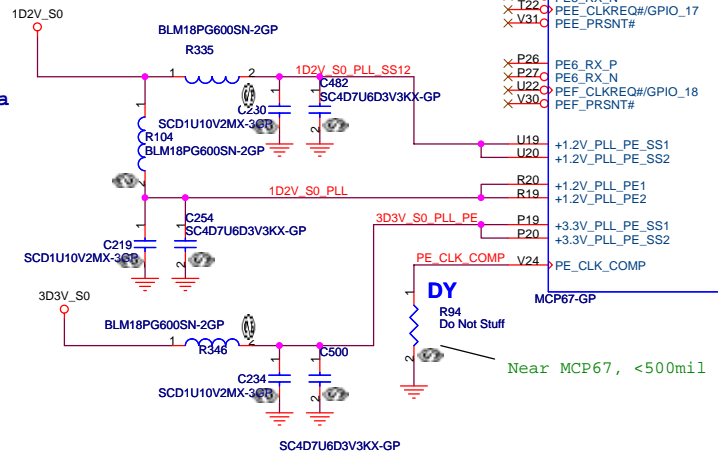
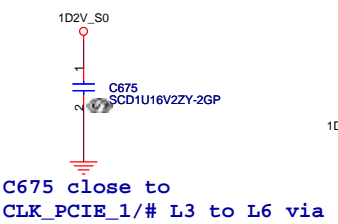
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NEW CARD

MINI CARD1

MINI CARD2

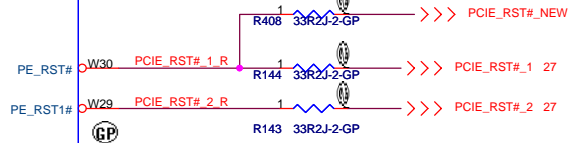


U55B 2 OF 8

F23	PE0_RX0_P	D24	PE0_TX0_P
G23C	PE0_RX0_N	C24	PE0_TX0_N
F24	PE0_RX1_P	A24	PE0_TX1_P
F25C	PE0_RX1_N	B24	PE0_TX1_N
D25	PE0_RX2_P	B25	PE0_TX2_P
D26C	PE0_RX2_N	C25	PE0_TX2_N
C28	PE0_RX3_P	B26	PE0_TX3_P
C29C	PE0_RX3_N	C26	PE0_TX3_N
C30	PE0_RX4_P	C27	PE0_TX4_P
D29	PE0_RX4_N	D27	PE0_TX4_N
D30C	PE0_RX5_P	A28	PE0_TX5_P
F26	PE0_RX5_N	B28	PE0_TX5_N
F27C	PE0_RX6_P	A29	PE0_TX6_P
F28	PE0_RX6_N	B29	PE0_TX6_N
F29	PE0_RX7_P	A30	PE0_TX7_P
H23	PE0_RX7_N	B30	PE0_TX7_N
H24C	PE0_RX8_P	B31	PE0_TX8_P
H25	PE0_RX8_N	B32	PE0_TX8_N
H26C	PE0_RX9_P	C31	PE0_TX9_P
H27	PE0_RX9_N	D31	PE0_TX9_N
H28	PE0_RX10_P	D32	PE0_TX10_P
K24	PE0_RX10_N	E31	PE0_TX10_N
K25C	PE0_RX11_P	E30	PE0_TX11_P
K27	PE0_RX11_N	F31	PE0_TX11_N
K28	PE0_RX12_P	F30	PE0_TX12_P
K29C	PE0_RX12_N	G29	PE0_TX12_N
J31	PE0_RX13_P	G30	PE0_TX13_P
J30C	PE0_RX13_N	H29	PE0_TX13_N
K31	PE0_RX14_P	H30	PE0_TX14_P
K30C	PE0_RX14_N	H31	PE0_TX14_N
	PE0_RX15_P	H32	PE0_TX15_P
	PE0_RX15_N	H31	PE0_TX15_N

Near Connector, <500mil

For New\_Card

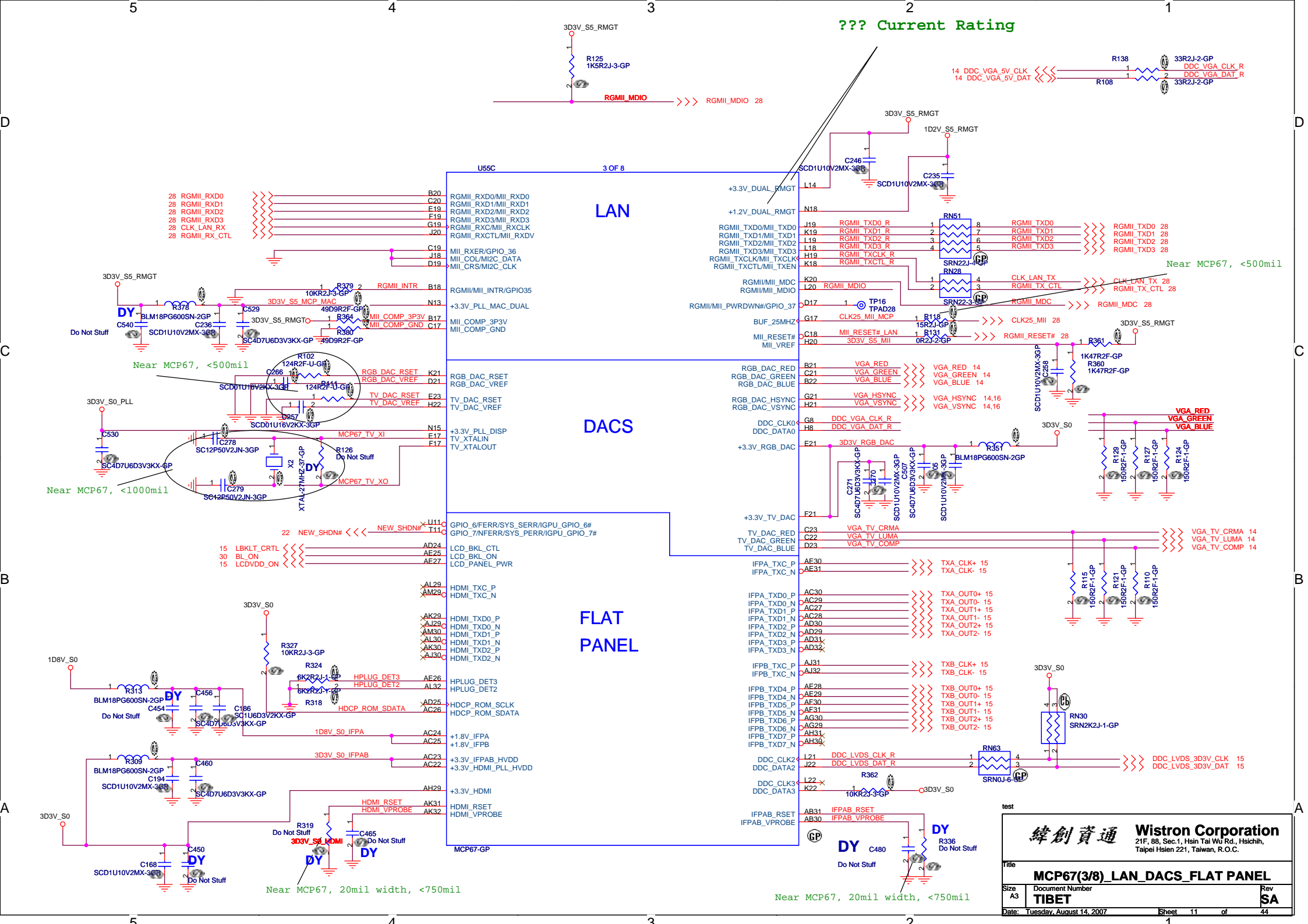


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**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP67(2/8)\_PCIE**

Size: A3	Document Number: <b>TIBET</b>	Rev: <b>SA</b>
Date: Tuesday, August 14, 2007	Sheet: 10	of: 44



??? Current Rating

LAN

DACS

FLAT PANEL

Near MCP67, <500mil

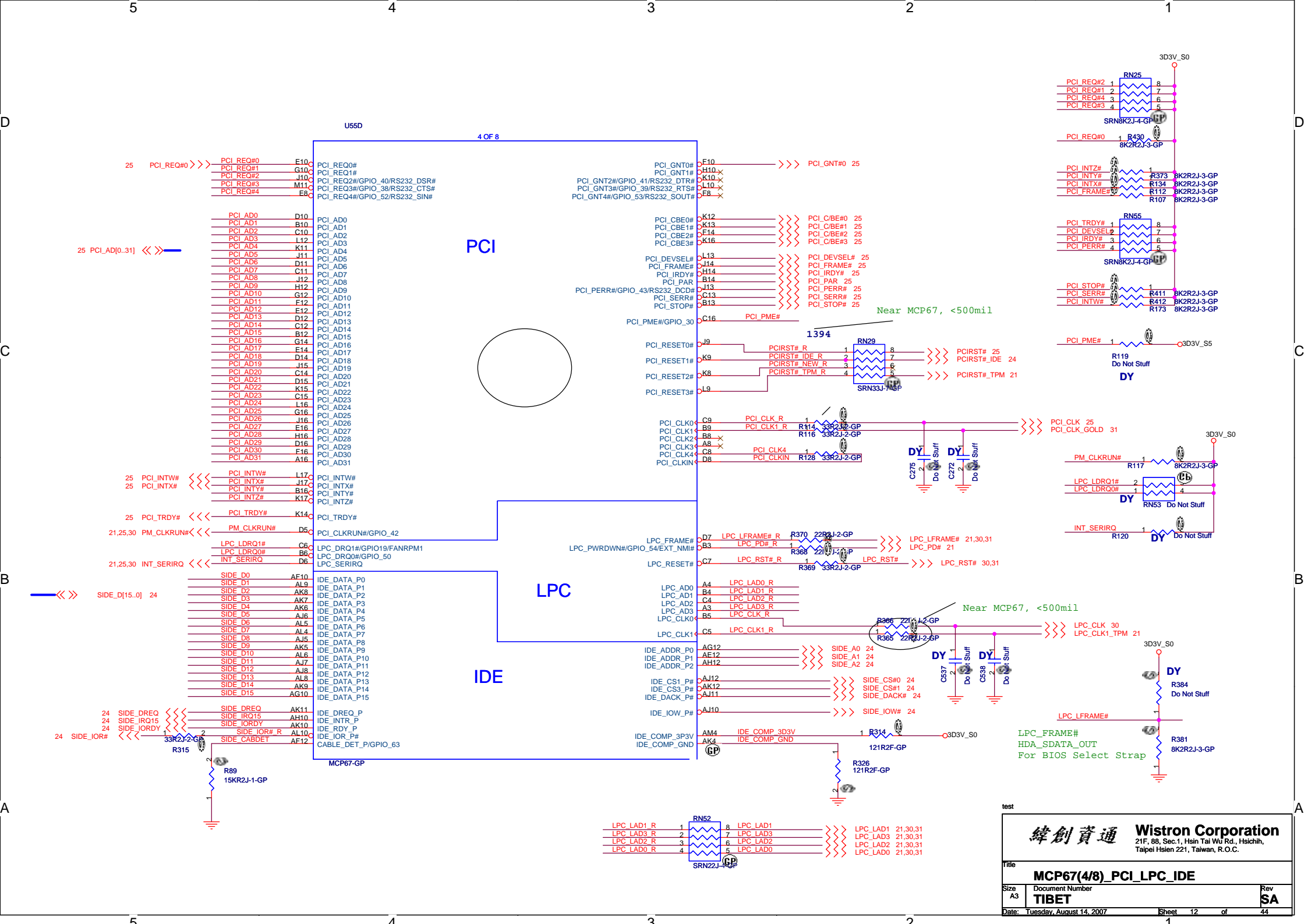
Near MCP67, <500mil

Near MCP67, <1000mil

Near MCP67, 20mil width, <750mil

Near MCP67, 20mil width, <750mil

<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>MCP67(3/8)_LAN_DACS_FLAT_PANEL</b>	
Title	Document Number
Size A3	<b>TIBET</b>
Date: Tuesday, August 14, 2007	Sheet 11 of 44
Rev SA	







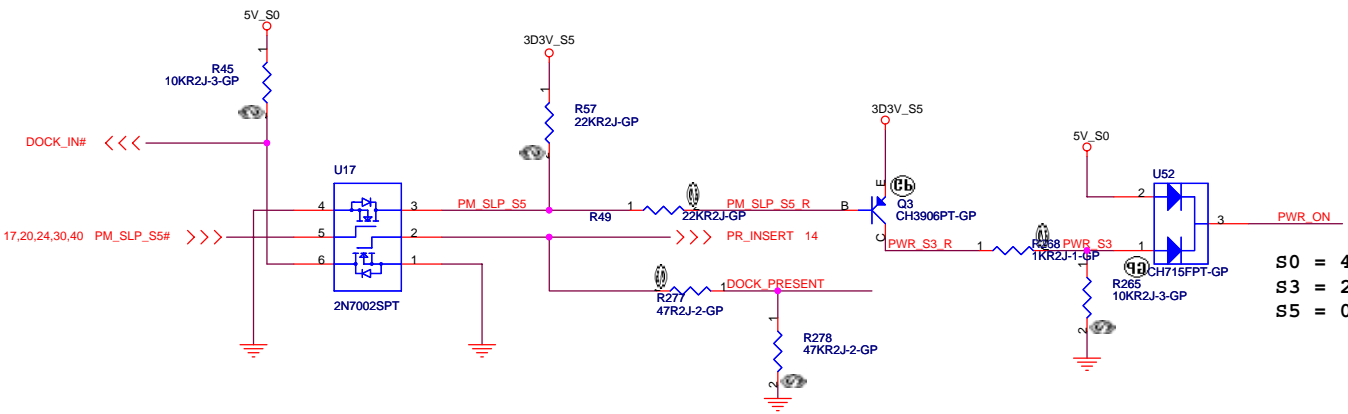
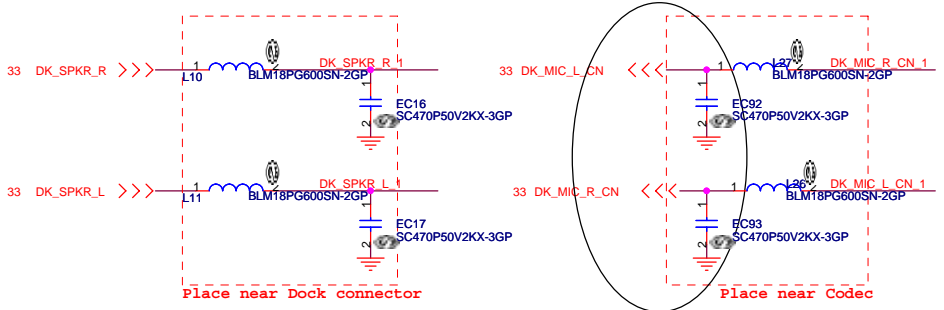
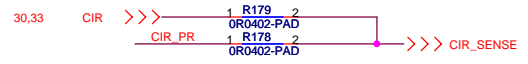
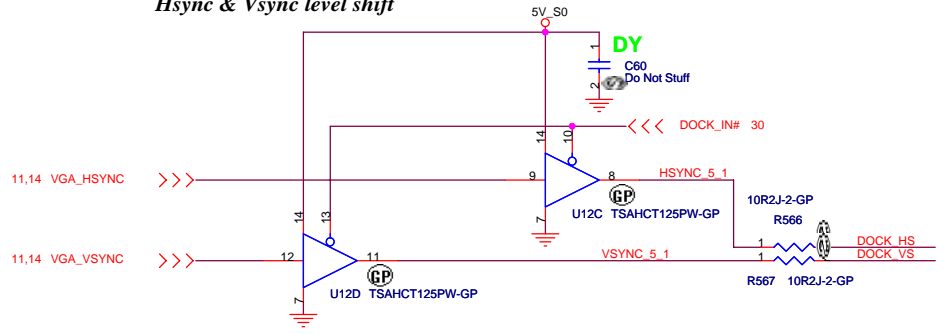




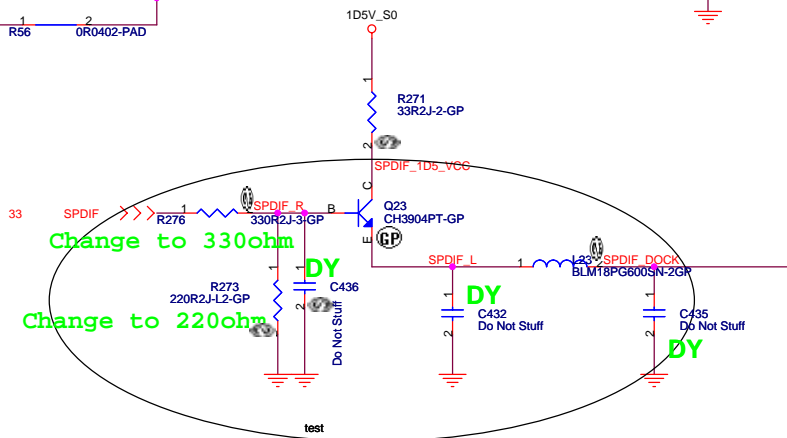
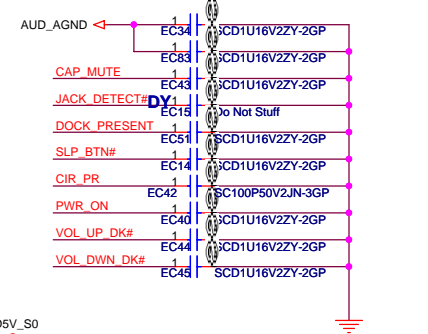
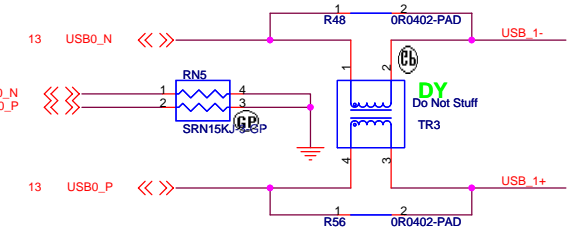
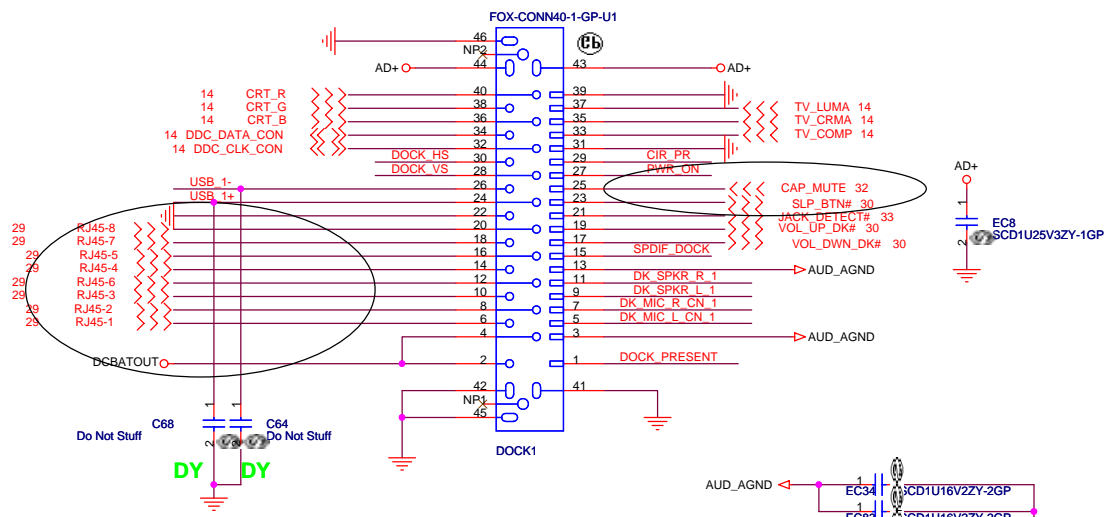


# Docking Connector

## Hsync & Vsync level shift



S0 = 4V  
S3 = 2.5V  
S5 = 0V

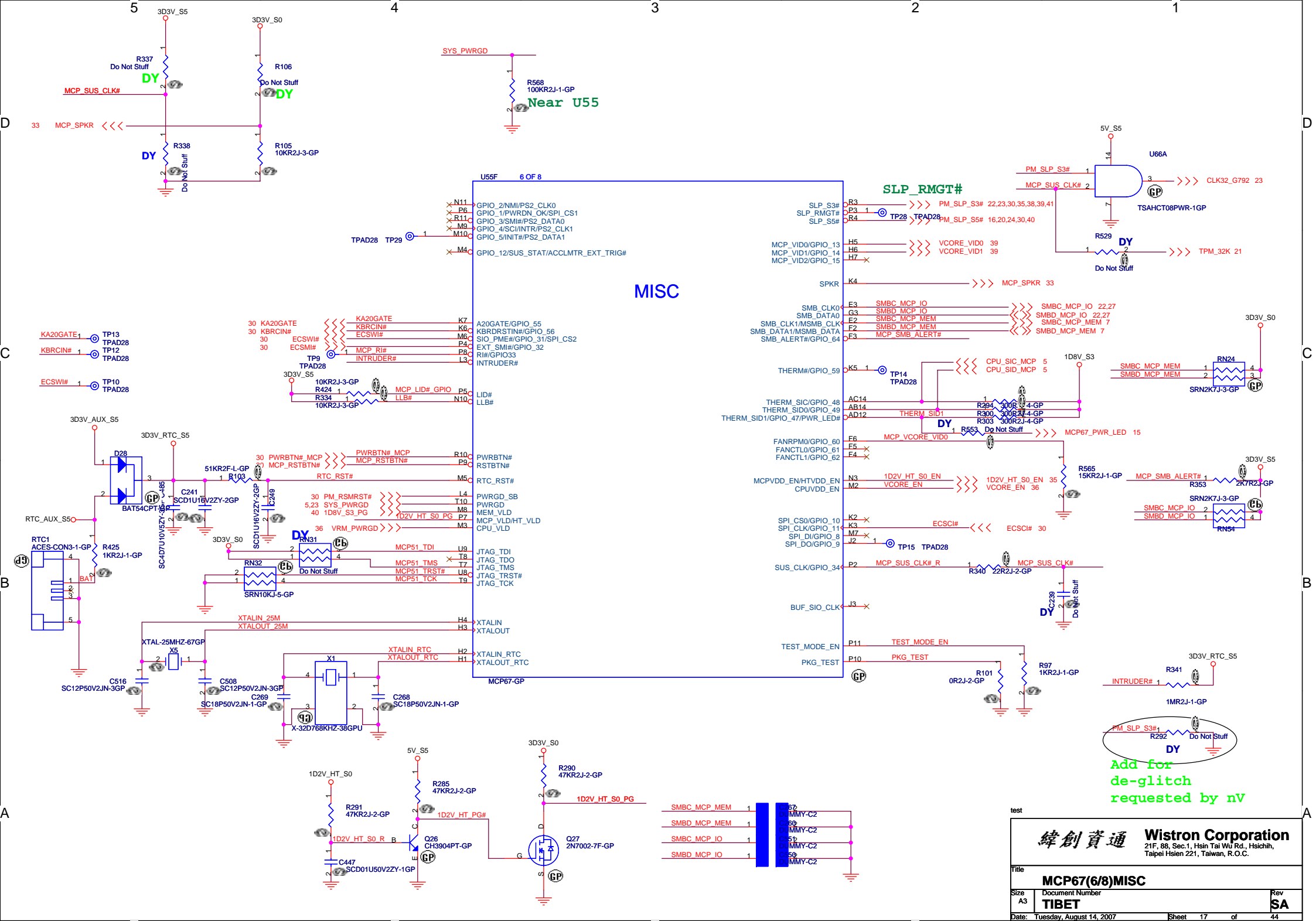


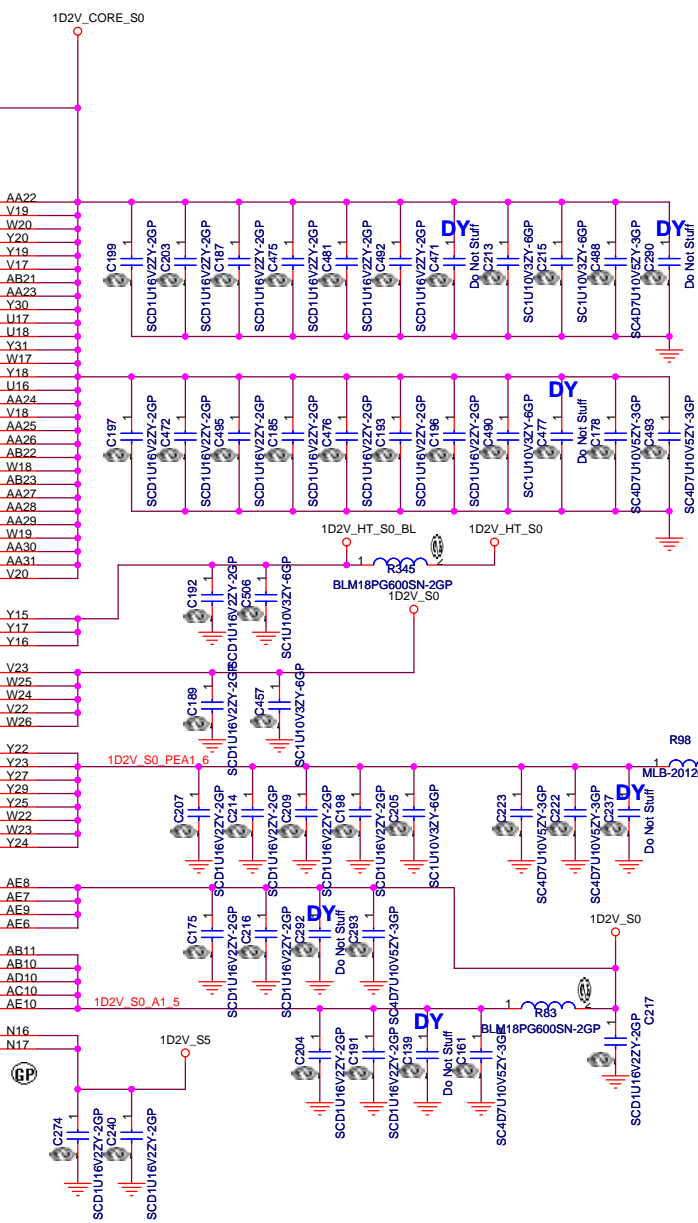
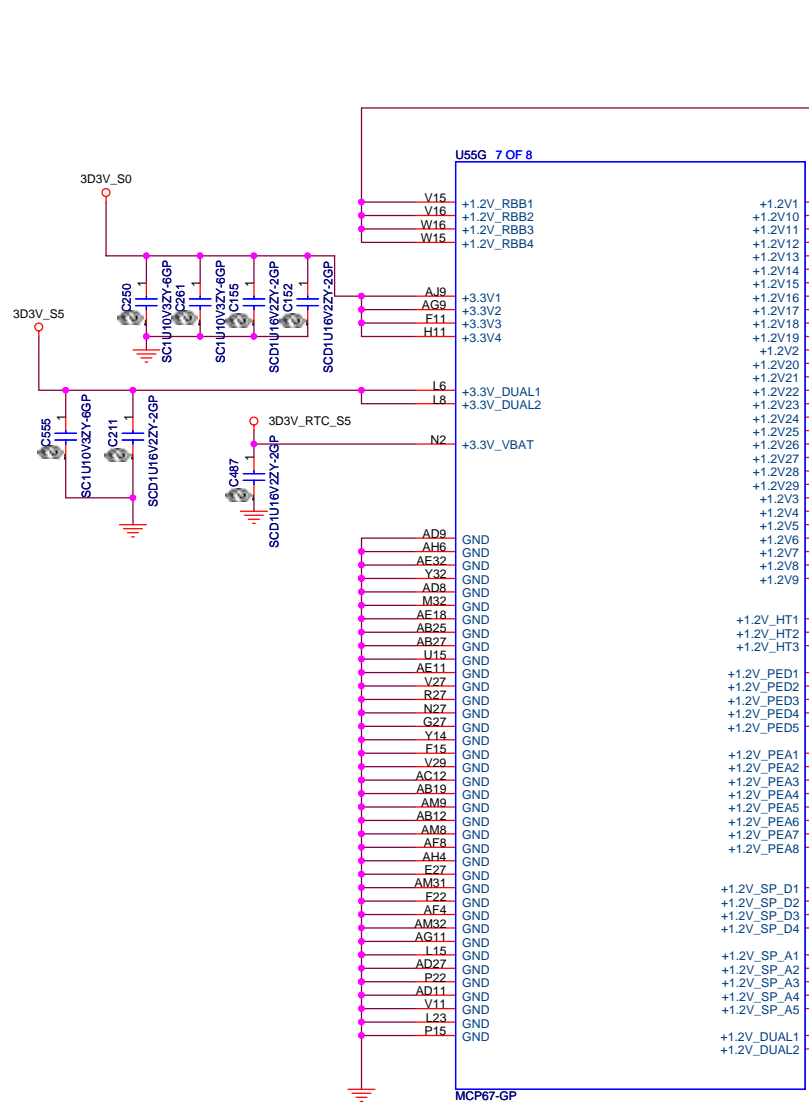
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Board to board conn/ Docking**

Size A3	Document Number	Rev
	<b>TIBET</b>	<b>SA</b>

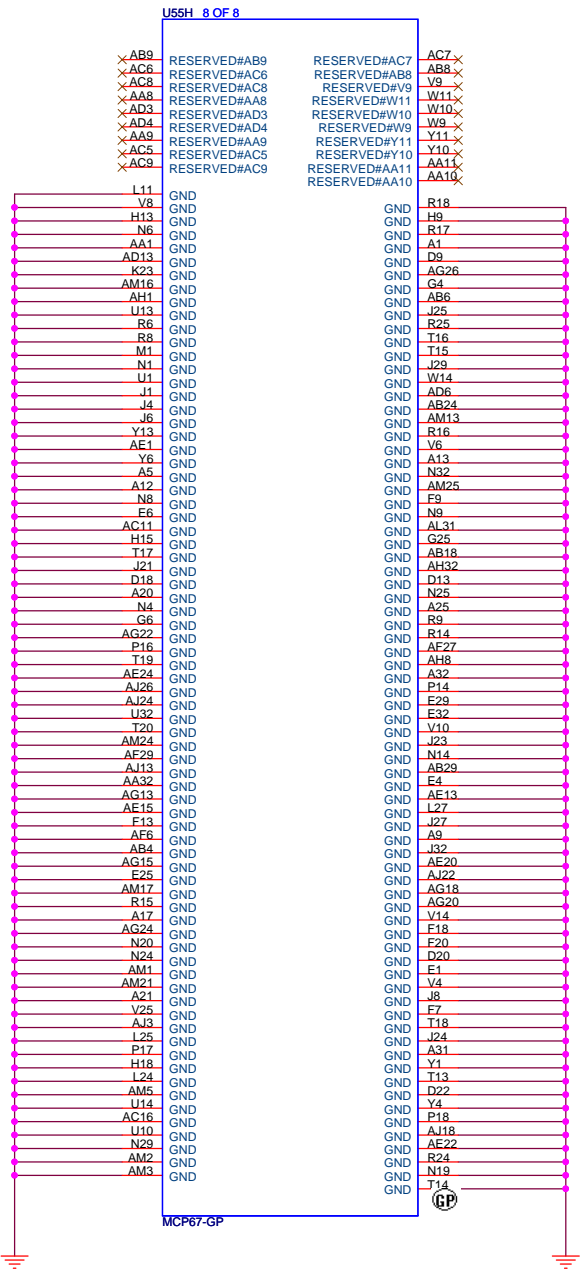
Date: Tuesday, August 14, 2007 Sheet 16 of 44



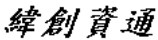


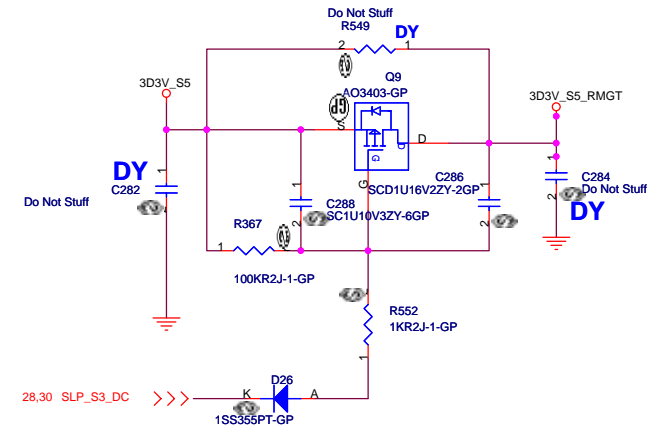
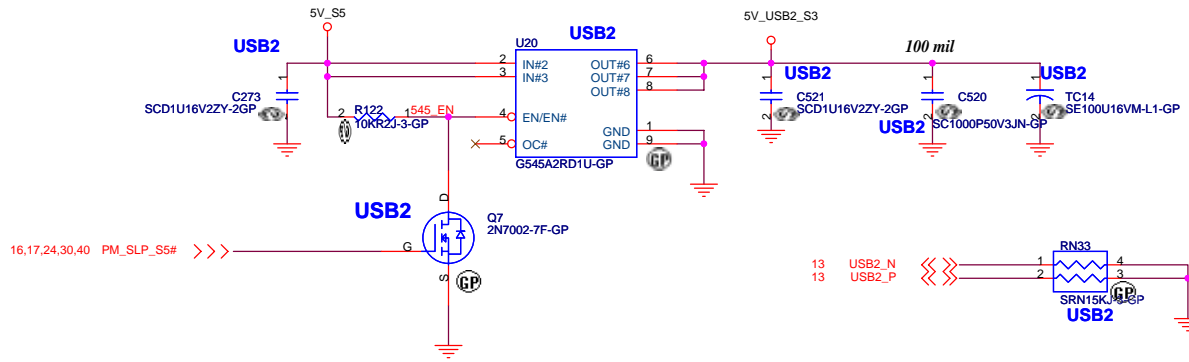
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<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: <b>MCP67(7/8)_POWER</b>			
Size: A3	Document Number: <b>TIBET</b>		Rev: <b>SA</b>
Date: Tuesday, August 14, 2007	Sheet: 18 of 44		

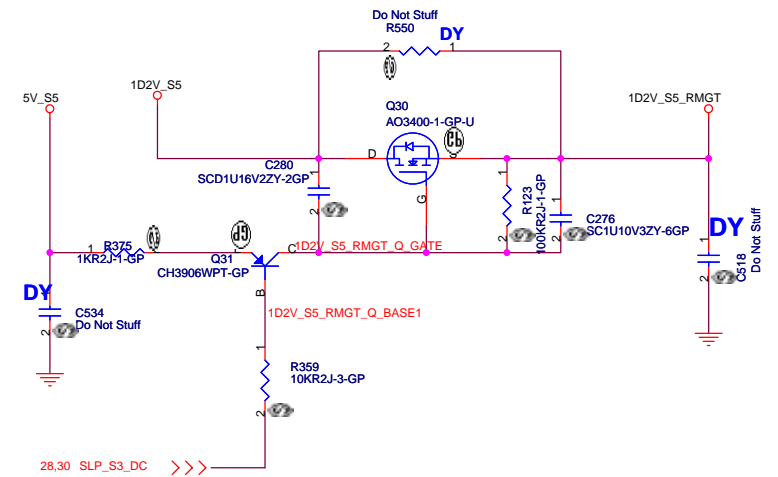
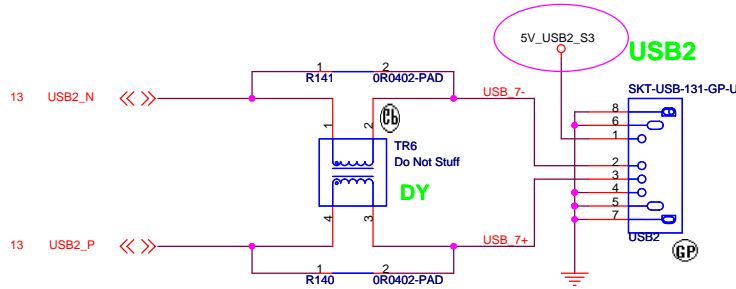


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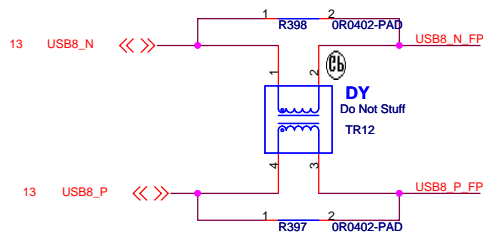
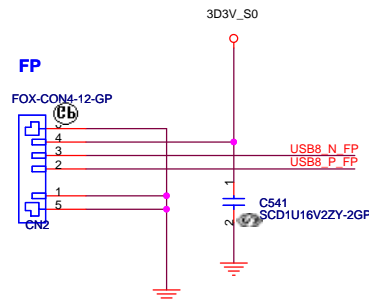
 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> <b>MCP67(8/8)_GND</b>	
<b>Size</b> A3	<b>Document Number</b> <b>TIBET</b>
<b>Date:</b> Tuesday, August 14, 2007	<b>Rev</b> <b>SA</b>
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??? Current Rating

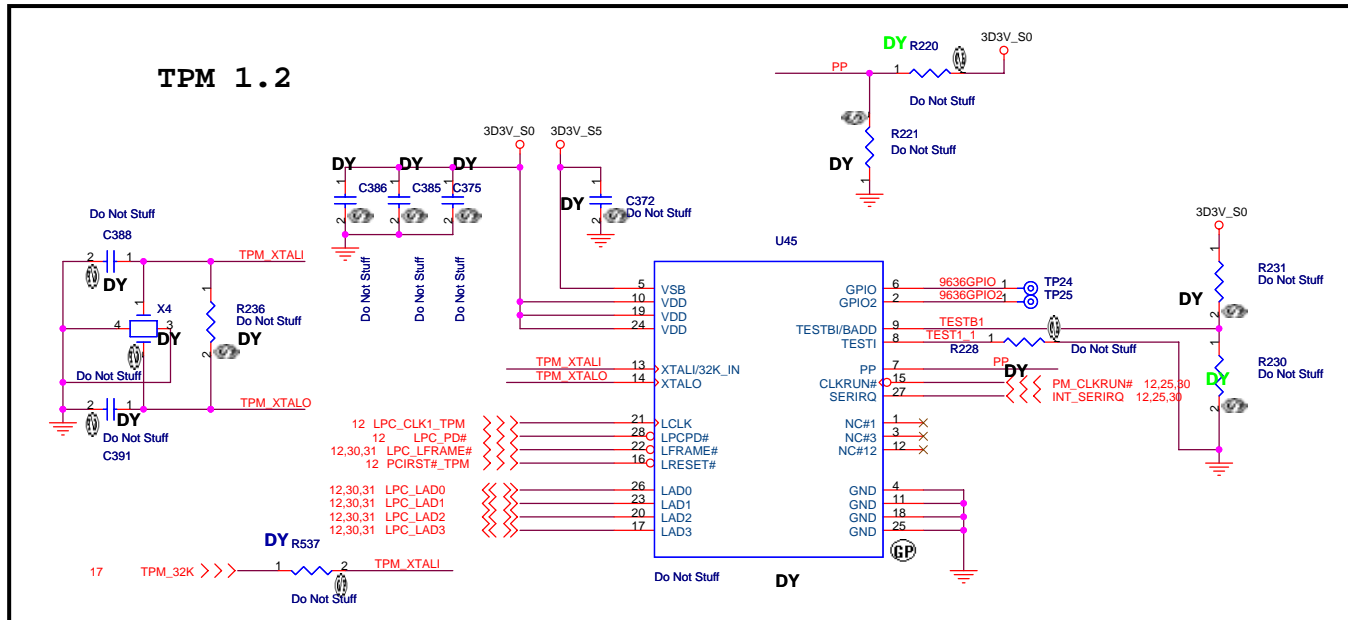


Finger Printer



test

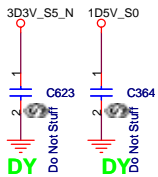
<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title <b>HDMI/FINGER PRINTER</b></p>	
Size A3	Document Number <b>TIBET</b>
Date: Tuesday, August 14, 2007	Sheet 20 of 44
	Rev <b>SA</b>



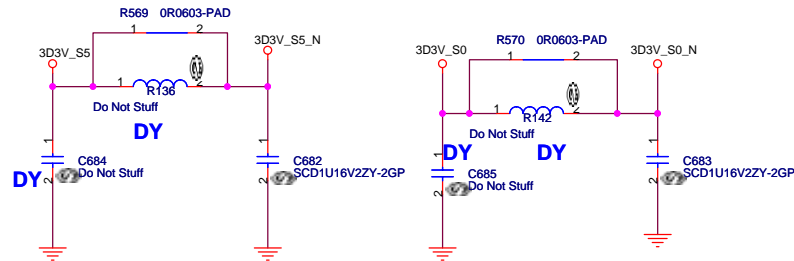
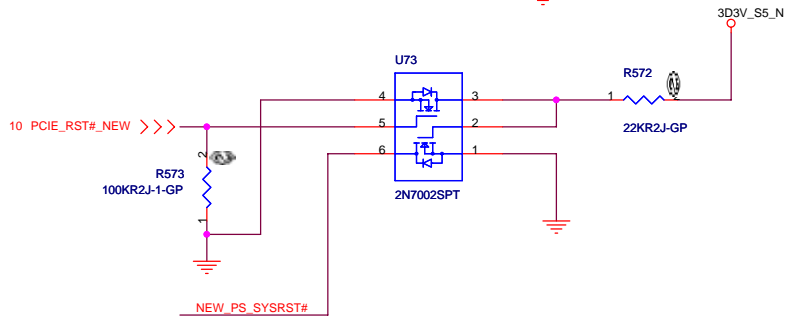
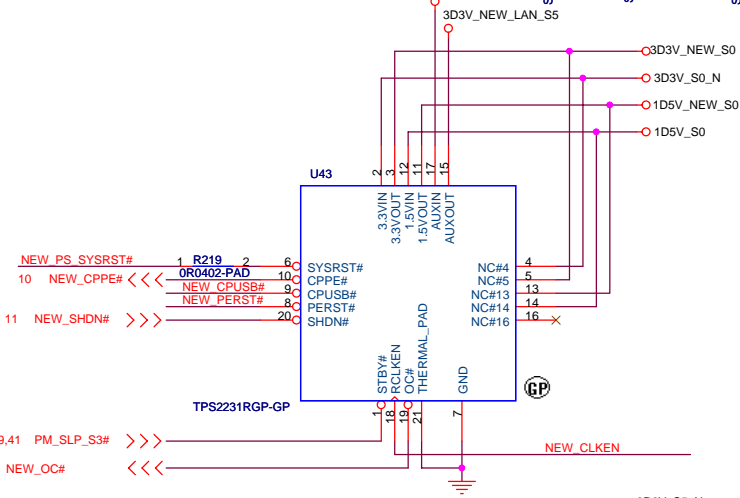
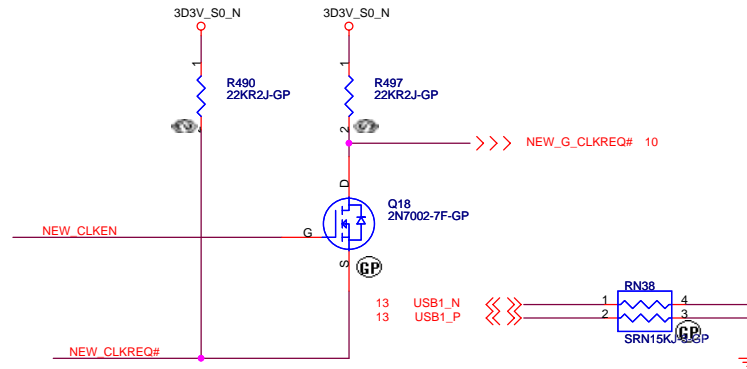
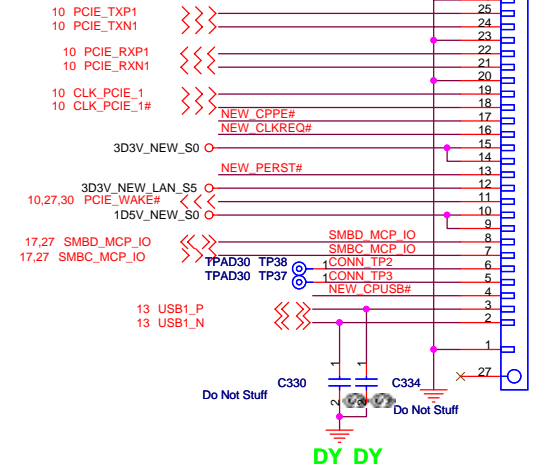
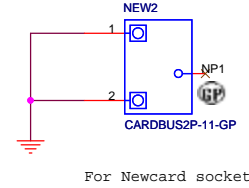
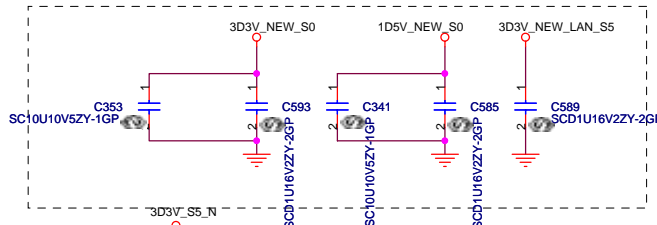
test

# NEWCARD Connector

Place them Near to Chip



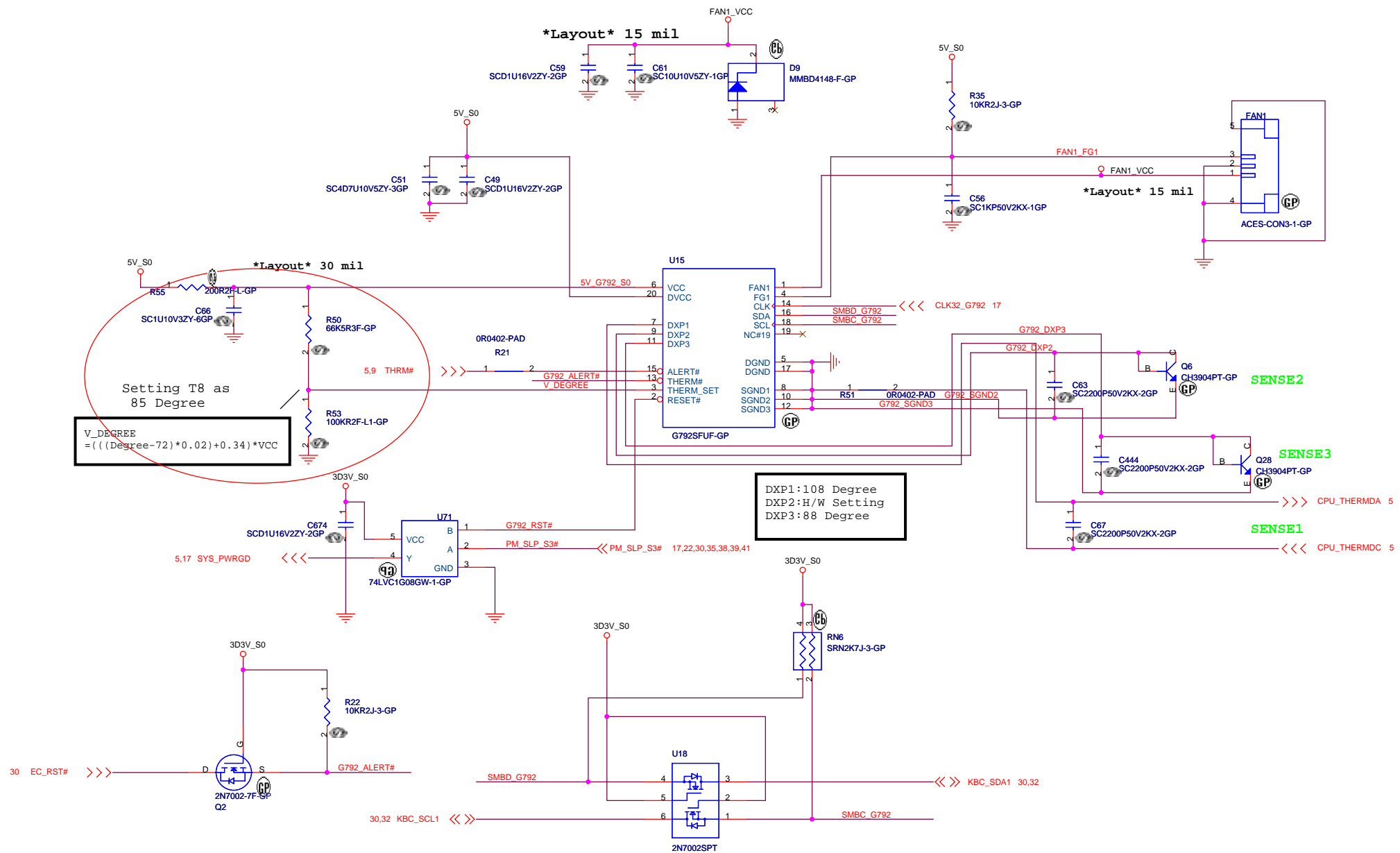
Place them Near to Connector



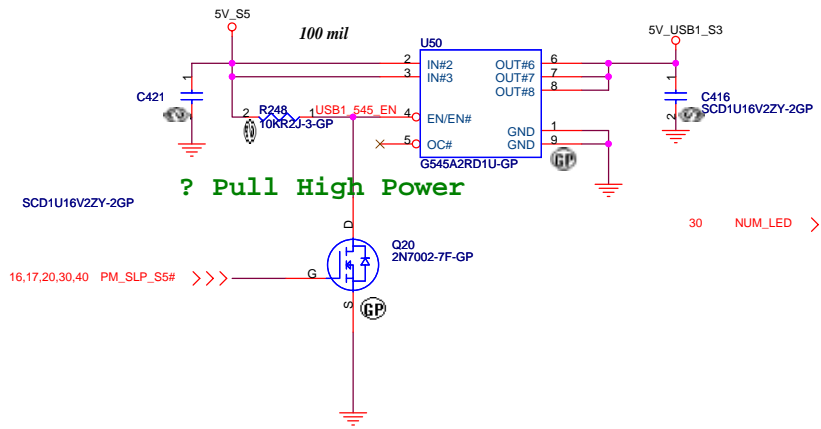
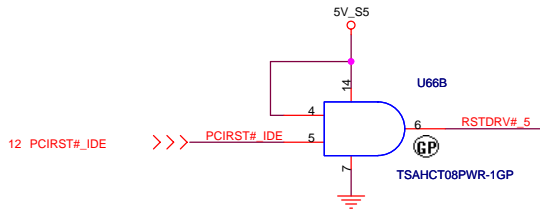
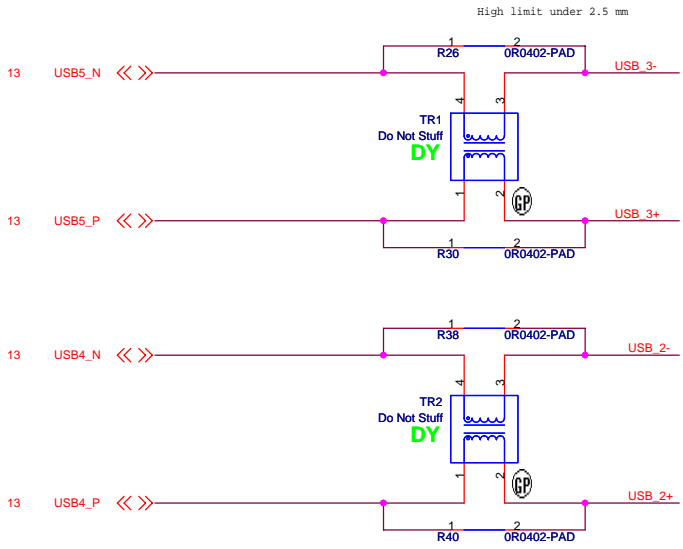
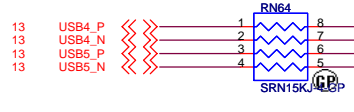
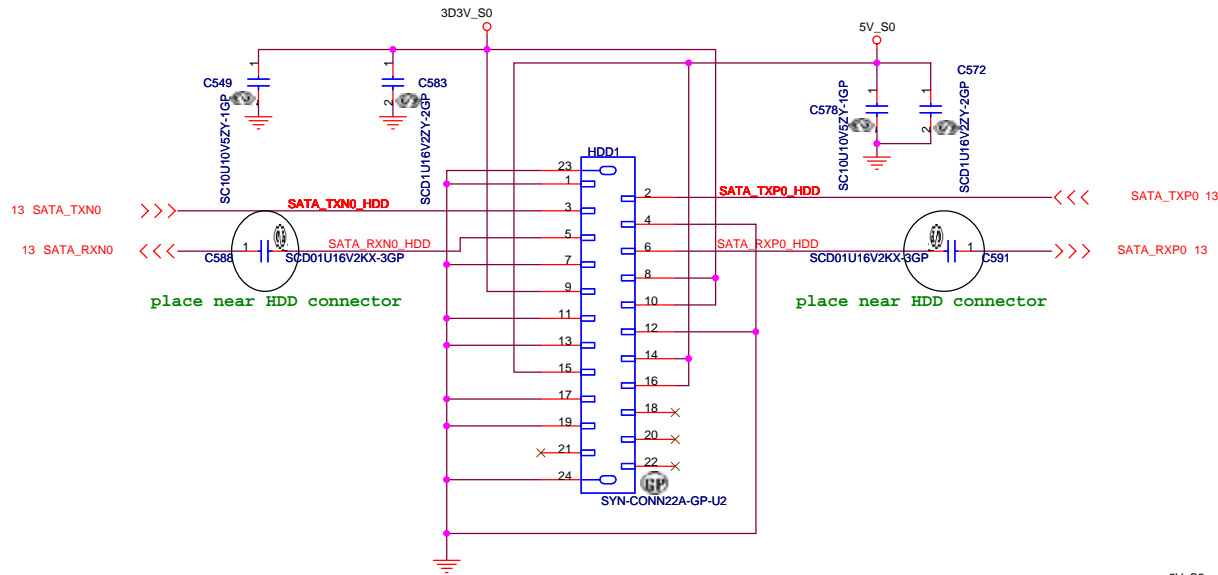
test

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>NEW CARD</b>			
Size A3	Document Number <b>TIBET</b>		Rev <b>SA</b>
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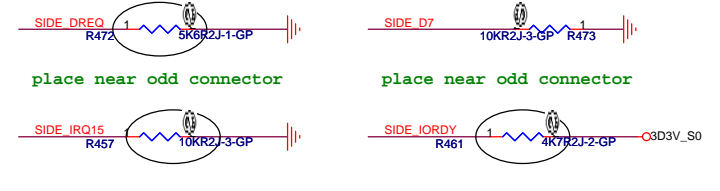
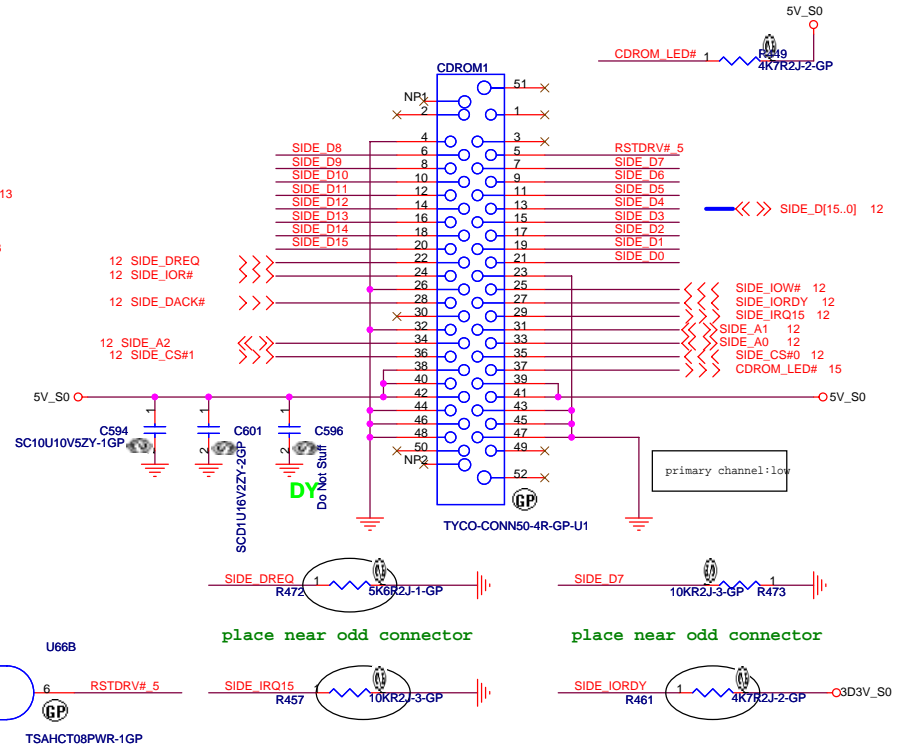




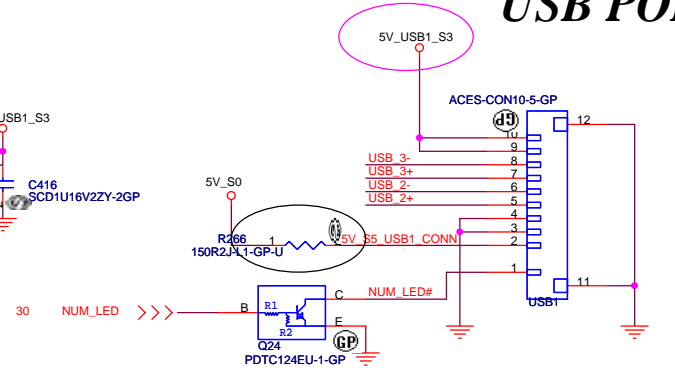
# SATA HD Connector



# CD-ROM CONNECTOR



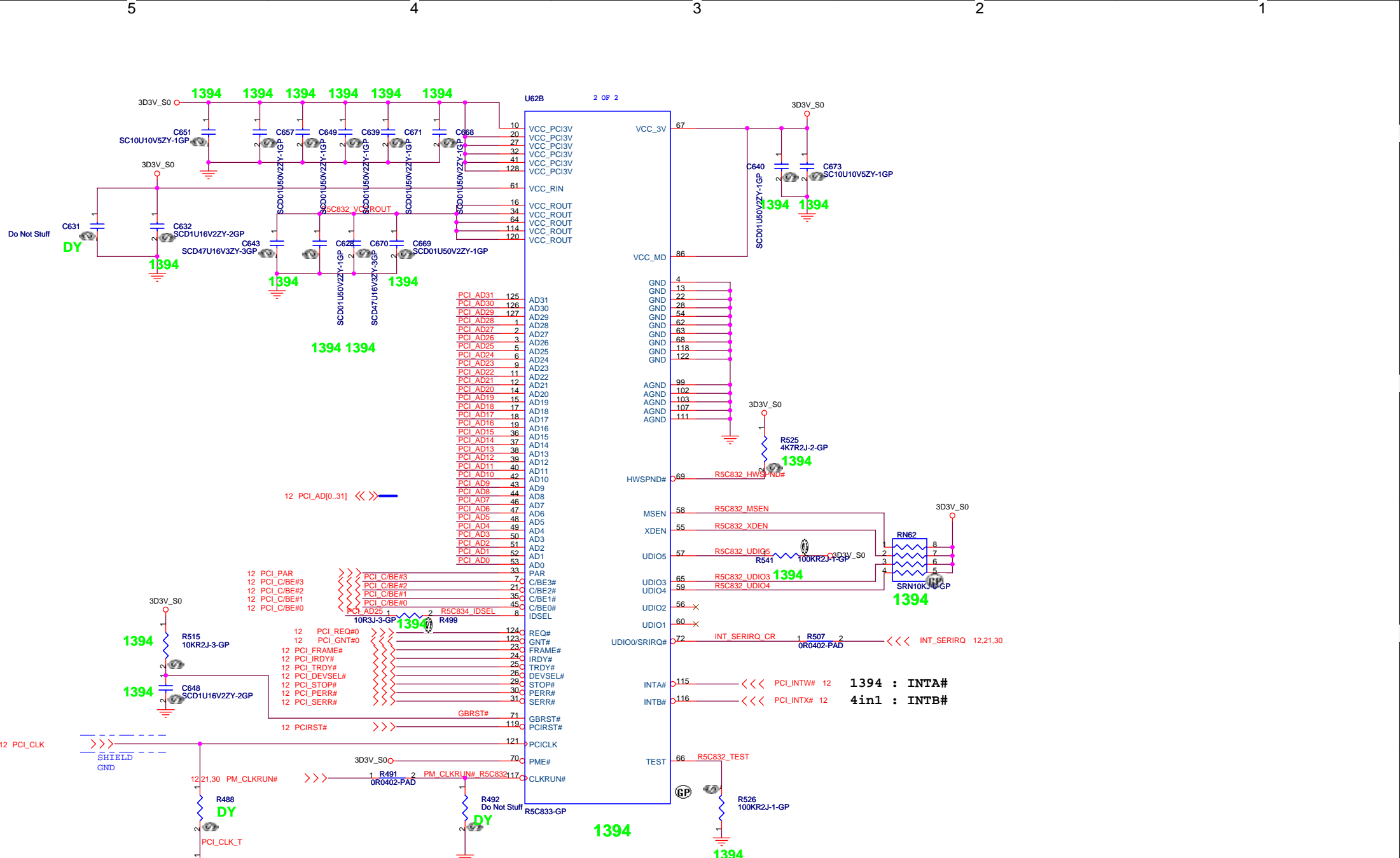
# USB PORT

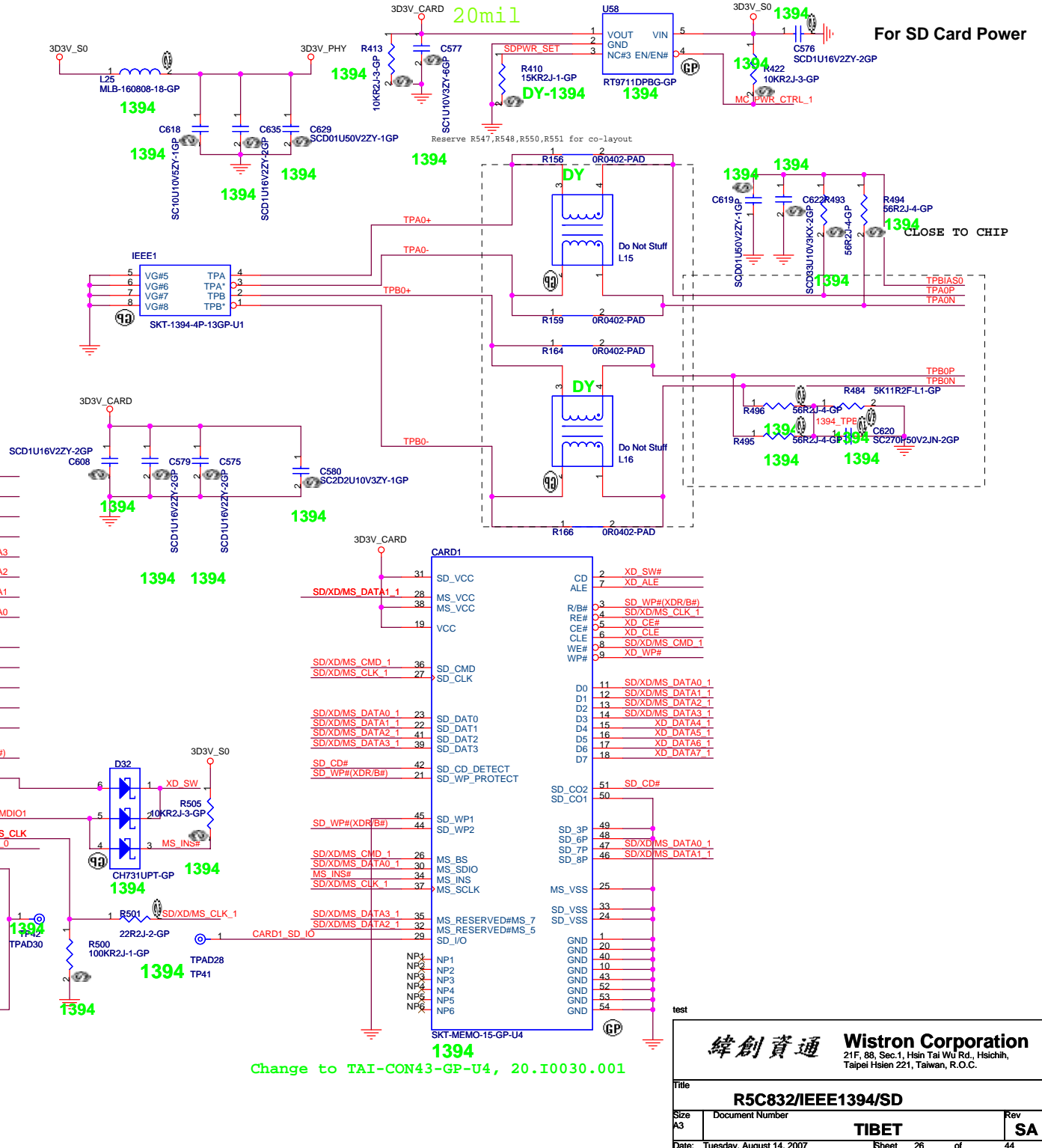
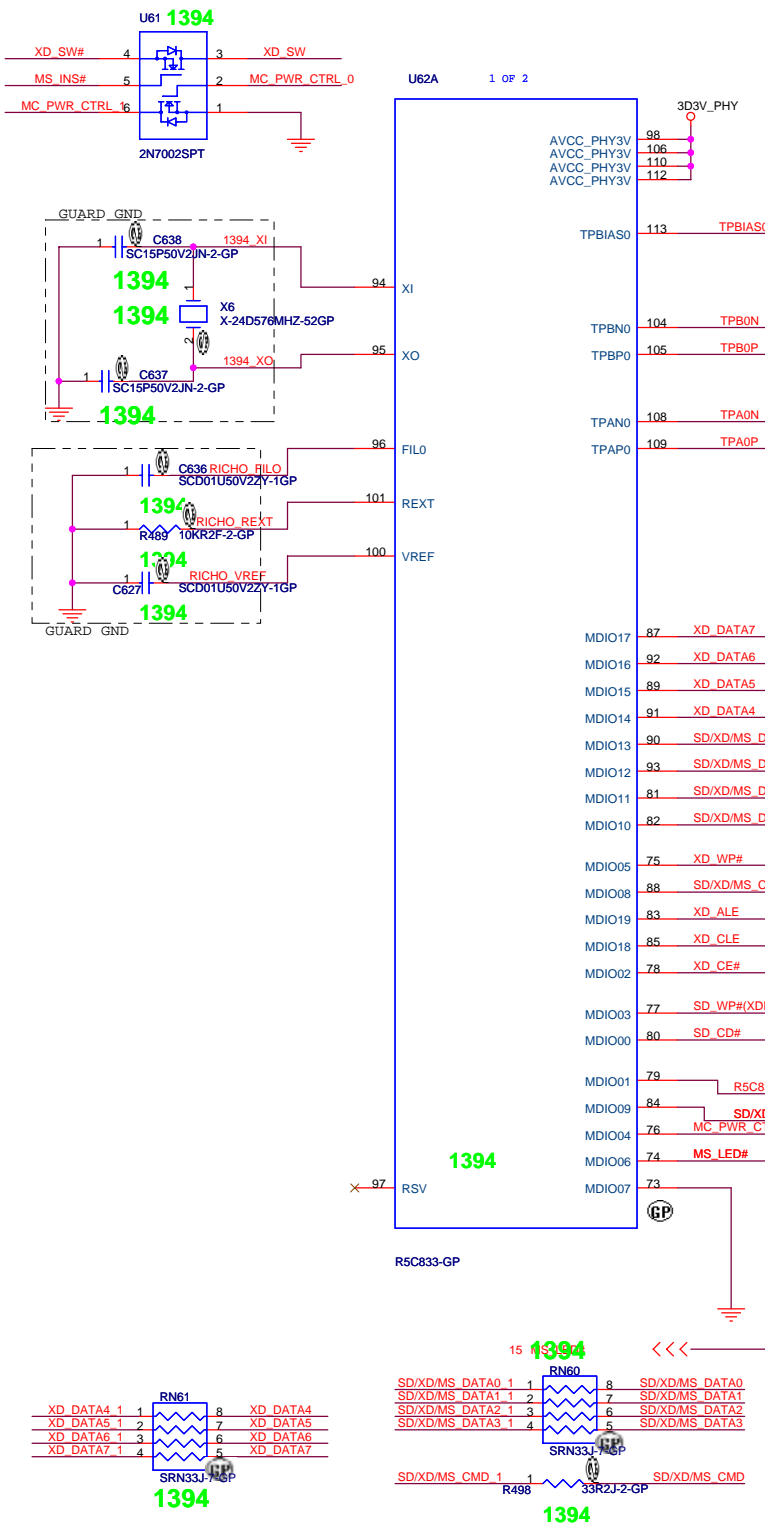


test

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Change to TAI-CON43-GP-U4, 20.I0030.001

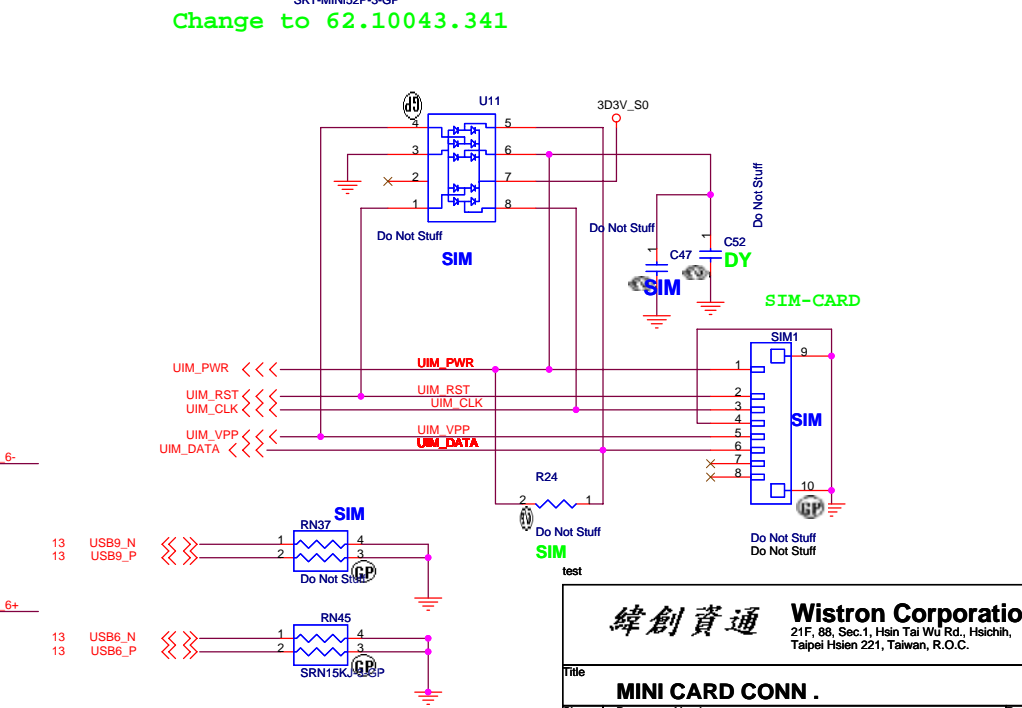
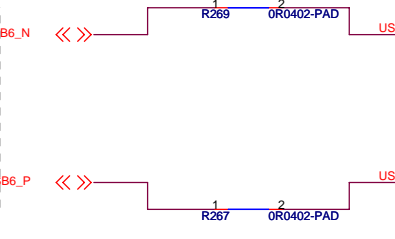
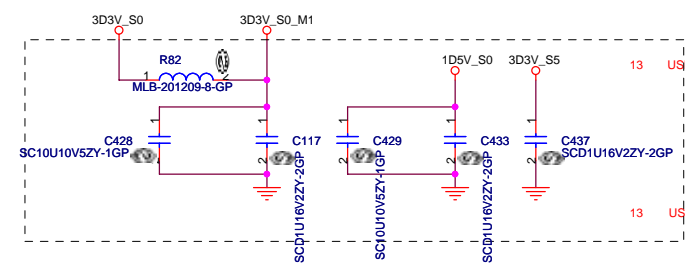
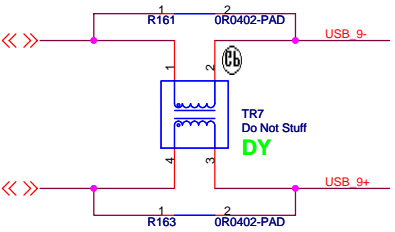
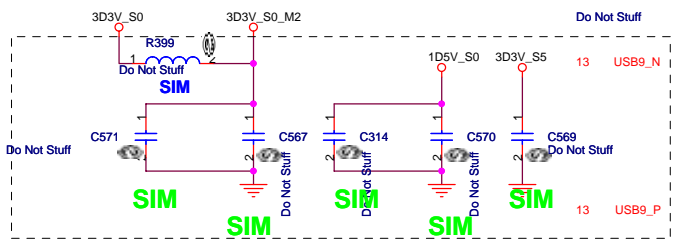
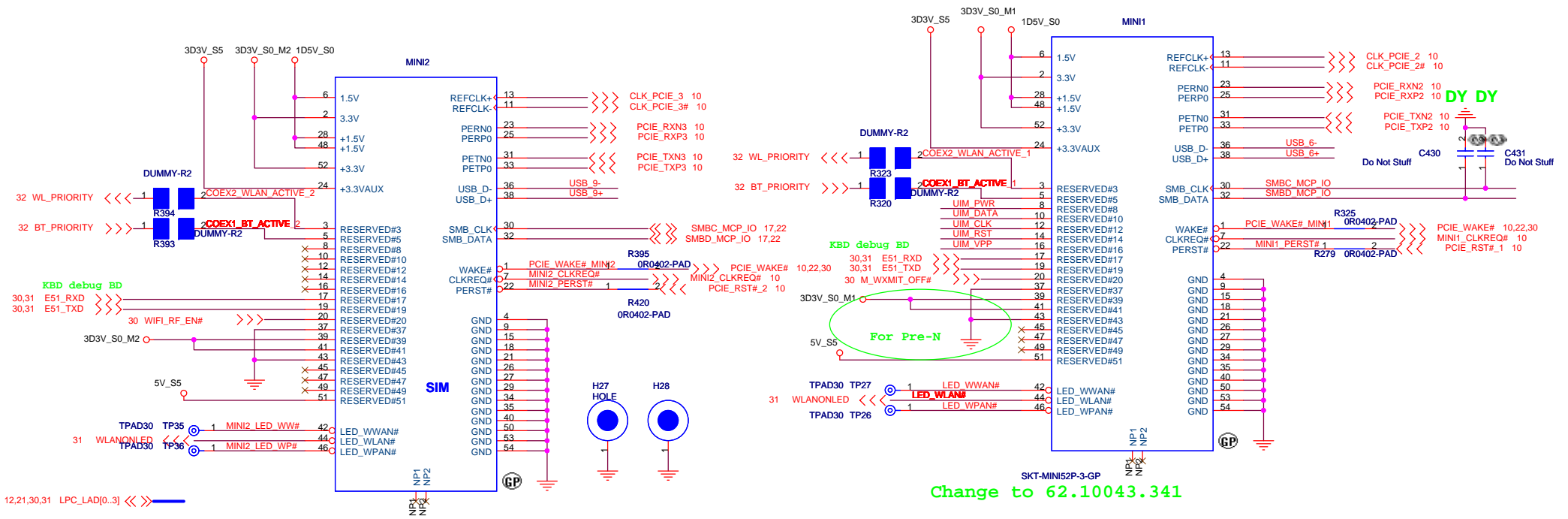
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
<b>R5C832/IEEE1394/SD</b>		
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# Mini Card Connector 2

Wireless Card

# Mini Card Connector 1

WWAN



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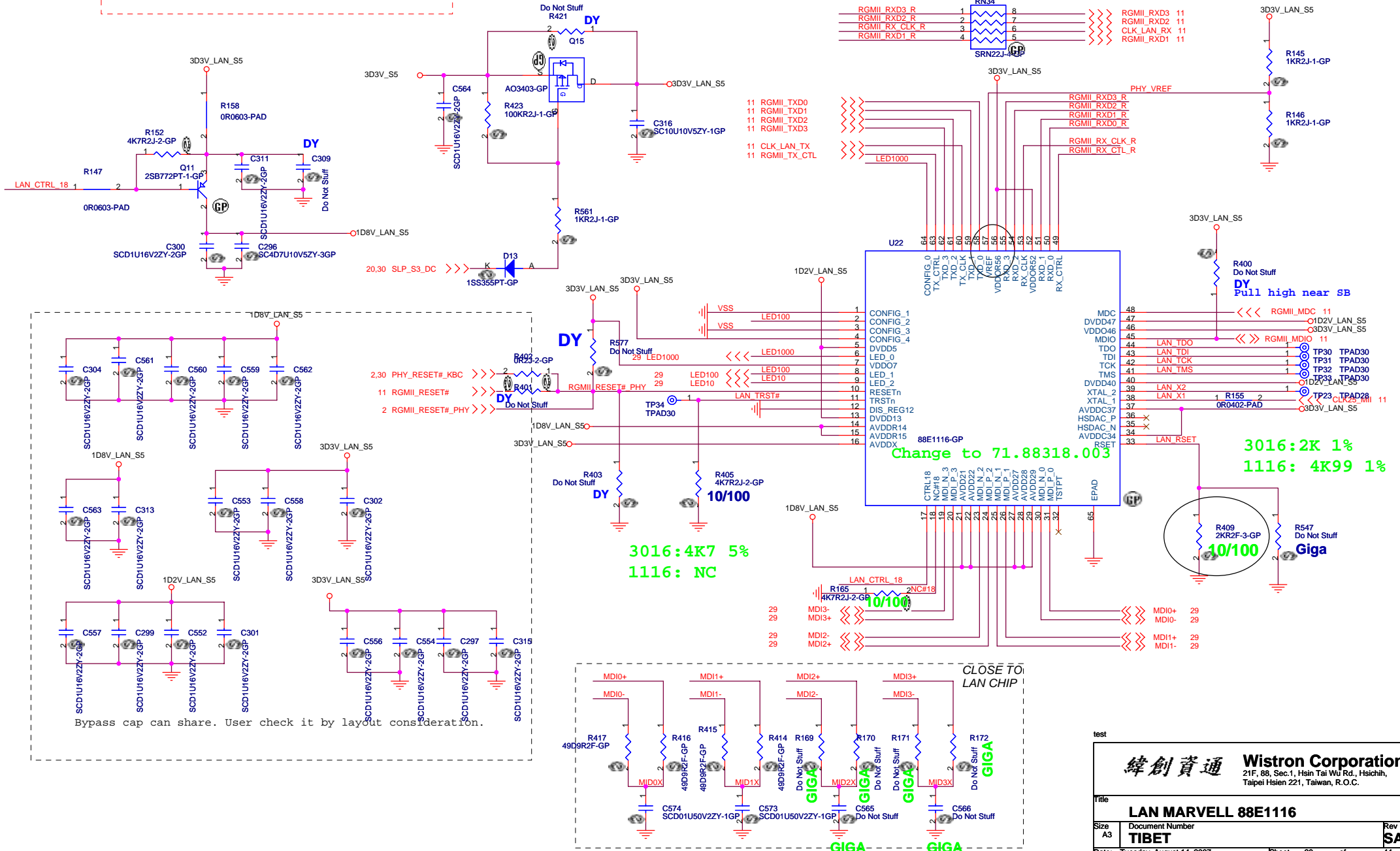
Title: **MINI CARD CONN.**

Size: A3 Document Number: **TIBET** Rev: SA

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1. PHY address:00001
2. ENA\_XC:Enable Auto-Crossover
3. RGMII\_TX:Transmit clock not internally delayed
4. RGMII\_RX:Receive clock transition when data transitions
5. Advertise all capabilities

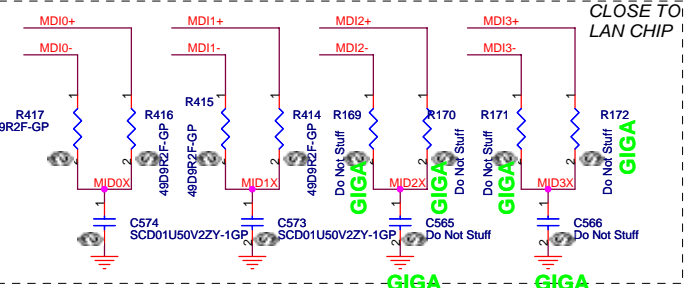
E1116 use external 2.5V single power supply.  
1.8V create by PNP and 1.2V use internal reg.



3016:4K7 5%  
1116: NC

Change to 71.88318.003

3016:2K 1%  
1116: 4K99 1%



CLOSE TO LAN CHIP

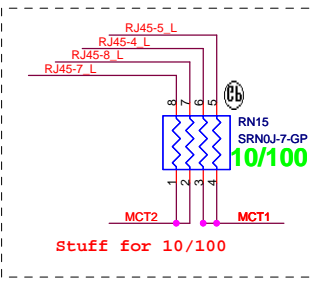
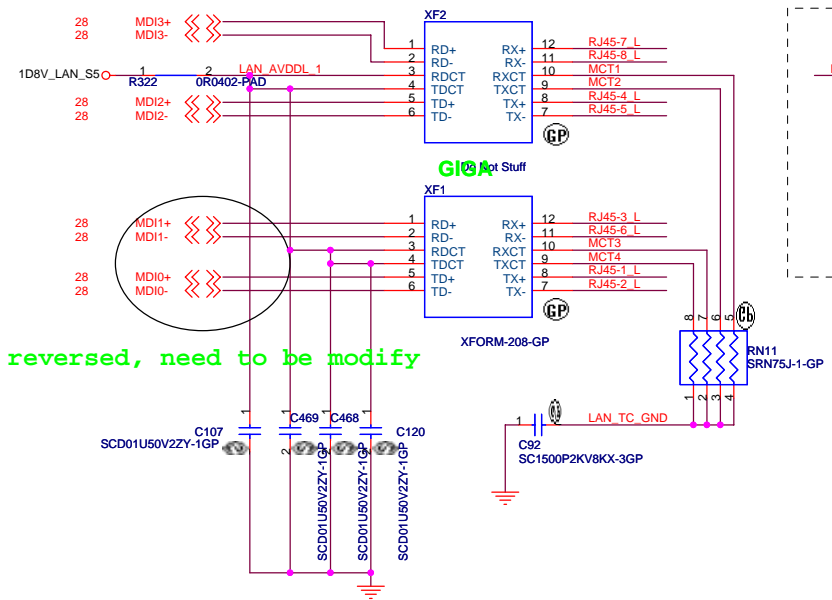
test

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Title: **LAN MARVELL 88E1116**

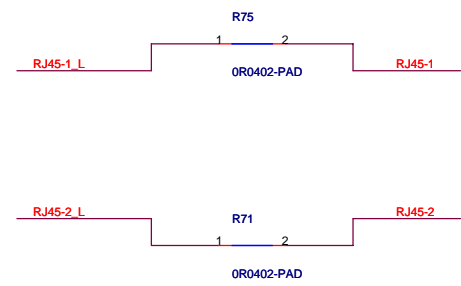
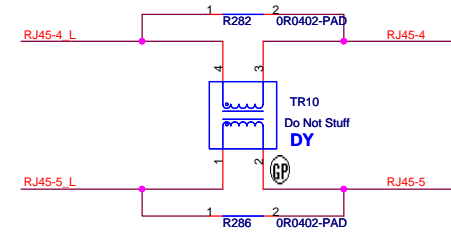
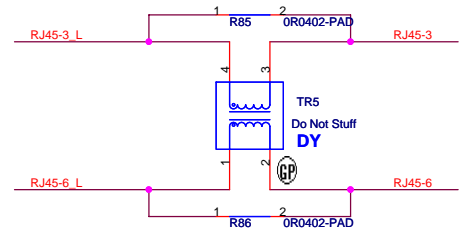
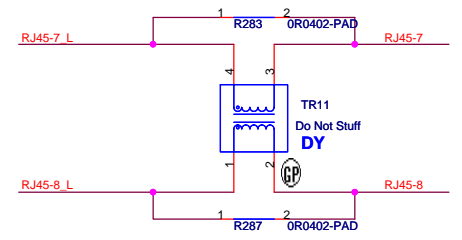
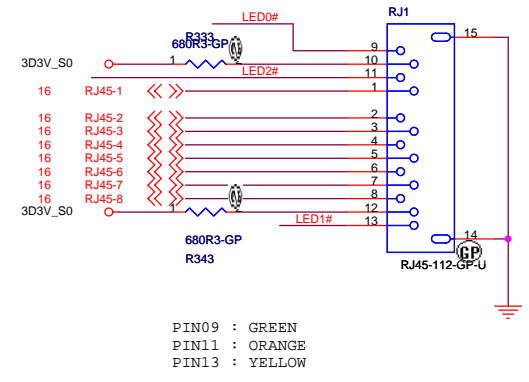
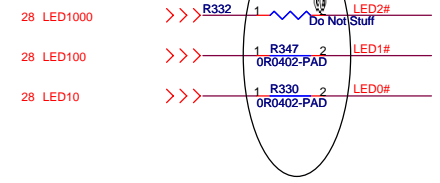
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1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

**GREEN: LINK 10/100 Mbps**  
**YELLOW: TX/RX ACTIVITY**  
**ORANGE: LINK 1000Mbps**



test

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Title: **LAN CONN**

Size: A3  
 Document Number: **TIBET**  
 Date: Tuesday, August 14, 2007

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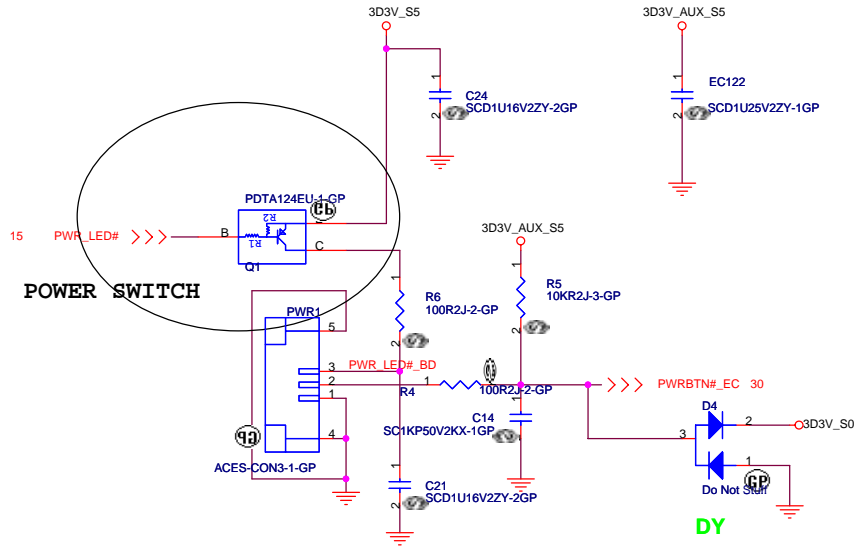


# GOLDEN FINGER FOR DEBUG BOARD

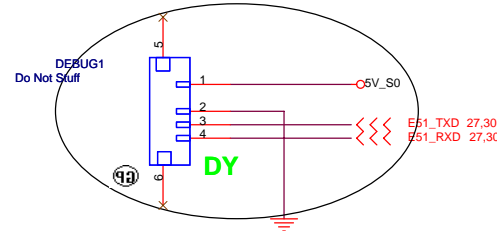
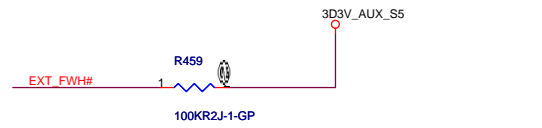
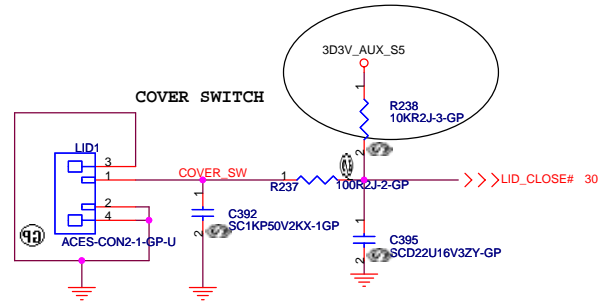
TOP VIEW

A15 (B1)  
A14 (B2)  
⋮  
A2 (B14)  
A1 (B15)

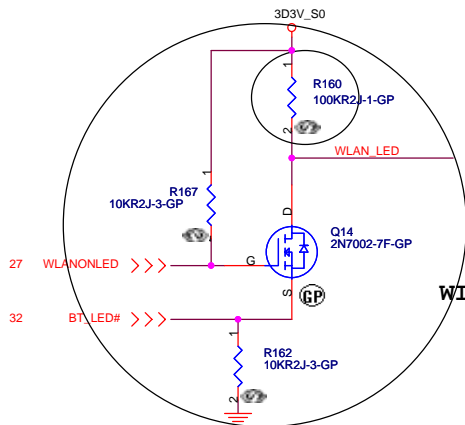
(BOTTOM VIEW)



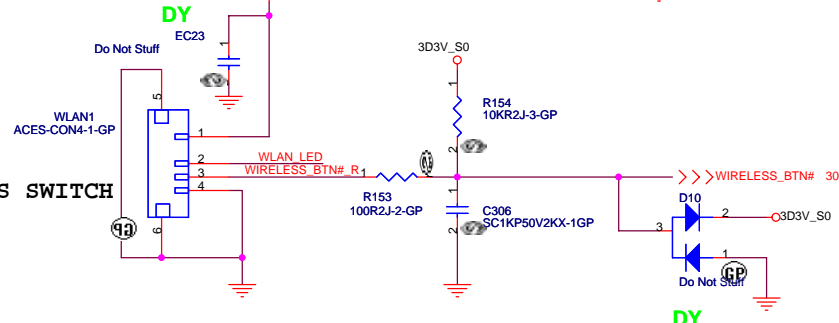
DY



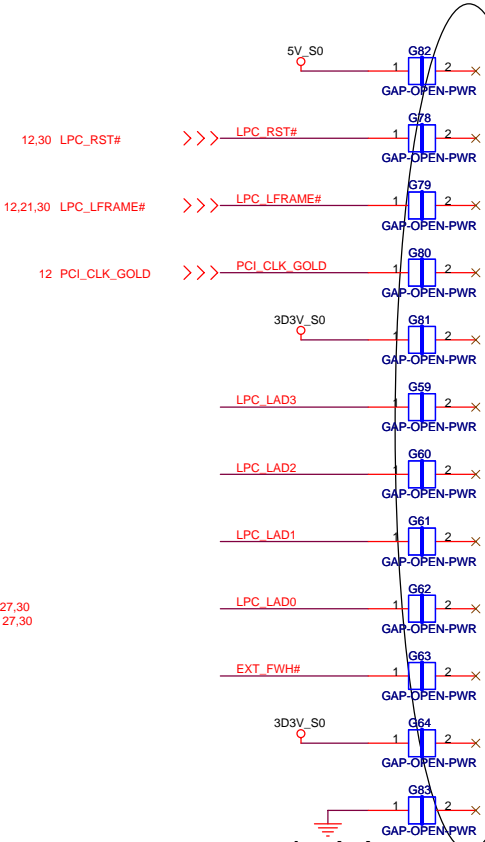
DY



DY



DY



Put near board edge  
test

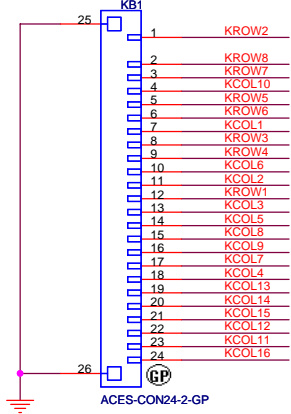
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
<b>FLASH and Debug</b>		
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### Internal Keyboard Connector

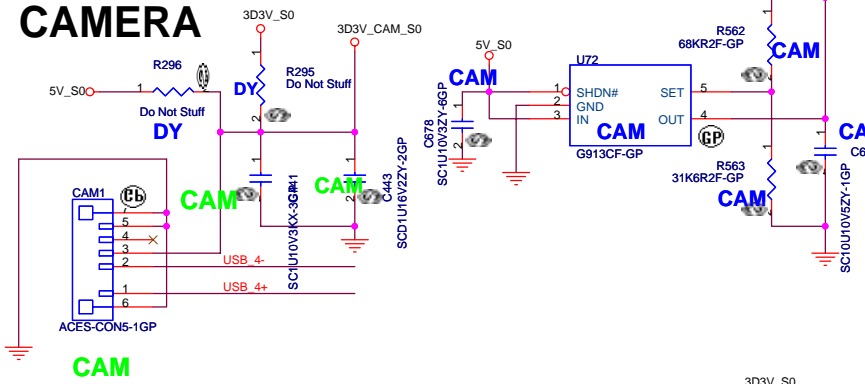
30 KROW[1..8] <<<<   
 30 KCOL[1..16] <<<< 

Keyboard matrix ( from vendor )

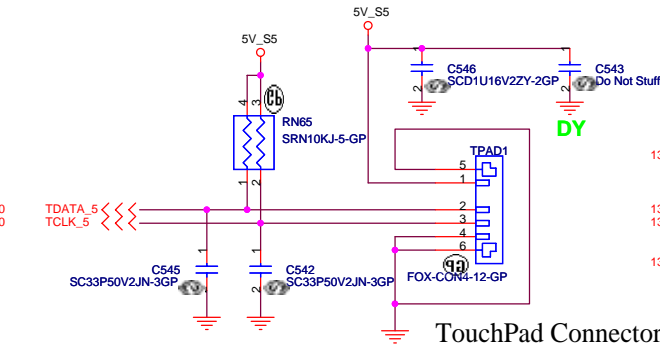
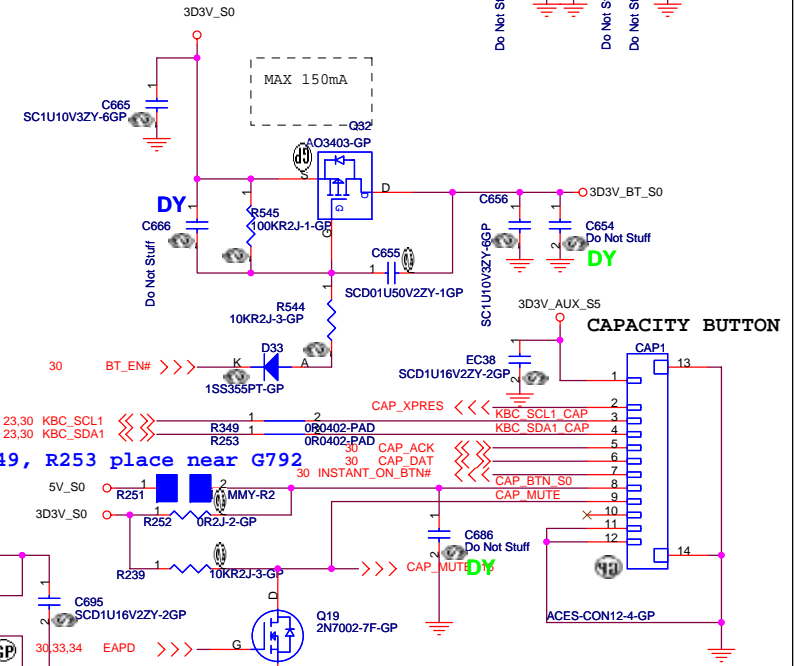
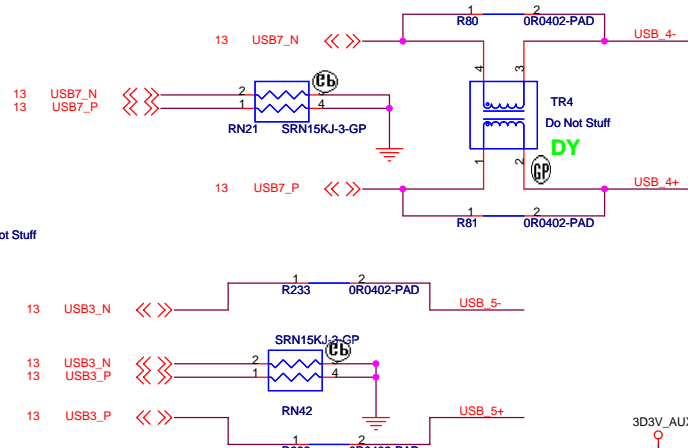
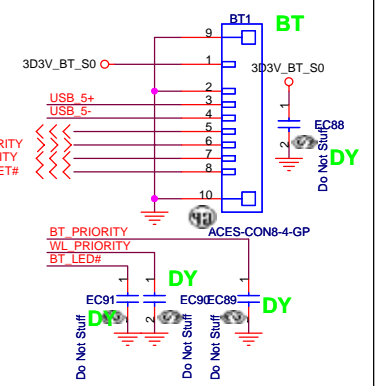
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



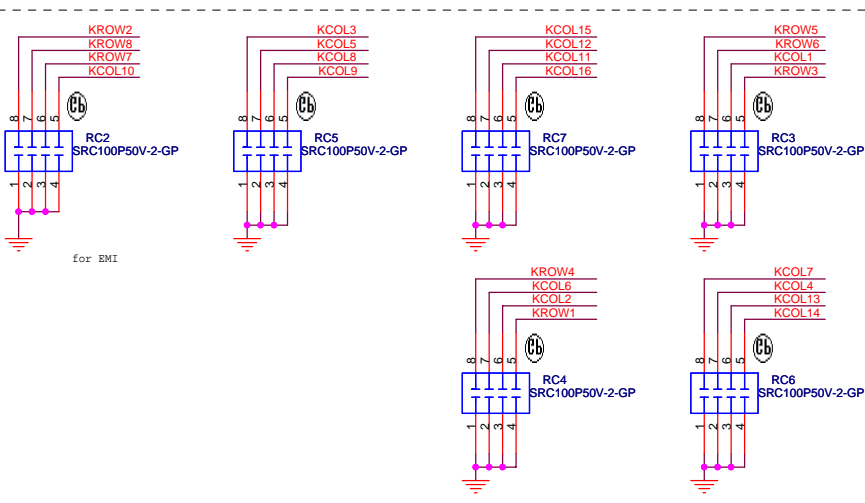
### CAMERA



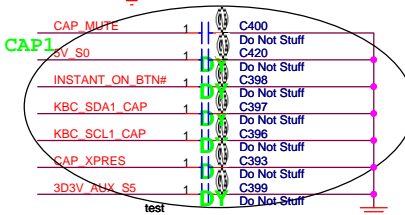
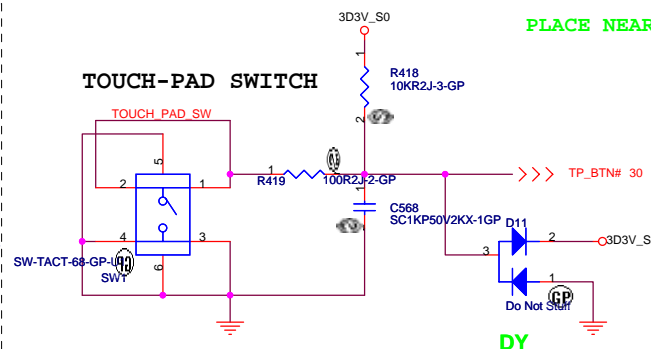
### BT



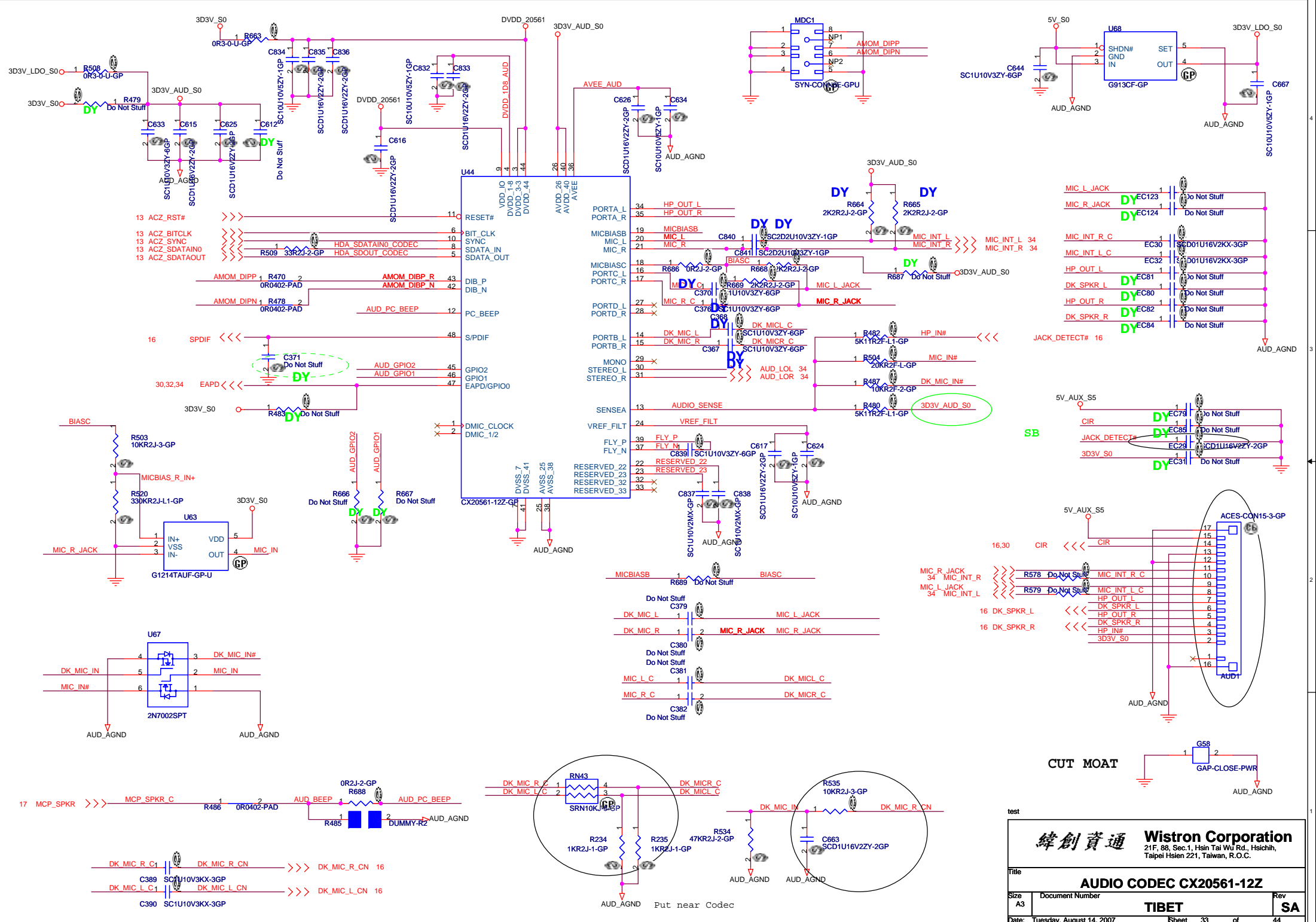
### TouchPad Connector



### TOUCH-PAD SWITCH



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<b>KeyBoard-CONN</b>	
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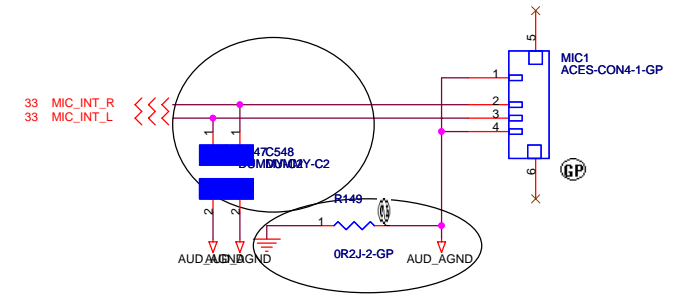
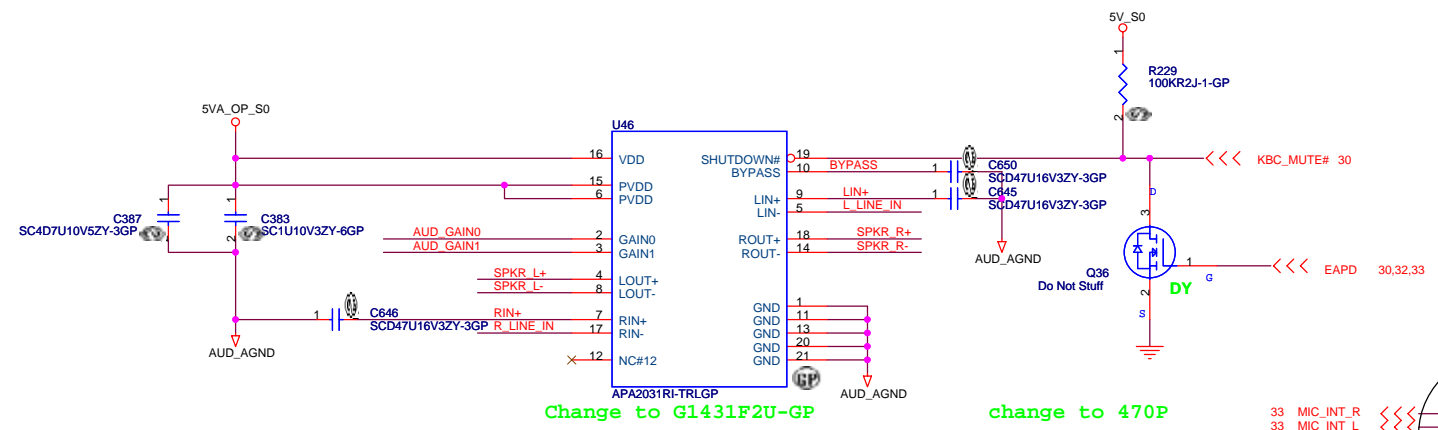
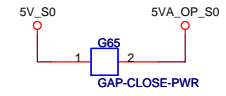


test

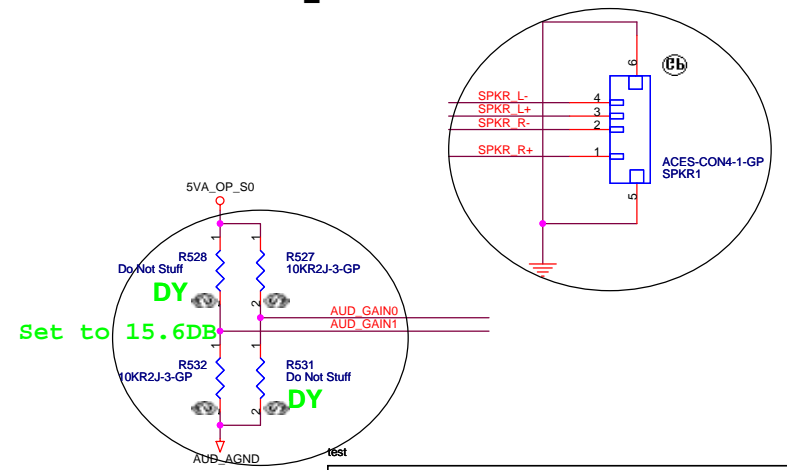
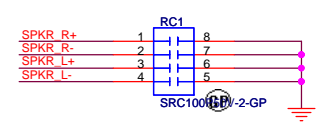
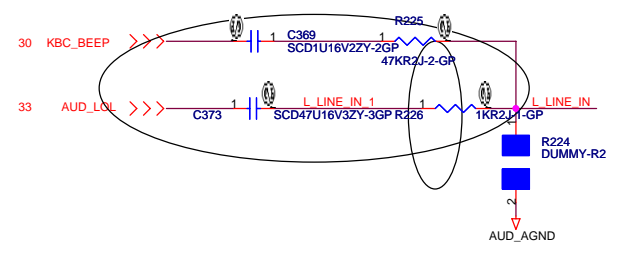
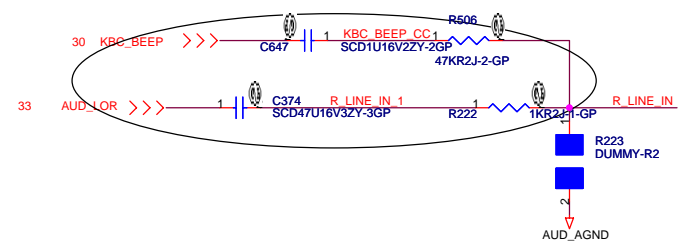
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Title: **AUDIO CODEC CX20561-12Z**

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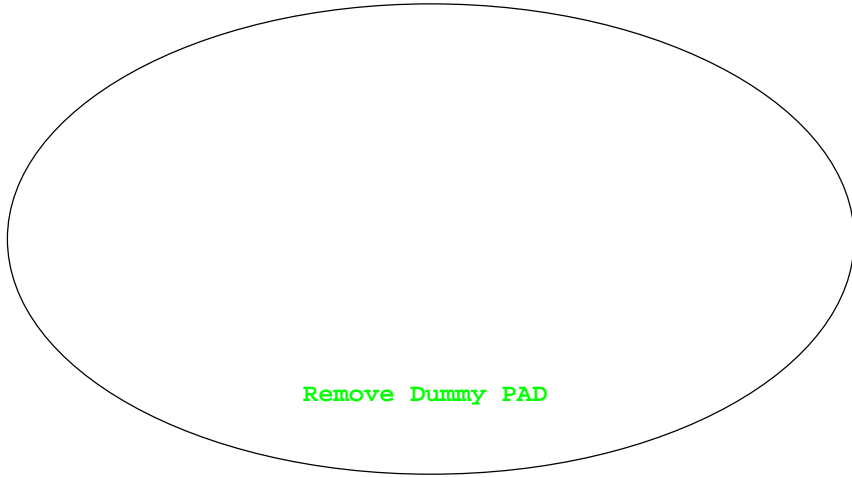


### Speaker

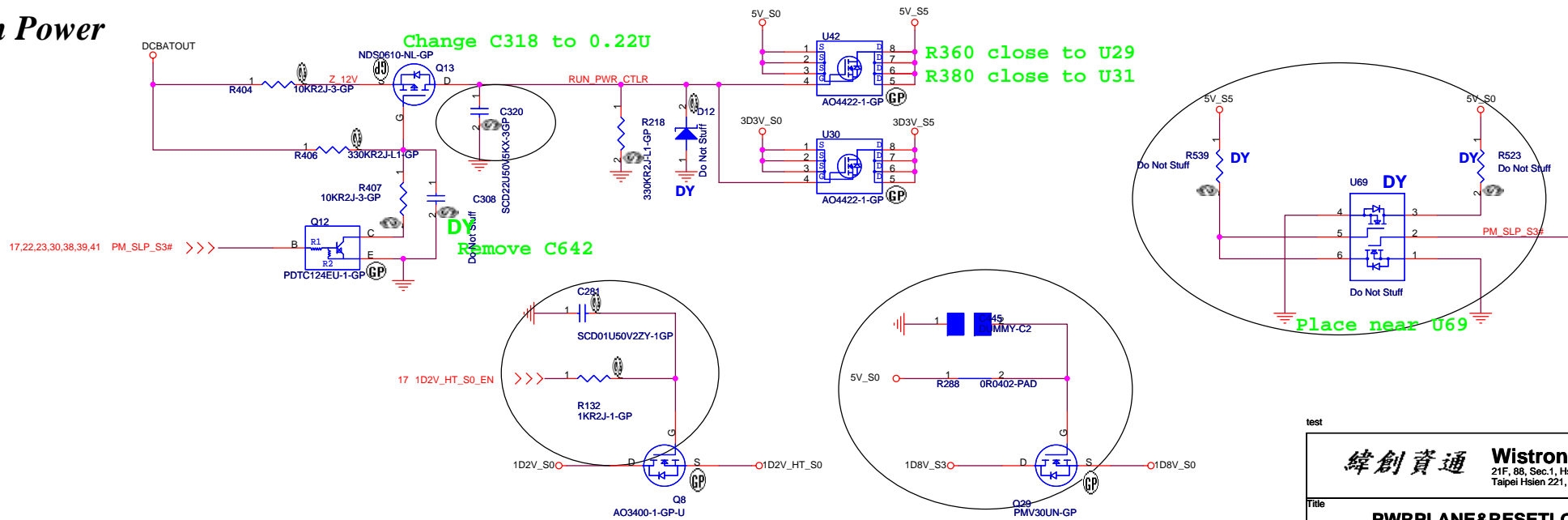


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<b>AUDIO AMP APA3031</b>	
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# Suspend Power



# Run Power

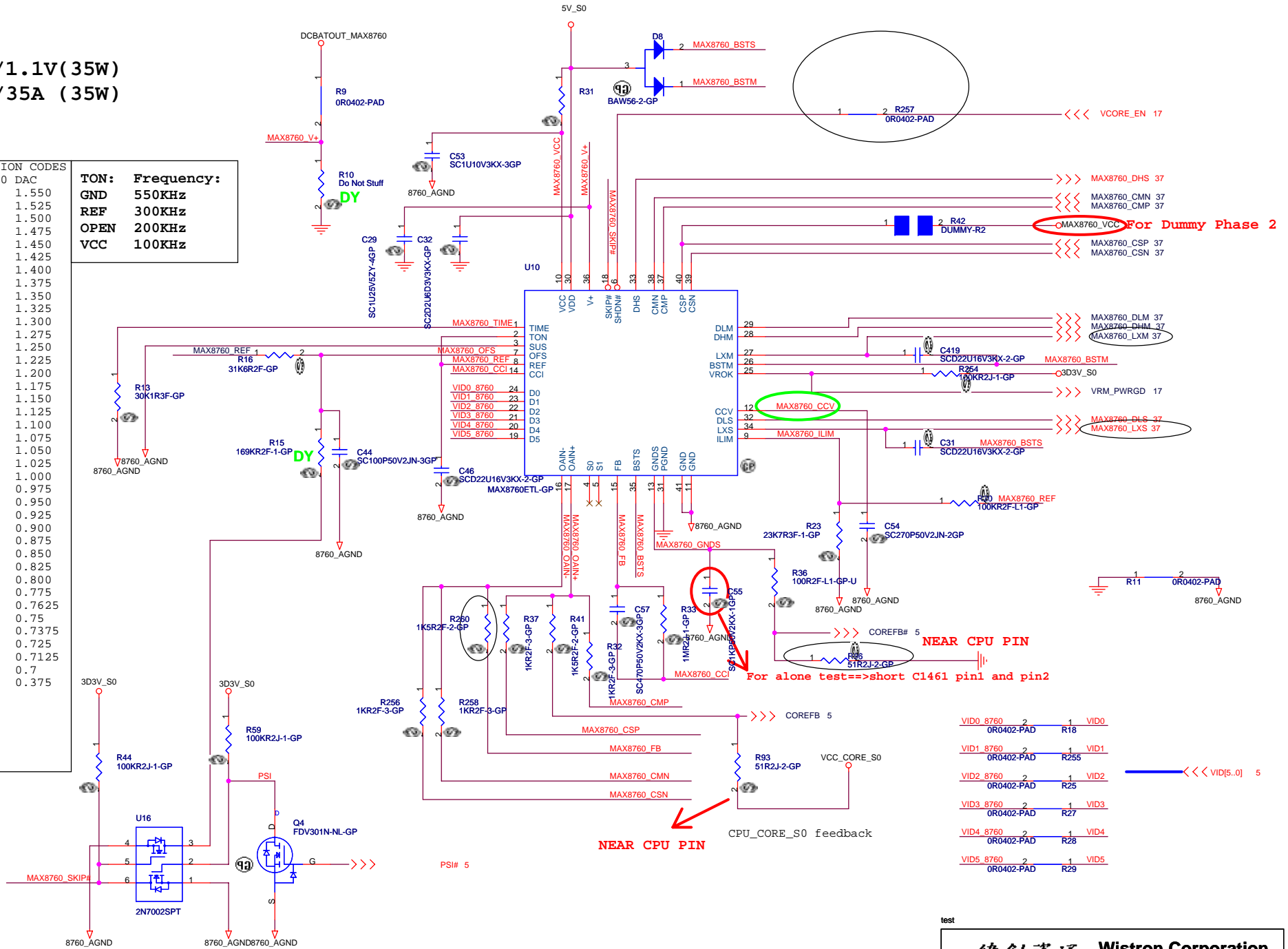


**CPU\_VCORE**  
**VID=1.15V(25W)/1.1V(35W)**  
**I<sub>omax</sub>=25A(25W)/35A(35W)**  
**OCP=40A~45A**

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375

**TON: Frequency:**  
**GND 550KHz**  
**REF 300KHz**  
**OPEN 200KHz**  
**VCC 100KHz**



VID0 8760	2	1	VID0
OR0402-PAD		R18	
VID1 8760	2	1	VID1
OR0402-PAD		R255	
VID2 8760	2	1	VID2
OR0402-PAD		R25	
VID3 8760	2	1	VID3
OR0402-PAD		R27	
VID4 8760	2	1	VID4
OR0402-PAD		R28	
VID5 8760	2	1	VID5
OR0402-PAD		R29	

test

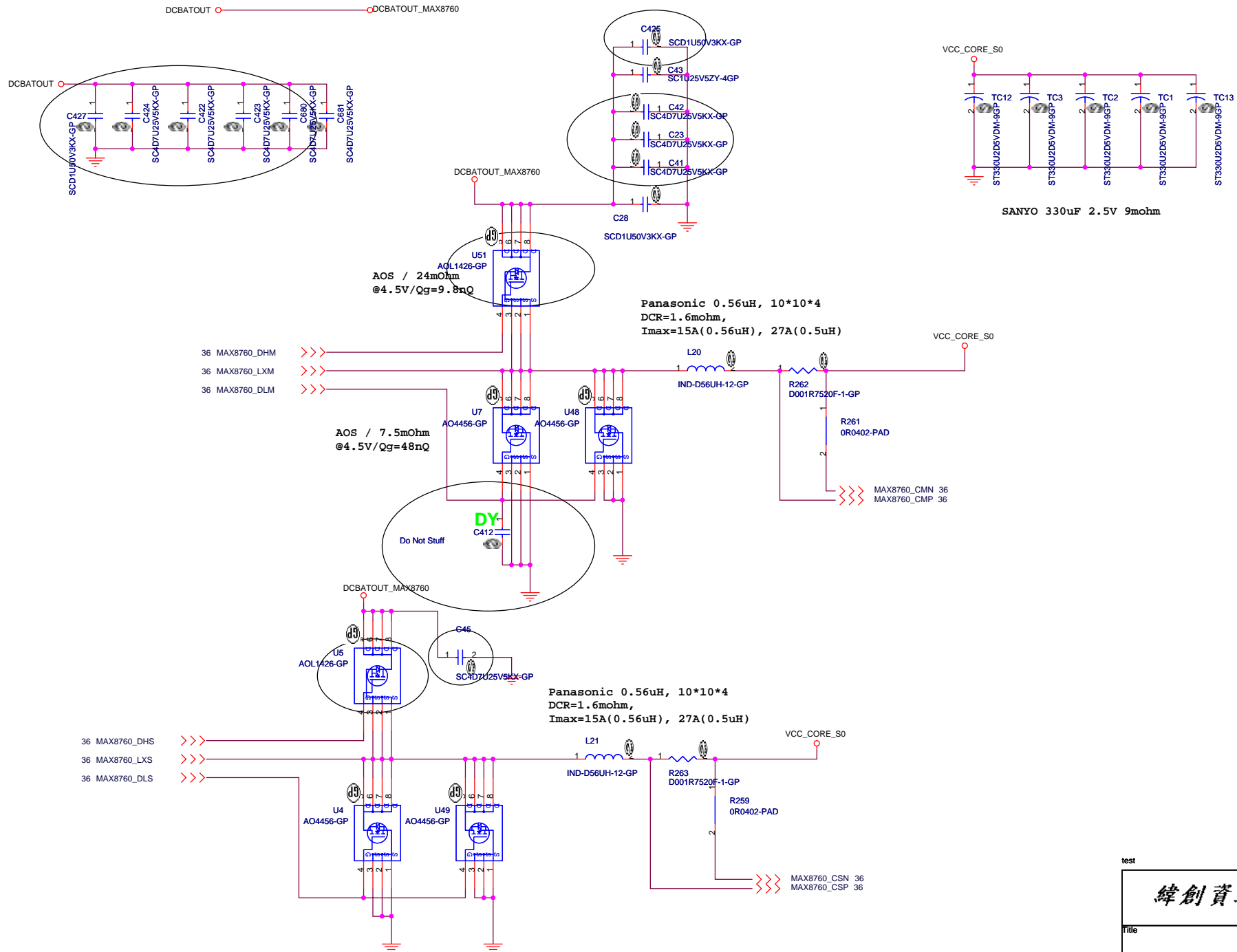
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU CORE MAX8760(1/2)**

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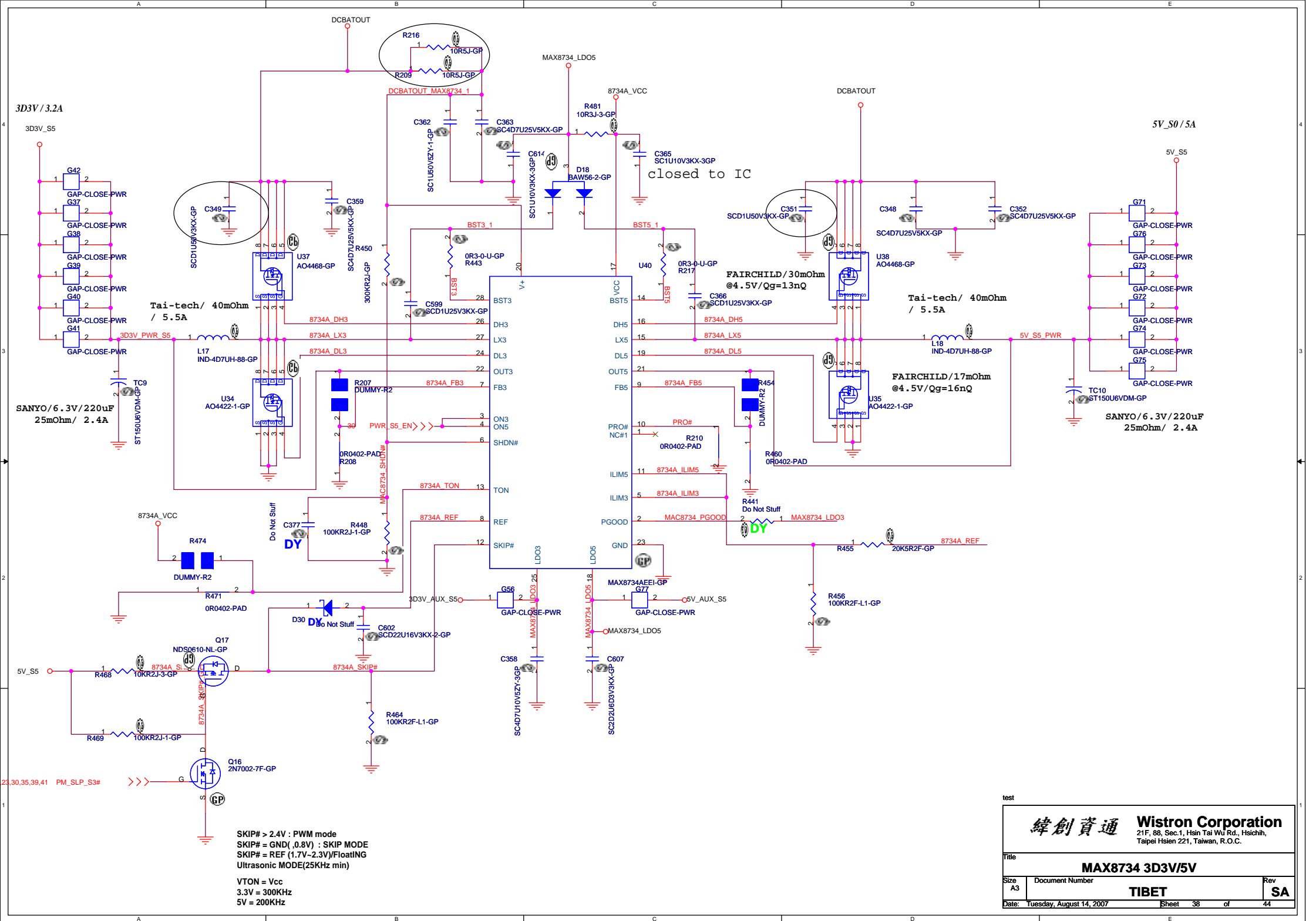




(Power Team)

test

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>CPU CORE MAX8760(2/2)</b>	
Title	
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3D3V/3.2A

5V\_S0/5A

closed to IC

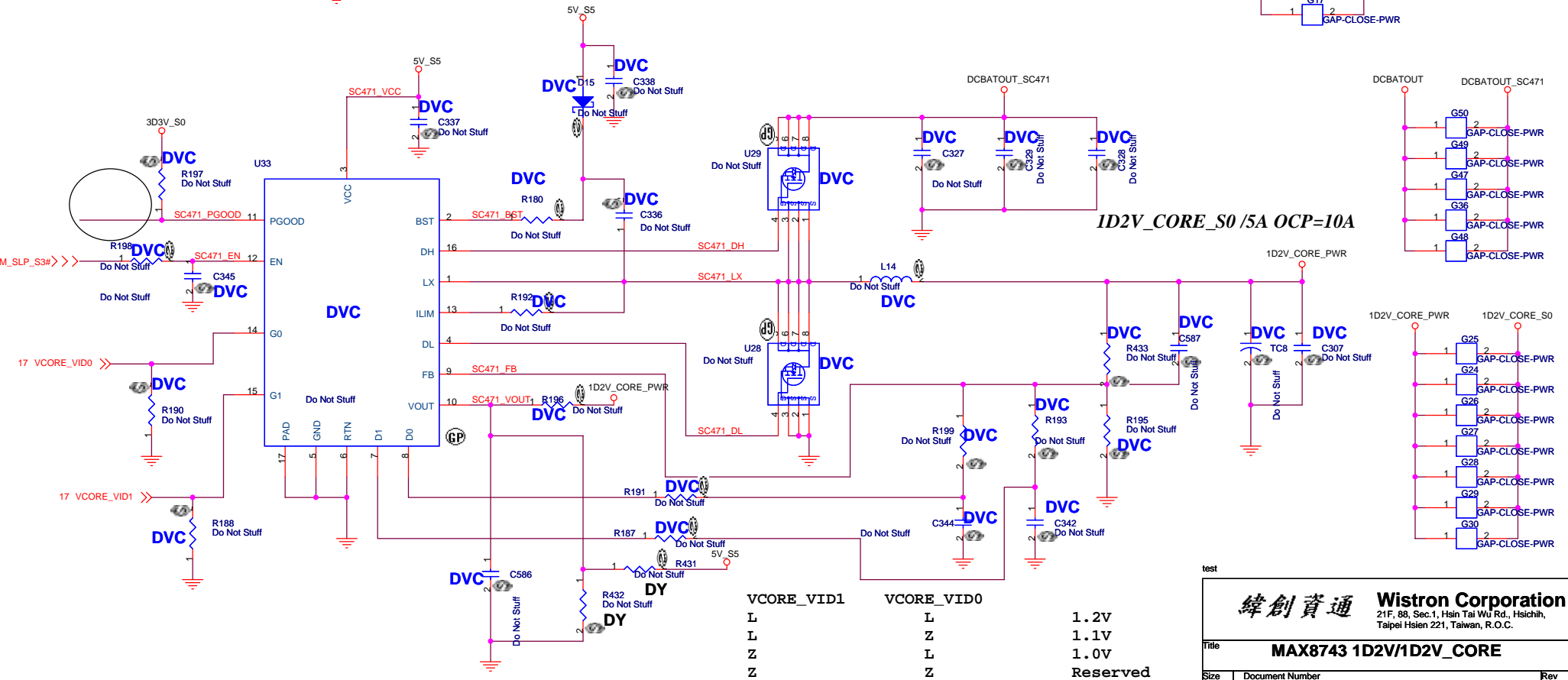
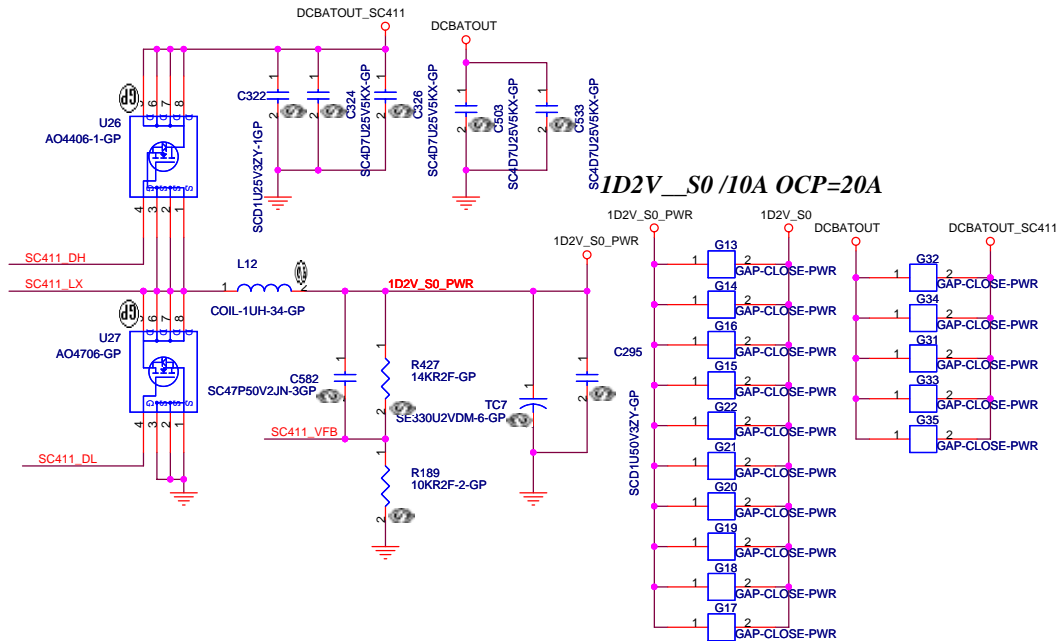
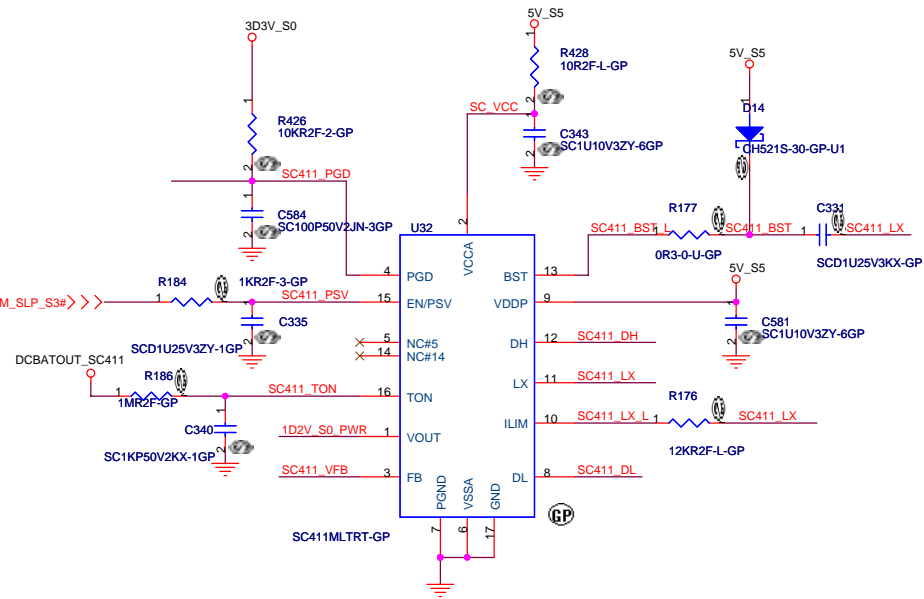
SANYO/6.3V/220uF  
25mOhm/ 2.4A

SANYO/6.3V/220uF  
25mOhm/ 2.4A

23,30,35,39,41 PM\_SLP\_S3#

SKIP# > 2.4V : PWM mode  
 SKIP# = GND(,0.8V) : SKIP MODE  
 SKIP# = REF (1.7V~2.3V)/FloatNG  
 Ultrasonic MODE(25KHz min)  
 VTON = Vcc  
 3.3V = 300KHz  
 5V = 200KHz

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>MAX8734 3D3V/5V</b>			
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VCORE_VID1	L	1.2V
L	Z	1.1V
Z	L	1.0V
Z	Z	Reserved

test

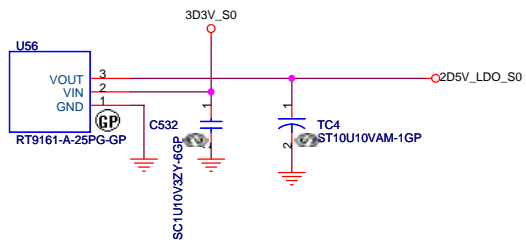
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MAX8743 1D2V/1D2V\_CORE**

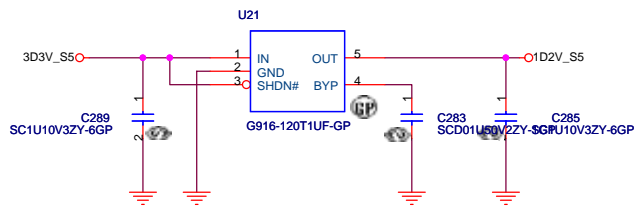
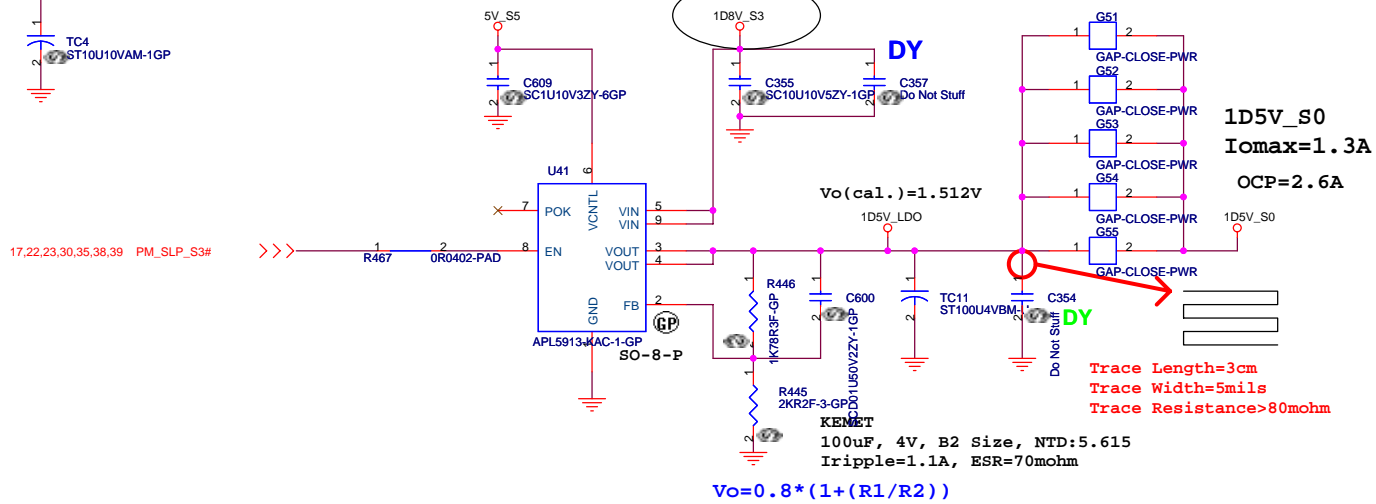
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**SA**





Change 3D3V\_S0 to 1D8V\_S3



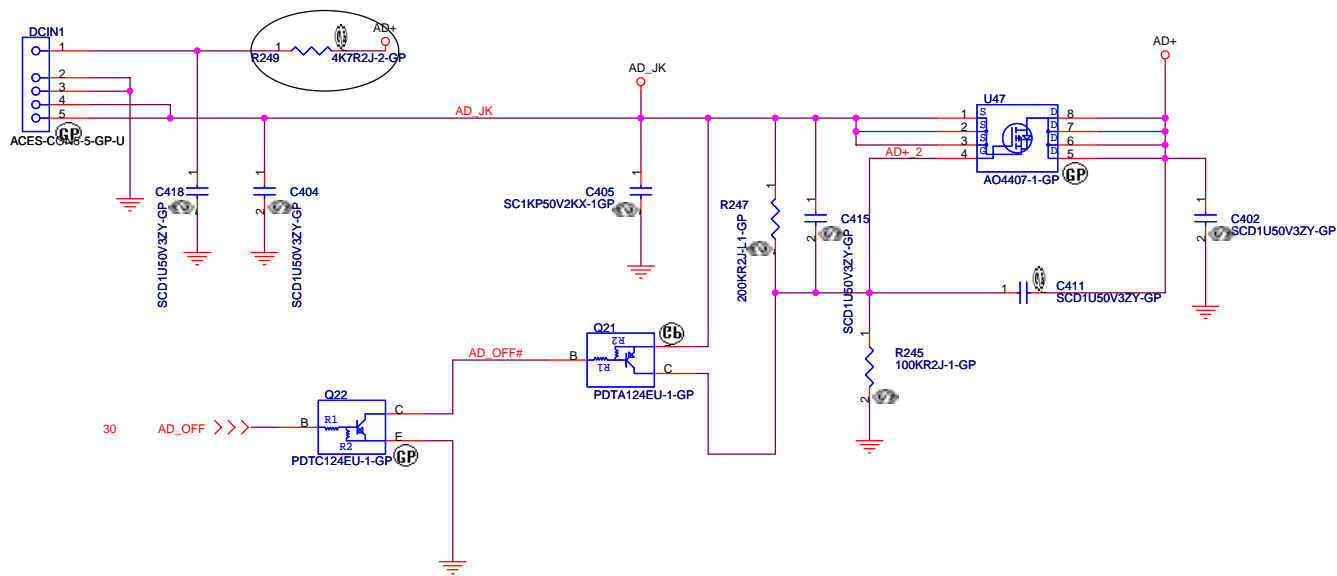
Change G914 to G916

test

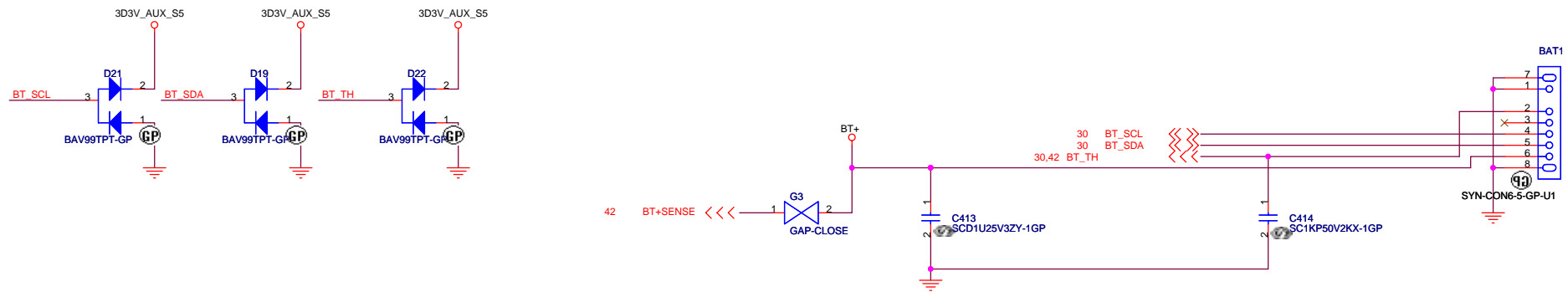
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>1D5V/2D5V/3D3V/5V_AUX</b>			
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# Adaptor in to generate DCBATOUT



# BATTERY CONNECTOR

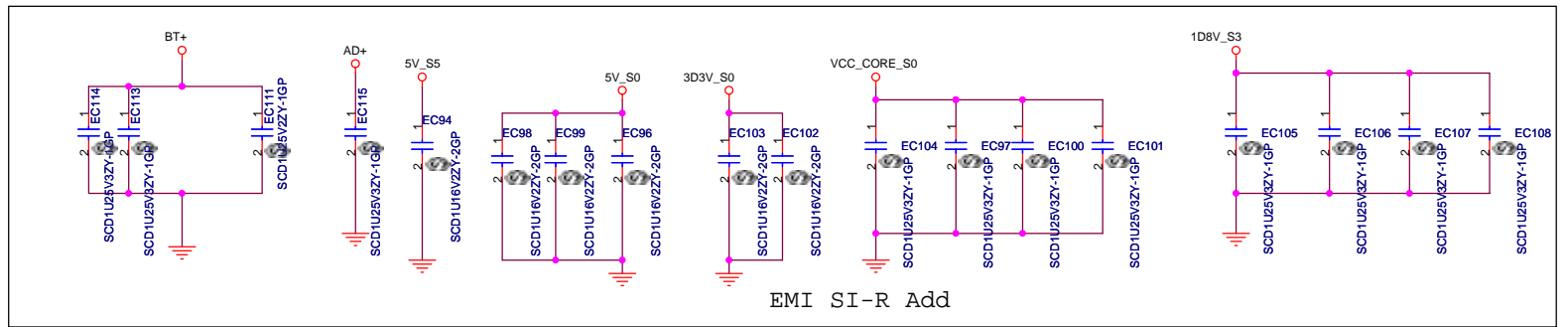
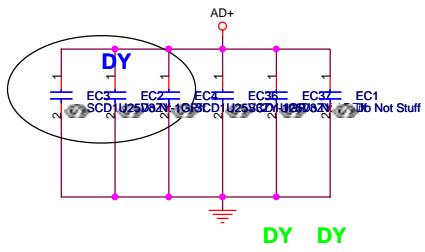


test

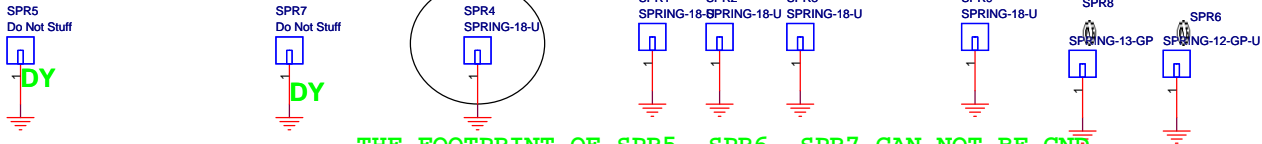
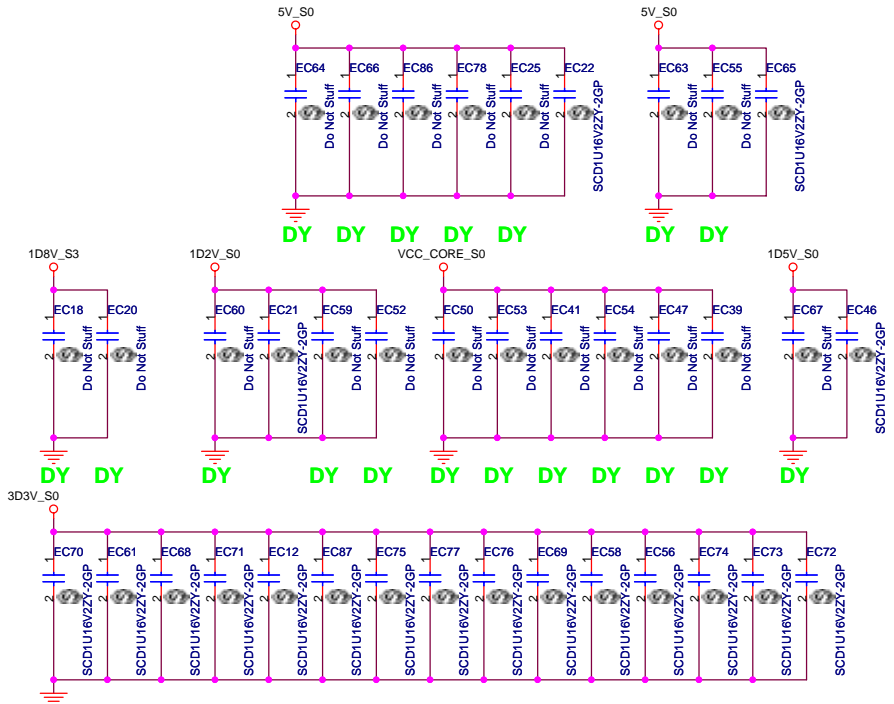
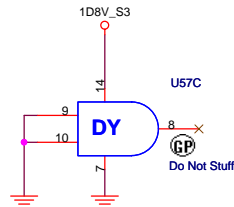
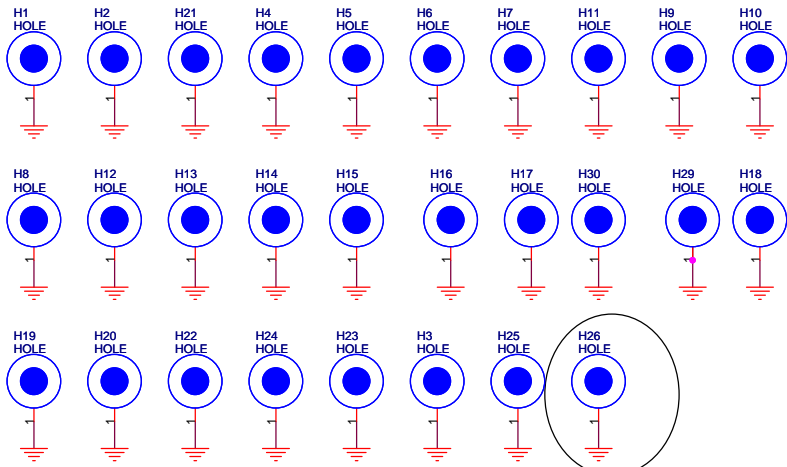
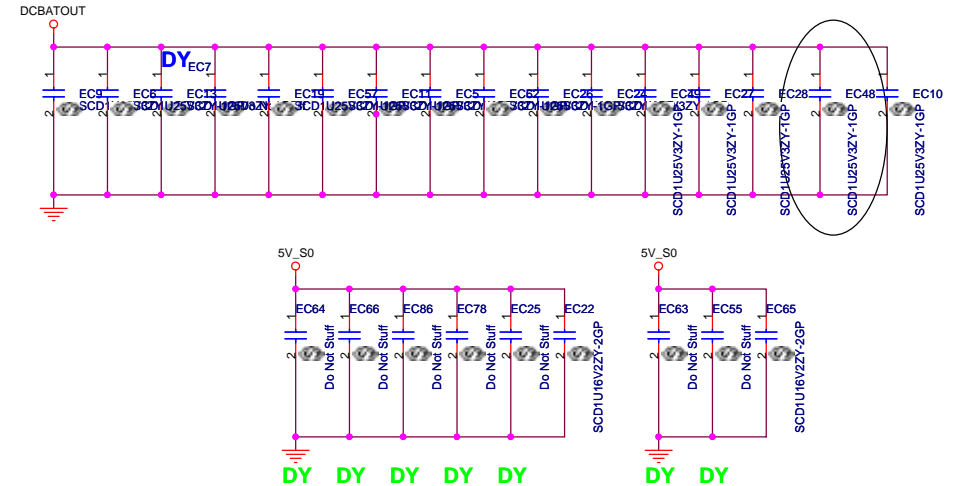
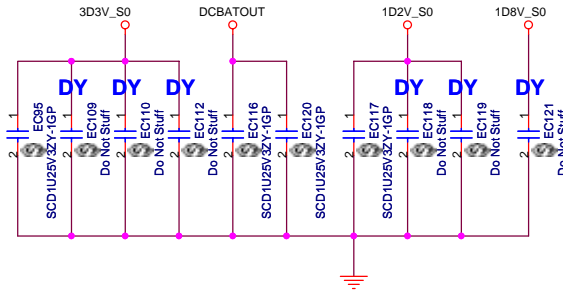
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

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	FF	DF
CAMERA	○	×
LAN	10/100	10/100
1394/5 IN 1	○	×
EXTRA USB	○	×
MIC	○	×
CR LED	○	×



test

**緯創資通** **Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **MISC**

Size A3 Document Number: **TIBET** Rev: **SA**

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