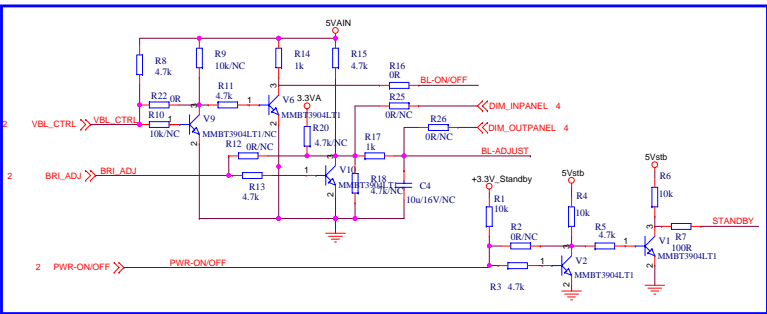
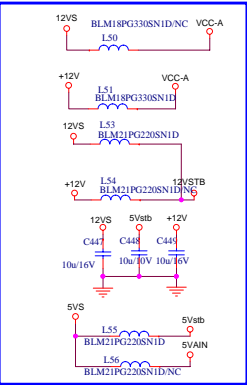
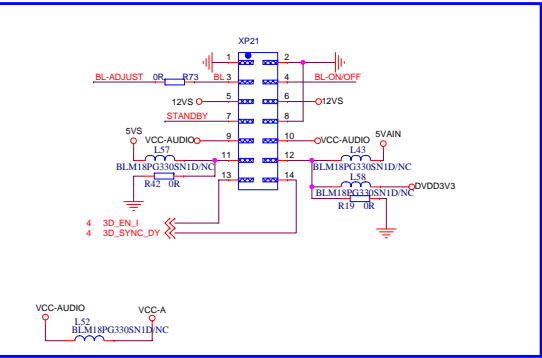
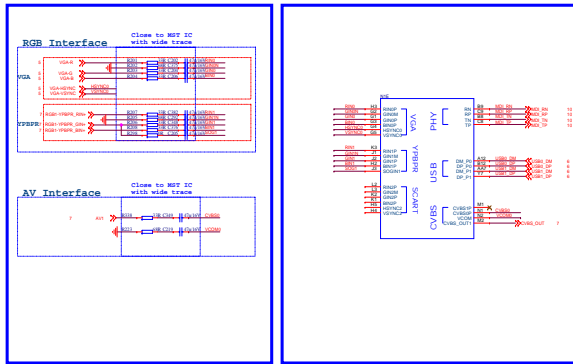


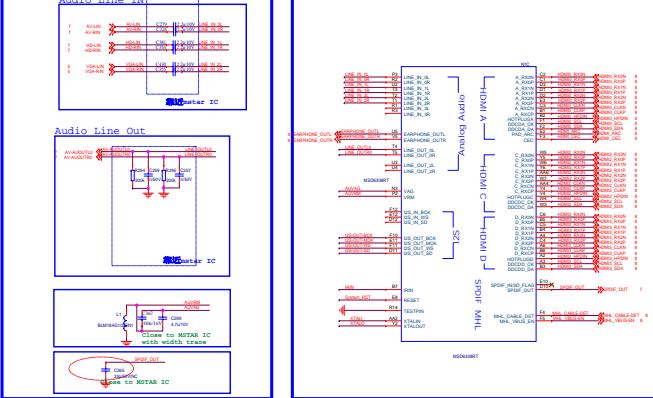
Power Input



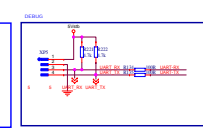
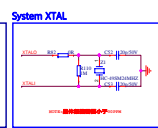
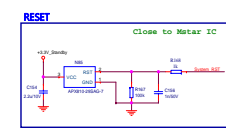
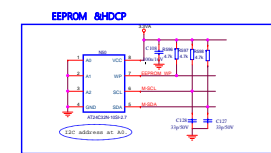
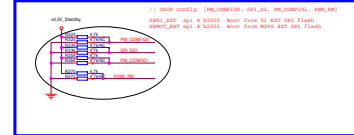
## video



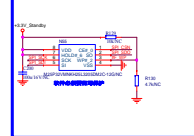
## HDMI & Audio



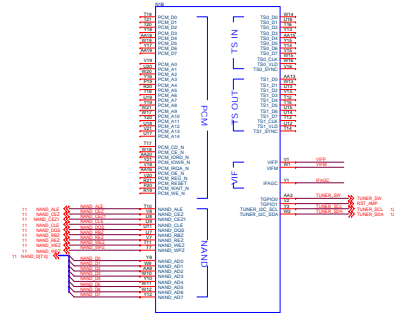
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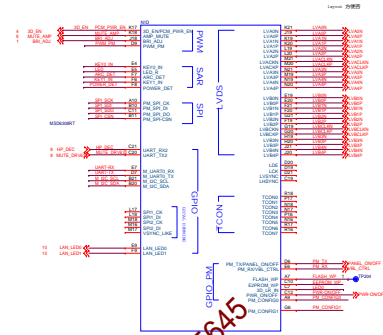
## FLASH



## NAND & CI & TS & Front End

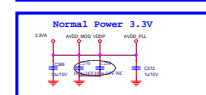
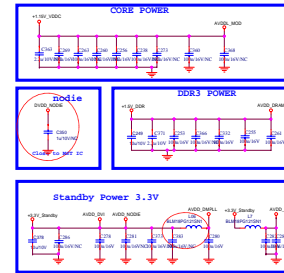
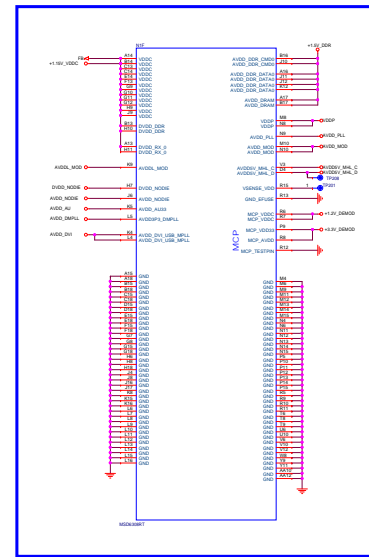


## GPIO & LVDS

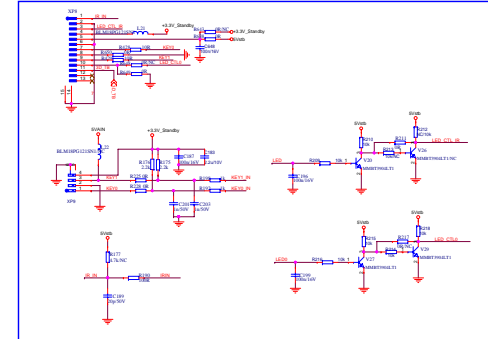


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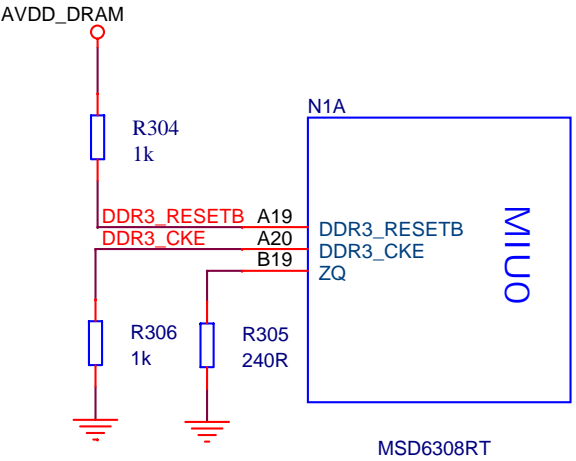
## POWER&GND



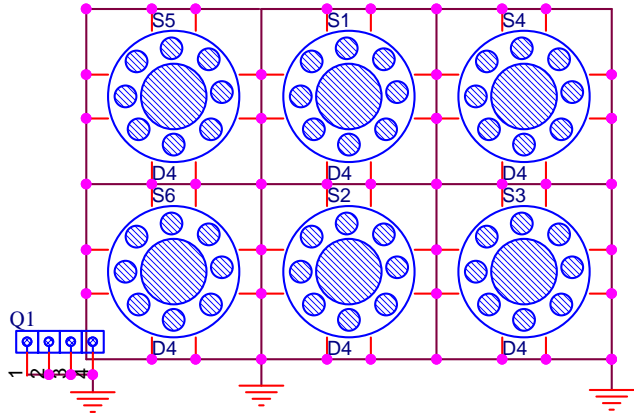
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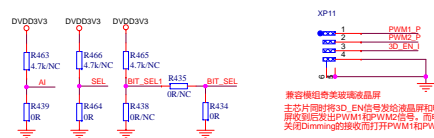
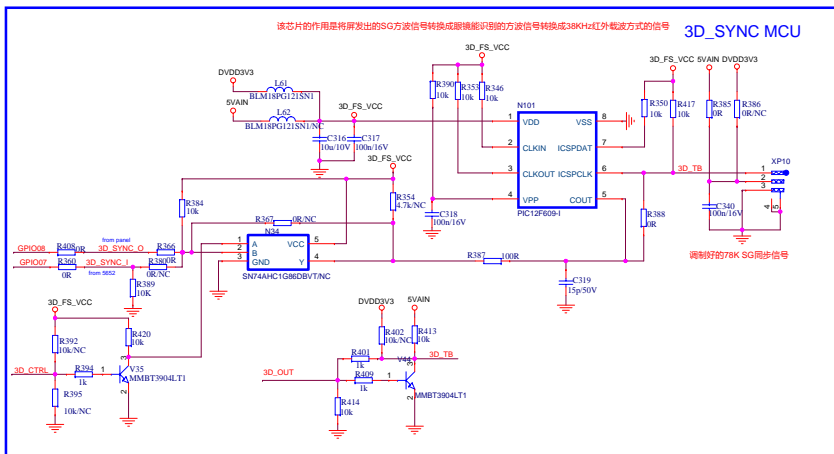
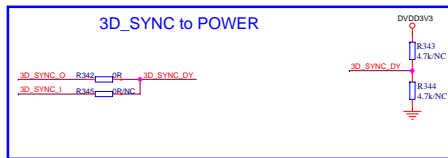
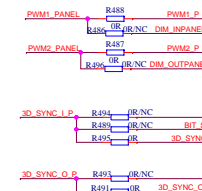
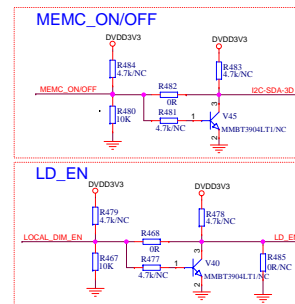
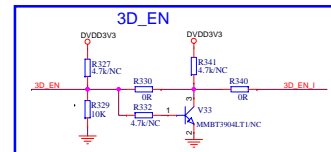
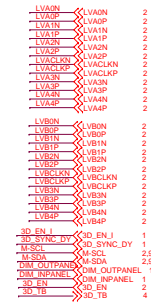
MSD MIU



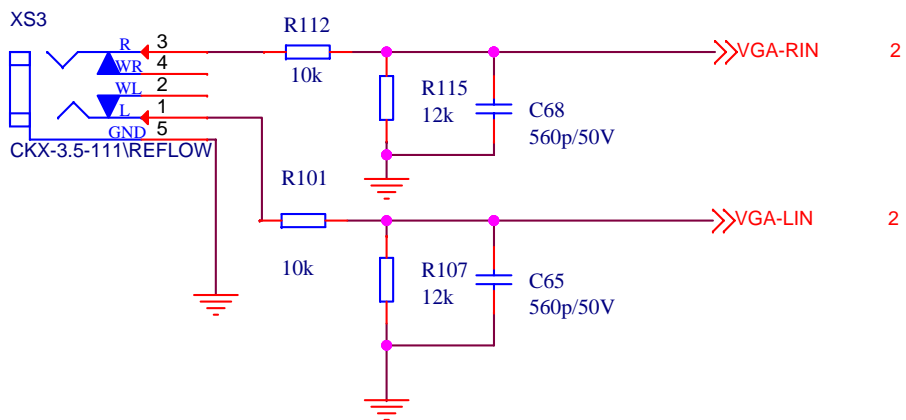
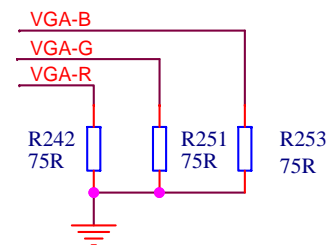
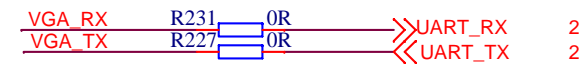
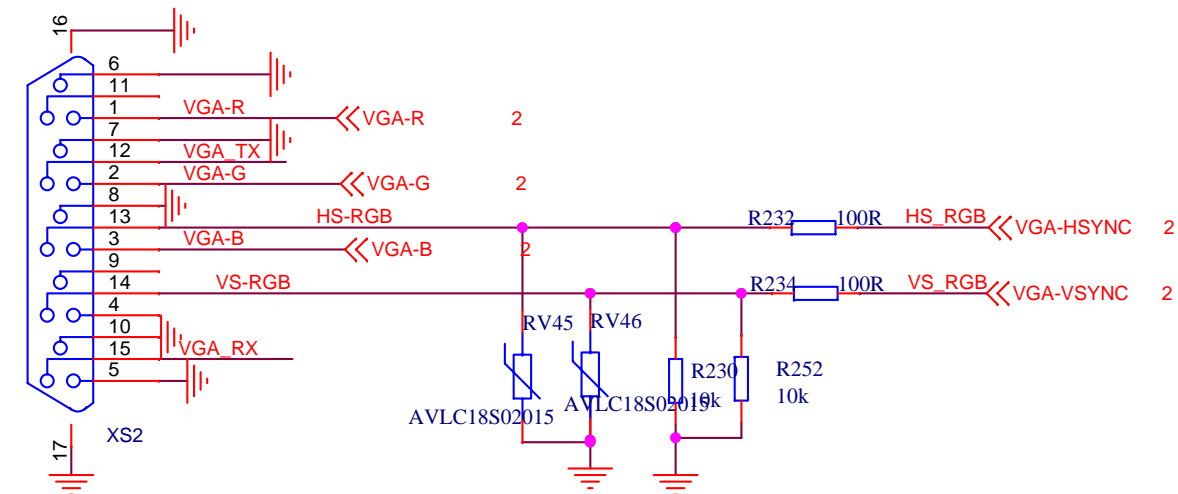
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Title Hisense MSD6308RT		
Size A	Schematic Name <Doc>	Rev 1.0
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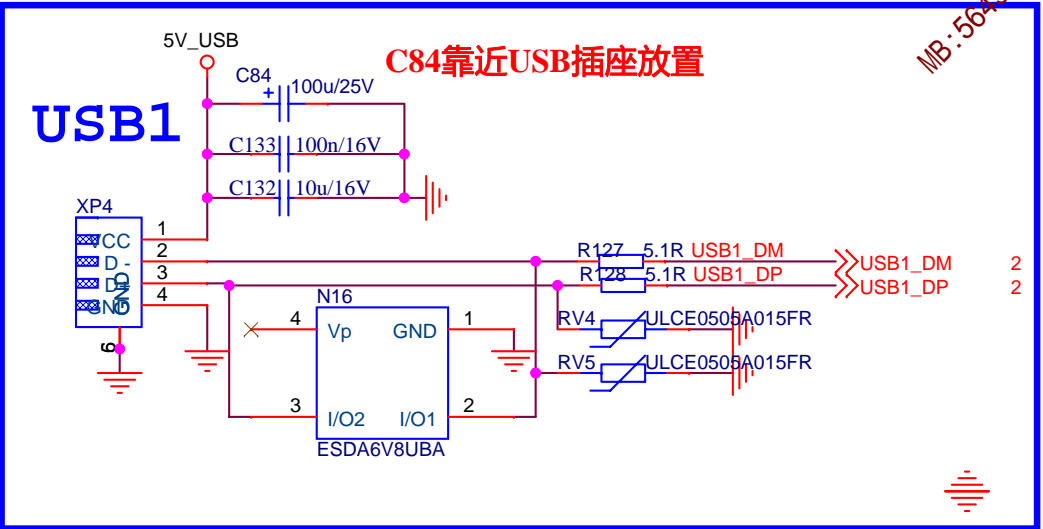
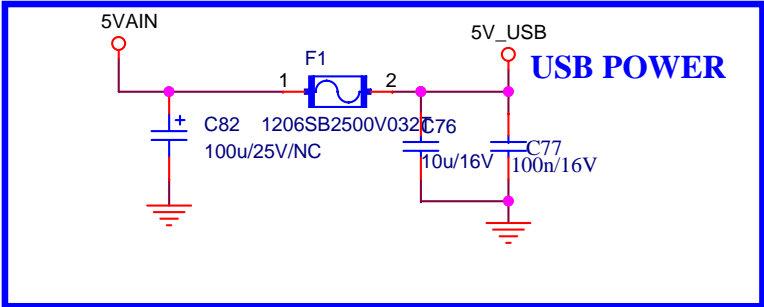
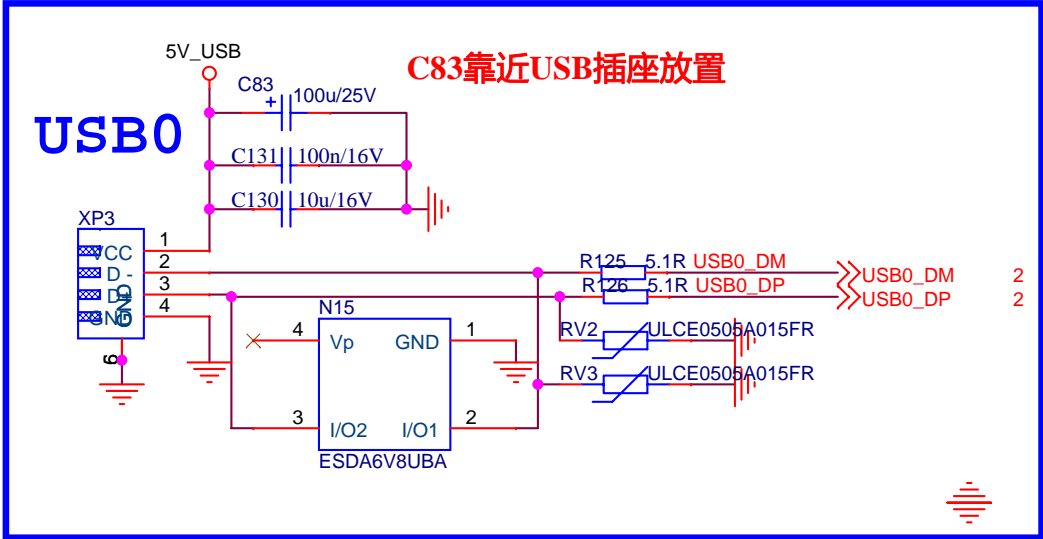
# VGA




MB:5645

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# USB INTERFACE



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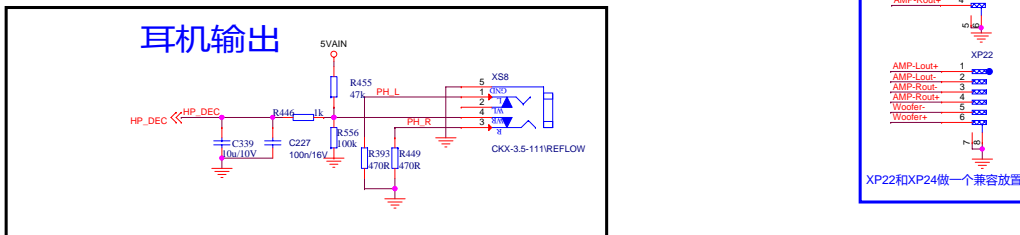
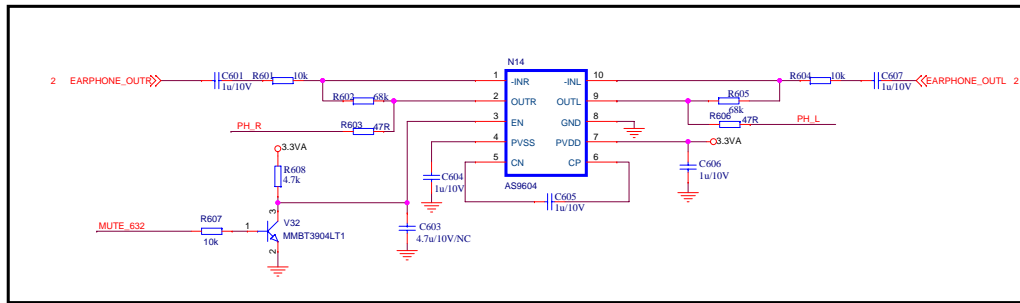
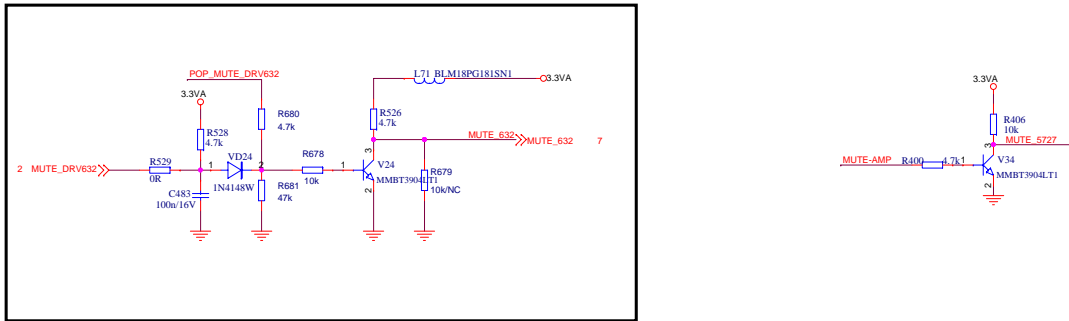
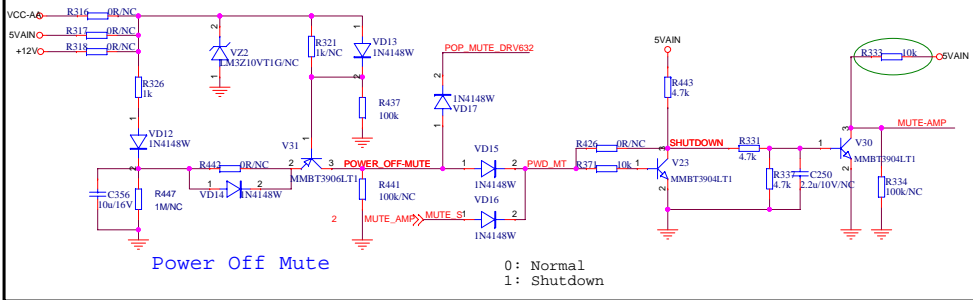
The diagram illustrates the PCB layout for the H3645 module, focusing on the placement of components near the IC. The top section shows the component footprints and their connections to the IC pins. The bottom section provides a detailed schematic of the H3645 IC, including its internal components and the placement of external components like resistors and capacitors. A large red watermark 'WB:5645' is overlaid on the diagram.

Diagram illustrating the HDML-ARC and CEC protocols. The HDML-ARC sequence is shown as HDML-ARC 0001 1 0 101 HDML-ARC, with a double arrow indicating the direction of transmission. The CEC sequence is shown as CEC 100 HDML-CEC, also with a double arrow indicating the direction of transmission. A red box highlights the '1' bit in the HDML-ARC sequence and the '100' sequence in the CEC sequence.

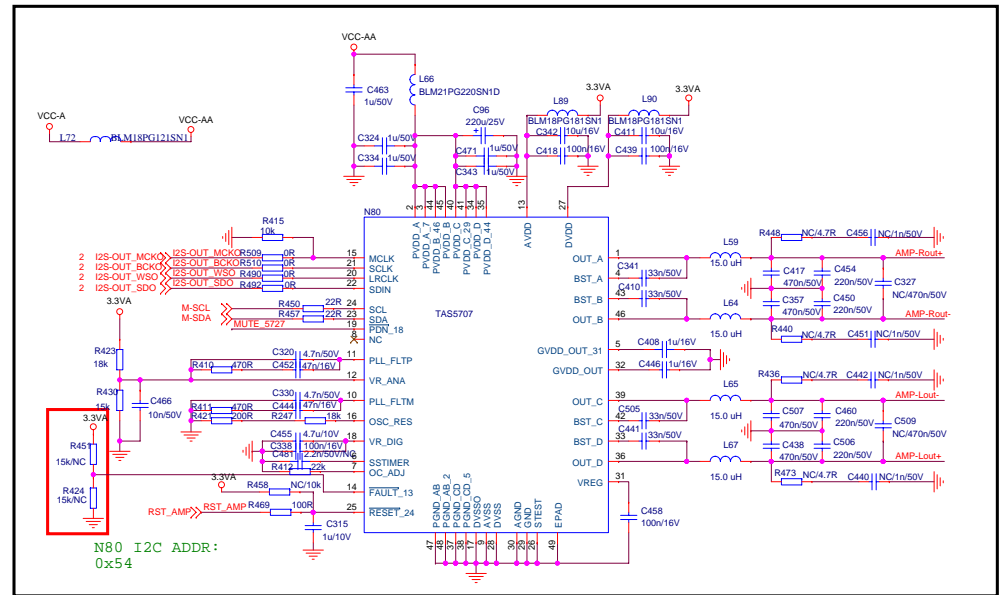
Schematic diagram of the MHL-CD-SENSE circuit. The circuit shows a voltage divider network connected to the MHL\_CD\_SENSE pin. The divider consists of a 300k resistor (R555) and a 47nF capacitor (C52) in parallel. The other end of the divider is connected to a 100k resistor (R549) which is tied to ground. The input signal is labeled HDM2-0V and AVDD05V\_MHL\_C. The output of the divider is connected to the MHL\_CD\_SENSE pin, which is also labeled MHL\_CABLE\_DET.

根据ARC所放的HDMI定义

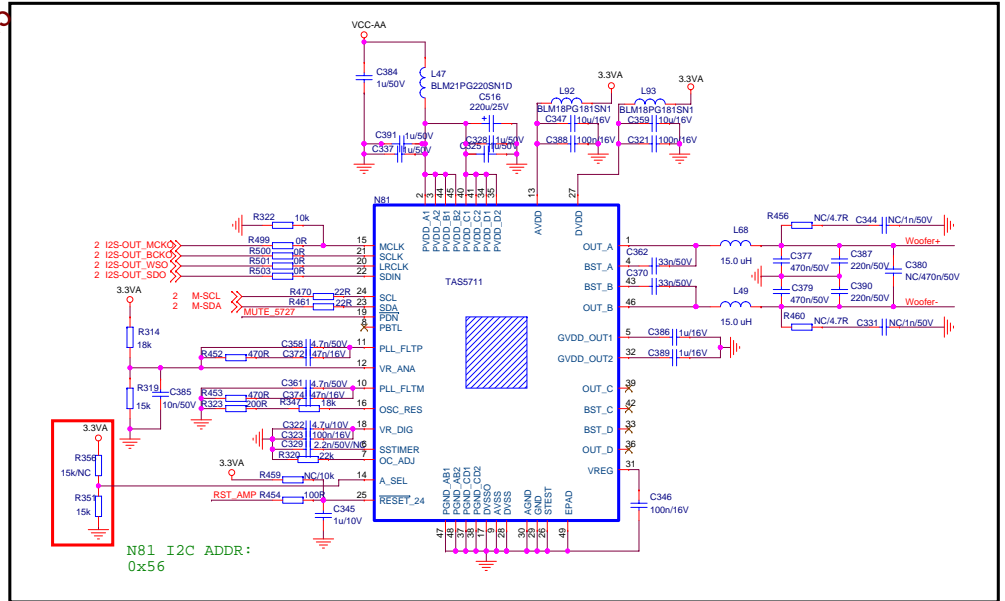
## MUTE



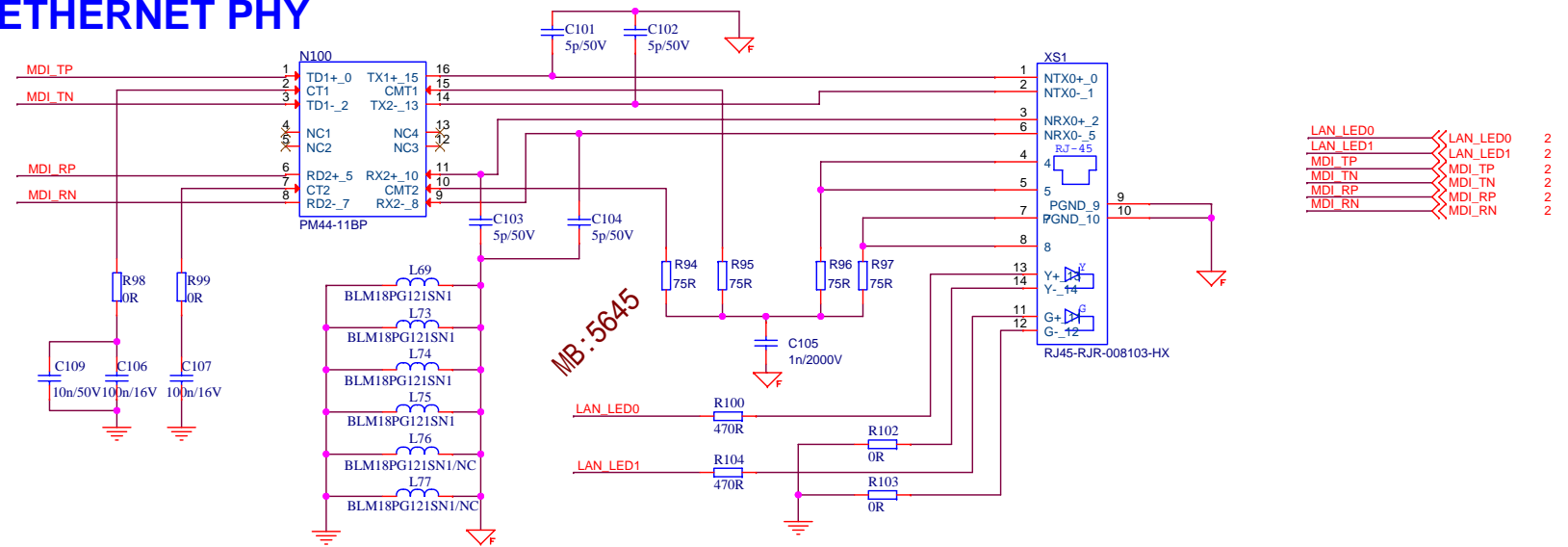
**SPEAKER AMP**



## WOOFER AMP



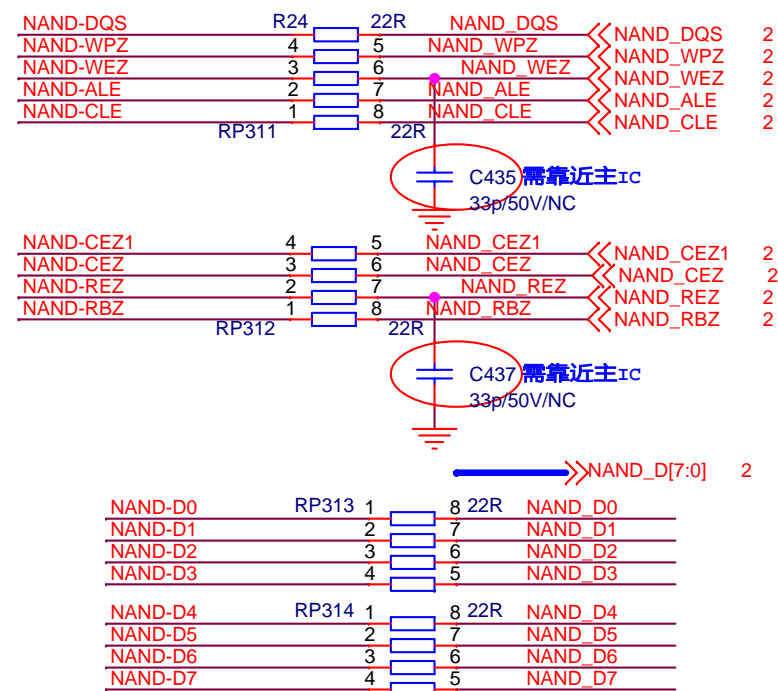
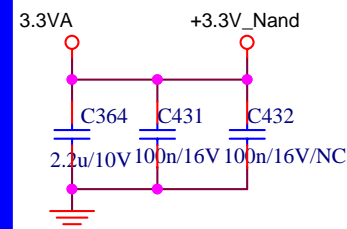
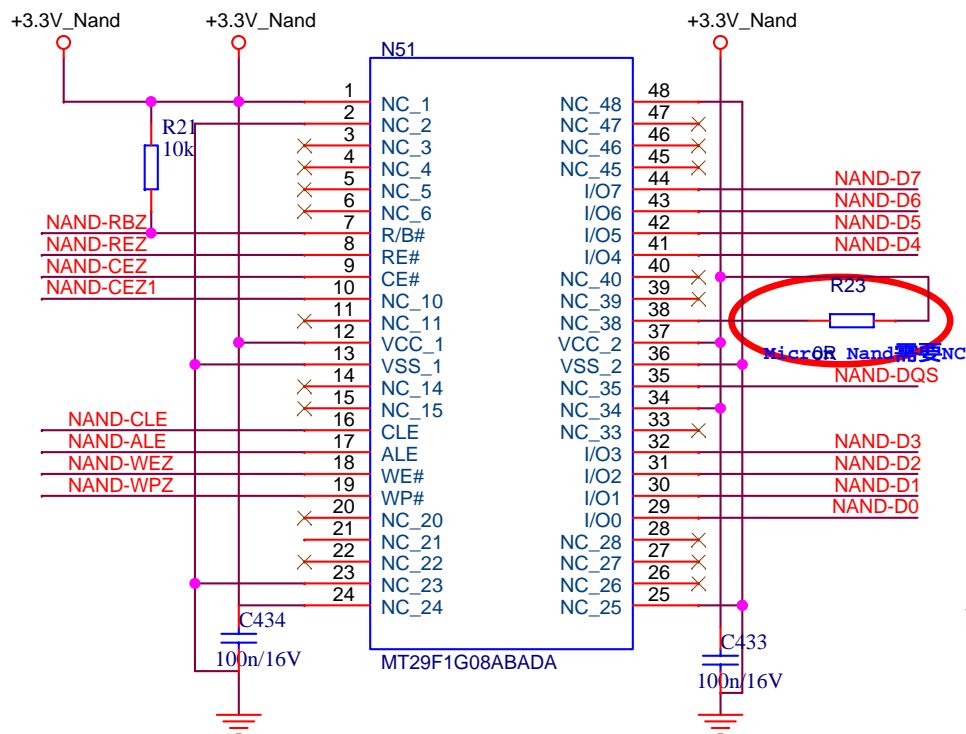
# ETHERNET PHY



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# NAND FLASH

# NAND Power



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Schematic Name  
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