

A	which are specified in OQA-2049	
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02_STANDBY / MAIN POWER

B5V_DC_PW



B3.3V

B1.8V



A3.3V

F

BLOCK NAME
high_xl4h_eu

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A

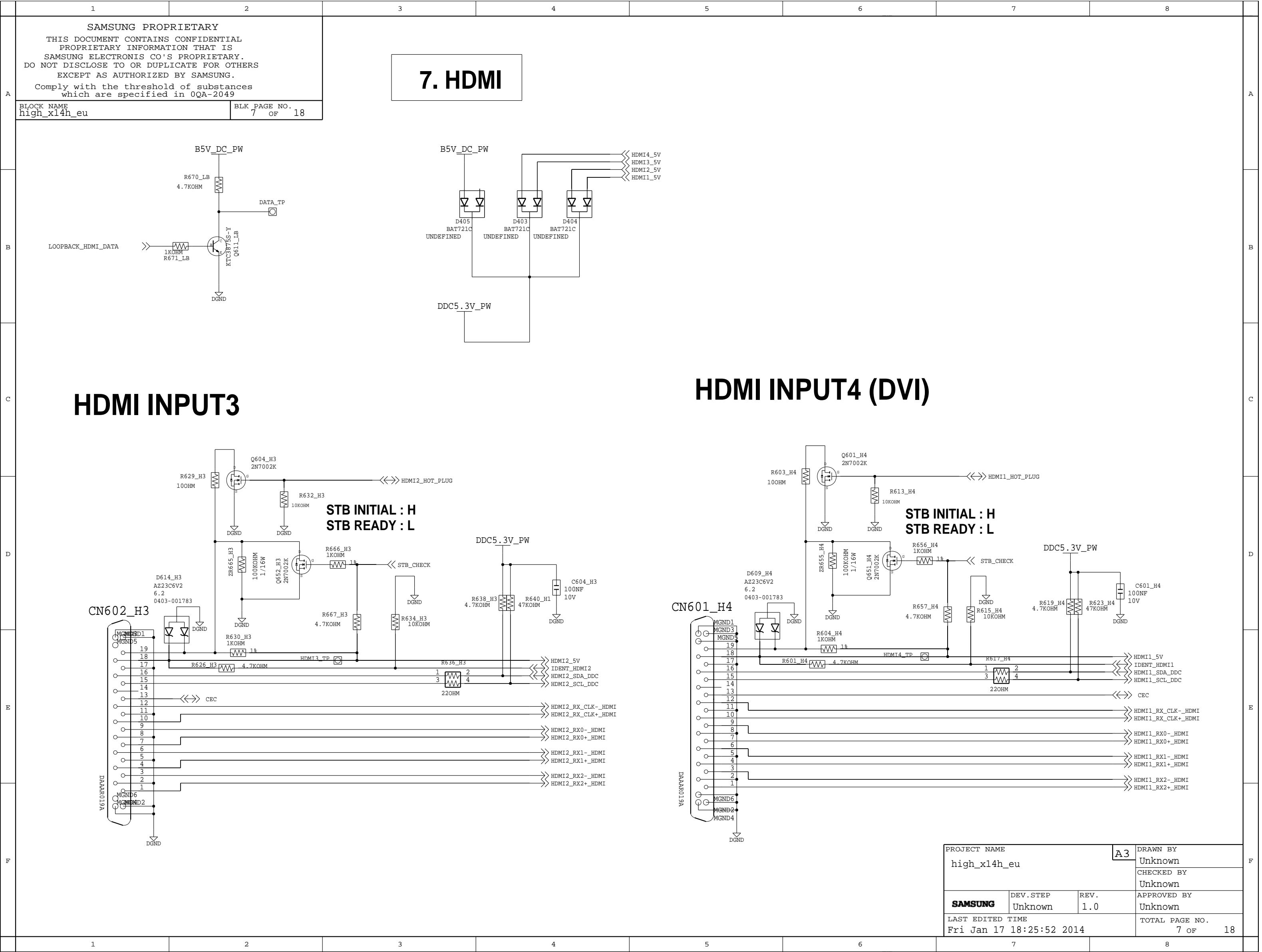
B

F

HDMI

HDMI1_RX0- _HDMI	>>	V3	RXA0N	RXC0N	J3	HDMI4_RX0- _HDMI
HDMI1_RX0+ _HDMI	>>	V2	RXA0P	RXC0P	J2	HDMI4_RX0+ _HDMI
HDMI1_RX1- _HDMI	>>	V1	RXA1N	RXC1N	J1	HDMI4_RX1- _HDMI
HDMI1_RX1+ _HDMI	>>	W3	RXA1P	RXC1P	K3	HDMI4_RX1+ _HDMI
HDMI1_RX2- _HDMI	>>	W1	RXA2N	RXC2N	K1	HDMI4_RX2- _HDMI
HDMI1_RX2+ _HDMI	>>	W2	RXA2P	RXC2P	K2	HDMI4_RX2+ _HDMI
HDMI1_RX_CLK- _HDMI	>>	U3	RXACEN	RXC0CN	H3	HDMI4_RX_CLK- _HDMI
HDMI1_RX_CLK+ _HDMI	>>	U2	RXACEP	RXC0CP	H2	HDMI4_RX_CLK+ _HDMI
<hr/>						
HDMI1_SCL_DDC >>		AB4	D0CDA_CK	D0CDC_CK	V6	HDMI4_SCL_DDC
HDMI1_SDA_DDC <<>>		AA6	D0CDA_DA	D0CCD_DA	W6	HDMI4_SDA_DDC
<hr/>						
HDMI1_HOT_PLUG <<		AC7	HOTPLUGA	HOTPLUGC	AC6	HDMI4_HOT_PLUG <<>>
<hr/>						
ARC1_SIGLE <<	C605_ARC 1UF	R641_ARC 00HM	ARC0	RXD0N	M3	HDMI3_RX0- _HDMI
HDMI2_RX0- _HDMI	>>	R3	RXB0N	RXD0P	M2	HDMI3_RX0+ _HDMI
HDMI2_RX0+ _HDMI	>>	R2	RXB0P	RXD1P	M1	HDMI3_RX1- _HDMI
HDMI2_RX1- _HDMI	>>	R1	RXB1N	RXD2P	N3	HDMI3_RX1+ _HDMI
HDMI2_RX1+ _HDMI	>>	T3	RXB1P	RXD2N	N1	HDMI3_RX2- _HDMI
HDMI2_RX2- _HDMI	>>	T1	RXB2N	RXD0CN	N2	HDMI3_RX2+ _HDMI
HDMI2_RX2+ _HDMI	>>	T2	RXB2P	RXD0CP	L3	HDMI3_RX_CLK- _HDMI
HDMI2_RX_CLK- _HDMI	>>	P3	RXC0CN		L2	HDMI3_RX_CLK+ _HDMI
HDMI2_RX_CLK+ _HDMI	>>	P2	RXC0CP	D0CDB_CK	Y5	HDMI3_SCL_DDC
<hr/>						
HDMI2_SCL_DDC >>		AA5	D0CDB_DA	D0CCD_DA	Y6	HDMI3_SDA_DDC
HDMI2_SDA_DDC <<>>		Y4	D0CDB_DA	HOTPLUGD	AD6	HDMI3_HOT_PLUG >>
<hr/>						
HDMI2_HOT_PLUG <<		AD7	HOTPLUGB			

[illegible]D:/atdm/projects/high x14h eu\high x14h eu.cpm



A

B

C

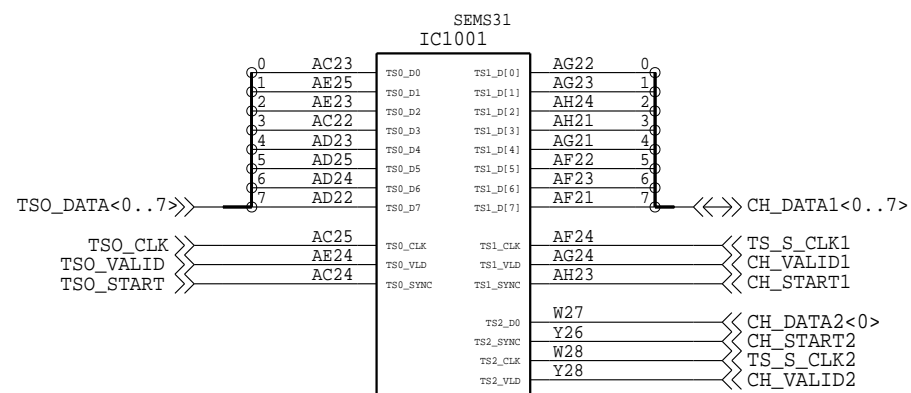
A

B

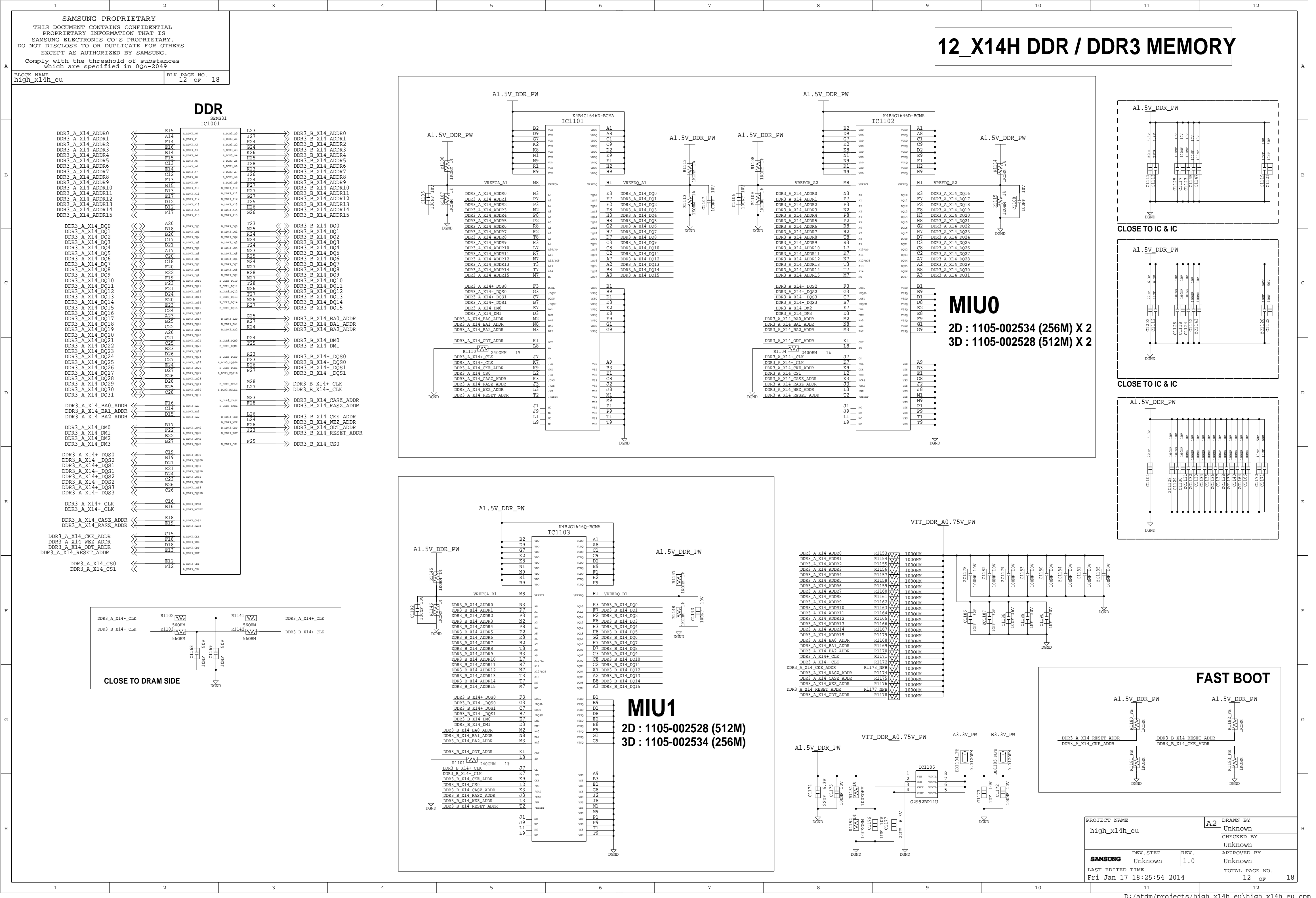
C



F



D:/atdm/projects/high_x14h_eu\high_x14h_eu.cpm

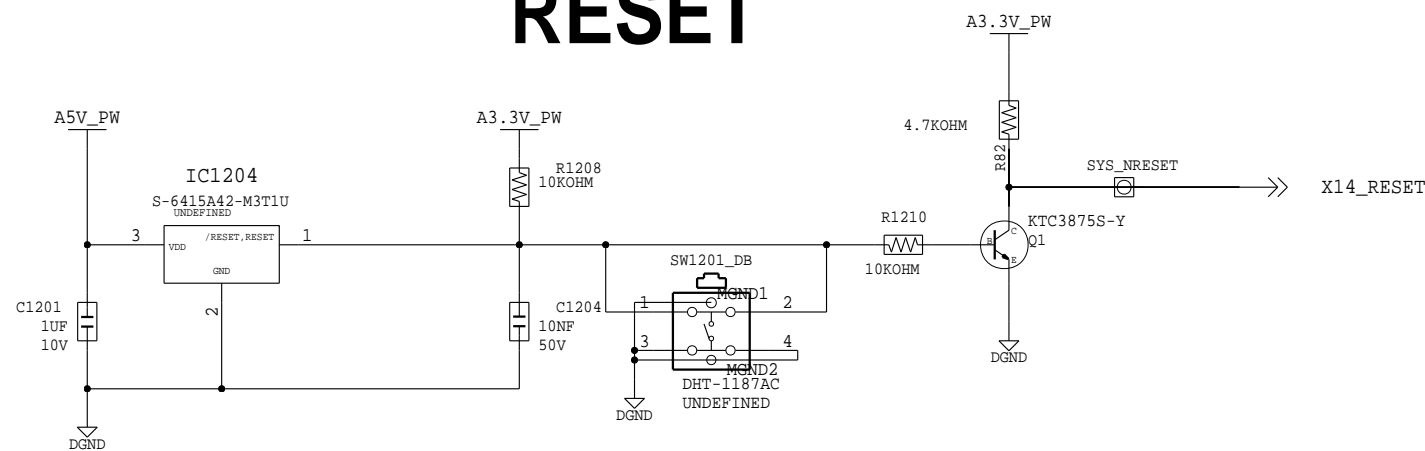


Comply with the threshold of substances
which are specified in OQA-2049

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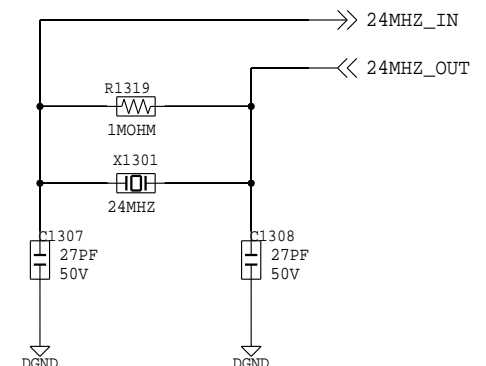
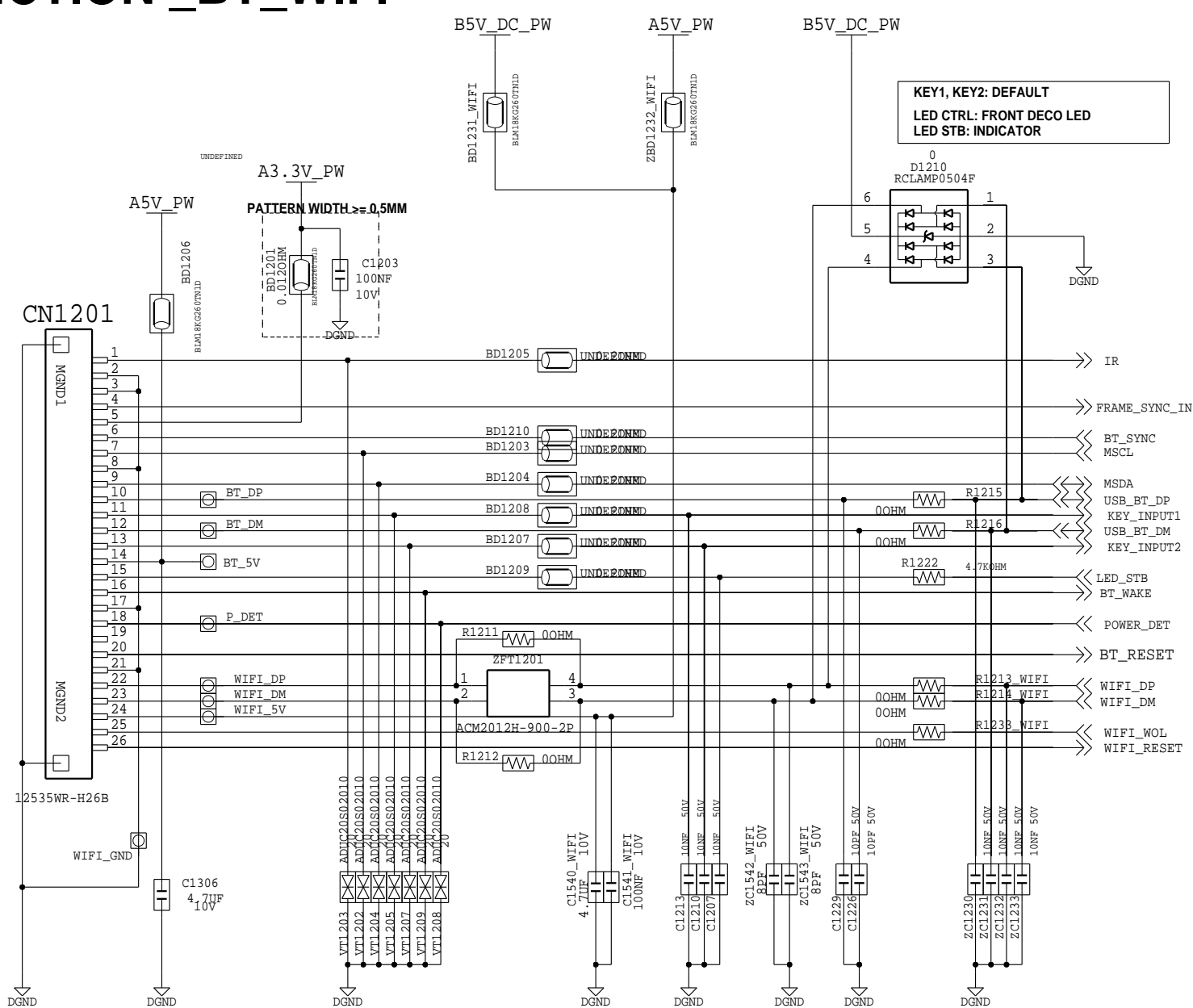
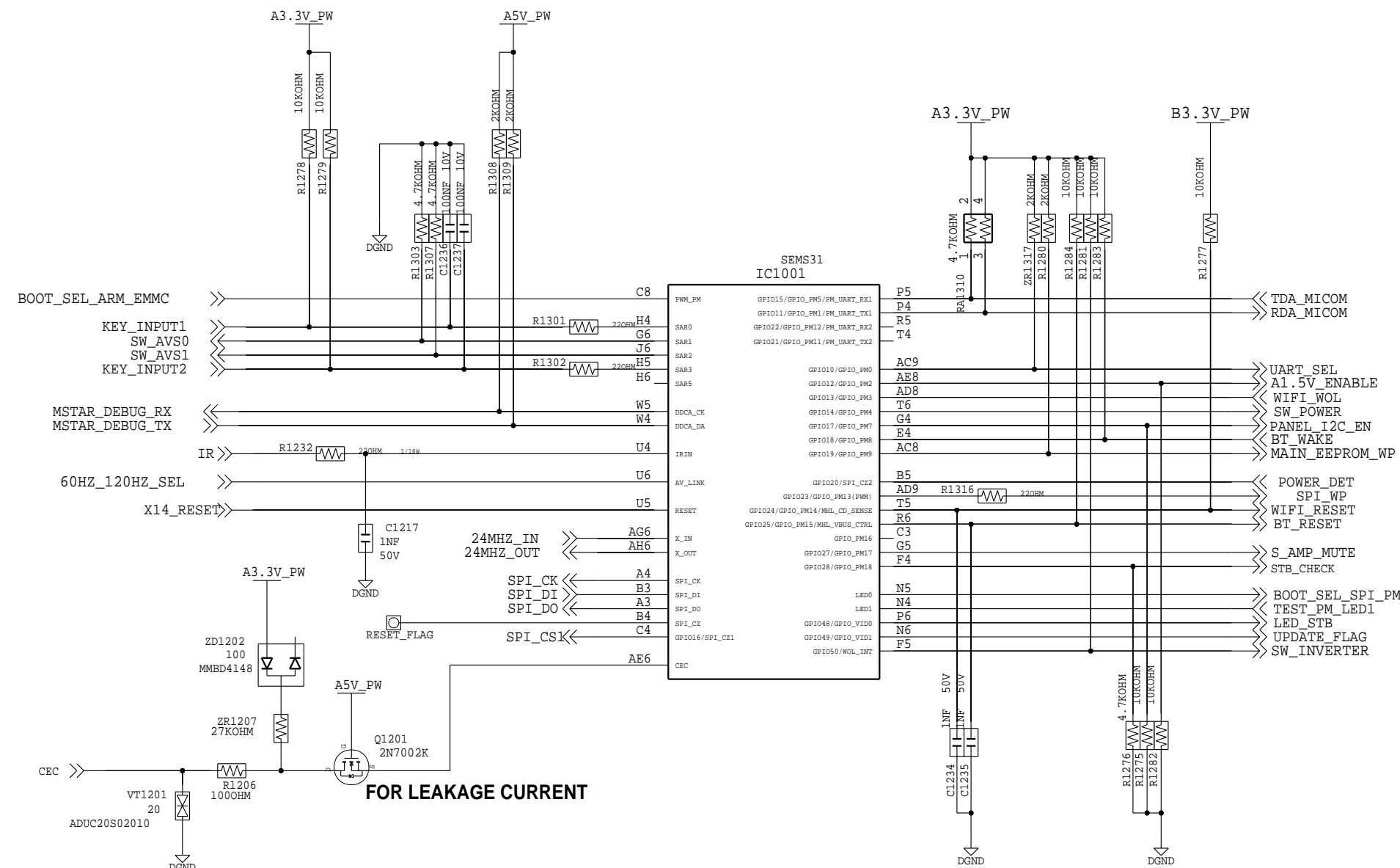
13_SUB MICOM FUNCTION / DEBUG PORT

RESET



POWER DET

FUNCTION_BT_WIFI



PROJECT NAME			A2	DRAWN BY	
high_x14h_eu				Unknown	
				CHECKED BY	
				Unknown	
SAMSUNG	DEV. STEP	REV.		APPROVED BY	
	Unknown	1.0		Unknown	
LAST EDITED TIME				TOTAL PAGE NO.	
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14_X14H CI / NAND / SPI FLASH

[illegible]

Schematic diagram of the SPI interface circuit for the W25Q40CLSSIP memory chip. The chip is connected to an A3.3V-PW supply. The VCC pin (8) is connected to the supply, and the GND pin (5) is connected to DGND. The CS pin (1) is connected to the SPI-CS signal. The DO pin (2) is connected to the SPI_DO signal, and the DI pin (3) is connected to the SPI_DI signal. The WP pin (4) is connected to the SPI_WP signal. The chip is also connected to a 220OHM resistor (R1306) in series with the SPI-CK signal. A 100NF capacitor (C1310) is connected between the VCC and GND pins. A 4.7KOHM resistor (R1320) is connected between the CS pin and GND.

PROJECT NAME			A3	DRAWN BY	
high_xl4h_eu				Unknown	
				CHECKED BY	
				Unknown	
SAMSUNG	DEV.STEP	REV.		APPROVED BY	
Unknown	Unknown	1.0		Unknown	
LAST EDITED TIME				TOTAL PAGE NO.	
Fri Jan 17 18:25:57 2014				14 OF 18	

A

B

F

USB1_HDD

